

(12) **United States Patent**
Ker et al.

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(54) **MIXED-VOLTAGE INPUT/OUTPUT BUFFER**

(56)

References Cited

(75) Inventors: **Ming-Dou Ker**, Hsinchu (TW);
Fang-Ling Hu, Jiaosi Township, Yilan
County (TW)

U.S. PATENT DOCUMENTS
6,320,414 B1 11/2001 Annema et al.
6,509,787 B1 * 1/2003 Kang 327/541

(73) Assignee: **National Chiao-Tung University**,
Hsinchu (TW)

OTHER PUBLICATIONS

(*) Notice: Subject to any disclaimer, the term of this
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U.S.C. 154(b) by 53 days.

Anne-Johan Annema, et al, 5.5V I/O in a 2.5-V 0.25- μ m CMOS
Technology, IEEE Journal, vol. 36 No. 3, Mar. 2001.

* cited by examiner

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Primary Examiner—An T Luu

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(74) *Attorney, Agent, or Firm*—Ming Chow Sinorica, LLC

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H03K 3/00 (2006.01)

(52) **U.S. Cl.** **327/108**; 327/112; 326/82;
326/85

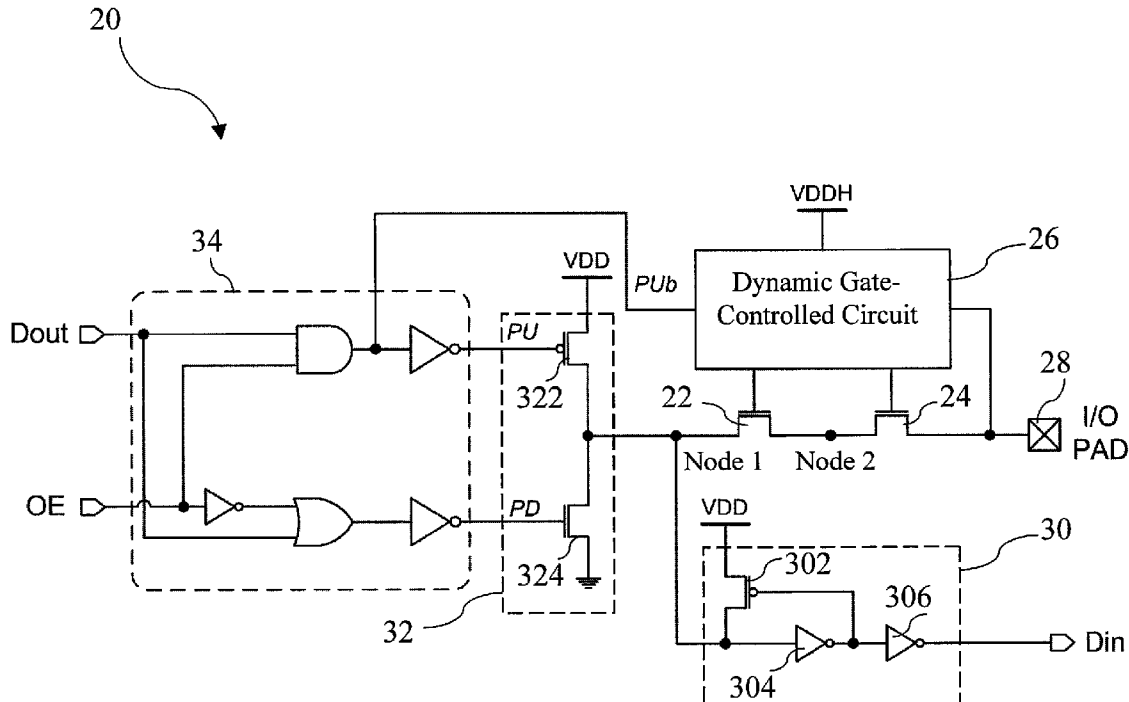
(58) **Field of Classification Search** 327/108–112;
329/82–87

See application file for complete search history.

ABSTRACT

A mixed-voltage I/O buffer comprises an input circuit, an output circuit, an I/O pad, a pre-driver circuit coupled to the output circuit, two added coupled N-type transistors, and a dynamical gate-controlled circuit coupled to each gate of the two N-type transistors and the pre-driver circuit; one of the N-type transistors is coupled to the input circuit and the output circuit; the other N-type transistor and the dynamic gate-controlled circuit are together coupled to the I/O pad. Thereby, a mixed-voltage I/O buffer which receives $2 \times V_{DD}$ -tolerant input signals and overcomes the hot-carrier degradation is realized.

12 Claims, 4 Drawing Sheets



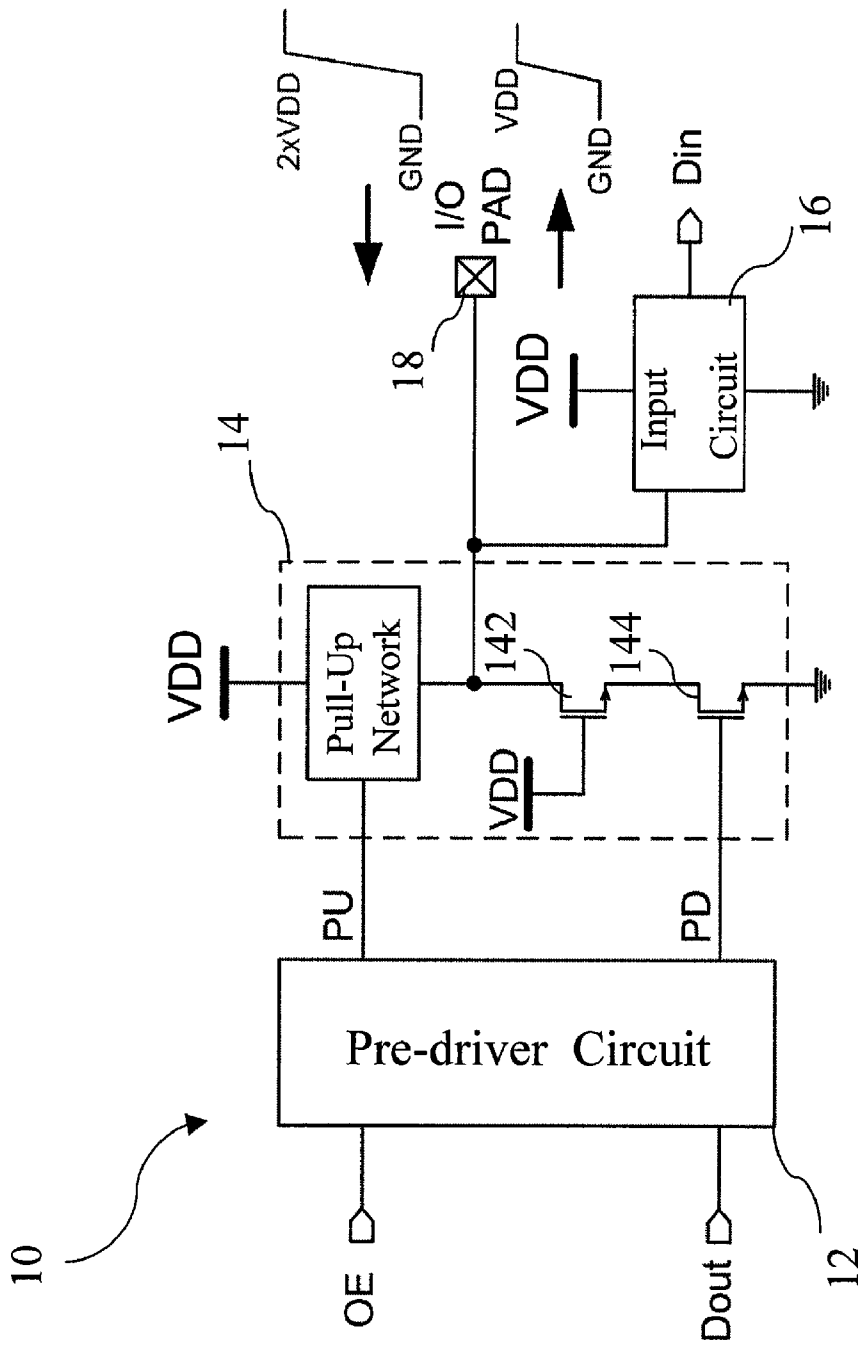


Fig. 1

(prior art)

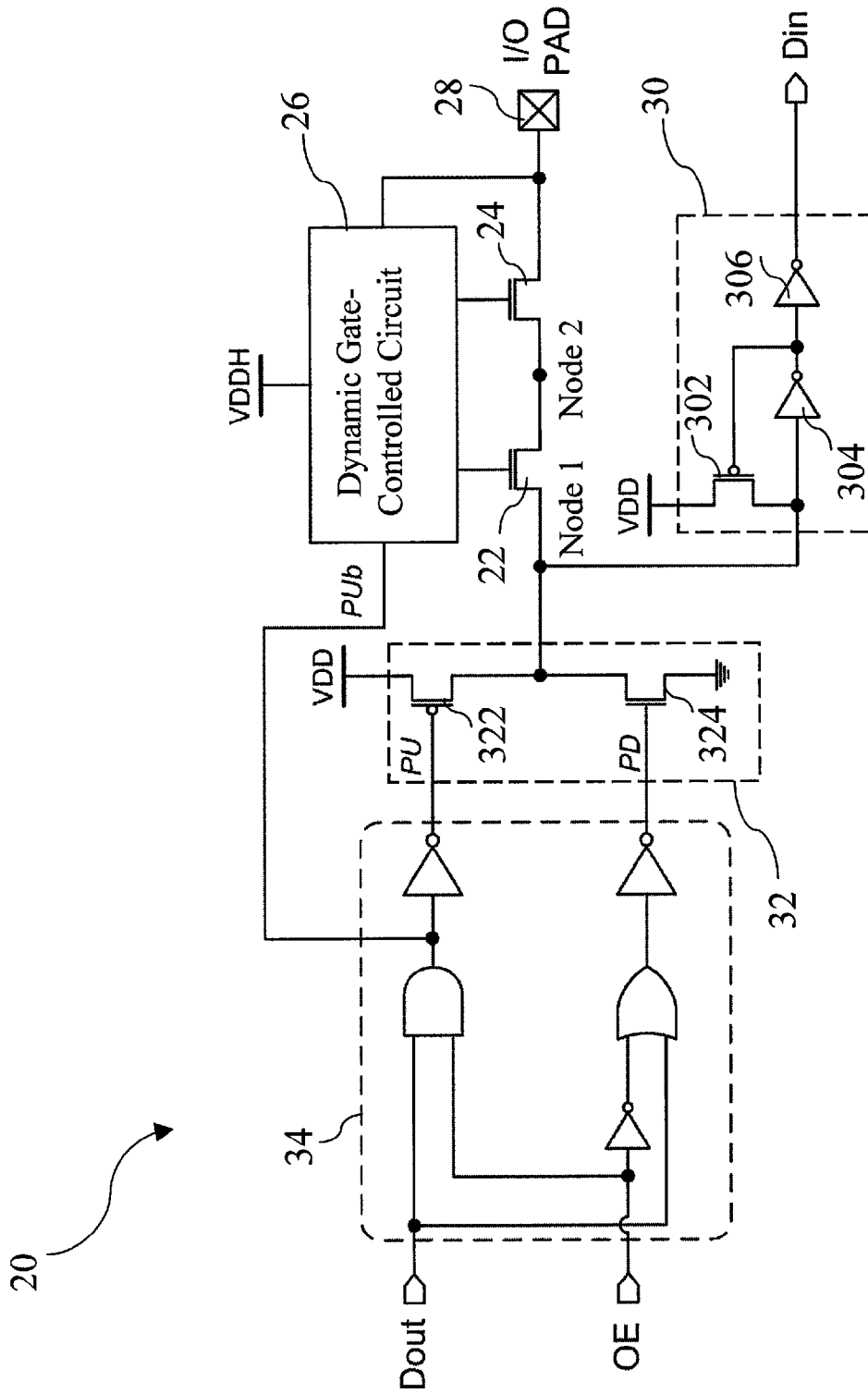


Fig. 2

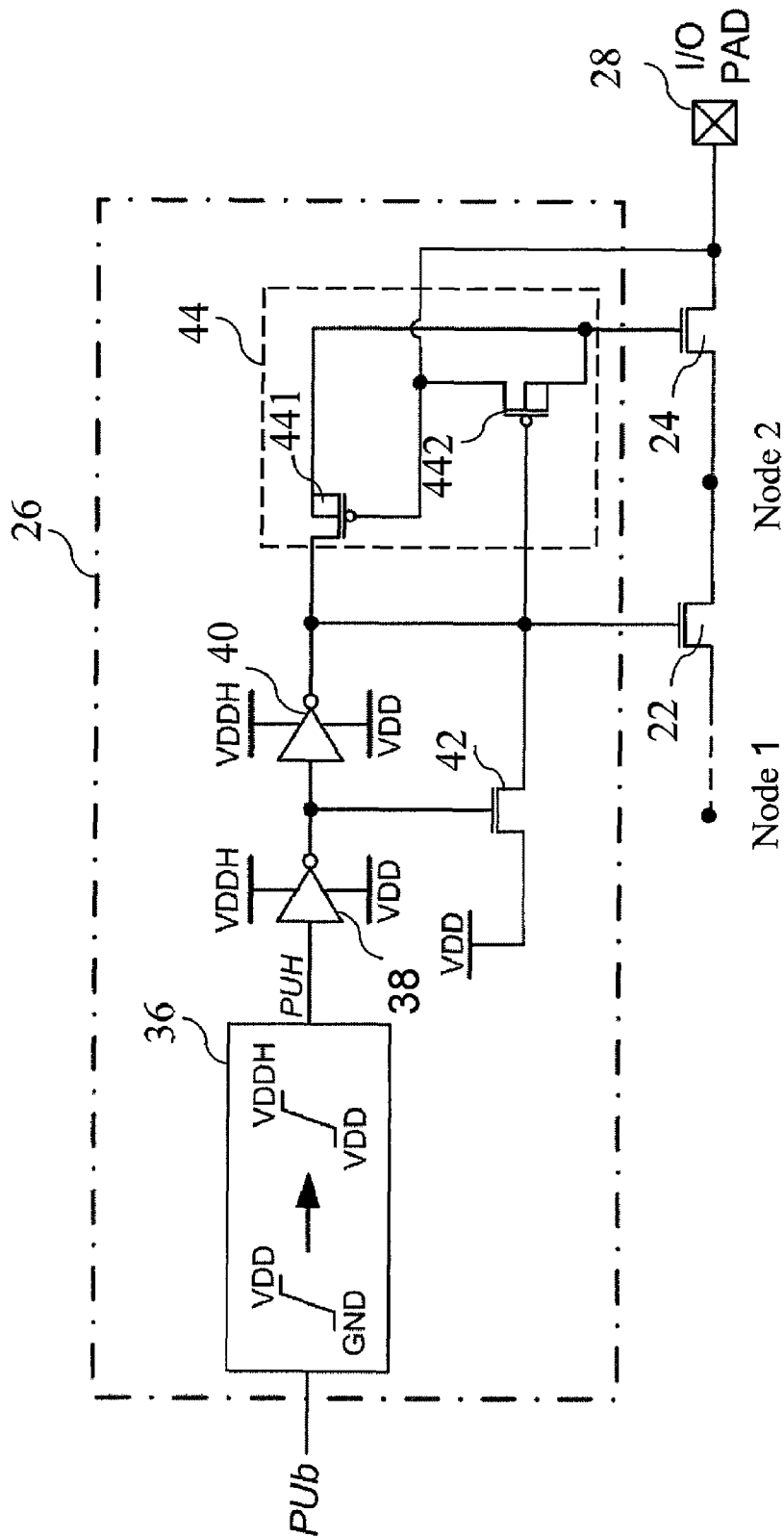


Fig. 3

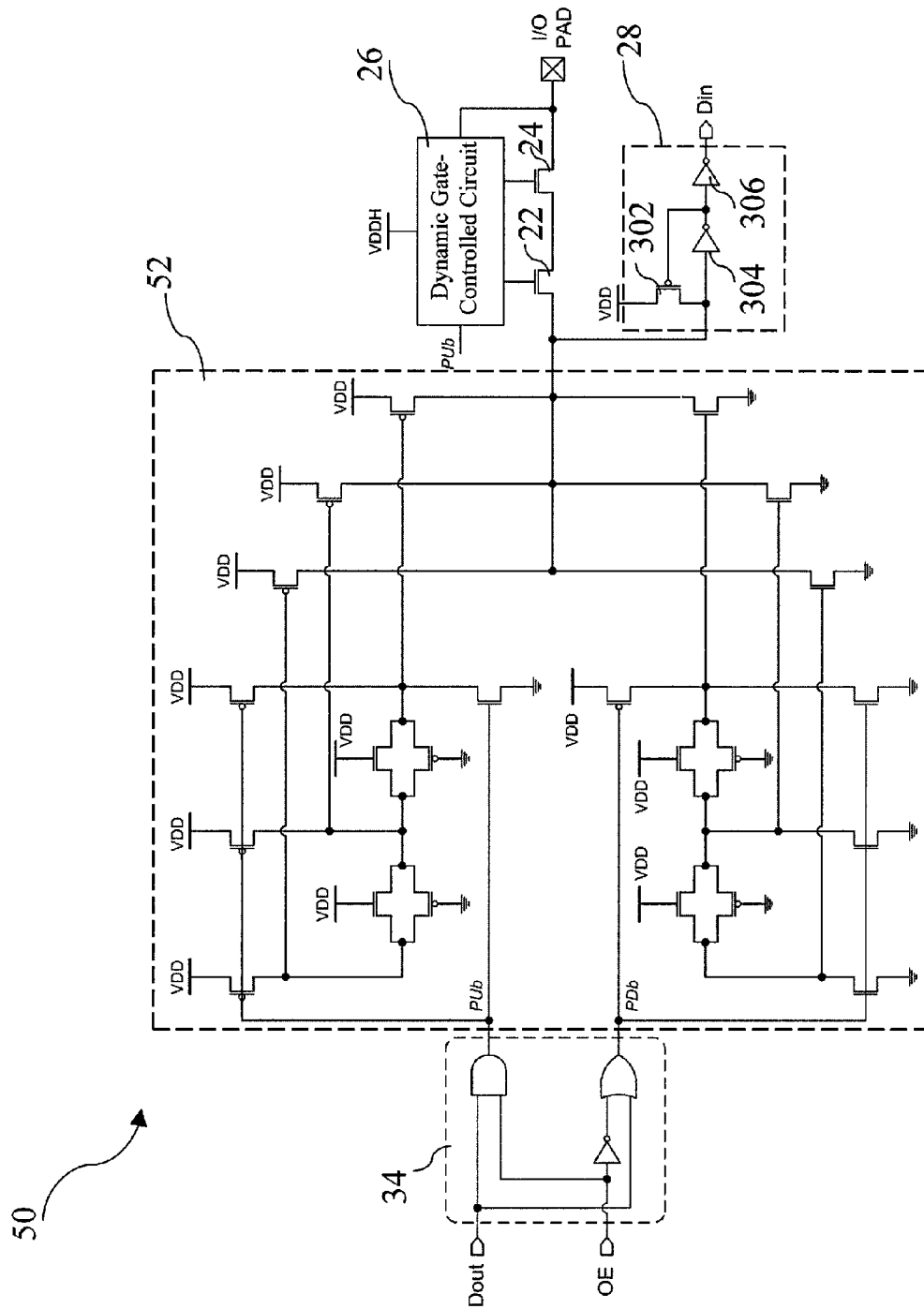


Fig. 4

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the receive mode, in the transmit mode or during the transition from receiving a $2 \times V_{DD}$ input signal to transmitting a 0V output signal, via two NMOS transistors and a dynamic gate-controlled circuit, the mixed-voltage I/O buffer of the present invention is free from the problems of gate-oxide reliability, current leakage and hot-carrier degradation. Further, the present invention incorporates a voltage slew-rate control output circuit in the mixed-voltage I/O buffer to realize a mixed-voltage I/O buffer with a voltage slew-rate control function.

Those described above are the embodiments to clarify the characteristics and technical thought of the present invention to enable the persons skilled in the art to understand, make and use the present invention. However, it is not intended to limit the scope of the present invention. Any equivalent modification or variation according to the spirit of the present invention is to be also included within the scope of the present invention.

What is claimed is:

1. A mixed-voltage input/output buffer, comprising:
 - a first N-type transistor coupled to an input circuit;
 - a second N-type transistor coupled to said first N-type transistor and an input/output pad;
 - a dynamic gate-controlled circuit externally connected to a high-level voltage and coupled to said input/output pad, a gate of said first N-type transistor and a gate of said second N-type transistor;
 - an output circuit externally connected to a low-level voltage and coupled to said first N-type transistor and said input circuit, wherein said output circuit is a voltage slew-rate control output circuit; and
 - a pre-driver circuit coupled to said output circuit and said dynamic gate-controlled circuit and controlling a voltage of said output circuit according to an output-enable signal and input data.
2. The mixed-voltage input/output buffer according to claim 1, wherein said dynamic gate-controlled circuit further comprises:
 - a level shifter coupled to said pre-driver circuit and receiving a voltage signal sent out by said pre-driver circuit and pulling up a level of said voltage signal;
 - a first inverter, wherein one end of said first inverter is coupled to said level shifter, and an other end is coupled to a second inverter and a gate of a third N-type transistor; and
 - a gate-tracking circuit coupled to said second inverter, said third N-type transistor, said gate of said first N-type transistor, said gate of said second N-type transistor and said input/output pad.
3. The mixed-voltage input/output buffer according to claim 2, wherein said gate-tracking circuit further comprises two first P-type transistors, which are coupled to each other.
4. The mixed-voltage input/output buffer according to claim 1, wherein said output circuit further comprises a pull-up P-type transistor and a pull-down N-type transistor.
5. The mixed-voltage input/output buffer according to claim 1, wherein said voltage slew-rate control output circuit

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further comprises a plurality of parallel pull-up P-type transistors and a plurality of parallel pull-down N-type transistors.

6. The mixed-voltage input/output buffer according to claim 1, wherein when said output-enable signal is high, said input/output buffer transmits an output signal from an output end of said pre-driver circuit transmits to said input/output pad.
7. The mixed-voltage input/output buffer according to claim 1, wherein said input circuit further comprises:
 - a second P-type transistor coupled to said output circuit and said first N-type transistor;
 - a third inverter coupled to said second P-type transistor, said output circuit and said first N-type transistor; and
 - a fourth inverter coupled to said second P-type transistor and said third inverter.
8. The mixed-voltage input/output buffer according to claim 1, wherein when said output-enable signal is low, said input/output buffer transmits said input signal from said input/output pad to an input end of said input circuit, and said pre-driver circuit turns off said output circuit, and said gate of said first N-type transistor maintains biased at said low-level voltage, and said gate of said second N-type transistor varies with a voltage of said input/output pad.
9. The mixed-voltage input/output buffer according to claim 8, wherein when said input signal received by said input/output buffer is at 0V voltage, said gate of said second N-type transistor is biased at said low-level voltage to enable said input/output pad to transmit a 0V input signal to said input circuit.
10. The mixed-voltage input/output buffer according to claim 8, wherein when said input signal received by said input/output buffer is at said high-level voltage, said gate of said second N-type transistor is biased at double said low-level voltage to enable said input/output pad to transmit an input signal of said low-level voltage to said input circuit via said first and second N-type transistors.
11. The mixed-voltage input/output buffer according to claim 6, wherein when said output signal transmitted by the output end of said pre-driver circuit is at said low-level voltage, said pre-driver circuit turns on a pull-up P-type transistor of said output circuit and turns off a pull-down N-type transistor of said output circuit, and said gate of said first N-type transistor and said gate of said second N-type transistor are biased at double said low-level voltage to enable the output end of said pre-driver circuit to transmit an output signal of said low-level voltage to said input/output pad.
12. The mixed-voltage input/output buffer according to claim 6, wherein when said output signal transmitted by the output end of said pre-driver circuit is at 0V, said pre-driver circuit turns off a pull-up P-type transistor of said output circuit and turns on a pull-down N-type transistor of said output circuit, and said gate of said first N-type transistor and said gate of said second N-type transistor are biased at said low-level voltage to enable the output end of said pre-driver circuit to transmit a 0V output signal to said input/output pad.

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