國立交通大學

電子工程學系電子研究所

博士論文

基體觸發技術與積體電路晶片上之靜電放電防護電路設計

SUBSTRATE-TRIGGERED TECHNIQUE FOR ON-CHIP ESD PROTECTION DESIGN IN DEEP-SUBMICRON CMOS INTEGRATED CIRCUITS

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摘要

本論文提出基體觸發技術在靜電放電下啟動的物理機制，並將其應用在深次微米互補式金氧半積體電路(deep-submicron CMOS IC)的靜電放電防護設計上，因應積體電路中不同的需求，而設計出各種靜電放電防護電路，以避免積體電路受到靜電放電的破壞。由於在先進的製程中，半導體元件的接面崩潰(Junction Breakdown)電壓越來越接近閘極氧化層(Gate Oxide)的崩潰電壓，在靜電放電(ElectroStatic Discharge, ESD)防護的設計上，傳統的設計方法已越來越加困難。閘極驅動(Gate Driven)技術以及基體觸發(Substrate Triggered)技術都是為了提昇靜電放電防護元件在靜電放電衝擊時的反應放率及防護能力，所發展出的最新技術。但是在進入深次微米的製程時，閘極驅動技術也越來越難以設計及控制，從本論文的研究中證實基體觸發技術對於靜電放電防護的設計是一個最佳最有效的方法。

首先，從靜電放電防護基本元件在遭到靜電放電衝擊下啟動的基本原理為起點，實際在 0.35 微米製程中，以變化不同的佈局參數，來改變指狀結構(Finger type)靜電放電防護基本元件的佈局結構，以靜電放電實驗及二次崩潰點(Secondary Breakdown)的量測來說明元件結構對靜電放電耐受力的影響，並由靜電放電防的測試結果中，求得最佳佈局方式，再從靜電放電防護元件之能帶圖(Energy Band Diagram)變化與觀察其在發射顯微鏡(EMission MIcroscope, EMMI)下的啟動變化分析，更進而說明元件在受到靜電放電衝擊下的啟動原理，並做一詳盡的物理定性分析，進而了解佈局參數對靜電放電防護能力影響的物理因素。從了解基本元件在遭到靜電放電衝擊下啟動的基本原理後，進一步分析閘極驅動技術及基體觸發技術的動作原理以及其對靜電放電防護的特性。由利用實驗設計的技巧，觀察其在發射顯微鏡下受到閘極驅動及基體觸發的啟動變化，並借由靜電放電防護

元件之能帶圖的變化進行比對分析，再以靜電放電實驗及二次崩潰點的量測分析，分別在0.18及0.35微米互補式金氧半製程中，用相同的實驗設計，均證實閘極驅動技術在高驅動電壓下，會對元件的靜電放電能力造成不良之影響，而對基體觸發技術而言，高觸發電流對元件的靜電放電能力卻有正面的影響。因此從閘極驅動技術及基體觸發技術不同的啟動機制實驗分析，得到基體觸發技術確實更能適用在深次微米的互補式金氧半積體電路中。

在積體電路中需要有全面性靜電放電防護設計(Full ESD Protection Design)的觀點是越來越重要，對於先進的積體電路，無論在輸入、輸出極甚至電源間皆必需有完整的靜電放電防護設計，在本論文中，將基體觸發技術實際應用在0.18微米互補式金氧半製程中，發展出一套基體觸發靜電放電防護電路，分別應用在輸入、輸出極以及電源VDD與VSS間，同時也在相同的製程中，製作傳統的靜電放電防護電路以做為比較。從人體模式(Human Body Model, HBM)的靜電放電測試中發現，在本製程中對靜電放電防護能力原本相當不理想的輸出極(W/L = 300μm/0.3μm)，在加入基體觸發技術的輸出保護電路後，可從原來0.65 kV的靜電放電耐受力增加到3.2 kV，證實了基體觸發技術的實用性。此外，在先進的深次微米製程中，由於元件的結構等比例地縮小，因此使用的電源電壓也必需從傳統的5伏特降下到3.3伏特甚至是1.8伏特，因此電子系統也必需混合5伏特及3.3伏特的電源電壓，例如一個3.3伏特電壓源的積體電路之輸入端，就可能必需接到一個5伏特的輸入訊號，因此在此種輸入端的靜電放電防護設計，就必需有特殊的考量。在本論文中，提供了一種新式且不需額外加遮蔽金屬矽化物的光罩(Salicide Blocking Mask)及專為靜電放電防護佈植(ESD implantation)的輸入極靜電放電防護電路，應用在這種混合電壓之電路的輸入極當靜電放電保護電路。在適當的佈局下，整個電路可以整合在一個單一的矽元件結構中，以加強其基體觸發的能力。在本論文中，此種設計也實際在0.25微米互補式金氧半的製程中製作出來，其中150微米總寬度的此種新式元件，在人體模式的靜電放電測試下，可以有效改善沒有基體觸發之基本元件的靜電放電耐受能力，在單位面積的比較下，實驗結果顯示其靜電放電耐受能力可以從原來的1.2 V/μm^{2}增加到1.73 V/μm^2。

而在電源間的靜電放電箝制電路方面，本論文除了在0.18微米製程中所設計的基體觸發電路外，本論文還在0.6微米互補式金氧半製程中提出四種新式的基體觸發靜電放電箝制元件，而為了使靜電放電電流能夠更均勻，這些靜電放電箝制元件被設計成多單元的四方形結構，並將其設計應用在靜電放電箝制電路中。這些靜電放電箝制元件是直接利用到互補式金氧半元件中具有寄生雙載子電晶體的特性，而將基體觸發的原理應用在這些元件上，使其在靜電放電時能夠迅速而均勻地開啟。這些元件包含了：基

體觸發水平雙載子電晶體(STLB)，基體觸發垂直雙載子電晶體(STVB)，基體觸發雙雙載子電晶體(STDB)，以及雙極觸發雙雙載子電晶體(DTDB)。在電路的設計方面，一種以電阻-電容為基礎的靜電放電偵測電路被用來做為主要的電路，以產生觸發電流來快速而有效地驅動這些靜電放電箝制元件。由靜電放電測試實驗結果顯示，具有基體觸發雙雙載子電晶體(STDB)的基體觸發之源極間的靜電放電箝制電路，可以比傳統閘極驅動之靜電放電箝制電路在同樣的箝制元件面積下改善 200%。

由於在類比電路中，積體電路的輸入電容不可太大，而且必需對輸入訊號的變化能有一穩定值，但為承受理想的靜電放電耐受能力，靜電放電防護元件通常具有較大的接面電容值，而且對電壓的變化又相當敏感。因此，在對元件啟動的特性了解後，本論文亦提出在類比電路中設計靜電放電防護電路的解決方案。由此設計理念，在 0.35 微米金氧半製程中，可以設計出 50 微米/0.5 微米大小的輸入/輸出極，使得整個輸入電容降到只有 ~0.4pF，而在人體模式及機械模式(Machine Model)的靜電放電防護測試下分別可以得到 6 kV 及 400 V 的靜電放電耐受力。在本論文中，更對此設計方式做一深入的探討，而提出一整套完整的設計方法來運用在所有類比電路的輸入/輸出設計中，使得輸入電容在隨 1 V 工作電壓變化範圍下能控制在 1%的誤差內。

此外，由於二極體可以在積體電路的靜電放電防護之設計上廣泛應用，但由於傳統二極體在積體電路中會形成寄生的雙載子電晶體，因此在實際應用時會有難以控制的漏電電流的產生，在本論文中也首先提出利用複晶矽二極體(Polysilicon Diode)應用到積體電路的靜電放電防護設計上，由此可以設計出全面性的靜電放電防護電路，而利用堆疊的複晶矽二極體當靜電放電控制電路的方法，也設計出一個在設計電路時可以有效控制漏電電流的電源間靜電放電箝制電路。在本論文中，對複晶矽二極體的雜質摻雜濃度以及一些佈局參數的變化對其特性及靜電放電耐受能力的影響，也做了詳細的分析。此外，利用堆疊的複晶矽二極體亦可設計出一種新式具有低漏電電流的電源間靜電放電箝制電路，此種電路在整個積體電路設計之初，即可事先模擬及安排，有效控制其在電源間的漏電電流。本論文將這些元件及電路實際應用到智慧卡(Smart Card)中，由整體的靜電放電防護設計下，可以成功地將原來只有 300 V 之人體模式靜電放電耐受力的產品，改善到大於 3 kV。

SUBSTRATE-TRIGGERED TECHNIQUE FOR ON-CHIP ESD PROTECTION DESIGN IN DEEP-SUBMICRON CMOS INTEGRATED CIRCUITS

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ABSTRACT

This thesis includes physical analysis for the turn-on mechanisms of ESD protection devices during ESD stress and the applications of on-chip substrate-triggered ESD protection design. Gate-driven and substrate-triggered technologies are used to improve the turn-on efficiency of ESD (ElectroStatic Discharge) protection devices. From the analysis of the turn-on mechanisms of ESD protection device with gate-driven and substrate-triggered design in this thesis, it is proved that the substrate-triggered ESD protection design can continually improve the ESD robustness of protection devices in deep-submicron CMOS process. But, the gate-driven design has been confirmed to cause a sudden degradation on ESD robustness of the ESD protection devices. By using the substrate-triggered technique, the input, output, and power-rail ESD protection circuits are developed to enhance the ESD robustness of integrated circuits in deep-submicron CMOS process.

To understand the turn-on mechanisms of ESD protection device during ESD stress, the turn-on characteristics of those devices must be measured and analyzed. The energy band diagrams, EMMI (EMission MIcroscope) photographs, and TLP (Transmission Line Pulsing) measurement have been used to analyze and explain the physical turn-on mechanisms of ESD protection device. From the investigation of layout dependence on ESD robustness of NMOS and PMOS with finger-type layout, the turn-on mechanisms of ESD protection devices can be

clearly understood to optimize the layout rules for the device dimensions, layout spacings, and clearances of those devices. To design high performance ESD protection device, some layout parameters must be optimized. The optimized layout parameters for a 0.35-μm CMOS process have been clearly investigated and analyzed in this thesis. To improve the ESD robustness of protection devices, gate-driven and substrate-triggered techniques have been developed. The gate-driven effect and substrate-triggered effect on ESD robustness of CMOS devices are also measured and compared in this thesis. The operation principles of gate-driven design and substrate-triggered design for ESD protection can be explained clearly by energy band diagrams and EMMI photographs. The experimental results have confirmed that the substrate-triggered design can effectively and continually improve ESD robustness of CMOS devices than the gate-driven design. But, the gate-driven design cannot continually improve ESD level of the device in the same deep-submicron CMOS process.

Full ESD protection design has became an important issue for integrated circuits in advanced deep-submicron CMOS process. To effectively improve ESD (electrostatic discharge) robustness of IC products, a novel substrate-triggered design for input, output, and power-rail ESD protection, as comparing to the traditional gate-driven technique, has been proposed in this thesis. With the substrate-triggered technique, the novel on-chip ESD protection circuits for the input, output, and power pins have been designed and verified in a 0.18-μm CMOS process. The HBM ESD robustness of output ESD protection circuits with ESD protection NMOS of W/L = 300μm/0.3μm can be improved from the original 0.65 kV with the traditional gate-driven design to become 3.2 kV by the proposed substrate-triggered design. With aggressive device scaling, the circuit operating voltage had been decreased correspondingly. Some early 5-V systems changed from 5 V to 3.3 V, or even 1.8 V. Thus, system voltages were no longer 5 V but mixed with 5 V and 3.3 V. For mixed-voltage input design, the IC with 3.3-V power supply needs to accept 5-V input signals. A substrate-triggered technique is proposed to improve ESD protection efficiency of the ESD protection circuit without extra salicide-blocking and ESD-implantation process modifications in a salicided shallow-trench isolation (STI) CMOS process. By using layout technique, the proposed input ESD protection circuit can be merged into a compact device structure to enhance the substrate-triggered efficiency. This substrate-triggered design can increase the ESD robustness and reduce the trigger voltage of the ESD protection device. This substrate-triggered input ESD protection circuit with a field oxide device of channel width of 150 μm can sustain a HBM (Human-Body-Model) ESD level of 3250V without any extra

process modification. Comparing to the traditional ESD protection design of gate-grounded NMOS (gg-NMOS) with salicide-blocking process modification in a 0.25-μm salicided CMOS process, the proposed substrate-triggered design without extra process modification can improve the ESD robustness per unit silicon area from the original 1.2 V/μm^2 of gg-NMOS to 1.73 V/μm^2.

Four novel ESD clamp devices for using in power-rail ESD clamp circuits with the substrate-triggered technique are proposed to improve ESD level in this thesis. The parasitic n-p-n and p-n-p bipolar junction transistors (BJT) in the CMOS devices are used to form the substrate-triggered devices for ESD protection. Four substrate-triggered devices are proposed and investigated in this work, which are named as the substrate-triggered lateral BJT (STLB), the substrate-triggered vertical BJT (STVB), the substrate-triggered double BJT (STDB), and the double-triggered double BJT (DTDB). An *RC*-based ESD-detection circuit is used to generate the triggering current to turn on the proposed substrate-triggered devices. In order to trigger on the parasitic bipolar transistors more effectively, the symmetric multiple-cell square-type layout method is used to realize these substrate-triggered devices. The power-rail ESD clamp circuits with such substrate-triggered devices have been fabricated in a 0.6-μm CMOS process. Experimental results have shown that the substrate-triggered device with double-BJT structure can provide 200% higher ESD robustness in per silicon area, as compared to the NMOS with the traditional gate-driven design.

To keep the total input capacitance almost constant for analog IC design, a design model to find the optimized device dimensions and layout spacings on the input ESD clamp devices is developed in this work, even if the analog signal has a varying input voltage. An analog ESD protection circuit has been designed to solve ESD protection challenge on the analog pins for high-frequency applications. The device dimension (W/L) of ESD protection device connected to the I/O pad can be reduced to only 50μm/0.5μm in a 0.35-μm silicided CMOS process, but it can sustain HBM (MM) ESD level up to 6kV (400V). With such a smaller device dimension, the input capacitance of this analog ESD protection circuit can be significantly reduced to only ~0.4pF for high-frequency applications. This input capacitance can be further reduced if the ESD protection devices are designed with smaller device dimensions. Moreover, by using the optimized layout design to draw the layout of ESD protection NMOS and PMOS devices, the voltage-dependent variation on input capacitance of this analog ESD protection circuit can be kept below 1% under an input voltage swing of 1V. With such almost constant input capacitance, the nonlinear distortion causing by on-chip

ESD protection circuit can be minimized for high-precision applications.

A novel on-chip ESD protection design by using polysilicon diodes as the ESD clamp devices in CMOS process is first proposed in this work. Different process splits have been experimentally evaluated to find the suitable doping concentration for optimizing the polysilicon diodes for both on-chip ESD protection design and the application requirements of the smart card IC's. The secondary breakdown current (It2) of the polysilicon diodes under the forward- and reverse-bias conditions has been measured by the transmission-line-pulsing (TLP) generator to investigate its ESD robustness. Moreover, by adding a new power-rail ESD clamp circuit with the stacked polysilicon diodes as the turn-on control circuit into the IC, the human-body-model (HBM) ESD robustness of the IC with polysilicon diodes as the ESD clamp devices has been successfully improved from the original ~300V to become ≥ 3kV. This design has been practically applied in a mass-production smart card IC.

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陳　東　暘
謹誌於竹塹交大
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INTRODUCTION

1.1 BACKGROUND

Electrostatic discharge (ESD) has become the main reliability concern on semiconductor products, especially in the scaled-down CMOS technologies [1], [2]. Due to low breakdown voltage of the thinner gate oxide in deep-submicron CMOS technologies, efficient on-chip ESD protection circuit should be designed and placed on each pad to clamp the overstress voltage across internal circuits. To sustain reasonable ESD robustness in deep-submicron CMOS IC's, on-chip ESD protection circuits must be added into the chips [1]. ESD level of commercial IC products is generally required to be higher than 2kV in the human-body-model (HBM) ESD stress [3]-[5]. The typical design of efficient ESD protection circuits in a CMOS IC is shown in Fig. 1.1 to protect the internal circuits against ESD damage [6]. But, circuit designers often confuse on how to optimize those ESD protection devices such as Mn1, Mn2, Mn3, Mp1, and Mp2 in Fig. 1.1. To design area-efficient ESD protection circuits, the ESD protection devices are desired as robust as possible in a limited layout area. To sustain the required ESD level, on-chip ESD protection circuits are often drawn with larger device dimensions. Such ESD protection devices with larger device dimensions are often realized with multiple fingers, as that shown in Fig. 1.2, to reduce total layout area [7].

To enhance the ESD robustness of CMOS IC's, the lateral SCR (LSCR) can be used in the ESD protection design [8]-[10]. The LSCR has been developed in some modifications, such as LVTSCR [11]-[12], MLSCR [13]-[14], and gate-coupled LVTSCR [15]-[16]…etc [17]-[31], to design in the ESD protection circuit of CMOS IC's. Due to the low holding voltage (~1V), the SCR devices in the on-chip ESD protection circuit can sustain much higher ESD voltage within smaller layout area, as comparing to the other ESD protection devices in the CMOS IC's. But, the lower trigger current may cause the SCR devices being accidentally triggered on by the external noise pulses while the CMOS IC is in the normal operating conditions. In order to safely apply the SCR device for ESD protection, the SCR device must have a lower triggered voltage and an enough noise margin for CMOS IC's in the noisy

environments [32]-[37]. In a system-level ESD/EMC [38] event easily causes the transient-induced latchup failure in the CMOS IC's. If the SCR devices are used as the ESD clamp devices between the VDD and VSS power lines of the CMOS IC's [18], [26], such ESD-protection SCR devices are easily triggered on by the system-level ESD/EMC transient pulses to cause very serious latchup problem in the CMOS IC's. So, the MOSFET devices are still popularly used in the ESD protection design of CMOS IC's.

But, the effectiveness of the ESD protection circuits is seriously degraded by the advanced CMOS fabrication technologies, especially when the LDD (Lightly-Doped Drain) structure and the silicide diffusion are used [39]. Therefore, salicide-blocking [40]-[45] and ESD-implantation [46]-[55] process modifications had been added into the CMOS processes to improve ESD robustness of MOSFET. These additional process modifications in CMOS technology must be done with extra process steps and mask layers, which increase the fabrication cost and slow down the throughput of production. Moreover, because the layout parameters can affect the geometrical structure of finger-type MOSFET, the turn-on efficiency of the parasitic devices in MOSFET under ESD stress must be changed by the different layout parameters. To optimize the best turn-on efficiency of CMOS devices during ESD stress, the turn-on mechanisms of CMOS devices with different layout parameters under high current stress must be understood and analyzed. To improve the ESD robustness of CMOS devices, the layout modifications of CMOS device have been discussed in some papers [56]-[61]. But, the non-uniform turn-on effect on the CMOS device is still a major problem during ESD stress.

To improve the turn-on uniformity among those multiple fingers of the CMOS devices, the gate-driven design [62]-[67] or substrate-triggered design [68]-[74] had been reported to increase ESD robustness of the large-device-dimension NMOS. Recently, ESD robustness of the gate-driven NMOS had been found to be decreased dramatically when the gate voltage is somewhat increased [44], [64], [75]. The gate-driven design causes ESD current mainly discharging through the strong-inversion channel of NMOS, therefore NMOS is easily burned out by ESD energy. However, with the substrate-triggered design, the parasitic lateral bipolar junction transistor (BJT) of MOSFET can sustain higher ESD current than the gate-driven MOSFET. To analyze and explain the failure mechanisms of device under ESD stress, some simulation methods have been developed [76], [77].

These prior arts, such as some SCR structures, process modifications, layout modifications, and triggered techniques, for ESD protection design are summarized in Table

1.1. The references for each item are also listed in this table. Generally, the SCR structures with smaller silicon area can sustain higher ESD voltage stress than CMOS devices, but the low holding voltage of SCR structures will cause the latchup issue in IC's. So, the SCR structures cannot be publicly used in the ESD protection circuits of IC's. Although some process modifications can improve the ESD robustness of MOSFET, the non-uniformly turn-on effect can cause the unexpected ESD level of MOSFET device with large dimension. Some layout parameters of MOSFET devices can mainly dominate the turn-on behavior of MOSFET devices during ESD stress. To improve the uniform turn-on behavior of MOSFET devices, those layout parameters must be finely investigated.

In this work, the dependences of layout parameters on the ESD robustness of NMOS and PMOS devices are investigated through the fabricated testchips. Besides, the gate-driven design and the substrate-triggered design used to improve ESD robustness of the ESD protection circuits are also investigated in more details [78]. To clearly understand the physical mechanisms on ESD current distribution in the device, the transmission-line-pulse (TLP) [79]-[83] measured results and energy band diagram are used to explain the potential distribution along MOSFET under the gate-driven or substrate-triggered designs. The ESD current distribution among the MOSFET with different layout parameters, gate-driven, or substrate-triggered designs can be well explained by the TLP measured results and the analysis of energy band diagram. Depending on the theory of the substrate-triggered technique, some substrate-triggered ESD protection circuits for input, output, and power-rail of on-chip integrated circuits are designed in this thesis to implement the applications of substrate-triggered technique.

For some high-precision analog circuits, the input capacitance of an analog input pin including ESD protection circuit and a bond pad is required as constant as possible. A major distortion in analog circuits, especially in the single-ended input implementations, comes from the voltage-dependent nonlinear input capacitance of ESD clamp devices connected to the analog input pin. The typical degradation on analog circuit performance due to the nonlinear input capacitance of ESD clamp devices had been reported in [84], where the input capacitance was varying from 4pF to 2pF due to the input voltage increasing from 0V to 2V. Thus for high-precision analog applications, the input capacitance generated from ESD clamp devices on the input pad needs to be kept as constant as possible. A design model to find the optimized device dimensions and layout spacings on the input ESD clamp devices is developed in this work to keep the total input capacitance almost constant, even if the analog

signal has a varying input voltage. An analog ESD protection circuit has been designed to solve ESD protection challenge on the analog pins for high-frequency applications in this thesis. By using the optimized layout design to draw the layout of ESD protection NMOS and PMOS devices with a suitable power-rail ESD clamp circuit, the device dimension (W/L) of ESD protection device connected to the I/O pad can be reduced to smaller silicon area with almost constant capacitance, but it can sustain more HBM ESD robustness.

The diodes or diode string can be designed as ESD protection device or some application in CMOS IC. When the on-chip diodes is realized in a CMOS IC with a p-type substrate, the diodes are often made by the p-n junctions across P+ diffusion and N-well. Due to the common p-substrate of a CMOS IC, there are some parasitic BJT's in the physical structure with the common p-substrate. Therefore, these parasitic BJT's would cause the degradation of signal or high leakage current in really applications. In some modified design, the diodes may be changed to NMOS or PMOS devices in the integrated circuit for realization in CMOS IC [85]. The parasitic vertical or lateral BJT's still exist among these device structures to degrade its transformation efficiency of signal. If the diodes in the CMOS IC are realized by the polysilicon diodes, which have no any parasitic BJT in their device structures, the aforementioned problem can be totally eliminated. However, due to the low heat dissipation capability of the polysilicon layer, the polysilicon diodes result in a very low human-body-model (HBM) ESD level. To understand the characteristics of the polisilicon diodes, different process splits have been experimentally evaluated to find the suitable doping concentration for optimizing the polysilicon diodes for both on-chip ESD protection design and the application requirements of the CMOS IC's. The secondary breakdown current (It2) [86]-[88] of the polysilicon diodes under the forward- and reverse-bias conditions has been measured by the TLP generator to investigate its ESD robustness in this thesis. Moreover, by adding an efficient VDD-to-VSS clamp circuit into the CMOS IC, the HBM ESD robustness of the IC with polysilicon diodes as the ESD clamp devices has been successfully improved. This design has been practically applied in a mass-production smart card IC.

1.2 ESD TESTING COMBINATIONS ON IC

Since the ESD stress may have positive or negative voltage on an input (or output) pin with respect to the grounded VDD or VSS pins, there are four different ESD-testing pin

combinations at each input (output) pin, which are shown in Fig. 1.3(a) and Fig. 1.3(b). For a comprehensive ESD verification, two additional ESD-testing pin combinations, the pin-to-pin ESD stress and the VDD-to-VSS ESD stress in Fig. 1.3(c) and Fig. 1.3(d), had been also specified to verify the whole-chip ESD reliability [6]. These two additional ESD-testing pin combinations often lead to more complex ESD current paths from the input or output pins through the power lines into the internal circuits, which will cause some unexpected damages on the internal circuits even if there are input and output ESD protection circuits in the IC's [89]-[93]. The ESD current discharging paths in an IC during the pin-to-pin ESD stress is illustrated in Fig. 1.4(a), where a positive ESD voltage is applied to an input pin with some output pin relatively grounded, but the VDD and VSS pins are floating. The ESD current will be diverted from the input pad to the floating VDD power line through the forward-biased diode in the input ESD protection circuit. The ESD current flowing on the VDD power line can be conducted into the internal circuits through the connection of VDD metal line. Then, the ESD current is discharged through the internal circuits and may cause random ESD damage in the internal circuits, as the current Path_1 shown in Fig. 1.4(a). If there is an effective ESD clamp circuit across the VDD and VSS power lines, the ESD current can be discharged through the current Path_2 in Fig. 1.4(a). Therefore, the internal circuits can be safely protected against the ESD damages under a negative ESD stress, the similar ESD current paths are shown in Fig. 1.4(b). Thus, an effective ESD clamp circuit with a quick turn-on speed across the power rails is necessary for protecting the internal circuits against ESD damage. However, even if there were suitable ESD protection circuits around the input and output pads, the internal circuits were still vulnerable to ESD damages. Whole-chip electrostatic discharge (ESD) protection has become an important reliability design for deep-submicron CMOS IC's.

Except for such ESD-zapping pin combinations in Fig. 1.3, an additional analog pin-to-pin ESD stress had been especially specified in the standards for the analog circuits with operational amplifiers or differential input stages to verify the ESD level of the analog pins. The analog pin-to-pin ESD stress for the differential input pins of an operational amplifier is illustrated in Fig. 1.5, where the positive or negative ESD voltage is applied to the inverting input pin with the corresponding noninverting input pin relatively grounded. During such an analog pin-to-pin ESD stress, all the other pins including both the VDD and VSS pins are floating. The ESD current during such an analog pin-to-pin ESD stress is illustrated in Fig. 1.6 with the differential input stage of an operational amplifier. Because of the lack of series

resistor between the analog input pad and the input circuits, the overstress ESD current easily reaches to the thinner gate oxide of the differential input stage with a common-source circuit structure. If the VSSA power connection between the inverting input pin and the noninverting input pin has a long metal line in the IC layout, the gate oxide of the differential input stage is easily ruptured by the ESD voltage to generate an ESD current discharging path, as the dashed line shown in Fig. 1.6. The ESD clamp device with large dimension between the inverting input pad and the VSSA power line cannot provide effective ESD protection against this additional analog pin-to-pin ESD stress. Therefore, some advanced designs should be included into the analog ESD protection circuit to overcome this analog pin-to-pin ESD-stress issue.

1.3 THESIS ORGANIZATION

To solve the turn-on efficiency and uniformity issues of on-chip ESD protection devices during ESD stress in deep-submicron CMOS IC's, the turn-on mechanisms of ESD protection device and some designs of ESD protection circuits are discussed in this thesis. The turn-on mechanisms of ESD protection device under ESD stress, gate-driven design, and substrate-triggered design are proposed in Chapter 2 and 3. Some novel substrate-triggered ESD protection designs are proposed from Chapter 4 to 6. The analog ESD protection design is proposed in Chapter 7. The application of polysilicon diodes is proposed in Chapter 8.

In Chapter 2, the dependence of layout spacings on the ESD robustness of finger-type CMOS devices in silicided CMOS process is detailedly investigated and discussed. The energy band diagrams, EMMI photographs, and TLP measurement have been used to analyze and explain the physical turn-on mechanisms of ESD protection device. From the explication of energy band diagrams, the larger channel current and smaller turn-on area of parasitic lateral BJT can cause the damage of MOSFET under ESD stress. This effect causes the degradation of ESD robustness in MOSFET's.

In Chapter 3, the gate-driven effect and substrate-triggered effect on ESD robustness of CMOS devices are measured and compared in this chapter. The operation principles of gate-driven design and substrate-triggered design for ESD protection are explained clearly by energy band diagrams and EMMI photographs. The gate-driven and substrate-triggered techniques can improve the turn-on uniformity of the large-dimension ESD protection devices. But, the higher gate bias can induce larger channel current and higher electric field across gate

oxide to damage MOSFET. This effect causes the degradation of ESD robustness in gate-driven devices. From energy band analysis, substrate-triggered design can continually increase the turn-on area for heat dissipation. Therefore, substrate-triggered design can effectively improve ESD robustness of the ESD protection devices.

In Chapter 4, a novel substrate-triggered design for input, output, and power-rail ESD protection, as comparing to the traditional gate-driven technique, is proposed. The novel on-chip substrate-triggered ESD protection circuits for the input, output, and power pins are designed and verified in a 0.18-μm CMOS process. With the proposed substrate-triggered designs, the ESD protection devices with smaller layout dimension can sustain higher ESD stress than the traditional gate-driven design. The HBM ESD robustness of output ESD protection circuits with ESD protection NMOS of W/L = 300μm/0.3μm can be improved from the original 0.65 kV with the traditional gate-driven design to become 3.2 kV by the proposed substrate-triggered design.

In Chapter 5, a substrate-triggered input ESD protection circuit for mixed-voltage application is realized in a 0.25-μm salicided CMOS process without extra salicide-blocking and ESD-implantation modifications. By using layout technique, the proposed input ESD protection circuit can be merged into a compact device structure to enhance the substrate-triggered efficiency. The trigger voltage of such input ESD protection circuit with field oxide device (FOD) is lowered from original 11.9 V to only 6.4 V to effectively protect the thinner gate oxide (50Å) of input stage in the 0.25-μm salicided CMOS process. The substrate-triggered input ESD protection circuit with a FOD of 150-μm channel width can improve the HBM ESD robustness per unit silicon area from the original 1.2 V/μm^2 of traditional gate-grounded NMOS (gg-NMOS) with salicide-blocking process modification to 1.73 V/μm^2.

In Chapter 6, four novel ESD clamp devices for using in power-rail ESD clamp circuits with the substrate-triggered technique are proposed to improve ESD level. The parasitic n-p-n and p-n-p bipolar junction transistors (BJT) in the CMOS devices are used to form the substrate-triggered devices for ESD protection. Four substrate-triggered devices are proposed and investigated in a 0.6-μm CMOS process, which are named as the substrate-triggered lateral BJT (STLB), the substrate-triggered vertical BJT (STVB), the substrate-triggered double BJT (STDB), and the double-triggered double BJT (DTDB). An *RC*-based ESD-detection circuit is used to generate the triggering current to turn on the proposed substrate-triggered devices. In the experimental results, the DTDB device has the best

performance among these four substrate-triggered devices. With suitable design on the substrate-triggered ESD-clamp circuit, the layout area of the ESD clamp circuit to achieve whole-chip ESD protection can be efficiently reduced to save the silicon cost of CMOS IC's.

In Chapter 7, a design model to find the optimized device dimensions and layout spacings on the input ESD clamp devices is developed, even if the analog signal has a varying input voltage. An analog ESD protection circuit has been designed to solve ESD protection challenge on the analog pins for high-frequency applications. The design model to optimize the device dimensions and layout spacings of ESD protection devices is clearly developed to keep the input capacitance as constant as possible in general CMOS processes. With suitable layout parameters on the input ESD clamp devices, the variation of total input capacitance of the analog ESD protection circuit can be designed below 1% while the analog input signal has an input voltage swing of 1V. The device dimension (W/L) of ESD protection device connected to the I/O pad can be reduced to only 50μm/0.5μm in a 0.35-μm silicided CMOS process, but it can sustain HBM (MM) ESD level up to 6kV (400V). With such a smaller device dimension, the input capacitance of this analog ESD protection circuit can be significantly reduced to only ~0.4pF for high-frequency applications.

In Chapter 8, a novel on-chip ESD protection design by using polysilicon diodes as the ESD clamp devices in CMOS process is first proposed. Different process splits have been experimentally evaluated to find the suitable doping concentration for optimizing the polysilicon diodes for both on-chip ESD protection design and the application requirements of the smart card IC's. The It2 of the polysilicon diodes under forward- and reverse-bias conditions and different layout parameters is clearly investigated. A novel power-rail ESD clamp circuit with the stacked polysilicon diodes as the turn-on control circuit is also designed and analyzed in this chapter. By adjusting the number of the stack diodes in the ESD detection circuit, the turn-on efficient VDD-to-VSS ESD clamp circuit can be applied in the IC with different VDD voltage levels. The HBM ESD level of the smart card IC with the polysilicon diodes as ESD protection devices has been successfully improved up to ≥ 3kV in cooperation with the turn-on efficient power-rail ESD clamp circuit.

Finally, the main results are summarized in Chapter 9. The future works about the turn-on mechanisms of ESD protection devices under ESD stress and substrate-triggered design are given in Chapter 9.

Table 1.1
The summary of ESD protection design methods in CMOS IC's.

Device	Category	Methods	Characteristics		References
SCR	LSCR		Small Layout Size	(1) High triggered voltage (2) Low holding voltage	[8]
	LVTSCR			(1) Low triggered voltage (2) Low holding voltage	[12]
	MLSCR			(1) Middle triggered voltage (2) Low holding voltage	[13]
	Gate-coupled LVTSCR			(1) Low triggered voltage (2) Low holding voltage	[15]
	High-current-triggered LVTSCR			(1) Low triggered voltage (2) High triggered current (3) Low holding voltage	[37]
	High-holding-voltage LVTSCR			(1) Epitaxial structure (2) Low triggered voltage (3) High holding voltage	[33]
MOSFET	Process Modification	Silicide Blocking	Selected drain regions having no silicided diffusion		[40]-[45]
		ESD Implantation	(1) Device without LDD peak structure (2) Reduce junction breakdown voltage		[46]-[55]
	Layout Modification	Multi-finger Type	(1) Easy layout (2) Non-uniformly turn-on effect		[7]
		Polygon Type	(1) Improve uniform turn-on behavior (2) Complicated layout		[60]
		Multi-finger Type with Butting Pickup	(1) Improve uniform turn-on behavior (2) Higher triggered current (3) Low turn-on efficiency		[61]
	Triggered Design	Gate-driven Design	(1) Very low triggered voltage (2) Improve uniform turn-on behavior (3) Over voltage on the gate will cause sudden degradation on ESD level		[62]-[67]
		Substrate-triggered Design	(1) Very low triggered voltage (2) Improve uniform turn-on behavior (3) Continually improve ESD robustness of MOSFET device (4) Small layout area than gate-driven design		[68]-[74]

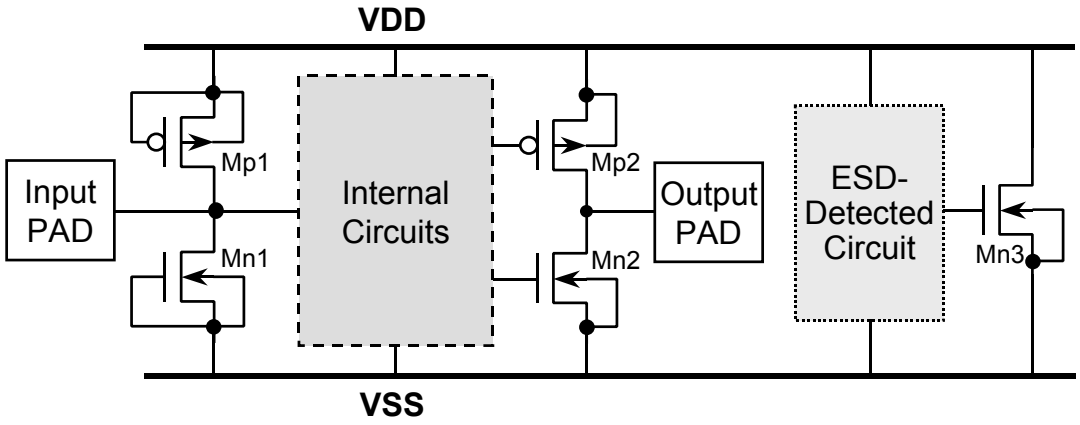


Fig. 1.1 Typical on-chip ESD protection circuits in a CMOS IC.

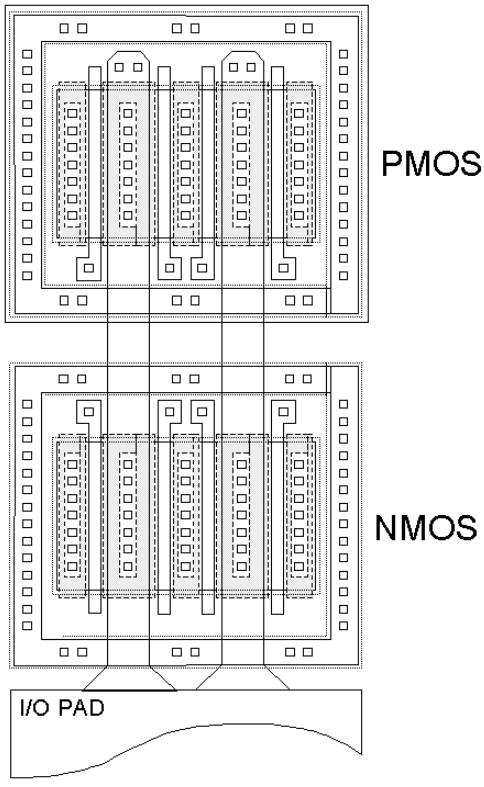


Fig. 1.2 Illustration of the traditional finger-type ESD protection device layout for input or output pads.

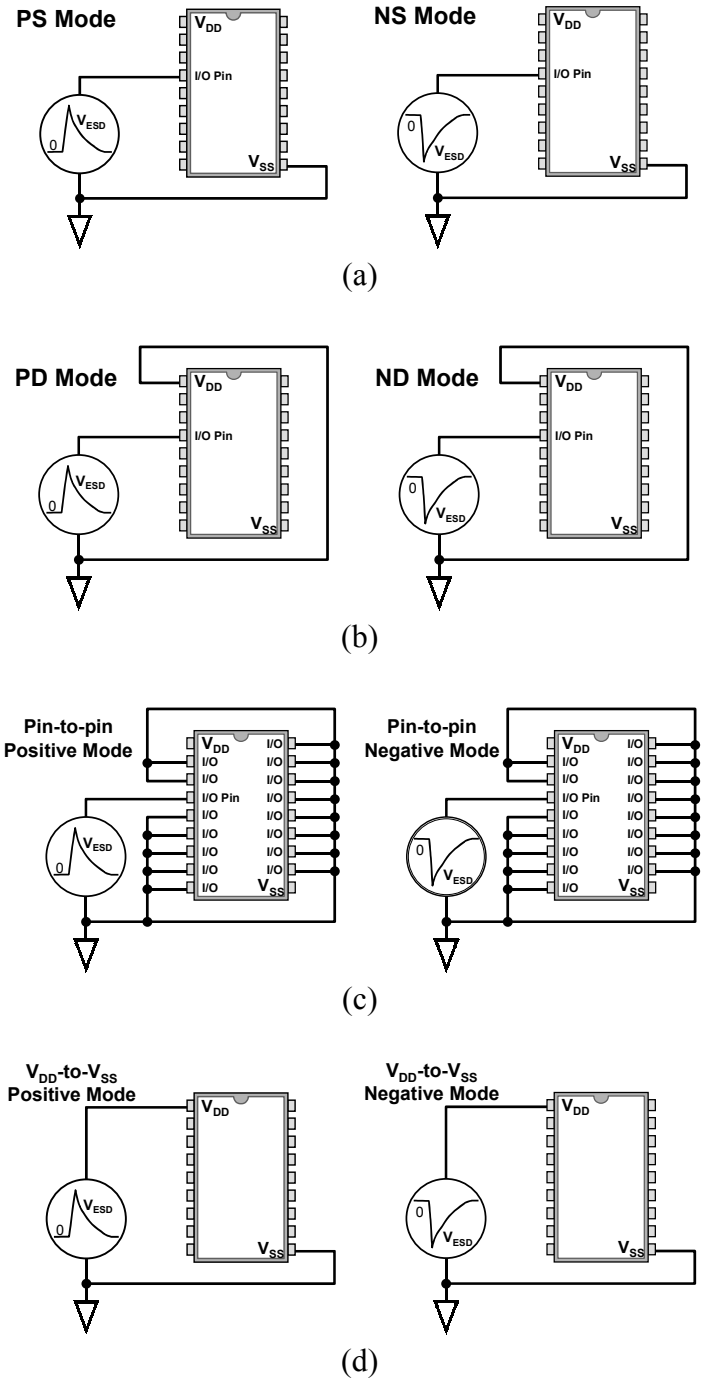
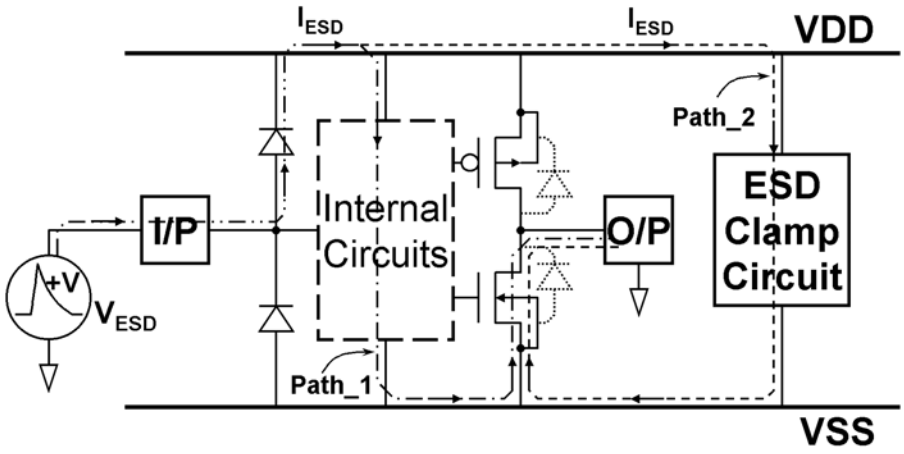
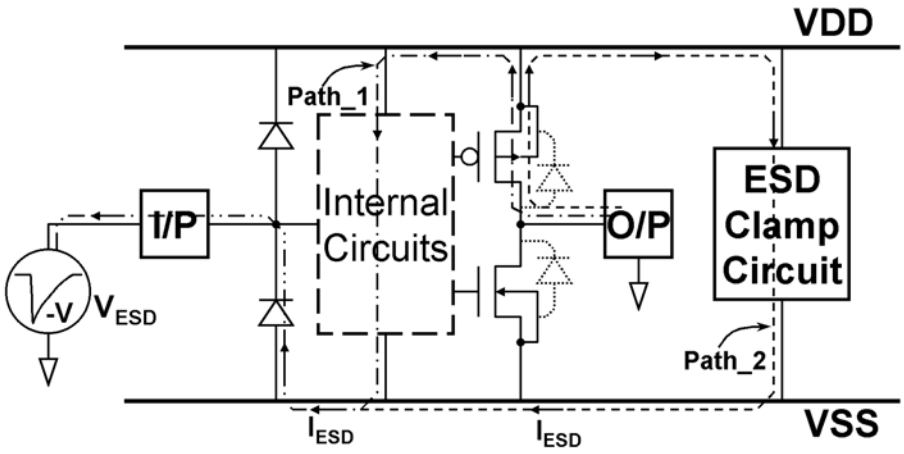


Fig. 1.3 (a) Positive and negative ESD stress on an input (or output) pin with respect to the grounded VSS. (b) Positive and negative ESD stress on an input (or output) pin with respect to the grounded VDD. (c) The pin-to-pin ESD stress: the ESD voltage is applied to an input (or output) pin while all other input or output pins are grounded but the VDD and VSS pins are floating. (d) The VDD-to-VSS ESD stress: the ESD voltage is directly applied to the VDD pin with the VSS pin grounded but all input and output pins are floating.



(a)



(b)

Fig. 1.4 The ESD current discharging paths in an IC during the (a) positive, and (b) negative, pin-to-pin ESD stress conditions. If the IC has no effective ESD clamp circuit between the VDD and VSS power rails, the ESD current is discharged through the Path_1, which often causes ESD damage located at the internal circuits. If the IC has an effective ESD clamp circuit between the VDD and VSS power rails, the ESD current is discharged through the Path_2.

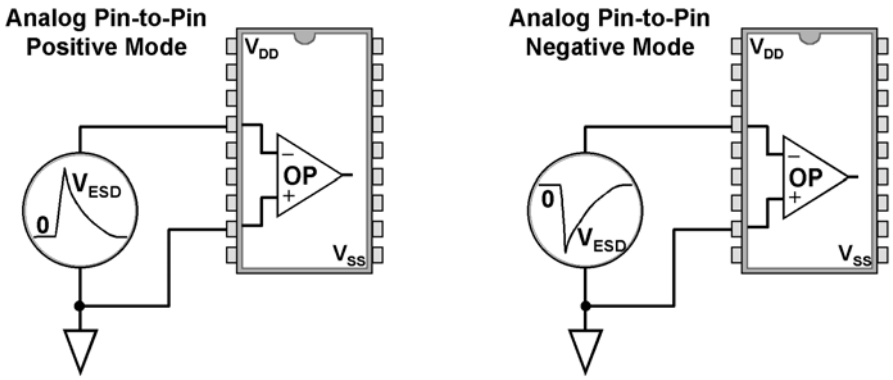


Fig. 1.5 Pin combination of the additional analog pin-to-pin ESD stress to verify the ESD level of analog circuits with the operational amplifier or differential input stage.

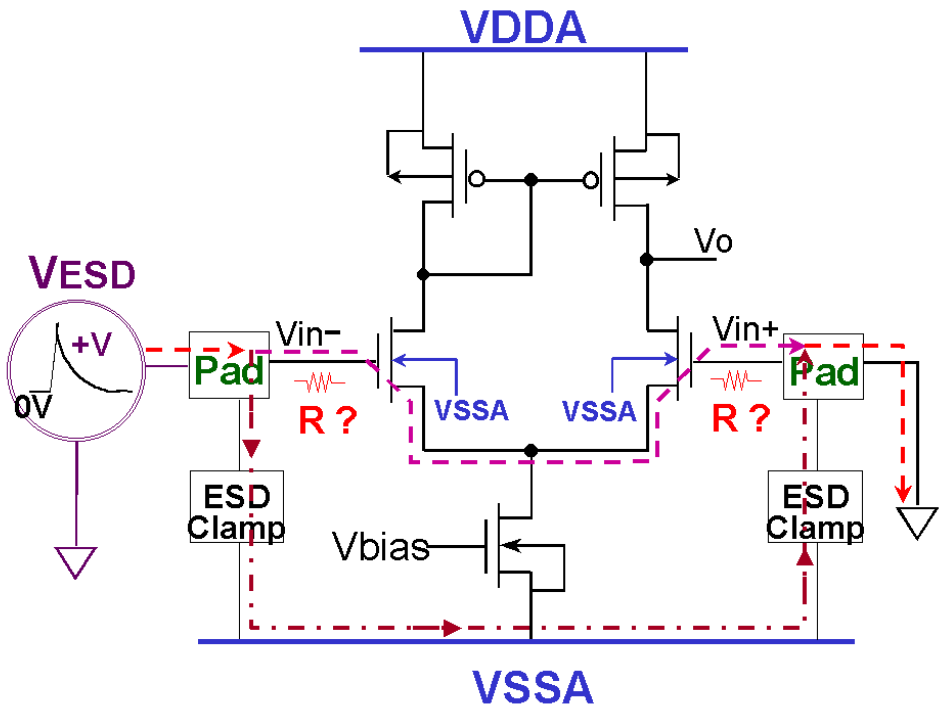


Fig. 1.6 ESD current path during the analog pin-to-pin ESD stress.

CHAPTER 2

DEPENDENCE OF LAYOUT PARAMETERS ON ESD ROBUSTNESS OF CMOS DEVICES

To sustain the required ESD level, on-chip ESD protection circuits are often drawn with larger device dimensions. Such ESD protection devices with larger device dimensions are often realized with multiple fingers to reduce total layout area [94]. An example of finger-type NMOS is shown in Fig. 2.1. Some layout parameters are also shown in this figure. However, some layout parameters can affect ESD robustness of those ESD protection devices [75], [95]-[96].

Because the layout parameters can affect the geometrical structure of finger-type MOSFET, the turn-on efficiency of the parasitic devices in MOSFET under ESD stress must be changed by the different layout parameters. To optimize the best turn-on efficiency of CMOS devices during ESD stress, the turn-on mechanisms of CMOS devices with different layout parameters under high current stress must be understood and analyzed. By using the TLPG (Transmission Line Pulsing Generator), turn-on characteristics of CMOS devices under high current stress can be found and analyzed [79]-[83]. From the investigation of layout parameters on the ESD robustness of CMOS device, the optimized parameters can be verified to enhance the turn-on efficiency of CMOS device under ESD stress.

In this chapter, the dependences of layout parameters on the ESD robustness of NMOS and PMOS devices are investigated through the fabricated testchips. To clearly understand the physical mechanisms on ESD current distribution in the device, the TLP measured results and energy band diagram are used to explain the effects of each layout parameters. The ESD current distribution among the CMOS device with different layout parameters designs can be well explained by the TLP measured results and the analysis of energy band diagram.

2.1 TURN-ON MECHANISM OF MOSFET UNDER ESD STRESS

To illustrate the turn-on behavior of gate-grounded MOSFET during ESD stress, one

unit-finger structure of a multiple-finger NMOS device is shown in Fig. 2.2. In this structure, two parasitic diodes D_S and D_D can be found in the p-n junctions between source/drain and guardring of Fig. 2.2. When the p-type substrate guardring, sources, and gate of this NMOS are connected to ground, the parasitic diode D_D between drain and substrate is reverse biased under the positive ESD stress (V_{ESD}) in Fig. 2.2. Some reverse-biased current (I_{SDD}) in Fig. 2.2 can flow into the substrate during the positive ESD stress on the drain of NMOS. The parasitic lateral BJT with a base resistance (R_B) can be found under the NMOS, as shown in Fig. 2.2. The reverse-biased current can increase base voltage of the parasitic lateral BJT. Due to the different distances from the base region to the substrate guardring, the base voltage of parasitic lateral BJT in the central region of finger-type NMOS is higher than that in the sided regions in Fig. 2.2. When the base voltage in the central region is increased up to trigger on the parasitic lateral BJT, the NMOS will enter into its snapback region. Under higher ESD stress, the turned-on region may be extended with more area in each finger of NMOS. But, the lateral BJT in the central region of NMOS is often firstly triggered into snapback to cause the non-uniform turn-on issue among the multiple fingers of NMOS device.

To understand the turn-on behavior of the parasitic lateral BJT in NMOS, the energy band diagrams of half unit-finger NMOS device under ESD stress are analyzed in Fig. 2.3. To simply analyze the variation of energy band diagrams, only conduction band variations on the x-y and y-z planes along the half unit-finger structure are illustrated in Fig. 2.3. Because the voltage drop implies the negative variation of energy band, the electrons flow from source to drain can be understood from Fig. 2.3. The related dependence between voltage drop variation and energy variation is expressed as

$$\Delta E_C = -q \cdot \Delta V_{DS}. \tag{2.1}$$

Because the reverse-biased current pulls down the energy band of base region in the parasitic lateral BJT, the depletion layer of reverse-biased junction can modulate the base width. The lower energy band barrier and shorter effective base width cause the fast turn on of the parasitic lateral BJT at the central region of the NMOS. Therefore, during positive ESD stress, the multiple fingers of NMOS cannot be uniformly turned on. Only some regions of several fingers in the NMOS were turned on and therefore damaged by ESD.

To verify the turn-on uniformity, different current pulses are applied to the drain of a gate-grounded NMOS, which has a W/L=300μm/0.5μm in a 0.35-μm silicided CMOS process. The measurement setup is shown in Fig. 2.4(a), where the current pulse has different pulse heights. The corresponding I-V curve of the gate-grounded NMOS is drawn in Fig.

2.4(b). The EMMI photographs on the gate-grounded NMOS during the stresses of different current pulses are shown in Figs. 2.4(c)~2.4(k) to observe its turn-on behavior. From the hot spots in Figs. 2.4(c)~2.4(f), the reverse-biased breakdown current in the gate-grounded NMOS is initially flowing toward the guardring. When the base potential is increased up to trigger on the parasitic lateral BJT, the hot spots become to locate at the central regions of the finger-type NMOS, as those shown in Figs. 2.4(g)~2.4(k). Because the short-channel NMOS has an obvious snapback I-V curve, as that shown in Fig. 2.5(a), the turned-on central fingers in Fig. 2.4(k) cause the ESD current mainly discharging through those fingers. If the turned-on region cannot be extended to full regions of all fingers before second breakdown occurs in NMOS, the turned-on central region in Fig. 2.4(k) will be burned out by the over-heating ESD current. This often causes a low ESD level, even if the multiple-finger NMOS has a large device dimension. On the contrary, the PMOS has no obvious snapback I-V curve, as that shown in Fig. 2.5(b). The PMOS eventually has a good uniform turn-on efficiency.

Depending on the doping profile of impurities in channel region and some layout parameters of MOSFET, the external ESD voltage can lower the energy band of surface channel or turn on the parasitic lateral BJT. Generally, there are three main current paths in MOSFET during ESD stress. The first path is the strong-inversion current along surface channel of MOSFET when some positive voltage is biased at the gate. This current path is shown as the Path1 in Fig. 2.6(a). The second path is formed by the drain-induced barrier lowering in LDD (lightly-doped drain) region nearby the surface channel, as the Path2 shown in Fig. 2.6(b), where the gate is biased at 0V. The third path is formed by the parasitic lateral BJT in MOSFET, but it is far away from the channel surface of MOSFET, which is shown as the Path3 in Fig. 2.6(c) with a 0-V gate bias. During positive ESD stress, a high voltage is applied on the drain of MOSFET and pulls down the energy band of drain. The corresponding two-dimension energy band diagrams on the x-y plane of NMOS under different conditions are illustrated in Fig. 2.6(d) with a positive gate bias, in Fig. 2.6(e) with lowered energy band nearby LDD, and in Fig. 2.6(f) with lowered energy band far away from surface, respectively. Three electron flow paths (Path1, Path2, and Path3) have been clearly indicated in those band diagrams. To further understand such turn-on paths, one-dimension energy band diagrams along the A-A' lines of Figs. 2.6(a), 2.6(b), and 2.6(c) in the x-axis direction are drawn in Figs. 2.6(g), 2.6(h), and 2.6(i), respectively. High electric field across the gate oxide can be found in Fig. 2.6(g) and Fig. 2.6(h), but it isn't found in Fig. 2.6(i) during ESD stress. With different

current paths, the NMOS during ESD stress may be damaged by different failure mechanisms. However, the gate or substrate biases of MOSFET can affect the current paths along the MOSFET during ESD stress. Therefore, the ESD robustness of MOSFET can be further improved by the gate-driven or the substrate-triggered designs.

2.2 LAYOUT DEPENDENCE

To design robust ESD protection devices, the layout spacings are the major considerations for finger-type CMOS devices. The main layout parameters to affect ESD robustness of the ESD protection devices are the channel width (W), the channel length (L), the clearance from contact to poly-gate edge at drain and source regions (Dcg and Scg), the spacing from the drain diffusion to the guardring diffusion (Sba), and the finger width (Wf) of each unit finger, which have been indicated in Fig. 2.1 with the 3-D device structure. When the dependences of ESD current paths on the layout parameters are well understood, ESD protection devices can be optimized to perform higher ESD robustness.

The layout factors to affect the ESD robustness of CMOS devices are practically investigated by the fabricated testchips in a 0.35-μm silicided CMOS process. The ZapMaster ESD tester, produced by Keytek Instrument Corp., is used to measure the human-body-model (HBM) ESD level of the fabricated testchips. The failure criterion is generally defined at 1-μA leakage current under 1.1 times VDD bias, when the device is kept off. The experimental results are measured and discussed in the following. To investigate the turn-on behavior of device during high ESD current stress, transmission line pulsing (TLP) technique has been widely used to measure the second breakdown characteristics of devices. The TLP measured results are also shown and analyzed in the following.

2.2.1 Channel Width and Silicide Effect

To discharge more ESD current, the channel widths of ESD protection devices are often designed with larger dimension. However, if non-uniform turn-on effect is considered, the MOSFET with a larger channel width cannot sustain high ESD level as expectation. The NMOS and PMOS devices with different channel widths (W) have been fabricated in a 0.35-μm silicided CMOS process. Each unit-finger width (Wf) of the NMOS and PMOS

devices in this investigation is kept as 50 μm. The NMOS and PMOS devices with or without the RPO layer [61] to block the silicided diffusion on the drain region are also drawn in the testchips to investigate their ESD levels. For both NMOS and PMOS devices in this investigation, the channel length (L), the clearance from the drain contact to poly-gate edge (Dcg), the clearance from the source contact to poly-gate edge (Scg), and the spacing from the drain diffusion to the guardring diffusion (Sba) are kept at 0.8μm, 3μm, 1μm, and 4μm, respectively.

To analyze the second breakdown characteristics of NMOS, the transmission line pulsing generator (TLPG) in Fig. 2.7(a) is used to measure the second breakdown current and the turn-on resistance of NMOS. The corresponding circuit for TLPG measurement on a gate-grounded NMOS is shown in Fig. 2.7(b). The measured I-V characteristics and leakage currents of NMOS with W/L=200μm/0.8μm by TLP with a pulse width of 100 ns are shown in Fig. 2.7(c). The second breakdown current is indicated as It_2 in Fig. 2.7(c). The turn-on resistance is defined as the voltage variation over current variation before second breakdown in the TLP measured I-V curve. The turn-on resistance can be expressed as

$$R_{device} \equiv \partial V_{DS}/\partial I_D. \tag{2.2}$$

From the TLP measured results, the relation between second breakdown current (It_2) and HBM ESD level (V_{ESD}) can be approximated as [45], [97]

$$\text{HBM } V_{ESD} \approx (1500+R_{device})\times It_2. \tag{2.3}$$

The turn-on resistances of finger-type NMOS devices with different channel widths, but with the same unit-finger width and channel length, are shown in Fig. 2.7(d). For an NMOS with 50-μm channel width, the turn-on resistance R_{50} in Fig. 2.7(d) is 6.83Ω. If the NMOS with longer channel width can be uniformly turned on, the dependence between the turn-on resistance and the channel width can be drawn as the ideal curve in Fig. 2.7(d). In the ideal case, the turn-on resistance of NMOS with 600-μm channel width must be only 0.57Ω. But, the experimental result on the turn-on resistance R_{600}(=1.64Ω) of NMOS with 600-μm channel width in Fig. 2.7(d) is far from the ideal turn-on resistance. It implies that the finger-type gate-grounded NMOS device with a longer channel width cannot be uniformly turned on during ESD stress.

The relations between the device channel widths (W) and the HBM ESD level of NMOS and PMOS devices in a 0.35-μm CMOS process are investigated in Fig. 2.8(a) and Fig. 2.8(b), respectively. In Fig. 2.8(a), the NMOS is stressed under the positive-to-V_{SS} ESD stress, whereas the PMOS is stressed under the negative-to-VDD ESD stress in Fig. 2.8(b). In

Fig. 2.8(a), the HBM ESD level of the NMOS device is increased while the device channel width is increased. If the device channel width is increased, more fingers can be drawn and connected in parallel to form the large-dimension NMOS device. The ESD robustness of such large-dimension device may be increased while the device channel width is increased. But, in Fig. 2.8(a), the ESD level (3.4kV) of the silicide-blocking NMOS with a channel width of 600μm is less than that (3.5kV) of the NMOS with a channel width of 400μm. This is due to the non-uniform turn-on issue among the multiple fingers of a large-dimension device. In the finger-type NMOS, if the base current can not uniformly trigger on the distributed parasitic lateral BJT's of the NMOS, the ESD current will be concentrated in some local regions to cause the non-uniform turn-on phenomena in the NMOS under ESD stress.

In Fig. 2.8(b), the HBM ESD levels of the PMOS with or without silicided diffusion are both increased as the device channel width is increased. The ESD level of the silicided PMOS with a channel width of 400μm is around -2.45kV, but that of the silicide-blocking PMOS with the same device dimension and layout style is -4.45kV. This verifies the effectiveness of the silicide-blocking process used to improve ESD level in deep-submicron CMOS technologies. The continue increase of ESD level, when the channel width of PMOS has been increased, is due to the less snapback characteristics of the PMOS. The snapback I-V characteristic of a PMOS is shown in Fig. 2.5(b). As comparing the I-V curves between Fig. 2.5(a) and Fig. 2.5(b), the PMOS with a less snapback characteristics causes a more turn-on uniformity among its multiple fingers. Therefore, it has a continue increase on its ESD level, when the channel width of PMOS is increased.

The NMOS with silicide-blocking process can sustain higher ESD level than that with the silicided diffusion [57]. NMOS devices with or without silicide-blocking mask have different turn-on resistances in the TLP-measured I-V curves of Fig. 2.9. The turn-on resistance of the silicided NMOS with W/L=200μm/0.8μm is only 2.45Ω, but that of the silicide-blocking NMOS with the same device dimension and layout style is 4.06Ω. However, the It_2 of silicide-blocking NMOS is 103% higher than that of the silicided NMOS.

The silicide diffusion on the drain of MOSFET can decrease the ballast resistance of the device structure [57] and change the current distribution in the device. The mainly ESD current in the silicided NMOS is concentrated in the channel surface of the NMOS, but it can be away from the channel surface in the silicide-blocking NMOS. Because the NMOS devices with or without silicided diffusion have different failure mechanisms, the silicide-blocking NMOS can sustain much higher HBM ESD stress in the experimental results of Fig. 2.8. The

average ESD level of the silicided NMOS with a channel width of 200μm is only 0.57kV, but that of the silicide-blocking NMOS with the same device dimension and layout style is 3kV.

To explain the degradation on ESD robustness of silicided NMOS device, the energy band diagrams of NMOS with or without the silicided diffusion are compared in Fig. 2.10(a) and Fig. 2.10(b), respectively. A positive ESD stress is applied to the drain of NMOS, whereas the gate, source, and bulk of NMOS are connected to ground. The energy band diagrams are analyzed along both the lines A-A' and B-B' in Fig. 2.10(a) with silicided diffusion, and in Fig. 2.10(b) without silicided diffusion. The E_C and E_V in Fig. 2.10 are the conduction and valence energy levels, respectively. In the device structures of Fig. 2.10(b), the V_{RD} (V_{RS}) is the voltage drop on the drain (source) diffusion, and the R_D (R_S) is the effective sheet resistance of drain (source) diffusion. The V_{act} is defined as the active turn-on voltage of parasitic lateral BJT in the NMOS. The regions G and S in Fig. 2.10 are defined as the effective current discharging regions in the substrate of NMOS under positive ESD stress. From Fig. 2.10(a), the drain voltage can pull down the band diagram at the drain silicided diffusion because of the silicided diffusion with a low resistance and close to the LDD structure. The major voltage drop of drain bias (V_{DS}) is located along the surface channel of MOSFET. Therefore, the energy band on the surface channel will be lowered. This effect of drain-induced barrier lowering can enhance the channel current forming in the NMOS device. Major ESD current will flow into the turned-on region G in Fig. 2.10(a), which is very close to the interface between gate oxide and surface channel of NMOS. With a shallower current path in the device, the ESD current can easily damage the surface channel and the gate oxide of NMOS. But, a silicide-blocking diffusion can reduce the turn-on probability of Path2 in Fig. 2.6. The energy band diagram in Fig. 2.10(b) can explain this phenomenon. The drain p-n junction near the surface channel is connected in series with a larger sheet resistance in the silicide-blocking NMOS, but the p-n junction at the bottom of drain diffusion has a smaller sheet resistance (R_D). The sheet resistance of silicide-blocking drain diffusion can reduce the voltage drop on the channel surface. So, the ESD current is discharged through the parasitic lateral BJT, which is far away from the channel surface. The silicide-blocking drain diffusion can avoid ESD overstress on the surface channel and the gate oxide, therefore the silicide-blocking NMOS has a much higher ESD robustness.

2.2.2 Channel Length

The TLP measured I-V curves of gate-grounded NMOS devices with different channel lengths (L=0.35μm, 0.8μm, 1.2μm, and 1.5μm) are compared in Fig. 2.11. The layout style and other parameters are all kept the same (W=200μm, Wf=50μm, Dcg=3μm, Scg=1μm, and Sba=4μm), but only the channel length is different under this investigation. Both the NMOS and POMS are fabricated with the RPO layer to block the silicided diffusion on the drain and source regions. The voltage drop (V_{DS}) from drain to source of the gate-grounded NMOS in snapback region can be expressed as

$$V_{DS} = V_{RD}+V_{act}+V_{RS} = I_D \cdot R_D+V_{act}+ I_D \cdot R_S \equiv I_D \cdot R_D'+V_{act}, \quad (2.4)$$

where the V_{RD} (V_{RS}) is the voltage drop on the drain (source) diffusion, and the R_D (R_S) is the effective sheet resistance of drain (source) diffusion as the definition of previous sub-section III.A in Fig. 2.10(b). The V_{act} is the active turn-on voltage of parasitic lateral BJT in the NMOS. Generally, the Scg parameter is drawn with a small clearance. During positive current stress, the resistance of R_S can be considered as a small constant value. To simplify the analysis, the sum of R_D and R_S is defined as R_D'. From equations (2.2) and (2.4), the turn-on resistance R_{device} can be re-written as

$$R_{device} = R_D'+\partial V_{act}/\partial I_D \equiv R_D'+R_{BJT}, \quad (2.5)$$

where the effective turn-on resistance R_{BJT} of parasitic lateral BJT is defined as $\partial V_{act}/\partial I_D$. The current I_D is a function of effective base width (W_B), turn-on area (A_D and A_S) in drain/source edge, voltage drop between base and emitter (V_{BE}), and voltage drop between base and collector (V_{BC}) in the parasitic lateral BJT [98]. It can be further expressed as

$$I_D = qA_S n_i^2 \left[\frac{D_B}{L_B N_B} \left(\frac{L_B}{W_B} \right) \right] \left(e^{qV_{BE}/kT} - 1 \right)$$

$$- qA_D n_i^2 \left[\frac{D_C}{L_C N_C} + \frac{D_B}{L_B N_B} \left(\frac{L_B}{W_B} + \frac{W_B}{2L_B} \right) \right] \left(e^{-qV_{CB}/kT} - 1 \right). \quad (2.6)$$

The turn-on areas of A_D and A_S imply two effective turn-on areas in the effective base region of the parasitic lateral BJT among multiple fingers of the NMOS. The active turn-on voltage V_{act} between collector and emitter of parasitic lateral BJT is the sum of base-to-emitter voltage V_{BE} and collector-to-base voltage V_{CB}, which is written as

$$V_{act} = V_{BE} + V_{CB}. \quad (2.7)$$

Generally, V_{BE} is larger than kT/q, and V_{CB} is a large reversed bias on the p-n junction of drain diffusion in the NMOS during positive ESD stress. The effective base width (W_B) is a function of NMOS's channel length (L) and depletion width (W_B') of the reverse-biased p-n

junction between the drain diffusion and the bulk of NMOS. It is expressed as

$$L \approx W_B + W_B'. \tag{2.8}$$

To simply analyze the geometric effect, the base concentration of N_B in (2.6) is assumed as a constant distribution in the bulk of NMOS.

In (2.6), the turn-on areas (A_S and A_D) of parasitic lateral BJT are further assumed as constant values in the following discussion. Under the same ESD stress, when the channel length ($L \approx W_B + W_B'$) of NMOS is increased, V_{BE} or V_{CB} must be increased to keep the I_D as a constant current in (2.6). So, V_{act} must be increased when the channel length (L) of NMOS is increased in this assumption. From (2.5) and (2.6), the effective turn-on resistance (R_{BJT}) of parasitic lateral BJT can be approximated as

$$R_{BJT} \approx \frac{kT}{q^2 A_S n_i^2}\left[\frac{L_B N_B}{D_B}\left(\frac{W_B}{L_B}\right)\right] e^{-qV_{BE}/kT}$$

$$+ \frac{kT}{q^2 A_D n_i^2}\left[\frac{D_C}{L_C N_C} + \frac{D_B}{L_B N_B}\left(\frac{L_B}{W_B}\right)\right]^{-1} e^{qV_{CB}/kT}. \tag{2.9}$$

From afore mentioned discussion, NMOS with a longer channel length has a larger R_{BJT} under the same current stress. If the effective sheet resistances of NMOS with different channel lengths were the same as each other's, the NMOS with a longer channel length should have a larger turn-on resistance under the same current stress. But from the experimental results of Fig. 2.11, the NMOS with channel length of 1.2μm has a lower turn-on resistance of 3.08Ω than that with a channel length of 0.8-μm, which has a 4.06-Ω turn-on resistance. So, the NMOS with channel length of 1.2μm must have a very low sheet resistance in the drain diffusion region of NMOS. The effective sheet resistance of the drain diffusion in NMOS is decreased, when the channel length of NMOS is increased under the same current stress, to have a lower turn-on resistance (R_{device}) in the TLP measured results of Fig. 2.11. In this assumption of fixed turn-on areas, the variation of channel length from shorter to longer in MOSFET can cause the moving of the turned-on region in the parasitic lateral BJT from the sideward to the bottom of drain diffusion in the MOSFET device structure.

By another assumption, if the turn-on areas of A_S and A_D are not fixed at some local regions, the V_{BE} and $|V_{BC}|$ can be fixed in certain voltages in equation (2.6) for NMOS devices with different channel lengths. While V_{BE} and $|V_{BC}|$ are fixed, W_B' is kept as a constant value for MOSFET devices with different channel lengths. To sustain the same

current stress in the turned-on parasitic lateral BJT's with different effective base widths, the turn-on areas of A_S and A_D must be increased when the channel length of MOSFET is increased. The ratios of A_S/W_B and A_D/W_B must be kept at constant values to limit the I_D as a constant current in (2.6). Then, the R_{BJT} will be a constant resistance from (2.9) in this assumption. Therefore, the larger turn-on areas can reduce the effective sheet resistances in the drain/source regions of MOSFET. This can explain why the gate-grounded NMOS with a long channel length has a lower turn-on resistance measured by TLP in Fig. 2.11. In the actual case, the turn-on mechanism is operated between these two assumptions. The turn-on areas of A_S, A_D and R_{BJT} can be increased, and the turned-on region can be moved or extended from the sideward to the bottom of drain/source diffusions in MOSFET, when the channel length L of MOSFET is increased.

The dependences of the device channel length (L) on the HBM ESD level of NMOS and PMOS devices in a 0.35-μm CMOS process are shown in Fig. 2.12(a) and Fig. 2.12(b), respectively. From the experimental results shown in Fig. 2.12(a), the HBM ESD level of the NMOS with a minimum channel length of 0.35μm is 3.25kV, whereas that of the NMOS with a channel length of 0.5 (0.8) μm is 2.9 (3.1) kV. In Fig. 2.12(a), the NMOS with a channel length of 0.5 μm has the lowest ESD level in this experimental investigation. When an NMOS has a shorter enough channel length, the efficiency and performance of the parasitic lateral BJT in the NMOS device is significantly improved. Therefore, it can sustain much higher ESD level than the NMOS with a medium channel length about 0.5 μm. On the contrary, the PMOS with a shorter channel length has a lower ESD level, as shown in Fig. 2.12(b). Even if the PMOS has a minimum channel length of 0.35 μm, its HBM ESD level is only -1.85kV because the turn-on efficiency of lateral p-n-p BJT in PMOS is not improved.

To summarize the explanation on the dependence of channel length parameter on the ESD robustness of NMOS device, the energy band diagrams of NMOS with long, normal, and short channel lengths are illustrated in Figs. 2.14(a), 2.14(b), and 2.14(c), respectively. Under the same current stress in Figs. 2.14(a), 2.14(b), and 2.14(c), the energy band diagrams are analyzed along the lines A-A', B-B', and C-C' in the device structure, respectively. The positive ESD current stress can induce the turn on of parasitic lateral BJT and discharge the ESD current through the region S of Fig. 2.13. If the discharge current is not crowded in the sideward of drain edge in NMOS, the turn-on area of parasitic lateral BJT at drain edge can be concentrated in the bottom of drain diffusion for long channel length NMOS in Fig. 2.13(a). The longer channel length device has a larger turn-on area in the NMOS to discharge the ESD

current. The parasitic lateral BJT has a larger turn-on volume for heat dissipation during the same ESD current stress.

From previous analysis, the turned-on parasitic lateral BJT in the NMOS with shorter channel length has a smaller turn-on area. Both the effective turn-on BJT resistance and effective sheet resistance of short channel length device must be larger than those effective resistances of long channel length device. But, the 3.84-Ω turn-on resistance of NMOS with 0.35-μm channel length is smaller than the 4.06-Ω turn-on resistance of NMOS with 0.8-μm channel length in the TLP measured results of Fig. 2.11. Because the LDD structures of short channel length device induce a shorter effective base width nearby the channel surface of NMOS, the energy band of region G in Fig. 2.13(c) can be lowered by the drain-induced barrier lowing in the short channel length device, as that shown in Fig. 2.13(c). Therefore, the short channel length device has an extended current path to discharge ESD current. A voltage drop is established in the region S of Fig. 2.13(c) to trigger on the parasitic lateral BJT, and another channel current is also formed in the region G of Fig. 2.13(c). The region G and S can be merged together to supply more area for heat dissipation under ESD stress. Owing to this phenomenon, NMOS device with shorter channel length can sustain higher ESD stress as the experimental data shown in Fig. 2.12(a). To avoid the hot carrier effect, the doping styles of the region G and S in NMOS device are different from that of PMOS device in the 0.35-μm CMOS process. There is no extended area in the region G to sustain more area for heat dissipation in PMOS device. So, we can't find the improvement of short channel effect in Fig. 2.12(b). From this experimental investigation, the selection on the channel length of NMOS and PMOS for ESD protection is quite different in the 0.35-μm silicided CMOS process.

2.2.3 Clearance from Drain/Source Contact to Poly-Gate Edge

Because the Dcg parameter can cause the capacitance variation of the reverse-biased drain diffusion junction in NMOS under positive ESD stress, the NMOS with different Dcg parameters will have different voltage drop (ΔV_{CB}) between the drain diffusion and the bulk of NMOS. The total junction capacitance (C_J) [99] of finger-type NMOS under reverse bias stress ($V_{BC}<0$) can be expressed as

$$C_J \approx Nf \cdot \left[Wf \cdot Dcg \cdot C_{J0} \cdot \left(1 + \frac{V_{CB}}{\phi_C}\right)^{-m_J} + Wf \cdot C_{JSWG\,0} \cdot \left(1 + \frac{V_{CB}}{\phi_{CSWG}}\right)^{-m_{JSWG}} \right.$$

$$+2\cdot Dcg\cdot C_{JSW0}\cdot\left[\left(1+\frac{V_{CB}}{\phi_{CSW}}\right)^{-m_{JSW}}\right]. \tag{2.10}$$

All of m_J, m_{JSWG}, and m_{JSW} are less than 1. Nf is the finger number of finger-type NMOS in Fig. 2.1. During ESD stress or TLP test, the total stress charge (Q_{stress}) can be approximated as

$$Q_{stress}=I_D\Delta t\approx-\int_0^{-\Delta V_{CB}}C_J\cdot dV_{BC}\ . \tag{2.11}$$

From the approximation of fixed charge stress in (2.10) and (2.11), the variation of Dcg parameter can affect the voltage drop (ΔV_{CB}) between the drain diffusion and the bulk of NMOS. The total stress charge (Q_{stress}) is re-calculated as

$$\begin{aligned}Q_{stress}\approx Nf\cdot\Bigg\{&\frac{Wf\cdot Dcg\cdot C_{J0}\cdot\phi_C}{1-m_J}\left[\left(1+\frac{\Delta V_{CB}}{\phi_C}\right)^{1-m_J}-1\right]\\&+\frac{Wf\cdot C_{JSWG0}\cdot\phi_{CSWG}}{1-m_{JSWG}}\left[\left(1+\frac{\Delta V_{CB}}{\phi_{CSWG}}\right)^{1-m_{JSWG}}-1\right]\\&+\frac{2\cdot Dcg\cdot C_{JSW0}\cdot\phi_{CSW}}{1-m_{JSW}}\left[\left(1+\frac{\Delta V_{CB}}{\phi_{CSW}}\right)^{1-m_{JSW}}-1\right]\Bigg\}.\end{aligned} \tag{2.12}$$

When the Dcg parameter is increased but all of other parameters (Nf, Wf, C_{J0}, m_J, ϕ_C, C_{JSWG0}, m_{JSWG}, ϕ_{CJSW}, C_{JSW0}, m_{JSW}, and ϕ_{CSW}) are fixed in (2.12), ΔV_{CB} must be decreased because of the fixed total stress charge (Q_{stress}). To discharge the same current stress in (2.6), the smaller ΔV_{CB} causes the larger turn-on area A_D (A_S) in the parasitic lateral BJT when the BJT is triggered on.

To investigate the I-V characteristics of the gate-grounded NMOS devices with different Dcg parameters during ESD stress, the TLP measured I-V curves of the NMOS devices with different Dcg parameters of 1.5μm, 3μm, and 5μm are shown in Fig. 2.14. In the silicide-blocking NMOS devices, all of the layout style and other parameters are kept the same (W=200μm, Wf=50μm, L=0.8μm, Scg=1μm, and Sba=4μm). From the previous discussion, the larger Dcg parameter can cause larger turn-on area in the parasitic lateral BJT of NMOS under ESD stress. Although a device with larger clearance of Dcg has larger turn-on area in NMOS, the device with larger Dcg parameter may have a larger sheet resistance in the NMOS. A simple model of sheet resistance in the drain diffusion of NMOS can be created from Fig. 2.10(b), which is approximated as

$$R_D \approx \rho \frac{\sqrt{Dcg^2 + W_D^2}}{A_D}. \quad (2.13)$$

When the variation of Dcg parameter is larger than the variation of effective turn-on area in the parasitic lateral BJT, the NMOS with larger Dcg parameter has a larger sheet resistance in the NMOS under ESD stress. On the other hand, because the larger Dcg parameter can cause the larger turn-on area A_D and the less reverse-biased voltage drop of V_{CB} in the parasitic lateral BJT under ESD stress, the effective turn-on resistance (R_{BJT}) of the parasitic lateral BJT in (2.9) can be decreased by the larger Dcg parameter. So, the total turn-on resistances (R_{device}) of the NMOS with different Dcg parameters are similar to each other's, as that shown in Fig. 2.14. The turn-on resistances of the NMOS devices with Dcg of 1.5μm, 3μm, and 5μm are 3.89Ω, 4.06Ω, and 3.96Ω, respectively. But, the NMOS with larger Dcg parameter can sustain the higher ESD stress owing to the larger turn-on area A_D.

The dependence of the clearances from the drain/source contact to the poly-gate edge (Dcg and Scg) on the HBM ESD level of NMOS and PMOS devices is shown in Fig. 2.15(a) and Fig. 2.15(b), respectively. In this investigation, all of the layout style and other spacings are kept the same (W=200μm, Wf=50μm, L=0.8μm, and Sba=4μm), but only the Dcg and Scg are varied from 1 to 8 μm in the testchips. Both the NMOS and POMS are fabricated with the RPO layer to block the silicided diffusion on the drain and source regions. From the experimental results, the clearance variation on the Scg from 1 to 5 μm at the source region (with a fixed Dcg of 3μm at the drain region) only leads to a slight variation on the average ESD level from 3.3kV to 3.6kV (-2.1kV to -2.2kV) in the silicide-blocking NMOS (PMOS) device. But, the clearance variation on the Dcg from 1.5 to 8 μm at the drain region (with a fixed Scg of 1μm at the source region) can cause significantly improvement on the ESD level from 2.4kV to 3.4kV (-1.7kV to -3.4kV) in the silicide-blocking NMOS (PMOS) device. Therefore, the clearance of Dcg in both PMOS and NMOS devices for ESD protection is suggested greater than 3 μm to achieve better ESD robustness in this 0.35-μm CMOS process.

To further explain the effect of Dcg factor, the energy bands of NMOS with short or long Dcg are illustrated in Fig. 2.16(a) and Fig. 2.16(b), respectively. The energy band diagrams along the lines A-A' and B-B' in the device structure of NMOS devices with or without high positive ESD stresses are compared in Fig. 2.16(a) with a short Dcg and in Fig. 2.16(b) with a long Dcg. The shorter clearance of Dcg can induce a smaller sheet resistance in drain diffusion of the NMOS. If the sheet resistance is smaller enough, the drain voltage can easily lower the energy band in the region G of NMOS, as that shown in Fig. 2.16(a). So, the

turn-on stress current from drain is very closed to the channel surface. However the channel surface and gate oxide of the NMOS are easily damaged by the ESD stress because of the high current density in region G. If the NMOS has a longer clearance of Dcg in Fig. 2.16(b), the turn-on current can be away from the channel surface of the NMOS because of the larger sheet resistance in the drain diffusion. Therefore, the major ESD current can flow into the region S of the NMOS in Fig. 2.16(b). From afore mentioned discussion, the larger clearance of Dcg can cause the larger turn-on area in MOSFET. So, the MOSFET with larger Dcg has larger turn-on area for heat dissipation to sustain higher ESD current stress in the experimental results of Fig. 2.15. The source diffusions of MOSFET are connected with the bulk of MOSFET, only a little efficiency of the Scg clearance can change the turn-on path of the parasitic lateral BJT. Therefore, the Scg clearance has no obvious impact on the ESD robustness of MOSFET in Fig. 2.15.

2.2.4 Spacing from Drain Diffusion to Guardring Diffusion

The spacing from the drain diffusion to the substrate guardring diffusion in the finger-type layout also has an obvious impact on the ESD robustness of the NMOS and PMOS devices. This spacing has been illustrated in Fig. 2.2 and marked as “Sba”. In Fig. 2.2, the wider spacing Sba contributes a larger base resistance (R_B) to the parasitic lateral n-p-n (p-n-p) BJT in the NMOS (PMOS) device. The parasitic lateral BJT with a larger R_B makes itself to be triggered on more quickly and uniformly to bypass ESD current. The ESD levels of NMOS and PMOS devices with different Sba spacings but the fixed other layout spacings (W=200μm, L=0.8μm, Dcg=3μm, Scg=1μm, and Wf=50μm) are investigated in Fig. 2.17(a) and Fig. 2.17(b), respectively. When this Sba spacing is increased from 3μm to 5μm, the HBM ESD level of the NMOS (PMOS) is improved from 2.8kV to 3.6kV (from -1.7kV to -2.2kV). This investigation confirms the important effect of the layout spacing Sba on the ESD robustness of the ESD protection device. Because the larger Sba can enhance the turn-on uniformity of lateral BJT for full fingers in MOSFET, the MOSFET can sustain higher ESD current.

2.2.5 Unit-Finger Width

In the finger-type layout, a large-dimension device is traditionally drawn with multiple

fingers in a parallel connection. If the unit-finger width (Wf) of every finger is shorter, more fingers must be used to construct the same large-dimension device. The large-dimension device with different numbers of unit finger and unit-finger width can cause different ESD performances, even if the device has the same W and L dimensions. To verify this issue, both the NMOS and PMOS devices with the fixed channel width/length of 200μm/0.8μm but different unit-finger widths are fabricated in a 0.35-μm silicided CMOS process and investigated by the ESD tester. The tested results are shown in Fig. 2.18(a) and Fig. 2.18(b).

The MOSFET with different unit-finger width has different geometrical layout area. The different geometrical layout can cause the different turn-on area of parasitic lateral BJT in the MOSFET. In Fig. 2.4(k), the major turn-on current of parasitic lateral BJT is concentrated in the central region of the NMOS during current stress. The effective turn-on area ($A_{effective}$) of parasitic lateral BJT on the drain edge of MOSFET can be assumed and approximated as

$$A_{effective} \approx (Nf - \alpha)\cdot(Wf - \beta)\cdot\sqrt{(\gamma\cdot Dcg)^2 + [\delta\cdot(W_D + W_B')]^2}\ , \tag{2.14}$$

where α is a modified parameter of the finger number, which can be a decimal number, and β is a modified parameter of the unit-finger width in the MOSFET. The γ and δ are weight coefficients of effective turn-on area on the bottom and sideward of drain diffusion in the MOSFET for the turned-on parasitic lateral BJT. Because those devices with the same total channel width but different unit channel width have the same channel length (L) and clearance of Dcg, the turn-on position and area per unit-finger width are assumed to be fixed and be constant in the turned-on parasitic lateral BJT of MOSFET. To simply explain the unit-finger width effect, the parameters (α, β, γ, and δ) in (2.14) can be assumed as some suitable constants for NMOS or PMOS, which have been listed in Table 2.1. Because the MOSFET with more effective turn-on area ($A_{effective}$) has larger turn-on volume for the heat dissipation to sustain higher ESD current, the larger calculated turn-on area ($A_{effective}$) of the MOSFET in Table 2.1 can sustain the higher ESD stress. From the calculated effective turn-on areas ($A_{effective}$) of NMOS and PMOS devices with the same total channel width in Table 2.1, their variation completely match to the curve variation in Fig. 2.18(a) and Fig. 2.18(b).

From the experimental results, the ESD level of the NMOS with W=200μm is deceased from 3kV to 2.7kV, while the NMOS is drawn with the finger number from 2 to 8 in the 0.35-μm silicided CMOS process. On the contrary, the PMOS drawn with 4 fingers leads to a slight higher ESD robustness.

2.3 SUMMARY

The dependence of layout spacings on the ESD robustness of CMOS devices in silicided CMOS process has been detailedly investigated and discussed. The device with a shorter channel length, a wider channel width, a larger clearance from drain contact to the poly-gate edge, and a wider spacing from the drain diffusion to the guardring diffusion generally leads to a higher ESD robustness. But, the channel length effect isn't an independent condition on the ESD robustness of protection device. From the proposed analysis, the clearance from drain contact to the poly-gate edge can affect the channel length effect on the ESD robustness of protection device. To further explain the current distribution along the NMOS device structure under ESD stress, the energy band diagram is used in the literature to clearly describe the dependence of ESD robustness on device layout parameters. From the explication of energy band diagrams, the larger channel current and smaller turn-on area of parasitic lateral BJT can cause the damage of MOSFET under ESD stress. This effect causes the degradation of ESD robustness in MOSFET's. The optimized layout parameters can be verified to control the turn-on efficiency of parasitic lateral BJT and improve the ESD robustness of MOSFET.

Table 2.1
The device parameters and calculated effective total turn-on area of NMOS and PMOS with the same total channel width (W=200μm) in equation (2.14).

NMOS									
α	β	γ	δ	Nf	Wf (μm)	Dcg (μm)	W_D (μm)	W_B' (μm)	$A_{effective}(\mu m^2)$
0.18	8	0.7	0.4	8	25	3	0.02	0.6	281.11
0.18	8	0.7	0.4	4	50	3	0.02	0.6	339.27
0.18	8	0.7	0.4	2	100	3	0.02	0.6	354.07
PMOS									
α	β	γ	δ	Nf	Wf (μm)	Dcg(μm)	W_D (μm)	W_B' (μm)	$A_{effective}(\mu m^2)$
0.18	2	0.8	0.1	8	25	3	0.02	0.5	431.77
0.18	2	0.8	0.1	4	50	3	0.02	0.5	440.17
0.18	2	0.8	0.1	2	100	3	0.02	0.5	428.16

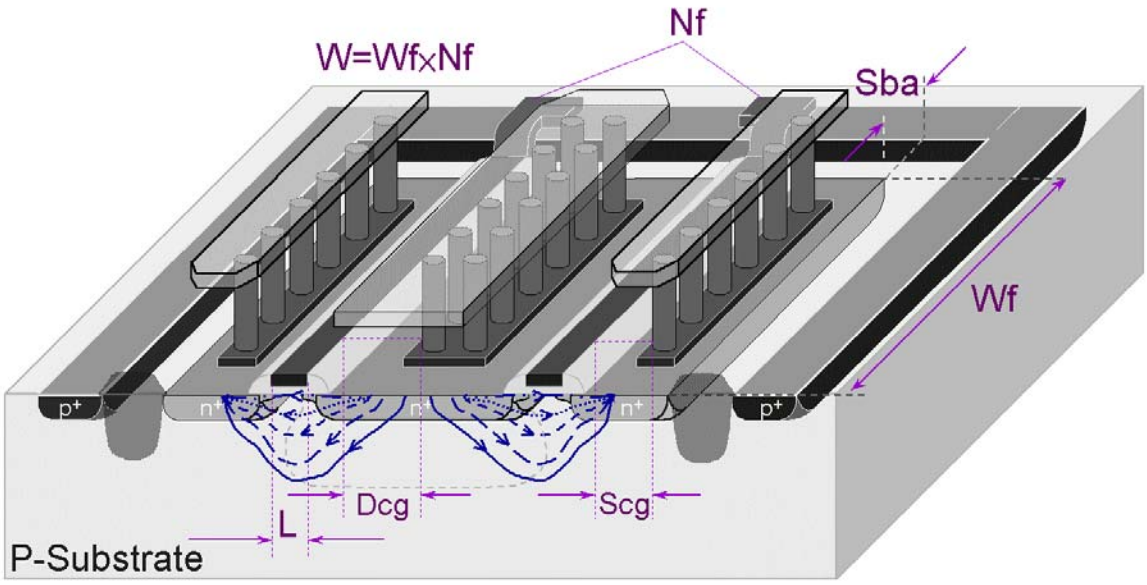


Fig. 2.1 3-D structure of finger-type NMOS device with layout parameters.

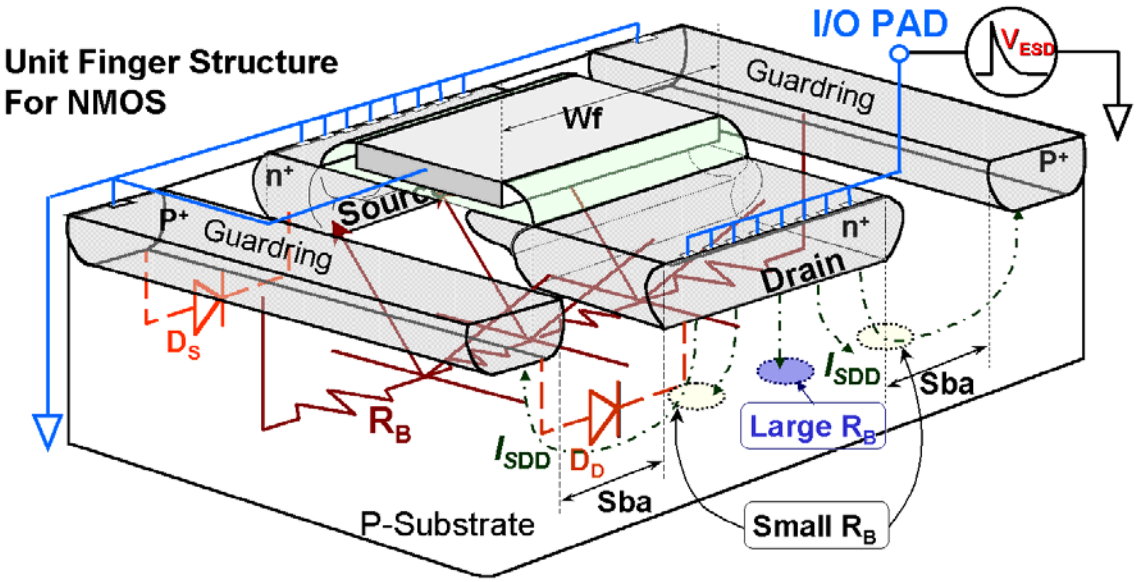


Fig. 2.2 Illustration of the parasitic devices and layout parameters in a unit-finger structure of a multiple-finger NMOS.

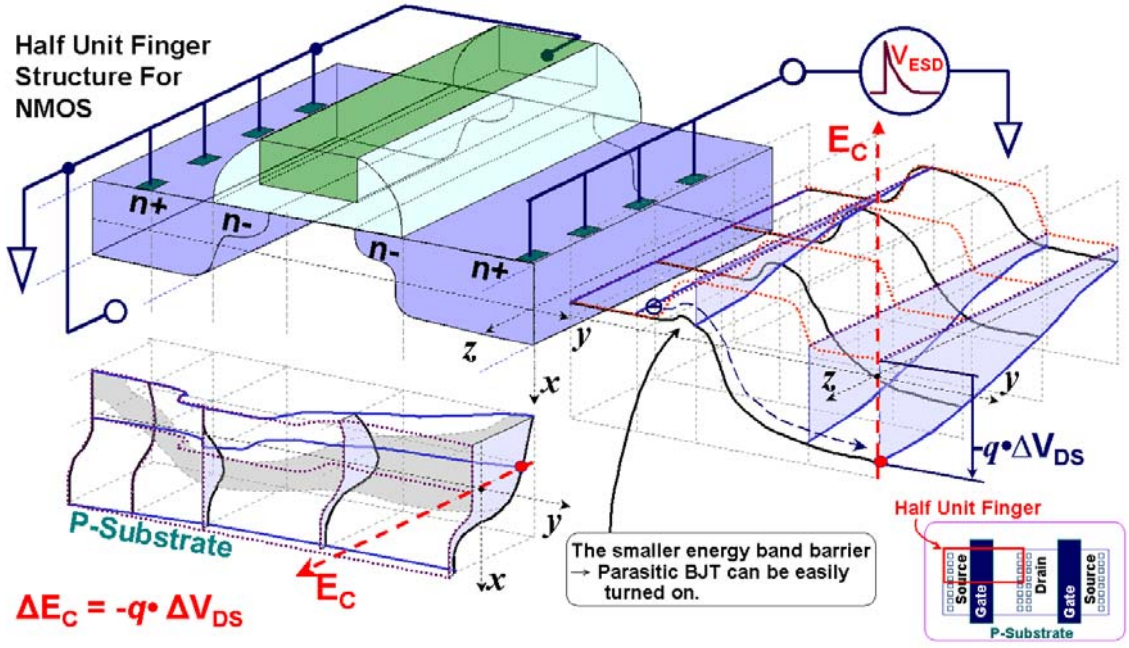


Fig. 2.3 Analysis of conduction energy band diagrams for a half unit-finger NMOS during positive ESD stress.

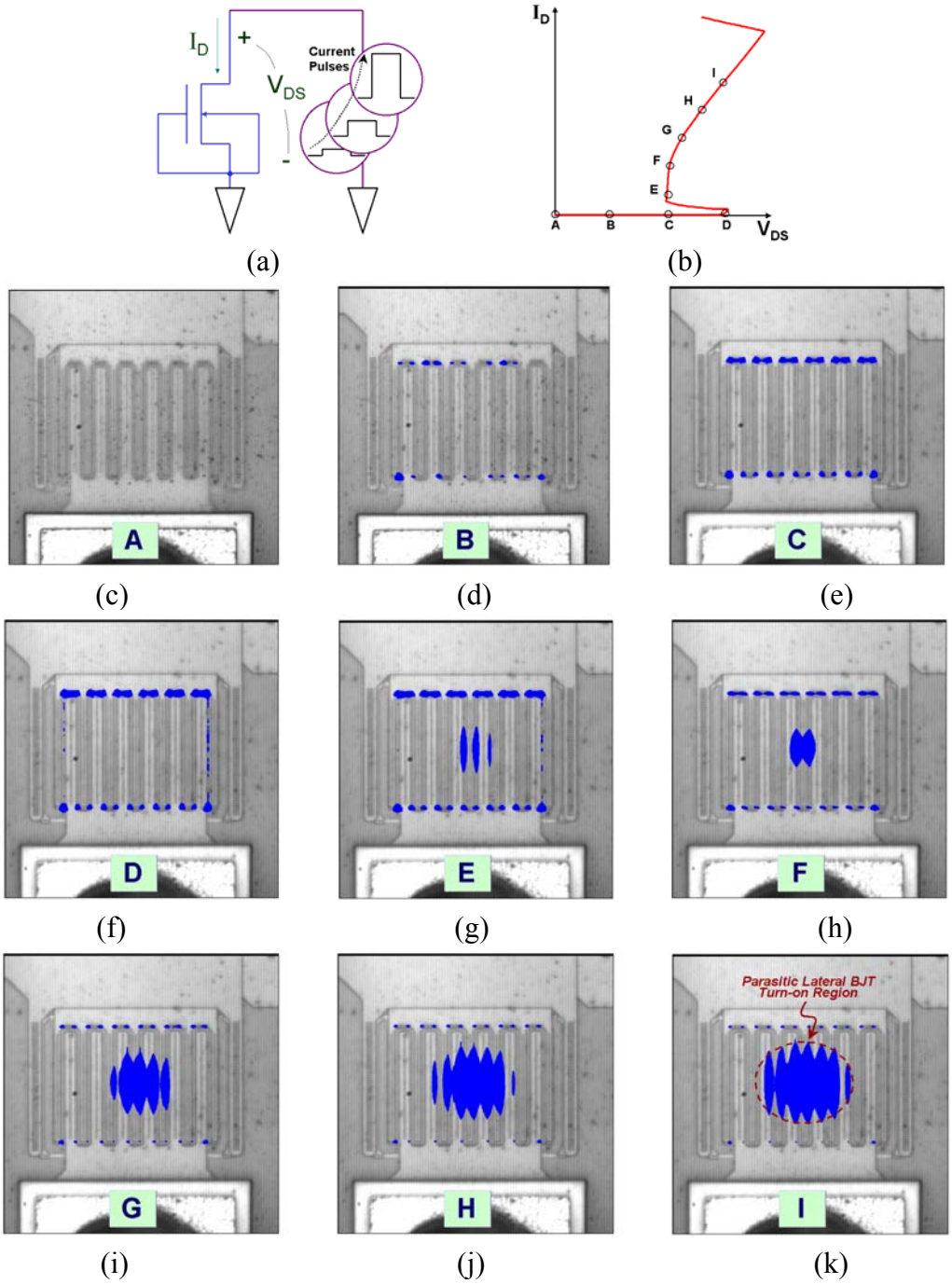
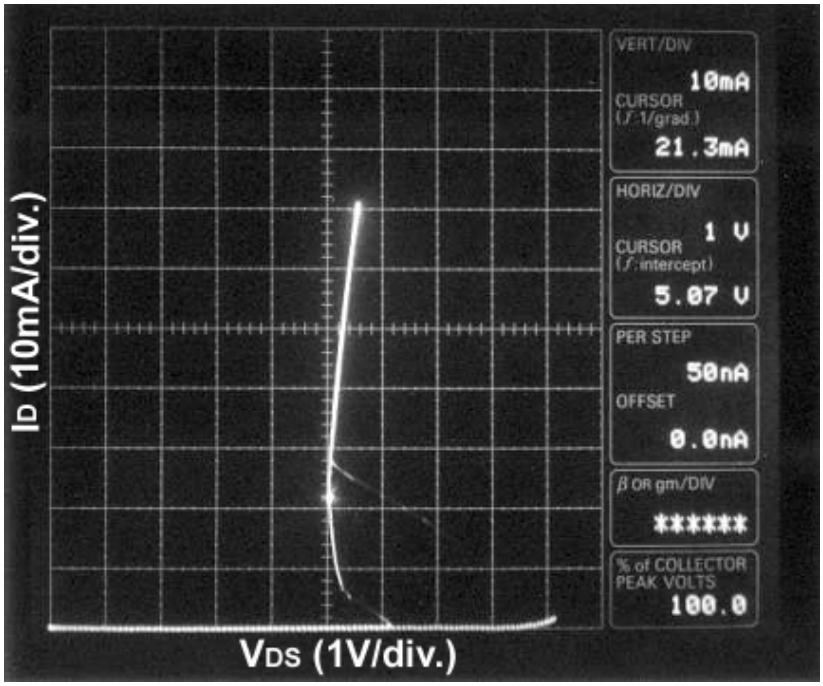
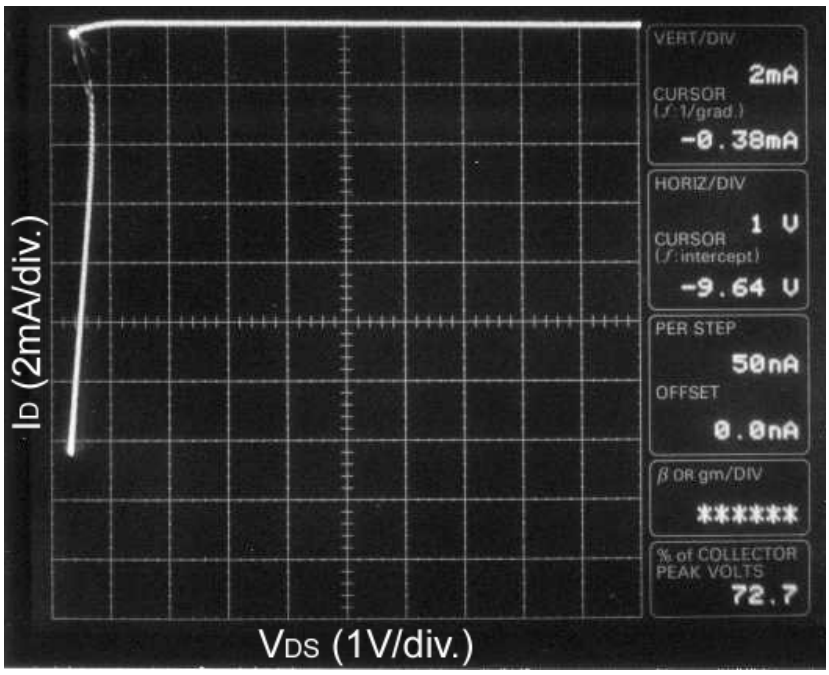


Fig. 2.4 The EMMI photographs on a gate-ground NMOS (W/L = 300μm/0.5μm) to observe its turn-on behavior under the stress of different pulsed currents. (a) The measurement setup, (b) the corresponding I-V curve of a gate-grounded NMOS, (c)-(f) the hot spots in the gate-grounded NMOS before it enters into snapback region, and (g)-(k) the hot spots in the gate-grounded NMOS after it enters into snapback region.



(a)



(b)

Fig. 2.5 The measured snapback I-V curves of (a) NMOS, and (b) PMOS, with a channel length of 0.35μm.

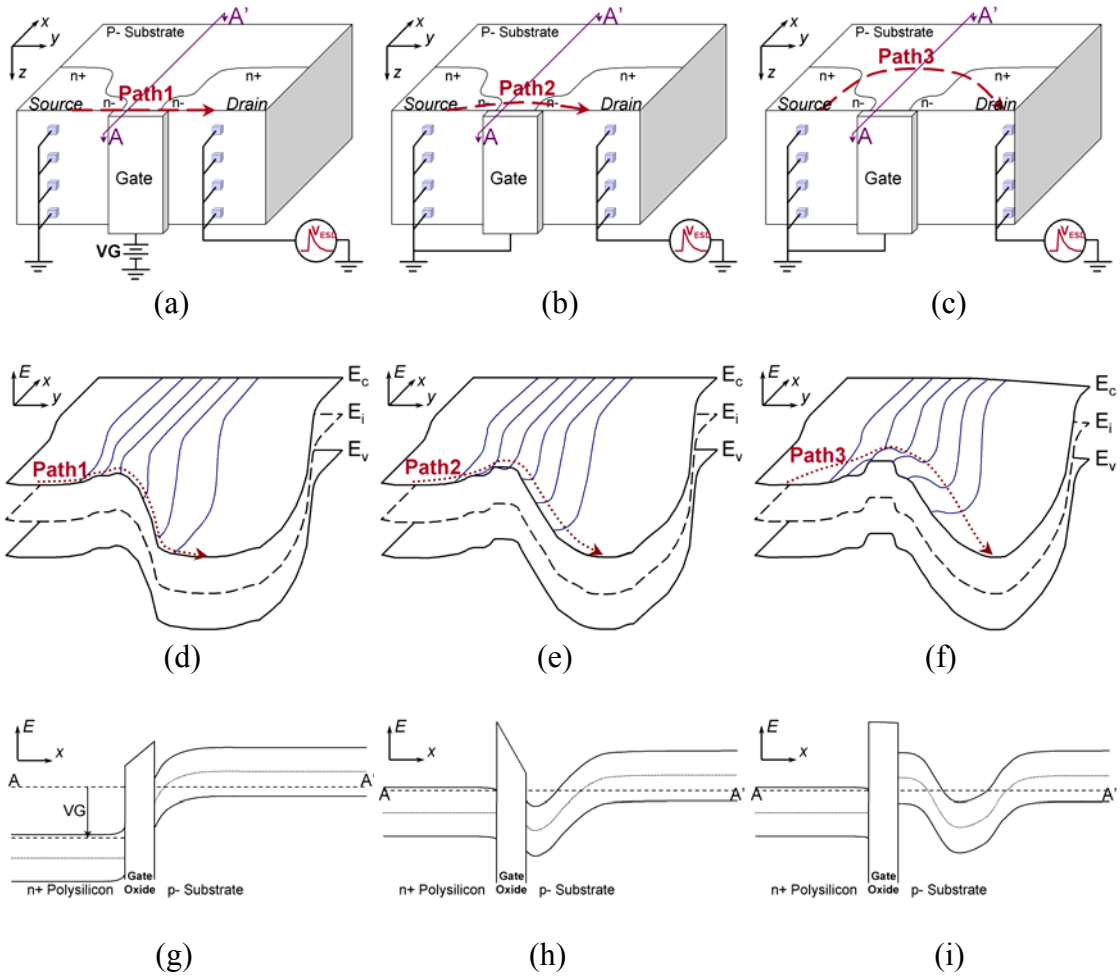


Fig. 2.6 Illustrations of energy band diagram for a non-silicided NMOS with different stress conditions. (a), (b), and (c) show devices under different biases. (d), (e), and (f) show two-dimension band diagrams of NMOS in the corresponding conditions of (a), (b), and (c), respectively. (g), (h), and (i) show the x-axis band diagrams along the line A-A' of NMOS in (a), (b), and (c), respectively. A gate voltage of VG is applied on the gate of NMOS in (a).

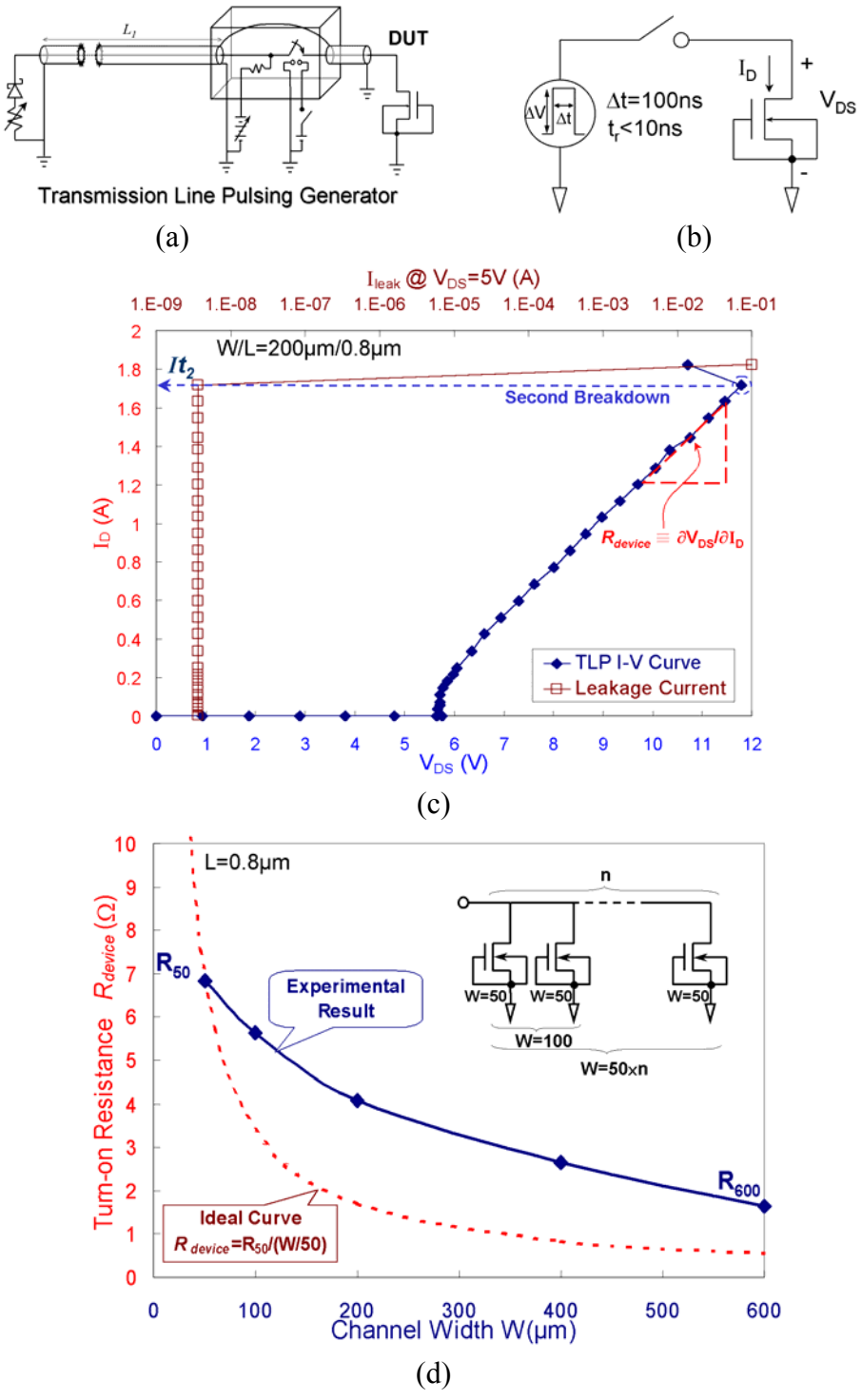
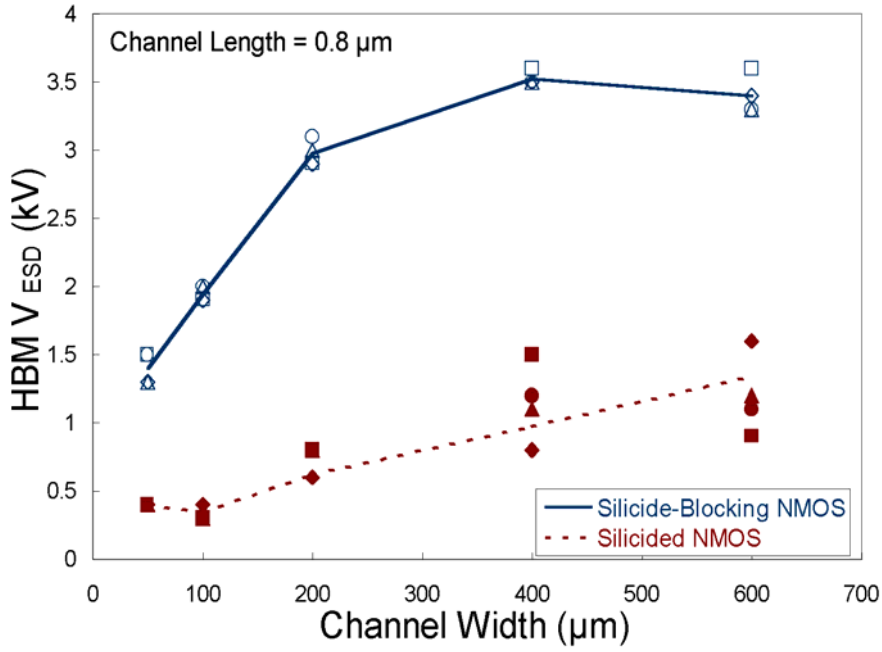
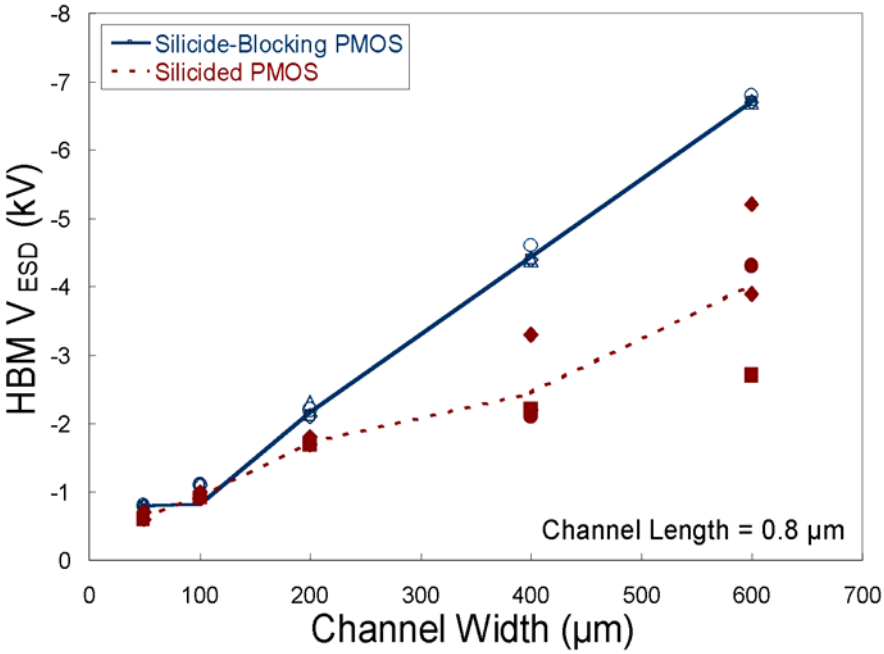


Fig. 2.7 (a) Illustration of transmission line pulsing generator (TLPG). (b) The corresponding circuit for TLPG measurement on a gate-grounded NMOS. (c) The measured I-V characteristics and leakage currents of NMOS by TLP with a pulse width of 100 ns. (d) The turn-on resistances of finger-type NMOS devices with different channel widths, but with the same unit-finger width and channel length.



(a)



(b)

Fig. 2.8 The dependence of HBM ESD level on the channel width of (a) NMOS, and (b) PMOS, with or without silicided diffusion.

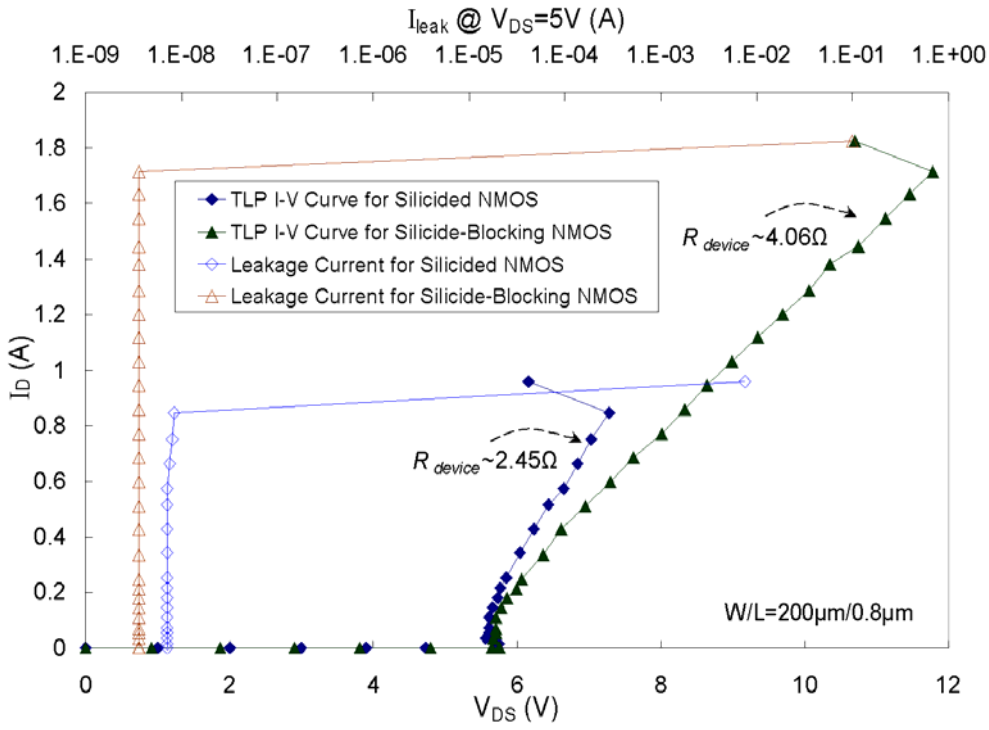


Fig. 2.9 TLP measured I-V curves of NMOS devices with or without silicided diffusion, but with the same device dimension of W/L=200μm/0.8μm.

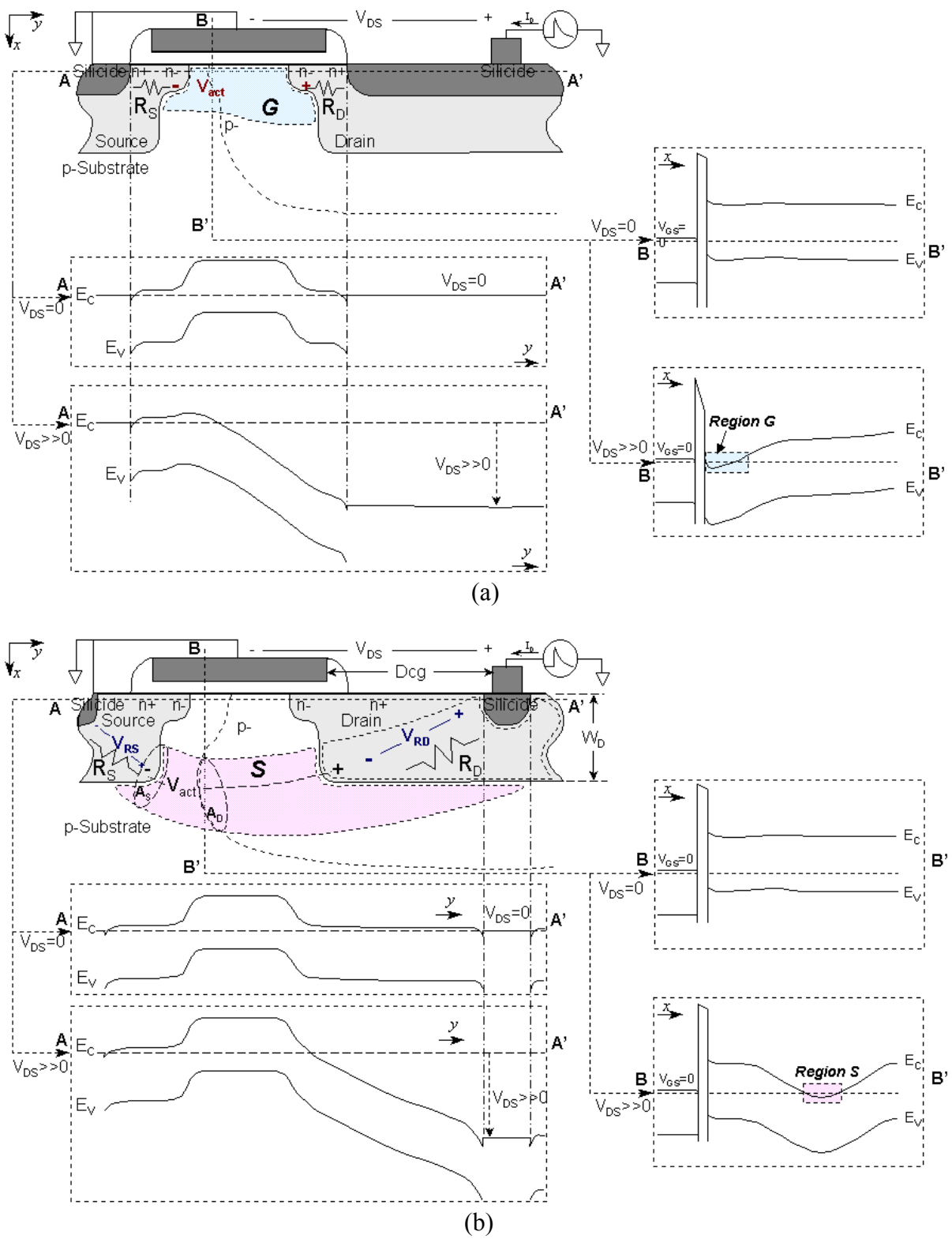


Fig. 2.10 Illustration of the variation on energy band of gate-grounded NMOS (a) with, and (b) without, silicided diffusion.

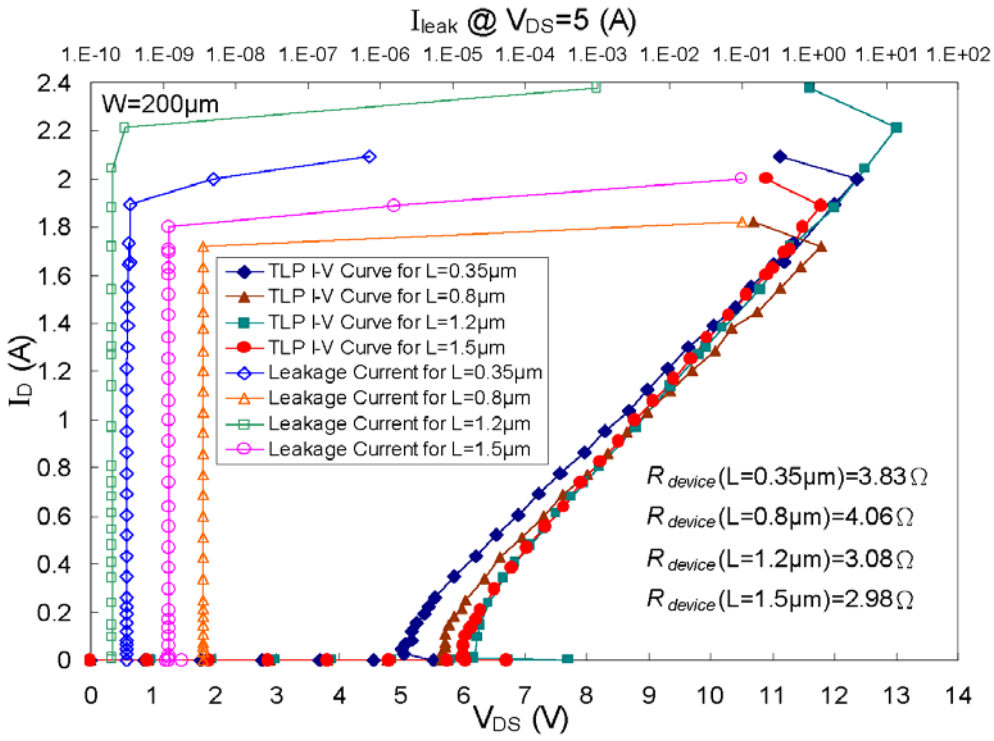
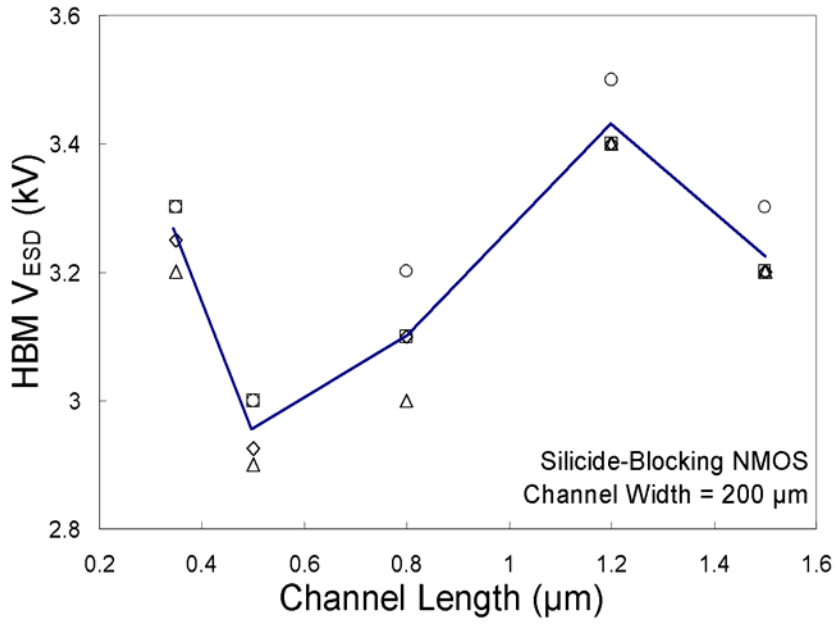
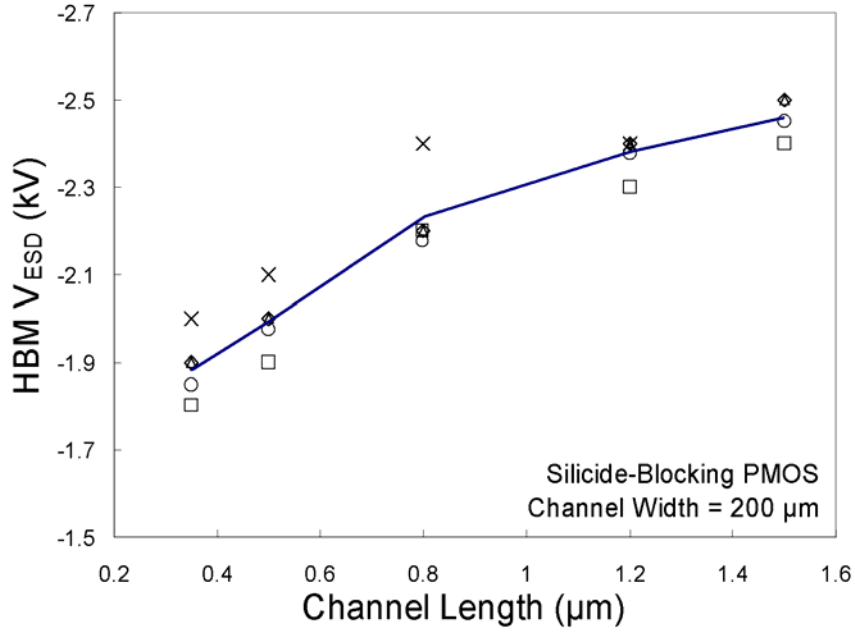


Fig. 2.11 TLP measured results for gate-grounded NMOS devices with different channel lengths (L=0.35μm, 0.8μm, 1.2μm, and 1.5μm).

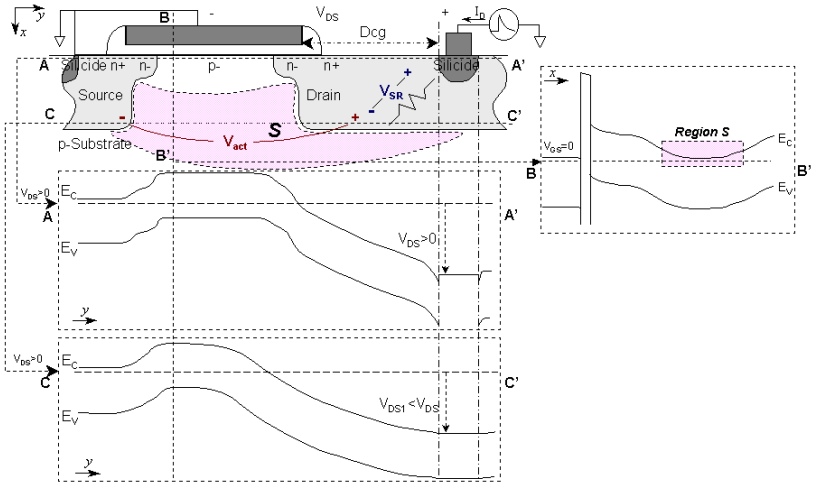


(a)

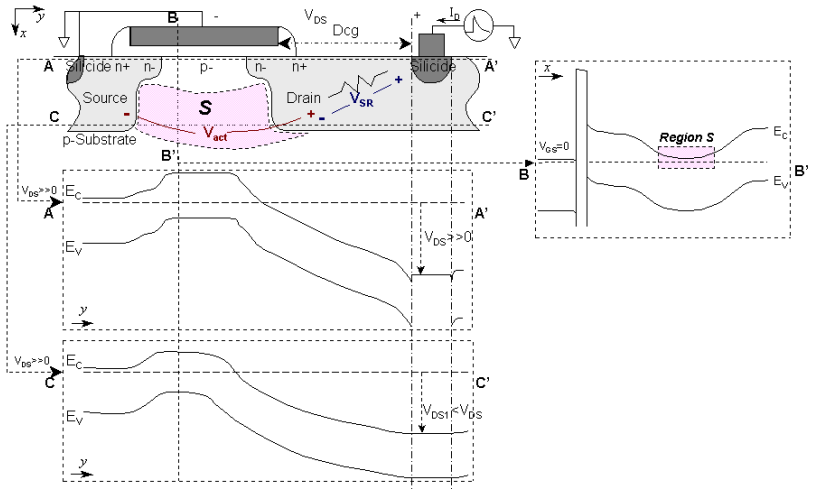


(b)

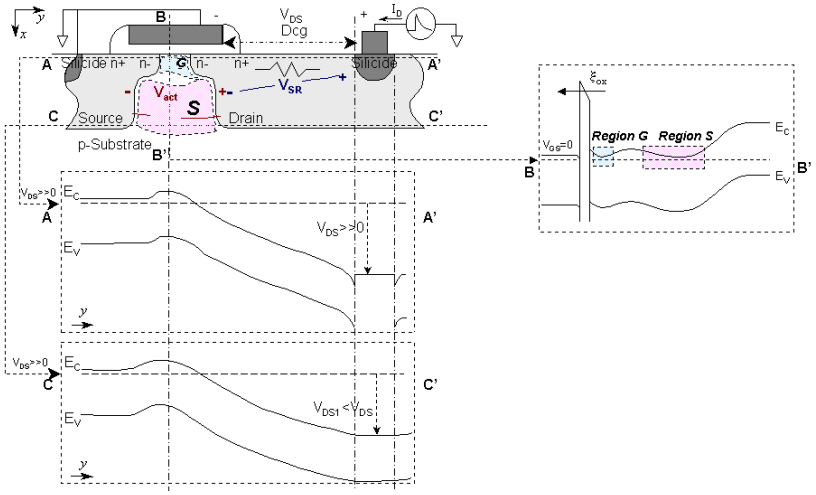
Fig. 2.12 The dependence of HBM ESD level on the channel length of (a) NMOS, and (b) PMOS, with a fixed channel width of 200μm.



(a)



(b)



(c)

Fig. 2.13 Illustration of the variation on energy band of gate-grounded NMOS with (a) long, (b) normal, and (c) short, channel lengths.

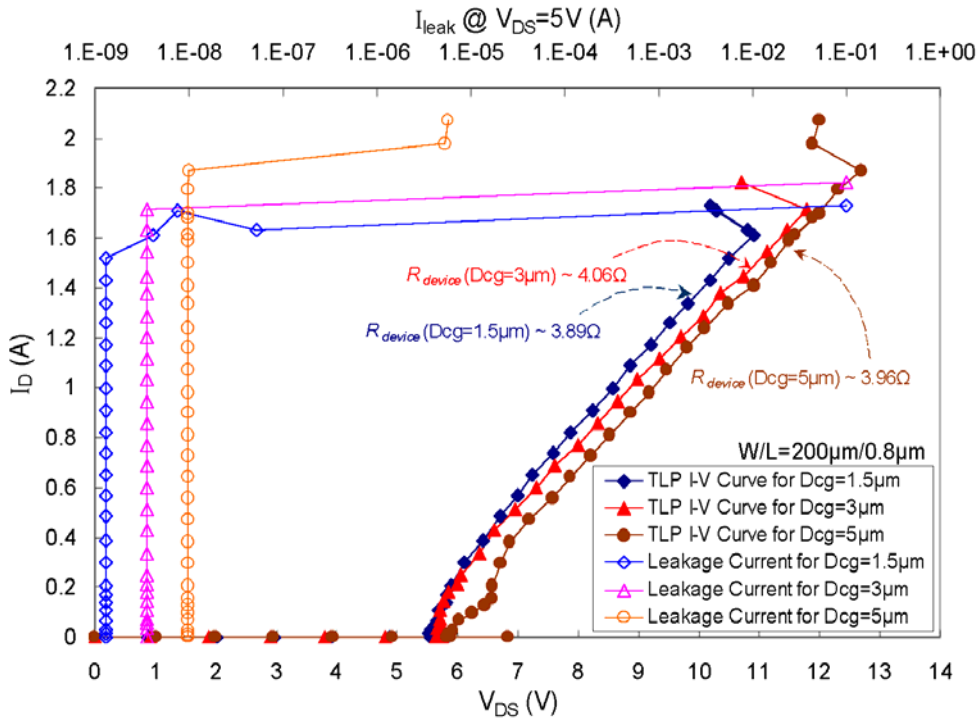
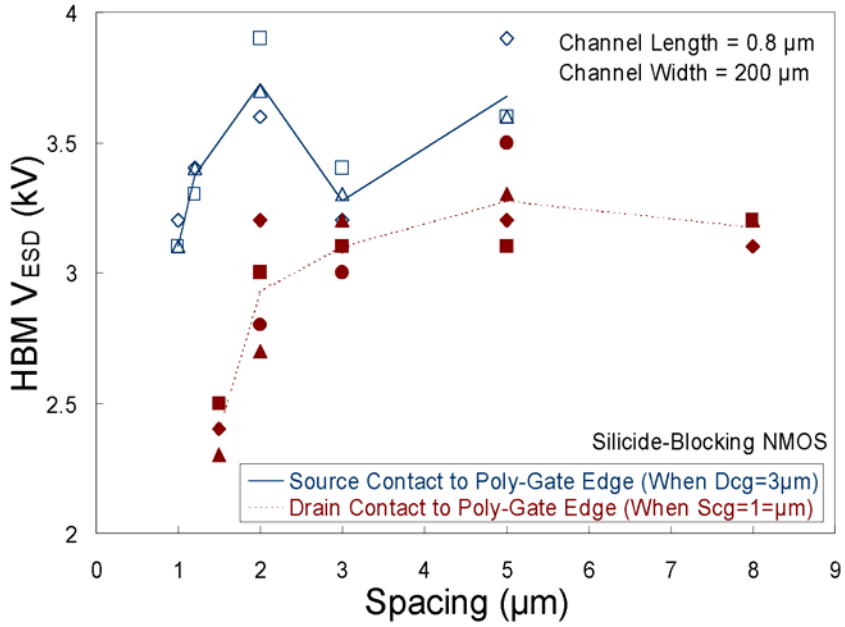
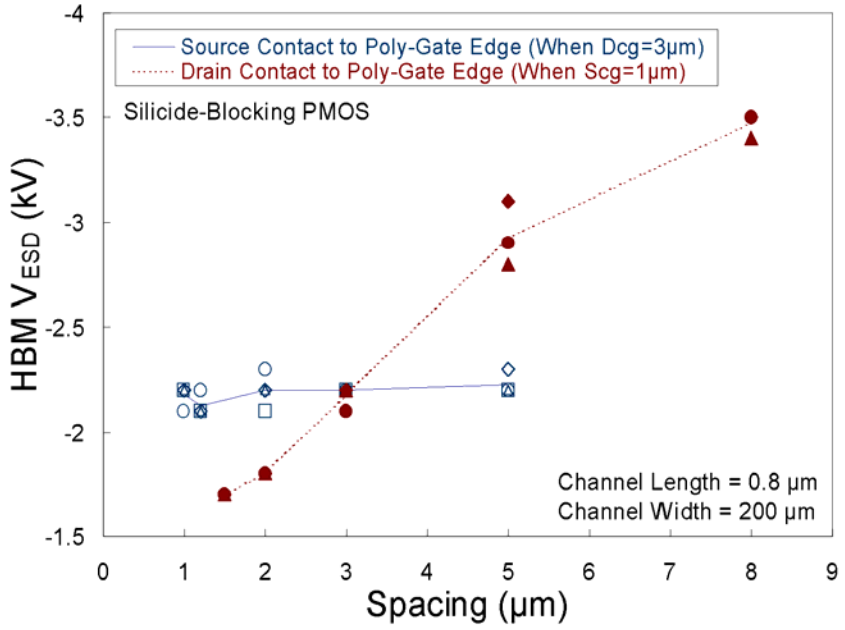


Fig. 2.14 TLP measured I-V curves for NMOS devices with different Dcg parameters (Dcg = 1.5μm, 3μm, and 5μm).



(a)



(b)

Fig. 2.15 The dependences of HBM ESD level on the clearance from the drain/source contact to poly-gate edge of silicide-blocking (a) NMOS, and (b) PMOS.

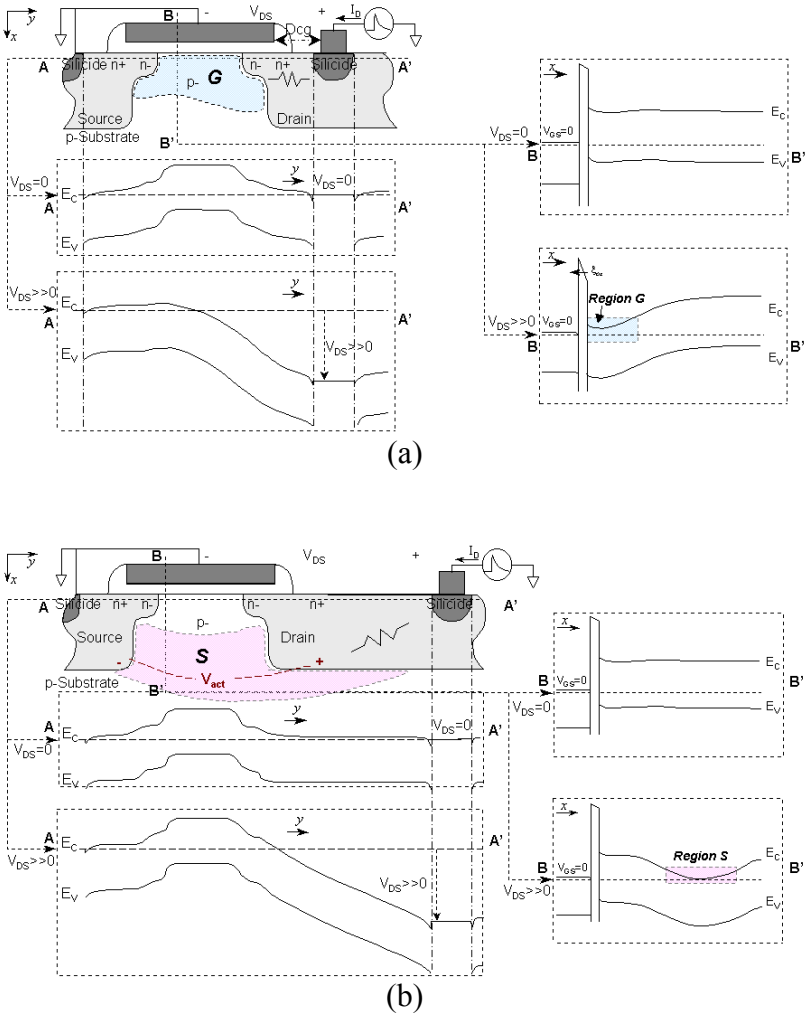
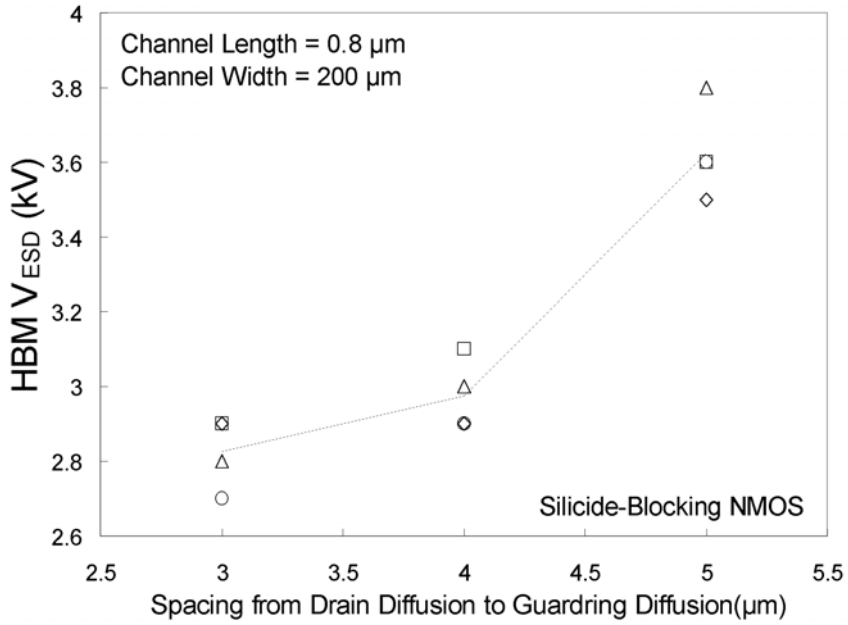
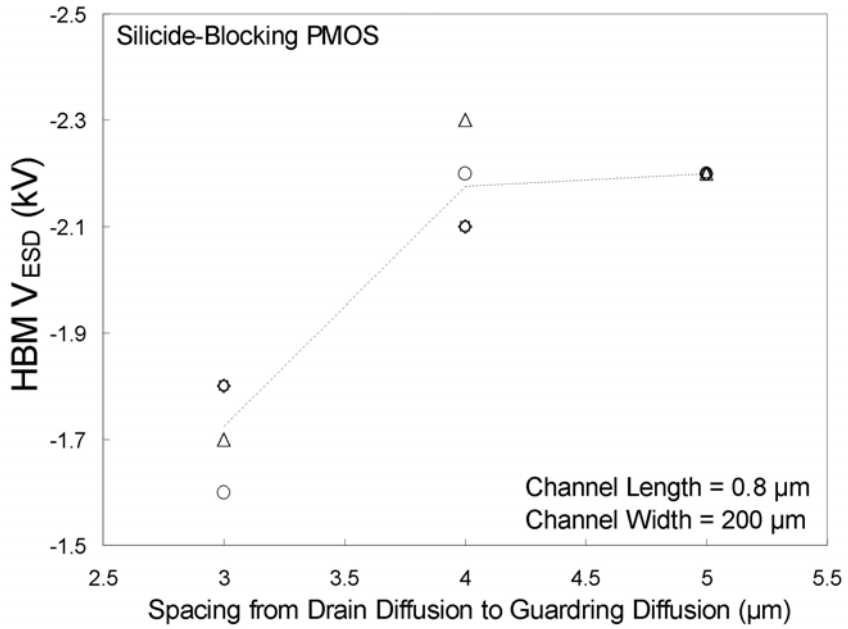


Fig. 2.16 Illustration of the variation on energy band of gate-grounded NMOS with (a) small and (b) long, clearance of contact to poly-gate edge (Dcg).

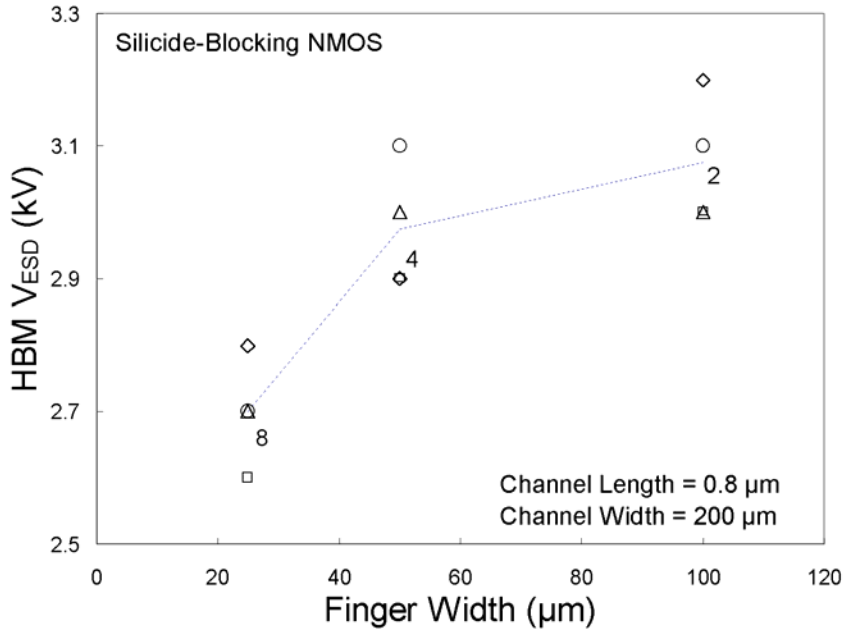


(a)

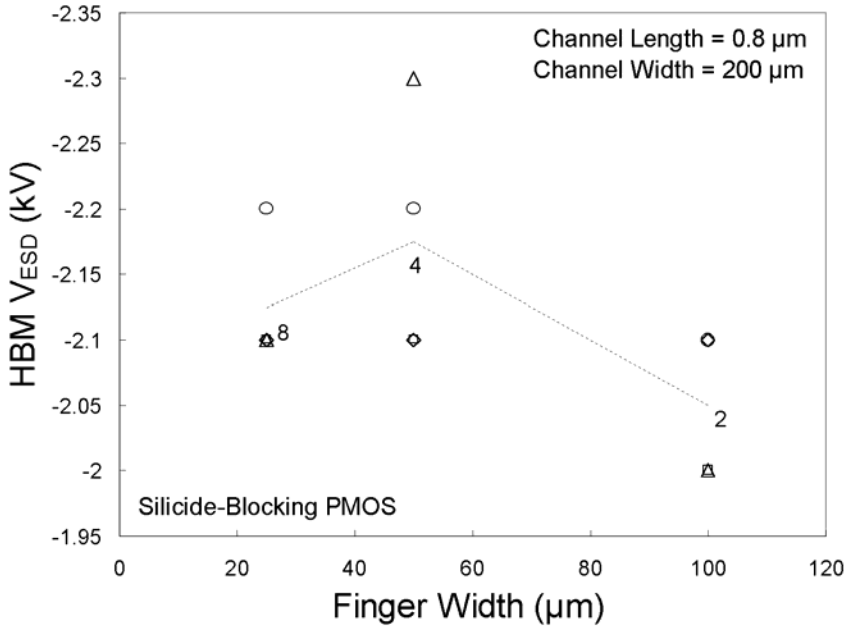


(b)

Fig. 2.17 The dependence of HBM ESD robustness on the Sba spacings of (a) NMOS, and (b) PMOS.



(a)



(b)

Fig. 2.18 The dependence of HBM ESD robustness on the finger width and finger number of (a) NMOS, and (b) PMOS, with W/L=200μm/0.8μm in the finger-type layout.

CHAPTER 3

GATE-DRIVEN EFFECT VERSUS SUBSTRATE-TRIGGERED EFFECT

In this chapter, the gate-driven and the substrate-triggered designs used in the ESD protection circuits are investigated in more details. To clearly understand the physical mechanisms on ESD current distribution in the device, TLP measured I-V curves, energy band diagram, and the EMMI photographs are used to explain the current distribution along MOSFET under the gate-grounded, gate-driven, or substrate-triggered designs. In the literature, the energy band analysis is first used in this paper to explain the ESD robustness of CMOS devices under ESD stress. The substrate-triggered design has been confirmed to be a good choice to improve ESD robustness of CMOS devices in sub-quarter-micron CMOS technologies.

3.1 GATE-DRIVEN EFFECT

To improve ESD robustness of the ESD protection devices, the gate-driven design had been reported to uniformly trigger on the multiple fingers of the large-dimension NMOS. But, the coupled voltage on the gate of NMOS also turn on the strong-inversion channel of the NMOS, therefore the ESD current is discharging through the channel region of the ESD protection NMOS. Due to the shallower junction depths and the LDD structure at the drain/source regions, the turned-on NMOS is weak to ESD stress [100].

3.1.1 Turn-on Mechanism of Gate-Driven Effect

To clearly explain the gate bias effect, the energy band diagrams of NMOS with different gate biases (V_{GS}=0, V_{GS}>0, V_{GS}>>0, and V_{GS}>>>0) are illustrated in Fig. 3.1. The same positive ESD stress is applied on the drain of NMOS for each case. The cross-sectional view of NMOS device is shown in Fig. 3.1(a). Energy bands along the lines A-A', B-B', and

C-C' of the NMOS in Fig. 3.1(a) are analyzed with the different gate biases, which are shown in Fig. 3.1(b) with V_G=0, in Fig. 3.1(c) with V_G>0, in Fig. 3.1(d) with V_G>>0, and in Fig. 3.1(e) with V_G>>>0, respectively. In the V_{GS}=0 case. There is no coupled voltage on the gate of NMOS. The ESD current is discharged through the region S of the NMOS in Fig. 3.1(b). When the V_{GS} is increased by an external gate bias, the energy band of the channel surface in NMOS can be lowered by the gate bias (V_{GS}). If the gate bias is increased larger enough, channel current can be formed by accumulation charges in the region G of Fig. 3.1(c). Therefore, the ESD current is discharged through the region G and the region S' in Fig. 3.1(c). So, the gate-driven NMOS has two current paths to discharge the ESD current. If the gate bias is continually increased, the discharge regions G and S' will be extended and combined together as the merged region GS" in Fig. 3.1(d). Then, the gate-driven ESD protection devices can sustain higher ESD robustness. But the turn-on mechanism depends on the impurities doping profiles in the region GS" of NMOS in Fig. 3.1(d). When a larger gate bias is applied on the gate of the NMOS, the more ESD current is concentrated into the turn-on surface region in Fig. 3.1(e), where the larger electric field is built across on the gate oxide.

To observe the turn-on behavior of gate-driven device, the gate of NMOS is biased with a power supply and an increased current pulse is applied to its drain, as that shown in Fig. 3.2(a). The corresponding I-V curve of a gate-driven NMOS can be drawn in Fig. 3.2(b). The EMMI photographs of the gate-driven NMOS with different stressed current pulses are shown in Figs. 3.2(c)~3.2(e). From the hot spots in Figs. 3.2(c)~3.2(e), the channels of all fingers can be uniformly turned on under any current pulse stress. But only some parasitic lateral BJT's in the central regions can be turned on during high current pulse stress, as that shown in Fig. 3.2(e). From the investigation of the EMMI photographs, the gate-driven technique can uniformly turn on the channel current but it cannot enhance the turn-on uniformity of parasitic lateral BJT's in MOSFET.

To further discuss the gate-driven effect, the electric field (ξ_{ox}) across the gate oxide of MOSFET is increased by the accumulation charges and gate bias (V_{GS}), as that shown in Fig. 3.1(d) and Fig. 3.1(e). The high electric field can easily destroy the gate oxide and damage the channel surface of MOSFET. On the other hand, the doping profile of impurities under the gate oxide is an important factor to affect the quantities of channel current and the turn-on area of lateral BJT. If the doping profiles of impurities are adjusted, the gate-driven design can be further optimized for ESD protection. For another issue in the gate-driven design, coupled voltage on the gate of ESD protection device must be limited to avoid damaging the

gate oxide and surface channel of MOSFET.

3.1.2 Experimental Results

To investigate this gate-driven effect, the sub-circuit inserted in Fig. 3.3 is used to measure ESD levels of the NMOS and PMOS under different gate biases. The layout parameters of NMOS and PMOS are the same as the data shown in Section III, but the gates of MOSFET's are biased at different voltage levels. The different gate biases are applied to the gate of MOSFET, and ESD voltage zaps into the drain of MOSFET. In the 0.35-μm CMOS process, the HBM ESD levels on both the NMOS and PMOS devices with different channel widths (W) are shown in Fig. 3.3(a) and Fig. 3.3(b), respectively. The ESD level of the NMOS with W=600μm is initially increased while the gate bias increases from 0V to 4V. But, the ESD level is suddenly decreased while the gate bias is greater than 6V (8.5V) for NMOS with the channel width of 200μm (600μm), as that shown in Fig. 3.3(a). There is a similar gate-driven effect on the PMOS device. In Fig. 3.3(b), the ESD level (in absolute value) of the PMOS with W=600μm is initially increased while the gate bias changes from 0V to -5V. But, the ESD level is suddenly decreased while the gate bias is lower than -5V. When the gate bias is increased up to some critical value, the ESD level of NMOS or PMOS is suddenly decreased.

In a 0.18-μm salicided CMOS process, the TLP measured I-V characteristics of gate-driven NMOS (W/L=300μm/0.3μm) with 0V, 0.1V, and 1.1V gate biases are shown in Fig. 3.4. From the experimental results in Fig. 3.4, the turn-on resistance is decreased from 3.8Ω to 2.86Ω when the gate bias is changed from 0V to 0.1V. But, the turn-on resistance is increased from 2.86Ω to 3.26Ω when the gate bias is increased from 0.1V to 1.1V. In the 0.18-μm salicided CMOS process, the dependences of second breakdown currents on the gate biases of NMOS with different channel widths are shown in Fig. 3.5. The second breakdown current of NMOS with W=300μm is initially increased from 0.69A to 1.03A while the gate bias increases from 0V to 0.3V. But the It_2 is suddenly decreased in Fig. 3.5 while the gate bias is only greater than 0.2V (0.3V) for NMOS with 100-μm (600-μm) channel width. Because only a very small voltage on the gate of NMOS can degrade the ESD robustness of NMOS, the gate-driven technique is hardly designed for ESD protection in the 0.18-μm salicided CMOS process.

From the TLP measured I-V curves in Fig. 3.4, the increase of lower gate-driven

voltage on the NMOS can decrease the turn-on resistance of the NMOS during the TLP measurement. But, the higher gate bias causes an increase on the turn-on resistance of NMOS. These imply that the higher gate bias will concentrate the ESD current at a smaller turn-on region in the channel surface of NMOS and build a very high electric field across on the gate-oxide. From the measured results in Fig. 3.3 and Fig. 3.5, the gate-coupled circuit used to improve ESD robustness of the ESD protection devices must be correctly optimized to avoid the sudden degradation on the ESD level of the gate-driven ESD protection devices.

3.2 SUBSTRATE-TRIGGERED EFFECT

To avoid the sudden degradation on ESD level of the gate-driven devices, the substrate-triggered design had been proposed to improve ESD robustness of the ESD protection devices.

3.2.1 Turn-on Mechanism of Substrate-Triggered Effect

To explain the effect of substrate-triggered design, the energy band diagrams with different substrate-triggered biases (V_{BS}=0, V_{BS}>0, and V_{BS}>>0) under the same positive ESD stress are shown in Fig. 3.6. The energy band diagrams along the lines A-A', B-B', and C-C' in Fig. 3.6(a) are analyzed in Fig. 3.6(b) with V_{BS}=0, in Fig. 3.6(c) with V_{BS}>0, and in Fig. 3.6(d) with V_{BS}>>0. Comparing to the gate-driven design, there is no gate bias to lower the energy bands on the surface channel of the substrate-triggered NMOS as shown in Fig. 3.6(c) and Fig. 3.6(d). In Fig. 3.6(b), there is no substrate bias on the NMOS, so the current distribution region S of the parasitic lateral BJT in NMOS is smaller than those regions S' and S" of the substrate-triggered devices in Fig. 3.6(c) and Fig. 3.6(d). The substrate bias can lower the energy bands in the substrate region and extend the current distribution from the region S in Fig. 3.6(b) to the region S' in Fig. 3.6(c) or the region S" in Fig. 3.6(d). The device with substrate-triggered design has more and wider current distribution region in its device structure. Therefore, the device with higher substrate-triggered bias has the more space for heat dissipation to sustain higher ESD stress. Therefore, substrate-triggered devices can sustain higher ESD robustness. From above explication, the turned-on region of parasitic lateral BJT can be extended into more area and be far away from the channel surface by the

substrate bias in MOSFET. Therefore, the ESD protection devices with substrate-triggered design can have much higher ESD robustness in general CMOS technologies.

To verify the turn-on behavior of substrate-triggered device, the substrate of NMOS is biased with a power supply and an increased current pulse is applied to its drain, as that shown in Fig. 3.7(a). The corresponding I-V curve of a substrate-triggered NMOS is drawn in Fig. 3.7(b). The EMMI photographs of the substrate-triggered NMOS under different current pulses are shown in Figs. 3.7(c)~3.7(e). From the hot spots in Figs. 3.7(c)~3.7(e), the parasitic lateral BJT's of all fingers in NMOS can be uniformly turned on under any current pulse stress. All fingers of NMOS can be magnificently turned on during high current pulse stress in Fig. 3.7(e). So, substrate-triggered technique can uniformly turn on the parasitic lateral BJT's in MOSFET during ESD stress.

3.2.2 Experimental Results

To investigate the substrate-triggered effect on ESD robustness of NMOS, different substrate currents are applied to the substrate of NMOS, and ESD current zaps into the drain of NMOS. The HBM ESD levels of the substrate-triggered NMOS in a 0.35-μm silicided CMOS process are shown in Fig. 3.8(a) and Fig. 3.8(b) with different channel widths and lengths. The inserted sub-circuit shows the experimental setup to measure the substrate-triggered effect. In Fig. 3.8(a), the ESD level of the NMOS with a device dimension of W=400μm and L=0.8μm can be significantly increased from 3.5kV to greater than 8kV while the substrate current increases from 0mA to 2.8mA. In Fig. 3.8(b), the NMOS device (W=200μm) with a shorter channel length and higher substrate current can sustain a much higher ESD level. The ESD level of the NMOS with a channel length of 0.5μm under 0-V gate bias and 0-A substrate current is only 2.8kV, but the ESD level is increased up to 4.4kV while the NMOS has a substrate current of 4mA. As shown in Fig. 3.8, the ESD level is continually improved while the substrate current increases up to 4mA.

In a 0.18-μm salicided CMOS process, the TLP measured I-V characteristics of substrate-triggered NMOS (W/L=300μm/0.3μm) with 0mA, 2mA, and 8mA substrate currents are shown in Fig. 3.9. From the experimental results in Fig. 3.9, the turn-on resistance is continually decreased from 3.92Ω to 2.73Ω while the substrate current is changed from 0mA to 8mA. The substrate current can change the turn-on resistance of NMOS during ESD stress. It implies that substrate current can change the turn-on area or

turn-on path of parasitic lateral BJT in the NMOS to sustain higher ESD stress. The dependence of It_2 on substrate current on the NMOS devices with different channel widths in a 0.18-μm salicided CMOS process are shown in Fig. 3.10. The second breakdown currents of NMOS with both W=300μm and W=100μm can be continually increased during high current pulse stress. The second breakdown current (It_2) of the NMOS with a channel width of 300μm under a 0-mA substrate current is only 0.8A, but it is increased up to 2.2A while the NMOS has a substrate current of 4mA.

The substrate-triggered design can effectively improve ESD robustness of the ESD protection devices without the sudden degradation as that shown in the gate-driven design. Therefore, this substrate-triggered design is more suitable to improve ESD robustness of the ESD protection devices and circuits in the sub-quarter-micron CMOS technologies.

3.3 SUMMARY

The gate-grounded large-dimension ESD protection devices have been proved that they cannot be uniformly turn on during ESD stress to sustain high ESD level as expectation in chapter 2. The gate-driven and substrate-triggered techniques can improve the ESD robustness of the large-dimension ESD protection devices. But, the higher gate bias can induce larger channel current and higher electric field across gate oxide to damage MOSFET from the explication of energy band diagrams. This effect causes the degradation of ESD robustness in gate-driven devices. Comparing to the gate-driven design, the substrate-triggered design can avoid the forming of channel current and enhance the space-charge region to sustain higher ESD current far away from the channel surface. From energy band analysis, substrate-triggered design can continually increase the turn-on area for heat dissipation. Therefore, substrate-triggered design can effectively improve ESD robustness of the ESD protection devices. From the experimental results, the gate-driven design has been confirmed to cause a sudden degradation on ESD robustness of the ESD protection devices. But, the substrate-triggered design can continually increase ESD robustness of the ESD protection devices. Therefore, the substrate-triggered design can be one of the most effective solutions to improve ESD robustness of CMOS devices in sub-quarter-micron CMOS technologies.

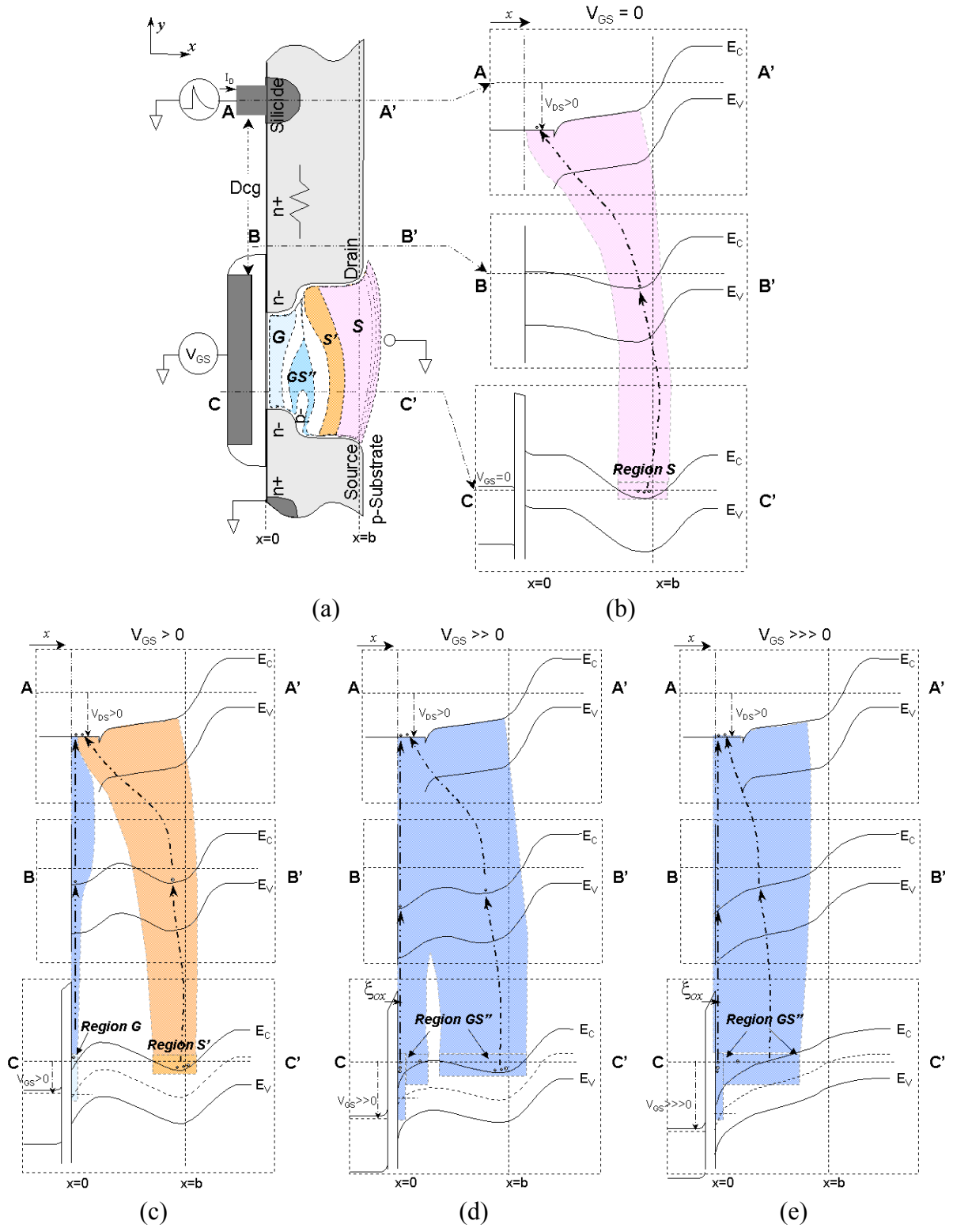


Fig. 3.1 Illustrations of (a) the gate-driven NMOS device structure, and the variation on energy band of the gate-driven NMOS with different gate biases of (b) V_{GS}=0, (c) V_{GS}>0, (d) V_{GS}>>0, and (e) V_{GS}>>>0.

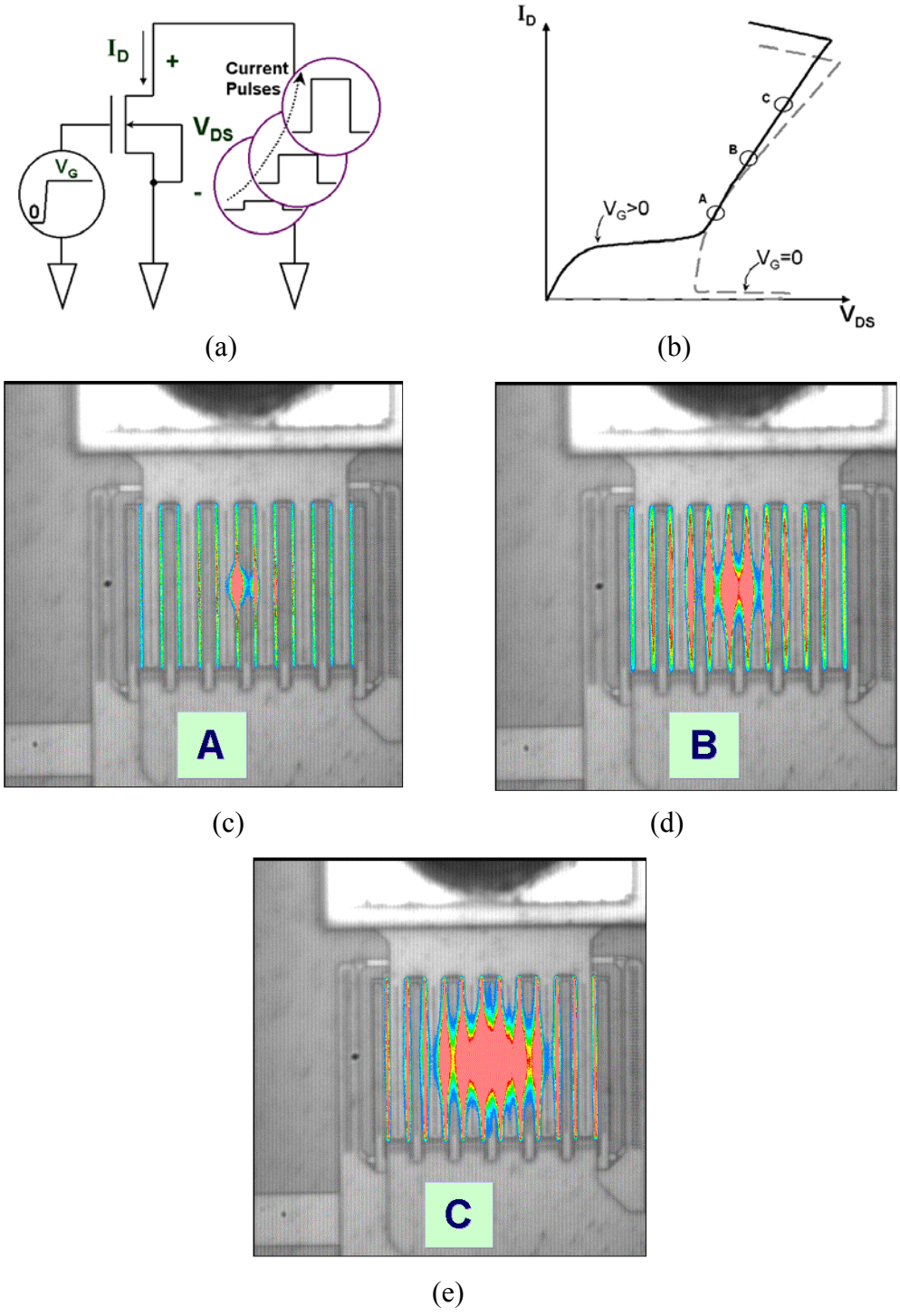
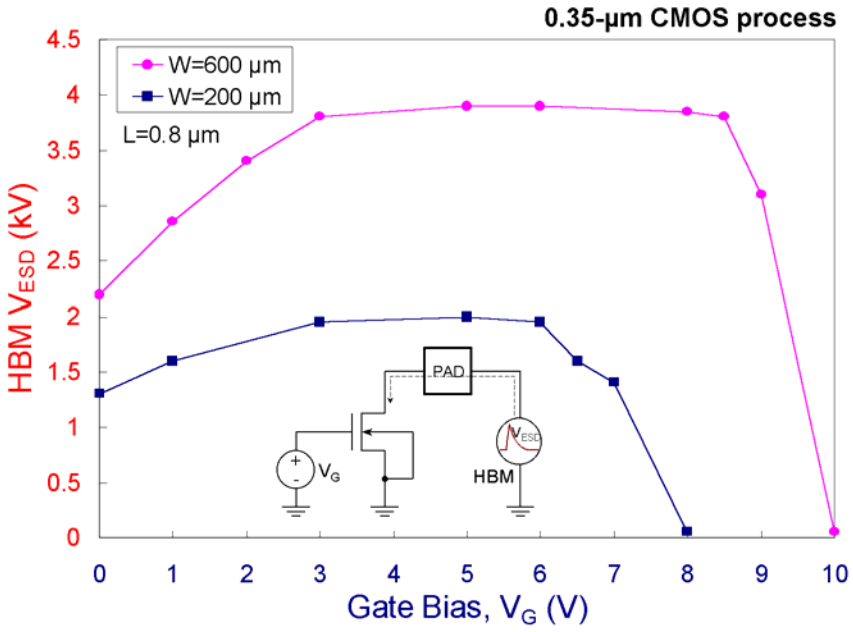
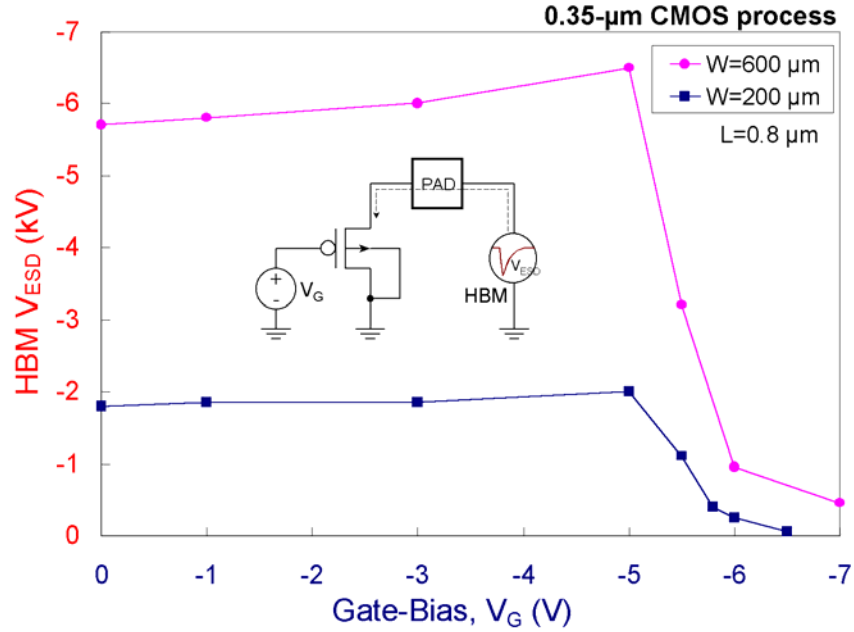


Fig. 3.2 The EMMI photographs on a gate-driven NMOS (W/L = 300μm/0.5μm) to observe its turn-on behavior under the stress of different pulsed currents. (a) The measurement setup, (b) the corresponding I-V curve of a gate-driven NMOS, (c)-(e) the hot spots in the gate-driven NMOS under different current stresses.



(a)



(b)

Fig. 3.3 The gate bias effect on the HBM ESD robustness of (a) NMOS, and (b) PMOS, without silicided diffusion in a 0.35-μm silicided CMOS process.

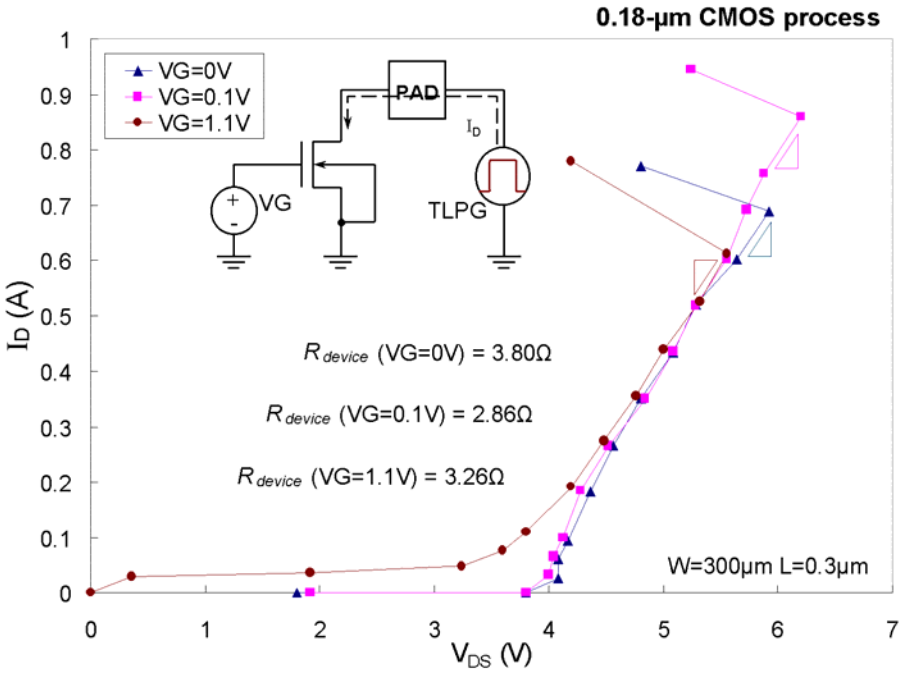


Fig. 3.4 TLP measured I-V curves and turn-on resistances of the gate-driven NMOS devices with silicide-blocking mask in a 0.18-μm salicided CMOS process.

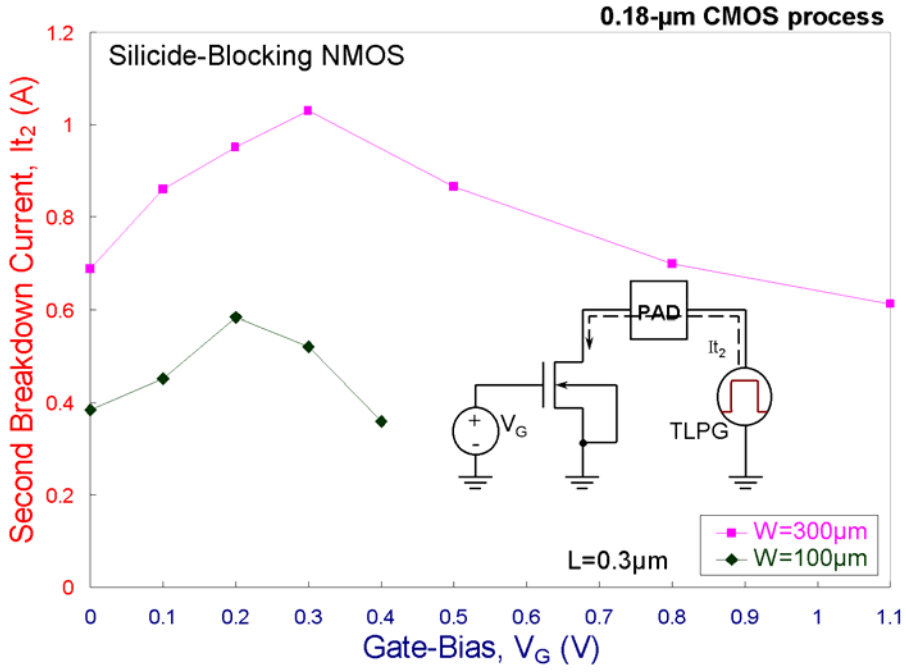


Fig. 3.5 The gate-driven effect on the second breakdown current of silicide-blocking NMOS in a 0.18-μm salicided CMOS process.

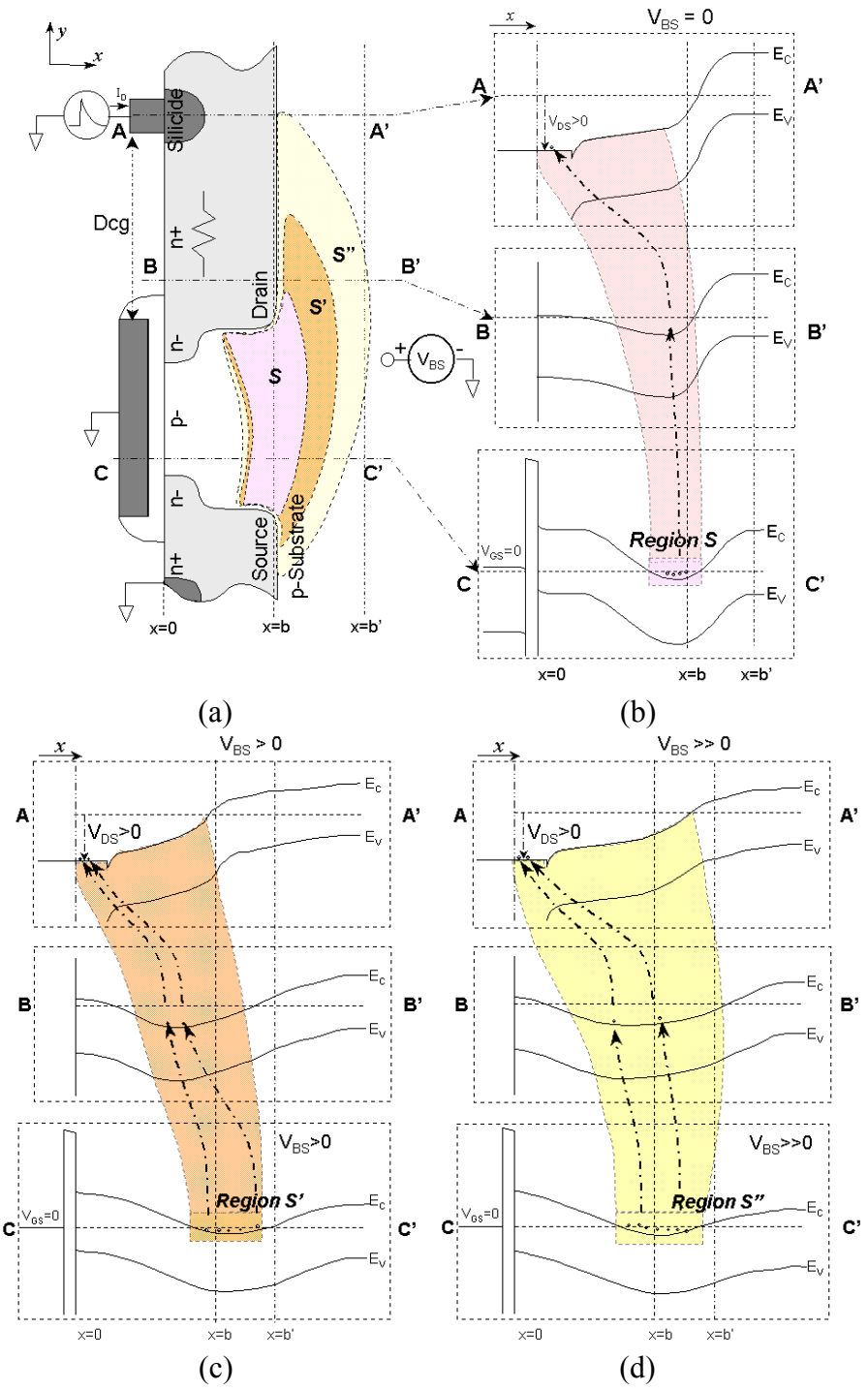
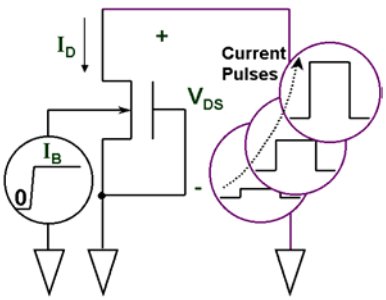
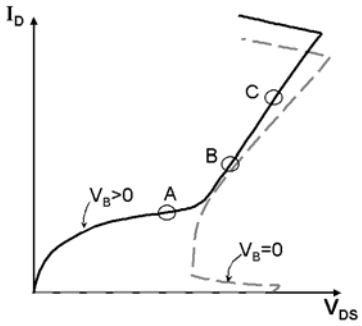


Fig. 3.6 Illustrations of (a) the substrate-triggered NMOS device structure, and the variation on energy band of the substrate-triggered NMOS with different substrate biases of (b) V_{BS}=0, (c) V_{BS}>0, and (d) V_{BS}>>0.



(a)



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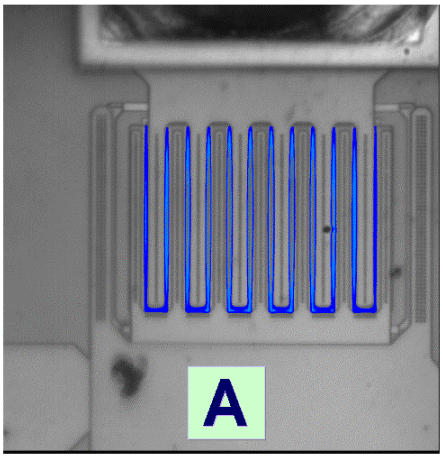
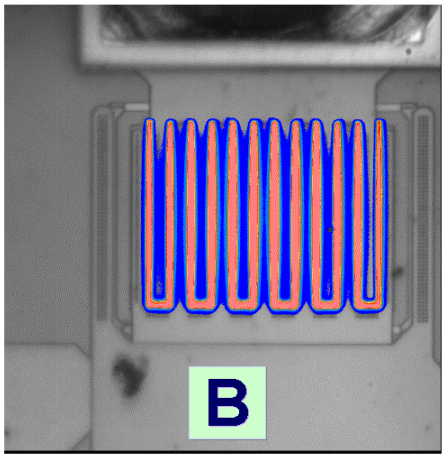


(c)



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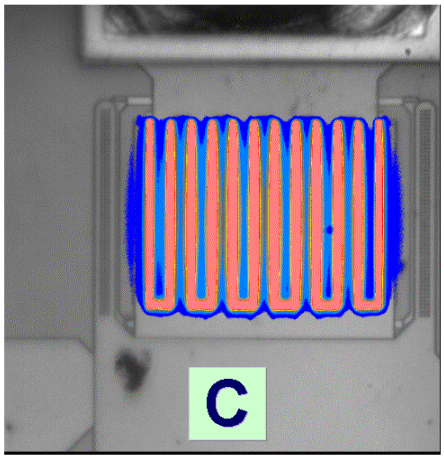
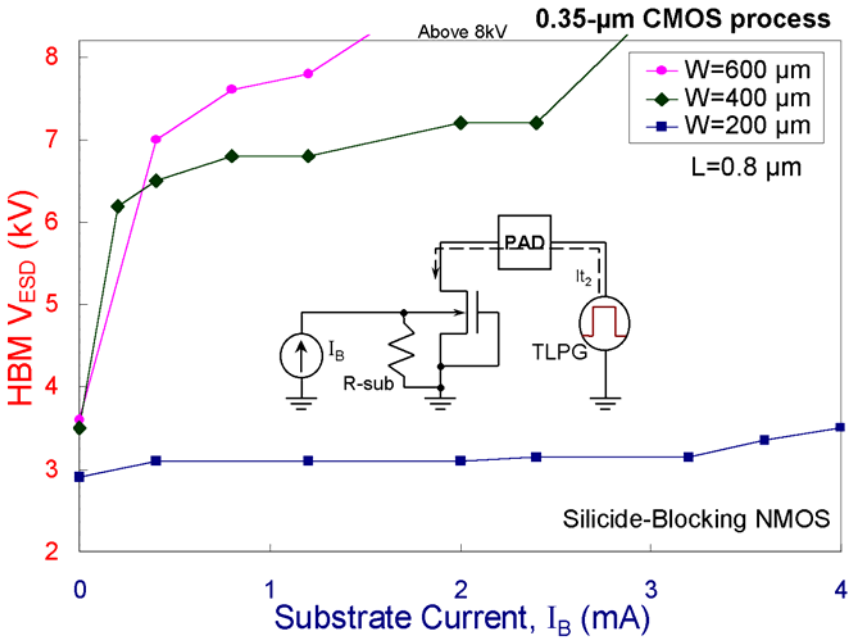
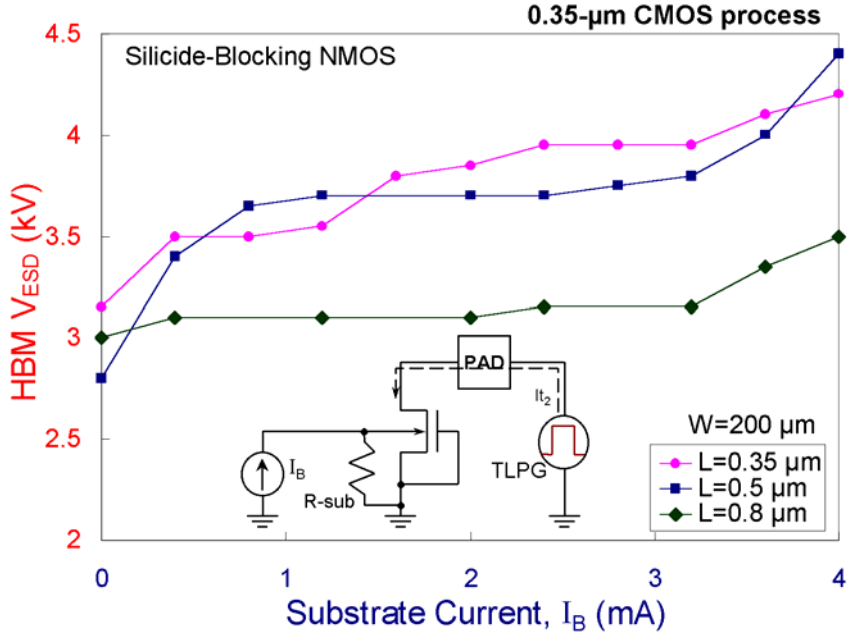


(e)

Fig. 3.7 The EMMI photographs on a substrate-triggered NMOS (W/L = 300μm/0.5μm) to observe its turn-on behavior under the stress of different pulsed currents. (a) The measurement setup, (b) the corresponding I-V curve of a substrate-triggered NMOS, (c)-(e) the hot spots in the substrate-triggered NMOS under different current stresses.



(a)



(b)

Fig. 3.8 The effect of substrate current on the ESD robustness of NMOS devices with (a) different channel widths, and (b) different channel lengths, in a 0.35-μm silicided CMOS process.

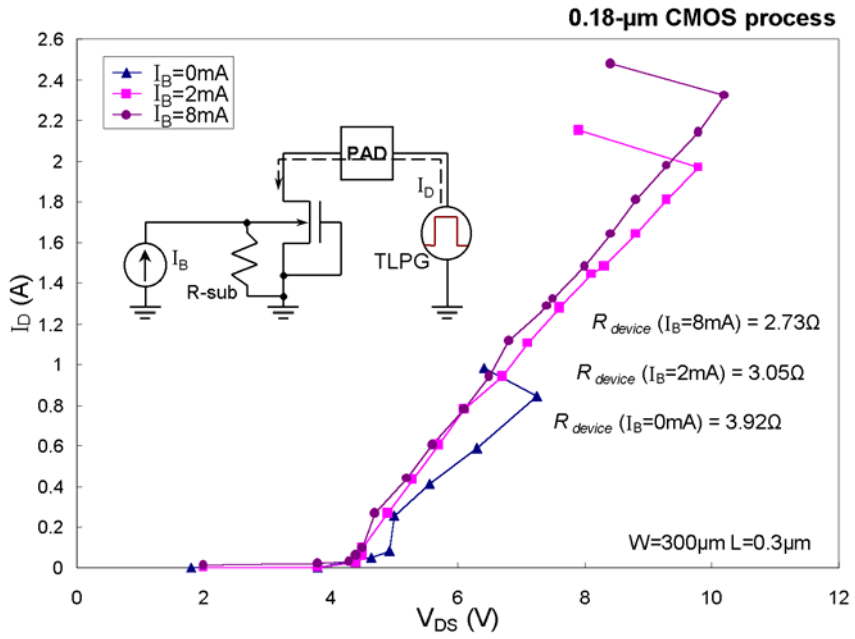


Fig. 3.9 TLP measured I-V curves and turn-on resistances of the substrate-triggered NMOS devices with silicide-blocking mask in a 0.18-μm salicided CMOS process.

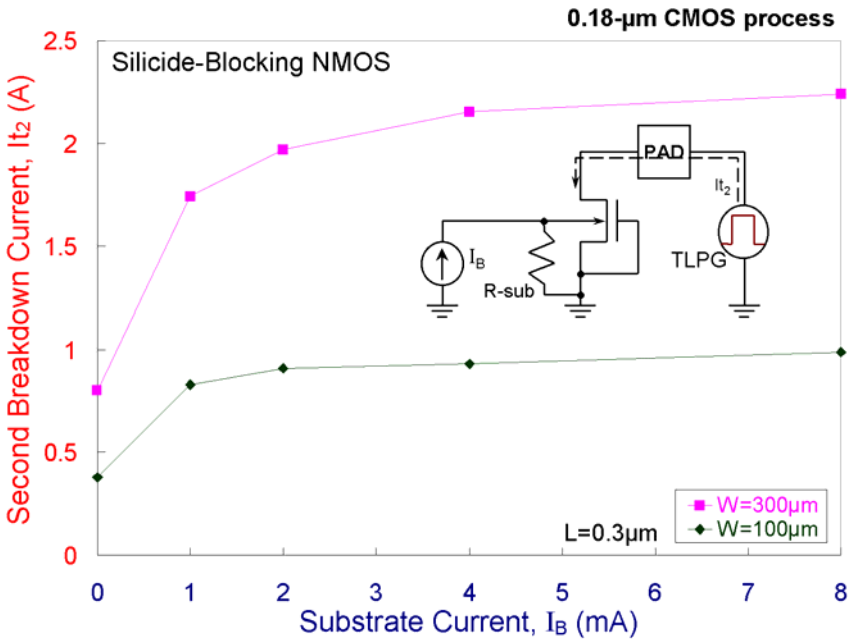


Fig. 3.10 The effect of substrate current on the ESD robustness of silicide-blocking NMOS devices with different channel widths in a 0.18-μm salicided CMOS process.

CHAPTER 4

ON-CHIP ESD PROTECTION CIRCUITS DESIGN BY USING SUBSTRATE-TRIGGERED TECHNIQUE

In this chapter, a novel substrate-triggered technique for input, output, and power-rail ESD protection, as comparing to the traditional gate-driven technique, is proposed to effectively improve ESD (electrostatic discharge) robustness of IC products. The substrate-trigger effect on MOSFET devices for ESD protection has been investigated in details by using the dc I-V curve, TLP-measured secondary breakdown current It_2, and the energy band diagrams in chapter 3. With the substrate-triggered design, the parasitic lateral BJT of MOSFET can sustain higher ESD current than the gate-driven MOSFET. Some novel on-chip ESD protection circuits for input, output, and power rails are therefore designed by using substrate-triggered technique [101]. The proposed ESD protection circuits have been successfully verified in a 0.18-μm salicided CMOS process. The HBM ESD robustness of output ESD protection circuits with ESD protection NMOS of W/L = 300μm/0.3μm can be improved from the original 0.65 kV with the traditional gate-driven design to become 3.2 kV by the proposed substrate-triggered design.

4.1 SUBSTRATE-TRIGGERED ESD PROTECTION DEVICE

4.1.1 Device Structure

To investigate ESD robustness of the substrate-triggered ESD protection device, the device cross-sectional views and corresponding finger-type layout patterns of the traditional gate-driven and the new proposed substrate-triggered NMOS's are shown in Fig. 4.1(a) and Fig. 4.1(b), respectively. The gate-oxide physical thicknesses of those devices are about ~ 30 Å in a 0.18-μm 1.8-V salicided CMOS process. Such thin gate-oxide NMOS's with different channel widths but a fixed channel length of 0.3μm and a fixed unit finger length of 25μm

had been fabricated in a 0.18-μm salicided CMOS process [102] with extra silicide-blocking mask to block the silicided diffusion. The clearances from the contact to poly gate edge in the drain and source diffusions of the traditional finger-type NMOS in Fig. 4.1(a) are 3μm and 1μm, respectively. To compare with the traditional NMOS and to reduce the total layout area, the clearances from the contact to poly gate edge on the drain and source diffusions of the substrate-triggered NMOS in Fig. 4.1(b) are designed as 2μm and 1μm, respectively. In Fig. 4.1(b), a p+ diffusion is located at the center of NMOS layout, which is used as the trigger node of ESD protection device. An N-well ring locating under the source regions and surrounding the whole device, as shown in the device structure of Fig. 4.1(b), is used to form a higher equivalent substrate resistance for more effective substrate-triggered design.

4.1.2 Device Characteristics

The dc I-V curves of the fabricated substrate-triggered NMOS with W/L=300μm/0.3μm under different substrate biases are measured in Fig. 4.2. The original trigger voltage and holding voltage of the substrate-triggered NMOS without substrate bias are 5.5V and 4V, respectively. The substrate current can lower the trigger voltage of the substrate-triggered NMOS in Fig. 4.2, which can improve the turn-on efficiency of ESD protection device during ESD stress.

To investigate the device behavior during high ESD current stress, transmission line pulsing (TLP) technique is used to measure the second breakdown characteristics of devices. The TLPG (transmission line pulse generator) with a pulse width of 100 ns is used to find the It_2 (second breakdown current) of the fabricated NMOS's under different substrate biases. The TLP-measured I-V characteristics of substrate-triggered NMOS (W/L=300μm/0.3μm) with 0V, 1V, and 8V substrate biases are shown in Fig. 3.9. The turn-on resistance is continually decreased from 3.92Ω to 2.73Ω while the substrate bias is changed from 0V to 8V. The substrate bias can change the turn-on resistance of substrate-triggered NMOS during ESD stress. It implies that substrate bias can change the turn-on area or turn-on path of parasitic lateral BJT in the substrate-triggered NMOS to sustain higher ESD stress. The dependence of It_2 on the substrate-biased voltage of the substrate-triggered NMOS devices with different channel widths in a 0.18-μm salicided CMOS process are shown in Fig. 3.10. The second breakdown currents of the substrate-triggered NMOS's with W=300μm or W=100μm can be continually increased by the substrate-biased voltage. The second breakdown current (It_2) of

the substrate-triggered NMOS with a channel width of 300μm under 0-V substrate bias is only 0.8A, but it is increased up to 2.2A while the NMOS has a substrate bias of 2V. With a higher It_2, the NMOS can sustain a higher ESD level. With a higher substrate-biased voltage up to 8 V, the It_2 in Fig. 3.10 is not degraded. Therefore, the substrate-triggered technique can continually improve ESD robustness of NMOS.

4.2 ESD PROTECTION CIRCUITS WITH SUBSTRATE-TRIGGERED DESIGN

Since the ESD events may have positive or negative voltage on an input (or output) pin with the VDD or VSS pins relatively grounded, there are four ESD-stress conditions on an input (or output) pin [5]. The input or output ESD protection circuits are therefore designed to discharge the ESD current from the stressed pin to the VDD or VSS pin. Generally, the ESD protection circuits have low ESD level under the positive-to-VSS and negative-to-VDD ESD-stress conditions, because the protection devices in these two ESD-stress conditions are often operated in the reverse-biased breakdown condition. Thus, the substrate-triggered design is used to significantly improve ESD robustness of ESD protection circuits in these two worst ESD-stress conditions.

4.2.1 Input ESD Protection Circuits

The input ESD protection circuit with the substrate-triggered design is shown in Fig. 4.3. To realize the ESD detection function, two RC-based ESD protection circuit is connected between the input pad, VDD, and VSS power lines. The ESD detection circuit with resistors (R1 and R2), capacitors (C1 and C2), and NMOS/PMOS (Mn2/Mp2) as connected in Fig. 4.3 are used to detect the ESD events. The ESD protection devices are designed to be triggered on when the ESD voltage appears across between the input pad and VSS power line, or between the input pad and VDD power line. But, the ESD protection device is kept off when the IC is under the normal circuit operating condition. To meet these requirements, the RC time constant in the ESD detection circuit is designed about 0.1 ~ 1 μs to achieve the desired operations. To efficiently clamp the ESD voltage across between the input pad and VSS or VDD power line before the input stage of internal circuit is damaged, the ESD detection

circuits (R2-C2-Mp2 and R1-C1-Mn2) are used to generate the substrate-triggered current to turn on the ESD protection devices. To simply explain the operation principle of the proposed input ESD protection circuit with substrate-triggered design during positive-to-VSS ESD stress, the ESD current discharging through the button half input ESD protection circuit is illustrated in Fig. 4.4(a). During negative-to VDD ESD stress, the ESD current discharging through the upper half input ESD protection circuit is illustrated in Fig. 4.4(b).

Initially, the nodes ni4 and nins in Fig. 4.4(a) have the voltage levels the same as the VSS level, because the IC under the positive-to-VSS ESD-stress condition has floating VDD power pin. The positive-to-VSS ESD voltage across the input pad and VSS power line will forward bias the parasitic diode of PMOS (Mp1) to VDD and charge up the node ni4 of the capacitor C2 in Fig. 4.4(a). The HBM ESD voltage has a rise time about ~10 ns [5]. The voltage level of node ni4 is increased much slower than the voltage level on the node ni1, because the R2-C2 circuit has a time constant in the order of microsecond (μs). Due to the delay of the voltage increase on the node ni4, the Mp2 device with a ~ 0V gate voltage is turned on by the ESD voltage at the pad and conducts a current Ip2 into the node nins (along the Path_1 in Fig. 4.4(a)) to trigger on the ESD protection NMOS (Mn1). The triggered-on NMOS, which provides a low-impedance path (Path_2) between the input pad and VSS power line, discharges the ESD current from the input pad to VSS. The turn-on time (t_{on}) of the ESD protection device can be mainly adjusted by the RC time constant in the ESD detection circuit. The turn-on time of the ESD protection device is designed about 200 ns to meet the half-energy discharging time of the HBM ESD event. Because the substrate-triggered ESD protection NMOS is turned on by a positive substrate current rather than by the drain snapback breakdown, the NMOS can be turned on at lower voltage to bypass the ESD current before the input circuits are damaged by the ESD overstress voltage. So, the internal circuits can be effectively protected by the proposed ESD protection circuit without ESD damage.

During the negative-to-VDD ESD-stress condition, the nodes ni5 and nips in Fig. 4.4(b) have the initial voltage levels the same as the VDD power line, which is initially grounded. The negative-to-VDD ESD voltage across the input pad and VDD power line will forward bias the parasitic diode of NMOS (Mn1) to the floating VSS power line and charge up the node ni5 of the capacitor C1 to a negative voltage level. The negative HBM ESD voltage has a fall time about ~10 ns. The voltage level of node ni5 is decreased much slower than the voltage level on the node ni1, because the R1-C1 circuit has a time constant in the order of

microsecond (μs). Due to the delay of the voltage decrease on the node ni5, the Vgs of Mn2 is greater than its threshold voltage during such a negative-to-VDD ESD stress. So, the Mn2 device is turned on by the ESD voltage and conducts a negative current In2 into the node nips (along the Path_3 in Fig. 4.4(b)) to trigger on the ESD protection PMOS (Mp1). The triggered-on PMOS, which provides a low-impedance path (Path_4) between the input pad and VDD power line, discharges the negative ESD current from the input pad to the grounded VDD. Because the substrate-triggered ESD protection PMOS is turned on by a substrate current rather than by the drain snapback breakdown, the PMOS can be turned on with a faster speed to bypass the ESD current before the input circuits are damaged by the ESD overstress voltage.

To meet the aforementioned circuit operations, the circuit simulation program *HSPICE* is used to find the suitable RC value and device sizes for the ESD detection circuit. The device dimensions for this ESD detection circuit in a 0.18-μm CMOS process are chosen as R1 = R2 = 10kΩ, C1 = C2 = 20pF, and W/L of Mp2 (Mn2) = 20μm/0.8μm. The *HSPICE* simulated voltage waveforms in the time domain at the node nins during the positive-to-VSS ESD-stress condition is shown in Fig. 4.5(a). The simulated voltage waveforms in the time domain at the node nips during the negative-to-VDD ESD-stress condition is shown in Fig. 4.5(b). In Fig. 4.5(a), a ramp voltage with a rise time of 10 ns is used to simulate the rising edge of an HBM ESD pulse in the positive-to-VSS ESD-stress condition. Because the NMOS snapback-breakdown voltage is about 5.5 V in the 0.18-μm CMOS process, the pulse height of the ramp voltage is set as 4 V to monitor the voltage on the node nins before the ESD protection NMOS is broken down. As shown in Fig. 4.5(a), the voltage waveform on the node nins is simultaneously increased when the ramp voltage is applied to the input pad, whereas the VSS is grounded and VDD is initially floating. By changing the RC time constant or the device size of Mp2, the turn-on time (t_{on}) of the ESD protection NMOS can be adjusted. In Fig. 4.5(b), a ramp voltage with a fall time of 10 ns is used to simulate the falling edge of a negative HBM ESD pulse in the negative-to-VDD ESD-stress condition. As shown in Fig. 4.5(b), the voltage waveform on the node nips is simultaneously decreased when the ramp voltage is applied to the input pad, whereas the VDD is grounded and VSS is initially floating. Because the NMOS Mn2 has higher driving current than that of PMOS Mp2 in the ESD detection circuit of Fig. 4.4, the simulated turn-on time (t_{on}) in Fig. 4.5(b) for the ESD protection PMOS is longer than that in Fig. 4.5(a) for the ESD protection NMOS. If the device dimension of Mp2 is increased, the turn-on time (t_{on}) in Fig. 4.5(a) can be further

increased. The dependence of turn-on time (t_{on}) on the device dimension of Mp2 or Mn2 is shown in Fig. 4.6. To design a suitable ESD detection circuit, the turn-on time can be modified by changing the device dimension of Mp2 or Mn2 or by changing the RC time constant.

When the IC is in the normal circuit operating condition with the power supplies, the node ni4 (ni5) is biased at VDD (VSS) through the resistor R2 (R1) to turn off the Mp2 (Mn2). Therefore, the substrate-triggered ESD protection NMOS (PMOS) is guaranteed to be kept off. In Fig. 4.7(a), a 0-to-1.8V square voltage pulse with a rise/fall time of 1 ns and a period of 10 ns is used to simulate the input signal and applied to the input pad with the input ESD protection circuit. Under such a normal signal input condition with 1.8-V VDD and 0-V VSS power supplies, the voltage waveforms on the nodes ni1, ni2, nins, and nips are shown in Fig. 4.7(b), where the voltage level of node nins (nips) under static state is kept at 0 V (1.8 V). During the transition of the input signal, the nins (nips) has a little voltage increase of 0.32 V (0.2 V) due to the parasitic capacitance coupling, which is smaller than the cut-in voltage (~0.7 V) of the parasitic BJT in the ESD protection NMOS (PMOS). Therefore, the ESD protection devices can be kept off when the IC is in the normal circuit operation conditions.

The device dimension of the ESD protection NMOS (PMOS) is adjusted to meet the required ESD level within a specified layout area to quickly discharge the ESD current. From the aforementioned turn-on mechanism of substrate-triggered design, the substrate-triggered technique can efficiently improve ESD robustness of the ESD protection device to protect the internal circuits of the IC.

4.2.2 Output ESD Protection Circuit

The output ESD protection circuit with the substrate-triggered design is shown in Fig. 4.8. The PMOS (Mp3) and NMOS (Mn3) of output buffer with larger device dimensions to drive external load in Fig. 4.8 also work as the ESD protection devices. To realize the ESD detection function, two RC-based circuits are connected with the output pad, VDD, and VSS power lines. The ESD detection circuits with resistors (R3 and R4), capacitors (C3 and C4), and NMOS/PMOS (Mn4/Mp4) are connected in Fig. 4.8 to detect the ESD events. The gates of output buffer are connected to the pre-driver buffer. The operation principles of the output ESD protection circuit during ESD-stress conditions are similar to that of the input ESD protection circuit described in the previous section. The ESD detection circuit is designed to

detect the ESD events and sends a triggered current into the trigger node of substrate-triggered NMOS (Mn3) or PMOS (Mp3).

Because the Mp3 and Mn3 devices in the output buffer are triggered on through their bulk nodes, the ESD detection circuit does not connect to the gates of the output buffer. The gates of output buffer can be fully controlled by its pre-driver circuit without any conflict to the ESD detection circuit. So, the proposed substrate-triggered design is more easily applied to trigger on the output Mp3 and Mn3, as compare to the gate-driven design.

4.2.3 Power-Rail ESD Clamp Circuit

The power-rail ESD clamp circuit with the substrate-triggered design is shown in Fig. 4.9. The ESD clamp circuit is designed to be turned on when the ESD voltage appears across the VDD and VSS power lines. But, this ESD clamp circuit is kept off when the IC is under the normal power-on condition. To efficiently clamp the ESD voltage across the VDD and VSS power lines before the internal circuits are damaged, an ESD detection circuit (R5, C5, Mn5, and Mp5) is used to turn on the substrate-triggered NMOS (Mn6). The ESD detection circuit with resistance (R5), capacitance (C5), NMOS (Mn5), and PMOS (Mp5) are connected in Fig. 4.9 to detect the ESD events. To meet these requirements, the RC time constant in the VDD-to-VSS ESD clamp circuit is designed about 0.1-1 μs to achieve the desired operations. The ESD detection circuit is designed to detect the ESD event and sends a triggering current to the substrate of the ESD protection NMOS (Mn6).

Initially, the nodes nc1 and nc2 in Fig. 4.9 have the voltage levels (0 V) the same as the grounded VSS pin, before the positive-to-VSS ESD voltage is applied to the VDD pin. The positive ESD voltage across the VDD and VSS power lines will charge up the node nc1 of capacitor C5 in Fig. 4.9. But, the voltage level of node nc1 is increased much slower than the voltage level on the VDD power line, because the R5-C5 circuit has a time constant in the order of microsecond (μs). Due to the delay of the voltage increase on the node nc1, the Vgs of Mn5 is small than its threshold voltage during such a positive ESD stress. But, the Mp5 device is turned on by the ESD voltage and conducts a triggering current into the node nc2 to trigger on the ESD protection NMOS (Mn6). The turn-on time of the ESD protection device is designed about 200 ns. The triggered-on ESD protection NMOS, which provides a low-impedance path between the VDD and VSS power lines, discharges the positive ESD current from the VDD to the grounded VSS. Because the ESD protection NMOS (Mn6) is

turned on by a substrate current rather than by the drain snapback breakdown, the ESD protection NMOS can be turned on at lower voltage to bypass the ESD current before the internal circuits are damaged by the ESD overstress voltage. So, the internal circuits can be effectively protected by the proposed power-rail ESD clamp circuit with substrate-triggered design.

To meet the aforementioned circuit operations, the circuit simulation program *HSPICE* is used to find the suitable RC value and device sizes for the ESD detection circuit. The device dimensions for this ESD detection circuit in a 0.18-μm CMOS process are chosen as R5 = 10kΩ, C5 = 20pF, W/L of Mp5 = 120μm/0.8μm, and W/L of Mn5 = 60μm/0.8μm. The *HSPICE* simulated voltage waveforms in the time domain at the node nc2 during the positive ESD-stress condition and the normal VDD power-on condition are shown in Fig. 4.10 and Fig. 4.11, respectively. In Fig. 4.10, a 4-V ramp voltage with a rise time of 10 ns is used to simulate the rising edge of an HBM ESD pulse in the positive ESD-stress condition. As shown in Fig. 4.10, the voltage waveform on the node nc2 is simultaneously increased when the ramp voltage is applied to VDD power line, whereas the VSS is grounded. In Fig. 4.11, a power-on voltage waveform with a rise time of 1 ms and a voltage height of 1.8 V is applied to the VDD power line of the proposed power-rail ESD clamp circuit. During such a VDD power-on condition, the voltage waveform on the node nc2 is also shown in Fig. 4.11, where the nc2 has a peak voltage of only about 1.2 μV which appears at the beginning of Fig. 4.11. With such a low voltage on the node nc2 during normal VDD power-on condition, the substrate-triggered ESD protection NMOS (Mn6) can be always kept off when the IC is in the normal circuit operation condition.

The device dimension of the substrate-triggered ESD protection NMOS is adjusted to meet the required ESD level within a specified layout area to quickly bypass the ESD current. From the aforementioned turn-on mechanism of substrate-triggered technique, the substrate-triggered design can efficiently improve the ESD robustness of ESD protection device than the traditional gate-driven design.

4.3 EXPERIMENTAL RESULTS

To compare with the substrate-triggered design, the traditional designs for the input/output ESD protection circuits and power-rail ESD clamp circuits are also fabricated in

the testchips of a 0.18-μm salicided CMOS process, as those shown in Fig. 4.12. The traditional ESD protection design for input, output, and power rails are illustrated in Figs. 4.12(a), 4.12(b), and 4.12(c), respectively. In Fig. 4.12(a), the NMOS (Mni1) and PMOS (Mpi1) have gate-coupled design to protect the input stage of internal circuits during ESD stress. In Fig. 4.12(b), the PMOS Mpo3 and NMOS Mno3 of the output buffer with larger dimensions are also used as the ESD protection devices to sustain ESD stress. In Fig. 4.12(c), an RC-based ESD clamp circuit with gate-driven design is used to protect the ESD stress across the power rail [5]. The device structures and dimensions of Mni1, Mno3, and Mnc2 are designed and fabricated as those shown in Fig. 4.1(a) with different total channel widths. The Mpi1 and Mpo3 have their device structures and dimensions similar to those of the NMOS devices.

4.3.1 HBM ESD test Results

The *ZapMaster* ESD tester, produced by Keytek Instrument Corp., is used to measure the HBM ESD level of the fabricated testchips. The failure criterion is generally defined at 1-μA leakage current under 1.1 times V_{DD} bias, when the ESD protection circuit is in the off state. The ESD levels of the fabricated input/output ESD protection circuits and power-rail ESD clamp circuits with the substrate-triggered or the traditional designs have been tested, and the results are compared in Fig. 4.13, Fig. 4.14, and Fig. 4.15, respectively.

In Fig. 4.13, the positive HBM ESD pulses are stressed on the input pad of the input ESD protection circuit with the VSS grounded under the positive-to-VSS HBM ESD test. The input ESD protection circuit with substrate-triggered design has an excellent improvement on its ESD level, as compared to the traditional design. The proposed input ESD protection circuit with substrate-triggered NMOS (W/L= 300μm/0.3μm) can sustain an ESD level of 3.3 kV. But, the input ESD protection circuit with the same device dimension under traditional design has an ESD level of only 0.8 kV.

In Fig. 4.14, the positive HBM ESD pulses are stressed on the output pad of the output ESD protection circuit with the VSS grounded under the positive-to-VSS HBM ESD test. The substrate-triggered design can also improve the ESD robustness of output ESD protection circuit with the NMOS of W/L=300μm/0.3μm from 0.65 kV with the traditional design to 3.2 kV with the substrate-triggered design.

In Fig. 4.15, the positive HBM ESD pulses are stressed on the VDD of the power-rail

ESD clamp circuit with the VSS grounded. The substrate-triggered designs are compared with the traditional gate-driven design on the ESD robustness. The ESD robustness of substrate-triggered ESD clamp circuit with substrate-triggered NMOS of W/L=300μm/0.3μm is 2.5 kV, but that with the traditional gate-driven design under the same device dimension can sustain the ESD level of only 1 kV. These have verified the excellent effectiveness of the proposed substrate-triggered technique to improve ESD robustness in a 0.18-μm salicide CMOS process.

4.3.2 Turn-on Verification

To verify the aforementioned ESD detection function in the proposed input ESD protection circuit, an experimental setup is shown in Fig. 4.16(a), where a voltage pulse generated from a pulse generator (*HP 8118*) is used to simulate the rising edge of a positive-to-VSS HBM ESD pulse. The voltage pulse generated from the pulse generator initially has a square-type voltage waveform with a rise time about ~10 ns and a pulse height of 4 V, as that shown in Fig. 4.16(b). When the positive voltage pulse is applied to the input pad of the proposed input ESD protection circuit with VSS grounded, the sharp-rising edge of the ESD-like voltage pulse will trigger on the ESD protection NMOS to provide a low-impedance path between the input pad and VSS power line. The voltage waveform on the input pad is therefore degraded by the turned-on ESD protection NMOS. The degraded voltage waveform on the input pad is also shown in Fig. 4.16(b). The voltage waveform is degraded at the rising edge because the ESD protection NMOS is simultaneously turned on when the ESD-like voltage pulse is applied to the input pad. The voltage degradation is dependent on the turned-on resistance of the parasitic lateral BJT in the ESD protection NMOS and the output resistance of the pulse generator. The maximum voltage drop from the applied 4-V voltage level in Fig. 4.16(b) is 1.5 V. The larger device dimension of the ESD protection device in the proposed input ESD protection circuit can lead to a lower voltage drop on the voltage waveform. When the node ni4 in Fig. 4.16(a) is charged up to turn off the PMOS (Mp2) in the ESD detection circuit, the ESD protection NMOS will be turned off and the voltage waveform will be restored to the original voltage level. From Fig. 4.16(b), the turn-on time (t_{on}) of the substrate-triggered NMOS has a turn-on time (t_{on}) of ~120ns under such a 4-V voltage pulse stress.

To verify the ESD detection function in the proposed power-rail ESD clamp circuit with

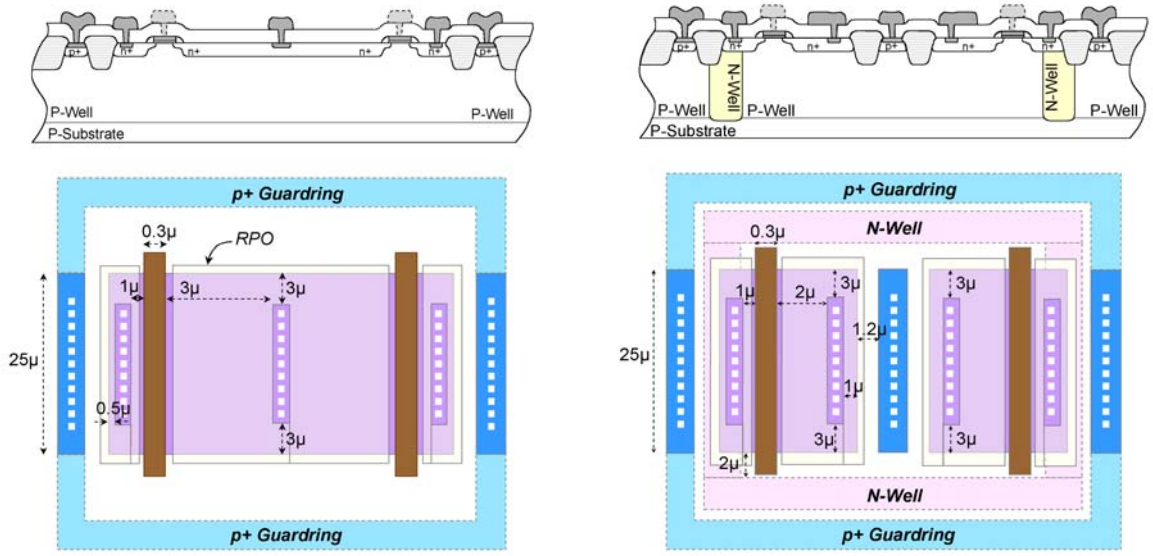
substrate-triggered design, an experimental setup is shown in Fig. 4.17(a), where the 4-V voltage pulse is applied to VDD power line to simulate the rising edge of a positive HBM ESD event. The voltage pulse generated from the pulse generator has a rise time about ~10 ns, as that shown in Fig. 4.17(b). When the positive voltage pulse is applied to the VDD power line of the proposed power-rail ESD clamp circuit with VSS grounded, the sharp-rising edge of the ESD-like voltage pulse will trigger on the ESD protection NMOS to provide a low-impedance path between the VDD and VSS power lines. The voltage waveform on the VDD power line will be degraded by the turned-on ESD protection NMOS. The degraded voltage waveform on the VDD power line is also shown in Fig. 4.17(b). The voltage waveform is degraded at the rising edge because the ESD protection NMOS is simultaneously turned on when the ESD-like voltage pulse is applied to the VDD power line. The maximum voltage drop from the applied 4-V voltage pulse in Fig. 4.17(b) is 1.9 V. When the node nc1 is charged up to the logic threshold voltage of the inverter (Mp5 and Mn5) in the ESD detection circuit, the ESD protection NMOS will be turned off and the voltage waveform will be restored to the original voltage level. In Fig. 4.17(b), the ESD protection NMOS has a turn-on time of ~ 160 ns under such a 4-V voltage pulse

To verify the turn-on behaviors of the proposed power-rail ESD clamp circuit in the normal VDD power-on condition, an experimental setup is shown in Fig. 4.18(a). A 0-to-1.8V ramp voltage with a rise time of 0.1 ms is applied to the VDD with the VSS grounded to simulate the VDD power-on condition. The voltage waveform on the VDD is monitored and shown in Fig. 4.18(b), where the voltage waveform is still remained as a ramp voltage without any degradation on its voltage waveform. So, the ESD protection NMOS in the power-rail ESD clamp circuit is indeed kept off during the normal VDD power-on transition. This power-rail ESD clamp circuit can be always kept off while the IC is in the normal circuit operating condition.

4.4 SUMMARY

From both of the physical analysis of turn-on mechanism and the experimental results, the substrate-triggered technique have been confirmed to continually improve the ESD robustness of ESD protection devices without sudden degradation as that by gate-driven design. With the efficient substrate-triggered ESD protection design, the input, output, and

power-rail ESD protection circuits have been successfully verified in a 0.18-μm CMOS process to protect the internal circuits of IC. With the proposed substrate-triggered design, the ESD protection devices with smaller layout dimension can sustain higher ESD stress than the traditional gate-driven design. This substrate-triggered technique will be one of the most effective solutions to improve ESD robustness of IC products in sub-quarter-micron CMOS technology.



(a) (b)

Fig. 4.1 Device structures and corresponding layout patterns of (a) the traditional finger-type NMOS, and (b) the proposed substrate-triggered NMOS, for ESD protection.

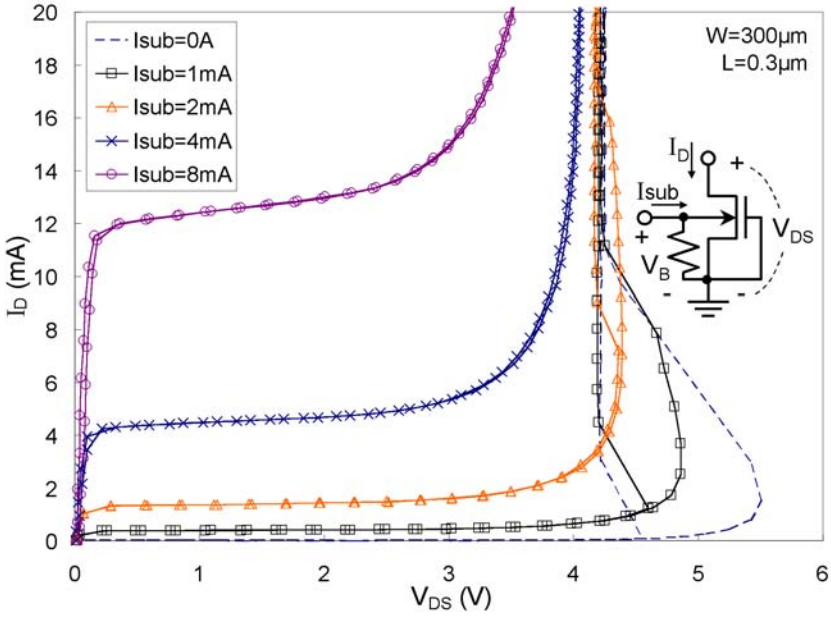


Fig. 4.2 The dc I-V curves of the substrate-triggered NMOS under different substrate current biases.

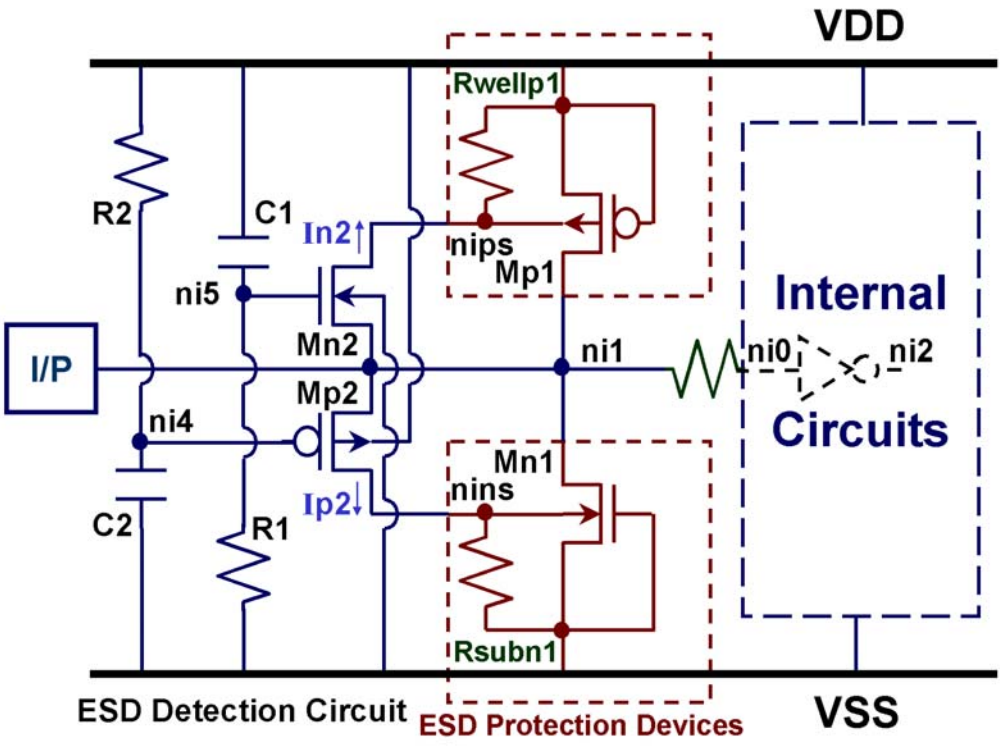
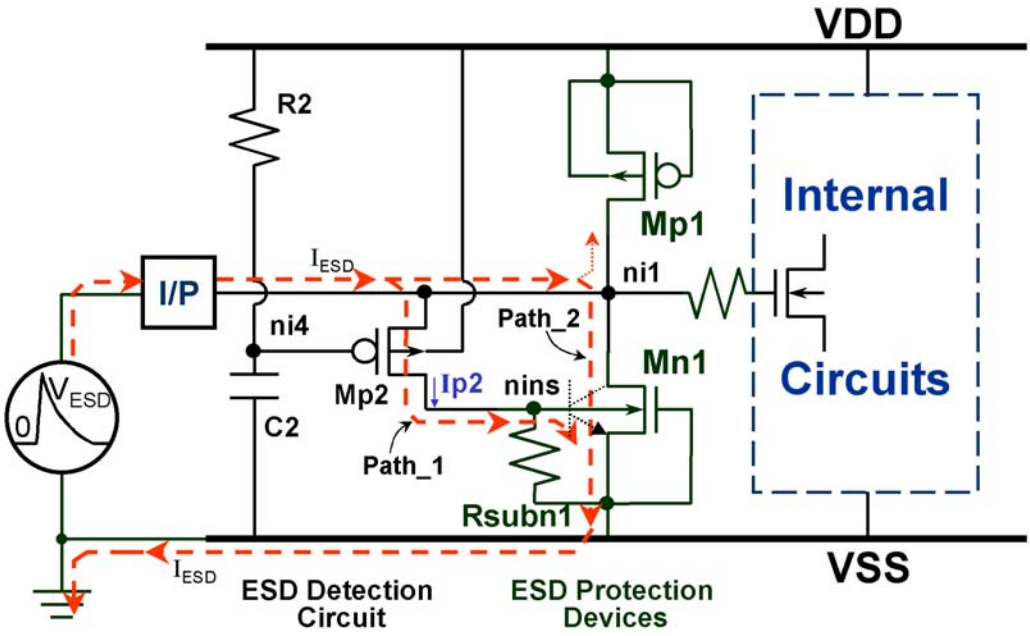
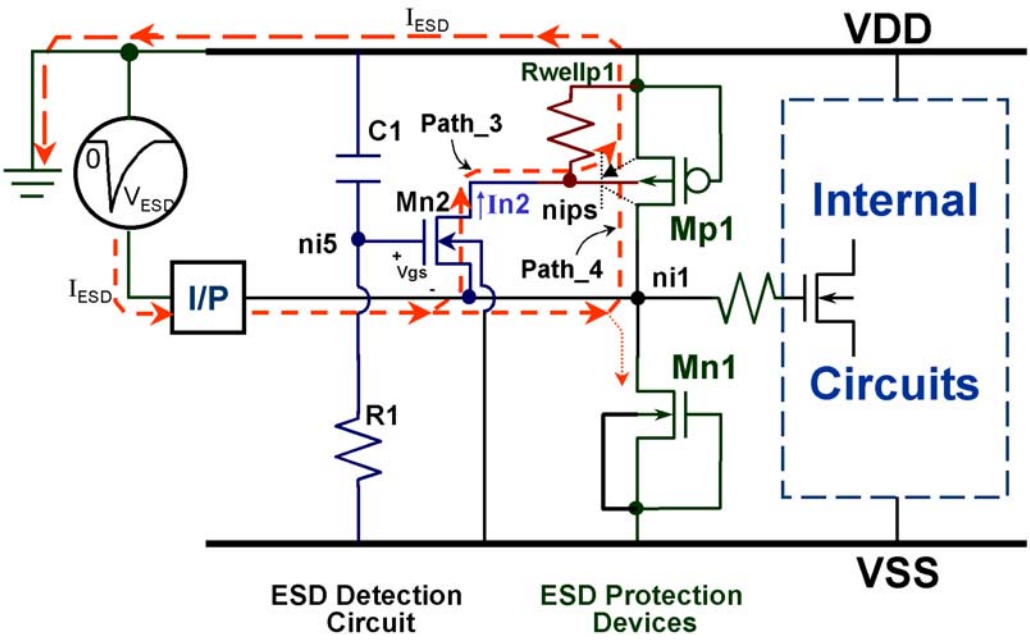


Fig. 4.3 The proposed input ESD protection circuit with substrate-triggered design.



(a)



(b)

Fig. 4.4 Illustration of the ESD current paths in the half input ESD protection circuit with substrate-triggered design during (a) the positive-to-VSS ESD stress, and (b) the negative-to-VDD ESD stress.

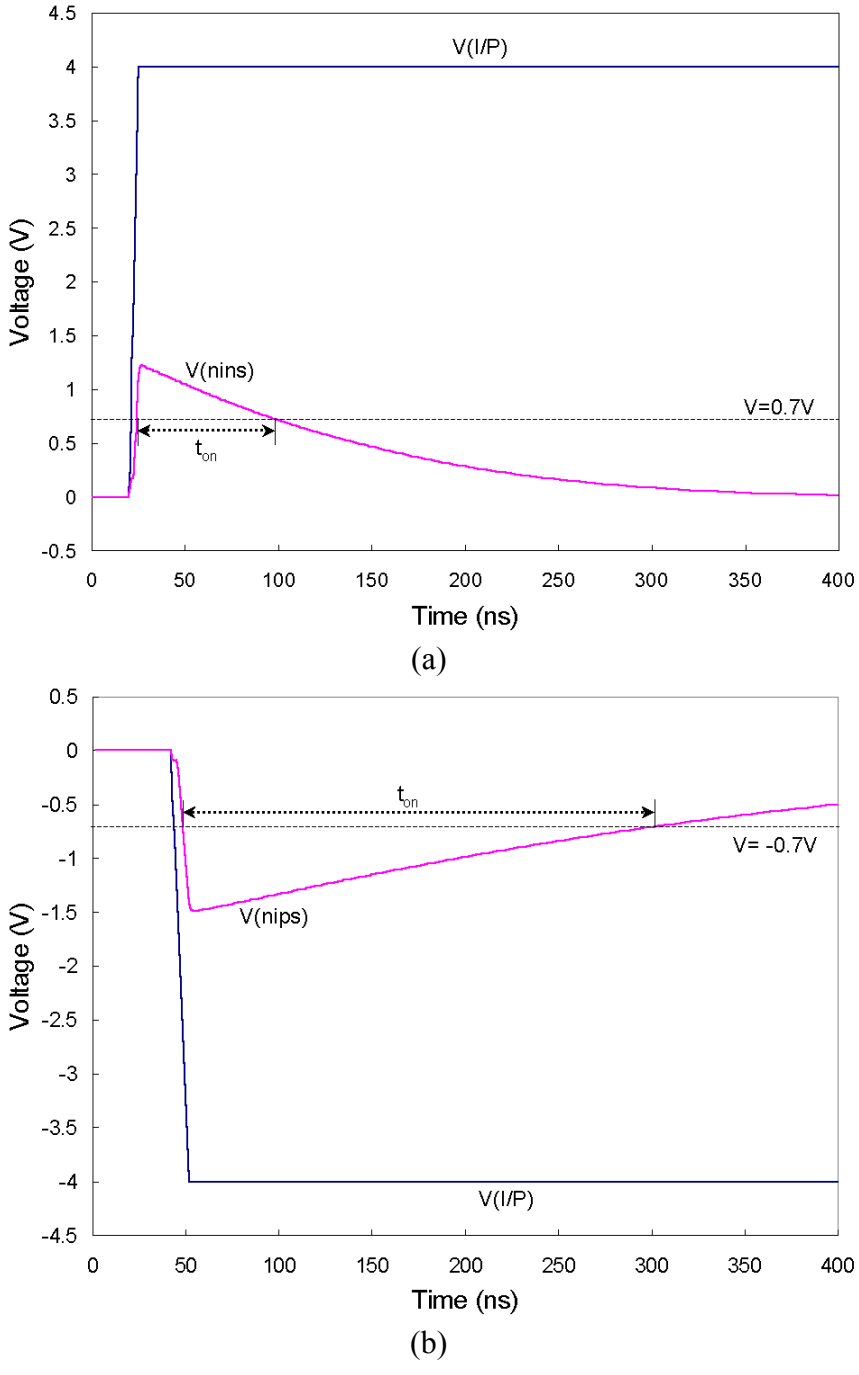


Fig. 4.5 *HSPICE* simulated voltage waveforms to find the turn-on time of the proposed input ESD protection circuit under (a) the positive-to-VSS ESD-stress condition, and (b) the negative-to-VDD ESD-stress condition.

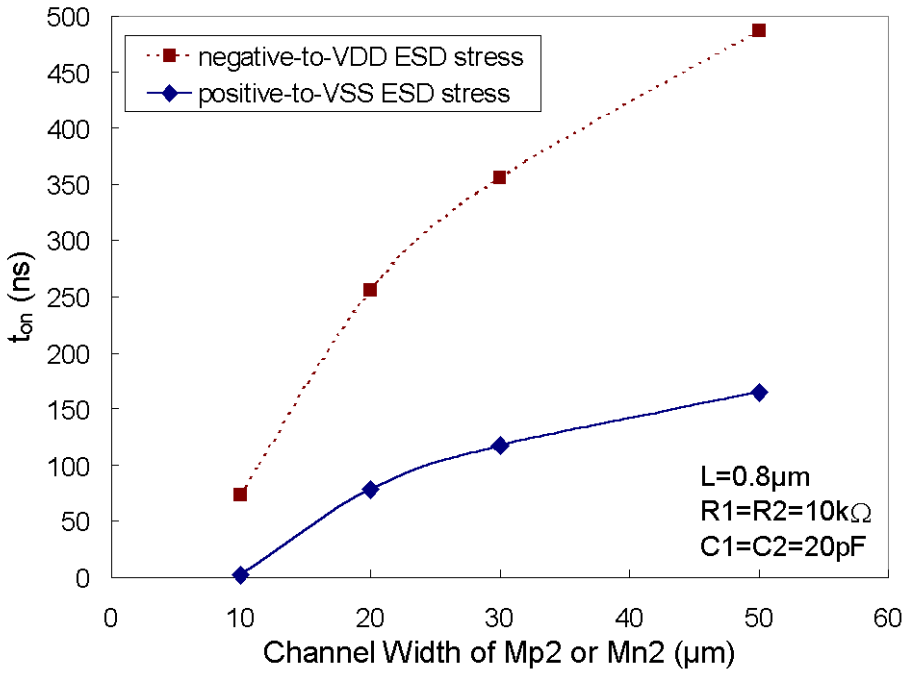
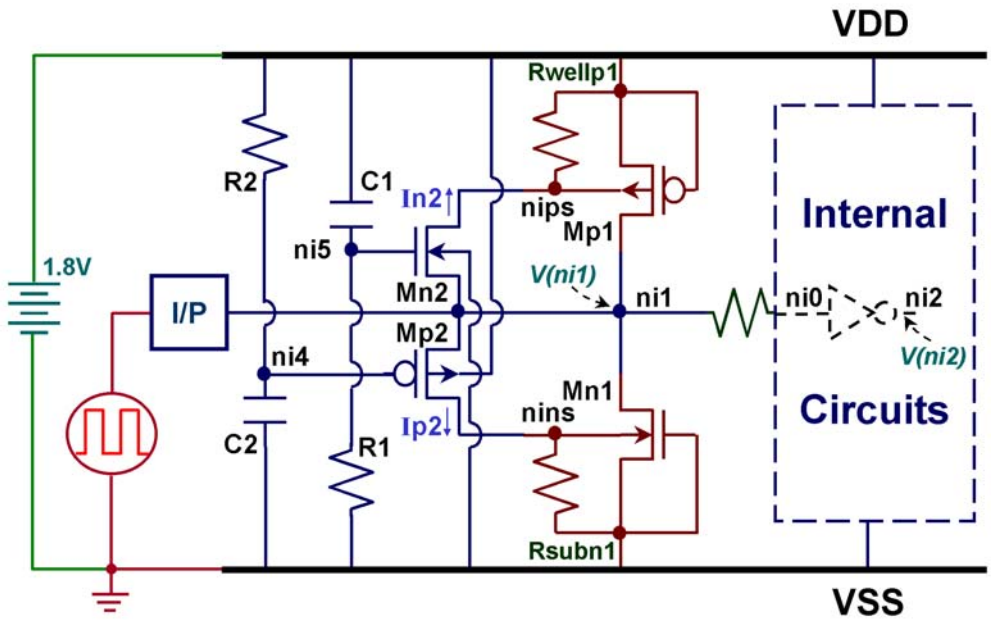
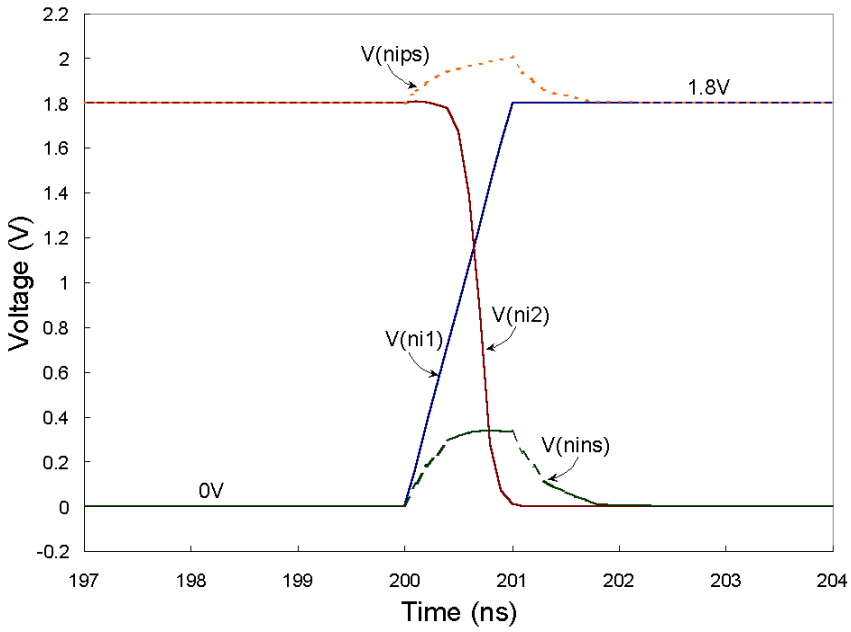


Fig. 4.6 The dependence between the turn-on time (t_{on}) and the device dimension of Mp2 or Mn2 in the proposed input ESD protection circuit during positive-to-VSS or negative-to-VDD ESD-stress conditions.



(a)



(b)

Fig. 4.7 (a) The circuit setup to simulate the voltage transition in the proposed input ESD protection circuit under the normal circuit operating condition with a 0-to-1.8V input signal. (b) The simulated voltage waveforms on the nodes ni1, ni2, nins, and nips of the proposed input ESD protection circuit when the input signal is applied on the input pad (the node ni1).

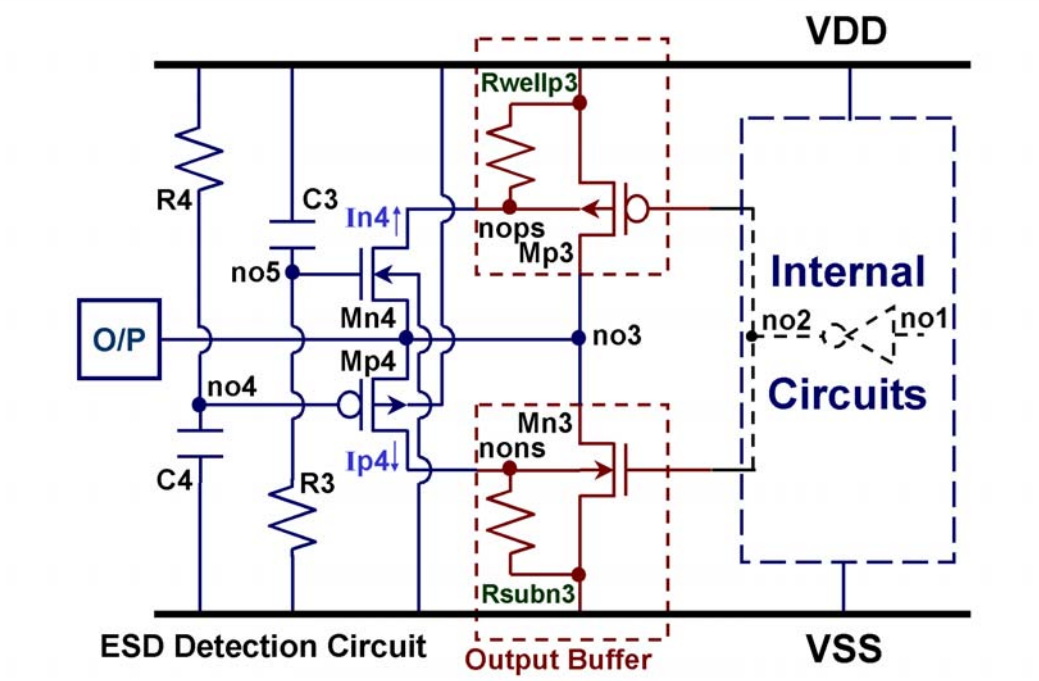


Fig. 4.8 Output ESD protection circuit with the proposed substrate-triggered design.

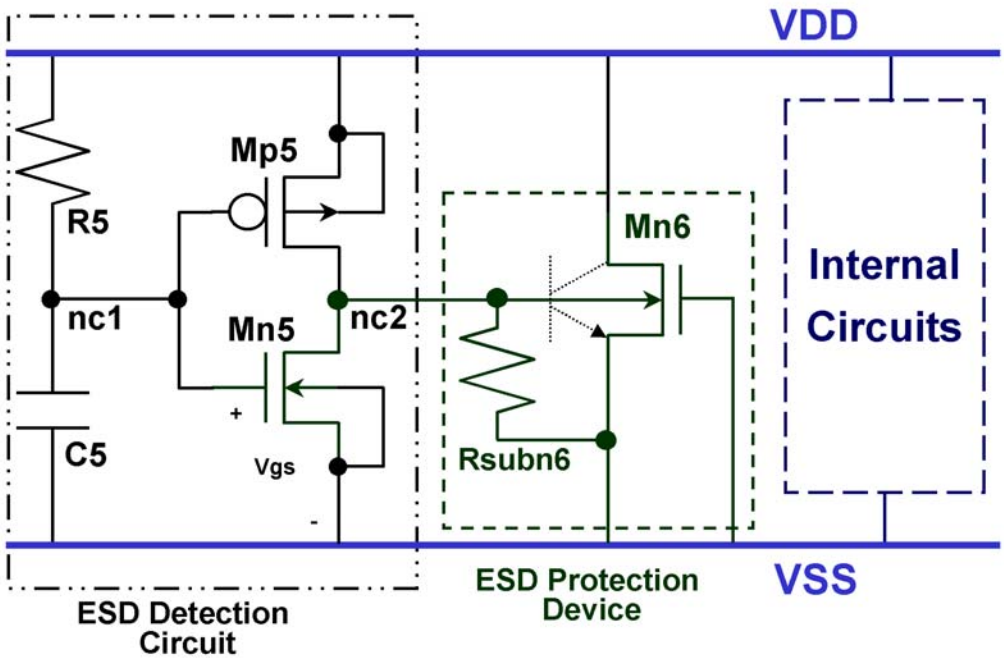


Fig. 4.9 Power-rail ESD clamp circuit with the proposed substrate-triggered design.

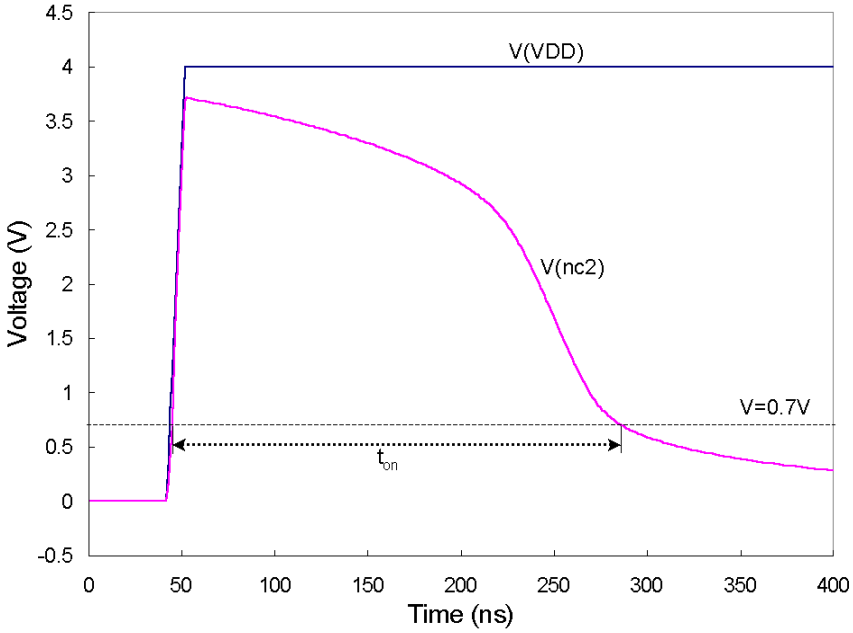


Fig. 4.10 The *HSPICE* simulated voltage waveforms on the VDD and the node nc2 of the proposed power-rail ESD clamp circuit under the positive ESD-stress condition, where a 4-V ramp voltage with a rise time of 10 ns is used to simulate the rising edge of an HBM ESD pulse.

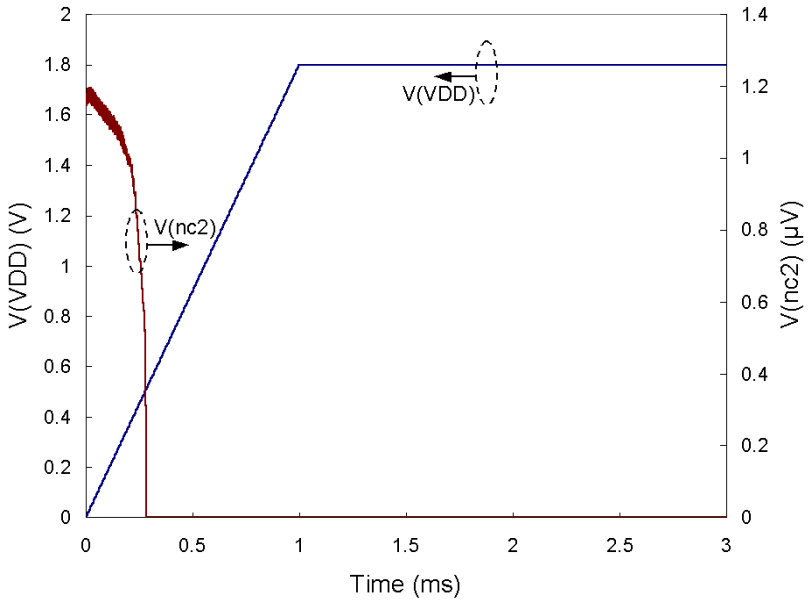


Fig. 4.11 The *HSPICE* simulated voltage waveforms on the VDD and the node nc2 of the proposed power-rail ESD clamp circuit under the normal power-on condition, where a 1.8-V ramp voltage with a rise time of 1 ms is applied to the VDD.

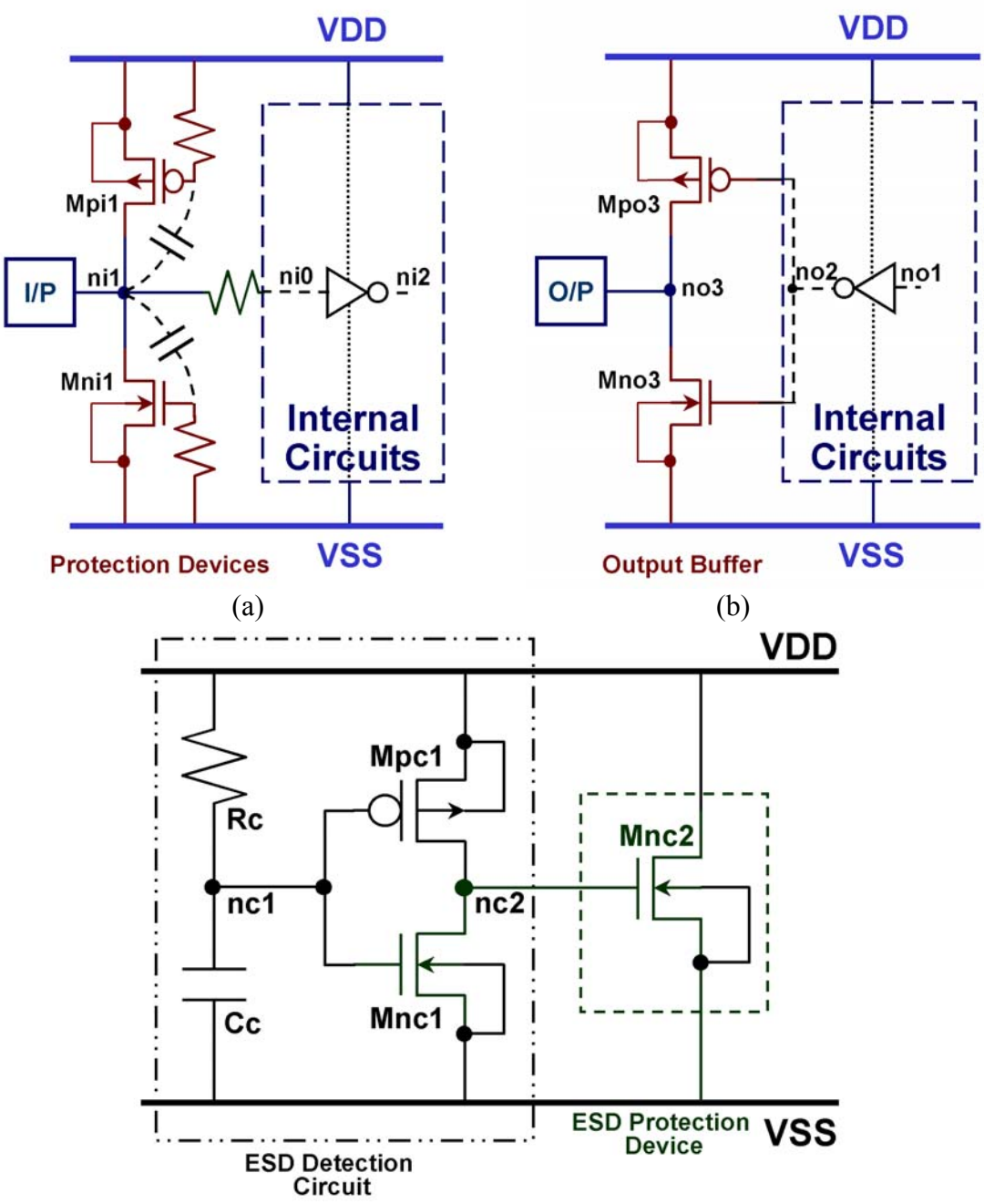


Fig. 4.12 Illustrations of the traditional (a) input ESD protection circuit, (b) output ESD protection circuit, and (c) power-rail ESD clamp circuit.

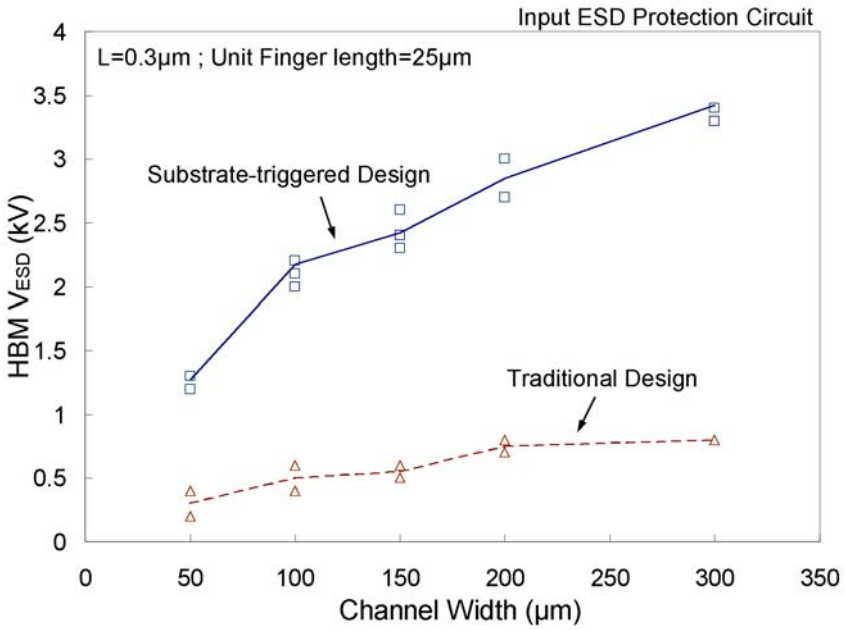


Fig. 4.13 Comparison on ESD robustness between the proposed substrate-triggered input ESD protection circuit and the traditional input ESD protection circuit.

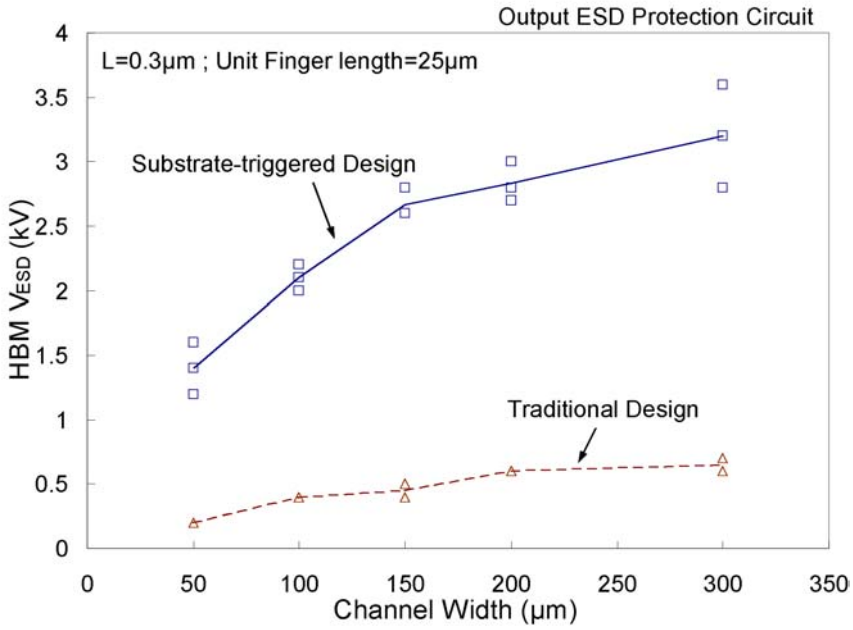


Fig. 4.14 Comparison on ESD robustness between the proposed substrate-triggered output ESD protection circuit and the traditional output ESD protection circuit.

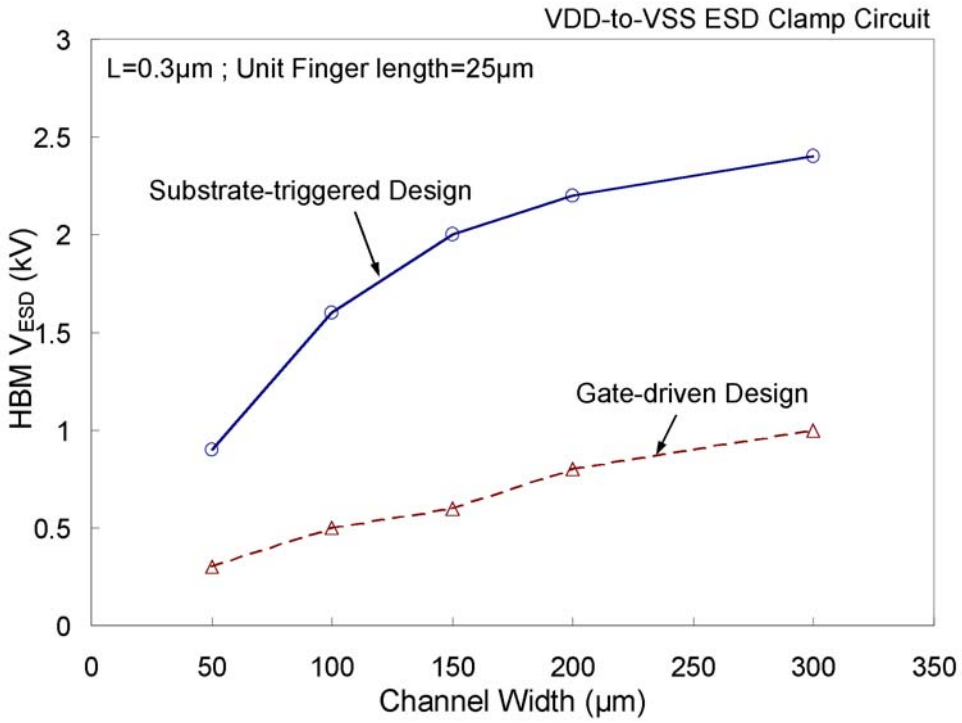
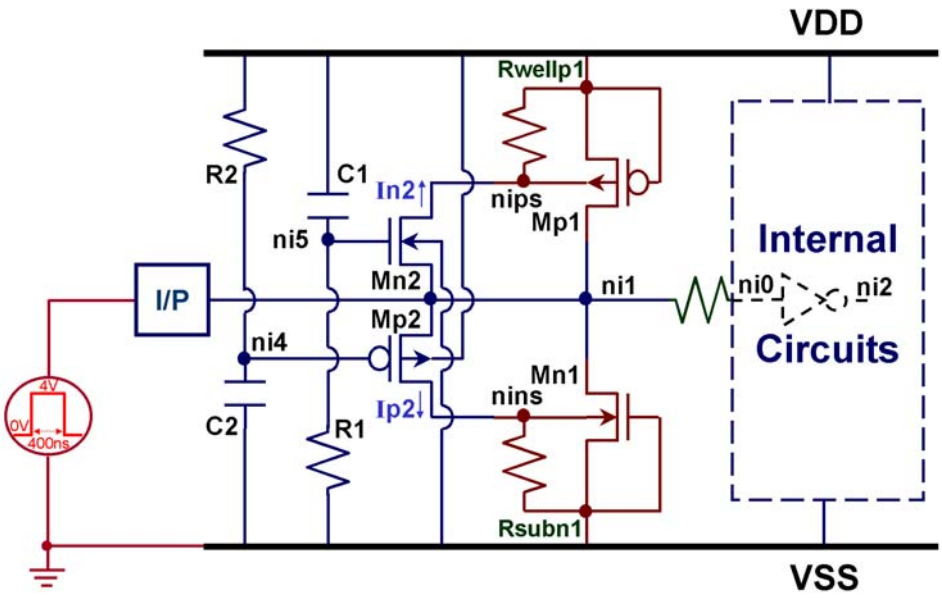
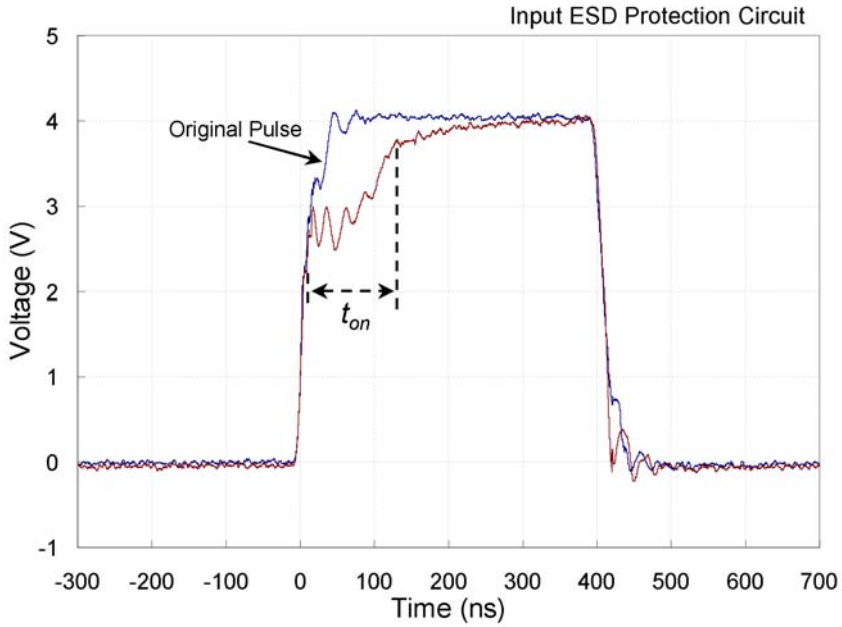


Fig. 4.15 Comparison on ESD robustness between the proposed substrate-triggered power-rail ESD clamp circuit and the gate-driven power-rail ESD clamp circuit.

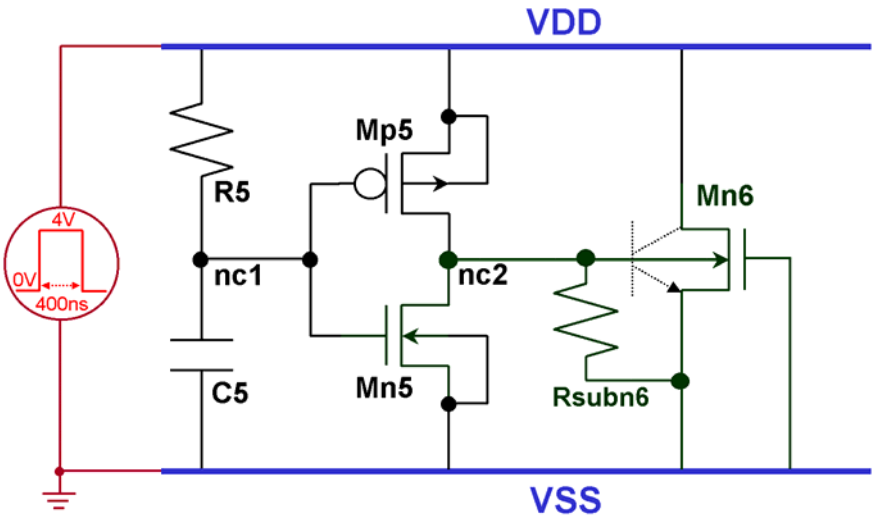


(a)

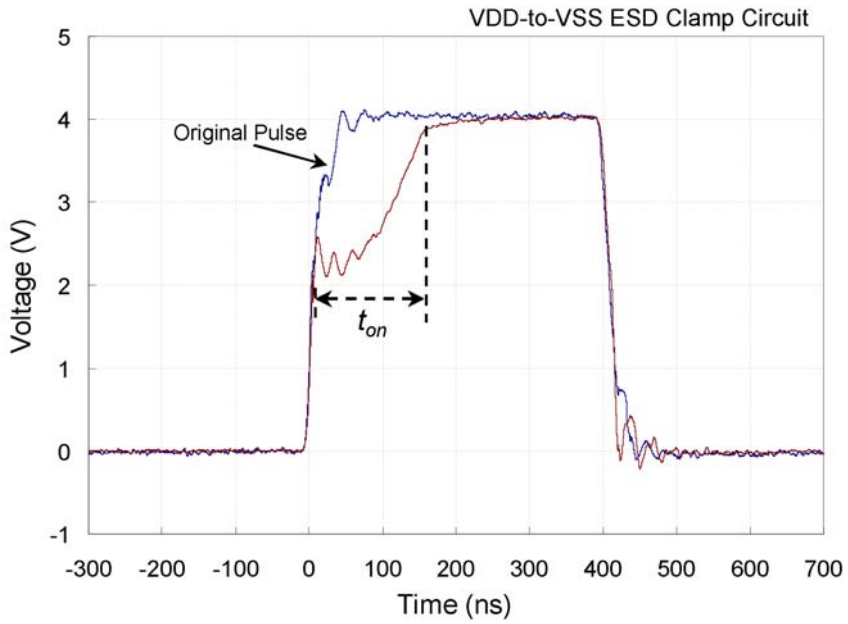


(b)

Fig. 4.16 (a) The experimental setup to verify the turn-on efficiency of the proposed input ESD protection circuit with substrate-triggered design, where a 4-V voltage pulse with a rise time of ~10 ns is used to simulate the rising edge of a positive-to-VSS HBM ESD event. (b) Comparison between the original 0-to-4V voltage waveform generated from a pulse generator and the degraded voltage waveform on the input pad of the proposed input ESD protection circuit.

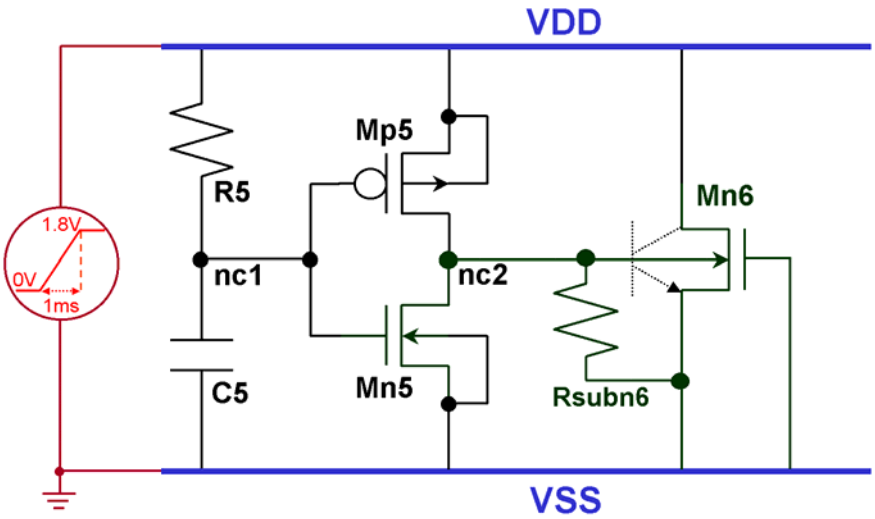


(a)

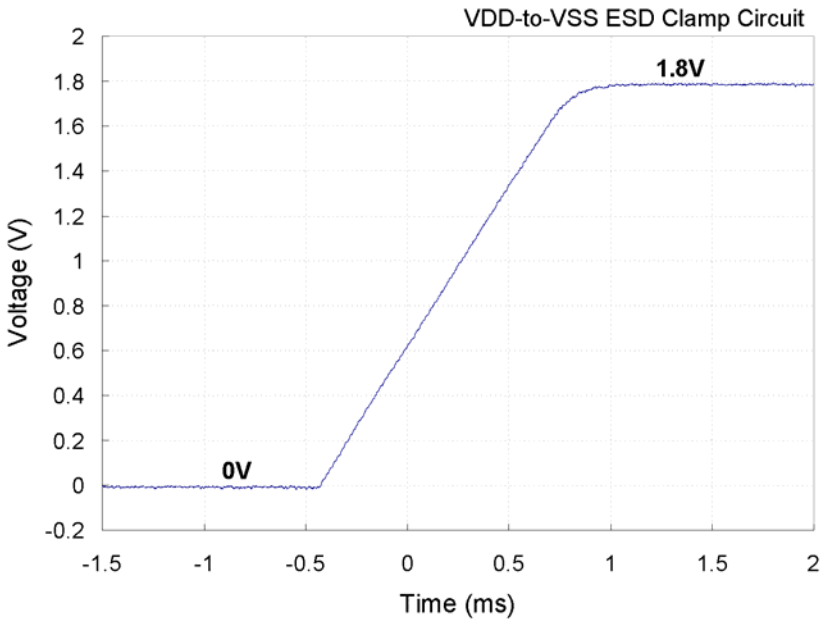


(b)

Fig. 4.17 (a) The experimental setup to verify the turn-on efficiency of the proposed power-rail ESD clamp circuit with substrate-triggered design, where a 4-V voltage pulse with a rise time of ~10 ns is used to simulate the rising edge of a positive VDD-to-VSS ESD event. (b) Comparison between the original 0-to-4V voltage waveform generated from a pulse generator and the degraded voltage waveform on the VDD of the proposed power-rail ESD clamp circuit.



(a)



(b)

Fig. 4.18 (a) The experimental setup to verify the power-on transition of the proposed power-rail ESD clamp circuit with substrate-triggered design, where a 0-to-1.8V ramp voltage with a rise time of 1 ms is used to simulate the normal power-on event. (b) The measured voltage waveform on the VDD of the proposed power-rail ESD clamp circuit, which is not degraded by the power-rail ESD clamp circuit.

CHAPTER 5

SUBSTRATE-TRIGGERED ESD PROTECTION CIRCUIT WITHOUT EXTRA PROCESS MODIFICATION

With aggressive device scaling, the circuit operating voltage had been decreased correspondingly. Some early 5-V systems changed from 5 V to 3.3 V, or even 1.8 V. Thus, system voltages were no longer 5 V but mixed with 5 V and 3.3 V. For mixed-voltage input design [103]-[106], the IC with 3.3-V power supply needs to accept 5-V input signals. In the traditional ESD protection design, the normal input signal with high voltage may turn on the ESD protection device, which is connected between input pad and VDD power line. Therefore, the traditional input ESD protection circuit must be modified for application in this situation of mixed-voltage interface.

The ESD stress on an input pin has four modes of pin combination: positive-to-VSS, negative-to-VSS, positive-to-VDD, and negative-to-VDD [5]. To protect the thinner gate oxide of input stage in CMOS IC's under all ESD-stress conditions, a traditional two-stage ESD protection circuit for digital input pin is shown in Fig. 5.1. A gate-grounded short-channel NMOS is used as the secondary protection device to clamp the overstress voltage across the gate oxide of the input circuits. To provide a high ESD level, a robust field oxide device (FOD) is often used as the main discharge element in the primary protection stage to discharge ESD current on pad. Between the primary stage and the secondary stage, a resistor R is added to limit the ESD current flowing through the short-channel NMOS in the secondary stage. The primary ESD clamp device must be triggered on to discharge ESD current before the gate-grounded NMOS (gg-NMOS) in the secondary stage is damaged by the overstress ESD current. If the primary ESD clamp device has a high turn-on voltage, the resistance of R should be large enough in the order of kΩ. Under the positive-to-VSS and negative-to-VSS ESD stress conditions, the ESD current can be discharged through the FOD and gg-NMOS. However, in the mixed-voltage situation, the diode or PMOS connected from the pad to VDD power line is forbidden by the normal circuit operation with a high-voltage input signal. Without the diode or PMOS connected from the pad to VDD, the

positive-to-VDD and negative-to-VDD ESD stresses are still discharged from the pad to VSS power line, and then conducted through the power-rail ESD clamp circuit to the grounded VDD pin. The power-rail ESD clamp circuit is important under such ESD-stress conditions to bypass the ESD current away from the internal circuits [6].

To sustain the required ESD level, the ESD protection device must be drawn with larger device dimensions, which was often realized in layout with multiple fingers to reduce total silicon area. But, during ESD stress, the multiple fingers of ESD protection MOSFET cannot be uniformly turned on. Only several fingers of the MOSFET were turned on and therefore damaged by ESD [62]. This often causes a low ESD level in the ESD protection circuit, even if the MOSFET has a large device dimension. To efficiently improve the turn-on uniformity among those multiple fingers, the gate-driven design [62]-[65] had been reported to increase ESD robustness of the large-device-dimension NMOS. Recently, ESD robustness of the gate-driven NMOS had been found to be decreased dramatically when the gate voltage is somewhat increased [65], [78]. The gate-driven design causes ESD current mainly discharging through the surface channel of NMOS, therefore NMOS is easily burned out by ESD energy. To avoid the sudden degradation on ESD level of the gate-driven devices, the substrate-triggered design had been proposed to improve ESD robustness of the ESD protection devices [68]-[74].

In this chapter, a new substrate-triggered design is proposed to improve the ESD robustness of the input ESD protection circuit without extra salicide-blocking and ESD-implantation process modifications. Such design can be further modified for using to improve ESD robustness of CMOS output buffer.

5.1 SUBSTRATE-TRIGGERED ESD PROTECTION CIRCUIT

5.1.1 The Substrate-triggered Input ESD Protection Circuit

The schematic diagram of the input ESD protection circuit with the substrate-triggered design is shown in Fig. 5.2. This input ESD protection circuit is combined with a short-channel gate-grounded NMOS Mn1, a resistor R, and a field oxide device (FOD). The short-channel gate-grounded NMOS Mn1 with lower snapback breakdown voltage can be more quickly triggered on than the FOD with larger breakdown voltage during ESD stress.

Both the source and the substrate of the gate-grounded NMOS Mn1 is connected with the substrate of the FOD to form a trigger path on the base node of the parasitic lateral bipolar junction transistor (LBJT), which is drawn by the dashed line beside the FOD of Fig. 5.2. The collector/emitter of parasitic LBJT is formed from the drain/source of the FOD, and the base formed from the substrate of the FOD. To effectively trigger on the parasitic LBJT, a suitable voltage has to be applied on the resistance R to turn on the base-emitter junction of parasitic LBJT during ESD stress.

When the positive ESD voltage is stressed on the input pad with VSS grounded, the ESD voltage can trigger the NMOS Mn1 into snapback breakdown. Therefore, a generated substrate current by the turned-on NMOS Mn1 will flow into the base of the parasitic LBJT in the FOD. Because the NMOS with shorter channel length has smaller snapback breakdown voltage, the channel length of the NMOS Mn1 has to be designed as small as possible to quickly turn on the NMOS Mn1 during the positive ESD event. In the input ESD protection circuit of Fig. 5.2, the parasitic LBJT of FOD will be triggered on by the triggering current, which is generated from NMOS Mn1. When the FOD in Fig. 5.2 is applied with a positive substrate bias voltage, the breakdown voltage of the FOD will be lower than the drain breakdown voltage of the FOD without base bias. Therefore, in the ESD event, the combination of the NMOS Mn1 and the resistor R can provide a substrate-triggered current to trigger on the parasitic LBJT of FOD to provide the desired ESD protection for the input stage of the IC in deep-submicron CMOS process.

During negative-to-VSS ESD-stress condition, the negative ESD voltage can forward bias the p-n junction between the substrate and the drain of FOD or NMOS Mn1 to discharge the ESD current. The forward-biased parasitic diode of FOD and NMOS Mn1 can sustain higher ESD level. During the positive-to-VDD and negative-to-VDD ESD-stress conditions, the ESD current is still discharged from the pad to VSS power line, and then conducted through the power-rail ESD clamp circuit to the grounded VDD pin.

By using substrate-triggered design, the FOD in Fig. 5.2 can be uniformly turned on to sustain higher ESD level than traditional design without substrate-triggered design during positive ESD stress conditions. The two-stage ESD protection design in Fig. 5.1 can only provide high ESD level for the digital input pins. But the large series resistance and the junction capacitance in the ESD clamp devices causes a long RC delay to the input signal, therefore this is not suitable for analog pins. For current-mode input signal or high-frequency applications, the series resistance between the input pad and input circuits is forbidden.

Therefore, the two-stage ESD protection design in Fig. 5.1 is no longer suitable for analog applications. But, the proposed substrate-triggered ESD protection circuit without the series resistance, as that shown in Fig. 5.2, can provide lower triggered voltage to protect the thin gate oxide and be suitable for analog applications.

5.1.2 Alternative Substrate-triggered Input ESD Protection Circuit

An alternative design of the proposed input ESD protection circuit with a long channel length NMOS is shown in Fig. 5.3. The alternative design is similar to the proposed circuit in Fig. 5.2, but the long channel length NMOS is used in place of the FOD. The schematic diagram of the ESD protection circuit includes a first NMOS Mn1, a resistor R, and a second NMOS Mn2. Both the source and the substrate of the first NMOS Mn1 are also connected together to the substrate-triggered point of the second NMOS Mn2. The gate of second NMOS Mn2 is connected with the VSS power line. The first NMOS Mn1 has to be designed with smaller snapback breakdown voltage than the second NMOS Mn2 to effectively form the substrate-triggered current. Further, a parasitic LBJT is also included in the second NMOS Mn2, as drawn in dashed lines beside the second NMOS Mn2 in Fig. 5.3. The parasitic LBJT has a collector/emitter formed from the drain/source of the second NMOS Mn2, and a base formed from the substrate of the second NMOS Mn2.

Under positive ESD-stress events, the parasitic LBJT in the second NMOS Mn2 can be triggered on by the substrate-triggered current from the NMOS Mn1 and resistor R. During all ESD-stress conditions, the operation principles of the input ESD protection circuit with long channel length NMOS are similar to that of the input ESD protection circuit with FOD device.

5.1.3 Realization of Substrate-Triggered ESD Protection Circuits

To realize the effective substrate-triggered input ESD protection circuit, the circuit is merged in a device structure. The cross-sectional view and layout top view of the input ESD protection circuit in Fig. 5.2 are shown in Fig. 5.4, which is fabricated in a 0.25-μm salicided shallow-trench-isolation CMOS technology [107]. The symmetric device structure of Fig. 5.4 allows a balanced current that can help increase the current uniformity among the multiple fingers of input ESD protection circuit. As shown in Fig. 5.4, the NMOS Mn1 with thin gate oxide, the resistor R, and the FOD are formed on a p-type substrate, but no salicide-blocking

and ESD-implantation process modifications are added in the device structure.

As shown in Fig. 5.4, a first N-well is connected to the input pad and also to the drain of the NMOS Mn1 to protect the NMOS Mn1 from being burned out during ESD stress. Because the NMOS Mn1 will be formed with a short channel, an LDD, and a silicide-based diffusion area, which would be weaken on its ESD robustness, the first N-well can allow the NMOS Mn1 to sustain the ESD current overstress before the FOD is being triggered on. The NMOS Mn1 can trigger on the FOD through the p-type substrate, but it is not the primary element to bypass the ESD current. Therefore, the provision of the first N-well would not affect the NMOS Mn1 in its triggering capability.

The resistor R is realized by using the parasitic substrate resistance. The second N-well is formed in the drain of the FOD. This N-well also has an effect to increase the equivalent resistance of the resistor R in the ESD protection circuit. The highly doped n-type diffusion area in the source of the FOD can collect the triggering current from the highly-doped p-type diffusion area to apply a forward bias voltage across the base-emitter junction of the parasitic LBJT in the FOD to trigger on the parasitic LBJT in the FOD. The geometric spacing between two highly-doped n-type diffusions of the FOD is marked as “B” in Fig. 5.4 and it can also affect the turn-on efficiency of the parasitic LBJT during ESD stress. In Fig. 5.4, the spacing between the edge of drain diffusion and the edge of N-well is kept at 0.3 μm for those devices with different “B” spacing. Therefore, when the NMOS Mn1 is triggered on due to an ESD stress and a triggering current is flow through the highly-doped p-type diffusion to the p-type substrate. The substrate-triggered current will be collected by the highly doped n-type diffusion in the source of the FOD to bias the base-emitter junction of the parasitic LBJT in the FOD. This can cause the FOD to be triggered on, thus the ESD current is discharged from the input pad into the VSS power line. The ESD protection circuit of the input ESD protection circuit is thus considerably enhanced on its ESD robustness through the substrate-triggered design.

The cross-sectional and layout top view of the input ESD protection circuit in Fig. 5.3 are shown in Fig. 5.5, which is fabricated in a deep-submicron salicided CMOS process. In Fig. 5.5, the realization of the input ESD protection circuit is fabricated and formed with a first N-well and a second N-well. The first N-well can suppress the ESD current flowing through the short-channel NMOS Mn1. The second N-well covers partial area of the source diffusion of the second NMOS Mn2, as that shown in Fig. 5.5. The second N-well can enhance the performance of the parasitic LBJT in the second NMOS Mn2 and increase the

substrate resistance of R in Fig. 5.3. The channel length of the NMOS Mn2 is marked as “B” to compare with the FOD device. No salicide-blocking and ESD-implantation process modifications are added for the input ESD protection circuit.

5.2 EXPERIMENTAL RESULTS

The robustness of ESD protection devices can be investigated by the ESD tester. The *ZapMaster* ESD tester, produced by Keytek Instrument Corp., is used to measure the human-body-model (HBM) ESD level of the fabricated testchips. The failure criterion is generally defined at 1-μA leakage current under 1.1 times VDD bias, when the ESD protection circuit is kept off. In the proposed design, the core circuits are operated under 3.3-V VDD bias. So, the failure criterion is defined at 1-μA leakage current under 3.63 V. To investigate the turn-on behavior of device during high ESD current stress, transmission line pulsing (TLP) technique has been widely used to measure the second breakdown characteristics of devices [79], [83]. The TLPG (transmission line pulse generator) with a pulse width of 100 ns is used to find the It2 (second breakdown current) of the fabricated NMOS’s under different substrate biases.

5.2.1 Device Characteristics

The proposed input ESD protection circuits with thin gate oxide, salicide diffusion, but without ESD implantation have been designed and fabricated in the salicided CMOS process. Comparing to the traditional design, the gg-NMOS devices with salicide-blocking process are also designed and fabricated in the 0.25-μm salicided shallow-trench-isolation CMOS process. To further understand the characteristics of the LBJT’s in FOD of Fig. 5.2 and in NMOS Mn2 of Fig. 5.3, the stand-alone FOD and NMOS Mn2 are also fabricated in the testchip. The *Tek 370A* curve tracer, produced by Tektronix Inc., is used to measure the DC I-V curve of the LBJT in FOD during DC stress. The test circuit and the measured DC I-V curve of the LBJT are shown in Fig. 5.6(a). The snapback breakdown voltage of the FOD is as high as 11.9 V, but the trigger voltage for the FOD entering into its snapback region is significantly reduced if there is a triggering current into its base. The DC I-V curve of the NMOS Mn2 with long channel length (L=2μm) in Fig. 5.3 is measured as that shown in Fig. 5.6(b). The test circuit

is also shown in Fig. 5.6(b). The snapback breakdown voltage of the NMOS Mn2 is as high as 8.4 V, but the trigger voltage for the NMOS Mn2 entering into its snapback region is also reduced if there is a triggering current into its base. The DC I-V curve of the whole substrate-triggered input ESD protection circuit with FOD in Fig. 5.2 is measured and shown in Fig. 5.7, which is the combination of the DC I-V curves of the FOD, the NMOS Mn1, and the substrate resistance. In Fig. 5.7, the trigger voltage of the input ESD protection circuit is lowered to only 6.4 V. So, the trigger voltage of the FOD has been significantly reduced by the substrate-triggered current generated from the NMOS Mn1 with short channel length. The turn-on efficiency of the FOD is also enhanced by the substrate-triggered current. Therefore, this input ESD protection circuit with FOD can provide effective voltage-clamping function to protect the thinner gate oxide of 50Å in the 0.25-μm salicided CMOS technology.

5.2.2 TLP Measurement

The secondary breakdown current (It2) of the input ESD protection circuit is also measured by the TLP (transmission line pulsing) system. When the HBM ESD-stress current on the input pad is greater than the It2 of the input ESD protection circuit, the input ESD protection circuit is permanently damaged by the overstress current. Adjusting the device layout parameters of the FOD (or the NMOS Mn2), the It2 can be proportionally increased. Thus, the ESD robustness of the input ESD protection circuit can be adjusted. Two important device layout parameters, which have strong effect on the HBM ESD level of the input ESD protection circuit, are the “B” spacing in Fig. 5.4 (Fig. 5.5) and the total channel width of the FOD (or the NMOS Mn2) in the input ESD protection circuits. The TLP measured I-V curves of the input ESD protection circuits in Fig. 5.4 and Fig. 5.5 with different “B” spacings but with the same channel width of 150 μm are shown in Fig. 5.8. From those TLP measured It2 as that shown in Fig. 5.8, the dependences of the secondary breakdown current It2 on the “B” spacing of the input ESD protection circuits with FOD and NMOS Mn2 (W=150μm) are measured and shown in Fig. 5.9(a). When the “B” spacing is increased from 1 μm to 5 μm, the It2 of the input ESD protection circuit with FOD is decreased from 1.38 A to 1.22 A in the TLP test results. But, the It2 of the input ESD protection circuit with NMOS Mn2 is increased from 1.11 A to 1.42 A when the “B” spacing is increased from 1 μm to 5 μm. The dependence of secondary breakdown current It2 on the channel width of the FOD and the NMOS Mn2 of the input ESD protection circuits are also measured and shown in Fig. 5.9(b). The FOD and

NMOS with longer channel width have larger secondary breakdown current It2.

5.2.3 ESD Test

The fabricated substrate-triggered input ESD protection circuits are also verified by the HBM ESD test. To compare with the traditional design, the input protection circuit with gg-NMOS is also verified by the HBM ESD test. The HBM ESD test results are shown in Figs. 5.10. In Fig. 5.10(a), the HBM ESD levels of the input ESD protection circuit with the FOD (W=150μm) is decreased from 3250 V to 2750 V as the "B" spacing in the FOD is increased from 1μm to 5μm. But, the HBM ESD level of the input ESD protection circuit with the NMOS Mn2 (W=150μm) is increased from 2250 V to 3000 V as the "B" spacing in the NMOS Mn2 is increased from 1μm to 5μm. With a "B" spacing of 2μm in the device structure, the input ESD protection circuit with the FOD can sustain an ESD level of 3250V in the silicon area of 1725 μm^2, and that with the NMOS Mn2 can sustain an ESD level of 2500V in the same silicon area. But, the gg-NMOS protection circuit with 2-μm channel length and the same total channel width of 150 μm can only sustain an HBM ESD level of 1800V in the silicon area of 1328 μm^2. The proposed ESD protection circuit with FOD has the largest ESD robustness of 1.73 V/μm^2 than that with NMOS Mn2 of 1.33 V/μm^2 and the gg-NMOS of 1.2 V/μm^2. In Fig. 5.10(b), the ESD robustness of the input ESD protection circuit with the FOD or the NMOS Mn2 is increased as the total channel width of the FOD or the NMOS Mn2 is increased from 100 μm to 300μm. These HBM ESD test results in Fig. 5.10 are consistent with the TLP measured results of It2 in Fig. 5.9. From HBM ESD level per silicon area of the input ESD protection circuits with the FOD and NMOS Mn2 are increased 44% and 11% more than that with traditional gg-NMOS, while the "B" spacing of the ESD protection device is kept at 2μm and the channel width is kept at 150 μm.

5.3 MODIFIED DESIGN WITH ENHANCED TURN-ON SPEED

To enhance the turn-on speed of the proposed input ESD protection circuit for the mixed-voltage application, a modified schematic diagram of the substrate-triggered input ESD protection circuit is shown in Fig. 5.11(a). An *R-C* based gate-coupled circuit is used to enhance the turn-on speed of NMOS Mn3 in Fig. 5.11(a). The NMOS Mn4 or FOD can be

used as the main ESD protection device. When a positive ESD is charged to the input pad of the modified ESD protection circuit, the gate of NMOS Mn3 will be coupled with a positive voltage. Because the triggering voltage of NMOS Mn3, which is turned on by gate-coupled circuit, is smaller than the snapback breakdown voltage of the NMOS Mn1 in Fig. 5.3, the NMOS Mn3 of the modified ESD protection circuit can be quickly turned on to generate a triggering current into the substrate of NMOS Mn4 during the positive ESD stress. Therefore, the parasitic LBJT of NMOS Mn4 or FOD can be quickly triggered on to discharge the ESD current from input pad to VSS. So, the modified design can enhance the turn-on speed of the proposed substrate-triggered input ESD protection circuits.

To improve the ESD robustness of output stage, a schematic diagram of the substrate-triggered output ESD protection circuit is shown in Fig. 5.11(b). The PMOS Mp6 and NMOS Mn6 of the output buffer in the integrated circuit are used as the main ESD protection devices. Basing on the previous modification in Fig. 5.11(a), the output ESD protection circuits can be designed with symmetric structure to provide the ESD discharged paths during all ESD-stress conditions. During positive-to-VSS ESD stress condition, the circuits of C1-R1 and NMOS Mn5 are used to detect the positive ESD stress and form the triggering current to turn on the ESD protection devices of NMOS Mn6. During negative-to-VDD ESD stress condition, the circuits of C2-R2 and PMOS Mp5 are used to detect the negative ESD stress and form a triggering current to turn on the ESD protection devices of PMOS Mp6. Therefore, the substrate-triggered ESD protection circuits with gate-coupled technique can provide high turn-on speed and high ESD robustness for the input and output ESD protection designs.

5.4 SUMMARY

The proposed input ESD protection circuit by using the substrate-triggered technique has been practically verified in a 0.25-μm salicided shallow-trench-isolation CMOS process without extra salicide-blocking and ESD-implantation modifications. The trigger voltage of the proposed input ESD protection circuit with FOD is lowered from original 11.9 V to only 6.4 V to effectively protect the thinner gate oxide (50Å) of input stage in the 0.25-μm salicided CMOS process. The proposed ESD protection circuit can be designed in a compact device structure to enhance the substrate-triggered performance. Comparing to the traditional

ESD protection gg-NMOS, the ESD levels of the proposed input ESD protection circuits with FOD and NMOS Mn2, while the “B” spacing is kept at 2 μm and the channel width is kept at 150 μm, are increased 44% and 11% per silicon area, respectively. To enhance the turn-on speed of the input or output ESD protection circuit during ESD stress, the gate-coupled circuit can be merged into the proposed substrate-triggered ESD protection circuits. So, the proposed substrate-triggered ESD protection design can suitably apply on the input and output stages of IC’s in deep-submicron CMOS process.

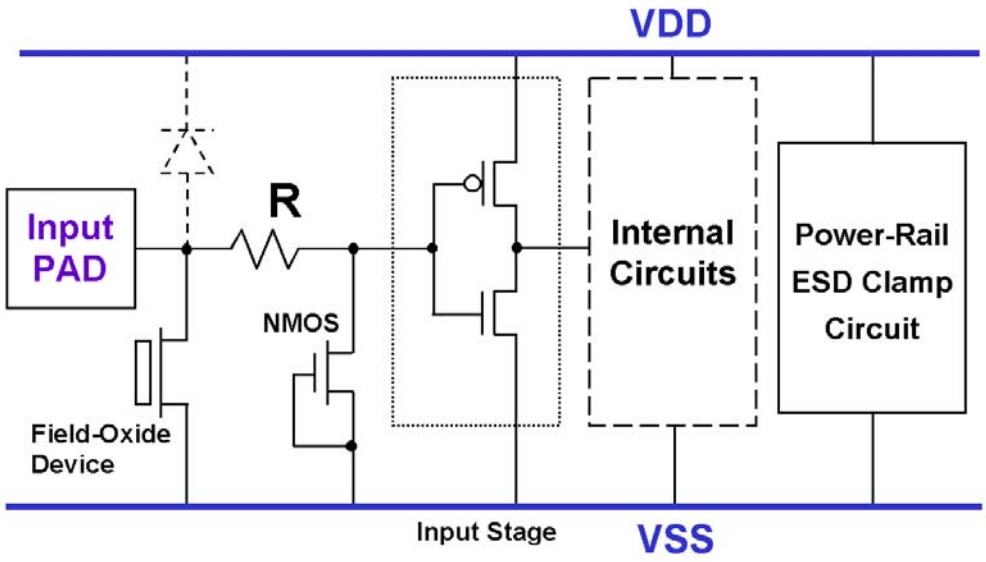


Fig. 5.1 The traditional input ESD protection circuit for digital input pin in CMOS IC's.

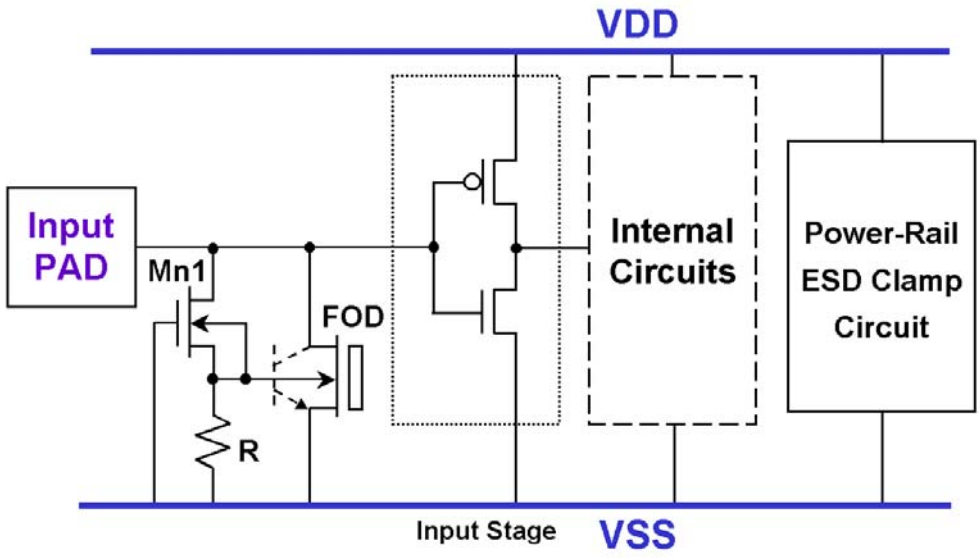


Fig. 5.2 The proposed substrate-triggered ESD protection circuit with field oxide device (FOD) to protect the thinner gate oxide of input stage.

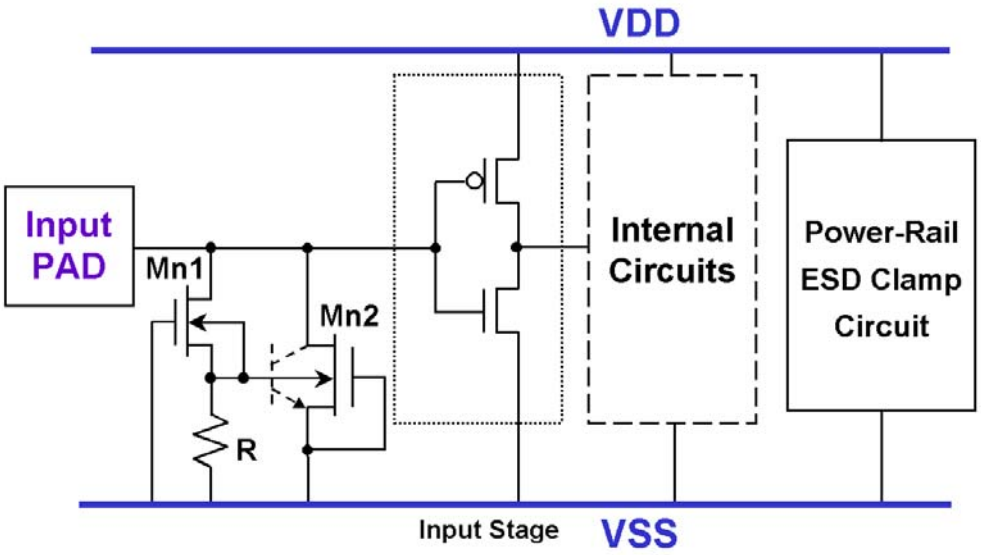


Fig. 5.3 An alternative design of the proposed substrate-triggered ESD protection circuit with long channel length NMOS to protect the thinner gate oxide of input stage.

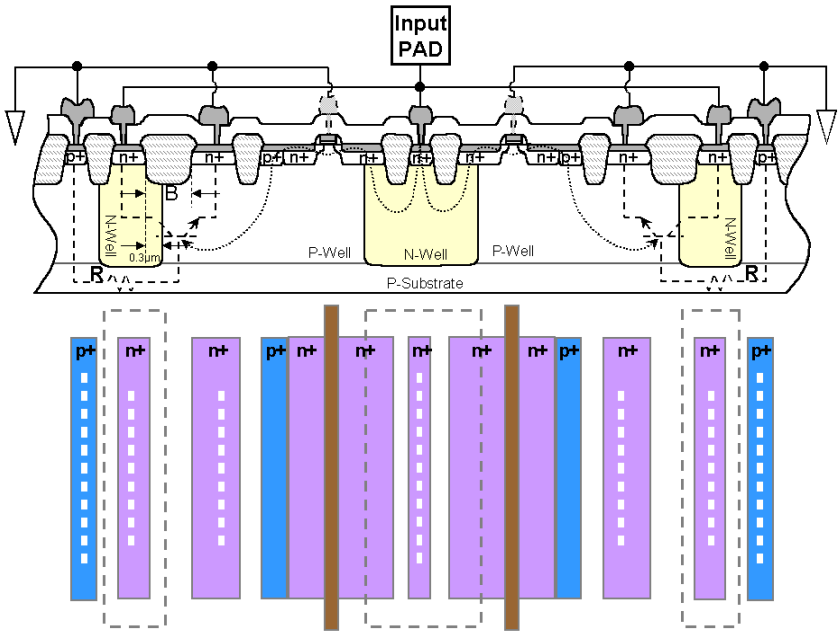


Fig. 5.4 The merged device structure of the proposed input ESD protection circuit with substrate-triggered FOD in Fig. 5.2.

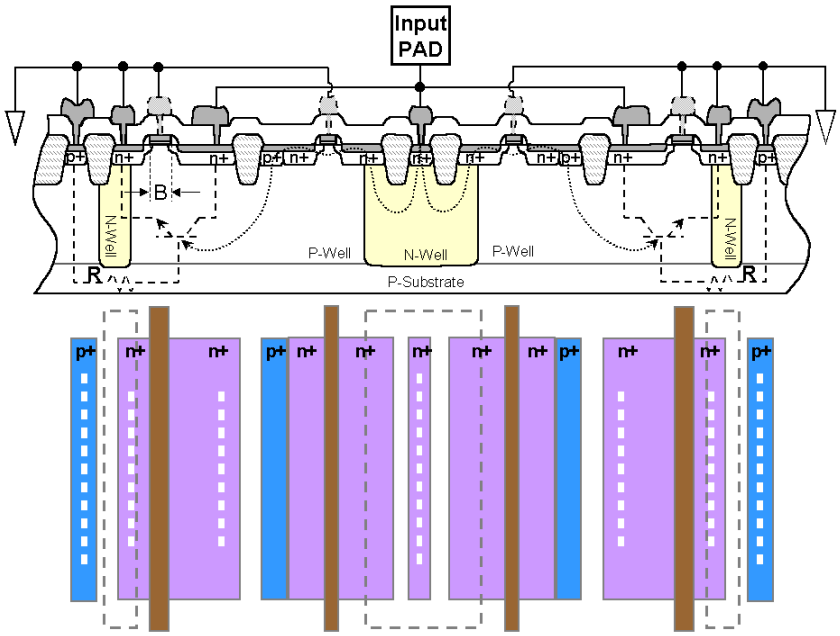
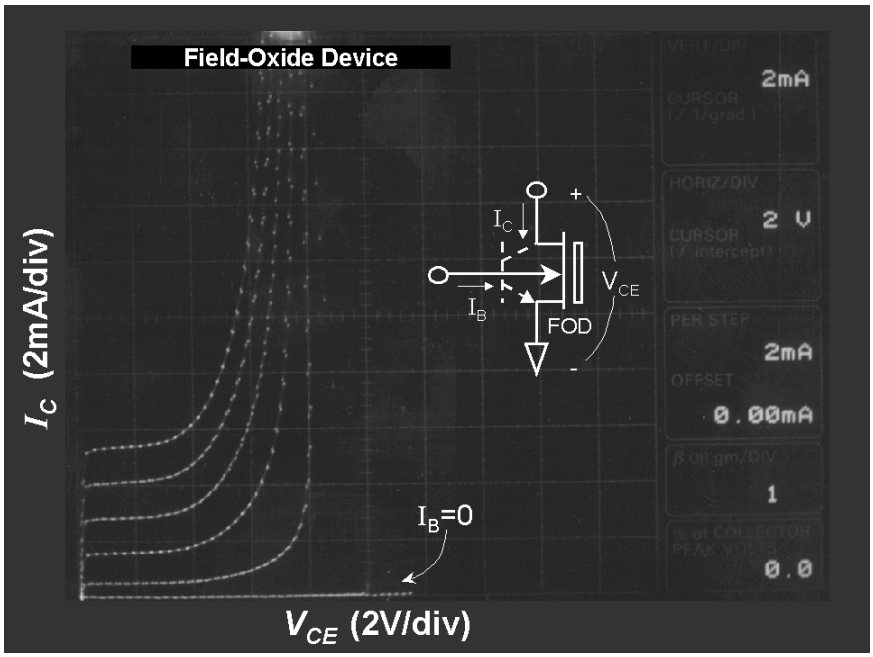
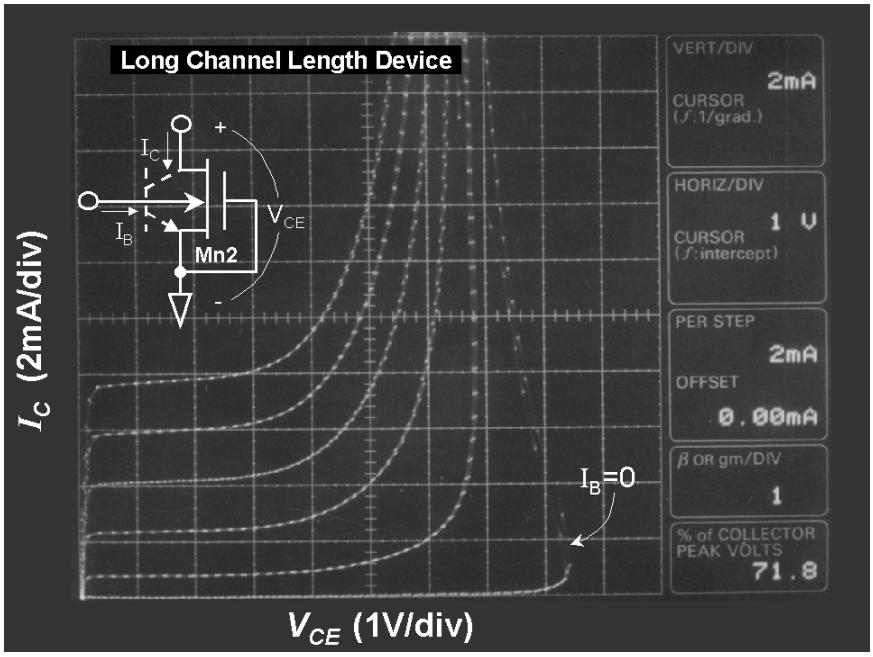


Fig. 5.5 The merged device structure of the alternative input ESD protection circuit with substrate-triggered NMOS Mn2 in Fig. 5.3.



(a)



(b)

Fig. 5.6 The measured DC I-V curve of a stand-alone (a) NMOS device, and (b) FOD, with a channel length of 2 μm under different substrate current biases.

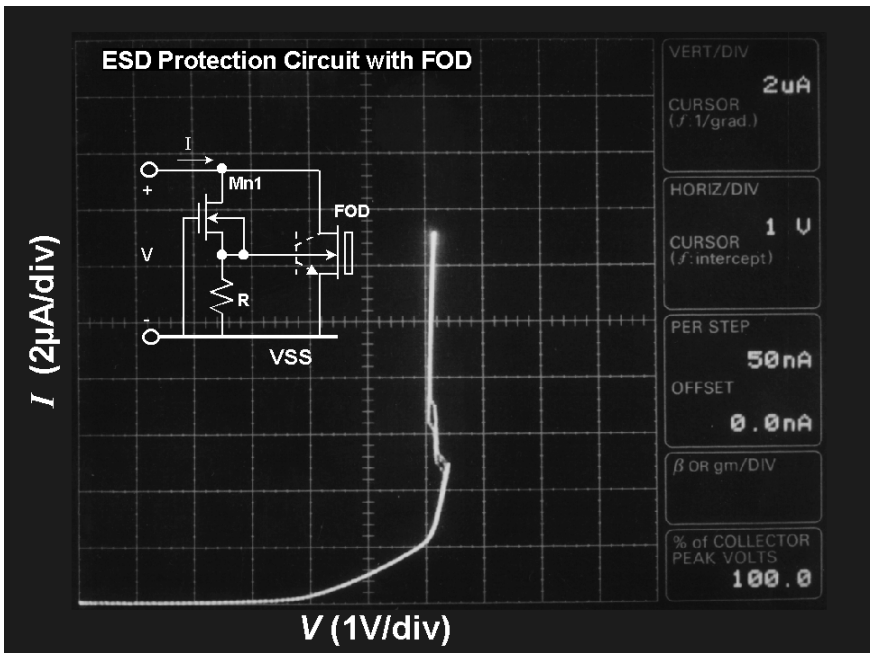


Fig. 5.7 The measured overall DC I-V curve of the proposed input ESD protection circuit with substrate-triggered FOD.

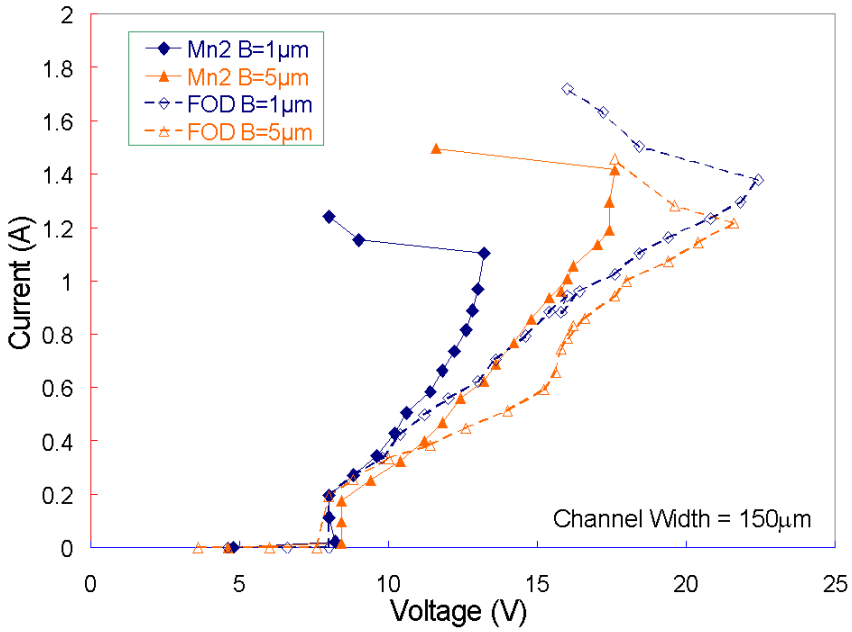
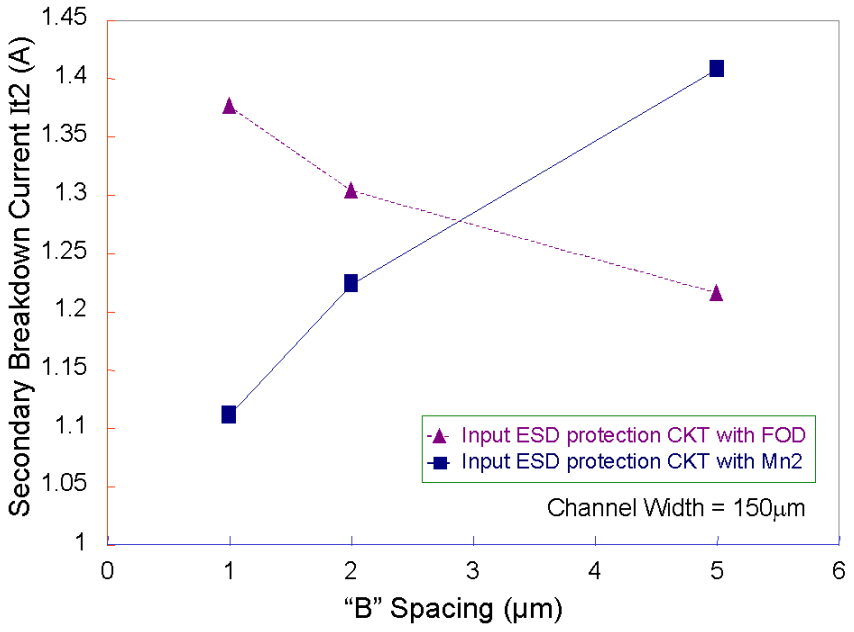
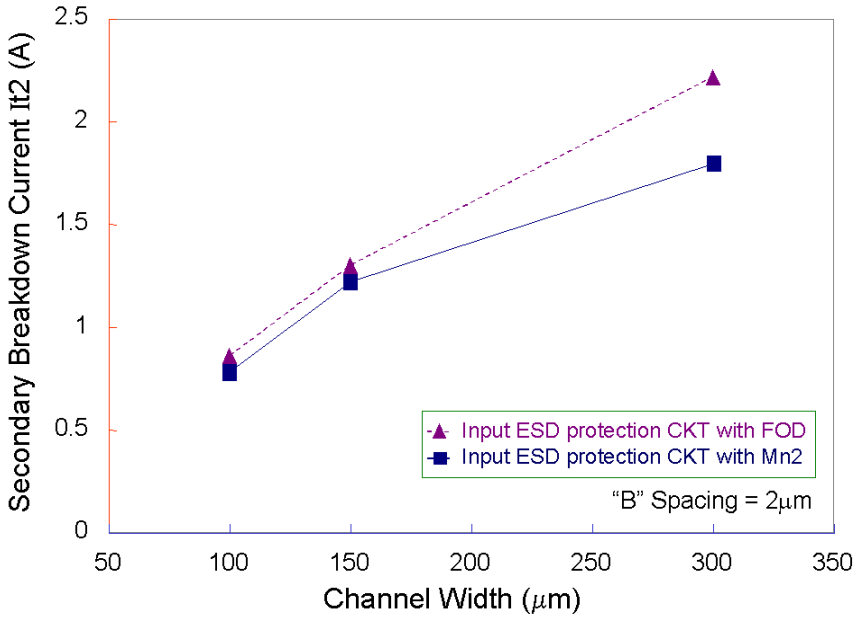


Fig. 5.8 The TLP measured I-V curves of the proposed input ESD protection circuits with NMOS Mn2 and FOD for different "B" spacings.

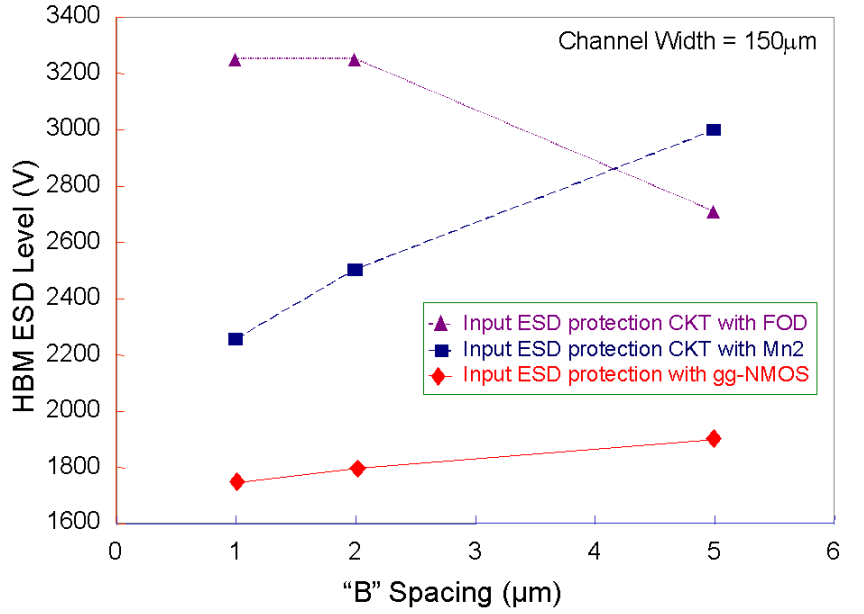


(a)

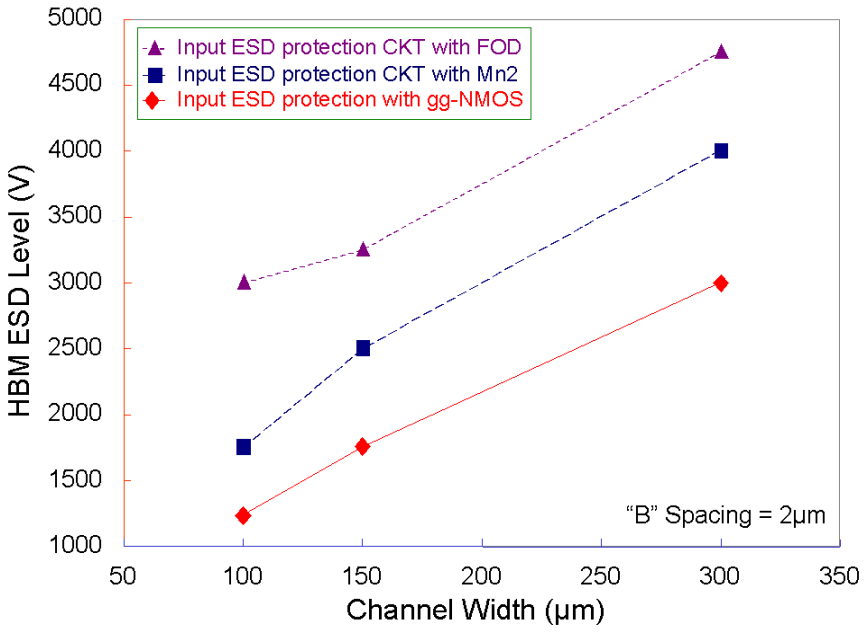


(b)

Fig. 5.9 The dependence of the It2 of the proposed input ESD protection circuits on (a) the "B" spacing, and (b) on the channel width, of the device structures in Fig. 5.4 (FOD) and Fig. 5.5 (Mn2).

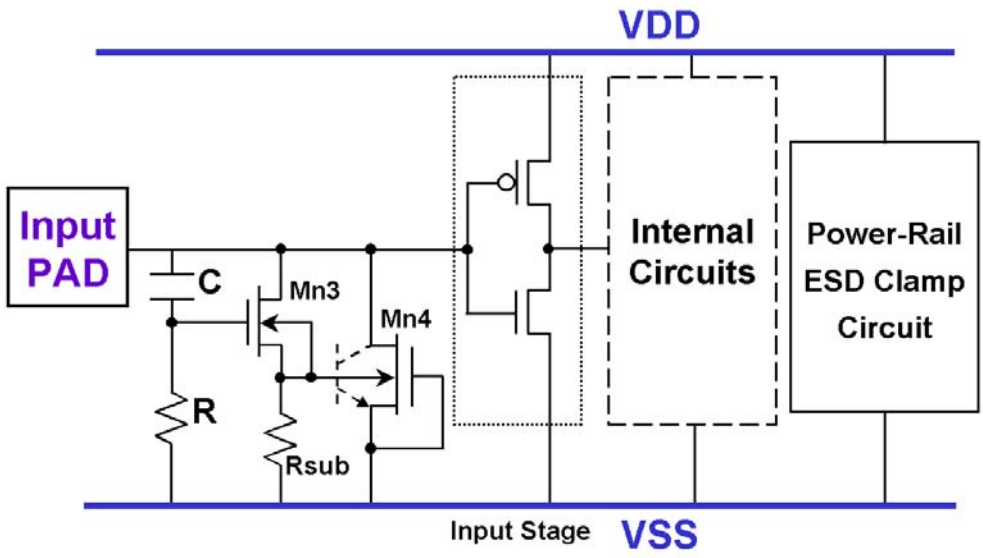


(a)

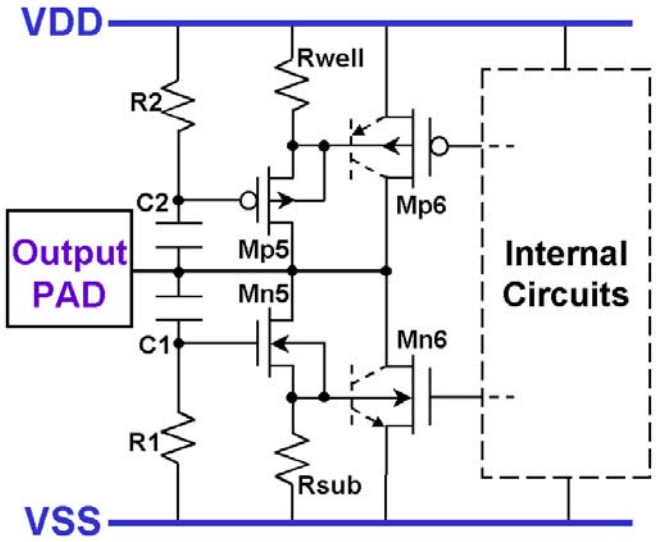


(b)

Fig. 5.10 The dependence of HBM ESD levels of the input ESD protection circuits (a) on the "B" spacing (channel length), and (b) on the channel width, of the ESD protection devices with the gg-NMOS, substrate-triggered FOD, or substrate-triggered NMOS Mn2.



(a)



(b)

Fig. 5.11 The modified substrate-triggered ESD protection design with enhanced turn-on speed for the (a) input, and (b) output, ESD protection circuits.

CHAPTER 6

POWER-RAIL ESD CLAMP CIRCUITS WITH SUBSTRATE-TRIGGERED TECHNIQUE

To overcome such unexpected ESD damage on the internal circuits beyond the input or output ESD protection circuits, some ESD clamp circuits across the VDD and VSS power rails had been reported [6], [108]-[113]. In [6] and [108]-[110], an *RC*-based ESD-detection circuit was used to turn on an NMOS to bypass the ESD current from VDD to VSS. The schematic circuit diagram of such a traditional design by gate-driven technique is illustrated in Fig. 6.1 with the cross-sectional view of NMOS device structure. During the ESD stress, the *RC*-based ESD-detection circuit conducts some ESD voltage from VDD power rail to bias the gate of the ESD-clamp NMOS. The positive gate voltage causes a strong inversion along the NMOS channel and leads to the ESD current focusing at the LDD peak structure. The ESD current, flowing through the very shallow junction depth of the LDD peak structure and the inversion layer along the channel, causes a very low ESD level on the NMOS. The over-biased gate voltage on NMOS had been reported to cause a lower second breakdown current (It_2) or ESD level on the NMOS devices, as compared to a gate-grounded NMOS. In order to sustain a desired 3-kV HBM ESD level, the ESD-clamp NMOS was designed with a huge device dimension of W/L = 8000μm/0.8μm in [108]. Such a huge ESD-clamp NMOS generally occupies a much more silicon area, which also causes a cost issue to IC products.

In [110]-[111], the diode string with multiple stacked diodes was reported as the ESD-clamp device across the power rails of an IC. The diode in the forward-biased condition can sustain a much higher ESD level than it in the reverse-biased condition. But, the forward-biased diode string conducts a considerable leakage current across the VDD and VSS power rails, when the IC with normal power supplies is operating in a higher temperature. In [112]-[113], the lateral SCR devices in CMOS process were used as the ESD-clamp device across the VDD and VSS power rails. The lateral SCR device can sustain a very high ESD stress with a much smaller silicon area, as compared to other ESD protection devices. But, the lateral SCR may be triggered on to cause latchup problem by the overshooting noise pulses across the power rails [114]-[118], when the IC is in the normal operation condition with

power supplies. In the system-level ESD testing [119] or the VDD-transient latchup testing [120], the SCR used as the ESD-clamp device across the power rails could be triggered on by the overshooting noise pulses to cause a serious latchup problem in CMOS IC's. Thus, an area-efficient and latchup-free ESD clamp circuit with quick turn-on speed across the power rails is strongly urged by the scaled-down CMOS IC's.

Recently, the substrate-triggered technique was reported to improve ESD level of NMOS devices in deep-submicron CMOS technologies for I/O ESD protection [68]-[74]. The potential of local substrate under the NMOS device is charged up in ESD-stress condition by both circuit design and suitable layout arrangement to earlier initiate the bipolar action of the NMOS device. When the parasitic lateral n-p-n BJT in the NMOS device is turned on, the ESD current is discharged through the BJT path in the NMOS structure. Such an ESD current discharging path is far away from the NMOS drain LDD peak and the NMOS surface channel. Therefore, the NMOS can sustain a higher ESD level by the substrate-triggered design, as compared to the gate-driven or gate-grounded design.

In this chapter, four substrate-triggered devices for using in the power-rail ESD clamp circuits are proposed and investigated. The parasitic lateral and vertical bipolar transistors in the NMOS or PMOS structures are used to discharge the ESD current, which are turned on by the substrate-triggered design. Therefore, the proposed ESD-clamp devices can sustain a much higher ESD level within a smaller silicon area.

6.1 SUBSTRATE-TRIGGERED ESD CLAMP DEVICES

ESD robustness of CMOS devices is strongly dependent on the device structure, layout style, and layout spacing. If the ESD current is uniformly discharged through the parasitic lateral bipolar junction transistor (BJT) of the MOS structure, the ESD current flows away from both the shallow surface channel and the LDD peak of MOS device. Therefore, the MOS device can sustain a much higher ESD stress. To induce the ESD current flowing through the parasitic lateral BJT away from the surface channel of MOS device, the substrate-triggered technique is proposed in this work to significantly improve ESD robustness of the ESD clamp devices.

To investigate the efficiency of the substrate-triggered technique, four substrate-triggered devices with different device structures are fabricated and investigated in a

0.6-μm CMOS process. In order to enhance the more uniform turn-on phenomena and the BJT action in the ESD clamp device, the cell-based square-type layout method [121] is used to realize these four substrate-triggering devices.

6.1.1 Substrate-Triggered Lateral BJT (STLB) Device

The schematic cross-sectional view of the STLB device with its corresponding control circuit is shown in Fig. 6.2(a), where the base of the lateral n-p-n BJT is controlled by the RC-based ESD detection circuit. During the ESD transition, the voltage on the capacitor C is initially kept at a low level due to the RC time delay in the ESD-detection circuit. The RC value is often designed around 0.1~1μs to distinguish the ESD transition or the normal VDD power-on transition. To efficiently turn off the surface channel of NMOS, the gate of NMOS is directly connected to ground (VSS). The inverter in Fig. 6.2(a) is self-biased by the ESD energy and provides a trigger current into the p-substrate from the node n2. The trigger current, flowing in the local p-substrate region, forward biases the base-emitter junction of the parasitic lateral n-p-n BJT of the gate-grounded NMOS device. The parasitic lateral n-p-n BJT is therefore triggered on, and the ESD current is discharged through the lateral n-p-n BJT, which is far from the surface channel and the LDD peak of the gate-grounded NMOS. To improve the turn-on speed of the lateral BJT, an N-well structure is especially inserted under the NMOS source region to collect the triggering current in the local substrate. This N-well structure also increases the equivalent base resistance of the lateral n-p-n BJT to improve its turn-on speed. Therefore, the bipolar action in the NMOS device can be earlier initiated to bypass the ESD current in the ESD-stress condition.

The practical layout of a unit cell of the STLB device is drawn in Fig. 6.2(b), and its symbol is shown in Fig. 6.2(c). To connect the gate of the NMOS to ground, the width of the gate is locally extended to the four corners in the unit cell. The device cross-sectional view along the line A--A' of Fig. 6.2(b) is corresponding to that drawn in Fig. 6.2(a). The P+ diffusion connected to the trigger node V_B is drawn at the center of the cell, and the P+ diffusion connected to VSS surrounds the whole unit cell at the outside. By using such a layout arrangement and the additional N-well inserted under the NMOS source region, the bipolar action of the NMOS can be earlier triggered on for effective ESD protection purpose. A unit cell of the STLB device realized in a 0.6-μm CMOS process occupies a silicon area of 47.7×47.4 μm^2. A STLB device with a larger device dimension can be assembled by a

plurality of such cells.

6.1.2 Substrate-Triggered Vertical BJT (STVB) Device

The vertical p-n-p BJT is also designed to discharge the ESD current across the power rails. The ESD clamp circuit with the schematic cross-sectional view of the STVB device is shown in Fig. 6.3(a). The vertical BJT is formed by the p^+ diffusion (connected to VDD) in the N-well, the N-well (connected to V_B), and the p-substrate (connected to VSS). To trigger on the vertical p-n-p BJT, the base node (N-well) of the vertical p-n-p BJT has to be kept at a low-voltage level during the ESD transition. On the contrary, the base node (N-well) must be kept at the voltage level of VDD to turn off the BJT when the IC is in normal operation condition. To achieve such requirement, two-stage inverters are inserted in the ESD detection circuit between the *RC* and the vertical BJT, as that shown in Fig. 6.3(a). The two inverters are self-biased by the ESD energy to keep the node V_B at a low voltage level in the ESD-stress condition, but the node V_B is biased at VDD when the IC is in the normal operation condition.

The practical layout of a unit cell of the STVB device is shown in Fig. 6.3(b), and its symbol is shown in Fig. 6.3(c). The device cross-sectional view along the line B--B' of Fig. 6.3(b) is corresponding to that drawn in Fig. 6.3(a). A unit cell of the STVB device realized in a 0.6-μm CMOS process occupies a silicon area of 40.5×40.5 μm^2. A STVB device with a larger device dimension can be assembled by a plurality of such cells.

6.1.3 Substrate-Triggered Double BJT (STDB) Device

To make a complementary design to the STLB (with NMOS), the parasitic p-n-p BJT in the PMOS device is also designed to discharge the ESD current across the power rails. The ESD clamp circuit and the schematic cross-sectional view are shown in Fig. 6.4(a). In Fig. 6.4(a), the source and gate of the ESD-clamp PMOS are connected together to VDD. The drain of the ESD-clamp PMOS is connected to VSS. When this ESD clamp circuit is stressed by a positive ESD, the surface channel of the ESD-clamp PMOS is kept off. A lateral p-n-p BJT is formed by the drain and source of the PMOS. There is also a parasitic vertical p-n-p BJT within this device structure to constitute the *double BJT* structure in the meanwhile. The vertical p-n-p BJT is formed by the source of the PMOS, the N-well, and the grounded

p-substrate, as that shown in Fig. 6.4(a).

The substrate-triggered technique is used to trigger on the *double BJT* structure. To trigger on the *double BJT*, the base (N-well) of the *double BJT* has to be kept at a low-voltage level during the ESD transition. But, the base (N-well) has to be kept at the voltage level of VDD when this circuit is under normal operation condition. In the normal operation condition, the node n1 on the capacitance *C* is charged up to VDD. Therefore, the node n3, connected to the n+ diffusion in the N-well, is biased at the voltage level of VDD to keep the parasitic p-n-p BJT's off in the STDB device. During the ESD transition, the node n1 in Fig. 6.4(a) is initially kept at a low-voltage level before the capacitance *C* is charged up to a high-voltage level. The node n2 in Fig. 6.4(a) is therefore charged to a high-voltage level by the ESD energy. Thus, the node n3 (also the node V_B) is kept at a low-voltage level. The emitter-base junction of the parasitic p-n-p BJT's in the STDB device is forward biased to turn on the STDB device during the ESD transition.

The practical layout of a unit cell of the STDB device is shown in Fig. 6.4(b), and its symbol is shown in Fig. 6.4(c). To connect the gate of the PMOS, the width of the gate is locally extended to inner at the four corners in the unit cell. The device cross-sectional view along the line C--C' of Fig. 6.4(b) is corresponding to that drawn in Fig. 6.4(a). A unit cell of the STDB device realized in a 0.6-μm CMOS process occupies a silicon area of 67.1×67.1 μm^2. A STDB device with a larger device dimension can be assembled by a plurality of such cells.

6.1.4 Double-Triggered Double BJT (DTDB) Device

To provide more current discharging path in per silicon area of the ESD clamp device, a double-triggered design is shown in Fig. 6.5(a) with the DTDB device. The *double BJT* structure is the same as that in the STDB device. The double-triggered design is achieved by applying the trigger voltage to the gate of ESD-clamp PMOS and the trigger current to the base of *double BJT* structure. Both the PMOS device and the *double BJT* structure can be quickly turned on to provide more ESD current discharging path in the device structure. The trigger circuit to turn on the DTDB is similar to that with the STDB device. During ESD transition, the ESD detection circuit provides a trigger current (voltage) into the N-well (gate) to turn on the DTDB device. While the IC is in the normal operation condition, the node V_B is biased at VDD voltage level. Therefore, the DTDB device is kept off.

The practical layout of a unit cell of the DTDB device is shown in Fig. 6.5(b), and its symbol is shown in Fig. 6.5(c). To connect the gate of the PMOS, the width of the gate is locally extended at the top and bottom sides in the unit cell. The device cross-sectional view along the line D--D' of Fig. 6.5(b) is corresponding to that drawn in Fig. 6.5(a). A unit cell of the DTDB device realized in a 0.6-μm CMOS process occupies a silicon area of 67.1×67.1 μm^2. A DTDB device with a larger device dimension can be assembled by a plurality of such cells.

6.2 CIRCUIT SIMULATION

To verify the actual operations of the *RC*-based ESD-detection circuits, the power-rail ESD clamp circuits with the STLB and DTDB devices are simulated by *HSPICE* in both the ESD stress condition and the normal VDD power-on condition.

6.2.1 ESD Stress Condition

A voltage pulse with a pulse width of 100ns and a rise time of 2ns is used to simulate the rising edge of an HBM ESD voltage. The *RC*-based ESD-detection circuits are designed to detect such a fast rising voltage on VDD and therefore to turn on the ESD clamp device. The pulse height of the applied voltage pulse used in this simulation is selected to 8V, which is smaller than the breakdown voltage of the proposed ESD clamp devices. The *RC*-based ESD-detection circuits are designed to turn on the ESD clamp devices during the ESD stress condition, before the ESD clamp devices are broken down by the overstress ESD voltage. Therefore, the power-rail ESD clamp circuits can be really triggered on earlier to bypass the ESD current, before the internal circuits are damaged by the ESD energy.

The simulated results are shown in Fig. 6.6(a) and 6.6(b), where an 8-V voltage pulse is applied to the VDD power rail and the VSS power rail is relatively grounded. Due to the time delay from the *RC* circuit of R=50kΩ and C=20pF, the voltage on the node n1 in Fig. 6.2(a) and Fig. 6.5(a) increases much slower than that on VDD power line, as the V(n1) curves shown in Fig. 6.6(a) and Fig. 6.6(b), respectively. Because the node n1 is kept at a low voltage level by the *RC* delay circuit, the PMOS (Mp1) of the inverter in the ESD-detection circuit is turned on simultaneously when the ESD pulse is applied on the VDD power rail. Therefore,

some ESD voltage is conducted from VDD to the node n2, which is used to bias the base of the lateral n-p-n BJT in the STLB device in Fig. 6.2(a). The forward biased base-emitter junction of the STLB device limits the voltage level around ~1V at the node n2, as the V(n2) curve shown in Fig. 6.6(a). With a base bias of ~1V, the lateral n-p-n BJT in the STLB device can be strongly turned on to generate the desired discharging Path_2 in Fig. 6-2 to bypass the ESD current from VDD to VSS. Thus, the internal circuits can be effectively protected by such a power-rail ESD clamp circuit.

In Fig. 6.6(b), the V(n2) waveform is almost the same as that of VDD, because the turned-on Mp1 of the first inverter charges up the node n2 (the input node of the second inverter) to the voltage level of VDD in the ESD-detection circuit of Fig. 6.5(a). Therefore, the NMOS Mn2 of the second inverter is turned on to bias the node n3 at a voltage level of VSS, as the V(n3) curve shown in Fig. 6.6(b). Because the node n3 is kept at voltage level of VSS by the ESD-detection circuit, the n-well (base of the p-n-p BJT) in the DTDB device is biased at a low voltage level in the ESD stress condition. The emitter of the p-n-p BJT in the DTDB device is directly connected to VDD in Fig. 6.5(b), which is biased at a high voltage level by the ESD energy. Therefore, the emitter-base junction of the p-n-p BJT is strongly forward biased to turn on the DTDB device for discharging the ESD current from VDD to VSS. From the simulated curves in Fig. 6.6(a) and 6.6(b), the proposed substrate-triggered devices can be quickly turned on by the ESD-detection circuits in Fig. 6.2(a) and Fig. 6.5(a), rather than by the junction breakdown. Thus, the internal circuits can be safely protected by such power-rail ESD clamp circuits.

6.2.2 VDD Power-on Condition

A voltage ramp with a pulse height of 5V and a rise time of 0.1ms is used to simulate the rising edge of the normal VDD power-on voltage waveform. The rise time of VDD power-on transition is generally in the range of several milli-second (ms). The rise time of 0.1ms used in this simulation is to verify that the substrate-triggered devices are not turned on in the power-on condition, even if the VDD has a fast power-on transition. The simulated results on the power-rail ESD clamp circuits with the STLB and DTDB devices are shown in Fig. 6.7(a) and 6.7(b), respectively.

Because the time constant of 1μs in the *RC*-based ESD-detection circuit, the voltage at node n1 can follow up the voltage increase with a rise time of ms on VDD power rail. The

simulated voltage waveform V(n1) in Fig. 6.7(a) is therefore the same as that of the applied VDD power-on voltage waveform. The PMOS Mp1 in Fig. 6.2(a) is always off, because its Vgs is kept at 0V during the VDD power-on transition. With an increasing voltage level at node n1, the NMOS Mn1 is turned on to keep the V(n2) curve always at 0V during the VDD power-on transition. Therefore, the base of the n-p-n BJT, which is biased by the node n2, in the STLB device is biased at 0V. So, the STLB device is always kept off during and after the VDD power-on transition.

In Fig. 6.7(b), the simulated V(n1) has the voltage waveform the same as that of VDD. The V(n2) has a little voltage glitch (below 0.5V) when the VDD starts to increase. But, the V(n3) still has the voltage waveform almost the same as that of VDD. The base voltage of the p-n-p BJT in the DTDB device in Fig. 6.5(a) is biased by the node n3. Because the emitter-base junction bias of the p-n-p BJT in the DTDB device is kept at 0V, the DTDB device is kept off during and after the VDD power-on transition. From this simulation, such power-rail ESD clamp circuits are guaranteed to be kept off, when the IC is in the normal operating condition. This has verified the actual operation of the *RC*-based ESD-detection circuits, which are used to control the substrate-triggered devices on and off.

6.3 EXPERIMENTAL RESULTS

6.3.1 Device Characteristics

The ESD clamp circuits with the proposed four substrate-triggered devices under different device sizes had been fabricated in a 0.6-μm non-silicided CMOS process. To find the I-V characteristics of these devices, every unit cell of the substrate-triggered devices is fabricated independently. The *Tektronix-370A* curve tracer is used to measure the I-V curves of the four substrate-triggered devices. The measured I-V curves of the STLB, STVB, STDB, and DTDB devices under different base current biases are shown in Figs. 6.8(a), 6.8(b), 6.8(c), and 6.8(d), respectively. In Fig. 6.8(a), the STLB device has the lowest snapback holding voltage (~7.6V) and breakdown voltage (~12V), as comparing to other 3 devices. In Fig. 6.8(b), the STVB device has the largest breakdown voltage (~37V) among the four devices. The breakdown voltage of the STDB device is 14.4V in Fig. 6.8(c), and that of the DTDB device is 14V in Fig. 6.8(d). The I-V characteristics of the STDB device and DTDB device

are similar, as those shown in Fig. 6.8(c) and Fig. 6.8(d). But, the collector current of the DTDB device is more than that of the STDB device under the same base current bias. This is due to the contribution of the channel current of the PMOS in the DTDB device.

The beta gains among the four devices are also measured and compared in Fig. 6.9. In Fig. 6.9, the X-axis with a logarithm scale is the collector current of the devices, and the Y-axis with a linear scale is the beta gain of the devices. The beta gain of STLB device becomes higher than 1, when the collector current is more than 12.7mA. The beta gain of STVB device drops from 16 to become less than 1, when the collector current is increased more than 14.3mA. The beta gain of STDB device drops from 18.5 to become less than 1, when the collector current is increased more than 38.4mA. The beta gain of DTDB device drops from 49 to become less than 1, when the collector current is more than 42.4mA. The DTDB structure with a collector current of 1μA has a highest beta gain (~49) among these four devices. In the low I_C region, the DTDB structure provides a high gain because the PMOS is also turned on. But in the high I_C region, the beta gains of STVB, STDB, and DTDB devices are degraded to be below one. But, the beta gain of STLB becomes higher than one.

To investigate the leakage current of the proposed substrate-triggering devices when they are kept off, the *HP-4145* is used to measure the total leakage current of the fabricated ESD clamp circuits with the proposed substrate-triggered devices. Under the normal VDD bias of 5V, the leakage currents of the ESD clamp circuits with the STLB (with a silicon area of 25148 μm^2), the STDB (with a silicon area of 46757 μm^2), and the DTDB (with a silicon area of 46757 μm^2) devices are all about 12.3pA. The leakage current of the ESD clamp circuit with the STVB device (with a silicon area of 16642 μm^2) is only 0.7pA. With such a small leakage current in the order of several pA, the *RC*-based ESD detection circuit can indeed keep the substrate-triggered devices off when the IC is under normal VDD bias.

6.3.2 ESD Performance and TLPG I-V Curves

The *KeyTek ZapMaster* is used to evaluate the ESD robustness of the fabricated ESD clamp circuits with the proposed substrate-triggered devices under different device dimensions. The applied HBM (Human Body Model) ESD voltages in the ESD tester are controlled from 200V to 1000V with a step of 200V and from 1000V to 8000V with a step of 500V. Every fabricated ESD clamp circuits in the testchip is placed in the stand-alone condition, where every power-rail ESD clamp circuit has its own VDD power pad. The failure

criterion to judge ESD level of the power-rail ESD clamp circuit is defined as 1-μA current leakage under a 5-V VDD bias. The HBM ESD test results are summarized in Fig. 6.10(a) and Fig. 6.10(b). The relations between ESD robustness and channel width of the proposed ESD clamp devices are shown in Fig. 6.10(a). The dependence of ESD level on the device silicon area among the four ESD clamp devices is shown in Fig. 6.10(b). The HBM ESD test results of all STVB devices with different device dimensions can pass the stress of 1000V, but they all fail when the HBM ESD voltage is over 1000V. The breakdown of the vertical p-n-p bipolar transistor in the STVB device causes the ESD current mainly flowing from the contact of p+ diffusion (emitter) into the p-substrate (collector). In this vertical p-n-p bipolar transistor, the base width, between the junction depths of the n-well and the p+ diffusion, is kept the same by the CMOS process. Therefore, even if the STVB has a wide layout area, its base width is still kept the same. Because the ESD current on this STVB device is mainly discharged through its base region to the grounded p-substrate, the STVB devices with different layout areas have the same low ESD level (~1000V) when the narrow base region is damaged by ESD energy. From Fig. 6.10(b), the ESD clamp circuits with the STLB, the STDB, or the DTDB structures can sustain higher ESD level in per silicon area. The average ESD robustness in per silicon area of both the STDB and DTDB device is about 0.30 V/μm^2, and that of the STLB is about 0.26 V/μm^2. The ESD clamp circuit with the STVB device only sustains a low ESD level of 1000V even if it was drawn with a larger device dimension and a large silicon area.

To investigate the snapback characteristics of devices during ESD transition, the TLPG system is used to measure the secondary breakdown currents (It_2) of the four substrate-triggered devices. The TLPG-measured results are shown in Fig. 6.11. From the experimental results, the STVB device with a silicon area of 4548 μm^2 has a much smaller It_2 of only 0.26A. The STVB device in the 0.6-μm CMOS process has the lowest ESD robustness and the largest breakdown voltage, as compared to the other three devices. This means that the STVB device has a lower ESD robustness, even if the STVB device is triggered by the substrate-triggering design.

From Fig. 6.11, the STDB and DTDB devices with a silicon area of 12352 μm^2 have the It_2 of 2.31A and 2.41A, respectively. The STLB device with a silicon area of 6546 μm^2 has the It_2 of 1.16A. Then, the It_2 in per silicon area of the STLB, STDB, and DTDB devices in the 0.6-μm CMOS technology can be calculated as 177 μA/μm^2, 187 μA/μm^2, and 195 μA/μm^2, respectively. The relation between the HBM ESD level and the secondary

breakdown current It_2 (which is measured by TLPG with a pulse width of 100ns) can be written in equation (2.3) [45]. The average HBM ESD level of the ESD clamp circuits with the STLB, STDB, and DTDB devices are nearly equal to the product of It_2 with the HBM resistance of 1500Ω in this experimental result.

The traditional power-rail ESD clamp circuit in Fig. 6.1 with an NMOS by gate-driven design is also fabricated in the same process. With a device dimension (W/L) of 500/1.0 (μm/μm) for the gate-driven NMOS, which occupies a layout area of 6931 μm^2, this traditional design of Fig. 6.1 can sustain an HBM ESD level of only 1000V. The ESD robustness in per silicon area of the NMOS is only 0.14 $V/\mu m^2$, but that of the STLB is improved to 0.26 $V/\mu m^2$. This verifies that the substrate-triggered technique can effectively improve ESD level of the NMOS. With the substrate-triggered technique, the STDB and DTDB devices can provide about two-times greater ESD level in per silicon area than the gate-driven NMOS.

From the measured results on the ESD level and the secondary breakdown current, the STLB, STDB, and DTDB devices with the substrate-triggered design and the cell-based layout method can significantly increase their ESD robustness in a limited silicon area.

6.3.3 Turn-On Verification

To verify the turn-on efficiency of the power-rail ESD clamp circuits, a voltage pulse with a rise time around 5~10 ns and a pulse width of 400 ns is applied to the VDD of the ESD clamp circuits with the VSS grounded to simulate the ESD-stress condition. The experimental setup to verify the turn-on efficiency for the ESD clamp circuits with the STLB, STVB, STDB, or DTDB devices is shown in Fig. 6.12(a). The original waveform of the voltage pulse generated from a pulse generator to investigate the turn-on efficiency of these ESD clamp circuits is shown in Fig. 6.12(b). The voltage waveform on the VDD node is observed to find the turn-on behavior of the ESD clamp circuits. When the 8-V voltage pulse is applied, the voltage waveforms on the VDD of the ESD clamp circuits with the STLB, STVB, STDB, and DTDB devices are measured and shown in Figs. 6.12(c), 6.12(d), 6.12(e), and 6.12(f), respectively. The 0-to-8 V voltage pulse is clamped by the turned-on ESD-clamp device (STLB, STVB, STDB, or DTDB), therefore the voltage pulse is degraded to a certain voltage level. When the capacitor C (node n1) in the *RC*-based ESD-detection circuit is charged up, the ESD-detection circuit will turn off the ESD-clamp device. Then, the voltage waveform is

restored to the original voltage level. Therefore, the period of the degraded voltage waveform can be defined as the turn-on time of the ESD-clamp devices in the power-rail ESD clamp circuits, which is marked as t_{on} in Figs. 6.12(c) ~ 6.12(f).

The turn-on time in Fig. 6.12(f) for the power-rail ESD clamp circuit with the DTDB device is about 140 ns. The turn-on time of the power-rail ESD clamp circuit is varying if the applied voltage pulse has different pulse heights. The relations between the turn-on time and the pulse height of the applied voltage pulse among the ESD clamp circuits with the four substrate- triggered devices are measured and summarized in Fig. 6.13. From the experimental results, the turn-on times of these ESD clamp circuits are around 150~210 ns when the pulse height has a voltage of 10V. The turn-on time of the ESD clamp circuit is almost linearly increased while the pulse height of the applied voltage pulse increases. This is due to the longer delay time to charge up the capacitor C in the *RC*-based ESD-detection circuit to a voltage level that causes the inverter changing its output state, when the applied voltage pulse has a higher voltage level.

A 5-V ramp voltage with a rise time of 0.1 ms is also applied to the VDD (with the VSS grounded) to verify whether the ESD clamp circuits are kept off in the normal VDD power-on condition. When the 0V-to-5V ramp voltage waveform is applied to the VDD of the ESD clamp circuits with the STLB, STVB, STDB, or DTDB devices, no degradation is found on the applied voltage waveform during this VDD power-on condition. Therefore, the ESD clamp circuits with the proposed four substrate-triggered devices are really kept off in the normal VDD power-on condition.

6.3.4 Power-Rail Noise Clamping

When the IC is in the normal operation condition with 5-V VDD and 0-V VSS power supplies, there are some system-level or board-level noise pulses coupled to the power lines to generate the overshooting noise pulse across the power lines. Such an overshooting noise pulse may initiate the occurrence of latchup in the CMOS IC's to burn out the IC's [114]-[115]. The ESD clamp circuits with the proposed substrate-triggered devices can be also triggered on to clamp such an overshooting noise pulse on the VDD power line. Therefore, the IC protected by such power-rail ESD clamp circuits has a high immunity to the transient-induced latchup. To verify this noise-clamping efficiency of the power-rail ESD clamp circuits with the proposed substrate-triggered devices, a 5-to-12 V overshooting

voltage pulse is added to the 5-V VDD power line of the power-rail ESD clamp circuits. The experimental setup to investigate the noise-clamping efficiency of the power-rail ESD clamp circuits is shown in Fig. 6.14(a). The original overshooting noise pulse with a rise time of ~10 ns and a pulse width of 200 ns generated from a pulse generator is shown in Fig. 6.14(b). The overshooting voltage waveforms clamped by the power-rail ESD clamp circuits with the STLB and DTDB devices are shown in Fig. 6.14(c) and Fig. 6.14(d), respectively.

In Fig. 6.14(c), the 5-to-12 V overshooting voltage pulse is clamped by the STLB to the voltage level of 9.2V, which is near to its snapback holding voltage. But after the triggering of the 5-to-12 V overshooting voltage pulse, the VDD voltage level is restored to the original 5V. In Fig. 6.14(d), the 5-to-12 V overshooting voltage pulse is initially clamped by the DTDB device to the voltage level around 10V, which is dependent on the device dimension of the DTDB device. A larger device dimension causes a lower clamped voltage level on the overshooting noise pulse. A larger *RC* time constant in the control circuit causes a longer turn-on time on the DTDB device to clamp the overshooting noise pulse. After the triggering of the 5-to-12 V overshooting voltage pulse, the VDD voltage levels are restored to the original 5V. The 5-to-12 V overshooting voltage pulse clamped by the STVB or STDB devices is almost the same as that clamped by the DTDB device. This verifies that the power-rail ESD clamp circuits with the substrate-triggered devices have the benefit to clamp the overshooting noise pulse on the VDD power line. After the noise transition, the power-rail ESD clamp circuits can turn off automatically to avoid current leaking from VDD to VSS through the power-rail ESD clamp circuits.

6.4 SUMMARY

Area-efficient power-rail ESD clamp circuits with four different substrate-triggered devices have been practically investigated in a 0.6-μm CMOS process. By using the substrate-triggered technique, the DTDB, STDB, and STLB devices can provide much higher ESD robustness within a smaller layout area, as compared to the traditional design with the gate-driven NMOS device. The STDB and DTDB devices with the parasitic vertical BJT have higher ESD robustness. But, a pure vertical p-n-p BJT in the 0.6-μm CMOS process even with a large device size still sustains a low HBM ESD level, due to the higher breakdown voltage and the lower secondary breakdown current of the STVB device. To improve ESD

robustness of an on-chip ESD protection circuit in a limited silicon area, the DTDB device has the best performance among these four substrate-triggered devices. With suitable design on both the bipolar structure in the ESD-clamp device and the substrate-triggered technique, the layout area of the ESD clamp circuit to achieve whole-chip ESD protection can be efficiently reduced to save the silicon cost of CMOS IC's.

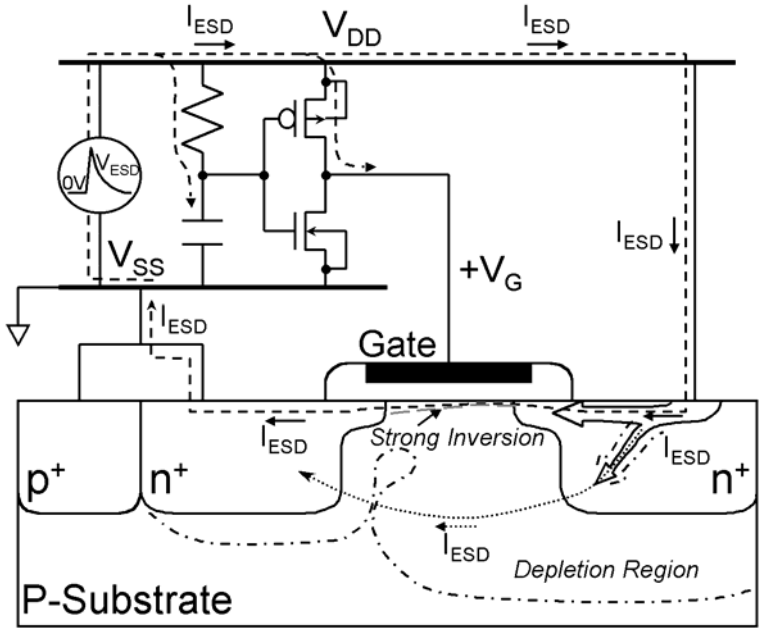
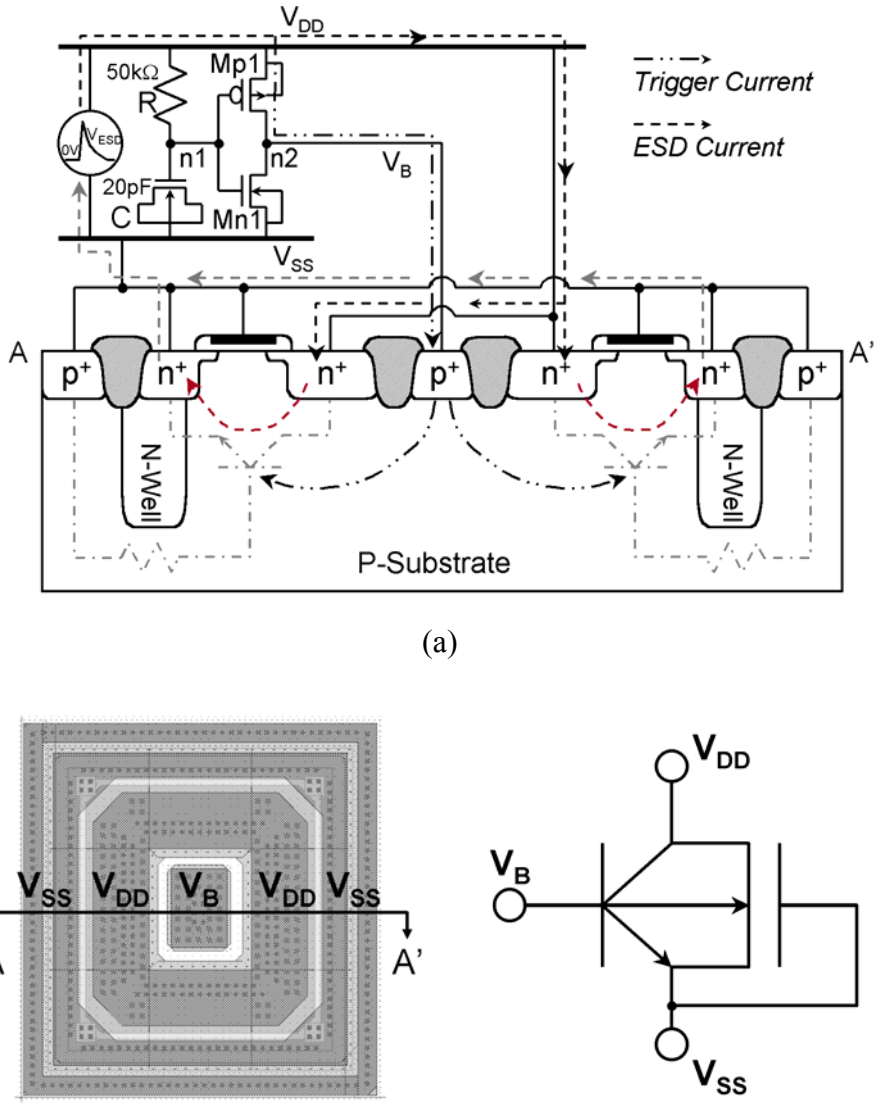


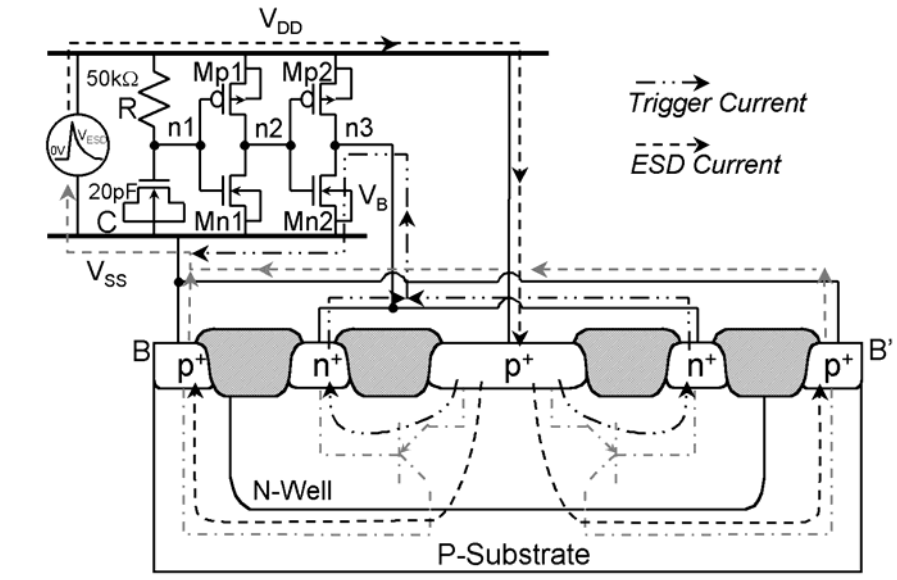
Fig. 6.1 The schematic diagram of the *RC*-based ESD clamp circuit with a gate-driven NMOS as the ESD clamp device between the VDD and VSS power rails.



(a)

(b) (c)

Fig. 6.2 (a) The schematic diagram of the ESD clamp circuit with the substrate-triggered lateral BJT (STLB) device. (b) The layout of a unit cell of the STLB device. (c) The symbol of STLB device.



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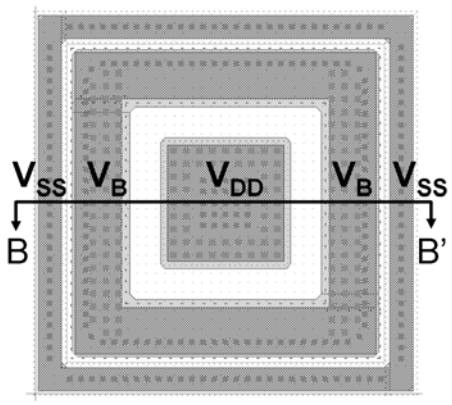

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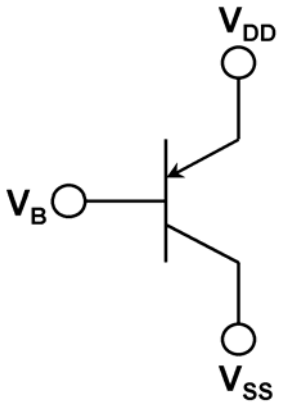
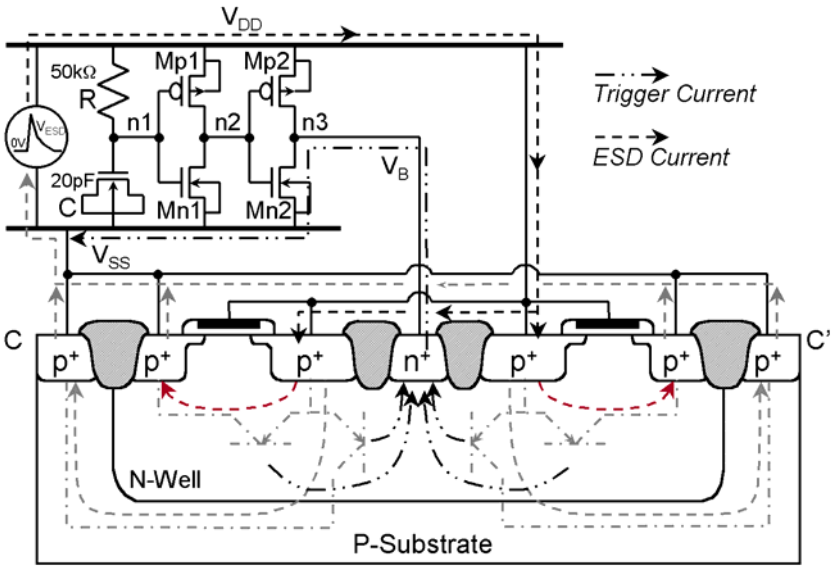
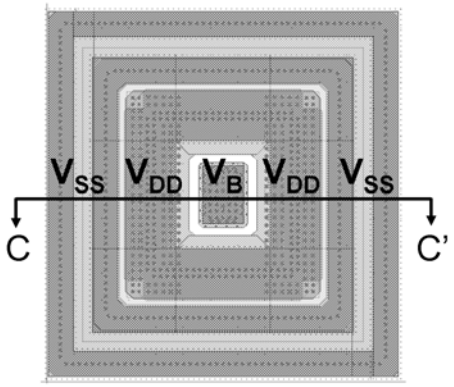


(c)

Fig. 6.3 (a) The schematic diagram of the ESD clamp circuit with the substrate-triggered vertical BJT (STVB) device. (b) The layout of a unit cell of the STVB device. (c) The symbol of STVB device.



(a)



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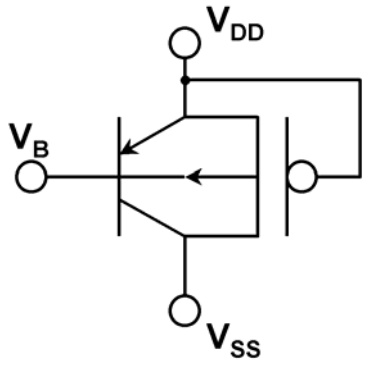
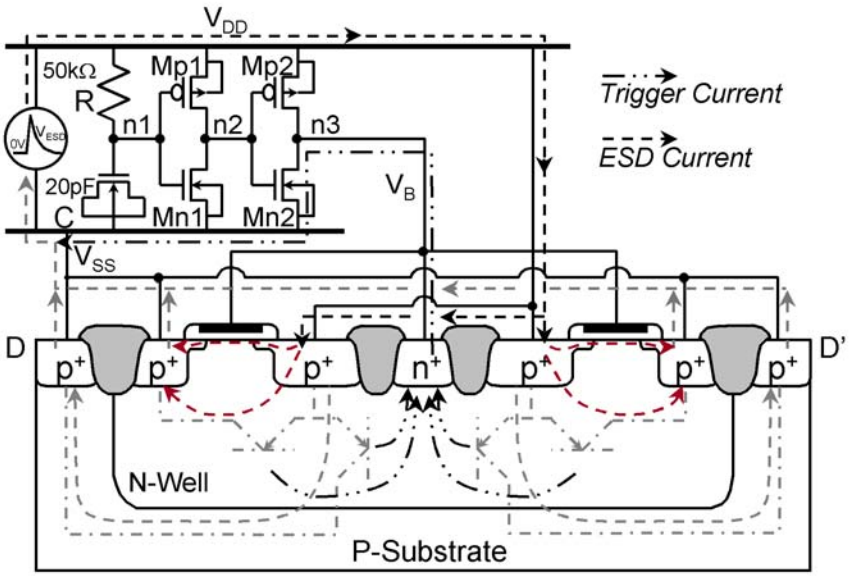
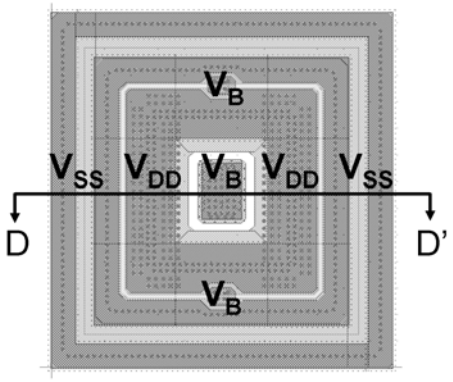


(c)

Fig. 6.4 (a) The schematic diagram of the ESD clamp circuit with the substrate-triggered double BJT (STDB) device. (b) The layout of a unit cell of the STDB device. (c) The symbol of STDB device.



(a)



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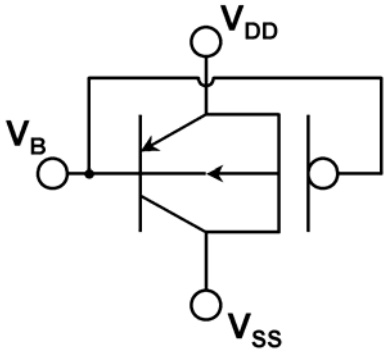
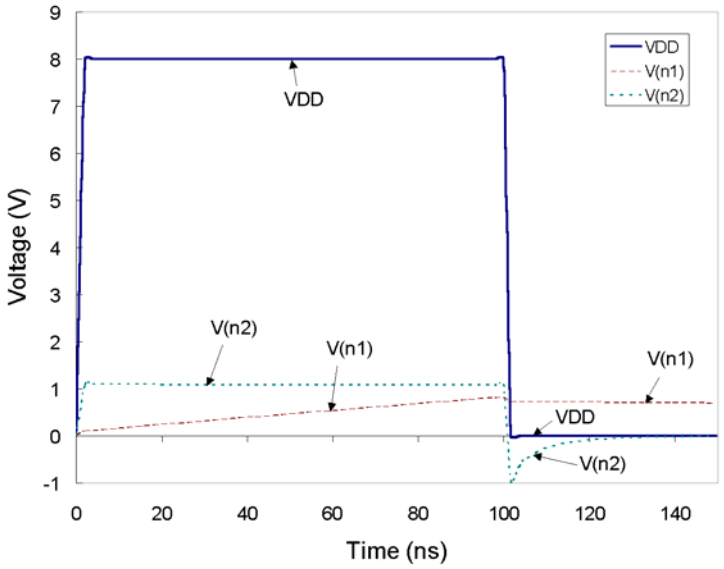


(c)

Fig. 6.5 (a) The schematic diagram of the ESD clamp circuit with the double-triggered double BJT (DTDB) device. (b) The layout of a unit cell of the DTDB device. (c) The symbol of DTDB device.



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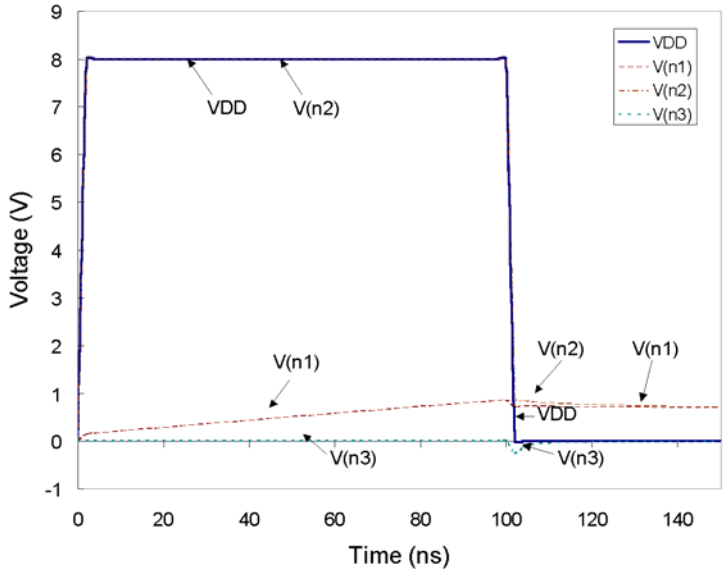
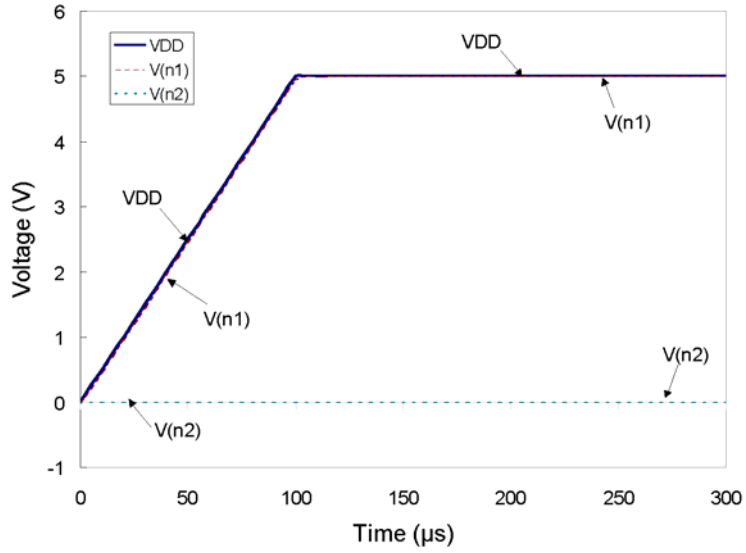


(b)

Fig. 6.6 The *HSPICE* simulated voltage waveforms for (a) the ESD clamp circuit with the STLB device, and (b) the ESD clamp circuit with the DTDB device, under the triggering of an 8-V voltage pulse with 100-ns pulse width and 2-ns rise time to simulate the ESD stress condition.



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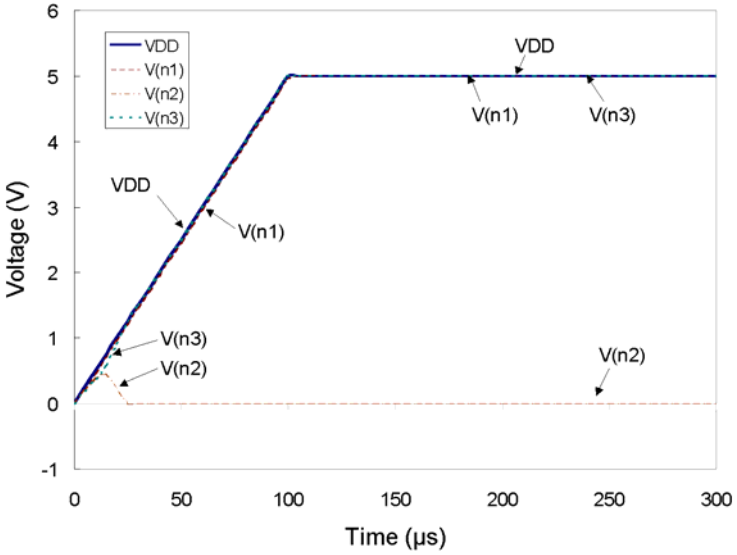


(b)

Fig. 6.7 The *HSPICE* simulated voltage waveforms for (a) the ESD clamp circuit with the STLB device, and (b) the ESD clamp circuit with the DTDB device, under the triggering of a 5-V ramp voltage with 0.1-ms rise time to simulate the VDD power-on condition.

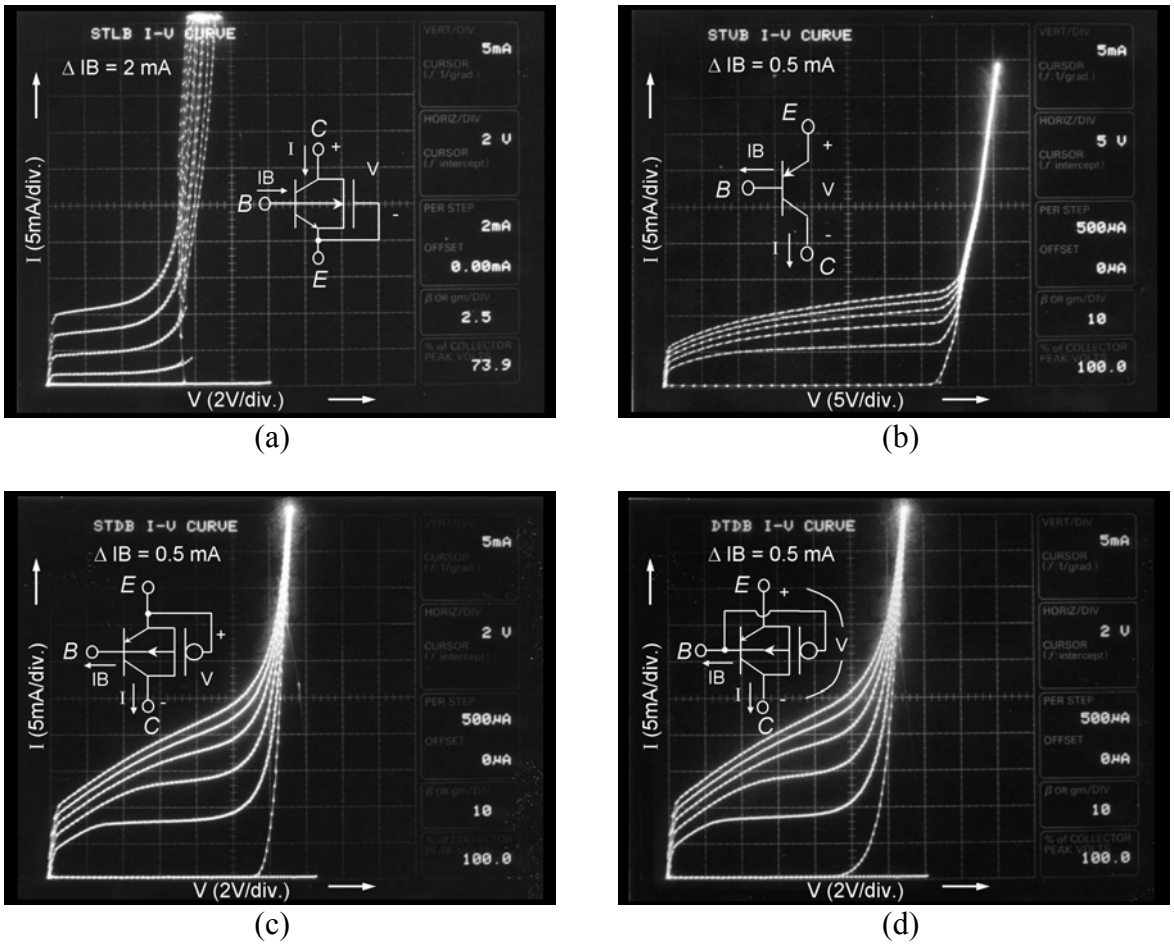


Fig. 6.8 The measured I-V curves of (a) the STLB, (b) the STVB, (c) the STDB, and (d) the DTDB devices. (X scale in (a), (c) and (d) is 2V/div.; X scale in (b) is 5V/div.; Y scale is 5mA/div.)

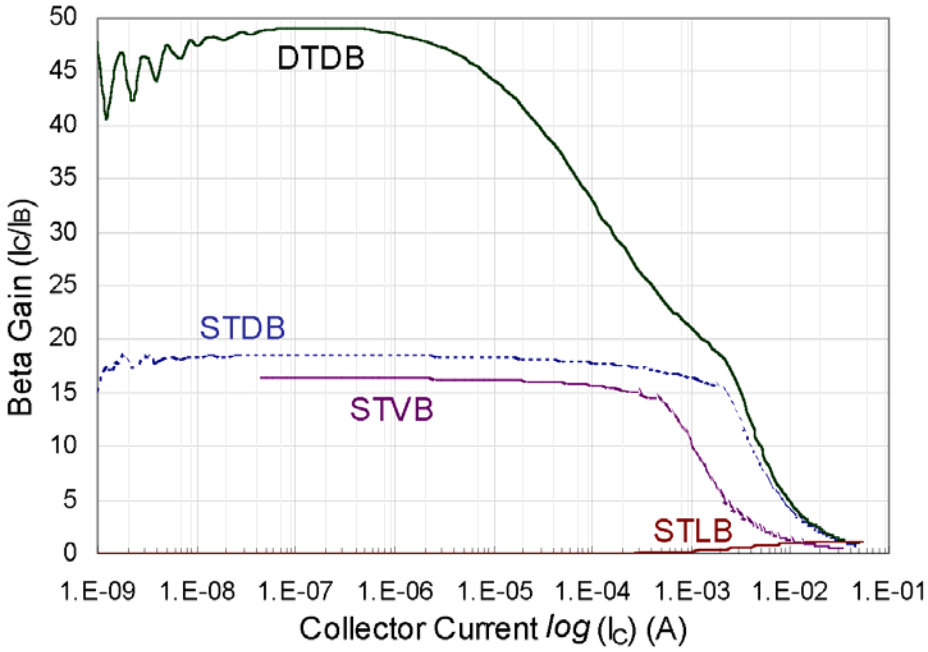
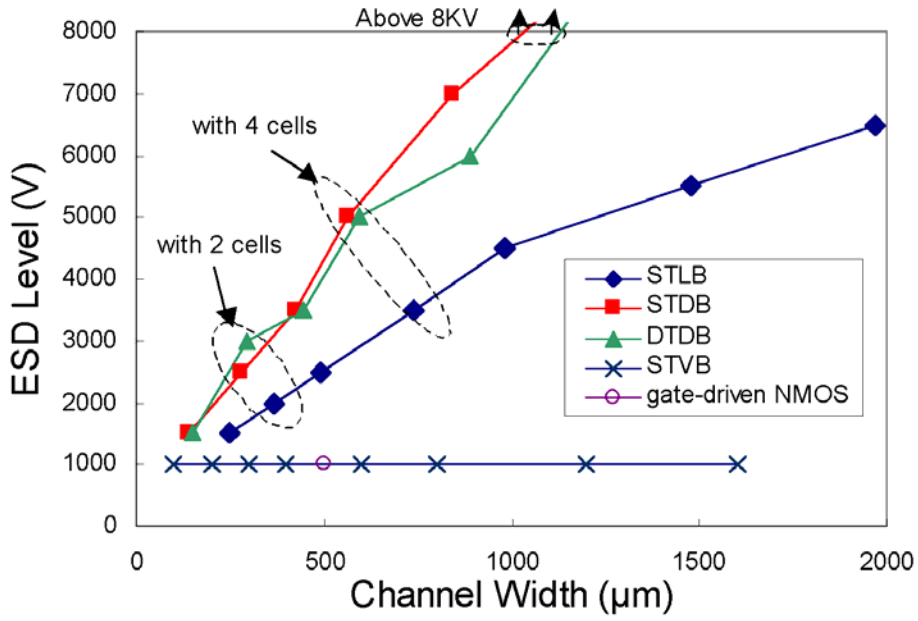
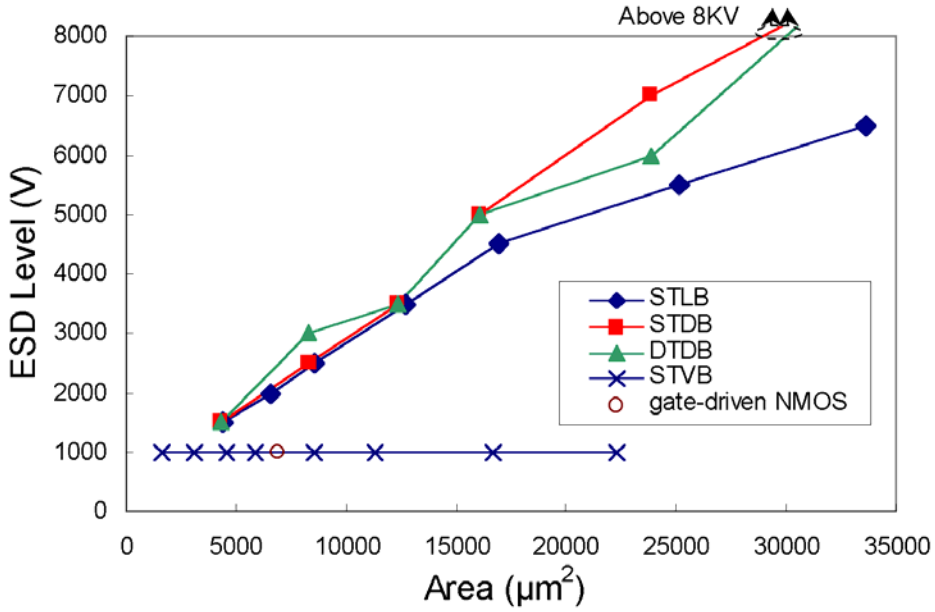


Fig. 6.9 The dependence of the beta gains on the collector currents among the STLB, STVB, STDB, and DTDB devices.



(a)



(b)

Fig. 6.10 The dependence of the HBM ESD level on (a) the channel width, and (b) the silicon area, of the power-rail ESD clamp circuits with different protection devices.

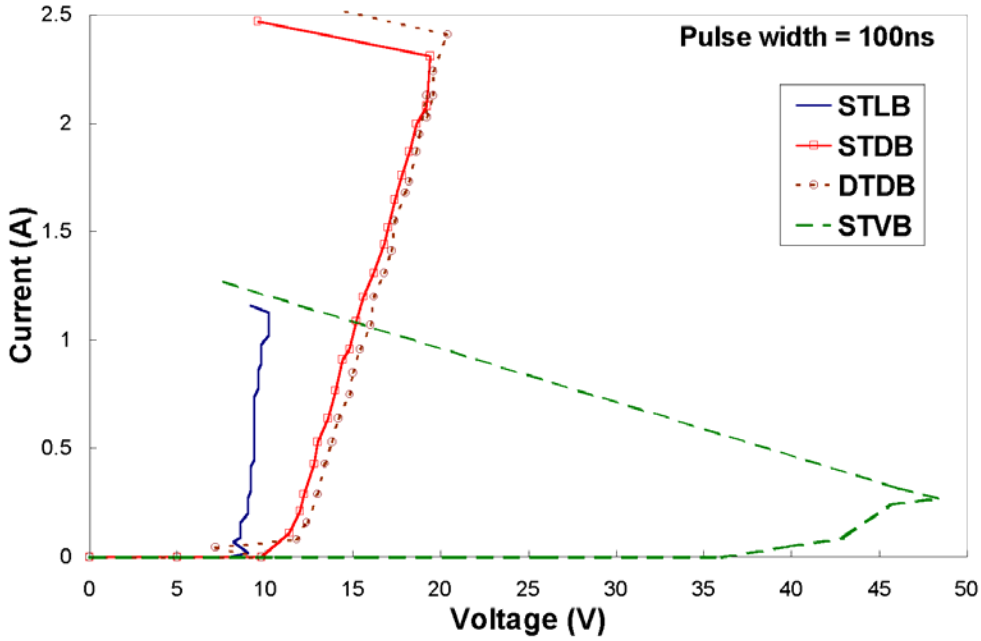


Fig. 6.11 The TLPG measured I-V curves of the substrate-triggered devices under 0-V substrate bias.

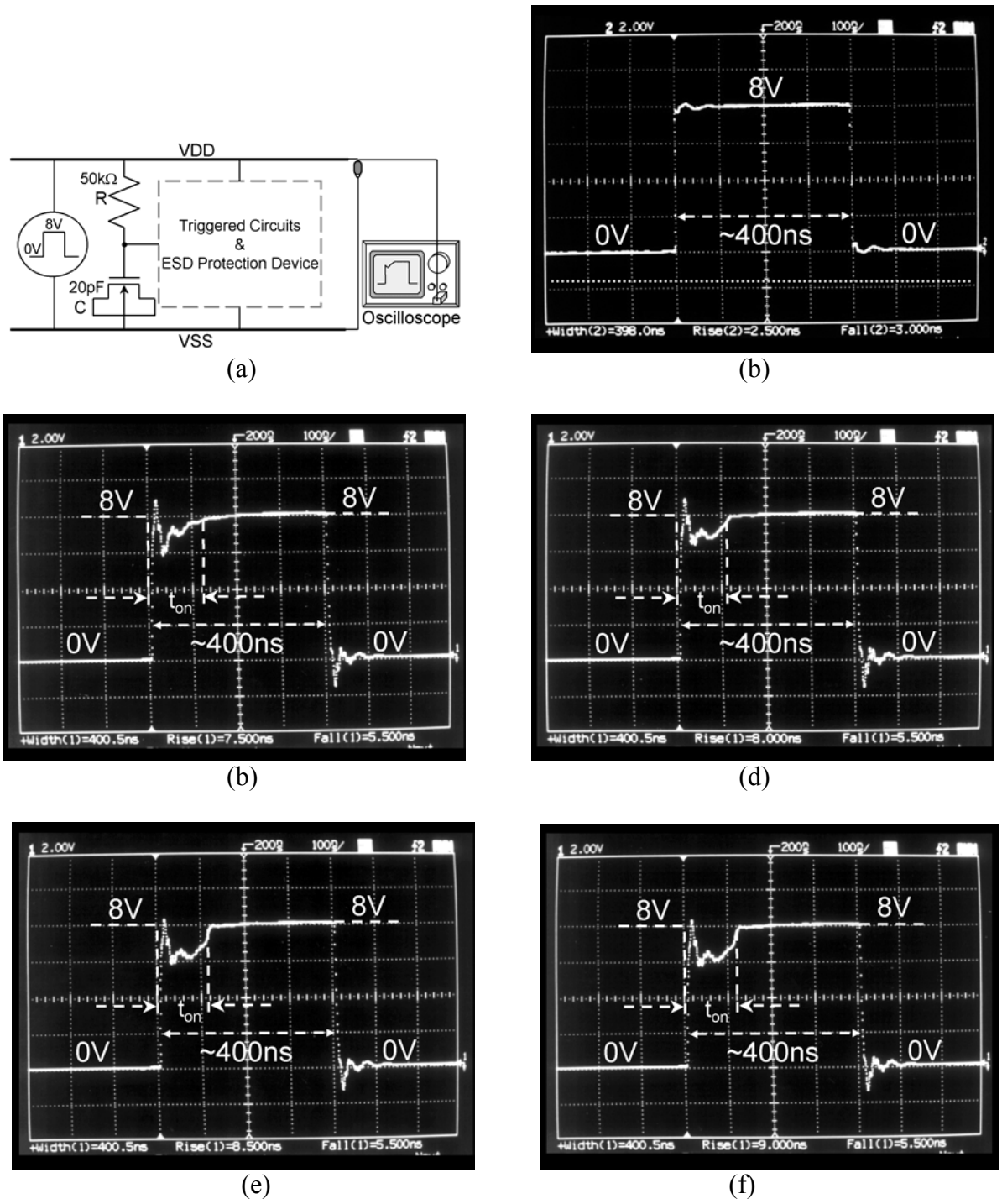


Fig. 6.12 (a) The experimental setup to verify the turn-on behavior of the power-rail ESD clamp circuits under ESD-stress condition. (b) The original 8-V voltage pulse generated from a pulse generator. The degraded voltage waveforms clamped by the power-rail ESD clamp circuits with the (c) STLB, (d) STVB, (e) STDB, and (f) DTDB devices. (X scale: 100ns/div.; Y scale: 2V/div.)

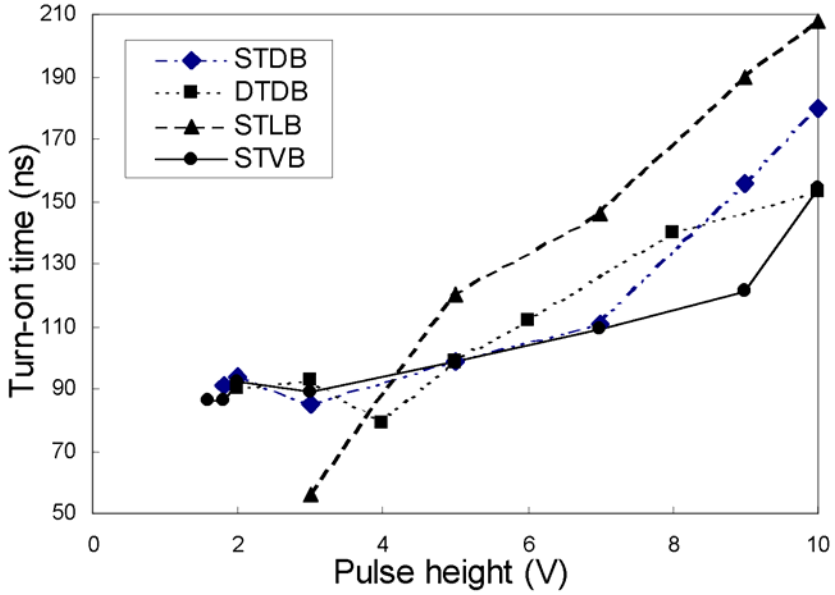


Fig. 6.13 The relations between the turn-on time and the pulse height of the applied voltage pulses on the power-rail ESD clamp circuits with different protection devices.

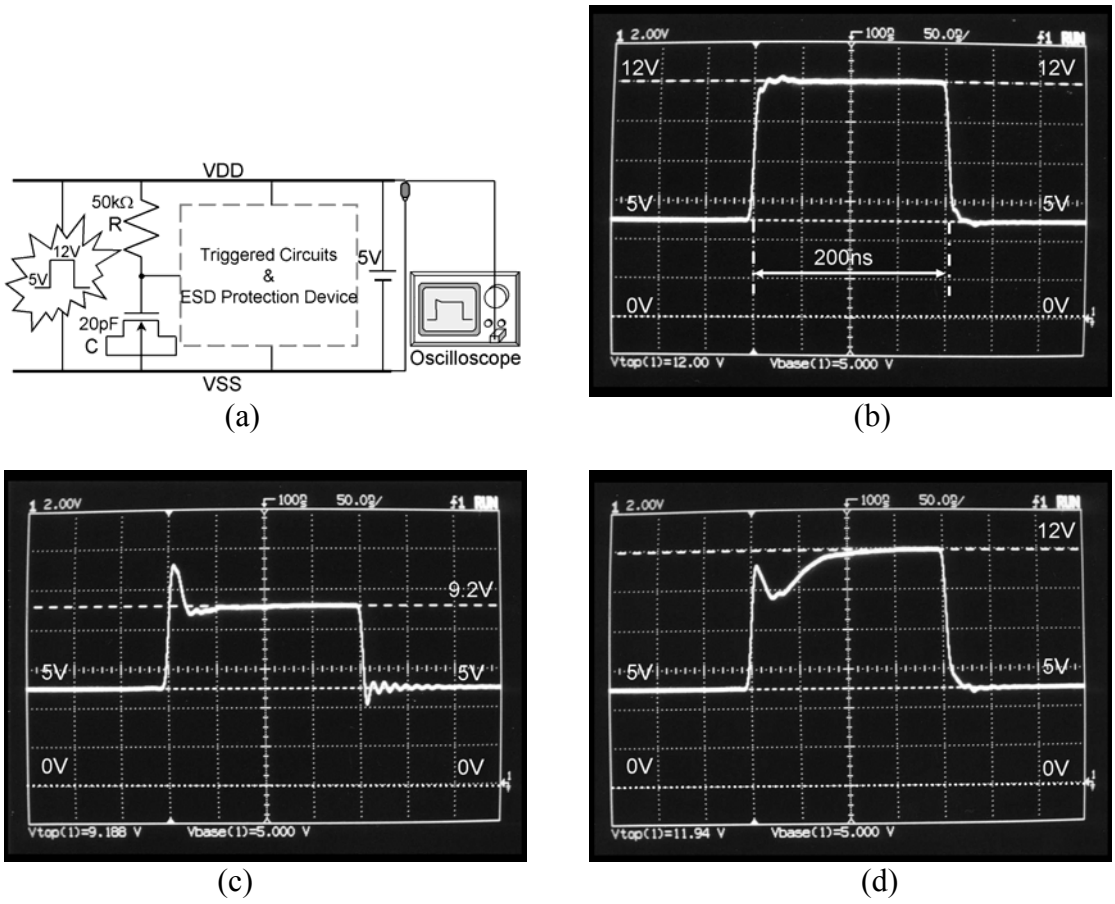


Fig. 6.14 (a) The experimental setup to verify the noise-clamping efficiency of the power-rail ESD clamp circuits when the IC is in the normal operating condition with 5-V VDD power supply and an overshooting noise pulse. (b) The original voltage waveform of a 5-to-12 V overshooting noise pulse. The degraded voltage waveforms of the 5-to-12 V overshooting noise pulse clamped by the power-rail ESD clamp circuits with the (c) STLB and (d) DTDB devices. (X scale: 50ns/div.; Y scale: 2V/div.)

CHAPTER 7

ANALOG ESD PROTECTION CIRCUIT WITH LOW INPUT CAPACITANCE FOR HIGH-FREQUENCY APPLICATIONS

The conventional input ESD protection circuit with two-stage protection scheme for digital input pins often has a series resistor connected between the primary ESD protection stage and the secondary ESD protection stage. But the large series resistance and the large junction capacitance in ESD clamp devices cause a long *RC* delay to the input signals, it is not suitable for analog pins, especially for the high-frequency applications [122]-[124]. For current-mode or RF input signals, the series resistance between the input pad and internal circuits is forbidden. Therefore, the traditional two-stage ESD protection design is no longer suitable for such analog input pins.

For some high-precision analog circuits, the input capacitance of an analog input pin including ESD protection circuit and a bond pad is required as constant as possible. A major distortion in analog circuits, especially in the single-ended input implementations, comes from the voltage-dependent nonlinear input capacitance of ESD clamp devices connected to the analog input pin. The typical degradation on analog circuit performance due to the nonlinear input capacitance of ESD clamp devices had been reported in [84], where the input capacitance was varying from 4pF to 2pF due to the input voltage increasing from 0V to 2V. Such nonlinear input capacitance caused an increase on the harmonic distortion in an analog-to-digital converter (ADC), and degraded precision of the ADC from 14-bit to become only 10-bit. Thus for high-precision analog applications, the input capacitance generated from ESD clamp devices on the input pad needs to be kept as constant as possible.

Recently, a turn-on efficient ESD protection circuit has been proposed to protect the high-frequency analog I/O pin, which is re-drawn in Fig. 7.1 [125]. This analog ESD protection circuit can sustain HBM (MM) ESD stress of up to 6kV (400V) in a 0.35-μm silicided CMOS process, but has a very small input capacitance of only ~0.4pF for high-frequency applications. The circuit operations and experimental results of this analog ESD protection circuit will be briefly summarized in Section 7.2. A design model to further

optimize the device dimensions and layout spacings of this analog ESD protection circuit is developed to keep the input capacitance almost constant for more high-precision applications [126]. From the calculation results, the voltage-dependent variation on input capacitance of this analog ESD protection circuit can be designed below 1% while the analog input signal has a voltage swing of 1V.

7.1 ANALOG ESD PROTECTION CIRCUIT

The analog ESD protection circuit is shown in Fig. 7.1, where Dp1 (Dn1) is the parasitic junction diode in drain region of Mp1 (Mn1) device. In order to reduce input capacitance on the analog pin, Mn1 and Mp1 are both designed with smaller device dimensions (W/L) of only 50μm/0.5μm [125]. The HBM ESD level of a stand-alone NMOS with a device dimension of 50μm/0.5μm is less than 500V in the 0.35-μm silicided CMOS process, while the NMOS is zapped in the PS-mode (positive to VSS) ESD stress. But, such a small NMOS can sustain an HBM ESD level of greater than 6000V in the same 0.35-μm silicided CMOS process, while the NMOS is zapped in the NS-mode (negative to VSS) ESD stress. In the PS-mode (NS-mode) ESD stress, the NMOS is operated in its drain junction reverse-breakdown (forward-bias) condition to discharge ESD current. Therefore, an NMOS has quite different ESD levels between the PS-mode and NS-mode ESD stresses. Of course, a stand-alone PMOS with a small device dimension also has a high ESD level in the PD-mode (positive to VDD) ESD stress, but has a much low ESD level in the ND-mode (negative to VDD) ESD stress.

To avoid the small-dimension Mn1 and Mp1 into the drain-breakdown condition under PS-mode or ND-mode ESD stresses to result in a much low ESD level, a turn-on efficient power-rail ESD clamp circuit is co-constructed into this analog ESD protection circuit to increase the overall ESD level. In Fig. 7.1, the *RC*-based ESD detection circuit is used to trigger on Mn3 device, when the pad is zapped under PS-mode or ND-mode ESD stresses. The ESD current paths along this analog ESD protection circuit are illustrated by the dashed lines in Fig. 7.2(a) and Fig. 7.2(b), respectively, when the analog pin is zapped in the PS-mode and pin-to-pin ESD stresses. In Fig. 7.2(b), the pin-to-pin ESD stress across the two input pins of a differential input stage can be transferred across the VDDA and VSSA power lines. Mn3 connected between VDDA and VSSA power lines is turned on by the *RC*-based

ESD detection circuit to conduct ESD current from VDDA to VSSA. Finally, ESD current flows out the chip from VSSA power line to the grounded pad through the forward-biased diode Dn4 in Mn4. With suitable design on the *RC*-based ESD detection circuit to quickly turn on Mn3, the pin-to-pin ESD stress can be effectively discharged away from the gate oxide of the differential input stage. Because Mn1 and Mp1 in this analog ESD protection circuit are not operated in the drain-breakdown condition, ESD current is discharged through the forward-biased drain diode Dp1 in Mp1 (Dn1 in Mn1) and the turned-on Mn3. So, Mn3 is especially designed with a larger device dimension (typically, W/L=1800μm/0.5μm) to sustain a high ESD level. Although the large-dimension Mn3 has a large junction capacitance, this capacitance does not contribute to the analog pad. Therefore, the analog pin can sustain a much higher ESD level but only with a very small input capacitance.

The spacing from drain contact to poly gate in both Mn1 and Mp1 is drawn as 3.4μm, whereas the spacing at source side is drawn as 1.55μm. With device dimension of 50μm/0.5μm in both Mn1 and Mp1, the input capacitance of this analog ESD protection circuit is varying from 0.37pF to 0.4pF when the input voltage increases from 0V to 3V. But, the input capacitance of a grounded gate NMOS (gg-NMOS) with a device dimension of 400μm/0.5μm varies from 1.83pF to 1.12pF, when the input voltage increases from 0V to 3V for an IC with 3V VDD power supply.

This analog ESD protection circuit had been practically fabricated in a 0.35-μm silicided CMOS process with an operational amplifier as its input circuit. Both the inverting and non-inverting input pins are protected by this analog ESD protection circuit. The silicide-blocking layer is also drawn on the devices Mn1, Mp1, and Mn3 to improve their ESD robustness, but without using the additional ESD-implantation process. The test results of the maximum sustaining ESD voltage under different pin combinations are summarized in Table 7.1, which includes the analog pin-to-pin ESD stress. The failure criterion is defined as the leakage current at the pad exceeds 1μA under 5V voltage bias after any ESD zapping. As shown in Table 7.1, this analog ESD protection circuit can successfully provide analog pins with HBM (MM) ESD level of 6000V (400V) in all ESD-stress conditions.

To verify turn-on efficiency of this analog ESD protection circuit during the pin-to-pin ESD stress, a voltage pulse generated from a pulse generator (hp 8118A) is applied to the inverting pin of an operational amplifier, whereas the non-inverting pin of this operational amplifier is relatively grounded and both the VDDA and VSSA pins are floating. The experimental setup to monitor turn-on efficiency under the positive pin-to-pin ESD stress is

shown in Fig. 7.3(a). The measured voltage waveform under the positive pin-to-pin ESD stress is shown in Fig. 7.3(b). The original voltage pulse generated from pulse generator has a pulse height of 8V and a pulse width of 200ns. The 8V voltage pulse has a rise time around ~10ns, which is similar to the rise time (5~15 ns) of an HBM ESD pulse. The drain breakdown voltage of NMOS Mn1 in the 0.35-μm silicide CMOS process without additional ESD implantation is 8.5V. Therefore, the voltage pulse with a pulse height of 8V does not cause drain breakdown on Mn1 in the analog ESD protection circuit. By applying such a voltage pulse to the analog pin, the turn-on efficiency of this analog ESD protection circuit can be clearly verified. While such a positive voltage pulse is applied to the analog pin as that shown in Fig. 7.3(a), it is clamped by the analog ESD protection circuit and the degraded voltage waveform is shown in Fig. 7.3(b). The pulse generator has a limited output current capability. The voltage pulse will be degraded if the analog ESD protection circuit is turned on, because the pulse generator cannot deliver enough current to sustain the voltage on the pad. The degraded voltage waveform proves that this analog ESD protection circuit can be actually turned on to clamp overstress voltage during the pin-to-pin ESD stress.

The turn-on efficiency of this analog ESD protection circuit during the ND-mode ESD stress is also verified with the experimental setup shown in Fig. 7.4(a). While the negative voltage pulse with a pulse height of -8V and a pulse width of 200ns is applied to the analog input pin under ND-mode ESD stress condition, it is clamped by the analog ESD protection circuit and the degraded voltage waveform on the pad is shown in Fig. 7.4(b). This has practically verified the turn-on effectiveness of this analog ESD protection circuit.

From experimental verification, the positive or negative voltage pulses are really clamped by this analog ESD protection circuit. Mn1 and Mp1 in this analog ESD protection circuit are operated in diode forward-based condition, rather than the drain breakdown condition, therefore it can sustain a much high ESD level even if Mn1 and Mp1 only have much smaller device dimensions. With such smaller device dimensions in Mn1 and Mp1, the total junction capacitance connected to the input pad can be actually reduced for high-frequency applications.

7.2 LAYOUT DESIGN ON THE INPUT CAPACITANCE

For high-precision and high-frequency analog applications, the input capacitance

generated from ESD protection devices needs to be kept not only small enough but also as constant as possible. In this Section, the input capacitance of this analog ESD protection circuit is calculated. A design model to optimize device dimensions and layout spacings on the ESD protection devices is developed to keep the input capacitance almost constant.

7.2.1 Calculation on the Input Capacitance

The main nonlinear source on the input capacitance comes from voltage-dependent junction capacitance at the drain regions of Mn1 and Mp1 in the analog ESD protection circuit. Such a drain junction capacitance increases while the magnitude of reverse-biased voltage across the junction decreases. The total input capacitance looking into the pad with this analog ESD protection circuit can be calculated as :

$$C_{in} = C_{PAD} + C_n + C_p \quad , \tag{7.1}$$

where C_{PAD} is the parasitic capacitance of the bond pad. A bond pad structure formed by different metal layers and different layout area results in different parasitic capacitance to the substrate. Typically, a bond pad with a pad size of 96×96μm^2 and four metal layers in a 0.35-μm CMOS process has a parasitic capacitance of ~0.67pF. This bond pad capacitance can be further reduced, if the pad size is drawn smaller. C_p (C_n) is the drain capacitance of Mp1 (Mn1), which includes junction capacitance and the drain-to-gate overlapped capacitance. The drain junction capacitance of NMOS or PMOS is strongly voltage-dependent. When the signal voltage level on the input pad increases, the drain junction capacitance of Mn1 decreases but the drain junction capacitance of Mp1 increases. On the contrary, the drain junction capacitance of Mn1 increases but the drain junction capacitance of Mp1 decreases, when the signal voltage level on the input pad decreases. With complementary structure on ESD clamp devices, the total input capacitance can be kept almost constant if suitable device dimensions and layout spacings are selected to draw Mn1 and Mp1 devices.

The ESD protection NMOS and PMOS are generally drawn in the multi-finger structure with central drain to save total layout area in the I/O cells. The three-dimension structure of a single-finger NMOS (or PMOS) device is shown in Fig. 7.5(a), whereas the layout top view with the specified layout spacings is shown in Fig. 7.5(b). An MOS device with multi-finger structure can be realized by combining such single-finger structures with sharing drain and source regions between every two adjacent fingers. The finger length of a single poly finger is

defined as G, which is also the channel width of the finger-type MOS device. The spacing from the center of drain contact to the edge of lightly-doped drain region is marked as X, which will be used in the following equations to calculate junction capacitance for the drain bottom plane. The clearance between the poly gate and the drain contact is marked as X_D, and the width of drain contact is marked as X_C. Therefore, the spacing X defined in Fig. 7.5 can be written as

$$X = X_D + \frac{1}{2}X_C - LDIF\,, \tag{7.2}$$

where *LDIF* is the length of the lightly-doped drain diffusion adjacent to the gate. This *LDIF* is an extracted device parameter and given in the *SPICE* parameters of a CMOS process.

The drain region of MOS device with a single poly finger, which is shown in Fig. 7.5, has three different junction capacitances (C_{DJ}, C_{DJSW}, and C_{DJSWG}) and one drain-to-gate overlapped capacitance (C_{GD}). The equation of each capacitance is listed as [127] :

$$C_{GD} = CGDO \cdot G \tag{7.3}$$

$$C_{DJ} = G \cdot X \cdot C_{DJ}' \tag{7.4}$$

$$C_{DJSW} = 2 \cdot X \cdot C_{DJSW}' \tag{7.5}$$

$$C_{DJSWG} = G \cdot C_{DJSWG}'\,, \tag{7.6}$$

where

$$C_{DJ}' = CJ\left(1 + \frac{V_R}{PB}\right)^{-MJ} \text{ F/m}^2 \tag{7.7}$$

$$C_{DJSW}' = CJSW\left(1 + \frac{V_{SW}}{PBSW}\right)^{-MJSW} \text{ F/m} \tag{7.8}$$

$$C_{DJSWG}' = CJSWG\left(1 + \frac{V_{SWG}}{PBSWG}\right)^{-MJSWG} \text{ F/m}\,. \tag{7.9}$$

C_{DJ}' is the junction capacitance per unit area of the drain bottom plane. C_{DJSW}' and C_{DJSWG}' are the junction capacitance per unit length of the drain region at the sidewall with field oxide and the sidewall with poly gate, respectively. The *SPICE* parameters used to calculate the capacitance of NMOS and PMOS devices in a 0.35-μm silicided CMOS process are summarized in Table 7.2 [128].

Substituting above equations into (7.1) with relative device parameters for Mn1 and Mp1, the total input capacitance C_{in} of the analog ESD protection circuit can be expressed as

$$C_{in} = C_{PAD} + k_n \cdot \left\{ G_n \cdot CGDO_n + G_n \cdot X_n \cdot CJ_n \left(1 + \frac{V_i}{PB_n} \right)^{-MJ_n} + \right.$$

$$\left. G_n \cdot CJSWG_n \left(1 + \frac{V_i}{PBSWG_n} \right)^{-MJSWG_n} + 2 \cdot X_n \cdot CJSW_n \left(1 + \frac{V_i}{PBSW_n} \right)^{-MJSW_n} \right\} +$$

$$k_p \cdot \left\{ G_p \cdot CGDO_p + G_p \cdot X_p \cdot CJ_p \left(1 + \frac{V_{DD} - V_i}{PB_p} \right)^{-MJ_p} + \right.$$

$$\left. G_p \cdot CJSWG_p \left(1 + \frac{V_{DD} - V_i}{PBSWG_p} \right)^{-MJSWG_p} + 2 \cdot X_p \cdot CJSW_p \left(1 + \frac{V_{DD} - V_i}{PBSW_p} \right)^{-MJSW_p} \right\} \qquad (7.10)$$

where

k_n (k_p) is the finger number of the poly gate in the multi-finger Mn1 (Mp1) layout;

G_n (G_p) is the finger length of the poly gate in the multi-finger Mn1 (Mp1) layout;

X_n (X_p) is the layout spacing from the drain contact to the poly gate, defined in (7.2), in the multi-finger Mn1 (Mp1) layout; and

V_i is input voltage level on the pad.

7.2.2 Layout Design to Minimize Capacitance Variation

When layout spacings in Mn1 and Mp1 are modified, the total input capacitance of the analog ESD protection circuit can be adjusted. Based on (7.10), the desired layout parameters to minimize variation on the voltage-dependent input capacitance can be obtained. The partial differential equation of (7.10) on the input voltage is derived as

$$\frac{\partial C_{in}}{\partial V_i} = k_n \cdot \left\{ -MJ_n \cdot G_n \cdot X_n \cdot \frac{CJ_n}{PB_n} \cdot \left(1 + \frac{V_i}{PB_n} \right)^{-MJ_n - 1} - \right.$$

$$MJSWG_n \cdot G_n \cdot \frac{CJSWG_n}{PBSWG_n} \cdot \left(1 + \frac{V_i}{PBSWG_n} \right)^{-MJSWG_n - 1} -$$

$$\left. 2 \cdot MJSW_n \cdot X_n \cdot \frac{CJSW_n}{PBSW_n} \cdot \left(1 + \frac{V_i}{PBSW_n} \right)^{-MJSW_n - 1} \right\} +$$

$$k_p \cdot \left\{ MJ_p \cdot G_p \cdot X_p \cdot \frac{CJ_p}{PB_p} \cdot \left(1 + \frac{V_{DD} - V_i}{PB_p} \right)^{-MJ_p - 1} + \right.$$

$$\mathrm{MJSWG_p \cdot G_p \cdot \frac{CJSWG_p}{PBSWG_p}\left(1+\frac{V_{DD}-V_i}{PBSWG_p}\right)^{-MJSWG_p-1}} +$$

$$\left. 2 \cdot \mathrm{MJSW_p \cdot X_p \cdot \frac{CJSW_p}{PBSW_p}\left(1+\frac{V_{DD}-V_i}{PBSW_p}\right)^{-MJSW_p-1}} \right\}. \tag{7.11}$$

If the value of (7.11) was equal to zero, the input capacitance would be independent to the input voltage level. Unfortunately, the layout parameters (K_n, K_p, G_n, G_p, X_n, and X_p) on Mn1 and Mp1 devices with the specified *SPICE* parameters in a 0.35-μm silicided CMOS process can not keep this $\partial C_{in}/\partial V_i$ always zero, while the input signal has a voltage swing from 0V to VDD (3V).

In analog applications, the analog input signal generally has a common reference voltage, indicated as V_{com} in this chapter. For symmetrical analog input signals with a maximum amplitude of ΔV, the minimum (V_{min}) and maximum (V_{max}) voltage level of analog input signals can be written as

$$V_{min} = V_{com} - \Delta V \text{ , and} \tag{7.12}$$

$$V_{max} = V_{com} + \Delta V \text{ .} \tag{7.13}$$

According to the mean value theorem [129], if input capacitances at the voltage levels of V_{min} and V_{max} are kept the same, the condition of $\partial C_{in}/\partial V_i=0$ is located within this analog input voltage range. Therefore, the input capacitance can have a minimized variation within the analog input voltage range between V_{min} and V_{max}. Substituting V_{min} and V_{max} into (7.10), the condition of $C_{in}(V_{max}) = C_{in}(V_{min})$ to keep the minimum variation on input capacitance can be obtained as

$$k_n \cdot \{\alpha \cdot G_n \cdot X_n + \beta \cdot G_n + 2 \cdot \gamma \cdot X_n\} = k_p \cdot \{\eta \cdot G_p \cdot X_p + \theta \cdot G_p + 2 \cdot \kappa \cdot X_p\}, \tag{7.14}$$

where

$$\alpha = CJ_n \left[\left(1+\frac{V_{min}}{PB_n}\right)^{-MJ_n} - \left(1+\frac{V_{max}}{PB_n}\right)^{-MJ_n} \right] \tag{7.15}$$

$$\beta = CJSWG_n \left[\left(1+\frac{V_{min}}{PBSWG_n}\right)^{-MJSWG_n} - \left(1+\frac{V_{max}}{PBSWG_n}\right)^{-MJSWG_n} \right] \tag{7.16}$$

$$\gamma = CJSW_n \left[\left(1+\frac{V_{min}}{PBSW_n}\right)^{-MJSW_n} - \left(1+\frac{V_{max}}{PBSW_n}\right)^{-MJSW_n} \right] \tag{7.17}$$

$$\eta = CJ_p\left[\left(1+\frac{V_{DD}-V_{\max}}{PB_p}\right)^{-MJ_p} - \left(1+\frac{V_{DD}-V_{\min}}{PB_p}\right)^{-MJ_p}\right] \tag{7.18}$$

$$\theta = CJSWG_p\left[\left(1+\frac{V_{DD}-V_{\max}}{PBSWG_p}\right)^{-MJSWG_p} - \left(1+\frac{V_{DD}-V_{\min}}{PBSWG_p}\right)^{-MJSWG_p}\right] \tag{7.19}$$

$$\kappa = CJSW_p\left[\left(1+\frac{V_{DD}-V_{\max}}{PBSW_p}\right)^{-MJSW_p} - \left(1+\frac{V_{DD}-V_{\min}}{PBSW_p}\right)^{-MJSW_p}\right]. \tag{7.20}$$

By applying the device parameters of Mn1 and Mp1 summarized in Table 7.2 into (7.14)-(7.20), the condition to keep the input capacitance with minimum variation under the voltage levels of V_{DD}=3V, V_{com}=1.5V, and ΔV=0.5V can be found as

$$\begin{aligned}&\mathrm{k_n}\cdot\left\{1.029515\times10^{-4}\cdot\mathrm{G_n}\cdot\mathrm{X_n}+1.098674\times10^{-11}\cdot\mathrm{G_n}+2.204072\times10^{-11}\cdot\mathrm{X_n}\right\}\\&=\mathrm{k_p}\cdot\left\{2.011205\times10^{-4}\cdot\mathrm{G_p}\cdot\mathrm{X_p}+1.156346\times10^{-11}\cdot\mathrm{G_p}+4.762930\times10^{-11}\cdot\mathrm{X_p}\right\}.\end{aligned} \tag{7.21}$$

Therefore, if the layout parameters (K_n, K_p, G_n, G_p, X_n, and X_p) on the multi-finger Mn1 and Mp1 devices are correctly chosen to meet the condition in (7.21), the minimum variation on input capacitance of this analog ESD protection circuit can be achieved within the desired input voltage range. This implies that only choosing suitable device dimensions and layout spacings in the multi-finger Mn1 and Mp1 devices can minimize the variation on input capacitance of ESD protection circuit. This is quite useful to design this analog ESD protection circuit with an almost-constant input capacitance for high-precision analog applications in a given CMOS process.

7.2.3 Calculation Results

Now, if k_p=k_n=2 and G_p=G_n=25μm are chosen with the voltage levels of V_{DD}=3V, V_{com}=1.5V, and ΔV=0.5V, the relation between layout spacings of X_n and X_p to meet the condition of (7.21) is calculated in Fig. 7.6(a), where X_n is found to be linearly dependent on X_p. Based on this condition with the specified layout parameters, the relation between the total input capacitance (without including C_{PAD}) and the input voltage level is calculated from (7.10) and shown in Fig. 7.6(b). The simulation results from *HSPICE* on the total input capacitance (without including C_{PAD}) of the analog ESD protection circuit are also included in Fig. 7.6(b) to verify the accuracy of the derived design model. The model calculated results agree very

well to the *HSPICE* simulated results in Fig. 7.6(b) under many sets of different layout parameters, where each set of different layout parameters meets the condition of (7.21). As shown in Fig. 7.6(b), if the layout parameters X_n and X_p are chosen with smaller values, the analog ESD protection circuit also has a smaller input capacitance. Besides, the analog ESD protection circuit has the smallest input capacitance, when the input voltage level is biased at the analog common reference voltage V_{com}. The percentage of variation on the input capacitance in Fig. 7.6(b) with respect to the smallest input capacitance at V_{com}=1.5V under different layout parameters are calculated and drawn as a function of input voltage in Fig. 7.6(c). If the layout parameters X_n and X_p are chosen with smaller values, the analog ESD protection circuit also has a smaller variation percentage on its input capacitance. Based on such layout parameters found by (7.21), the relation between the partial differential value of $\partial C_{in}/\partial V_i$ calculated from (7.11) and the input voltage is shown in Fig. 7.6(d). The $\partial C_{in}/\partial V_i$ has a value of zero when the input voltage level just biased at the V_{com} of 1.5V. Within the desired analog input voltage range of 1 ~ 2V, the variation percentage on input capacitance is found within 1% in the work region shown in Fig. 7.6(c). With such a small 1% variation on the input capacitance, this analog ESD protection circuit is very suitable for high-frequency and high-precision analog applications.

In Figs. 7.6(a) ~ 7.6(d), the input capacitance is calculated with the analog common reference voltage (V_{com}) chosen at 1.5V, which is equal to the half of 3V VDD. If analog input signals have different common reference voltages, the input capacitance with minimum variation within the desired input voltage range can be still found from above equations. For example, if the voltage levels of V_{DD}=3V, V_{com}=1.0V, and ΔV=0.5V are chosen with k_p=k_n=2 and G_p=G_n=25μm, the relation between X_n and X_p to sustain the condition of (7.14) becomes X_n=1.01604·X_p-0.04261968. Based on this condition, the relation between the input capacitance and the input voltage level is calculated in Fig. 7.7(a), and the variation percentage on input capacitance (without including C_{PAD}) is shown in Fig. 7.7(b) under many sets of layout parameters. Because the analog common reference voltage (V_{com}) is chosen at 1.0V in Fig. 7.7, the input capacitance has the smallest capacitance when the input voltage level is biased at 1V. Within the desired analog input voltage range of 0.5 ~ 1.5V, the variation percentage on input capacitance is also within 1% in the work region shown in Fig. 7.7(b).

On the contrary, if the analog common reference voltage (V_{com}) is chosen at 2.0V for analog applications with a higher input voltage level, the relation between X_n and X_p to sustain the condition of (7.14) becomes X_n=3.75596·X_p+0.09672 with the other parameters of

V_{DD}=3V, ΔV=0.5V, k_p=k_n=2, and G_p=G_n=25μm. Based on this condition, the relation between the input capacitance (without including the C_{PAD}) and the input voltage level is calculated in Fig. 7.8(a), and the variation percentage on input capacitance is shown in Fig. 7.8(b) under many sets of layout parameters. Because the analog common reference voltage (V_{com}) is chosen at 2.0V in Fig. 7.8, the input capacitance has the smallest capacitance when the input voltage level is biased at 2V. Within the desired analog input voltage range of 1.5 ~ 2.5V, the variation percentage of the input capacitance is also within 1% in the work region shown in Fig. 7.8(b). This has shown the flexibility of the derived design model to find suitable layout parameters for minimizing the voltage-dependent variation on input capacitance of the analog ESD protection circuit.

The calculated results in Figs. 7.6 ~ 7.8 are all based on the same layout parameters of k_p=k_n=2 and G_p=G_n=25μm but with different layout parameters of X_n and X_p. The layout parameter of X_n (X_p) has been defined in (7.2) and Fig. 7.5 for Mn1 (Mp1) in the analog ESD protection circuit. For the most general analog applications with the analog common reference voltage (V_{com}) biased at V_{DD}/2 (=1.5V), the relation between X_n and X_p has been shown in Fig. 7.6(a), where X_n is almost two times of X_p to meet the condition in (7.21). For example, if X_p is chosen at 4μm, the corresponding X_n must be drawn about 8.07μm. With such a wider X_n, the layout area of Mn1 is increased but the W/L of Mn1 still keeps the same, as comparing to the original layout design with the same X_n and X_p.

If the finger number (k_n) of Mn1 is increased from 2 to 4, the ratio between X_n and X_p can be found at around 1.0 under the condition of G_p=G_n. Moreover, the total device dimension (W/L) of Mn1 can be increased when the finger number (k_n) of Mn1 is increased from 2 to 4. The relation between the X_n/X_p ratio and the finger length G_p (G_n) to meet the condition of (7.21) is further calculated in Fig. 7.9(a), where the other parameters are V_{DD}=3V, V_{com}=1.5V, ΔV=0.5V, k_p=2, and k_n=4. In Fig. 7.9(a), the X_n/X_p ratio is kept around 1 with only slight variation (from 1.06 to 0.95), even if the finger length G_p (G_n) of Mp1 (Mn1) has a wide-range variation from 0.1 to 1000μm in the 0.35-μm silicided CMOS process. Based on the chosen layout parameters, the relation between input capacitance and input voltage level is calculated in Fig. 7.9(b), and the variation percentage on input capacitance is shown in Fig. 7.9(c) under different sets of layout parameters G_p and G_n. The variation percentage on input capacitance under different layout parameters G_p and G_n is almost the same, as that shown in Fig. 7.9(c). Within the chosen V_{work}=1.5V±0.5V, the variation percentage on input capacitance is still kept below 1%.

From above detailed calculations and analyses on the input capacitance, the derived design model to find suitable layout parameters for minimizing the input capacitance variation can help the analog ESD protection circuit to be well realized in general CMOS processes. The input capacitances calculated and shown in Figs. 7.6 ~ 7.9 only include the junction capacitances of ESD protection NMOS and PMOS in the analog ESD protection circuit. The bond pad capacitance (C_{PAD}) with a wide metal plate to the substrate is essentially a constant capacitor. This bond pad capacitance (C_{PAD}) can be further reduced 50% by a low-C layout design [130]. In the silicon-on-insulator (SOI) CMOS process, ESD protection diodes can be stacked from the pad to VDD and VSS to further reduce the total input junction capacitance. By using the same concept of this design model, the optimized layout for the stacked SOI diodes can be found to further minimize the voltage-dependent variation on input capacitance of ESD protection circuits for more high-precision and high-frequency applications.

If the pure junction diodes are used in this analog ESD protection circuit to replace Mn1 and Mp1 devices, similar calculation as that shown in this design model can be also derived to find the optimized layout for minimizing variation on the voltage-dependent input capacitance. The design model described in this chapter has been derived under the layout condition of Mn1 and Mp1 devices having even number of poly gate fingers. If Mn1 and Mp1 devices are drawn with an odd number of total poly gate fingers, an additional sidewall junction capacitance ($G \cdot C_{DJSW'}$) should be added into the capacitance equation in (7.10) with some modification. But, such a layout style of ESD protection NMOS having an odd number of total poly gate fingers is not recommended in IC products, because the parasitic device interaction between the unguarded drain diffusion and a nearby N+ diffusion often causes some unexpected ESD damages to lower the overall ESD level [131].

7.3 SUMMARY

An analog ESD protection circuit with a very low and almost constant input capacitance, high ESD level, but no series resistance, has been successfully designed and verified in a 0.35-μm silicided CMOS process. The ESD test results and turn-on verifications have shown that this analog ESD protection circuit can effectively protect the analog circuits, especially the differential input stage under the pin-to-pin ESD stress condition. A design model to optimize the device dimensions and layout spacings of ESD protection devices has been

clearly developed to keep the input capacitance as constant as possible in general CMOS processes. If analog input signals have different common reference voltages, this design model can still find suitable device dimensions and layout spacings on ESD protection devices to keep the input capacitance with minimum variation during the desired input voltage range. This has shown the flexibility of the derived model for minimizing voltage-dependent variation on input capacitance of the ESD protection circuit. With suitable layout parameters on the input ESD clamp devices, the variation of total input capacitance of the analog ESD protection circuit can be designed below 1% while the analog input signal has an input voltage swing of 1V. With a much small and almost constant input capacitance, this analog ESD protection circuit is very suitable for current-mode, high-frequency, and high-precision circuit applications with high enough ESD reliability.

Table 7.1
ESD level of the analog ESD protection circuit in human-body-model (HBM) and machine-model (MM) ESD stresses under different pin combinations.

	Pin Combination in ESD Test				
	PS-mode	NS-mode	PD-mode	ND-mode	Pin-to-Pin
HBM (V)	6000	- 8000	7000	- 7000	6000
MM (V)	400	- 400	400	- 400	400

Table 7.2
SPICE parameters on the drain capacitance of NMOS and PMOS devices in a 0.35-μm silicided CMOS process.

	NMOS	PMOS
CGDO	2.79e-10 F/m	2.31e-10 F/m
CJ	1.01893e-3 F/m^2	1.46829e-3 F/m^2
CJSW	3.057956e-10 F/m	4.173308e-10 F/m
CJSWG	1.524314e-10 F/m	1.013197e-10 F/m
MJ	0.3075043	0.5464087
MJSW	0.1929617	0.3948903
MJSWG	0.1929617	0.3948903
PB	0.6944474 V	0.9191281 V
PBSW	0.6944494 V	0.9191281 V
PBSWG	0.6944494 V	0.9191281 V
LDIF	1.2e-7 m	1.2e-7 m

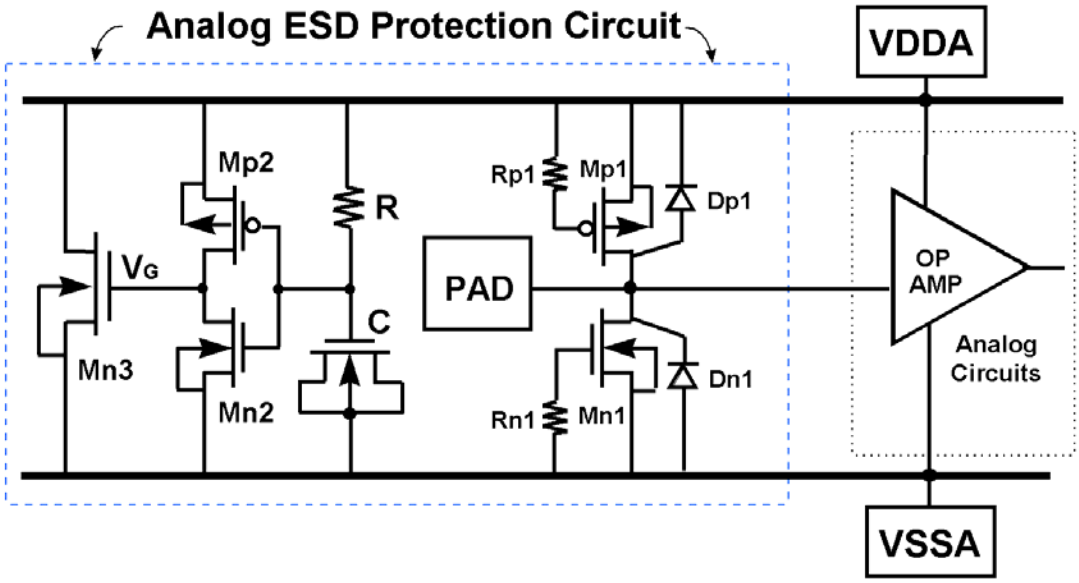
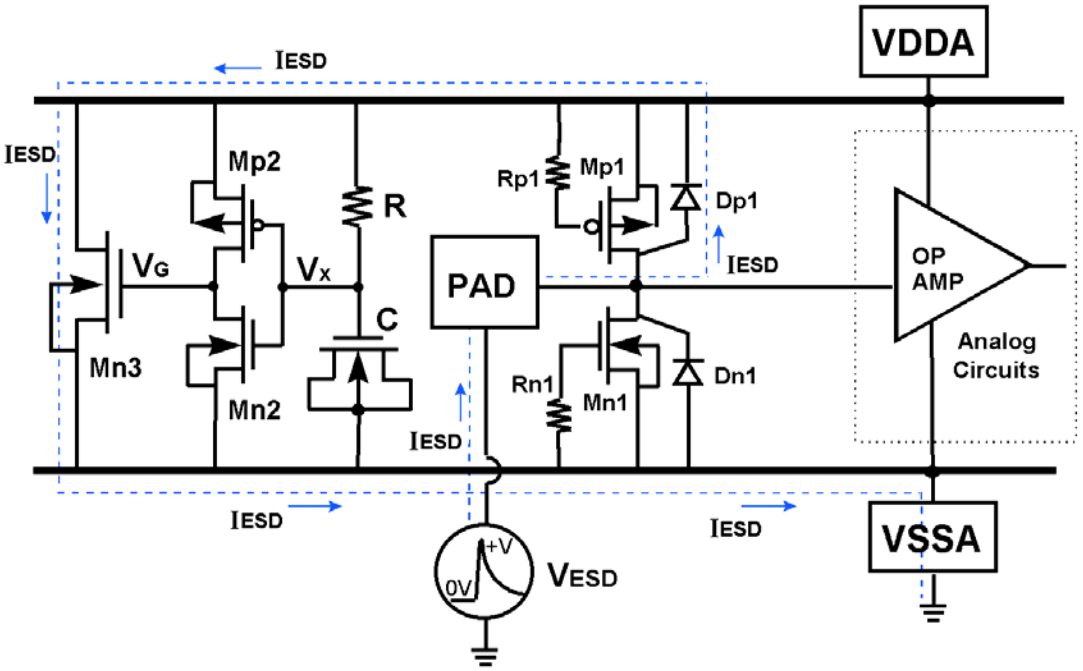
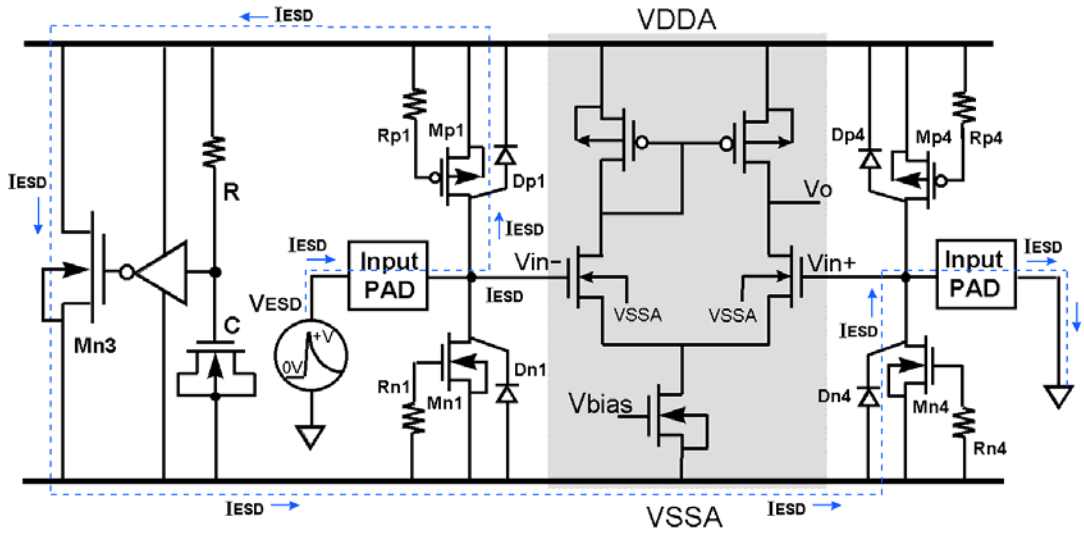


Fig. 7.1 The ESD protection circuit for high-frequency analog pin [125].

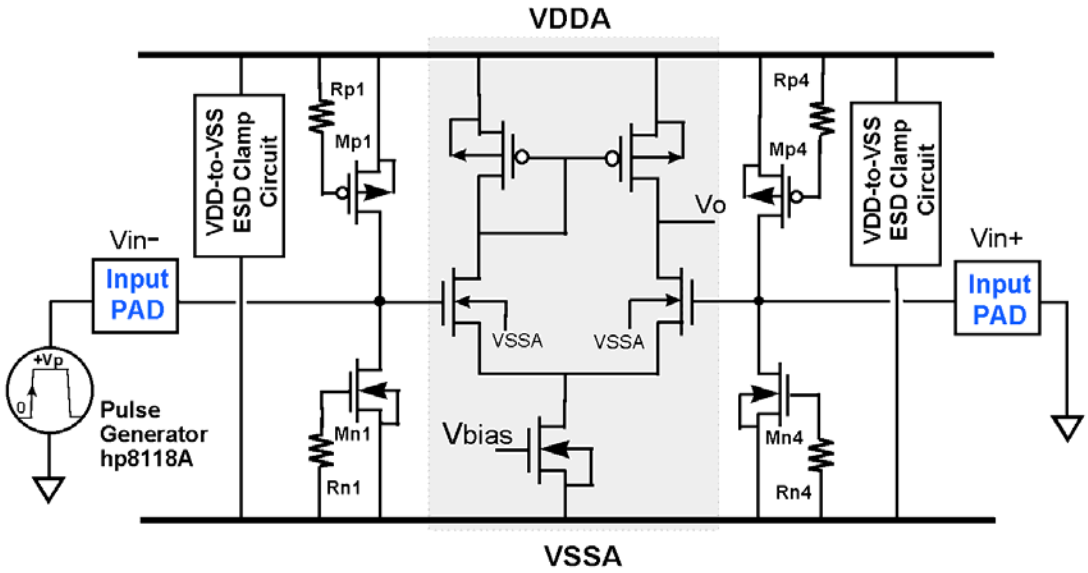


(a)

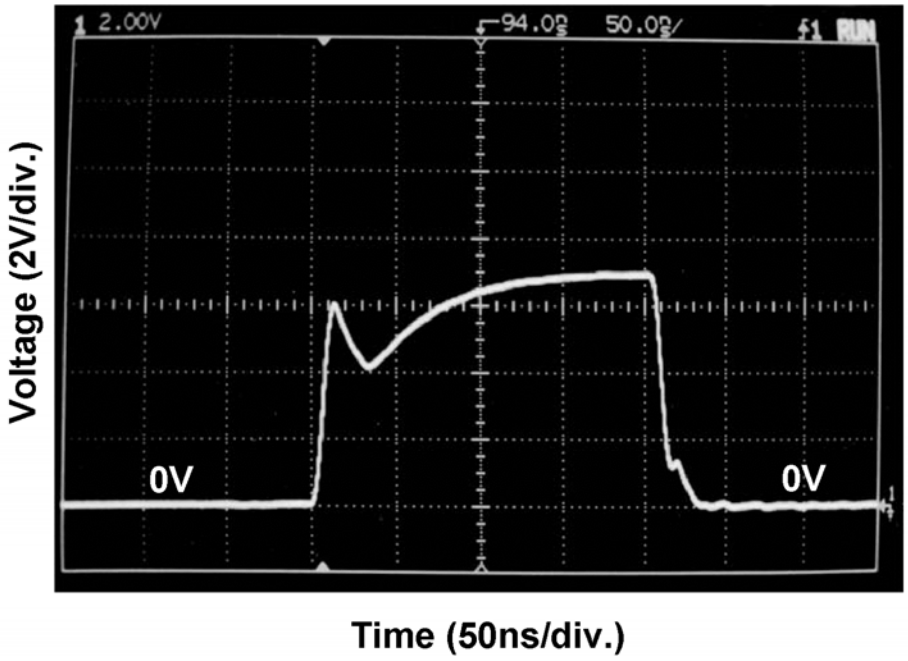


(b)

Fig. 7.2 The ESD current path along the analog ESD protection circuit when the analog pin is zapped in (a) the PS-mode, and (b) the pin-to-pin, ESD stresses.

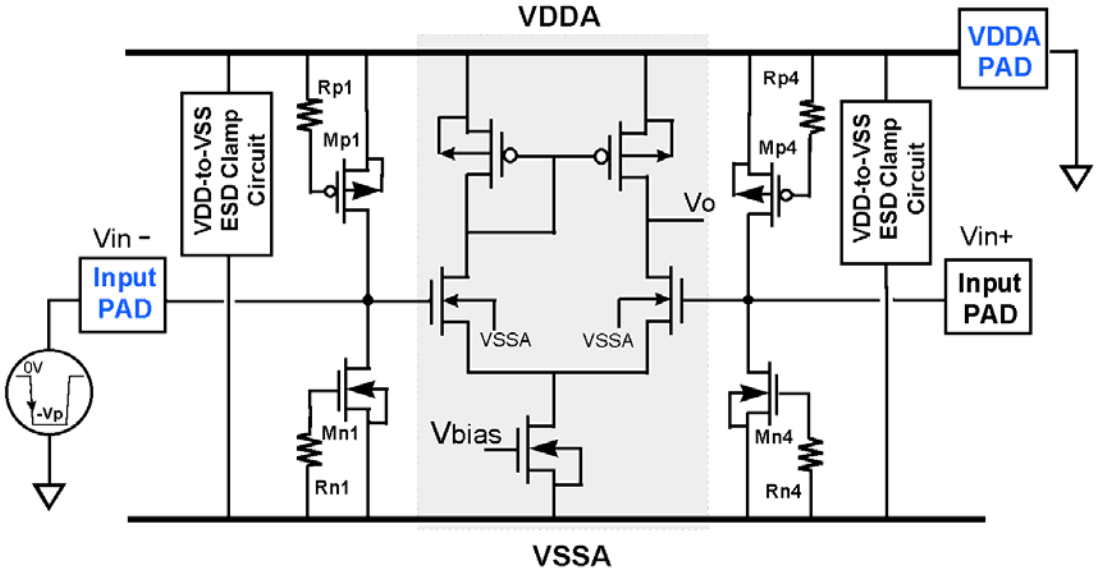


(a)

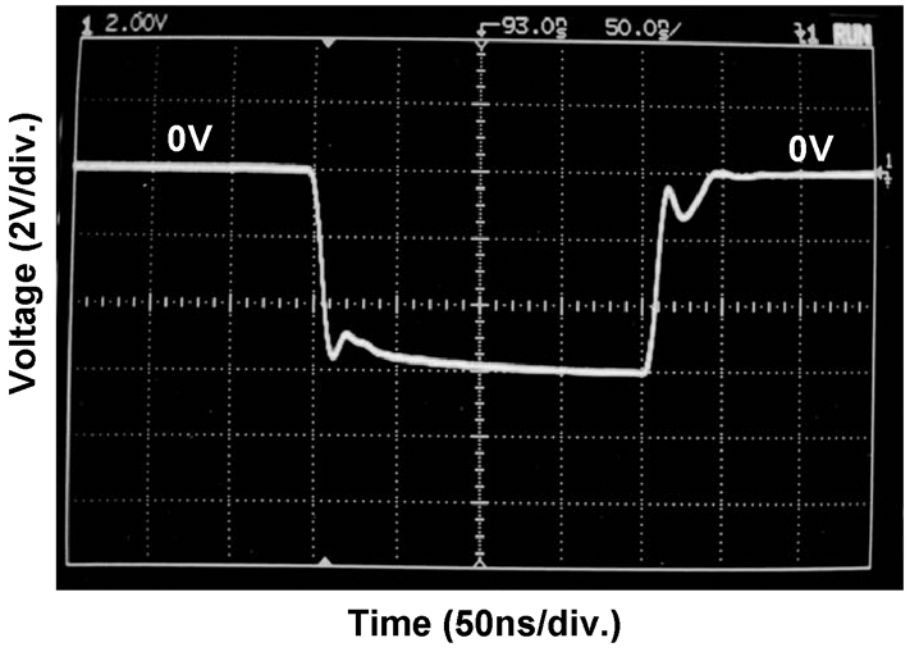


(b)

Fig. 7.3 (a) The experimental setup to verify turn-on efficiency of the analog ESD protection circuit during the positive pin-to-pin ESD stress condition. (b) The degraded voltage waveform when an 8V voltage pulse is applied to the inverting input pin under the pin-to-pin ESD stress condition.

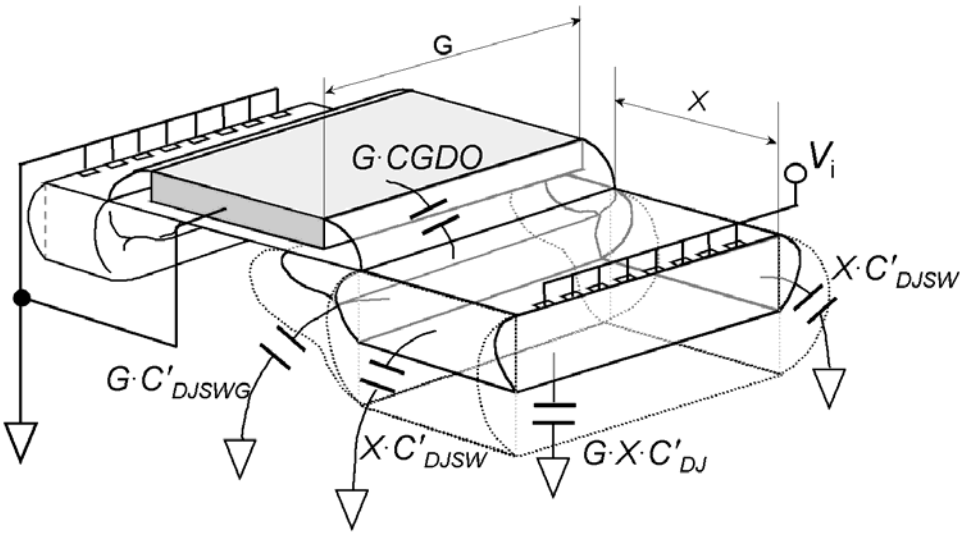


(a)

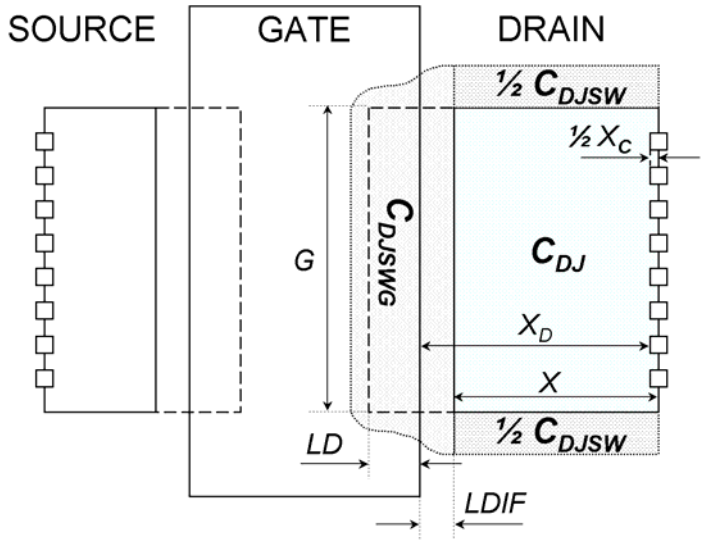


(b)

Fig. 7.4 (a) The experimental setup to verify turn-on efficiency of the analog ESD protection circuit during the ND-mode ESD stress. (b) The degraded voltage waveform when the negative (-8V) voltage pulse is applied to the inverting input pin under the ND-mode ESD stress condition.

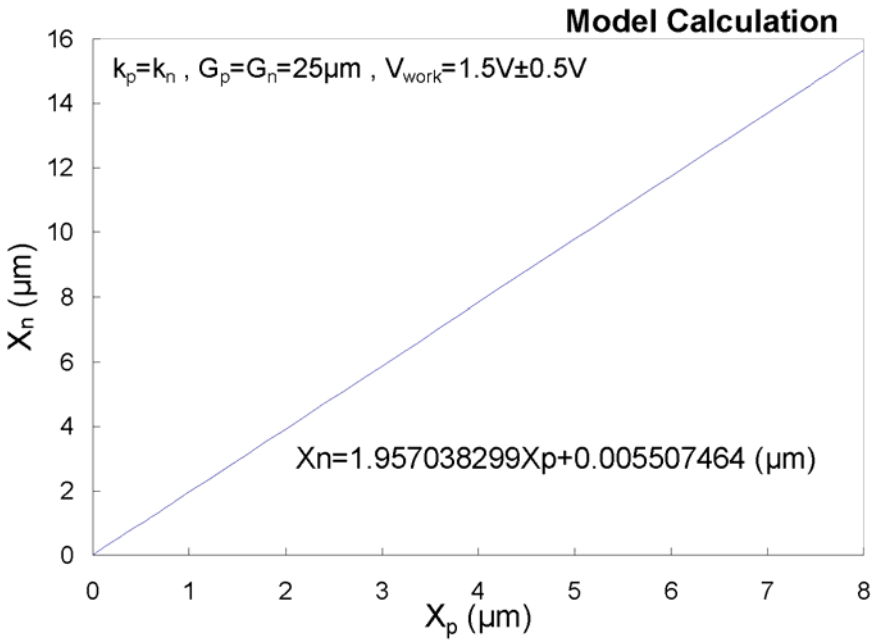


(a)

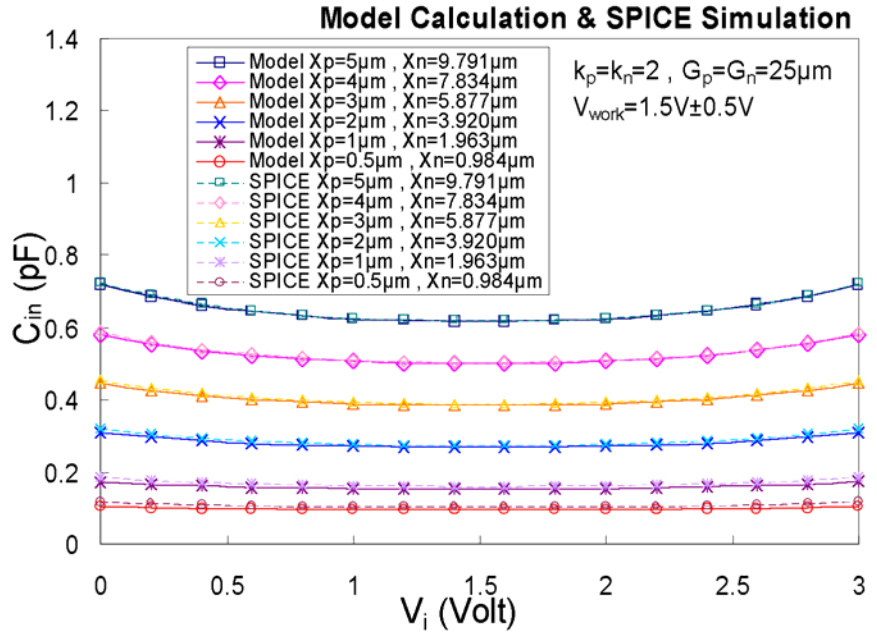


(b)

Fig. 7.5 (a) The three-dimension structure of a single-finger MOS device. (b) The corresponding layout top view of a single-finger MOS device with specified layout spacings.



(a)



(b)

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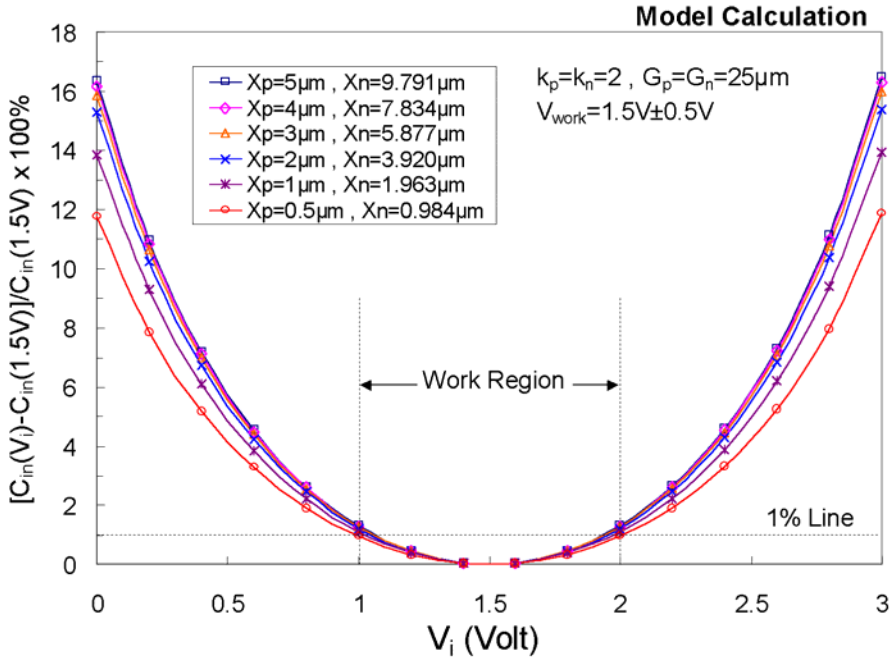
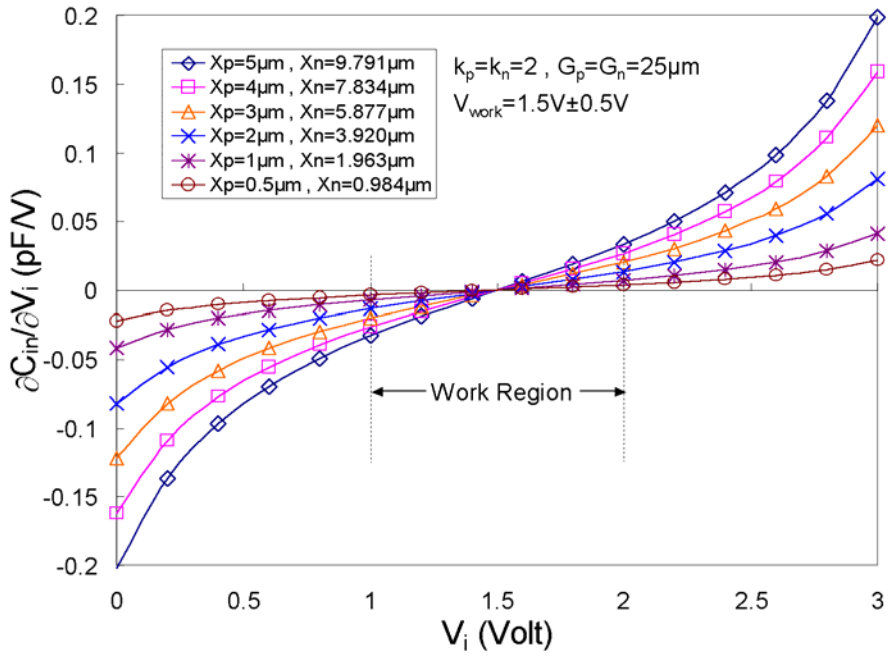
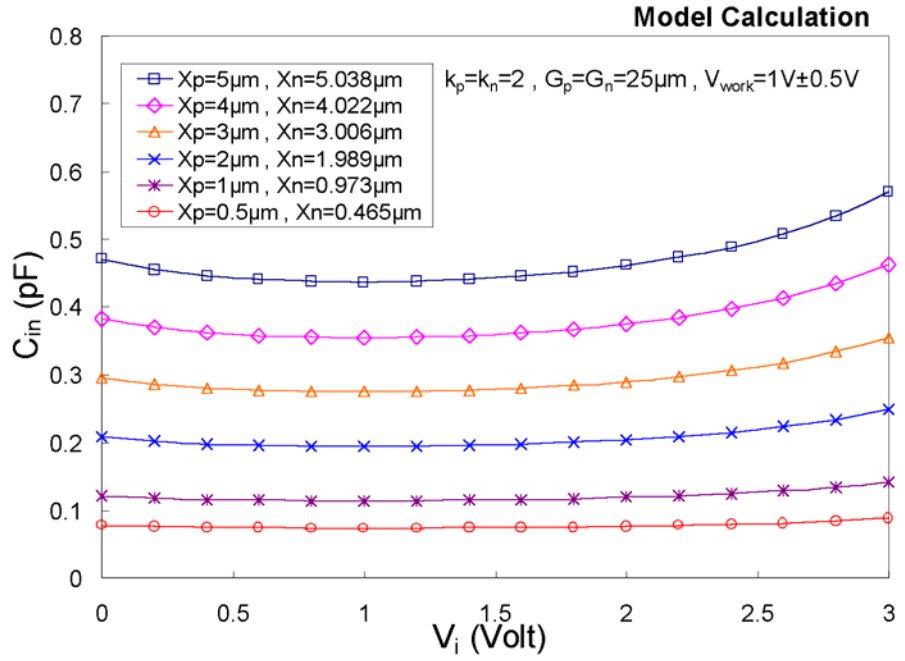


(c)

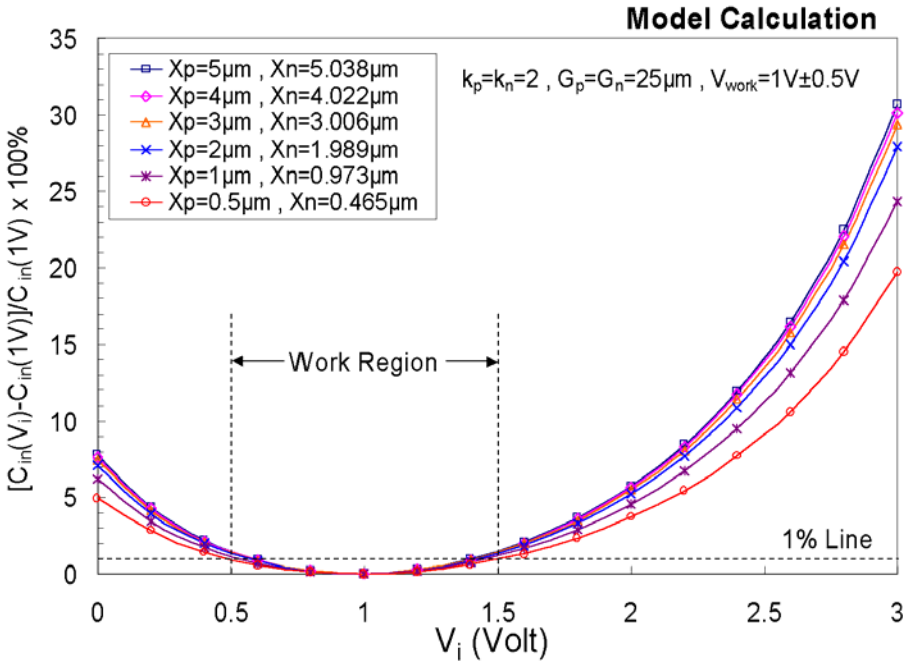


(d)

Fig. 7.6 (a) The relation between layout parameters X_n and X_p to meet the condition in equation (7.21) with the analog common reference voltage biased at 1.5V. (b) The relation between the total input capacitance and the input voltage level under different layout parameters X_n and X_p. (c) The relation between the variation percentage on the input capacitance and the input voltage level under different layout parameters X_n and X_p. (d) The relation between the calculated $\partial C_{in}/\partial V_i$ value and the input voltage level under different layout parameters X_n and X_p.

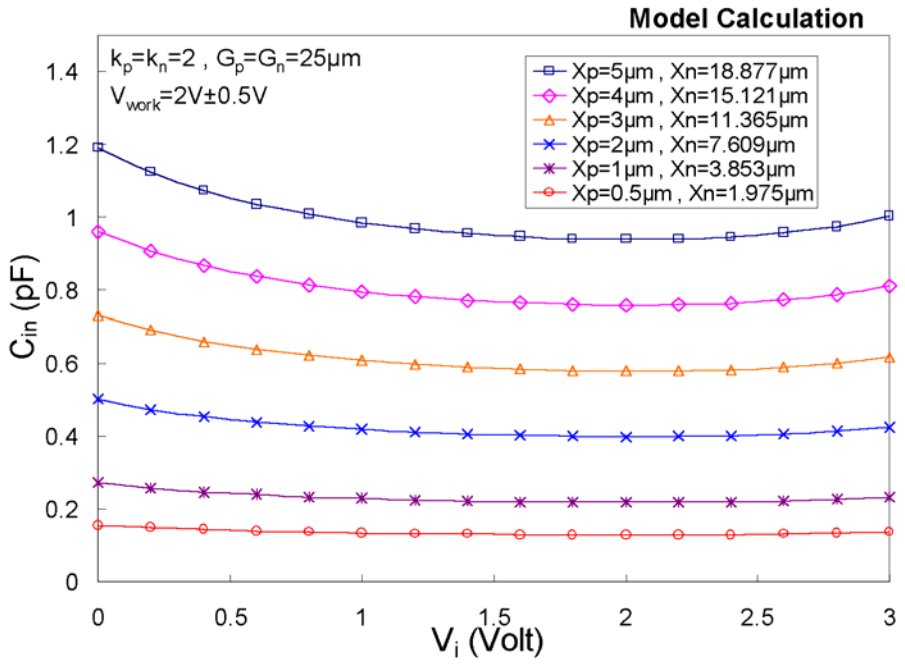


(a)

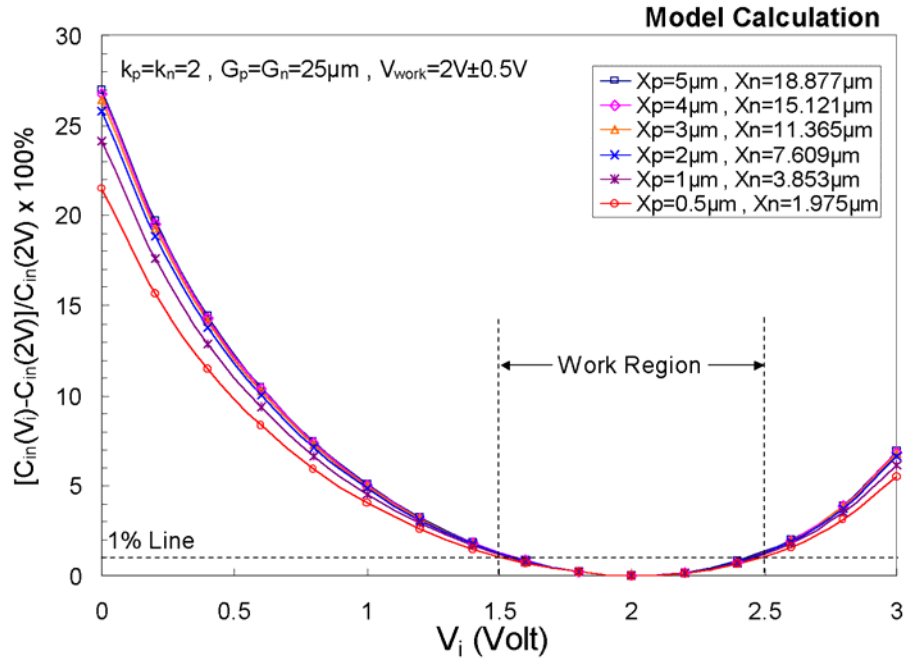


(b)

Fig. 7.7 The relations between (a) the total input capacitance, and (b) the variation percentage on the input capacitance, of the analog ESD protection circuit and the input voltage level under different layout parameters X_n and X_p, which meet the condition in equation (7.14) with an analog common reference voltage biased at 1.0V.

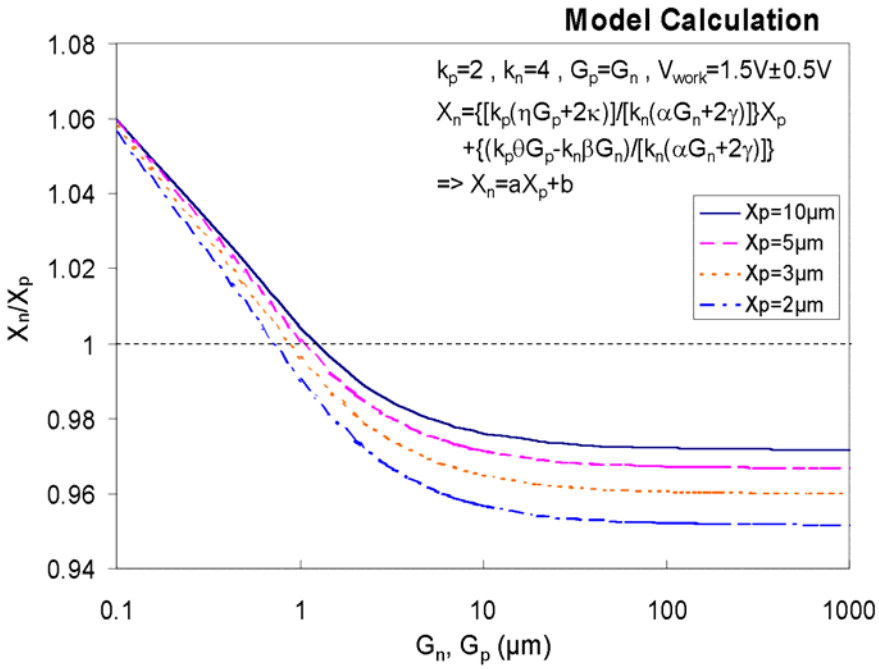


(a)

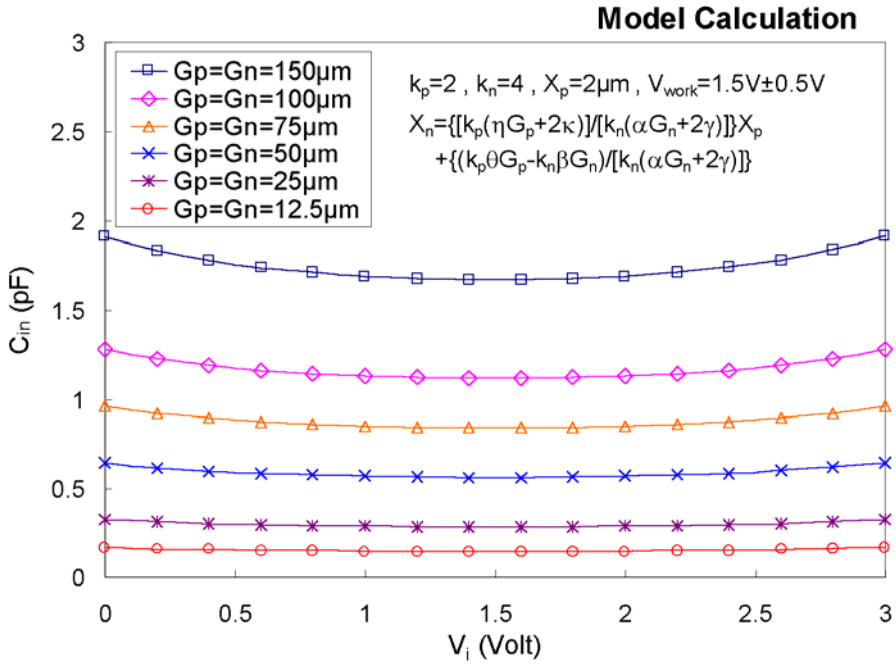


(b)

Fig. 7.8 The relations between (a) the total input capacitance, and (b) the variation percentage on the input capacitance, of the analog ESD protection circuit and the input voltage level under different layout parameters X_n and X_p, which meet the condition in equation (7.14) with an analog common reference voltage biased at 2.0V.



(a)



(b)

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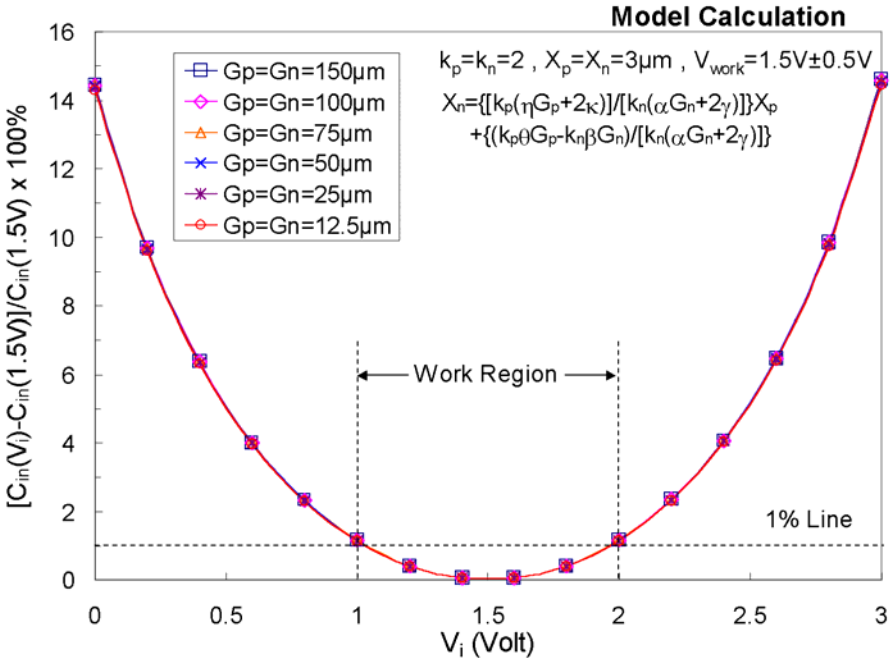


(c)

Fig. 7.9 (a) The relation between the ratio of X_n/X_p and the finger lengths G_n and G_p to meet the condition in equation (7.21) with k_p=2, k_n=4, and V_{work}=1.5V±0.5V. (b) The relation between the total input capacitance of the analog ESD protection circuit and the input voltage level under different layout parameters G_n and G_p. (c) The relation between the variation percentage on the input capacitance and the input voltage level under different layout parameters G_n and G_p.

CHAPTER 8

ON-CHIP ESD PROTECTION DESIGN BY USING POLYSILICON DIODES IN CMOS PROCESS

In the smart card IC application, the electrical power for circuit operations is generated from the transformer (formed by several loops of planner inductor on the circuit board) and the on-chip bridge rectifying circuit into the smart card IC. The traditional full-wave bridge rectifying circuit formed by four diodes to convert the AC power into DC power is shown in Fig. 8.1. An AC voltage between terminals Vs1 and Vs2 is rectified into a DC voltage and stored in the capacitor Cs for application across the load. When the smart card is close to a card reader (or detector), the electromagnetic field generated from the card reader is coupled by the transformer in the smart card and charges up the electrical power of the smart card for circuit operation. The coupled AC power is converted into DC power by the on-chip four-diode bridge rectifying circuit in the smart card IC. With the converted DC power, the information stored in the smart card IC can be emitted out and detected by the card reader for personal identification or other applications. The typical application of such a smart card IC to enter a controlled door is illustrated in Fig. 8.2.

When the on-chip rectifying circuit is realized in a CMOS IC with a p-type substrate, the diodes D1 and D2 are often made by the p-n junctions across P+ diffusion and N-well. The diodes D3 and D4 are often made by the p-n junctions across N+ diffusion and p-substrate. The diode device structures in a CMOS IC with a common p-substrate are illustrated in Fig. 8.3. Due to the common p-substrate of a CMOS IC, besides the diode structures in Fig.3, there are four parasitic bipolar junction transistors (BJT's) Q1, Q2, Q3, and Q4 in this structure. Q1 (Q2) is a parasitic vertical p-n-p BJT between the Vs1 (Vs2) and the common p-substrate. Q3 (Q4) is a parasitic lateral n-p-n BJT between the Vs2 (Vs1) and the VDD-biased N-well. These parasitic BJT's would cause the degraded rectification efficiency, or even no rectification at all, for the full-wave bridge rectifying circuit. The parasitic BJT's are drawn into the full-wave bridge rectifying circuit and illustrated in Fig. 8.4 to show its influence. When the AC voltage is in its positive half-wave period (Vs1 > Vs2), the base-emitter junction (the diode D3) of the parasitic BJT Q3 is forward biased to

turn on the BJT Q3. Thereby, a great amount of charge current is created that directly flows through the parasitic BJT Q3 (from VDD node to Vs2) instead of through the capacitor Cs. During the positive half-wave period (Vs1 > Vs2), the diode D1 is also forward biased and therefore turns on the parasitic BJT Q1. Some of the charge current is directly flowing through the parasitic vertical BJT Q1 (from Vs1 to VSS node) instead of through the capacitor Cs. Similarly, the same problem caused by the parasitic BJT's Q2 and Q4 occurs during the negative half-wave period (Vs1 < Vs2). Therefore, the rectification efficiency of this full-wave bridge rectifying circuit realized in the CMOS IC with a common substrate is seriously decreased, and can even have no rectification at all.

In some modified design, the diodes may be changed to NMOS or PMOS devices in the full-wave bridge rectifying circuit for realization in CMOS IC [132]. The parasitic vertical or lateral BJT's still exist among device structures to degrade its rectification efficiency. Moreover, the different connections between the bulk and the source of NMOS or PMOS devices in the full-wave bridge rectifying circuit cause the body effect to degrade the power converting speed and results in a poor rectification efficiency [132].

If the diodes in the full-wave bridge rectifying circuit are realized by the polysilicon diodes, which have no any parasitic BJT in their device structures, the aforementioned problem can be totally eliminated. Therefore, the rectification efficiency can become much high to convert the coupled AC power into DC power for circuit operation in a smart card. However, due to the low heat dissipation capability of the polysilicon layer, the polysilicon diodes connected at the VS1 and Vs2 nodes (which are wire-bonded to the circuit board in final application) result in a very low human-body-model (HBM) ESD level of around 200~300V. With such a low ESD level, the die of smart card IC assembled into the smart card by the COB (chip-on-board) bonding is very susceptible to ESD events. This limits the ability to mass produce this smart card IC.

In this chapter, the breakdown voltage, leakage current, and ESD performance of the polysilicon diodes are first evaluated in the literature by performing different n- or p-type doping concentrations with experimental process splits. The dependence between the It2 (measured by transmission line pulse generator) and layout spacing in the polysilicon diodes is also characterized in detail. The HBM ESD level of the smart card IC can be finally improved to $\geq$ 3kV by using a new power-rail ESD clamp circuit with the stacked polysilicon diodes as the turn-on control circuit [133].

8.1 ORIGINAL DESIGN IN A SMART CARD IC

Due to the aforementioned concerns on both leakage and substrate current in the practical smart card applications, the four-diode bridge rectifying circuit cannot be simply realized by using the n+ / P-substrate or the p+ / N-well junction diodes in a bulk CMOS process. Therefore, the on-chip bridge rectifying circuit in this smart card IC is realized by four polysilicon diodes, which is shown in Fig. 8.5. The coupled AC voltage across the pad1 and pad2 has a maximum voltage swing of 12V and a frequency of 125 kHz in the smart card application. The memorized data or number in the smart card IC for identification is emitted out by the output PMOS (Mp2) in cooperation with the off-chip transformer. The diodes (Dp1, Dn1, Dp2, and Dn2) to form the four-diode bridge rectifying circuit are all realized by the polysilicon layer with p+ / n- / n+ doping concentration. The device structure and layout top view of the polysilicon diodes realized in a CMOS process are shown in Fig. 8.6(a) and Fig. 8.6(b), respectively. The polysilicon layer has a thickness of 1500Å in a 0.8-μm CMOS process. The layout spacing S of the lightly doped center region in polysilicon diode is originally drawn as 3 μm. The anode and cathode contacts of the polysilicon diode have a clearance of 4 μm to the lightly doped center region.

To sustain a higher breakdown voltage (>12V) of the polysilicon diode for smart card application, an extra mask layer is added into the CMOS process flow to implant the n- region in the polysilicon diode. The p+ (n+) region in the polysilicon diode is implanted with a doping concentration of 6E15 (3.5E15) cm^{-3}, which is the same as the drain/source implantation of PMOS (NMOS) in the CMOS process.

Due to the limitation of using the bulk p-n junction diodes to realize the bridge rectifying circuit, the on-chip ESD protection circuits for pad1 and pad2 are therefore also realized by the polysilicon diodes (Dp1, Dn1, Dp2, and Dn2) with an input series resistor (R1, R2) of 500Ω. Each polysilicon diode has a total perimeter of 250μm. The n- region has a width of 3μm between the p+ and n+ regions of the polysilicon diode. A gate-coupled NMOS with a device dimension (W/L) of 300μm/ 2μm is also added into the chip across VDD and VSS power lines as the VDD-to-VSS clamp circuit for ESD protection. Such an NMOS has a breakdown voltage of ~16.5V. However, the human-body-model (HBM) ESD level of this smart card IC fabricated in a 0.8-μm CMOS process is only around ~300V, especially on the pad1 pin with the polysilicon diodes which are fully isolated from the p-substrate. With an

ESD level below 500V, the die of smart card IC assembled into the smart card by the COB (chip-on-board) bonding is very susceptible to ESD events.

To improve the ESD level of the smart card IC, a process split on increasing the doping concentration of the n- region in the polysilicon diode had been investigated in the 0.8-μm CMOS process. The increased doping concentration of the n- region can lower the breakdown voltage of the polysilicon diode, therefore reducing the ESD-generated heat located on the polysilicon diode. The experimental results are summarized in Table 8.1, where the HBM ESD level of pad1 pin in VSS(+) test mode is only varying from 150V to 300V when the n- doping concentration is increased from 3E13 to 9E13 cm^{-3}. Even in the VSS(-) ESD test mode, where the polysilicon diode is forward stressed, the HBM ESD level of pad1 pin is varying from 400V to 600V only. This is quite low for a diode with a perimeter of 250μm in forward-biased condition. The high turn-on resistance of the polysilicon diode would limit the ESD current discharged through the polysilicon diode and cause ESD damage located on the internal devices.

The photo-emission-microscope (EMMI) pictures of failure locations on the smart card IC after the VSS(+) and VDD(-) ESD stresses are shown in Fig. 8.7(a) and Fig. 8.7(b), respectively. In Fig. 8.7(a) [Fig. 8.7(b)], the ESD failure is located on the NMOS (PMOS) gate oxide of the first input stage that connected to the pad1 pin through the resistor R1, rather than on the polysilicon diodes Dp1 or Dn1. The PMOS and NMOS in the 0.8-μm CMOS process have a gate-oxide thickness of 250Å. In this original design, the polysilicon diodes and the VDD-to-VSS ESD clamp circuit with gate-coupled NMOS cannot effectively protect the 250-Å gate oxide of the input circuits. The inefficiency of the original ESD protection design in Fig. 8.5 could be caused by the high trigger voltage (Vt1) of the VDD-to-VSS ESD clamp circuit, the parasitic resistance along the VDD/VSS power rails [91]-[93], or the high turn-on resistance of the polysilicon diodes.

Therefore, only simply changing the n- doping concentration cannot effectively improve ESD level of the pad1 pin in such a smart card IC. A more efficient ESD protection design should be developed to overcome this problem in the smart card IC with the polysilicon diodes.

8.2 NEW ON-CHIP ESD PROTECTION DESIGN

8.2.1 ESD Protection Circuit

To still apply the polysilicon diodes as the ESD protection devices at the pad1 pin, the concept of whole-chip ESD protection by using a more efficient VDD-to-VSS ESD clamp circuit to significantly improve ESD level of I/O pin [6], [108], [125], [134]-[135] is applied into this smart card IC. The new proposed on-chip ESD protection circuit is shown in Fig. 8.8 with a novel VDD-to-VSS ESD clamp circuit [136], where the ESD protection circuit for pad1 pin has two-stage protection diodes. The VDD-to-VSS ESD clamp circuit is formed by the NMOS Mn3 and its corresponding ESD-detection circuit. The gate of Mn3 is controlled by a stacked diode string, which is also realized by the polysilicon diodes. If the stacked diodes were realized by the p+ diffusion in N-well in CMOS process with a common p-substrate, there was a significant leakage current on the order of mA from VDD to VSS due to the parasitic vertical BJT effect in CMOS process [111], [137]. But, when the stacked diodes are realized by the polysilicon layer, the leakage current can be reduced below 1μA under 5-V VDD bias. Therefore, the leakage current from VDD to VSS through the diode string and the resistor R3 of 10kΩ in Fig. 8.8 can be designed smaller than 1μA, if the diode number in the stacked diode string is large enough. The detailed calculation to find the suitable number (n) of the stacked polysilicon diodes in the proposed VDD-to-VSS ESD clamp circuit has been derived in the Appendix.

For use in the smart card IC with a converted VDD power, 8 polysilicon diodes are used in the diode string to control the gate voltage of Mn3, which has a device dimension (W/L) of 300μm/2μm in the practical IC. When the VDD is charged no more than 5V, the Mn3 is kept off. But when the VDD is charged up greater than 5V, the Mn3 is turned on to clamp the VDD voltage level. By changing the number of polysilicon diodes in the stacked diode string, the clamped voltage level on VDD can be adjusted for different applications.

With the novel VDD-to-VSS ESD clamp circuit, the ESD current under the VSS(+) ESD stress is discharged through the forward-biased Dp1a to VDD, and then discharged through the turned-on Mn3 to VSS, rather than the breakdown of polysilicon diode Dn1a. In the VDD(-) ESD stress, the negative ESD current is conducted to VSS through the forward-biased Dn1a, and then discharged to the grounded VDD through turned-on Mn3, without causing breakdown on polysilicon diode Dp1a. The second diode stage with Dp1b and Dn1b is used to further clamp overstress voltage across the gate oxide of the input circuits for more safe ESD protection. The partial picture of a smart card IC with realization of ESD

protection circuit on the pad1 pin and the VDD-to-VSS ESD clamp circuit is shown in Fig. 8.9, where the polysilicon diodes of pad1 pin are all drawn in the multiple-fingers style with a total perimeter of 300μm for each diode.

8.2.2 Leakage Current in the VDD-to-VSS ESD Clamp Circuit

The leakage current from VDD to VSS in the new proposed VDD-to-VSS ESD clamp circuit can be calculated to find the suitable number (*n*) of diodes in the stacked diode string under different VDD voltage levels. The leakage current includes the sub-threshold current of Mn3 and the diode string current. Due to the diodes are all realized by the polysilicon layer, there is no parasitic vertical BJT in these diodes. The leakage current in such polysilicon diode strings is not increased by the parasitic vertical BJT effect [112], [137]. This makes the proposed VDD-to-VSS ESD clamp circuit to have a much lower leakage current in the IC normal operating condition.

When the diode string has 8 stacked diodes (*n*=8), the leakage current in the proposed VDD-to-VSS ESD clamp circuit under different resistance of R3 is simulated by *HSPICE*, and the results are shown in Fig. 8.10. When the R3 has a higher resistance, the leakage current is slightly increased due to the more sub-threshold current of Mn3, or significantly increased if the Mn3 is turned on. By changing the number of diodes in the stacked diode string, the leakage current of the proposed VDD-to-VSS ESD clamp circuit can be obviously reduced. The *HSPICE* simulated results between the leakage current and VDD voltage level under different diode number (*n*) are shown in Fig. 8.11, where the R3 is kept at 10kΩ. The y-axis of Fig. 8.11 is drawn in log scale to more clearly distinguish the leakage current under different diode number. As seen in Fig. 8.11, the increase of diode number (*n*) causes a smaller leakage current at a fixed VDD voltage level. For general IC specification, the leakage current should be smaller than 1μA. The turn-on voltage *Von* (defined at I=1μA) can be found from the I-V curves of Fig. 8.11. The relation between *Von* and the diode number (*n*) under R3 of 10kΩ or 100kΩ is compared in Fig. 8.12. The increase of R3 resistance only causes a slight increase on the turn-on voltage *Von*, but the increase of diode number causes a significant increase on the turn-on voltage *Von*. The turn-on voltage *Von* (defined @ I=1μA) should be greater than VDD of the IC to meet the leakage current specification of smaller than 1μA. The device dimension (W/L) of Mn3 in these calculations (Fig. 8.10 ~ Fig. 8.12) is fixed at 300μm/2μm. The leakage current is also increased if the device dimension of Mn3 is

increased. For the IC applications in different CMOS process, the suitable diode number in the stacked diode string can be found by the equations in Appendix or *HSPICE* simulation.

8.2.3 Process Splits

To choose a better doping concentration for the n- region in the polysilicon diode for smart card application, a comprehensive process split with different implantation energy is investigated in Table 8.2. If the n- region has a higher doping concentration or a higher implantation energy, the polysilicon diode has a lower breakdown voltage and a higher forward-biased current, which will be better for ESD protection. But, because the transformer-coupled AC voltage could have a maximum voltage swing of 12V, the breakdown voltage of polysilicon diode is selected to be greater than 12V for safe application. Therefore, the split case of #n2 in Table 8.2 is suitable for using in this smart card IC.

Besides, the polysilicon diode can be also realized with a p-type lightly doping region, as that shown in Fig. 8.13(a) and Fig. 8.13(b). The process split is also used to investigate the characteristics of such a p+ / p- / n+ polysilicon diode. The experimental results are listen in Table 8.3, where the polysilicon diode has a layout spacing (the p- doping region) S of 3μm. Due to the concern for the transformer-coupled maximum AC voltage swing of 12V, the split case of #p2 in Table 8.3 is suitable for using in this smart card IC.

8.3 DEPENDENCE OF LAYOUT PARAMETERS ON It2 OF POLYSILICON DIODES

Although the process splits can find the optimized doping concentration for the lightly doped center region in the polysilicon diode, the ESD performance of the polysilicon diode can be further improved by suitably choosing its layout parameters. Under a fixed process split condition with the n- (of 1.5E14 cm^{-3}) doped center region, a lot of polysilicon diodes are fabricated in a test wafer with different layout spacings S of the lightly-doped center region and different total perimeters Wt. A polysilicon diode with a large device dimension is drawn in the multiple-fingers layout style, in which every finger has a layout length of 30 μm. For a polysilicon diode with a total perimeter (Wt) of 300 μm, there are 10 fingers drawn in parallel in the device layout. The measured I-V curves of the polysilicon diodes with a fixed Wt of 300 μm but different S spacings are shown in Fig. 8.14. The polysilicon diode with a

narrower spacing S has a smaller cut-in voltage in the forward-bias condition, and a smaller (in magnitude) breakdown voltage in the reverse-biased condition.

To further investigate ESD performance of the fabricated polysilicon diodes, the TLPG has been successfully set up with a pulse width of 100ns and used to measure It2 of the polysilicon diodes. The TLP-measured I-V curves of the polysilicon diodes with a fixed Wt of 300 μm but different S spacings are shown in Fig. 8.15(a) and Fig. 8.15(b) in the forward- and reverse-biased conditions, respectively. The dependence of It2 on the layout parameter S in both the forward- and reverse-biased conditions is summarized in Fig. 8.16. The TLP-measured I-V curves of the polysilicon diodes with a fixed spacing S of 3 μm but different total perimeters Wt are shown in Fig. 8.17(a) and Fig. 8.17(b) in the forward- and reverse-biased conditions, respectively. The dependence of It2 on the total perimeter Wt of the polysilicon diode in both forward- and reverse-biased conditions is compared in Fig. 8.18. A polysilicon diode with a wider perimeter Wt also has a larger volume for heat dissipation, therefore it has a higher It2 value.

As seen in Fig. 8.16 and Fig. 8.18, the polysilicon diode in forward-biased condition has a much higher It2 value than it does in the reverse-biased condition. This is due to the different power (= $I_{ESD} \times$ Vop, the product of ESD current and the operating voltage of device) generated by the ESD current on the polysilicon diode in the forward- and reverse-biased conditions. The diode in the reverse-biased condition has a higher operating voltage (Vop) across itself than it in the forward-biased condition. Therefore, the ESD current (I_{ESD}) generates more heat on the polysilicon diode in the reverse-biased condition to cause a lower It2.

When the spacing S increases in the polysilicon diode, the It2 is also decreased, even if the diode is stressed in the forward-biased condition. In the forward-biased condition, the power generated by ESD current on the polysilicon diode is mainly decided by the turn-on resistance of the diodes. A polysilicon diode with a smaller layout spacing S has a lower turn-on (breakdown) resistance, therefore it has a relatively higher It2 in the forward-(reverse-) biased condition. With well understood and detailed investigation on It2 of the polysilicon diodes under different bias conditions and layout parameters, ESD robustness of the smart card IC can be effectively improved by arranging the polysilicon diodes to discharge ESD current in its forward-biased condition. This can be achieved by designing a more efficient VDD-to-VSS ESD clamp circuit into the chip, as that shown in Fig. 8.8. The efficient VDD-to-VSS ESD clamp circuit should have a fast turn-on speed and a low turn-on

voltage to discharge the ESD current from VDD to VSS.

8.4 EXPERIMENTAL RESULTS AND DISCUSSION

8.4.1 ESD Test and Failure Analysis

The smart card IC's with the polysilicon diodes and the new proposed ESD protection design in Fig. 8.8 have been fabricated. The polysilicon diodes realized with the n- or p-doped center regions can perform the desired circuit function for smart card application. The HBM ESD test results of this new ESD protection design with the polysilicon diodes of n- or p- doped center regions are listed in Table 8.4. While the polysilicon diodes are realized by the n- (p-) doped center region with a doping concentration of 9E13 (5E13) cm^{-3} and a total perimeter of Wt=300μm (under the spacing of S=3μm), the HBM ESD-sustained level of pad1 pin in the VSS(+) ESD test mode is improved to 3kV (3.5kV). In the VDD(-) ESD test mode, the HBM ESD-sustained level is improved to >4kV (3kV). In both the VSS(-) and VDD(+) ESD test modes, the smart card IC with the polysilicon diodes can sustain the ESD-stress voltage of greater than 4kV. The HBM ESD level of this smart card IC under the direct VDD-to-VSS ESD stress is also greater than 4kV.

The picture showing the failure location on the smart card IC with the p- doped polysilicon diodes after the pad1 pin is zapped with a 4-kV VSS(+) HBM ESD stress is shown in Fig. 8.19(a), where the ESD failure is located on the polysilicon diode Dp1a, rather than on the Dn1a or the gate oxide of input circuits. In Fig. 8.19(b), it shows that the ESD failure is located on the polysilicon diode Dn1a, rather than the diode Dp1a, after the pad1 pin is zapped with a 4-kV VDD(-) HBM ESD stress. From the ESD failure analysis, it has conformed that the ESD current is actually discharged through the polysilicon diodes in the forward-biased conditions. This is achieved by adding the turn-on efficient VDD-to-VSS ESD clamp circuit into the chip, as well as by reducing the parasitic resistance along the power rails, as that shown in Fig. 8.8. The ESD test results have successfully verified the proposed ESD protection design in the smart card IC by using the polysilicon diodes as the ESD clamp devices.

The smart card IC with the n- doped polysilicon diodes has been also verified by the charged- device-model (CDM) ESD test in a socketed CDM tester. The maximum CDM

ESD-sustained voltage level of the fabricated smart card IC is 750V and 600V in the positive and negative CDM stresses conditions, respectively. The picture to indicate the ESD failure location on the smart card IC with the n- doped polysilicon diodes after a negative 700V CDM ESD stress is shown in Fig. 8.20, where the ESD failure is located on the polysilicon diode Dn1a, not on the gate oxide of the first input stage. To sustain a higher CDM ESD level, the layout spacing S of the lightly doped center region has to be reduced to lower the breakdown voltage and to decrease the ESD-generated heat on the polysilicon diodes. The polysilicon diode with a reduced spacing S also has a smaller turn-on resistance to quickly discharge the ESD current. But, the minimum breakdown voltage of the polysilicon diode in this smart card application is limited to 12V, due to the coupled maximum AC voltage. This requirement can be further achieved by arranging the polysilicon diodes into the multi-stage configuration [136], as that shown in Fig. 8.21. The polysilicon diode in every stage has different layout spacing S. The polysilicon diode close to the first input stage of the internal circuits has a narrower spacing S, but the polysilicon diode close to the bond pad has a wider spacing S. The resistance R between every stage can be further reduced to improve CDM ESD level but without degrading its HBM ESD level.

8.4.2 Turn-on Verification

The I-V curve of the new proposed VDD-to-VSS ESD clamp circuit with 8-stacked n-doped polysilicon diodes is measured in Fig. 8.22. When the applied voltage across VDD and VSS is increased higher to bias the gate of Mn3 greater than its threshold voltage, the NMOS Mn3 is turned on to conduct current from VDD to VSS. So, the measured I-V curve in Fig. 8.22 has a sharp current increase when the applied voltage is greater than 5V.

In order to investigate the turn-on efficiency of the polysilicon diodes at the pad1 (Fig. 8.8) with the help of the new proposed VDD-to-VSS ESD clamp circuit, a 0-to-8V voltage pulse is directly applied to the pad1 with the VSS pin relatively grounded and the VDD pin floating. The original 0-to-8V voltage pulse is generated from a pulse generator with a pulse width of 4μs and a rise time of ~10 ns, as the dashed line shown in Fig. 8.23. When such a voltage pulse is applied to the pad1, it is clamped to the voltage level shown in Fig. 8.23. Because the polysilicon diodes of pad1 have a breakdown voltage around 12V, the applied 8-V voltage does not cause any breakdown on the polysilicon diodes of pad1. But, the 0-to-8V voltage pulse is actually clamped to about 6.5V in Fig. 8.23. This is due to the

turn-on of the VDD-to-VSS ESD clamp circuit. Therefore, the overstress voltage on the pad1 is discharged from the pad1 to VDD through the forward-biased polysilicon diode, and then discharged to VSS through the turned-on VDD-to-VSS ESD clamp circuit. This has successfully verified the effectiveness of the new proposed VDD-to-VSS ESD clamp circuit with the stacked polysilicon diodes to significantly improve ESD level of the I/O pad.

8.5 SUMMARY

The device characteristics of the polysilicon diodes in CMOS process have been experimentally evaluated by process splits with different doping concentrations. The It2 of the polysilicon diodes under forward- and reverse-bias conditions and different layout parameters has been clearly investigated. The HBM ESD level of the smart card IC with the polysilicon diodes as ESD protection devices has been successfully improved up to ≥ 3kV in cooperation with a turn-on efficient VDD-to-VSS ESD clamp circuit. By adjusting the number of the stack diodes in the ESD detection circuit, the turn-on efficient VDD-to-VSS ESD clamp circuit can be applied in the IC with different VDD voltage levels. Such ESD-improved smart card IC's have been in mass production with a large sale volume to offer smart card manufacturability without any ESD problem.

8.6 APPENDIX

In Fig. 8.24(a), a diode-string of polysilicon diodes is used to trigger the gate of NMOS. The equivalent circuit of each forward-bias diode is shown in Fig. 8.24(b), where the series resistor (r_d) is turn-on resistance of a polysilicon diode. The equivalent circuit of an NMOS is shown in Fig. 8.24(c) with the consideration of drain and source resistance, r_D and r_S. The current of each diode is:

$$i_d = I_S\left(e^{v_d/\eta v_T} - 1\right). \tag{A.1}$$

The voltage drop on each diode (v_d) is the same to each other. I_S is the saturation current, v_T is the thermal voltage, and the factor η generally has a value between 1 and 2. The total voltage drop (V_{drop}) across the stacked diodes and the resistor *R3* (connected between the gate of NMOS and VSS) can be expressed as:

$$V_{drop} = i_d \cdot R3 + n \cdot (i_d \cdot r_d + v_d) = i_d (R3 + n \cdot r_d) + n\eta v_T \ln\left(1 + \frac{i_d}{I_S}\right), \quad \text{(A.2)}$$

where n is the stacked number of diodes. This equation can be re-written to find the n as function of the gate voltage (v_{gs}) of NMOS as:

$$n = \frac{V_{drop} - v_{gs}}{\eta v_T \ln\left(1 + \frac{v_{gs}}{R3 \cdot I_S}\right) + \frac{r_d}{R3} \cdot v_{gs}}, \quad \text{(A.3)}$$

where

$$v_{gs} = i_d R3. \quad \text{(A.4)}$$

From circuit connection of Fig. 8.8, the V_{drop} equals to VDD. So, the number (n) of stacked polysilicon diodes can be adjusted to reduce the total leakage current, when IC is operating in normal condition. To limit the leakage current through NMOS, the gate voltage of NMOS has to be less than its threshold voltage (V_{th}). The leakage current of NMOS operated in the sub-threshold region ($v_{gs}<V_{th}$) is [138]

$$i_{mn} = \frac{1}{2}\mu_n C_{OX} a v_T^2 \frac{W_{eff}}{L_{eff}} \left(\frac{n_i}{N_A}\right)^2 \left(1 - e^{-\frac{VDD - i_{mn}\cdot(r_D + r_S)}{v_T}}\right) e^{\frac{\psi_s}{v_T}} \left(\frac{\psi_s}{v_T}\right)^{-1/2}. \quad \text{(A.5)}$$

Therefore, the total leakage current of this proposed power-rail ESD clamp circuit can be expressed as:

$$i_{leakage} = i_d + i_{mn}, \quad \text{(A.6)}$$

where the leakage current through stacked polysilicon diodes (i_d) can be got from (A.4), and the leakage current through the NMOS (i_{mn}) can be got from (A.5). Finally, the total leakage current ($i_{leakage}$) can be further expressed as function of v_{gs}:

$$i_{leakage} = \frac{v_{gs}}{R3} + K \cdot \sqrt{\frac{v_T}{\psi_s(v_{gs})}} \cdot e^{\frac{\psi_s(v_{gs})}{v_T}}, \quad \text{(A.7)}$$

where

$$\psi_s(v_{gs}) = (v_{gs} - V_{FB}) - \frac{1}{2}\xi\left\{\sqrt{1 + \frac{4}{\xi}(v_{gs} - V_{FB} - v_T)} - 1\right\}. \quad \text{(A.8)}$$

In these equations, the parameters of K and ξ are constant factors for a CMOS process, and they are defined as:

$$K \equiv \frac{1}{2}\mu_n C_{OX} a v_T^{\,2} \frac{W_{eff}}{L_{eff}} \left(\frac{n_i}{N_A}\right)^2 \left(1 - e^{-\frac{VDD - i_{mn}\cdot(r_D + r_S)}{v_T}}\right), \text{ and} \tag{A.9}$$

$$\xi \equiv a^2 v_T . \tag{A.10}$$

For a given CMOS process, the value of K and ξ can be determined from process parameters.

From (A.3) and (A.7), the relation between n and $i_{leakage}$ can be calculated with the specified factors of *VDD*, *R3*, diode parameters, and NMOS dimension. First, some suitable series resistances (*R3*) are temporarily chosen to calculate the relation between v_{gs} and n from (A.3). The condition of choosing *R3* is considered to keep the gate voltage (v_{gs}) of NMOS smaller than its threshold voltage (V_{th}) in the normal circuit operating condition. If NMOS is turned off, the leakage current will mainly appear through the diode-string and resistor *R3*. For example, when v_{gs} is smaller than 0.01V, *R3*=10KΩ can be chosen to meet the condition of $i_{leakage}$<1μA. Second, the relation between gate voltage (v_{gs}) of NMOS and the total leakage current ($i_{leakage}$) must be calculated to determine the exact value of n. From (A.2) and (A.4), the relation between v_{gs}, i_d, and *R3* can be calculated. Using these values of v_{gs}, the total leakage current ($i_{leakage}$) can be calculated from (A.7).

Table 8.1
HBM ESD level of a smart-card IC with the original ESD protection design under different n-doping concentrations.

n- Doping Concentration (cm-3)	HBM ESD Level (Volt)			
	VDD(+)	**VDD(-)**	**VSS(+)**	**VSS(-)**
9E13	600	300	300	600
5E13	550	300	250	500
3E13	400	250	150	400

(Failure criterion : $I_{Leakage}$ > 1μA @ 5-V bias)

Table 8.2
Process splits on the n-doping concentration to investigate the breakdown voltage and the forward-biased current of the polysilicon diodes.

Split Case	N- Doping Concentration (cm-3)	Current @1-V forward-bias	Breakdown Voltage @1-μA current
# n1	7E13, 80KeV	3.4 μA	23 V
# n2	9E13, 80KeV	24.2 μA	15.6 V
# n3	2E14, 80KeV	807.8 μA	7.8 V
# n4	9E13, 50KeV	7.7 μA	16.5 V
# n5	2E14, 50KeV	706.2 μA	7.8 V

Table 8.3
Process splits on the p-doping concentration to investigate the breakdown voltage and the forward-biased current of the polysilicon diodes.

Split Case	P- Doping Concentration (cm-3)	Current @1-V forward-bias	Breakdown Voltage @1-μA current
# p1	1E13, 80KeV	8.4 μA	21.5 V
# p2	5E13, 80KeV	252 μA	12.4 V
# p3	9E13, 80KeV	928 μA	9.3 V

Table 8.4
HBM ESD level of the smart-card IC with the new proposed ESD protection design.

Polysilicon-Diode Doping Concentration (cm-3)	HBM ESD Level (Volt)			
	VDD(+)	**VDD(-)**	**VSS(+)**	**VSS(-)**
N-, 9E13	> 4kV	> 4kV	3kV	> 4kV
P-, 5E13	> 4kV	3kV	3.5kV	> 4kV

(Failure criterion : $I_{Leakage}$ > 1μA @ 5-V bias)

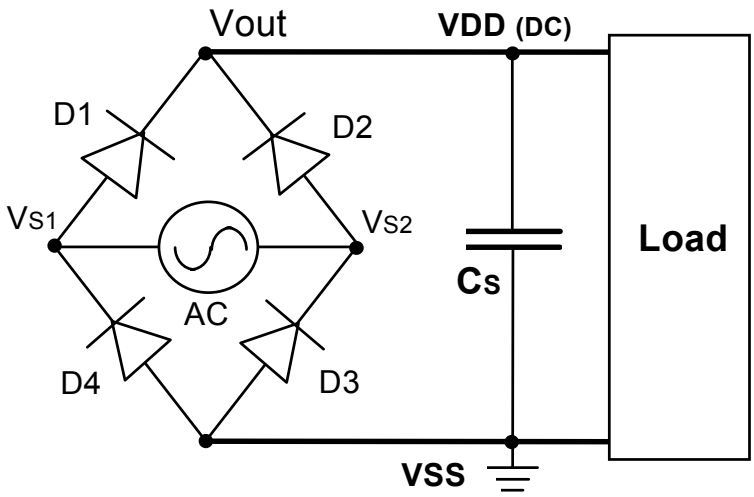


Fig. 8.1 The traditional full-wave bridge rectifying circuit formed by four diodes to convert the AC power into DC power.

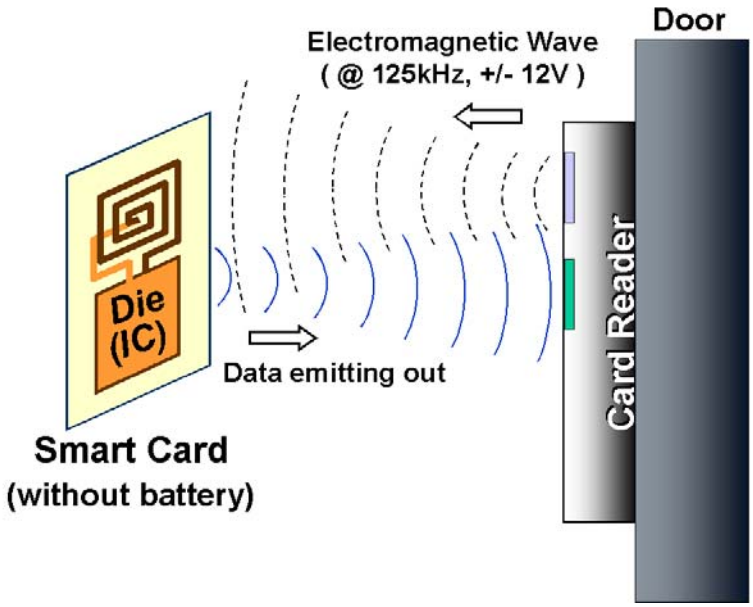


Fig. 8.2 The typical application of a smart card IC for personal identification to enter a controlled door.

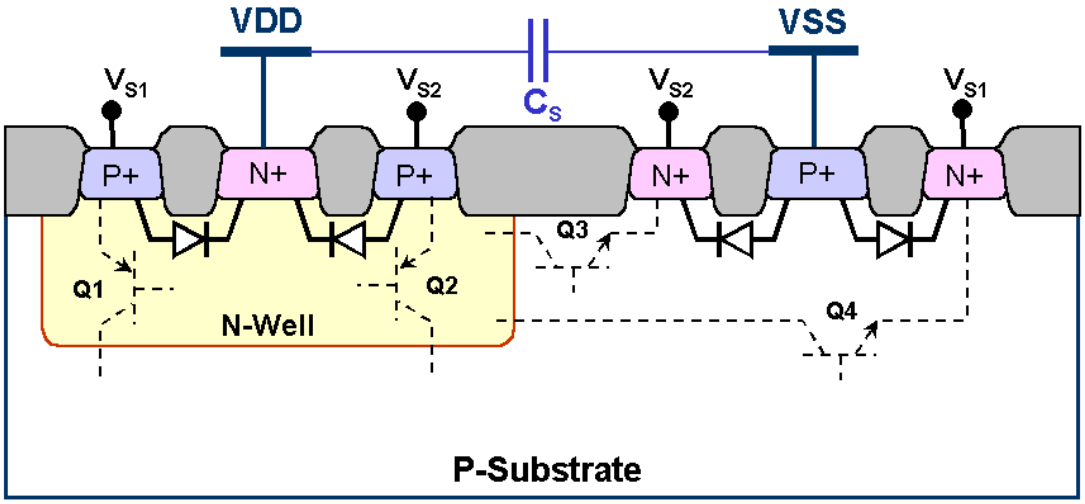


Fig. 8.3 Device cross-sectional view of the four p-n junction diodes of the full-wave bridge rectifying circuit realized in a CMOS IC with a common p-type substrate.

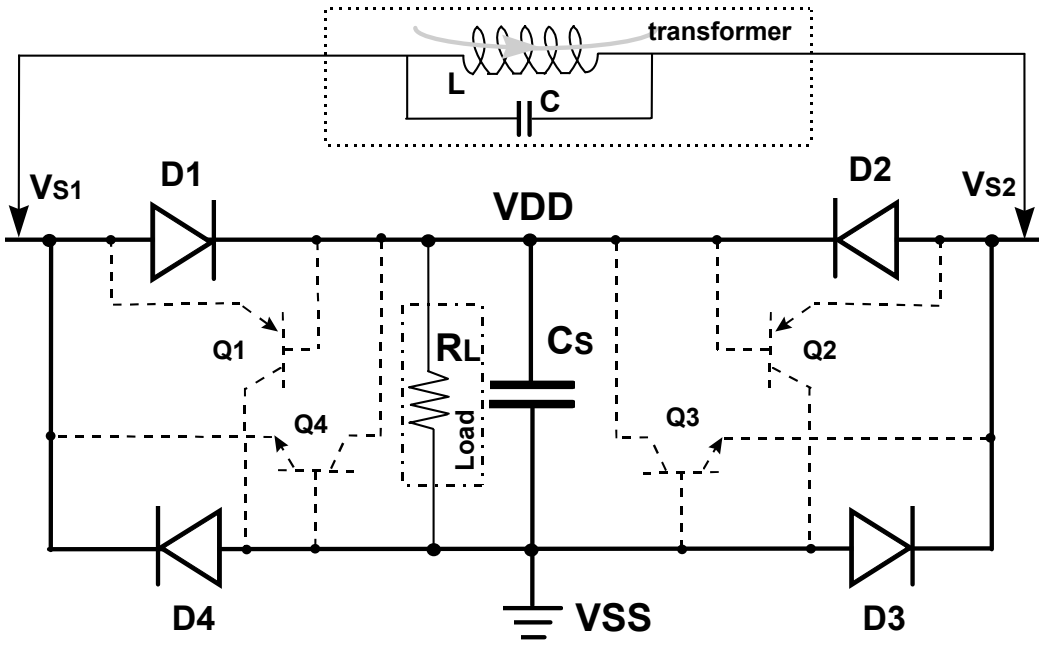


Fig. 8.4 The leakage current paths along the parasitic BJT's in the traditional full-wave bridge rectifying circuit realized in CMOS IC with a common p-type substrate.

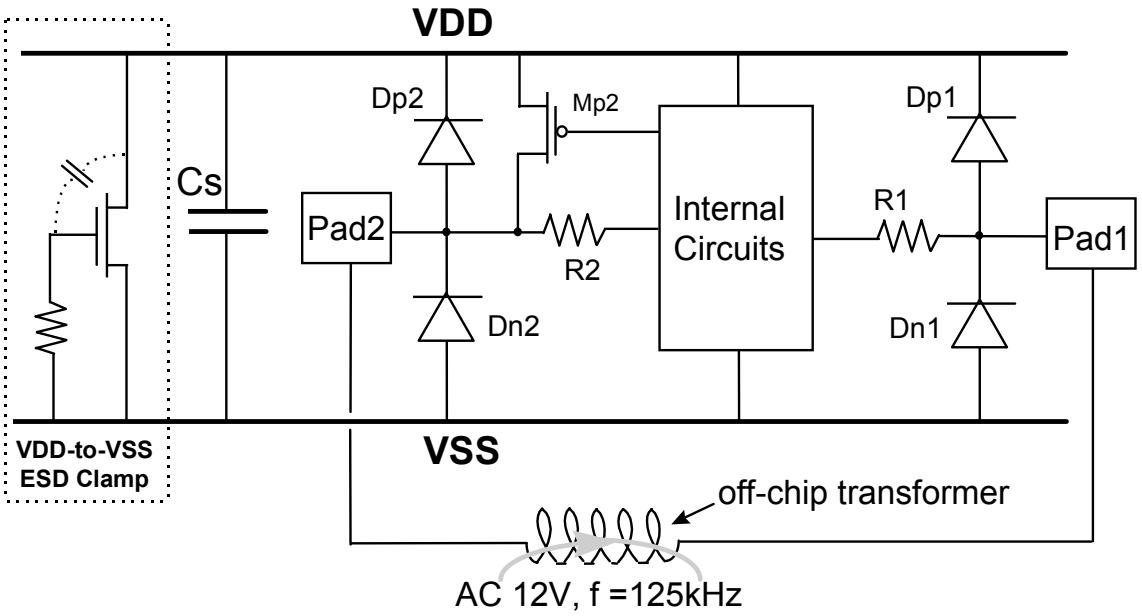


Fig. 8.5 The on-chip bridge rectifying circuit in a smart card IC realized by four polysilicon diodes with the original design of on-chip ESD protection circuits.

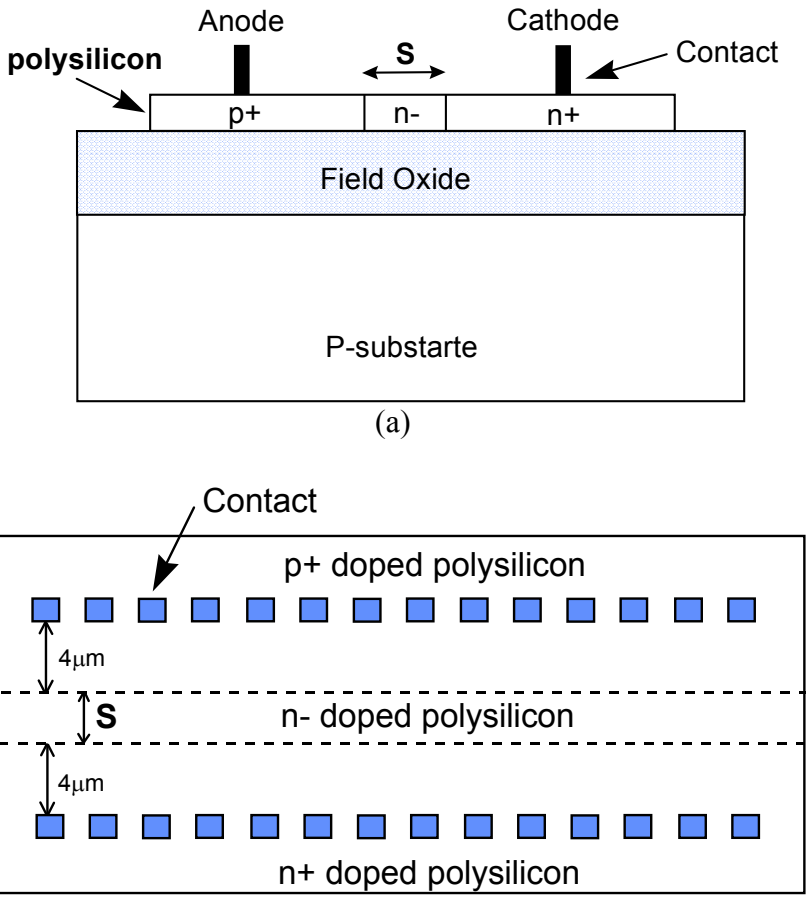
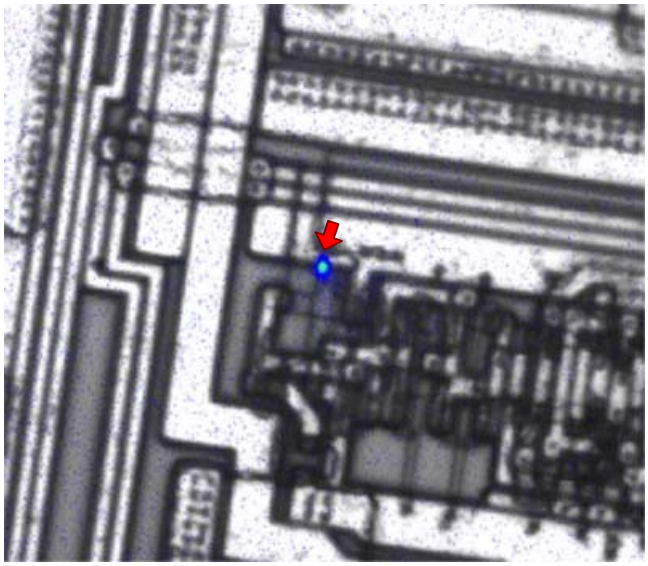
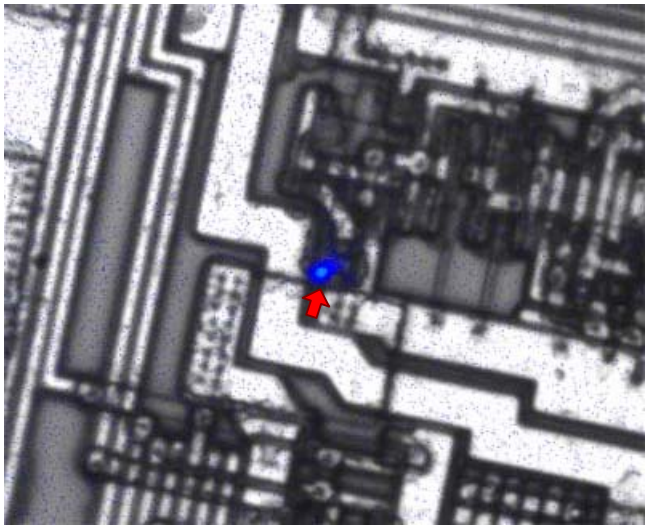


Fig. 8.6 (a) The device structure, and (b) the layout top view, of the p+/n-/n+ polysilicon diode realized in a 0.8-μm CMOS process.



(a)



(b)

Fig. 8.7 The EMMI pictures to show the ESD failure location (indicated by the arrows) on the input circuits after the (a) VSS(+) test mode, and (b) VDD(-) test mode, HBM ESD stresses.

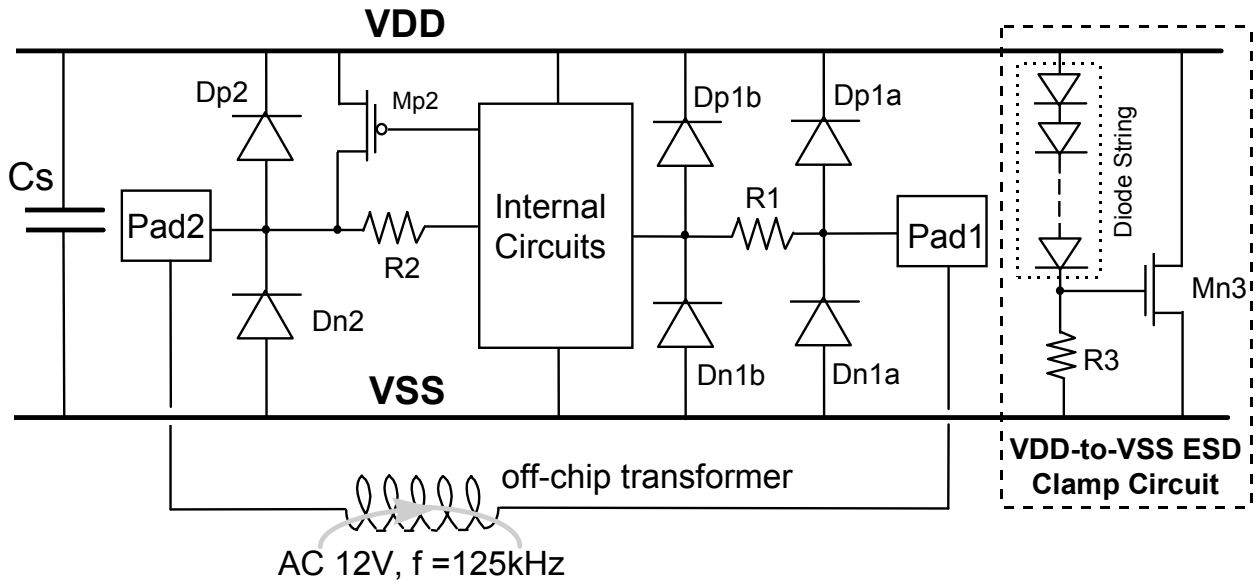


Fig. 8.8 The new design of on-chip ESD protection circuit with a novel VDD-to-VSS ESD clamp circuit in the smart card IC.

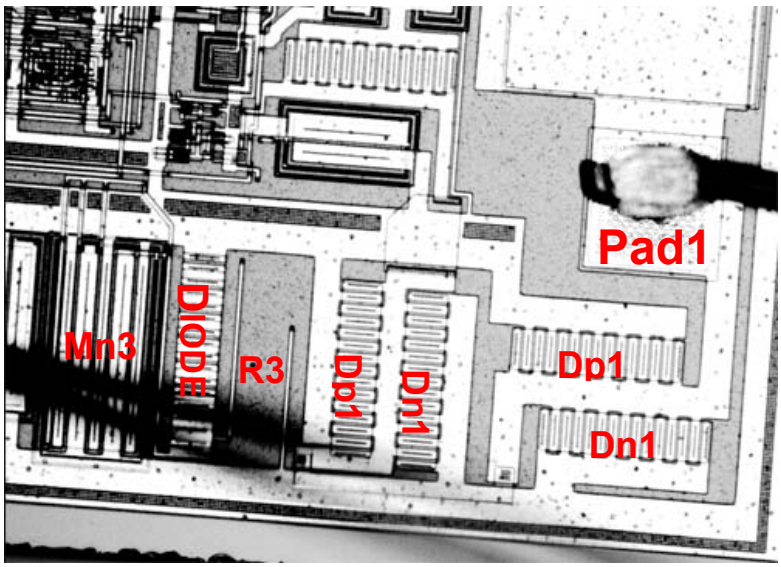


Fig. 8.9 The partial picture of a smart card IC with the realization of ESD protection circuit on the pad1 pin and the VDD-to-VSS ESD clamp circuit.

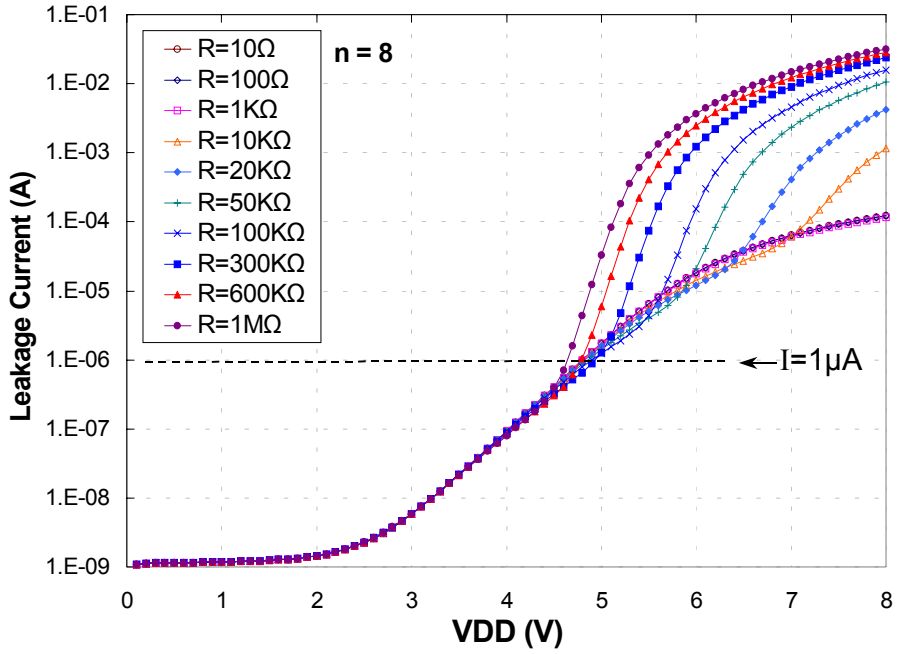


Fig. 8.10 *HSPICE* simulated leakage current of the proposed VDD-to-VSS ESD clamp circuit with 8 diodes in the stacked diode string under different resistance of R3. (Y axis is drawn in logarithmic scale.)

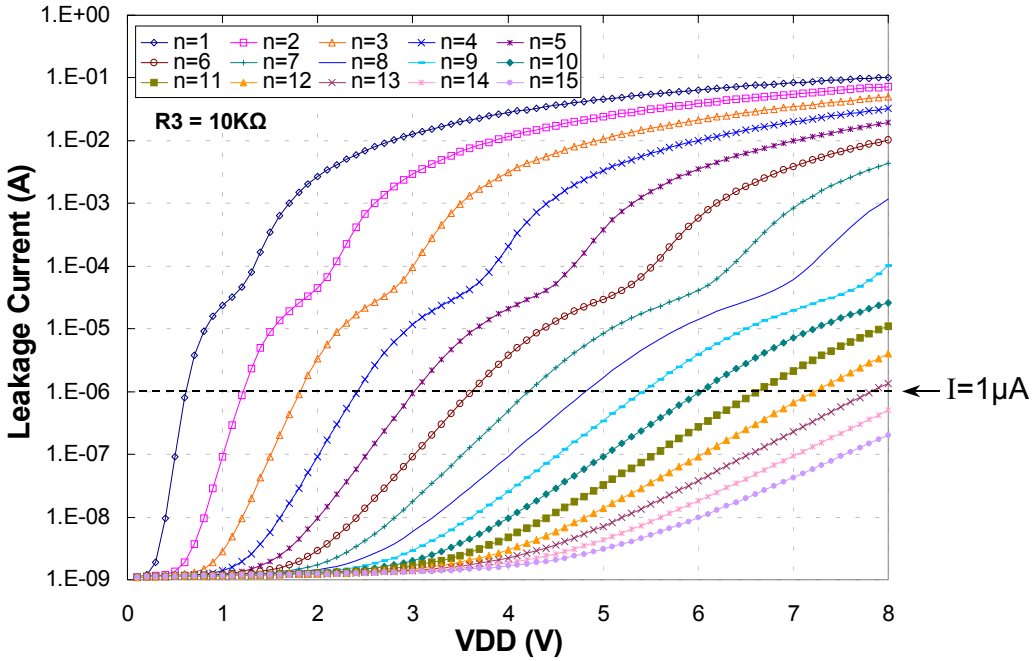


Fig. 8.11 *HSPICE* simulated leakage current of the proposed VDD-to-VSS ESD clamp circuit with a fixed R3 of 10kΩ but different diode number (*n*) in the stacked diode string. (Y axis is drawn in the logarithmic scale.)

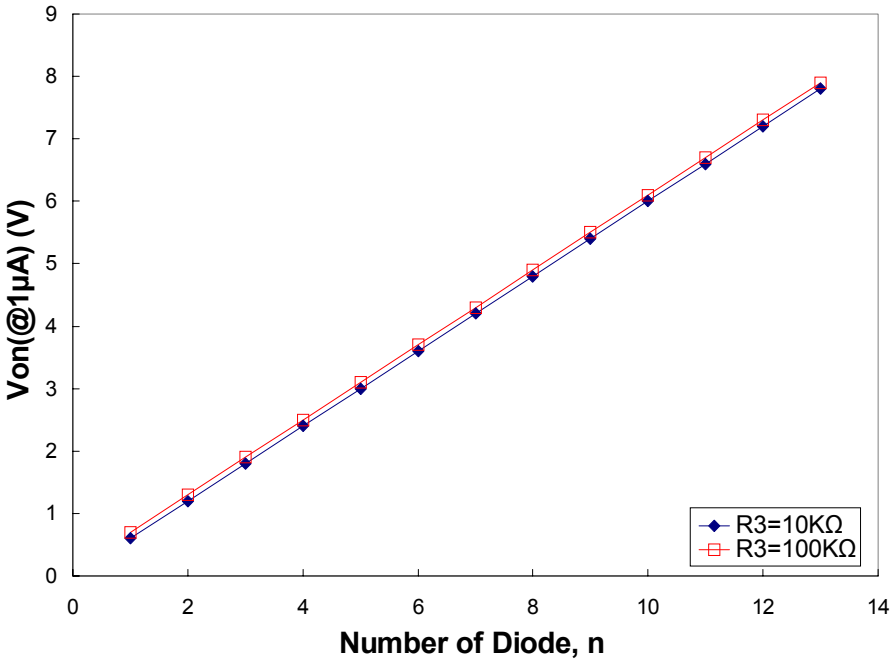


Fig. 8.12 The relation between *Von* defined at I=1μA and the diode number (*n*) of the VDD-to-VSS ESD clamp circuit under R3 of 10kΩ or 100kΩ.

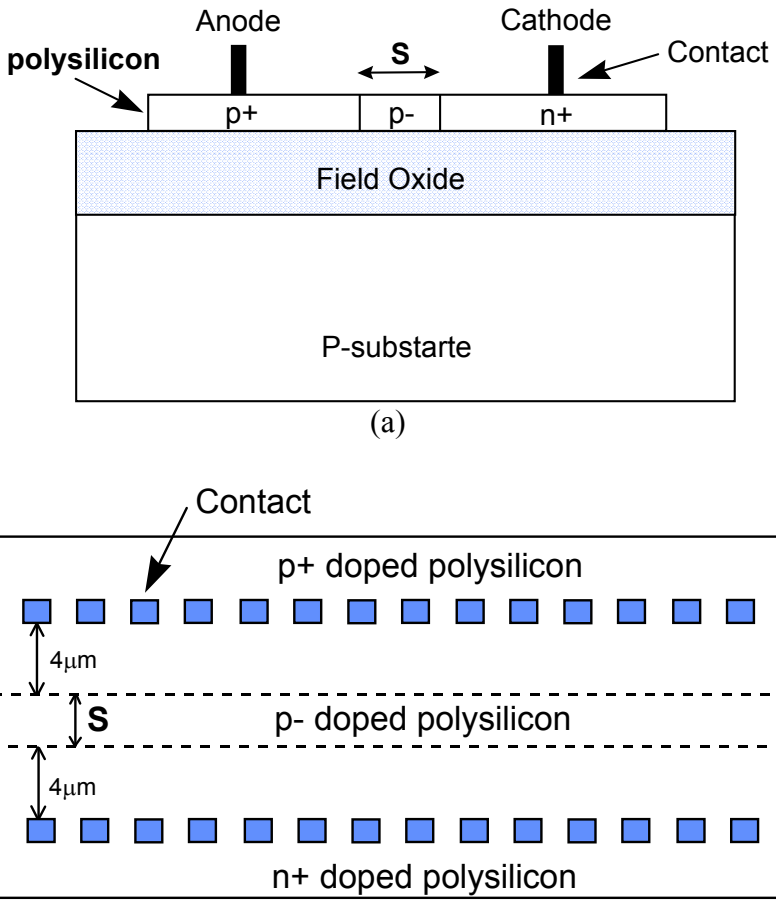


Fig. 8.13 (a) The device structure, and (b) the layout top view, of the p+ / p- / n+ polysilicon diode realized in a CMOS process.

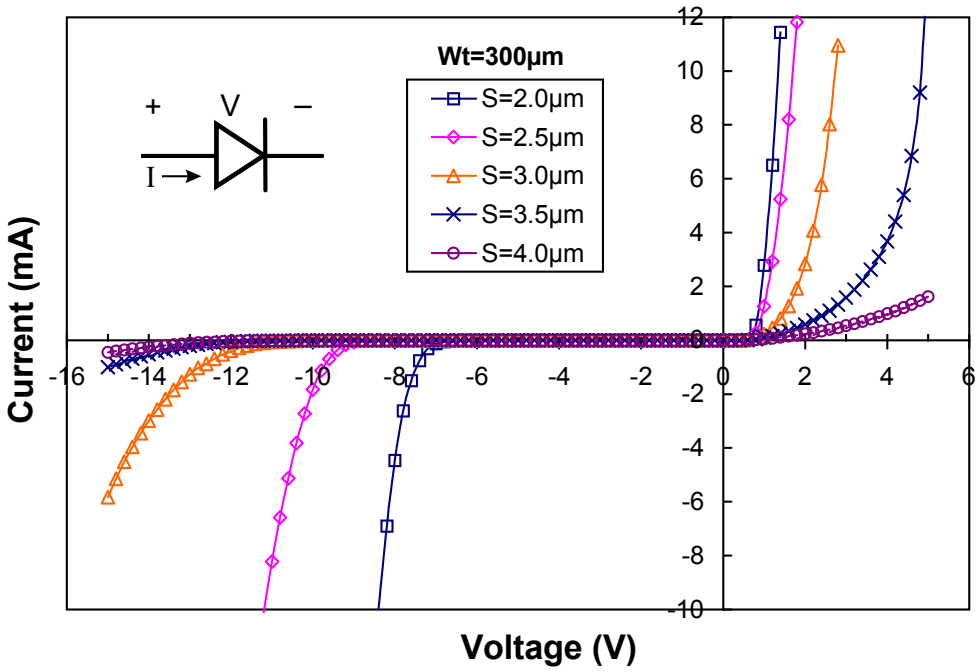
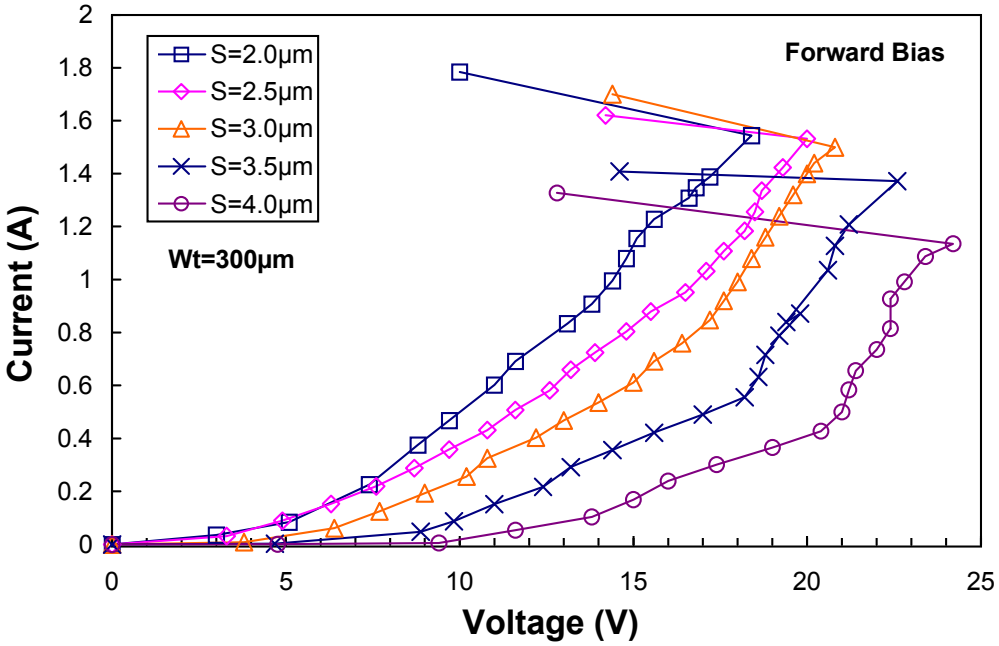
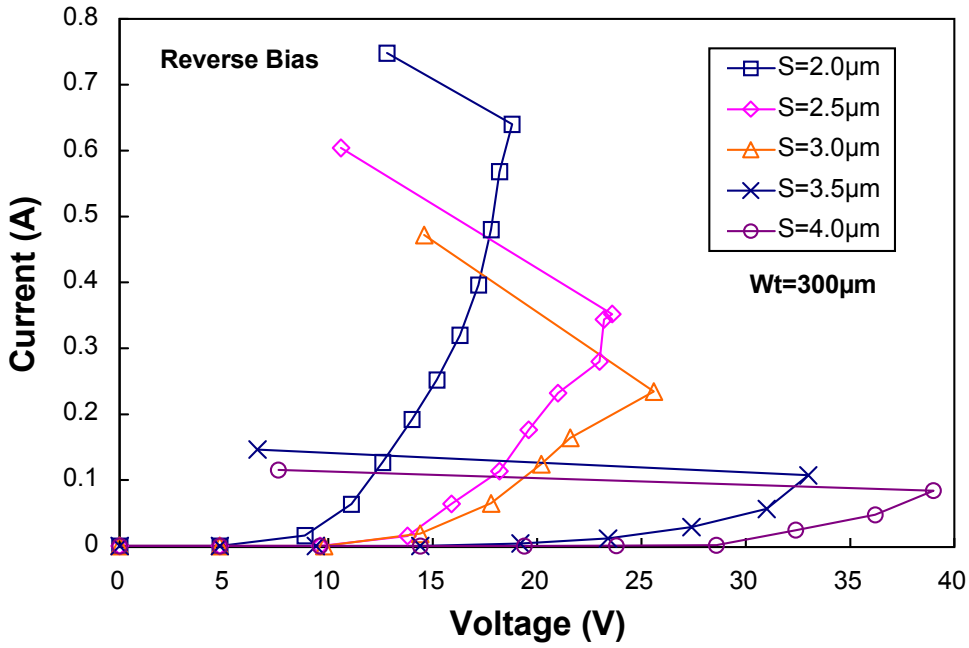


Fig. 8.14 The measured I-V curves of the p+ / n- / n+ polysilicon diodes with a fixed Wt of 300 μm but different S spacings in a CMOS process.



(a)



(b)

Fig. 8.15 The TLP-measured I-V curves of the polysilicon diodes, in (a) the forward-biased condition; and (b) the reverse-biased condition, with a fixed Wt of 300 μm but different S spacings.

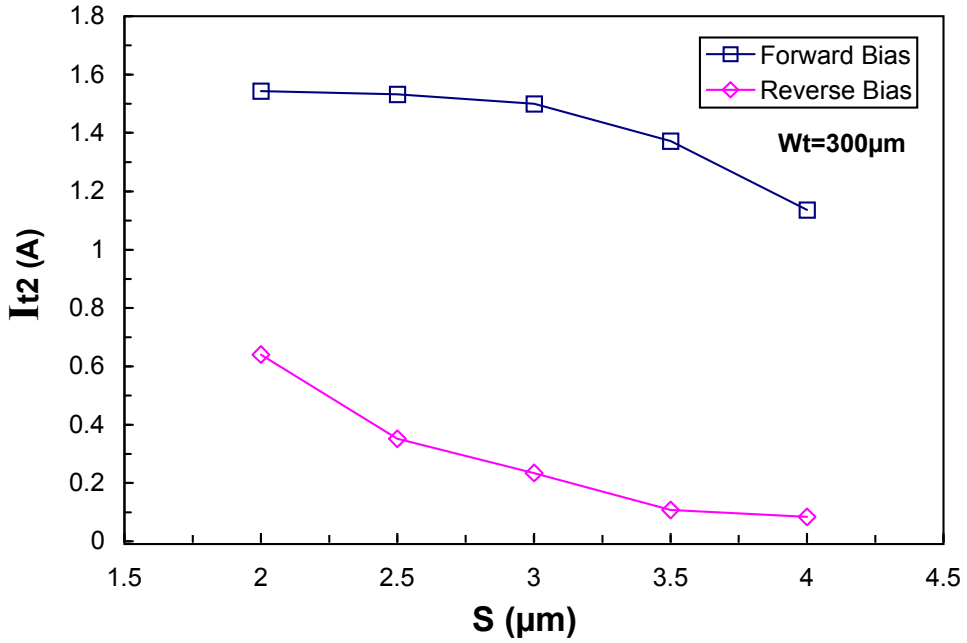
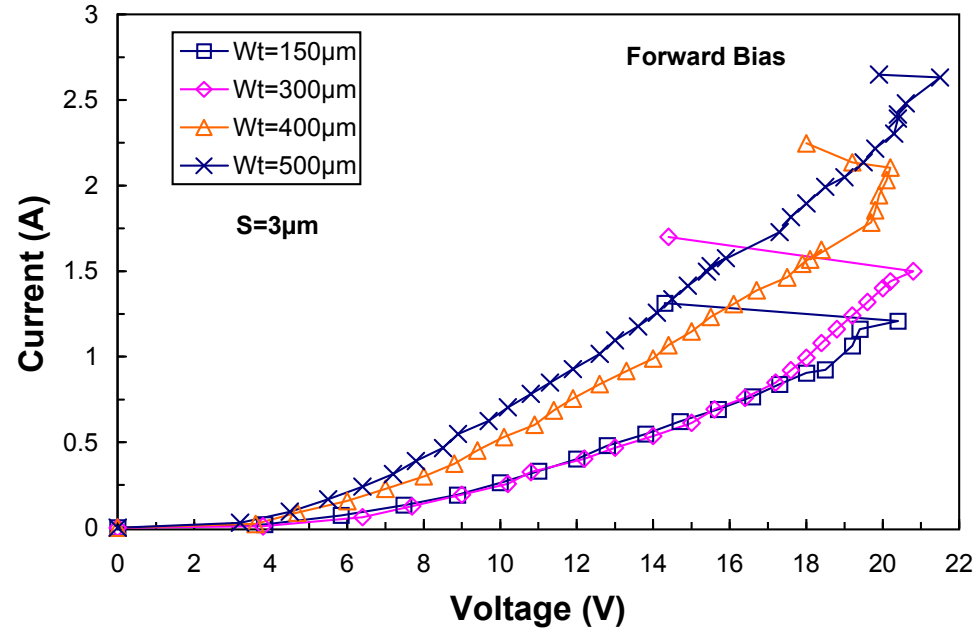
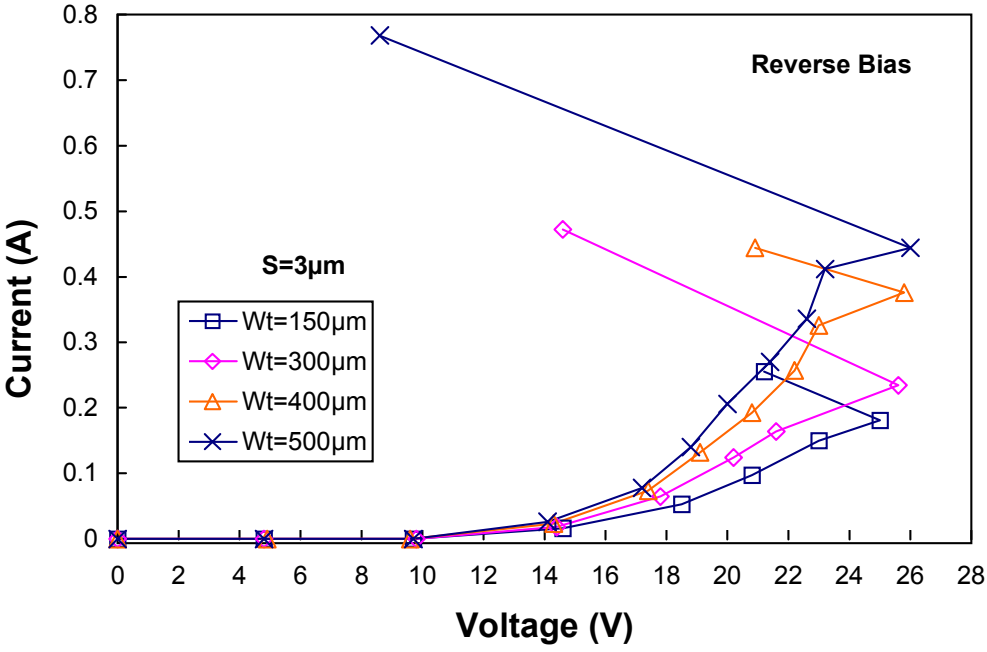


Fig. 8.16 Dependence of the TLP-measured It2 on the layout parameter S of the polysilicon diodes in both the forward- and reverse-biased conditions.



(a)



(b)

Fig. 8.17 The TLP-measured I-V curves of the polysilicon diodes, in (a) the forward-biased condition; and (b) the reverse-biased condition, with a fixed spacing S of 3 μm but different total perimeters Wt.

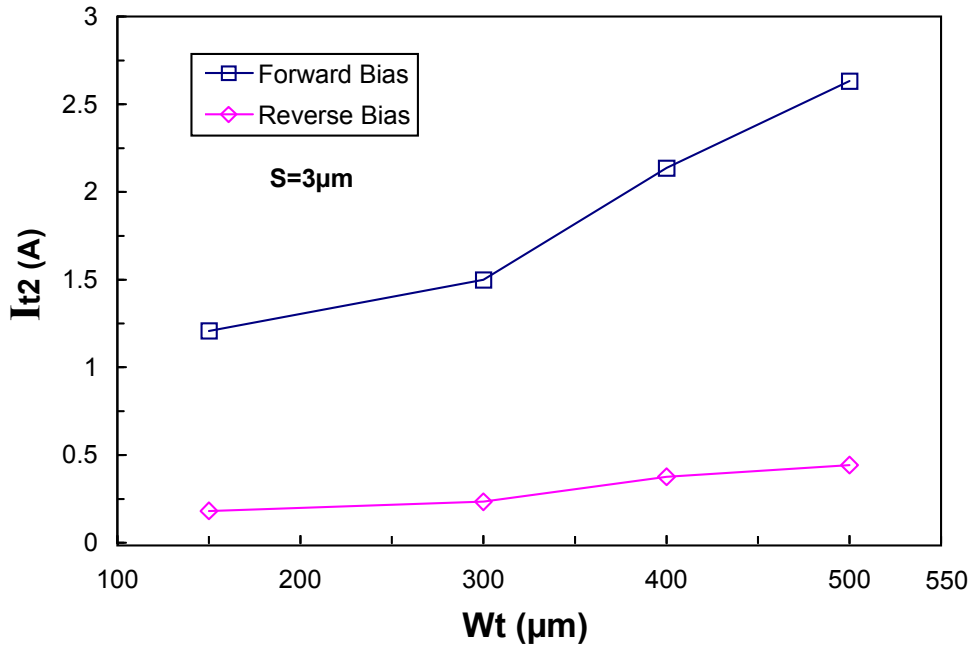
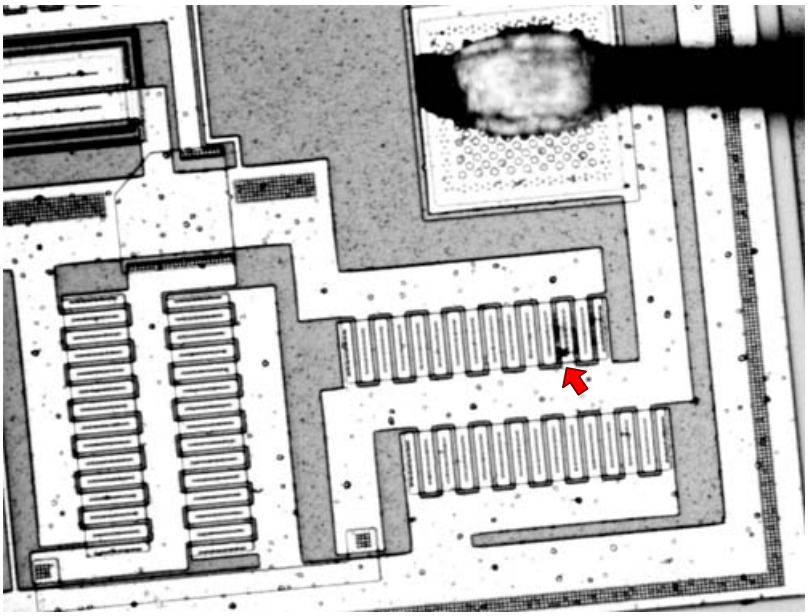
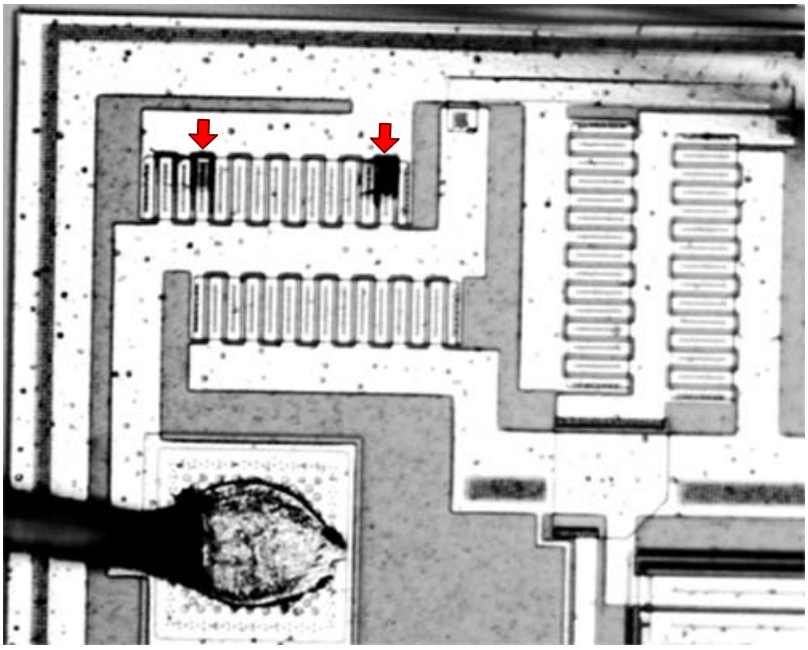


Fig. 8.18 Dependence of the TLP-measured It2 on the layout parameter Wt (total perimeter) of the polysilicon diodes in both the forward- and reverse-biased conditions.



(a)



(b)

Fig. 8.19 The pictures to show the ESD failure location (indicated by the arrows) on the smart card IC with the p- doped polysilicon diodes after the pad1 pin is zapped with a 4-kV HBM ESD stress in (a) the VSS(+), and (b) the VDD(-), ESD test conditions.

Fig. 8.20 The picture to show the ESD failure location (indicated by the arrow) on the smart card IC with the n- doped polysilicon diodes after a negative 700V CDM ESD stress.

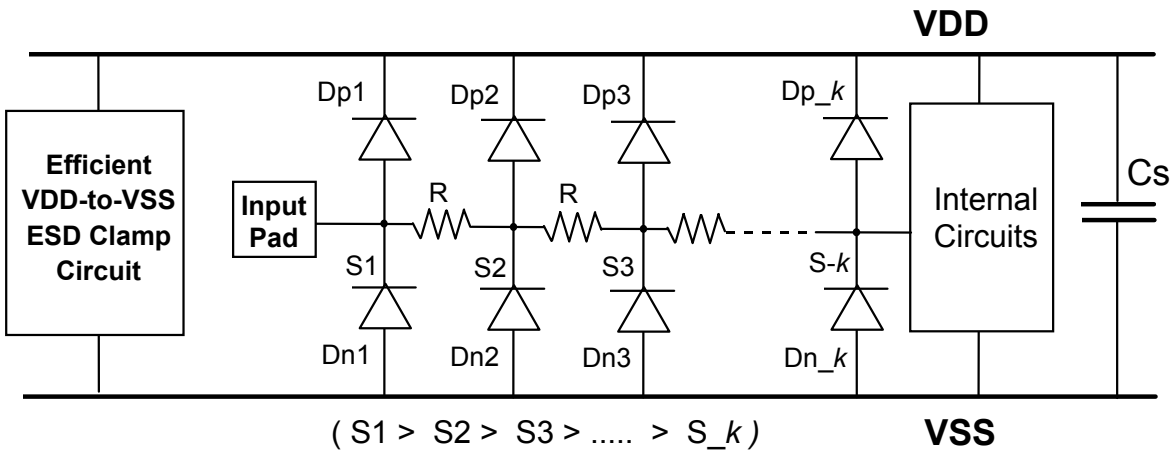


Fig. 8.21 The alternative input ESD protection design with the polysilicon diodes in a multi-stage configuration to achieve better ESD protection.

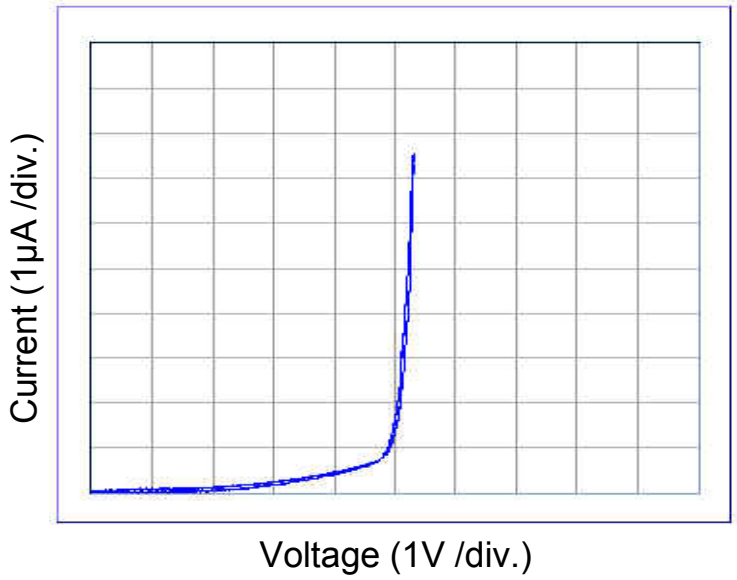


Fig. 8.22 The measured I-V curve from VDD to VSS of the new proposed VDD-to-VSS ESD clamp circuit with 8-stacked n- doped polysilicon diodes.

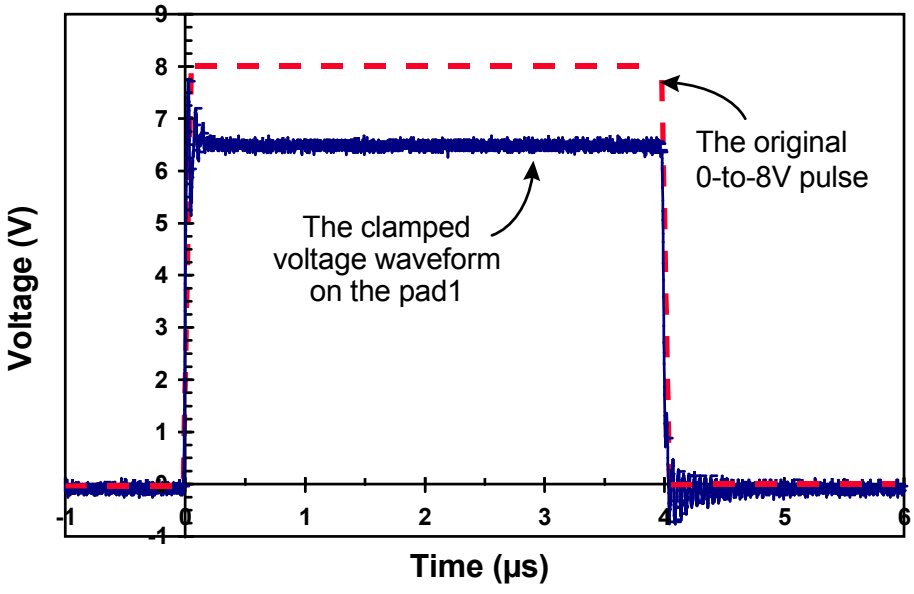
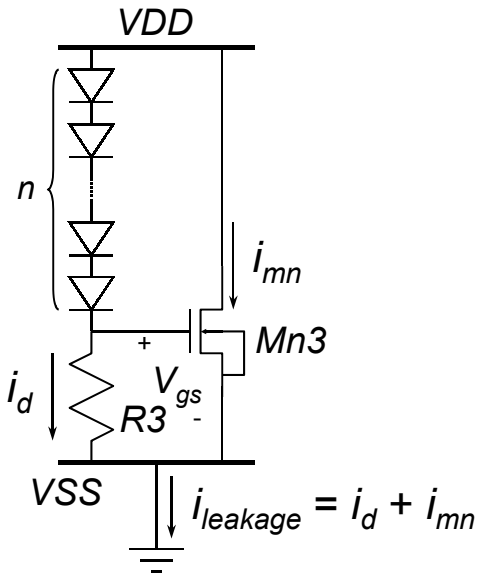
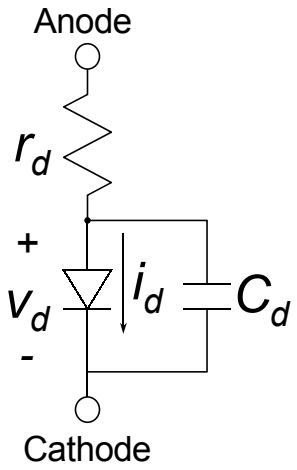


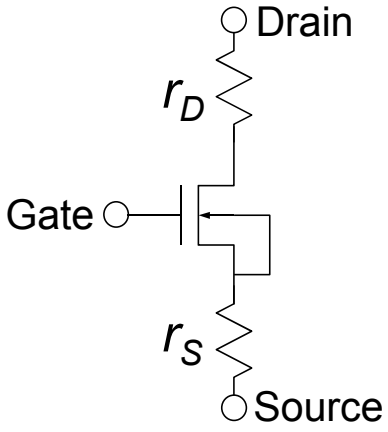
Fig. 8.23 The measured voltage waveform at the pad1 when a 0-to-8V voltage pulse is applied to the pad1 with the VSS grounded.



(a)



(b)



(c)

Fig. 8.24 (a) The ESD clamp circuit with stacked polysilicon diodes; and the equivalent circuits of (b) a diode, and (c) an NMOS, for model calculation.

CHAPTER 9

CONCLUSIONS AND FUTURE WORKS

9.1 MAIN RESULTS OF THIS THESIS

The current distribution along the NMOS device structure under ESD stress has been further explained by the energy band diagram and EMMI photographs. The dependence of layout spacings on the ESD robustness of CMOS devices in silicided CMOS process has been detailedly investigated and discussed. From the explication of energy band diagrams, the larger channel current and smaller turn-on area of parasitic lateral BJT can cause the damage of MOSFET under ESD stress. This effect causes the degradation of ESD robustness in MOSFET's. The gate-driven and substrate-triggered techniques can improve the ESD robustness of the large-dimension ESD protection devices. But, the higher gate bias can induce larger channel current and higher electric field across gate oxide to damage MOSFET. This effect causes the degradation of ESD robustness in gate-driven devices. From energy band analysis, substrate-triggered design can continually increase the turn-on area for heat dissipation. Therefore, substrate-triggered design can effectively improve ESD robustness of the ESD protection devices. So, the substrate-triggered design can be one of the most effective solutions to improve ESD robustness of CMOS devices in sub-quarter-micron CMOS technologies.

With efficient substrate-triggered ESD protection design, the input, output, and power-rail ESD protection circuits have been successfully verified in 0.18-μm, 0.25-μm, and 0.6-μm CMOS processes to protect the internal circuits of IC. With the proposed substrate-triggered designs, the ESD protection devices with smaller layout dimension can sustain higher ESD stress than the traditional gate-driven design. For the substrate-triggered output ESD protection design in a 0.18-μm CMOS process, the HBM ESD robustness of the output ESD protection circuits with ESD protection NMOS of W/L = 300μm/0.3μm can be improved from the original 0.65 kV with the traditional gate-driven design to become 3.2 kV by the proposed substrate-triggered design. The substrate-triggered input ESD protection circuit for mixed-voltage application has been realized in a 0.25-μm salicided CMOS process

without extra salicide-blocking and ESD-implantation modifications. The trigger voltage of such input ESD protection circuit with FOD is lowered from original 11.9 V to only 6.4 V to effectively protect the thinner gate oxide (50Å) of input stage in the 0.25-μm salicided CMOS process. Comparing to the traditional ESD protection gg-NMOS, the ESD levels of the proposed input ESD protection circuits with FOD and NMOS Mn2, while the "B" spacing is kept at 2 μm and the channel width is kept at 150 μm, are increased 44% and 11% per silicon area, respectively. In a 0.6-μm CMOS process, area-efficient power-rail ESD clamp circuits with four different substrate-triggered devices have been practically investigated to provide much higher ESD robustness within a smaller layout area, as compared to the traditional design with the gate-driven NMOS device. In the experimental results, the DTDB device has the best performance among these four substrate-triggered devices. With suitable design on the ESD-clamp device and the substrate-triggered technique, the layout area of the ESD clamp circuit to achieve whole-chip ESD protection can be efficiently reduced to save the silicon cost of CMOS IC's.

The discrimination between the ESD protection design methods in this thesis and prior arts is summarized in Table 9.1. The material cost, process cost, and silicon area cost are included in the "cost" of this table. There is no latchup issue in the design of high-holding-voltage LVTSCR, but the epitaxial wafer must be used in this design. So, the material cost of high-holding-voltage LVTSCR is higher than other techniques. For gate-coupled, gate-driven, and substrate-triggered techniques, some external triggered circuits must be added in the ESD protection designs to improve the turn-on uniformity of protection devices. So, the external silicon area will be increased in those designs. But the ESD protection device in substrate-triggered technique can be designed in a smaller dimension than gate-driven design. So, the cost of substrate-triggered technique is cheaper than gate-driven design. Moreover, the triggered voltage of the gate-coupled and gate-driven designs must be well controlled to avoid the degradation on the ESD level of protection devices. So, the design difficulty will be increased in the gate-coupled and gate-driven designs. In the substrate-triggered design of chapter 5, there are no silicide blocking and ESD implantation process modifications. So, the cost of this design can be more decreased than other designs. For high turn-on efficiency designs, the triggered voltage and triggered current of ESD protection circuit must be well controlled to detect the ESD signal. So, only gate-driven and substrate-triggered design can lower the triggered current and voltage of ESD protection device. From the contrast, the substrate-triggered design is the better choice for on-chip ESD

protection in sub-quarter-micron CMOS technologies.

For analog I/O ESD protection design, an ESD protection circuit with a very low and almost constant input capacitance, high ESD level, but no series resistance, has been successfully designed and verified in a 0.35-μm silicided CMOS process. The ESD test results and turn-on verifications have shown that this analog ESD protection circuit can effectively protect the analog circuits, especially the differential input stage under the pin-to-pin ESD stress condition. The design model to optimize the device dimensions and layout spacings of ESD protection devices has been clearly developed to keep the input capacitance as constant as possible in general CMOS processes. With suitable layout parameters on the input ESD clamp devices, the variation of total input capacitance of the analog ESD protection circuit can be designed below 1% while the analog input signal has an input voltage swing of 1V. With a much small and almost constant input capacitance, this analog ESD protection circuit is very suitable for current-mode, high-frequency, and high-precision circuit applications with high enough ESD reliability.

To solve the leakage current issue of traditional junction diode, the device characteristics of the new polysilicon diodes have been experimentally evaluated by process splits with different doping concentrations. The It2 of the polysilicon diodes under forward- and reverse-bias conditions and different layout parameters has been clearly investigated. A novel power-rail ESD clamp circuit with the stacked polysilicon diodes as the turn-on control circuit has been designed and analyzed in this thesis. By adjusting the number of the stack diodes in the ESD detection circuit, the turn-on efficient VDD-to-VSS ESD clamp circuit can be applied in the IC with different VDD voltage levels. The HBM ESD level of the smart card IC with the polysilicon diodes as ESD protection devices has been successfully improved up to ≥ 3kV in cooperation with the turn-on efficient power-rail ESD clamp circuit.

9.2 FUTURE WORKS

The turn-on mechanisms of CMOS device under ESD stress with gate-grounded, gate-driven, and substrate-triggered designs have been analyzed and discussed in this thesis. But, there are no simulation results for the current, temperature, and electric field distributions of those CMOS devices in this thesis because of the lack of some simulation tools and device process parameters. To enhance the evidence of the proposed turn-on mechanisms, some

physical characteristics of ESD protection devices with process parameters can be simulated to optimize the device structure for ESD protection. Moreover, the layout parameters of those CMOS device have strong effects on the ESD protection capability from the analysis of this thesis. The CAD method should be developed to check or to simulate the ESD robustness of CMOS IC before the IC is fabricated. Thus, the future work to simulate the ESD robustness of protection devices will do more effort on those physical simulation results.

Table 9.1
The discrimination between the ESD protection design methods in this thesis and prior arts.

(▲: High, ◊: Middle, ▼: Low, ○: Use, ×: Unused, ◙: Selectable, √: Yes, №: No)

	Cost	Silicide Block	Latchup Issue	Turn-on Uniformity	Turn-on Efficiency	Design Difficulty	Layout Complexity
LSCR	▼	×	√	◊	▼	▼	▼
LVTSCR	▼	◙	√	◊	▼	◊	▼
MLSCR	▼	×	√	◊	▼	◊	▼
Gate-coupled LVTSCR	◊	◙	√	▲	◊	▲	◊
High-current-triggered LVTSCR	▼	○	√	◊	▼	▲	▲
High-holding-voltage LVTSCR	▲	◙	№	◊	◊	▲	◊
MOSFET with ESD Implantation	▲	○	№	▼	◊	▼	▼
Multi-finger Type MOSFET	◊	○	№	▼	◊	▼	▼
Polygon Type MOSFET	◊	○	№	◊	◊	◊	▲
Multi-finger Type MOSFET with Butting Pickup	◊	○	№	◊	▼	▼	▼
Gate-driven Design	▲	○	№	▲	▲	▲	◊
Substrate-triggered CKT in Chapter 4	◊	○	№	▲	▲	◊	◊
Substrate-triggered CKT in Chapter 5	▼	×	№	▲	▲	◊	◊
Substrate-triggered CKT in Chapter 6	◊	○	№	▲	▲	◊	◊

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1. 1997年碩士論文"The Design and Analysis of Electrostatic Discharge Protection Devices and Circuits Using Transmission-Line-Pulsing Technique and Substrate-Triggering Technique"，獲得第十一屆*acta*論文優等獎。
2. 2001年以一篇"Design on ESD Protection Circuit with Very Low Constant Input Capacitance"論文，獲頒***IEEE ISQED*** 2001 Best Ph.D. Student Forum Award。
3. 2001年於電子月刊7月號上所著"傳輸線觸波技術在深次微米互補式金氧半積體電路之靜電放電防護的應用"一文，榮獲*電子月刊*第六屆金筆獎首獎。