國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

具有基體觸發技術之矽控整流器
及其在積體電路晶片靜電放電防護上之應用

SILICON-CONTROLLED RECTIFIER
WITH SUBSTRATE-TRIGGERED TECHNIQUE
FOR ON-CHIP ESD PROTECTION
IN CMOS INTEGRATED CIRCUITS

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中華民國　九十二年九月

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摘要

在眾多的靜電放電(Electrostatic Discharge, ESD)防護元件中[如:二極體(Diode)、矽控整流器(SCR)、雙載子電晶體(BJT)、金氧半場效電晶體(MOSFET)或者是場氧化層電晶體(Field Oxide Device, FOD)]，矽控整流器在互補式金氧半導體(CMOS)製程技術中，具有最高的靜電放電防護能力，應用在晶片上當靜電放電防護元件也有一段很長的時間。矽控整流器(SCR)基本特性是由電流觸發而導通的元件，所以當有一電流施加於矽控整流器的基體時，矽控整流器可以很快地經由正回授再生機制(Positive-Feedback Regeneration Mechanism)觸發進入閉鎖狀態，而不需透過原本的纍增崩潰機制(Avalanche Breakdown Mechanism)。本論文深入研究矽控整流器與電流觸發的基本關係，利用電流觸發的概念並進一步設計出相關的控制電路，並實際應用在積體電路晶片上之靜電放電防護電路。

在本論文中，首先提出具有互補電路型式的基體觸發矽控整流器，用來排放焊墊到 VDD 或 VSS 電源腳位的靜電放電電流。此新型的互補式基體觸發矽控整流器具有以下優點: 可調整的切換電壓(Switching Voltage)、低持有電壓(Holding Voltage)、較快的導通速度(Turn-on Speed)、以及製程步驟完全相容於一般互補式金氧半導體的製程，不需增加額外的光罩如遮蔽金屬矽化物光罩(Silicide-Blocking Mask)和離子佈植(ESD Implantation)光

罩。在 0.25 微米全金屬矽化的互補式金氧半導體製程中，當基體觸發電流由零增加到 8 mA 時，基體觸發矽控整流器的切換電壓會由原本高達 22 V 的電壓準位降到只有 1.85 V，非常接近其持有電壓(約 1.35 V)。而且，當觸發脈衝電壓的準位由 1.5 V 增加到 4 V 時，基體觸發矽控整流器的導通時間(Turn-on Time)可由 27.4 ns 縮短到只有 7.8 ns，具有明顯增進導通速度的效果。

基體觸發矽控整流器在本論文實際製作中具有的主動面積(Active Area)只有 20 微米x20 微米的大小，這麼小的佈局面積使得基體觸發矽控整流器在靜電放電防護電路設計中可以被堆疊以避免暫態過程所引發的閉鎖效應(Transient-Induced Latchup Issue)。對於 VDD 為 2.5 V 的 0.25 微米全金屬矽化的互補式金氧半積體電路應用而言，具有兩個基體觸發矽控整流器堆疊結構的靜電放電防護電路，其箝制電壓約為 3.2 V，可免於閉鎖效應的危險，且仍可承受大於 8 kV 的人體放電模式(Human-Body-Model, HBM)及 700 V 的機械放電模式(Machine-Model, MM)的靜電放電耐受能力。此外，基體觸發矽控整流器的整體持有電壓也可藉由疊接二極體串來達到線性的增加。由互補式基體觸發矽控整流器搭配兩個二極體所設計的靜電放電防護電路，不具有閉鎖效應的疑慮，並可應用在輸出輸入焊墊(I/O Pads) 及 VDD/VSS 電源焊墊使用之靜電放電防護電路，在 0.25 微米全金屬矽化的互補式金氧半導體製程中也實際被製作，在很小的佈局面積下具有 7.25 kV 的人體放電模式及 500 V 的機械放電模式的靜電放電耐受能力。

導通效率一直是矽控整流器作為晶片上靜電放電防護電路的主要隱憂，特別是在未來奈米製程中具有超薄閘氧化層的互補式金氧半導體製程。也由於矽控整流器的元件結構中，包含了一橫向的 NPN 及一縱向的 PNP 雙載子電晶體，於是本論文另外提出了創新的雙觸發技術，同時觸發 NPN 和 PNP 電晶體，更能增快矽控整流器的導通速度，用作於晶片上的靜電放電防護電路，能更有效地保護在未來奈米互補式金氧半導製程中的超薄閘氧化層。從 0.25 微米互補式金氧半製程中的實驗結果得知，具有 20 微米x20 微米佈局面積的雙觸發矽控整流器，其切換電壓和導通時間均會

因雙觸發技術而更有效地降低。雙觸發矽控整流器的切換電壓，在 N 井觸發電流為-3 mA 之下，會進一步地由 21 V 降低至 1.5 V，當基體觸發電流由 0 mA 增加至 3 mA 時。在 P 型觸發端施加固定的一 1.5 V 正的脈衝電壓，且施加在 N 型觸發端負電壓脈衝的絕對脈衝高度由 0 V 增加到 5 V 的條件下，雙觸發矽控整流器的導通時間會由 37.6 ns 大幅縮短至 11.8 ns。

本論文另外也提出了一種帶有基體觸發技術和假閘極阻隔結構的矽控整流器用來改善矽控整流器的導通速度，用於晶片上的靜電放電防護電路，可為較薄的閘氧化層提供更有效的防護。這種具有假閘極結構的矽控整流器其製程是完全相容於一般互補式金氧半導體的製程，不需增加額外的光罩及製程步驟。從閘氧化層厚度為 50 埃的 0.25 微米互補式金氧半製程中的實驗結果得知，和一般具有淺溝槽隔離(Shallow Trench Isolation, STI)結構的矽控整流器相比，具有假閘極結構的基體觸發矽控整流器其切換電壓、導通速度、導通電阻(Turn-on Resistance)和元件充電放電模式(Charged-Device-Model, CDM)的靜電放電耐受能力均有顯著的改善。當施加於 P 型觸發端的基體觸發電流由 0 mA 增加至 6 mA 時，具有淺溝槽隔離結構的矽控整流器其切換電壓會由 22 V 降低至 7 V，但具有假閘極結構的矽控整流器其切換電壓卻會由 18 V 大大地降低至 3 V。

為了能快速地將靜電放電能量排放及有效率地保護超薄閘氧化層，本論文另外提出了一種新型的原生性 N 型金氧半電晶體觸發矽控整流器(Native-NMOS-Triggered SCR, NANSCR)，作為晶片上的靜電放電防護。在靜電放電發生的情況下，原生性 N 型金氧半電晶體(Native NMOS)是一已導通的元件，故可以快速地引導靜電放電電流去觸發矽控整流器進入閉鎖狀態，最後，靜電放電電流便可透過導通的原生性 N 型金氧半電晶體觸發矽控整流器排放掉。從供應電壓為 1.2 V 的 0.13 微米互補式金氧半製程中的實驗結果得知，和傳統的低壓觸發矽控整流器(Low-Voltage Triggering SCR, LVTSCR)相比，原生性 N 型金氧半電晶體觸發矽控整流器的切換電壓、持有電壓、導通電阻、導通速度和元件充電放電模式的靜電放電耐受能力均有明顯的改善，更能保護超薄閘氧化層對抗靜電放電的應力(ESD Stress)。

所提出的原生性 N 型金氧半電晶體觸發矽控整流器可被運用在輸入、輸出和電源線間的靜電放電防護電路且可免於閉鎖效應的危險。利用所提出的原生性 N 型金氧半電晶體觸發矽控整流器設計而成的全晶片靜電放電防護架構(Whole-Chip ESD Protection Scheme)，也已經藉有針腳對針腳(Pin-to-Pin) 靜電放電測試的數據去驗證其保護效能。對於具有多電源準位的超大型互補式金氧半積體電路而言，所提出具有原生性 N 型金氧半電晶體觸發矽控整流器和靜電放電路徑(ESD Path)的全晶片靜電放電防護架構，是一種可以快速地排放所有靜電放電應力和有效保護內部電路的創新解決方案。

在本博士論文中，共計有五種利用基體觸發技術所設計出的矽控整流器元件，每一種元件之效能均已在實際晶片上成功驗證，並有相對應的國際期刊論文發表。本論文所研發之基體觸發矽控整流器及其相關電路設計，非常適合應用在深次微米以及未來奈米半導體製程所製作的積體電路晶片上，以有效提昇積體電路對靜電放電的防護能力。

SILICON-CONTROLLED RECTIFIER WITH SUBSTRATE-TRIGGERED TECHNIQUE FOR ON-CHIP ESD PROTECTION IN CMOS INTEGRATED CIRCUITS

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ABSTRACT

With the highest electrostatic discharge (ESD) robustness in the smallest layout area, the silicon-controlled rectifier (SCR) device had been used in the on-chip ESD protection circuits for a long time among various ESD protection devices (such as the diode, SCR, BJT, MOS, or field oxide device) in CMOS technologies. The turn-on mechanism of a SCR device is essentially a current triggering event. While a current is applied to the base or substrate of the SCR device, it can be quickly triggered on into its latching state through the positive-feedback regeneration mechanism without involving the original avalanche breakdown mechanism. In this thesis, the dependence of the device characteristics of SCR on the triggering current is investigated in details. Then, based on the current triggering mechanism of SCR device, the corresponding ESD detection circuits are proposed to generate the triggering currents. Finally, the on-chip ESD protection circuit with the SCR devices and current-triggering circuits are realized to protect the CMOS ICs.

First, a complementary circuit style with the substrate-triggered SCR (STSCR) devices is designed to discharge both of the pad-to-VSS and pad-to-VDD ESD stresses. The novel complementary STSCR devices have the advantages of controllable switching voltage, lower holding voltage, faster turn-on speed, and fully process-compatible to general CMOS processes without extra process modification such as the silicide-blocking mask and ESD

implantation. The switching voltage of the fabricated STSCR device can be reduced from ~22 to only 1.85 V, which almost equals to the holding voltage (~1.35 V) of the STSCR, when the substrate-triggered current is increased to 8 mA in a 0.25-μm fully salicided CMOS process. The turn-on time of the STSCR device can be reduced from 27.4 to 7.8 ns, while the pulse height of the triggering voltage pulse is increased from 1.5 to 4 V.

The STSCR device with a small active area of only 20 μm×20 μm can be stacked in the ESD protection circuits to avoid the transient-induced latch-up issue. For the IC application with VDD of 2.5 V, the ESD protection circuit designed with two STSCR devices in stacked configuration has a clamp voltage of ~3.2 V, free from latchup issue, and the human-body-model (HBM) (machine-model (MM)) ESD level of > 8 kV (700 V) in a 0.25-μm fully salicided CMOS process. In addition, the total holding voltage of the STSCR device can be linearly increased by adding the stacked diode string. The on-chip latchup-free ESD protection circuits designed with the proposed complementary STSCR devices and two stacked diode string for the I/O pads and power pad have been successfully verified in a 0.25-μm salicided CMOS process with the HBM (MM) ESD level of ~7.25 kV (500 V) in a small layout area.

Turn-on efficiency is the main concern for SCR devices used as on-chip ESD protection circuit, especially in future nanoscale CMOS processes with ultra-thinn gate oxide. The SCR device consists of a lateral NPN and a vertical PNP bipolar transistors, which is inherent in the CMOS processes. In this thesis, a novel double-triggered technique, used to synchronously trigger the NPN and PNP transistors in the SCR structure, is also proposed to further improve the turn-on speed of SCR devices for using in on-chip ESD protection circuit to effectively protect the much thinner gate oxide in nanoscale CMOS processes. From the experimental results in a 0.25-μm salicided CMOS process, the switching voltage and turn-on time of such double-triggered SCR (DTSCR) device, which is drawn as 20 μm×20 μm, has been confirmed to be reduced more efficiently by this double-triggered technique. The switching voltage of DTSCR under the N-well triggered current of -3 mA is further reduced from ~21 to ~1.5 V, when the substrate-triggered current is increased from 0 to 2 mA. Under the positive voltage pulse of 1.5 V at p-trigger node, the turn-on time of DTSCR can be reduced from 37.6 to 11.8 ns, while the absolute pulse height of negative voltage pulse applied to the n-trigger node is increased from 0 to 5 V.

A novel dummy-gate-blocking SCR device with substrate-triggered technique is also

proposed to improve the turn-on speed of SCR device for using in the on-chip ESD protection circuit to effectively protect the much thinner gate oxide. The fabrication of the proposed SCR device with dummy-gate structure is fully process-compatible to general CMOS process, without using extra mask layer or increasing process step. From the experimental results in a 0.25-μm CMOS process with the gate-oxide thickness of ~50 Å, the switching voltage, turn-on speed, turn-on resistance, and charged-device-model (CDM) ESD levels of the SCR device with dummy-gate structure have been greatly improved, as compared to the normal SCR with shallow trench isolation (STI) structure. When the substrate-triggered current applied at the p-trigger node is increased from 0 to 6 mA, the switching voltage of STSCR with STI is reduced from ~22 to ~7 V, whereas that of STSCR with dummy-gate structure is greatly reduced from ~18 to ~3 V.

In order to quickly discharge the ESD energy and to efficiently protect the ultra-thin gate oxide, a novel native-NMOS-triggered SCR (NANSCR) is proposed for on-chip ESD protection. Native NMOS is an already-on device under ESD events, so it can quickly conduct some ESD current to trigger SCR into latching state. Then, ESD current can be quickly discharged through the turned-on NANSCR device. From the experimental results in a 0.13-μm CMOS process with voltage supply of 1.2 V, the switching voltage, holding voltage, turn-on resistance, turn-on speed, and CDM ESD level of NANSCR can be greatly improved to protect the ultra-thin gate oxide against ESD stresses, as compared with the traditional low-voltage triggering SCR (LVTSCR). The proposed NANSCR can be designed for the input, output, and power-rail ESD protection circuits without latchup danger. A new whole-chip ESD protection scheme realized with the proposed NANSCR devices is also demonstrated with the consideration of pin-to-pin ESD zapping. For ultra large-scale CMOS ICs with multiple power pins, the proposed whole-chip ESD protection scheme with NANSCR and ESD path is an overall solution to quickly discharge all kinds of ESD stresses and to provide efficient protection for the internal circuits.

In summary, there are totally 5 different designs on substrate-triggered SCR devices developed in this thesis. Each of the substrate-triggered SCR devices and its corresponding circuit for ESD protection have been successfully verified in the testchips and also published in the International Journals or Transactions. The developed substrate-triggered SCR devices are highly useful for on-chip ESD protection in the sub-quarter-micron CMOS integrated circuits without process modification.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Electrostatic discharge (ESD) phenomenon originates from the transfer of electrostatic charges between two objects with different electrical potentials, which results in damage to integrated circuits (ICs) due to large energy dissipation in an extremely short time less than 150 ns. ESD failure will become more and more serious reliability concern in nanoscale CMOS IC products. Common ESD failures are catastrophic, leading to immediate malfunction of IC chips caused by either thermal breakdown in silicon and/or metal interconnects due to high-current transient, or dielectric breakdown in gate oxide due to high-voltage overstress [1]. The ESD specifications of commercial IC products are generally required to be higher than 2 kV in human-body-model (HBM) [2] ESD stress and 200 V in machine-model (MM) [3] ESD stress. Therefore, in order to provide efficient ESD protection for CMOS ICs against unexpected ESD damages in the internal circuits of CMOS ICs [4]-[11], the on-chip ESD protection circuits have to be designed and placed around the input, output, and power pads to clamp the overstress voltage across the internal circuits, and to provide a low impendence path to discharge the ESD current of several Ampere to ground. The locations of the ESD protection circuits to achieve whole-chip ESD protection for CMOS ICs are illustrated in Fig. 1.1.

Due to the low holding voltage (Vh, about ~1.5 V in general CMOS processes) of silicon controlled rectifier (SCR) device [12], [13], the power dissipation (power $\cong I_{ESD} \times Vh$) located on the SCR device during ESD stress is significantly less than that located on other ESD protection devices, such as the diode, MOS, BJT, or field-oxide device. The SCR device can sustain a much higher ESD level within a smaller layout area in CMOS ICs, so it had been used to protect the internal circuits against ESD damage for a long time. But, the SCR device still has a higher switching voltage (i.e., trigger voltage, ~22 V) in the sub-quarter-micron CMOS technology, which is generally greater than the gate-oxide

breakdown voltage of the input stages. Furthermore, the gate oxide thickness, its time-to-breakdown (t_{BD}), or charge-to-breakdown (Q_{BD}) will also be decreased with the shrinkage of CMOS technologies. So, it is imperative to reduce the switching voltage of SCR and to enhance the turn-on speed of SCR for efficiently protecting the ultra-thin gate oxide from latent damage or rupture [14], especially against the fast charged-device-model (CDM) [15] ESD events. Therefore, to provide more effective on-chip ESD protection, the modified lateral SCR (MLSCR) [16] and the low-voltage triggering SCR (LVTSCR) [17], [18] had been invented to reduce the switching voltage of SCR device. Moreover, some advanced trigger-assist circuit techniques had been also reported to reduce the switching voltage and to enhance the turn-on speed of SCR device, such as the gate-coupled technique [19], the hot-carrier triggered technique [20], the GGNMOS-triggered technique [21], [22], the substrate-triggered technique [23]-[26], double-triggered technique [27], native-NMOS-trigger technique [28], etc. For mixed-voltage I/O buffer, the stacked-NMOS triggered SCR was invented to improved the ESD level of stacked NMOS [29], [30].

The review of SCR-based devices for on-chip ESD protection is investigated and compared in this chapter [31]. In addition, the solutions to avoid the transient-induced latchup issue [32] of SCR-based devices in CMOS IC products with maximum voltage supply greater than 1.5 V are also discussed. However, such latchup issue will vanish certainly when the maximum voltage supply of IC products is smaller than the holding voltage of SCR devices. For example, a single SCR with holding voltage of ~1.6 V can be safely used as ESD protection without latchup danger in a 0.13-μm CMOS process with maximum voltage supply of 1.2 V.

1.2 TURN-ON MECHANISM OF SCR DEVICE

The equivalent circuit schematic of a SCR device is shown in Fig. 1.2(a). SCR device consists of a lateral NPN and a vertical PNP bipolar transistors and forms a 2-terminal and 4-layer PNPN (P+/N-well/P-well/N+) structure, which is inherent in the CMOS processes. The switching voltage of the SCR device is dominated by the avalanche breakdown voltage of N-well/P-well junction, which is about ~22 V in a 0.25-μm CMOS process, or ~18 V in a 0.13-μm CMOS process. When a positive voltage applied on the anode of SCR is greater

than the breakdown voltage and its cathode is relatively grounded, for example, the hole and electron current will be generated through the avalanche breakdown mechanism [33], [34]. The hole current will flow through the P-well to P+ diffusion connected to ground, whereas the electron current will flow through the N-well to N+ diffusion connected to the anode of SCR. As long as the voltage drop across the P-well resistor (Rpwell) (N-well resistor (Rnwell)) is greater than 0.7 V, the NPN (PNP) transistor will be turned on to inject the electron (hole) current to further bias the PNP (NPN) transistor and initiates the SCR latching action. Finally, the SCR will be successfully triggered on into its latching state to discharge ESD current through the positive-feedback regenerative mechanism [35], [36].

The DC I-V characteristic of SCR device is shown in Fig. 1.2(b). Once the SCR is triggered on, the required holding current to keep the NPN and PNP transistors on can be generated through the positive-feedback regenerative mechanism of latchup without involving the avalanche breakdown mechanism. So, the holding voltage (Vh) of SCR can be reduced to a lower voltage level of ~1.5 V, typically. When a negative voltage is applied on the anode terminal of SCR, the parasitic diode (N-well/P-well junction) inherent in SCR structure will be forward biased to clamp the negative voltage at a lower voltage level of ~-1 V (cut-in voltage of a diode). Whatever the ESD energy is positive or negative, the SCR device can clamp ESD overstresses to a lower voltage level, so the SCR device can sustain the highest ESD robustness within a smaller layout area in CMOS ICs.

1.3 SCR-BASED DEVICES FOR CMOS ON-CHIP ESD PROTECTION

1.3.1 Lateral SCR (LSCR) [12], [13]

The lateral SCR (LSCR) device was used as an effective input ESD protection element in CMOS ICs. The device structure of the LSCR is illustrated in Fig. 1.3(a), and the corresponding I-V characteristic of the LSCR in a 0.25-μm CMOS process is shown in Fig. 1.3(b). The example of the LSCR device in the input ESD protection circuit is shown in Fig. 1.3(c). In some applications, the N-well of LSCR is connected to the input pad, but not to VDD, to eliminate the forward-bias diode from the pad to VDD. The LSCR has the higher switching voltage (~22 V) in a 0.25-μm CMOS process, which is generally greater than the

gate-oxide breakdown voltage of the input stages. Therefore, the SCR device needs the additional secondary protection circuit (the series resistor and the gate-grounded NMOS, GGNMOS, in Fig. 1.3(c)) to perform the overall ESD protection function to protect the input stages. The secondary protection circuit has to sustain the ESD stress before the LSCR is triggered on to discharge the ESD current on the input pad. The relationship among the LSCR's switching voltage (Vt1_SCR), series resistor (R), secondary breakdown voltage of GGNMOS (Vt2_GGNMOS), and secondary breakdown current of GGNMOS (It2_GGNMOS) can be approximated as following:

$$Vt1\_SCR < (It2\_GGNMOS \times R) + Vt2\_GGNMOS \quad (1.1)$$

Because the LSCR is hard to be triggered on in time, the secondary ESD protection circuit was designed with larger-sized GGNMOS and series resistor to protect itself from ESD damage, and to make the LSCR be triggered on successfully. This secondary ESD protection circuit with large device dimensions often occupies more layout area. If the secondary protection circuit was not properly designed, it had caused the fail window in the ESD test scanning from the low voltage to high voltage [37]. Such input ESD protection circuit was found to pass the ESD stress with low voltage level or high voltage level, but it was failed when the ESD stress with a middle voltage level [37]. So, the design of the secondary protection circuit with the LSCR for the overall input ESD protection circuit is somewhat critical in the CMOS ICs.

1.3.2 Modified Lateral SCR (MLSCR) [16]

In order to reduce the switching voltage of LSCR device to provide more effective ESD protection for the internal circuits, the modified lateral SCR (MLSCR) was invented. The device structure of the MLSCR is illustrated in Fig. 1.4(a), and the corresponding I-V characteristic of the MLSCR in a 0.25-μm CMOS process is shown in Fig. 1.4(b). The example of using the MLSCR device as the input ESD protection circuit is shown in Fig. 1.4(c). In some applications, the N-well of MLSCR is connected to the input pad. The MLSCR is made by adding an N+ diffusion across the N-well/P-well junction to lower the avalanche breakdown voltage of N-well/P-well junction. However, the switching voltage (~12 V) of the MLSCR is still greater than the gate-oxide breakdown voltage of input stages in the same process. Therefore, the MLSCR has to be still cooperated with the secondary

protection circuit to perform the overall ESD protection functions to the input stages. Due to the lower switching voltage (~12 V) in the MLSCR in the 0.25-μm CMOS process, the secondary protection circuit could have smaller device dimensions to save total layout area. Unsuitable design or layout on the secondary protection circuit still causes the ESD damage located on the secondary protection circuit rather than the MLSCR device. For output stage, the two-stage ESD protective configuration will cause some signal delay under normal circuit operating conditions, so the LSCR and MLSCR devices are seldom used in the output ESD protection designs.

1.3.3 Low-Voltage Triggering SCR (LVTSCR) [17], [18]

To more effectively protect the input stages and even the output stages, the low-voltage triggering SCR (LVTSCR) had been invented. The device structure of the LVTSCR is illustrated in Fig. 1.5(a), and the corresponding I-V characteristic of the LVTSCR in a 0.25-μm CMOS process is shown in Fig. 1.5(b). The example of using the LVTSCR device as the input ESD protection circuit is shown in Fig. 1.5(c). In some applications, the N-well of LVTSCR is connected to the input pad. The switching voltage of the LVTSCR (~7 V) is equivalent to the drain breakdown or punchthrough voltage of the short-channel NMOS device, which is inserted into the LSCR structure, rather than the original switching voltage of LSCR device (~22 V). With such a low switching voltage, the LVTSCR can provide effective ESD protection for the input or output stages of CMOS ICs without secondary ESD protection circuit. Therefore, the total layout area of the ESD protection circuits with the LVTSCR can be significantly saved. Furthermore, to protect both PMOS and NMOS in the input or output stage of CMOS ICs, the complementary-LVTSCR structure [18] had been invented to provide the better ESD protection.

1.3.4 Gate-Coupled LVTSCR [19]

To effective protect the ultra-thin gate oxide in deep-submicron CMOS process, the gate-coupling technique was applied to further reduce the switching voltage of the LVTSCR without involving avalanche breakdown mechanism. The ESD protection circuit for input or output pad with the complementary gate-coupled LVTSCR devices (NMOS-triggered LSCR (NTLSCR) and PMOS-triggered LSCR (PTLSCR)) is shown in Fig. 1.6(a). The device

structure of the complementary gate-coupled NTLSCR / PTLSCR is illustrated in Fig. 1.6(b), and the I-V characteristics of the gate-coupled NTLSCR in a 0.25-μm CMOS process is shown in Fig. 1.6(c). The dependence of the switching voltage of SCR device on the gate-bias voltage of the NTLSCR device is shown in Fig. 1.6(d). The capacitances (Cn and Cp) in Fig. 1.6(a) must be designed at some suitable value, where the coupled voltage under normal circuit operating conditions is smaller than the threshold voltage of NMOS / PMOS, but greater than the threshold voltage of NMOS / PMOS under ESD zapping conditions [38]. The switching voltage of the gate-coupled NTLSCR (PTLSCR) can be adjusted with the coupled voltage on the gate of the short-channel NMOS (PMOS) in the SCR device structure. The higher coupled voltage on the gate of the short-channel NMOS / PMOS in the NTLSCR / PTLSCR leads the lower switching voltage of NTLSCR / PTLSCR. Therefore, the gate-coupled NTLSCR / PTLSCR devices can quickly discharge ESD current to more effectively protect the ultra-thin gate oxide of the input or output stages.

1.3.5 Hot-Carrier Triggered SCR (HCTSCR) [20]

The power-rail ESD clamp protection circuit with hot-carrier triggered SCR (HCTSCR) is shown in Fig. 1.7(a). The device structures of primary protection devices including the SCR and trigger NMOS (M1) are shown in Fig. 1.7(b). The triggering mechanism of HCTSCR is initiated by the substrate hole current generated from the hot carrier effect of M1 during an ESD event. To ensure the proper operation of HCTSCR, M1 the must be active to provide sufficient substrate current to trigger on the SCR before other devices connected to VDD are damaged by ESD energy. The switching voltage of HCTSCR is dependent on the substrate hole current, which is the function of gate length, gate voltage, and drain voltage of the M1 [39]. The smaller gate length of M1 results in the lower switching voltage of HCTSCR. The gate voltage coupled through the capacitor (M2) has to be carefully designed to gain the peak substrate current. The device dimensions of M2 and M3 have to be optimized to ensure that the gate voltage of M1 is greater than its threshold voltage to trigger the HCTSCR on during ESD stresses. In addition, a double guardring has to be used around the perimeter of HCTSCR to prevent the SCR from being accidentally triggered on by the current injected from the exterior. With a SCR as the power-rail ESD clamp circuit, it can effectively clamp the ESD overstress voltage to avoid ESD damage on internal circuits.

However, this SCR in power-rail ESD clamp circuit could be triggered on by transient-induced latchup [32], when IC is under normal operating conditions. This will cause serious latchup failure on the CMOS IC, if the holding voltage of SCR device is smaller than the VDD voltage level.

1.3.6 Grounded-Gate NMOS Triggered SCR (GGSCR) [21], [22]

The grounded-gate NMOS triggered SCR (GGSCR) is another choice for on-chip ESD protection circuit. A NMOS transistor, which resembles a GGNMOS configuration, is used as an external trigger device to trigger on the GGSCR. In contrast to the LVTSCR, the drain of the external trigger NMOS in GGSCR is directly coupled to the pad and its gate and source are coupled into the P-substrate (the base of NPN). The example of using the GGSCR device as the input ESD protection circuit is shown in Fig. 1.8(a). The layout top view of the GGSCR is illustrated in Fig. 1.8(b) [22]. When an ESD zapping is applied to the I/O pad in Fig. 1.8(a), the external trigger NMOS will enter avalanche breakdown first to inject the triggering current into the P-substrate and poly resistor. As long as the base voltage of NPN is greater than 0.7 V, the GGSCR will be triggered on. The poly resistor in Fig. 1.8(b) allows to control the triggering and holding current and to prevent the false trigger of GGSCR. From the experimental results, the GGSCR, designed with a shorter anode-to-cathode spacing, will have the lower holding voltage, higher It2, better dV/dt triggering ability, and faster turn-on speed than those of LVTSCR with a longer anode-to-cathode spacing.

1.3.7 Substrate-Triggered SCR (STSCR) [23]-[26]

The turn-on mechanism of an SCR device is essentially a current triggering event. SCR can be quickly triggered on into its latching state, while a current is applied to its base or substrate. With the substrate-triggered technique, the p-type substrate-triggered SCR (P_STSCR) and n-type substrate-triggered SCR (N_STSCR) devices for ESD protection are proposed and investigated in Chapters 2 and 3 in this thesis. Furthermore, the STSCR device with dummy-gate structure to further reduce the switching voltage and to improve the turn-on speed of STSCR [40]-[42] is discussed in Chapter 5 in this thesis.

1.3.8 Double-Triggered SCR (DTSCR) [27]

Another method, to reduce the switching voltage of LSCR device and to further enhance the turn-on speed of LSCR device more efficiently, is the double-triggered technique, which is used to synchronously trigger the NPN and PNP bipolar transistors in SCR structure. The device characteristics, turn-on properties, and the corresponding ESD detection circuits of DTSCR device are investigated in detail in Chapter 4 in this thesis. The dummy-gate structure used to block the STI in SCR device can be applied to the DTSCR structure to further reduce the switching voltage and to enhance the turn-on speed of DTSCR more efficiently.

1.3.9 Native-NMOS-Triggered SCR (NANSCR) [28]

The native NMOS is directly built in a lightly-doped p-type substrate in sub-quarter-micron CMOS process, whereas the normal NMOS (PMOS) is in a heavily-doped P-well (N-well) in a P-substrate twin-well CMOS technology. The native NMOS and lateral SCR can be merged together to be a new ESD protection device, native-NMOS-triggered SCR (NANSCR), which is discussed in detail in Chapter 6 in this thesis.

1.3.10 Stacked-NMOS Triggered SCR (SNTSCR) for Mixed-Voltage I/O Buffer [29], [30]

To improve the ESD robustness of stacked NMOS in mixed-voltage I/O buffer, the stacked-NMOS triggered SCR (SNTSCR) had been reported without using the thick gate oxide. The ESD protection circuit combined gate coupling circuit with SNTSCR for mixed-voltage I/O buffer is shown in Fig. 1.9(a). The ESD detection circuit and the device structure of SNTSCR are shown in Fig. 1.9(b). Such an ESD protection circuit with only thin gate oxide is fully process-compatible with general CMOS processes without causing the gate-oxide reliability issue. During normal circuit operating conditions, the Mn3 in Fig. 1.9(b) acts as a resistor to bias the gate voltage (Vg1) of Mn1 at VDD. But, the gate of Mn2 is grounded through the resistor R2. So, all the devices in the ESD protection circuit can meet the electrical-field constraint of gate-oxide reliability in the normal circuit operation

condition. Under the positive-to-VSS (PS) ESD-zapping condition (with grounded VSS but floating VDD), the Mp is turned on but Mn3 is off since the initial voltage level on the floating VDD line is zero. The capacitors C1 and C2 are designed to couple ESD transient voltage from the I/O pad to the gates of Mn1 and Mn2, respectively. The coupled voltage should be designed greater than the threshold voltage to turn on Mn1 and Mn2 for triggering on the SNTSCR device, before the devices in the mixed-voltage I/O circuit are damaged by ESD stress. With the gate-coupling circuit technique, the switching voltage of SNTSCR can be nearly reduced to its holding voltage, so the SNTSCR can be quickly triggered on to discharge ESD current. From the experimental results in 0.35-μm CMOS process, the HBM ESD level of the mixed-voltage I/O buffer with this ESD protection circuit can be greatly improved to 8 kV, as compared with that (~2 kV) of the traditional mixed-voltage I/O buffer with only stacked NMOS device.

1.3.11 Dual-Direction SCR [43]

A typical ESD protection scheme must protect each I/O pad against ESD events in all stressing modes with respect to both VDD and VSS power lines (i.e., PS, negative-to-VDD (ND), positive-to-VDD (PD), and negative-to-VSS (NS) ESD-zapping conditions). The dual-direction SCR device was invented in BiCMOS technology to provide the ESD protection in all stressing modes through the active SCR current paths to discharge ESD current. The device structure of a dual-direction SCR device illustrated in Fig. 1.10(a) is a symmetrical 5-layer NPNPN structure comprising one lateral PNP (Q1) and two vertical NPN (Q2 and Q3) in the BiCMOS process. The trigger-assist circuit to reduce the switching voltage of dual-direction SCR comprises two pairs of Zener diodes (D1~D4) with back-to-back connection, as shown in Fig. 1.10(b). When a positive ESD pulse is applied to the anode of dual-direction SCR and its cathode is relatively grounded (e.g., PS or ND ESD-zapping condition), the Zener diode D1 will be reverse breakdown first to conduct some ESD current to trigger on the NPN bipolar Q3 and then in turn turns on the PNP bipolar Q1. The positive ESD current can be discharged through the current path1 in Fig. 1.10(b). Similarly, when a negative ESD pulse is applied to anode of dual-direction SCR with its cathode grounded (e.g., PD or NS ESD-zapping condition), the negative ESD current can be discharged through the current path2 in Fig. 1.10(b). The I-V characteristic of the

dual-direction SCR is shown in Fig. 1.10(c). Such a dual-direction SCR can provide the desired low holding voltage and low impedance path to protect the internal circuit under positive and negative ESD zapping. To realize the dual-direction SCR device in the CMOS process, an extra deep N-well mask will be added into the process flow. In the earlier literature, the full-SCR protection design for I/O pad with four SCR in CMOS IC had been reported [44].

1.3.12 SCR Devices in Other Applications

Except the standard CMOS process, SCR devices can be used as the ESD protection circuits in other applications, such as high-voltage process. The drain-extended NMOS (DENMOS) or lateral DMOS (LDMOS) had been well studied and used in mature high-voltage processes to tolerant the large gate-to-drain voltage. However, the area-efficient ESD robustness of DENMOS or LDMOS is very poor to sustain the required ESD specifications under the limitation of parasitic capacitance. The DENMOS merged with an SCR [45], [46] and the embedded SCR LDMOS (ESCR-LDMOS) [47] had been reported to improve ESD level of high-voltage IC products. Another ESD protection device for high-voltage applications is the mirrored lateral SCR (MILSCR) [48]. The MILSCR, which is designed with dual-direction active SCR current paths, comprises two vertical NPN transistors, one vertical, and one lateral PNP transistors in N-epi P-substrate high-voltage CMOS process. The MILSCR was designed for high-voltage applications [48], but its switching voltage can also be adjusted to meet the requirements of the low-voltage CMOS ICs as the MLSCR or the LVTSCR. Although the SCR-based devices can elevate the ESD levels of high-voltage CMOS IC products, how to avoid the transient-induced latchup issue [32] of SCR-based devices under normal circuit operating conditions in high-voltage process is another serious concern.

1.4 SCR LATCHUP ENGINEERING

In order to make SCR-based devices with low enough switching voltage for effective ESD protection, transient-induced latchup issue [32] must be avoided. There are two solutions to avoid the SCR-based devices with low switching voltage being accidentally

triggered on by noise pulse when CMOS ICs are in normal circuit operating conditions. As shown in Fig. 1.11(a), one is to increase the triggering current of the low-voltage-trigger SCR-based devices, but the switching voltage and the holding voltage are kept the same. With higher triggering current, the low-voltage-trigger SCR-based devices such as LVTSCR has enough noise margin against the overshooting or undershooting noise pulses on the pads. A high-current NMOS-trigger lateral SCR (HINTSCR) [49] device has been successfully designed by adding a bypass diode into the LVTSCR structure to increase its triggering current up to 218.5 mA in a 0.6-μm CMOS process. Such HINTSCR has a noise margin greater than VDD+12 V in the 3-V application. In addition, a high holding current SCR (HHI-SCR) device, which is modified from the GGSCR, was reported with a holding current of ~70 mA in a 0.1-μm CMOS process by adjusting the external poly resistance from ~kΩ in GGSCR to only ~10 Ω in HHI-SCR.

Another method immune from latchup is to increase the holding voltage of the SCR-based devices to be greater than the maximum voltage level of VDD, as shown in Fig. 1.11(b). By using the epi-substrate, the holding voltage of SCR device can be increased to avoid latchup problem [50]. But, the fabrication cost of CMOS wafer will be also increased. By stacking the voltage drop elements (such as diode or the SCR devices) with the SCR-based device can elevate its total holding voltage in the bulk CMOS process. The switching voltage and current can be still kept at a lower voltage level by suitable trigger-assist circuit design. A cascaded-LVTSCR [51] structure was designed to increase the holding voltage (> VDD) without degrading its ESD robustness in a 0.35-μm silicided CMOS technology. In addition, the ESD protection circuits designed with stacked STSCR devices [24], or designed with a STSCR device and stacked diode string [26], had been reported to have 7-kV HBM ESD level and free to latchup issue in a 0.25-μm silicided CMOS technology. Recently, the holding voltage of a single SCR device can be dynamically adjusted for ESD protection (with low holding voltage) and for normal circuit operation (with higher holding voltage) [52]. A dynamic holding voltage SCR (DHVSCR) was reported to be an ESD protection device with high latchup immunity. The device structure of DHVSCR is shown in Fig. 1.12(a). A PMOS and a NMOS are inserted into the DHVSCR device structure, as compared with LSCR structure. The I-V characteristics of the DHVSCR under normal circuit operating conditions and ESD-zapping conditions in a 0.25-μm CMOS process are shown in Fig. 1.12(b). Under normal circuit operating conditions, the gates (Vg1 and Vg2) of

PMOS and NMOS are biased at 2.5 V (VDD), but at 0 V under ESD-zapping conditions. The holding voltage and holding current of DHVSCR under normal circuit operating conditions are 2.8 V and 172 mA, respectively. Thus, the DHVSCR will not be kept in the latchup state in normal circuit operating conditions. However, the holding voltage and holding current of DHVSCR under ESD-zapping conditions are dropped to 2.2 V and 91 mA, respectively. So, the DHVSCR can also clamp the ESD overstress to a lower voltage level to sustain the higher ESD levels. The holding voltage and holding current of DHVSCR can be adjusted by controlling the gate voltages of PMOS and NMOS, which are merged with the SCR structure.

However, with the scaled-down CMOS technologies, the power-supply voltages in CMOS ICs have also been scaled downwards to follow the constant-field scaling requirement and to reduce power consumption. For CMOS IC products realized in a 0.13-μm silicided CMOS process, the maximum supply voltage for the internal circuit has been reduced to 1.2 V, so the latchup concern inherent in SCR-based device will vanish certainly. Therefore, SCR-based device with lower switching voltage can be a great candidate for on-chip ESD protection due to its highest ESD robustness, smallest layout area, and free to latchup danger, as compared with other ESD protection devices. However, in such a 0.13-μm CMOS process with ultra thinner gate oxide, the turn-on speed of SCR devices should be enhanced to quickly discharge ESD overstress voltage for protecting such thinner gate oxide. The NANSCR [28] and the dummy-gate structure [40] to improve the turn-on speed of SCR-based device will be a better choice to protect such an ultra thinner gate oxide in nanoscale CMOS processes.

The comparison among various SCR-based devices for on-chip ESD protection has been summarized in Table 1.1. The HBM and MM ESD levels of SCR-based devices are always superior to other non-SCR ESD protection devices. The switching voltage and the turn-on speed of SCR-based devices must be finely designed to fully and effectively protect the ultra-thin gate oxide of input stages, especially against the fast CDM ESD events. The switching voltage and turn-on speed of SCR-based devices will be the dominated factors on the overall performances of on-chip ESD protection circuits with SCR-based devices in nanoscale CMOS process with the maximum voltage supply smaller than 1.2 V.

1.5 THESIS ORGANIZATION

To reduce the switching voltage and to improve the turn-on speed of SCR device for effective ESD protection, some advanced trigger-assist circuits applied to SCR device are proposed and discussed in this thesis. This thesis contains seven chapters. Chapter 1 introduces the background of ESD events and the turn-on mechanism of SCR device. An overview of the ESD protection circuit with SCR-based devices for general or high-voltage CMOS processes is presented. Moreover, two practical problems (such as higher switching voltage and transient-induced latchup issue) limiting the use of SCR-based devices in on-chip ESD protection are discussed. Some modified device structures and trigger-assist circuit techniques to reduce the switching voltage of SCR-based devices are reported. The solutions (increase the triggering current or holding voltage) to overcome latchup-issue in the SCR-based devices are also discussed to safely apply the SCR-based devices in the ESD protection circuits of CMOS IC products.

In Chapter 2, an SCR device with substrate-triggered technique is first proposed for effective on-chip ESD protection. The DC I-V characteristics of a single STSCR device or stacked STSCR devices are investigated and discussed in detail in a 0.25-μm CMOS process. The ESD-like voltage pulses are applied to the STSCR device to verify its turn-on time under different substrate biases. The ESD-zapping and TLP measurements have been used to verify the ESD robustness of the STSCR devices under different substrate-triggered currents. For CMOS IC applications with maximum voltage level of 2.5 V, the on-chip ESD protection circuit with two STSCR devices in stacked configuration has a clamp voltage of ~3.2V, the HBM (MM) ESD level of > 8 kV (700 V), and free to latchup issue.

In Chapter 3, a complementary circuit style with the substrate-triggered SCR devices is designed to discharge both of the pad-to-VSS and pad-to-VDD ESD stresses. The DC I-V characteristics of an STSCR device with stacked diode string are investigated and discussed in detail in a 0.25-μm CMOS process. The advanced ESD detection circuits are proposed to provide the substrate- and well-triggered currents according to the principle of RC delay (used to distinguish ESD-zapping events or the normal circuit operating conditions) or the gate-coupled circuit technique (used to generate the trigger current) to turn on this STSCR device during ESD zapping. To verify the functions of the input, output, and power-rail ESD protection circuits, the turn-on waveforms on the I/O pad and power pad are measured under

normal circuit operating conditions and ESD-zapping conditions. For the CMOS IC applications with VDD of 2.5V, the latchup-free ESD protection circuits designed with complementary-STSCR devices and two stacked diodes can sustain the HBM (MM) ESD level of ~7.25kV (500V) in a 0.25-μm fully salicided CMOS process without using silicide-blocking mask.

In Chapter 4, to further enhance the turn-on speed of SCR device, a double-triggered technique is proposed to synchronously trigger the NPN and PNP transistors in the SCR structure. With the double-triggered technique, the switching voltage and turn-on time of SCR device can be reduced more efficiently and quickly. Moreover, the required pulse widths to trigger on the SCR device can be significantly reduced by double-triggered technique. A series of turn-on waveforms used to verify the turn-on efficiency of the double-triggered SCR (DTSCR) device are investigated in this chpater. The corresponding ESD-detection circuits to synchronously generate the substrate and well triggered currents are also proposed for input, output, and power-rail ESD protection circuits.

In Chapter 5, a novel dummy-gate structure is used to block the shallow trench isolation (STI) and silicide between the diffusion regions in the SCR device, and therefore to further enhance its turn-on speed and CDM ESD levels. The DC I-V curves, turn-on waveforms, ESD-zapping, and TLP measurements are applied to verify the characteristics of STSCR with dummy-gate structure. From the experimental results in a 0.25-μm CMOS process with the gate-oxide thickness of ~50 Å, the switching voltage, turn-on speed, turn-on resistance, and CDM ESD levels of the SCR device with dummy-gate structure have been greatly improved, as compared to the normal SCR with STI structure.

In Chapter 6, a novel native-NMOS-triggered SCR (NANSCR) is proposed for on-chip ESD protection in a 0.13-μm CMOS process with voltage supply of 1.2 V. From the experimental results, the switching voltage, holding voltage, turn-on resistance, turn-on speed, and CDM ESD level of NANSCR can be greatly improved to protect the ultra-thin gate oxide against ESD stresses, as compared with the traditional low-voltage triggering SCR (LVTSCR). The emission microscope (EMMI) photographs are used to verify the turn-on process of NANSCR device under different ESD voltages. The proposed NANSCR can be designed for the input, output, and power-rail ESD protection circuits without latchup danger. In addition, a new whole-chip ESD protection scheme realized with the proposed NANSCR devices is also proposed to provide efficient and overall protection for the internal circuits in

the ultra large-scale CMOS ICs with multiple power pins.

Finally, the main results of this thesis are summarized in Chapter 7. Some suggestions for the future works are also addressed in this chapter.

TABLE 1.1

Comparison among the SCR-based devices for on-chip ESD protection.

Application	SCR Category	Switching Voltage	Turn-on Speed	*Latchup Issue	Protection Circuit Complexity	Overall Performance
Standard CMOS Process	**Lateral SCR (LSCR)** [12], [13]	high	slow	Yes	hard	poor
	Modified LSCR (MLSCR) [16]	middle	slow	Yes	hard	middle
	Low-Voltage-Triggered SCR (LVTSCR) [17], [18]	low	middle	Yes	easy	good
	Gate-Coupled PTLSCR/NTLSCR [19]	lower + tunable	fast	Yes	middle	better
	High-Current-Triggered LVTSCR (HINTSCR) [49]	low	middle	No	middle	better
	High-Holding-Voltage LVTSCR [51]	low	middle	No	hard	good
	Hot-Carrier-Triggered SCR (HCTSCR) [20]	low + tunable	slow	Yes	hard	middle
	GGNMOS-Triggered SCR (GGSCR) [21], [22]	low	fast	Yes	easy	better
	High-Holding-Current SCR (HHI-SCR) [22]	low	slow	No	middle	better
	Dual-Direction SCR [43]	low	middle	Yes	hard	good
	Stacked-NMOS-Triggered SCR (SNTSCR) [29], [30]	lower + tunable	middle	Yes	hard	better
	Substrate-Triggered SCR (STSCR) [23]-[26]	***lower + tunable***	***fast***	***Yes***	***middle***	***better***
	Double-Triggered SCR (DTSCR) [27]	***lower + tunable***	***faster***	***Yes***	***middle***	***better***
	Dummy-Gate-Blocking STSCR [40]-[42]	***lower + tunable***	***faster***	***Yes***	***middle***	***better***
	Native-NMOS-Triggered SCR (NANSCR) [28]	***lower + tunable***	***faster***	***Yes***	***easy***	***best***
	Dynamic-Holding-Voltage SCR (DHVSCR) [52]	lower	fast	No	middle	better
High-Voltage Process	**Mirrored Lateral SCR (MILSCR)** [48]	high	slow	Yes	easy	middle
	DENMOS with Self-Aligned STI-Blocked SCR [45], [46]	high	slow	Yes	easy	middle
	Embedded SCR LDMOS [47]	high	slow	Yes	easy	middle

***Some of latchup issue can be solved by stacking the multiple SCR devices to have a total holding voltage greater than the maximum voltage level of VDD or signals of CMOS ICs.**

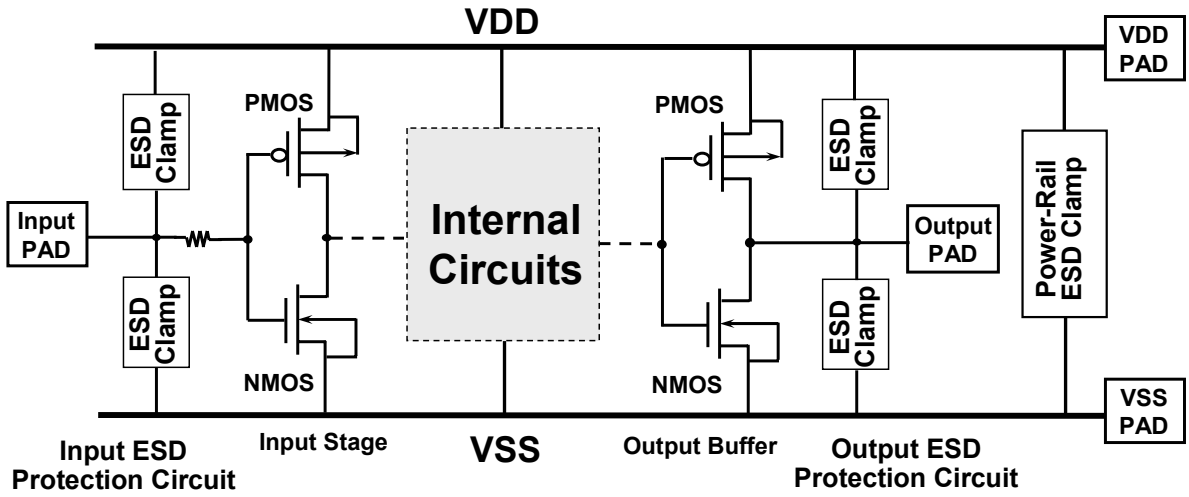
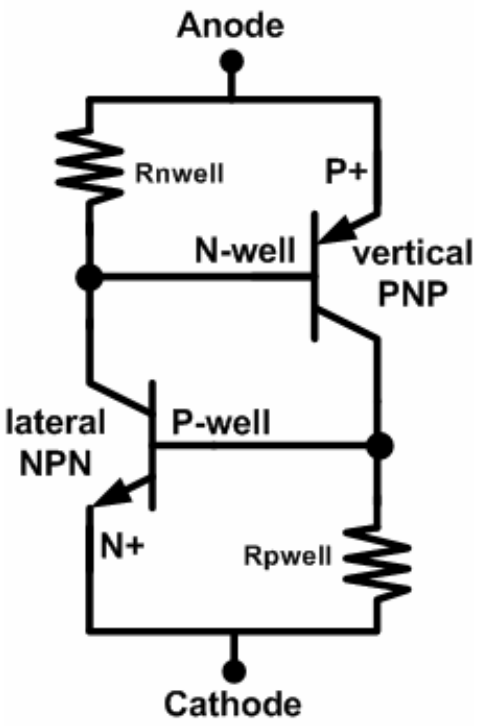
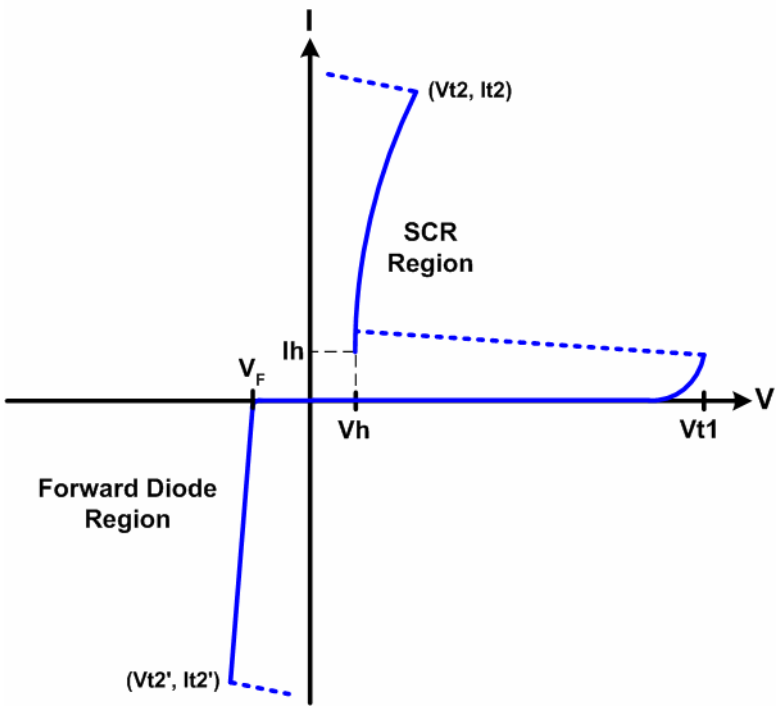


Fig. 1.1 The typical design of on-chip ESD protection circuits in CMOS ICs.

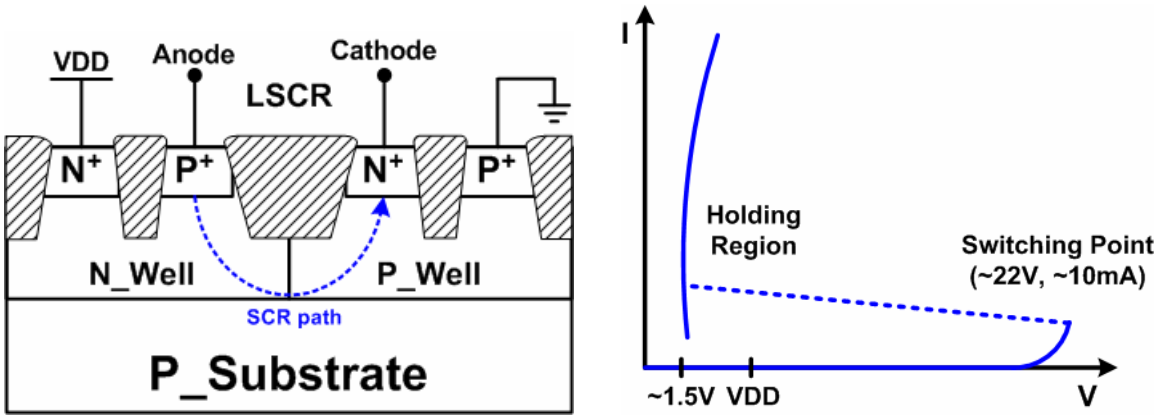


(a)

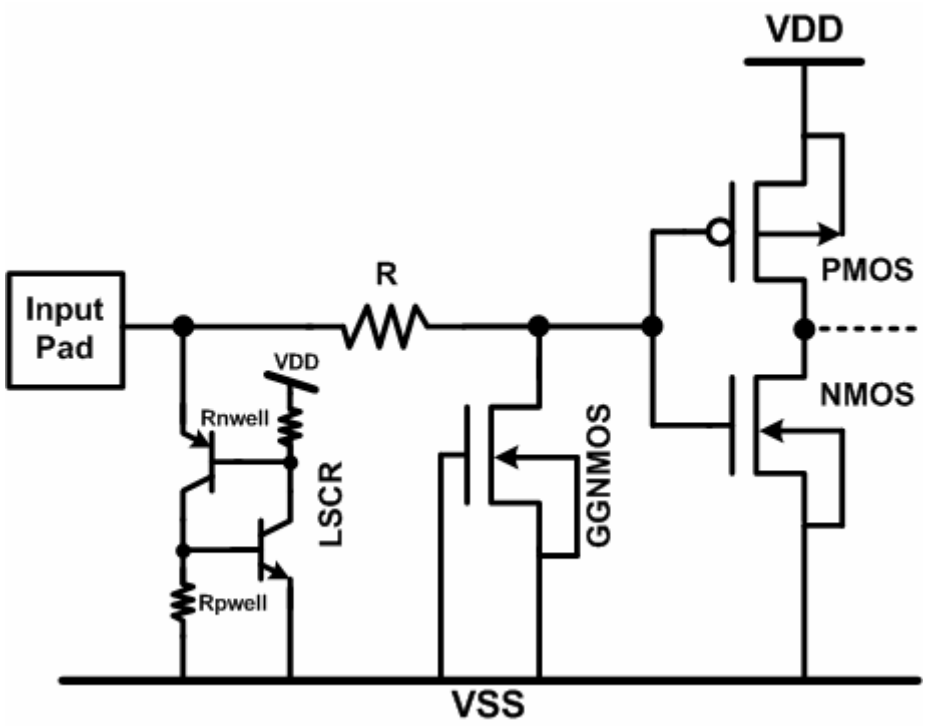


(b)

Fig. 1.2 (a) The equivalent circuit schematic of a SCR device. (b) The I-V characteristics of SCR device in CMOS process under positive and negative voltage biases.

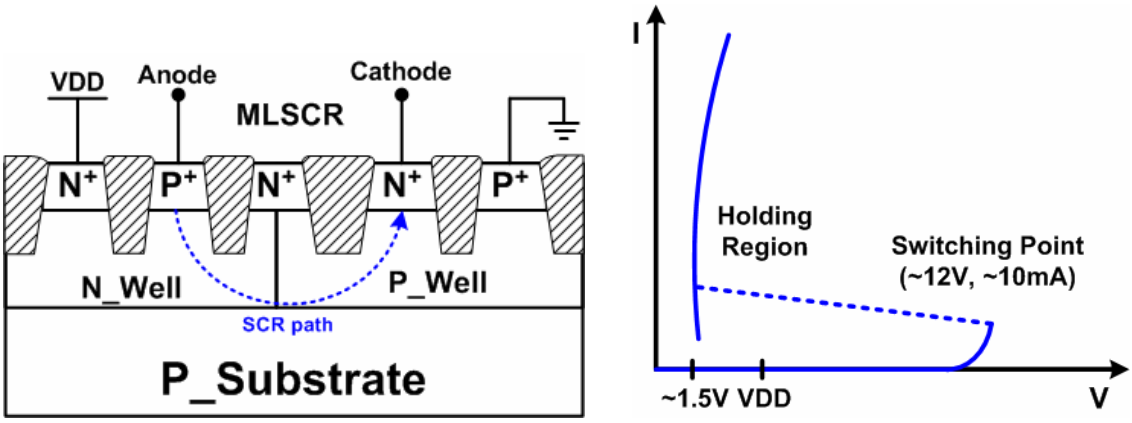


(a) (b)

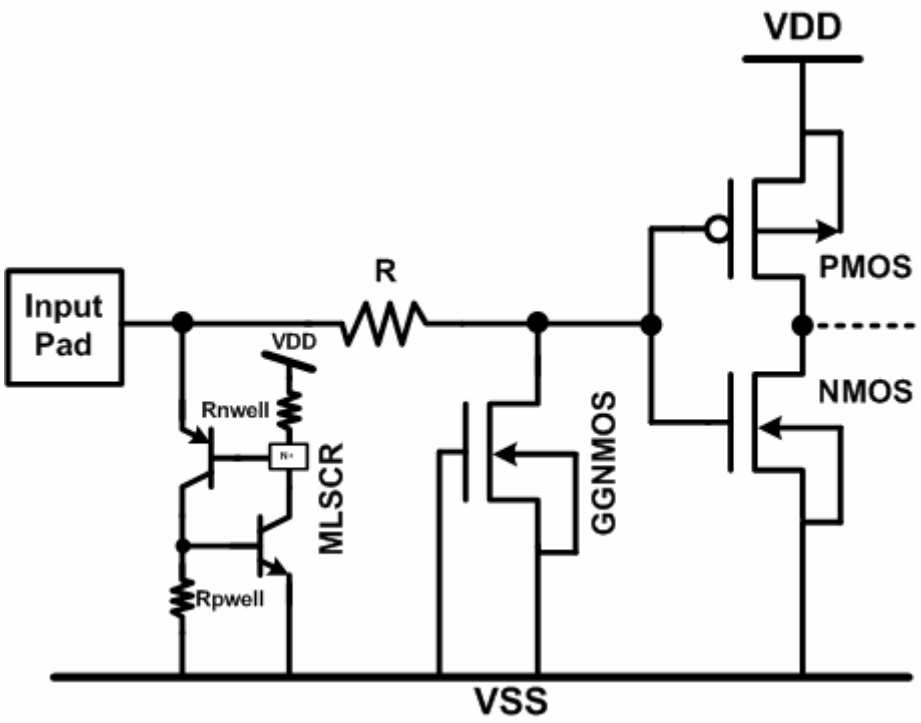


(c)

Fig. 1.3 (a) The device structure of the lateral SCR (LSCR) in CMOS process. (b) The I-V characteristics of the LSCR in a 0.25-μm CMOS process. (c) The input ESD protection circuit with the LSCR device.

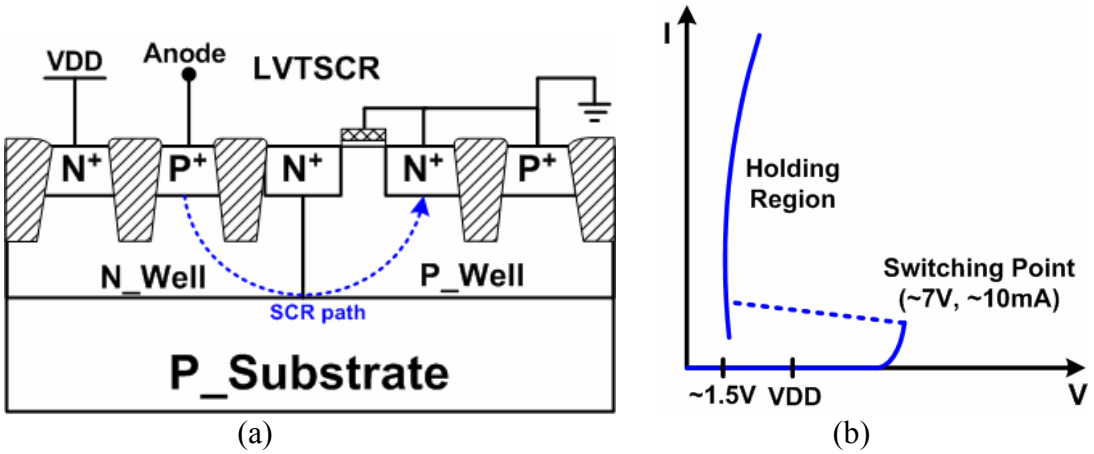


(a) (b)

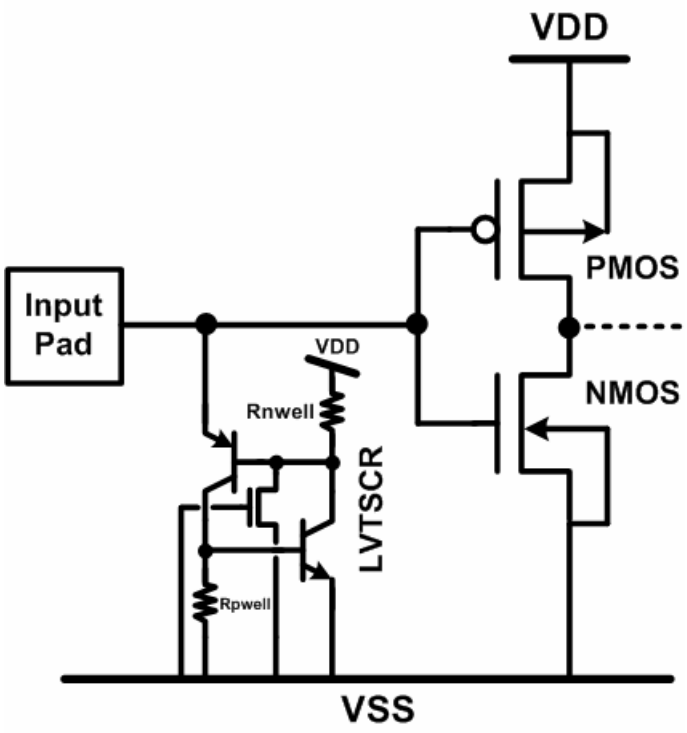


(c)

Fig. 1.4 (a) The device structure of the modified LSCR (MLSCR) in CMOS process. (b) The I-V characteristics of the MLSCR in a 0.25-μm CMOS process. (c) The input ESD protection circuit with the MLSCR device.



(a) (b)



(c)

Fig. 1.5 (a) The device structure of the low-voltage triggering SCR (LVTSCR) in CMOS process. (b) The I-V characteristics of the LVTSCR in a 0.25-μm CMOS process. (c) The example of input ESD protection circuit with the LVTSCR device.

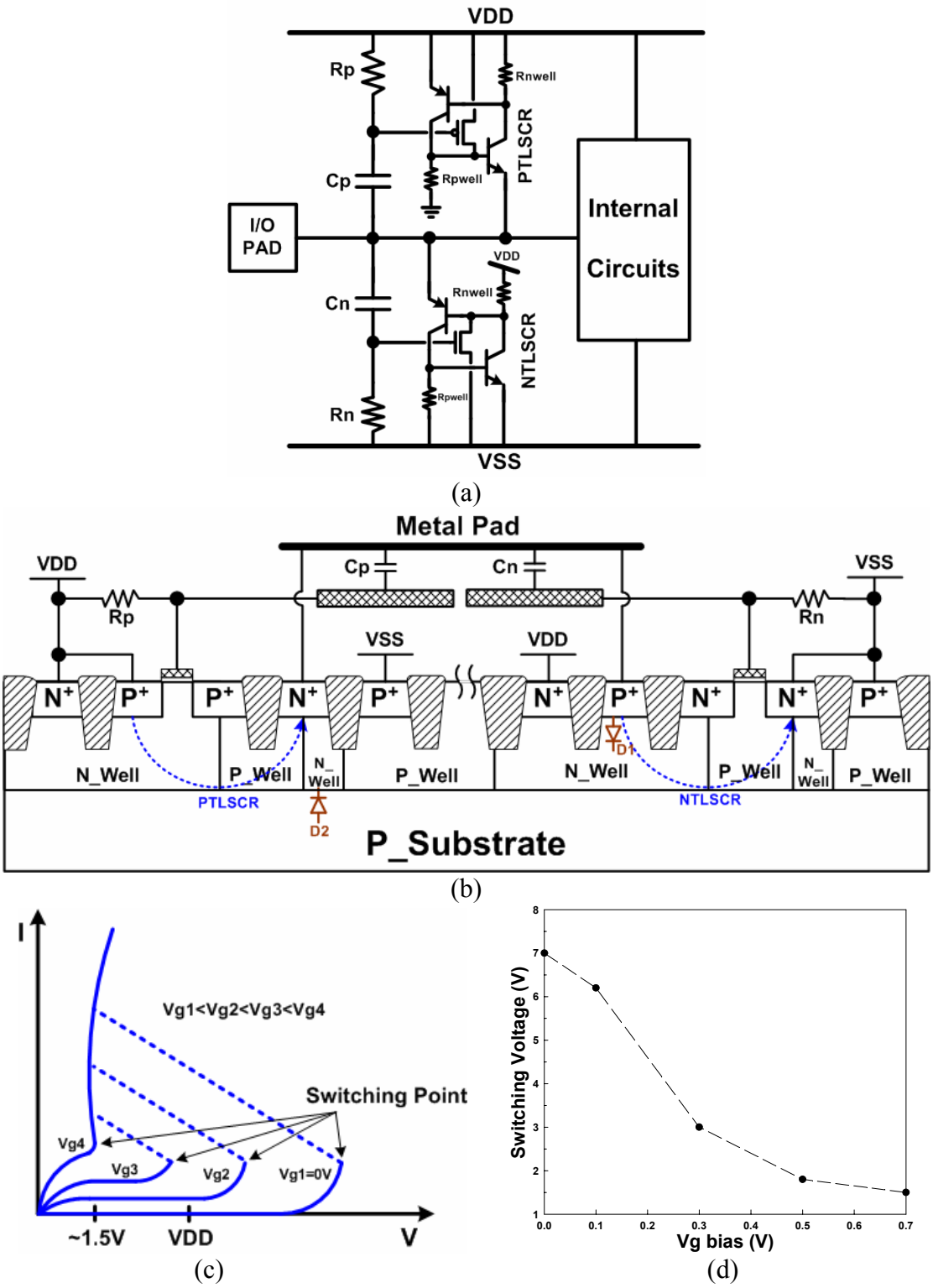
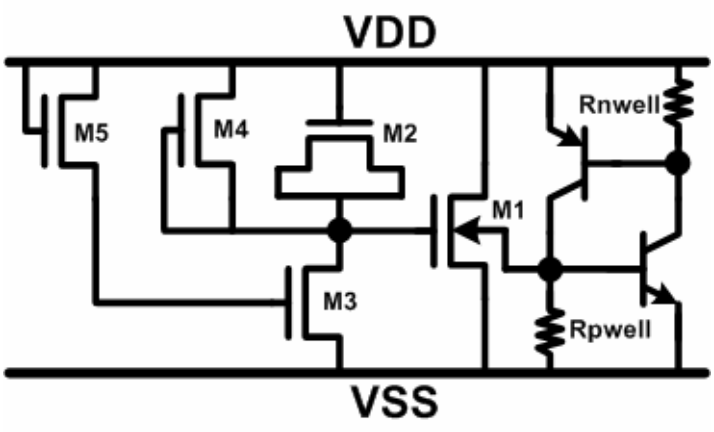
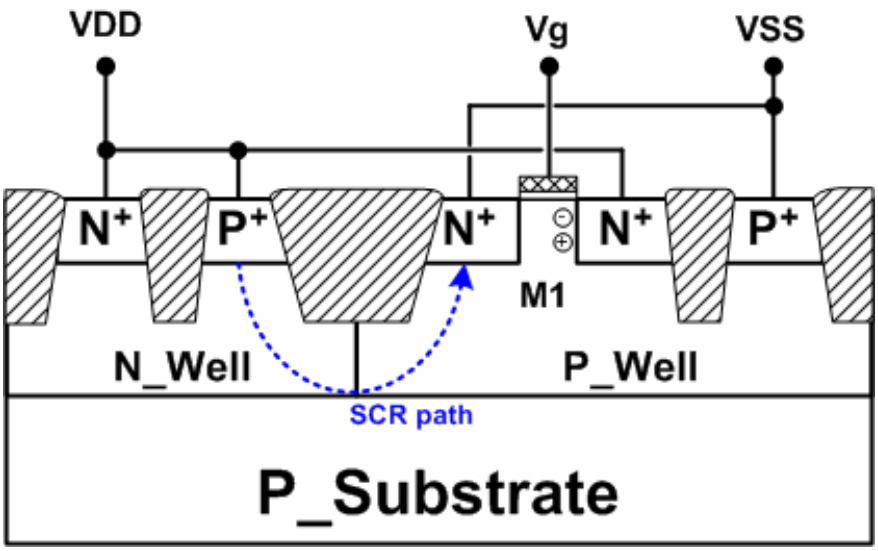


Fig. 1.6 (a) The ESD protection circuit with the gate-coupled NTLSCR and PTLSCR devices. (b) The device structure of the gate-coupled NTLSCR / PTLSCR devices in CMOS process. (c) The I-V characteristics of the gate-coupled NTLSCR device in a 0.25-μm CMOS process. (d) The dependence of switching voltage of SCR device on the gate bias voltage of the NTLSCR device.

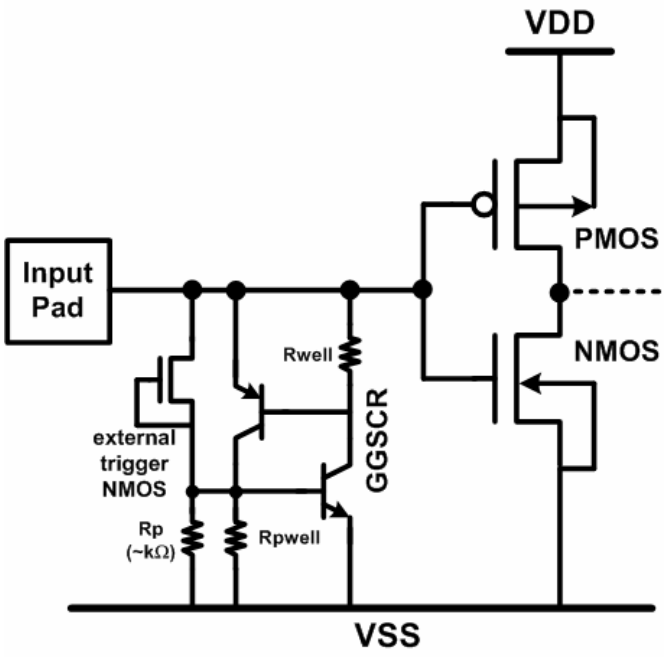


(a)

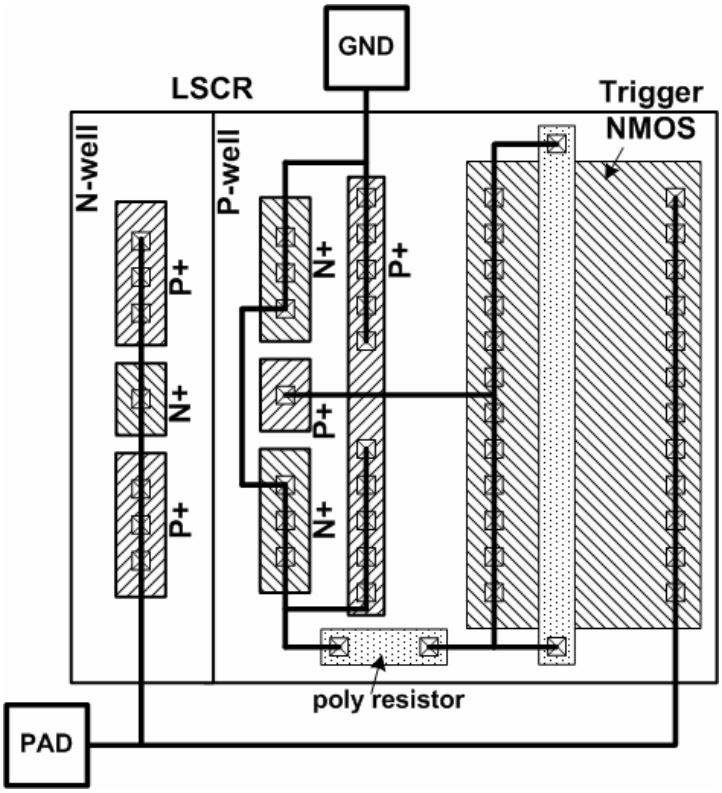


(b)

Fig. 1.7 (a) The power-rail ESD clamp circuit with the hot-carrier triggered SCR (HCTSCR) device. (b) The device structures of primary protection devices including SCR and NMOS M1.

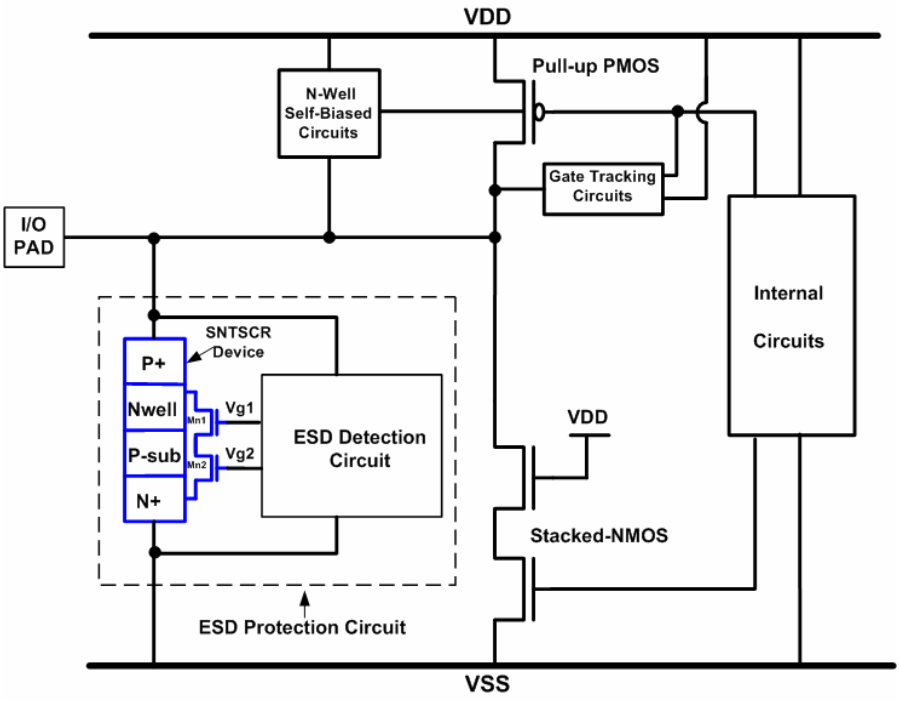


(a)

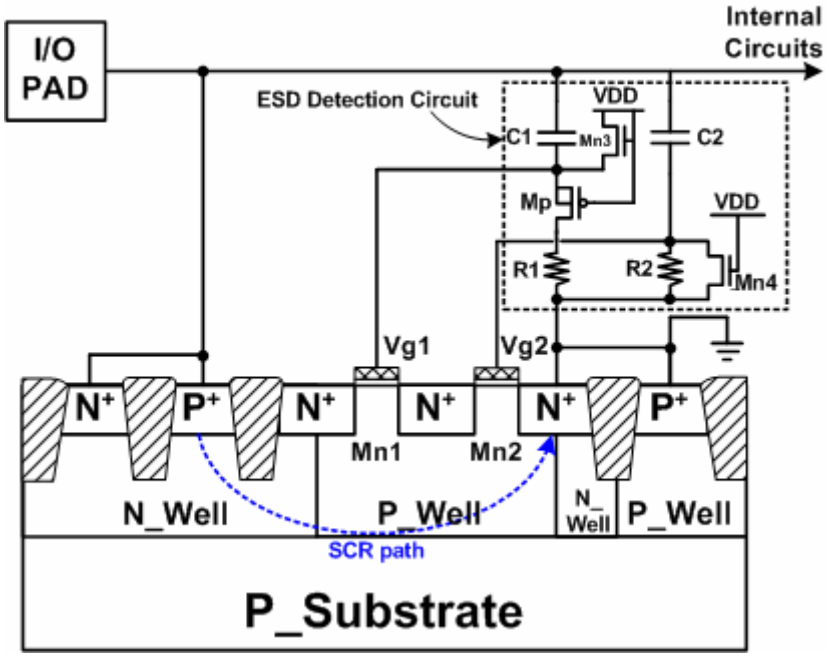


(b)

Fig. 1.8 (a) The input ESD protection circuit with the grounded-gate NMOS triggered SCR (GGSCR) device. (b) The layout top view of the GGSCR in a CMOS process.



(a)



(b)

Fig. 1.9 (a) The ESD protection circuit with stacked-NMOS triggered SCR (SNTSCR) device for mixed-voltage I/O interface. (b) The ESD detection circuit and the device structure of the SNTSCR.

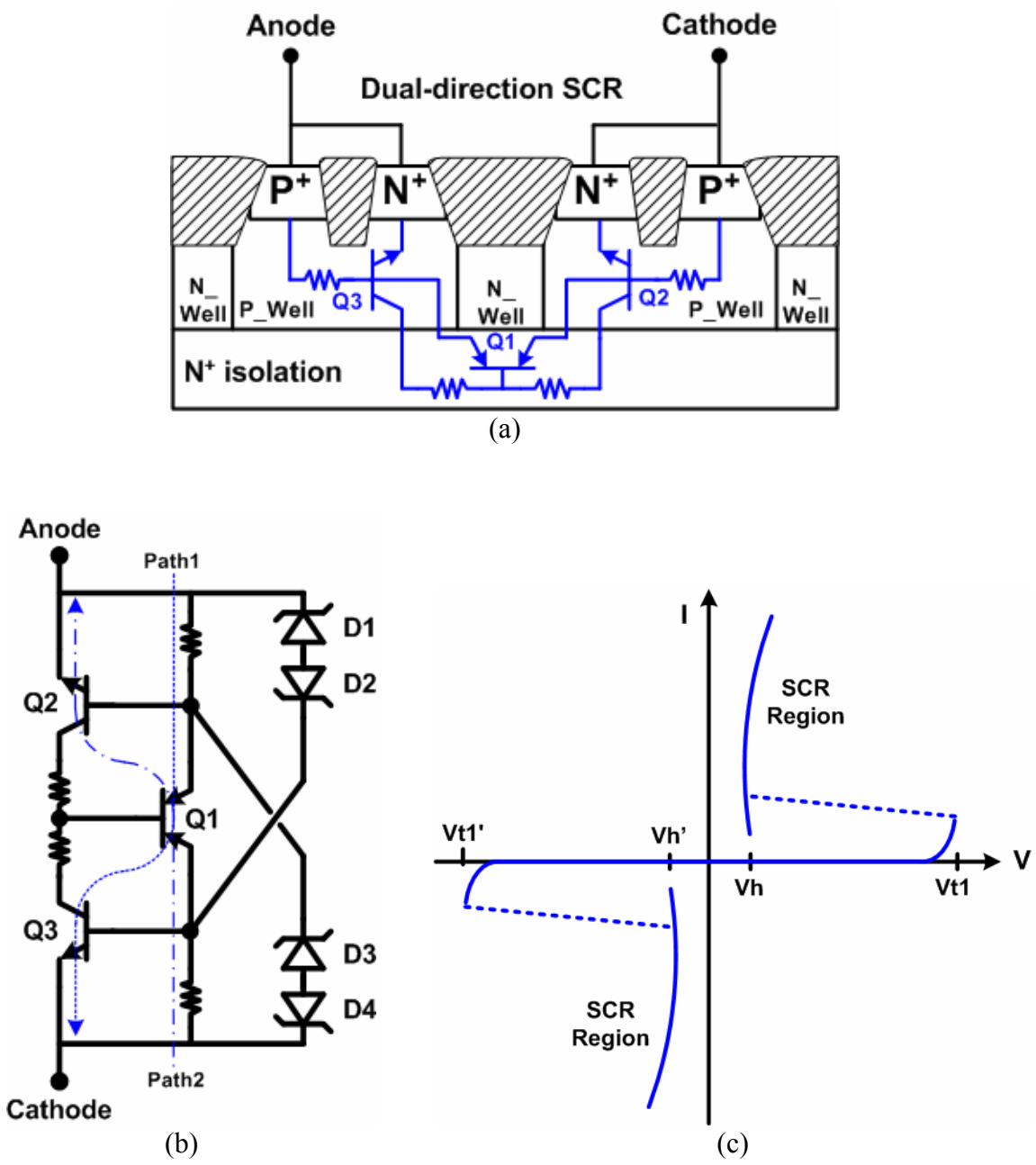
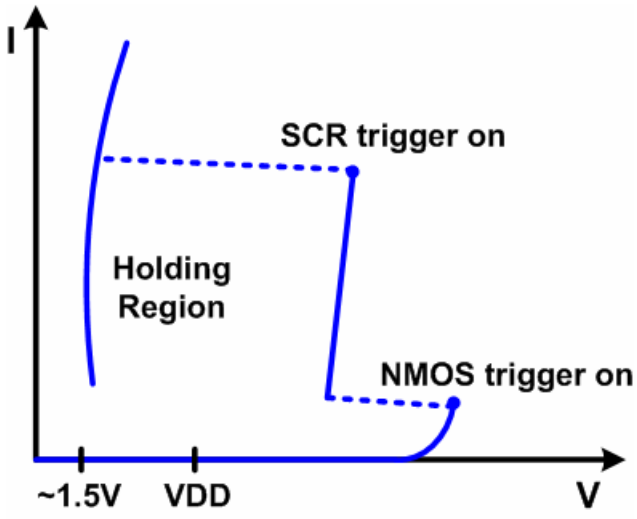
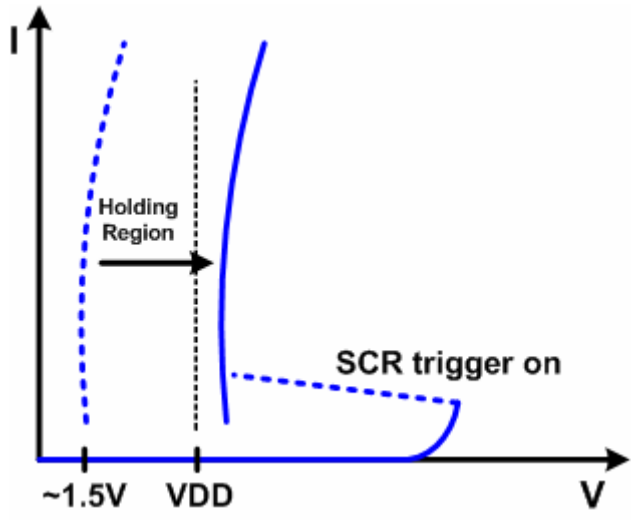


Fig. 1.10 (a) The device structure of the dual-direction SCR. (b) The circuit schematic of the low-trigger-voltage ESD protection circuit consists of a core dual-direction SCR and two back-to-back Zener diodes. (c) The I-V characteristics of the dual-direction SCR device.

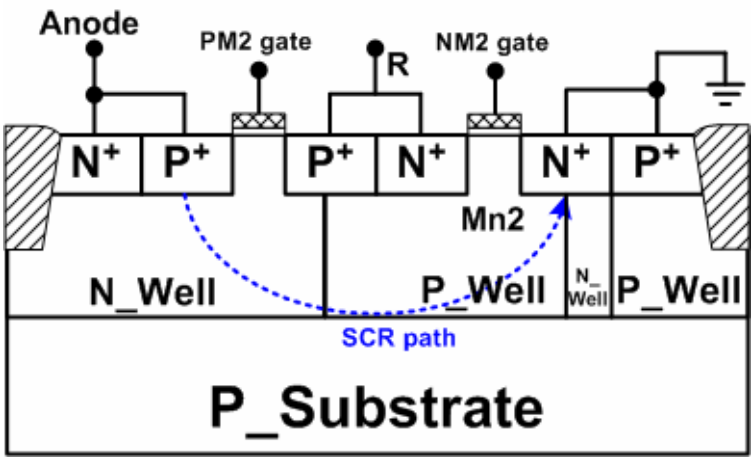


(a)

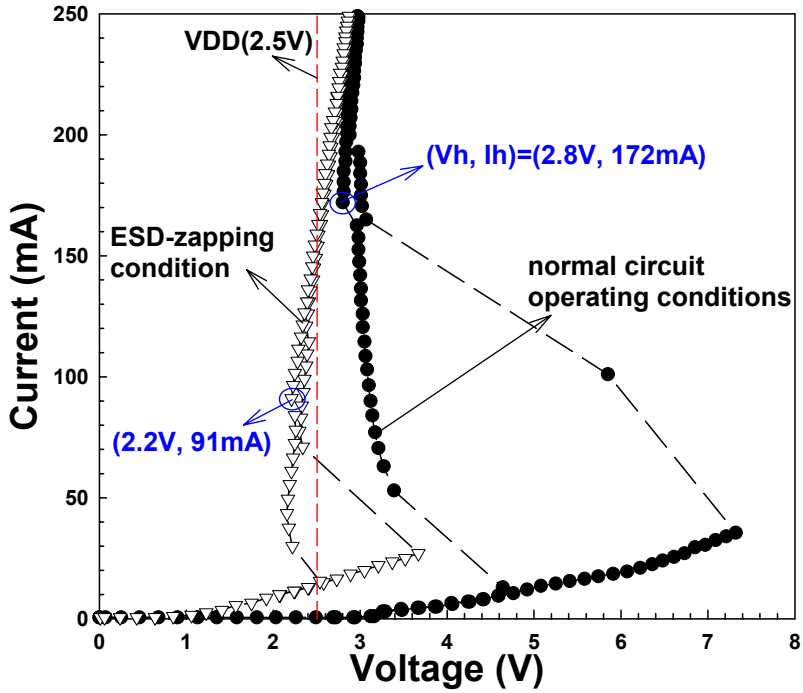


(b)

Fig. 1.11 Two solutions to overcome latchup issue in the ESD protection design with SCR-based device. (a) Increasing the trigger current and (b) increasing holding voltage to avoid the SCR-based devices being accidentally triggered on by noise pulse.



(a)



(b)

Fig. 1.12 (a) The device structure of dynamic holding voltage SCR (DHVSCR) in CMOS process. (b) The I-V characteristics of the DHVSCR under normal circuit operating conditions and ESD-zapping conditions in a 0.25-μm CMOS process.

CHAPTER 2

DEVICE CHARACTERISTICS OF SUBSTRATE-TRIGGERED SCR

In this chapter, a novel substrate-triggered SCR (STSCR) device having the ability of low switching voltage without inserting NMOS or PMOS into the SCR structure is proposed. The device characteristics of STSCR will be investigated in detail through the DC I-V measurement, turn-on verification, TLP measurement, ESD zapping, etc. The novel fully silicided STSCR device, which is compatible to general CMOS processes without extra process modification, has the advantages of controllable switching voltage and faster turn-on speed. Furthermore, the STSCR devices in stacked configuration has the adjustable holding voltage, so the ESD protection circuit with stacked STSCR devices can be designed free of the latch-up issue. Such stacked STSCR devices are designed to be kept off during the normal circuit operating conditions, and to be quickly triggered on by substrate-triggered technique during the ESD zapping conditions. The on-chip ESD protection circuits designed with such stacked STSCR devices for input pads, output pads, and power rails have been successfully verified in a 0.25-μm salicided CMOS process [23], [24].

2.1 SUBSTRATE-TRIGGERED SCR (STSCR) DEVICE

The switching voltage of LVTSCR [12] device in Fig. 1.5 relies on the drain breakdown voltage of the inserted NMOS, which is about ~7 V in the 0.25-μm CMOS process. Under ESD stress, the LVTSCR is triggered on by the current generated from the drain avalanche breakdown of the inserted NMOS. On the moment of ESD energy discharging, some electrons or holes from the ESD current of several Ampere near the drain side might be injected into the gate oxide of the NMOS [53], [54]. In Ref. [53], Aur et al. had proposed that the hot carrier lifetime would be decreased with a factor as much as of 4 due to the low-level ESD zaps (below the ESD failure threshold). Later on, Mistry et al. had also demonstrated

that the significant hole-trapping and interface trap generation occur during the snapback operation. Snapback-induced gate hole current can dramatically reduce not only the gate oxide charge-to-breakdown but also the hot carrier lifetime [54]. Therefore, for LVTSCRs, the issue that ESD charges may be injected into the gate oxide of the inserted NMOS must be well controlled, when the ESD event is zapping on such a device with much thinner gate oxide in subquarter-micrometer CMOS process.

In order to improve the quality of IC products, the reliability of the core circuits and the ESD protection circuits must be carefully concerned. Based on above discussion, the ESD protection circuits designed with a LVTSCR device might have the reliability issue if the ESD event is frequent and the gate oxide becomes much thinner. In this work, the STSCR device with lower switching voltage and higher ESD robustness is proposed, which has no gate-oxide reliability issue under low-level ESD zaps. The device structure of the proposed STSCR device is shown in Fig. 2.1, where the SCR current paths are indicated by the dashed lines. As compared with the traditional LSCR device structure, the extra P+ diffusions are inserted into the STSCR device structure. The inserted P+ diffusions are connected out as the trigger node of the STSCR device. When a trigger current is applied into this trigger node, the STSCR will be triggered into its latching state. The purpose of the additional N-well regions under the cathode (N+ diffusion) of the STSCR device is used to further enhance the turn-on speed of the STSCR for more effective ESD protection, because they increase the equivalent substrate resistance (Rsub).

Such an STSCR device has been drawn in layout and fabricated in a 0.25-μm salicided CMOS process. The experimental setup to measure I-V characteristics of the STSCR device is illustrated in Fig. 2.2(a), and the measured I-V curves of STSCR device under various substrate-triggered currents and substrate bias voltages by the curve tracer (Tektronix 370A) are shown in Figs. 2.2(b) and 2.2(c), respectively. The biased source shown in Fig. 2.2(a) can be a current source or voltage source. The triggering current (bias voltage) applied into the trigger node has a step of 1 mA (100 mV) in Fig. 2.2(b) (Fig. 2.2(c)). When the STSCR device has no substrate-triggered current (Ibias=0), the STSCR is essentially triggered on by junction avalanche breakdown between its N-well and P-substrate. In Fig. 2.2(b), the switching voltage of the fabricated STSCR device is as high as 22 V, when the substrate-triggered current is zero. But, the switching voltage of the fabricated STSCR device is reduced to only 9 V, when the substrate-triggered current is 5 mA. Moreover, the switching

voltage of the fabricated STSCR device is reduced to only 1.85 V, which almost equals to the holding voltage (~1.35 V) of the STSCR, when the substrate-triggered current is increased to 8 mA. In Fig. 2.2(c), the switching voltage of the fabricated STSCR device is reduced to 5.15 V (1.55 V) when the substrate bias voltage is increased to 1.02 V (1.06 V). So, the STSCR can be quickly triggered on by applying the triggering current or the bias voltage into this trigger node without involving the avalanche breakdown mechanism. The dependence of the switching voltage of the STSCR device on the substrate-triggered current or the substrate bias voltage applied into the trigger node of STSCR device is shown in Fig. 2.2(d). The higher substrate-triggered current or substrate bias voltage leads to a much lower switching voltage in the STSCR device. The proposed STSCR device with low switching voltage can be turned on more quickly to discharge ESD energy and to provide more effective protection for internal circuits.

Turn-on behaviors of the STSCR device with or without substrate bias have also been investigated in Fig. 2.3 under different substrate biases and voltage pulses. The voltage pulse generated from the pulse generator (HP 8110) is directly applied to the anode of STSCR device with its cathode grounded to verify its turn-on behaviors. While a 5-V voltage pulse with a rise time of 10 ns and pulse width of 400 ns is applied to the anode of STSCR without any substrate triggering, the voltage waveform on the anode is still the same as the original voltage pulse, because the switching voltage of the STSCR device is as high as 22 V. However, it is clamped to a low voltage level of only ~1.6 V in Fig. 2.3(a) by the STSCR device with a substrate bias voltage of 1.05 V. For a stand-alone STSCR device with substrate bias voltage of 0 V, it cannot be triggered on until the pulse height of the applied voltage pulse is increased up to 20 V. The voltage waveform on the anode clamped by the stand-alone STSCR device with substrate bias voltage of 0 V is shown in Fig. 2.3(b). Because of the output resistance of the pulse generator and the turn-on resistance of the STSCR device, the clamped voltage (~2.4 V) in Fig. 2.3(b) is greater than the holding voltage (~1.35 V) of a STSCR device measured in Fig. 2.2(b). Due to the dV/dt transient current, the dynamic switching voltage (20 V) of STSCR device is smaller than the static switching voltage (22 V) of STSCR device. An ESD protection device with a switching voltage of 20 V is too high to provide effective ESD protection for core circuits in a 0.25-μm CMOS process. However, the STSCR device with suitable substrate bias has a much lower switching voltage to quickly discharge the ESD current. This is a very excellent feature of the proposed STSCR device for

using in the on-chip ESD protection circuits.

Another issue of using SCR device as the ESD protection device is the transient-induced latch-up concern [32], when the IC is operating under normal circuit operations. As a result, the total holding voltage of the ESD protection circuit with SCR devices must be designed greater than the maximum voltage level of VDD during the normal circuit operating conditions to avoid the latch-up issue. This can be achieved by stacking the STSCR devices in the ESD protection circuits. Fig. 2.4 shows the dependence of the total holding voltage of the STSCR devices on different temperatures under different number of stacked STSCR devices. The experimental setup is depicted in Fig. 2.4(a). The I-V curves of two (three) STSCR devices in stacked configuration, which is marked as 2STSCR (3STSCR), under different temperatures are measured in Fig. 2.4(b) (Fig. 2.4(c)). The inserts in Figs. 2.4(b) and 2.4(c) are the enlarged views at the holding point. The total holding voltage has a bit of degradation when the operating temperature is increased, because the current gain (β) of the parasitic bipolar transistor in the SCR device is increased with the increase of operating temperature. The holding voltages of 3STSCR, for example, are 4.5, 4.2, and 3.9 V at the operating temperatures of 25 ^{o}C, 75 ^{o}C, and 125 ^{o}C, respectively. The total holding voltage, however, can be still raised up by increasing the number of the stacked STSCR devices. The holding voltages of 1STSCR, 2STSCR, and 3STSCR at the temperature of 25 ^{o}C are 1.4, 3, and 4.5 V, respectively. The measured results of the dependence of holding voltage on temperature in the stacked STSCR devices are summarized in Fig. 2.4(d) for clear comparison. Although the STSCR devices in stacked configuration will increase the total switching voltage, such stacked STSCR devices can be still quickly triggered on at a lower voltage level to provide effective ESD protection, if the substrate bias voltage can be simultaneously applied to the trigger nodes of the stacked STSCR devices.

To investigate the characteristics of the stacked STSCR devices, the measured I-V curves are depicted in Fig. 2.5 and the measurement setup is also inset into Fig. 2.5. In Fig. 2.5(a), the switching voltage of 2STSCR is reduced to ~24 V dominated by the switching voltage of first STSCR device, STSCR_1, if the voltage bias is only applied to the trigger node of second STSCR device, STSCR_2. If a 3.5-V voltage bias is simultaneously applied to the both trigger nodes of two STSCR devices, as the measurement setup inserted in Fig. 2.5(b), the total switching voltage of 2STSCR is reduced to ~5 V in Fig. 2.5(b). The higher substrate bias leads to the lower switching voltage of the stacked STSCR configuration.

Hence, the stacked STSCR configuration can be still turned on quickly if there is suitable substrate bias. The diodes, Db1~Db*k*, in the inset of Fig. 2.5 are used to block the current flowing through the metal connected among the trigger nodes of the stacked STSCR devices. Without the blocking diodes, the accumulative property in holding voltage for stacked STSCR configuration does not exist.

2.2 ON-CHIP ESD PROTECTION CIRCUITS WITH STSCR DEVICES

2.2.1 ESD Protection Circuit for the Input/Output Pads

The ESD protection circuits for input and output pads, realized with the stacked STSCR devices and ESD-detection circuit, are shown in Figs. 2.6(a) and 2.6(b). All the p-trigger nodes of the stacked STSCR devices are connected to the output node of the ESD-detection circuit, which is formed with an RC and an inverter. The input node of the inverter is connected to VDD through the resistor R. The resistor R is better realized by using the diffusion resistance for the concern of antenna effect [55]. A capacitor C is placed between the input node of the inverter and VSS. This capacitor can be formed by the parasitic capacitance at the input node of the inverter. Under the normal circuit operating conditions with VDD and VSS power supplies, the input voltage of the inverter is kept at VDD. Therefore, the output voltage of the inverter is biased at VSS due to the turn-on of NMOS in the inverter. The p-trigger nodes of the stacked STSCR devices are biased at VSS by the output voltage of the inverter, so the stacked STSCR devices are guaranteed to be kept off in the normal circuit operating conditions. When a positive-to-VSS ESD stress zapping on the pad, the input voltage of the inverter is initially kept at zero and the inverter is biased by the ESD energy on the pad. The output voltage of the inverter is charged up to high by the ESD energy to generate the trigger current into the trigger nodes of the stacked STSCR devices. Therefore, the STSCR devices are turned on and the ESD current is discharged from the pad to VSS through the stacked STSCR devices. However, the input voltage of the inverter may be charged up by the ESD energy through the forward-biased diode between the pad and VDD power rail. Therefore, the RC time constant in the ESD-detection circuit is designed to keep the input voltage of inverter with a relative low voltage level during the ESD stress

condition. The design and simulation on this RC-delay ESD-detection circuit will be described in the next subsections.

2.2.2 ESD Clamp Circuit between the Power Rails

The stacked STSCR devices can be also applied to design the power-rail ESD clamp circuit. The VDD-to-VSS ESD clamp circuit realized with the stacked STSCR devices is shown in Fig. 2.7. The number of the stacked STSCR devices between VDD and VSS power rails is dependent on the maximum voltage level between VDD and VSS in the normal circuit operating conditions to avoid the latch-up issue. The function of the ESD-detection circuit is similar to the ESD-detection circuit used in the I/O pads, but the RC time constant is designed to distinguish the VDD power-on event (with a rise time of ~ms) from the ESD-stress events (with a rise time of ~ns) [11]. The detail simulation results are shown in the next subsection. During the normal VDD power-on transition (from low to high), the input voltage of the inverter in Fig. 2.7 can follow up in time with the power-on VDD signal, so the output voltage of the inverter is kept at zero. Hence, the stacked STSCR devices are kept off and do not interfere with the functions of internal circuits.

When a positive ESD voltage is applied to the VDD line with the VSS line relatively grounded, the RC delay will keep the input voltage of the inverter at a low voltage level for a long time, therefore the output voltage of the inverter will become high to trigger the stacked STSCR devices. While the stacked STSCR devices are triggered on, the ESD current is discharged from VDD to VSS through the stacked STSCR devices. By suitable design on the ESD-detection circuit, the stacked STSCR devices can be quickly triggered on to discharge the ESD current.

The detection of ESD transition is based on the RC delay in the ESD-detection circuits, which are the same function in the input and output ESD protection circuits and the VDD-to-VSS ESD clamp circuit. So, the RC connected between VDD and VSS in the ESD protection circuits in Figs. 2.6 and 2.7 can be implemented with the same one in the whole chip of a CMOS IC to save the layout area.

2.2.3 Simulation Results

The optimum design on the ESD-detection circuit with RC-inverter to trigger on the

stacked STSCR devices for discharging ESD current from VDD to VSS is studied in Fig. 2.8. The design parameters of the R, C, and PMOS channel width (Wp) of the inverter are first considered. Fig. 2.8(a) shows the transient simulations of the ESD-detection circuit under different resistance of R, where C is fixed at 1 pF and the devices dimensions (W/L) of PMOS and NMOS are 30/0.5 and 10/0.5, respectively. An 8-V voltage pulse with a rise time of 10 ns is applied to the VDD pin to simulate the ESD event. The Y-axis in Fig. 2.8(a) is the output current from the inverter of the ESD-detection circuit. From Fig. 2.2(d), the switching voltage of the STSCR device is reduced to only 1.85 V, if the substrate-triggered current is 8 mA. Based on this condition, the trigger time that the output current of inverter is greater than 8 mA is defined as "Ttrig" in Fig. 2.8. The Ttrig is increased with the increase of the resistance R in Fig. 2.8(a). Because the turn-on time of STSCR device, which is defined from triggering state to latching state, will take about 20 ns, the Ttrig must be designed greater than 20 ns to ensure that the STSCR device can enter into latching state. The dependence of the Ttrig on the resistance (R) under different capacitances (C) is simulated and shown in Fig. 2.8(b). The Ttrig is increased while the resistance (R) or the capacitance (C) is increased, because the input voltage of inverter can be kept at low level for a relatively longer time. The relation between the resistance (R) and capacitance (C) under different Ttrig time periods are simulated and shown in Fig. 2.8(c). The suitable values for the resistance (R) and capacitance (C) can be finely tuned from Figs. 2.8(b) and 2.8(c). Under ESD zapping, the PMOS is on and NMOS is off initially, thus the output current of inverter is dominated by the PMOS. After the input voltage of inverter is charged up and greater than the threshold voltage of NMOS, the output current of the inverter is decided by the pull-up current of PMOS and the pull-down current of NMOS. The relation between channel width (Wp) of PMOS and the Ttrig under different RC time constants (τ) are shown in Fig. 2.8(d). With the increase of the channel width of PMOS or the RC time constant, the corresponded Ttrig is increased. To meet the Trig of 20 ns, the PMOS with a larger channel width only needs a smaller RC time constant. Such optimum design on device parameters in the ESD-detection circuit can be finely tuned by HSPICE simulation for different CMOS IC applications.

2.3 EXPERIMENTAL RESULTS

The proposed ESD protection circuits have been designed with different numbers of stacked STSCR devices and fabricated in a 0.25-μm salicided CMOS process. The layout views of one STSCR device and 2STSCR are depicted in Figs. 2.9(a) and 2.9(b), respectively. Each STSCR device is realized with a layout area of 40 μm×30 μm including P+ and N-well rings in the 0.25-μm salicided CMOS process. However, the active area of each STSCR surrounded by the dashed line in Fig. 2.9(a) without including the guard rings is only 20 μm×20 μm. Each blocking diode, which is shown in Fig. 2.9(b), has only been drawn with an anode area of 3.1 μm×1.3 μm. The human-body-model (HBM) and machine-model (MM) ESD stresses are applied to the ESD protection circuits to verify their ESD robustness. The HBM ESD test results on the stacked STSCR devices in the device level (without ESD-detection circuit) and the circuit level (with ESD-detection circuit) are compared in 2. 11. In this experimental measurement, the ESD-detection circuit including R, C, and inverter are realized with R=100 kΩ, C=3 pF, PMOS dimension (W/L)=80/0.5, and NMOS dimension (W/L)=20/0.5. In this ESD verification, the failure criterion is defined as the leakage current of the device or circuit after ESD stress is greater than 1μA under the voltage bias of 2.5 V. For device level, because the total holding voltage of the stacked STSCR configuration is increased with the increase of the number of the stacked STSCR devices, the HBM ESD robustness of the stacked STSCR is decreased with the increase of the number of the stacked STSCR devices except for the condition of 2STSCR. It is supposed that there are additional parasitic SCR paths between the two STSCR devices, which can be triggered on in time to discharge ESD energy. So, the HBM ESD robustness of 2STSCR is slightly greater than that of 1STSCR. The anticipated ESD discharging path is from the STSCR_1 to STSCR_2. The additional ESD discharging path is from the P+, N-well (STSCR_1), P-substrate to N+ (STSCR_2), and so on. However, for 3STSCR or 4STSCR, the HBM ESD robustness is dominated by the total holding voltage, whereas the additional parasitic SCR path can not be triggered on in time to bypass ESD current. So, the HBM ESD levels of 3STSCR and 4STSCR are degraded while the number of stacked STSCR is increased. But, the ESD level of stacked STSCR devices can be greatly improved especially for the 3STSCR or 4STSCR, if the ESD-detection circuit is used to trigger the stacked STSCR devices. From Fig. 2.10, the ESD levels of the stacked STSCR with ESD-detection circuit are all boosted up to >8 kV.

However, the ESD level of 1STSCR device is still kept at the same ESD level. For 1STSCR, having no additional SCR path, the aim of the substrate-triggered technique is to reduce the switching voltage and to enhance the turn-on speed of the SCR device.

For MM ESD event, because it has a faster ESD transition than the HBM event, the additional parasitic SCR paths in the stacked STSCR may not be triggered on in time to bypass ESD current under such fast MM ESD zapping conditions. The measurement results on the MM ESD levels of the stacked STSCR with or without ESD-detection circuit are shown in Fig. 2.11. The MM ESD level is decreased when the number of stacked STSCR devices is increased. However, the MM ESD levels of the stacked STSCR devices can be also improved if the ESD-detection circuit is used to trigger the stacked STSCR devices.

A gate-grounded NMOS (GGNMOS) device with W/L of 200/0.5 had been fabricated in the same CMOS process with extra silicide-blocking mask for comparison reference. Such GGNMOS occupied a large layout area of 25.8 μm×60 μm including a P+ guard ring can sustain the HBM ESD level of 3.5 kV. The active area of GGNMOS without including guard ring is 25.8 μm×50 μm. The comparison on the ESD robustness between the stacked STSCR devices and GGNMOS is shown in Table 2.1. For the ESD protection circuit designed with 2STSCR and ESD-detection circuit, the HBM (MM) ESD level per layout area is >10 V/μm^2 (0.88 V/μm^2), but it is only 2.71 V/μm^2 (0.29 V/μm^2) for the GGNMOS. This has verified the excellent area efficiency of the ESD protection circuits realized with the proposed stacked STSCR devices.

By using the transmission line pulsing (TLP) measurement [56], [57], the secondary breakdown current (It2) of the STSCR device can be found. It2 is another index for the HBM ESD robustness, which is indicated in this work by the sudden increase of the leakage current at the voltage bias of 2.5 V. The relation between second breakdown current (It2) and HBM ESD level (V_{ESD}) can be approximated as:

$$V_{ESD} \cong (1500+Ron) \times It2, \tag{2.1}$$

where Ron is the dynamic turn-on resistance of the device under test. The TLP-measured I-V curves of the stacked STSCR devices with different number of STSCR devices are shown in Fig. 2.12. The It2 in Fig. 2.12 is almost decreased with the increase of the number of stacked STSCR devices except the condition of 2STSCR, which is similar to the results of HBM ESD level. The above hypothesis about the existence of the additional parasitic SCR paths can be also used to explain why the 2STSCR has a higher It2. The TLP-measured I-V curves of the

4STSCR under different substrate bias voltages are shown in Fig. 2.13. Although the It2 of 4STSCR without substrate bias is only 0.93 A, it can be improved to 3.45 A, if a 6-V voltage bias is applied to the trigger nodes through the blocking diodes in Fig. 2.13. With increasing the substrate bias voltage, the It2 of the stacked STSCR is also increased. In Fig. 2.13, the total switching voltage of the stacked STSCR devices can be reduced to a low voltage level when the voltage bias is applied to all of the trigger nodes, which is consistent with the results shown in Fig. 2.5. Therefore, the ESD protection circuits with stacked STSCR device and ESD-detection circuit have the advantages of a lower switching voltage, no latch-up issue, and higher ESD robustness.

In order to investigate the turn-on efficiency of the ESD protection circuit realized with STSCR devices, the experimental setup to measure the required turn-on time of the STSCR device is illustrated in Fig. 2.14. The measured results in time domain are shown in Fig. 2.15, where the V_anode (V_trigger) is the voltage waveform on the anode (trigger) of the STSCR shown in Fig. 2.14. A 5-V voltage bias is connected to the anode of the STSCR device through a resistance of 47 Ω, which is used to limit the sudden large transient current from power supply when the STSCR is turned on. A voltage pulse with a pulse width of 400 ns and a rise time of 10 ns is applied to the trigger node. While a voltage pulse of 1 V is applied to the trigger node, the V_anode has no significant change, as shown in Fig. 2.15(a). So, the STSCR device has at least a substrate noise margin of 1 V. The V_anode, however, is triggered into latching state while the pulse voltage is increased to 2 V, as shown in Fig. 2.15(b). The forward-biased P+ trigger node to cathode in the STSCR device limited the full swing of the 2-V applied voltage waveform in Fig. 2.15(b). After the triggering of the 2-V voltage pulse, the V_anode is still kept at a low voltage level of 2.5 V. The STSCR device has been successfully triggered on and provided a low-impedance path to discharge ESD current from its anode to its cathode. The required turn-on time for the STSCR device into its latching state is observed by the close-up views of the V_anode waveform at the falling edge, which are shown in Fig. 2.15(c) to Fig. 2.15(e) under different triggering voltage pulses. The dependence of turn-on time of such STSCR device on the pulse height of the triggering voltage pulse is compared in Fig. 2.15(f). From Fig. 2.15(f), the turn-on time of the STSCR device can be reduced from 27.4 ns to 7.8 ns, while the pulse height of the triggering voltage pulse is increased from 1.5 V to 4 V. The turn-on speed is improved with a factor of ~4. The measured results have shown that the novel ESD protection circuit proposed in this chapter

can indeed be turned on more quickly to discharge ESD current. Therefore, the proposed ESD protection circuit can provide the more effective protection for internal circuits as long as enough substrate bias is supplied.

To verify the property of free to latch-up issue, another verification to measure the holding voltages of the stacked STSCR devices is tested under transient conditions, and the results are shown in Fig. 2.16. The stacked STSCR devices can be triggered on by the ESD-detection circuit and provide a low impedance path to discharge the ESD energy. In Fig. 2.16, a 0-to-8V voltage pulse applied to the VDD line of Fig. 2.7 is clamped to 1.6V (3.2V) by the ESD protection circuit with 1STSCR (2STSCR) device and the ESD-detection circuit. When the voltage pulse is applied to the VDD line, the voltage pulse is quickly clamped to a low voltage level within only several ns. The clamped voltage level of the ESD protection circuit can be linearly adjusted by changing the number of stacked STSCR devices for practical applications in CMOS IC products with different VDD voltage levels. For the IC application with VDD of 2.5V, the ESD protection design with 2STSCR and ESD-detection circuit has a clamp voltage of ~3.2V and the HBM (MM) ESD level per layout area of >10V/μm^2 (0.88V/μm^2).

The function of the ESD-detection circuit, RC-inverter, is used to distinguish the VDD power-on event (with a rise time of ~ms) from ESD-stress events (with a rise time of ~ns). The function has been successfully confirmed in Fig. 2.17. When a 0-to-5V voltage pulse with a rise time of 10 ns to simulate the ESD transient is applied to the VDD line of Fig. 2.7, where only one STSCR device is placed between the power rails in this verification, the voltage waveform in Fig. 2.17 has obvious degradation and clamped to ~1.6 V by the STSCR device. On the contrary, while the voltage pulse with a rise time of 1 ms is applied to the VDD pin, the applied 0-to-5V voltage waveform has no degradation in Fig. 2.17. So, the proposed ESD protection circuit with the STSCR device and ESD-detection circuit is kept off during the normal circuit operating conditions.

2.4 SUMMARY

A novel substrate-triggered SCR (STSCR) device used for on-chip ESD protection circuits has been successfully investigated in a 0.25-μm salicided CMOS process. By using

the substrate-triggered technique, the STSCR device has the advantages of controllable switching voltage (~1.85 V@8 mA or ~1.55 V@1.06 V) and high ESD robustness in a smaller layout area (~16 V/μm^2). On-chip ESD protection circuits designed with the stacked STSCR devices and ESD-detection circuit have the advantages of high latch-up immunity, controllable switching voltage, adjustable holding voltage, fast turn-on speed, and higher ESD robustness, which are very useful in CMOS IC products in sub-quarter-micron CMOS processes. The experimental result has shown that the turn-on time of STSCR can be reduced from 27.4 ns to 7.8 ns by the substrate-triggering technique. For the IC applications with VDD of 2.5V, the ESD protection circuit designed with two STSCR devices in stacked configuration and ESD-detection circuit can sustain the HBM (MM) ESD level per area of >10V/μm^2 (0.88 V/μm^2) in a 0.25-μm fully salicided CMOS process without using extra process modification.

TABLE 2.1

Comparison on the ESD robustness between the stacked STSCR devices and the GGNMOS.

Device	2STSCR	3STSCR	GGNMOS
Active Area (μm^2)	20×20×2	20×20×3	25.8×50
HBM (kV)	> 8	> 8	3.5
$\frac{V_{ESD,HBM}}{Area}$ ($V/\mu m^2$)	> 10	> 6.67	2.71
MM (V)	700	525	375
$\frac{V_{ESD,MM}}{Area}$ ($V/\mu m^2$)	0.88	0.44	0.29

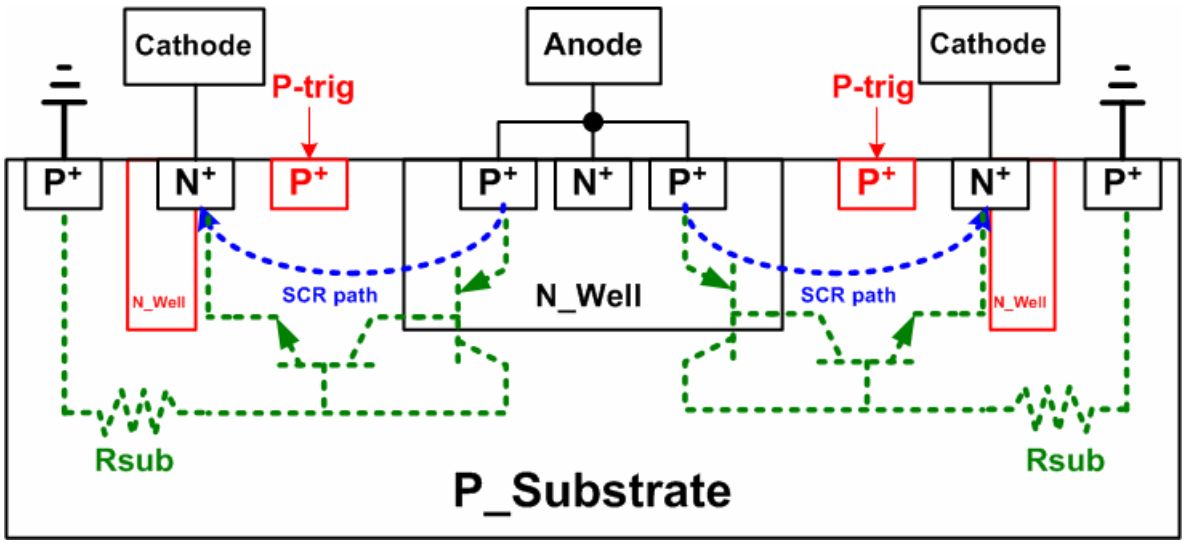


Fig. 2.1 Device structure of the proposed substrate-triggered SCR (STSCR) device.

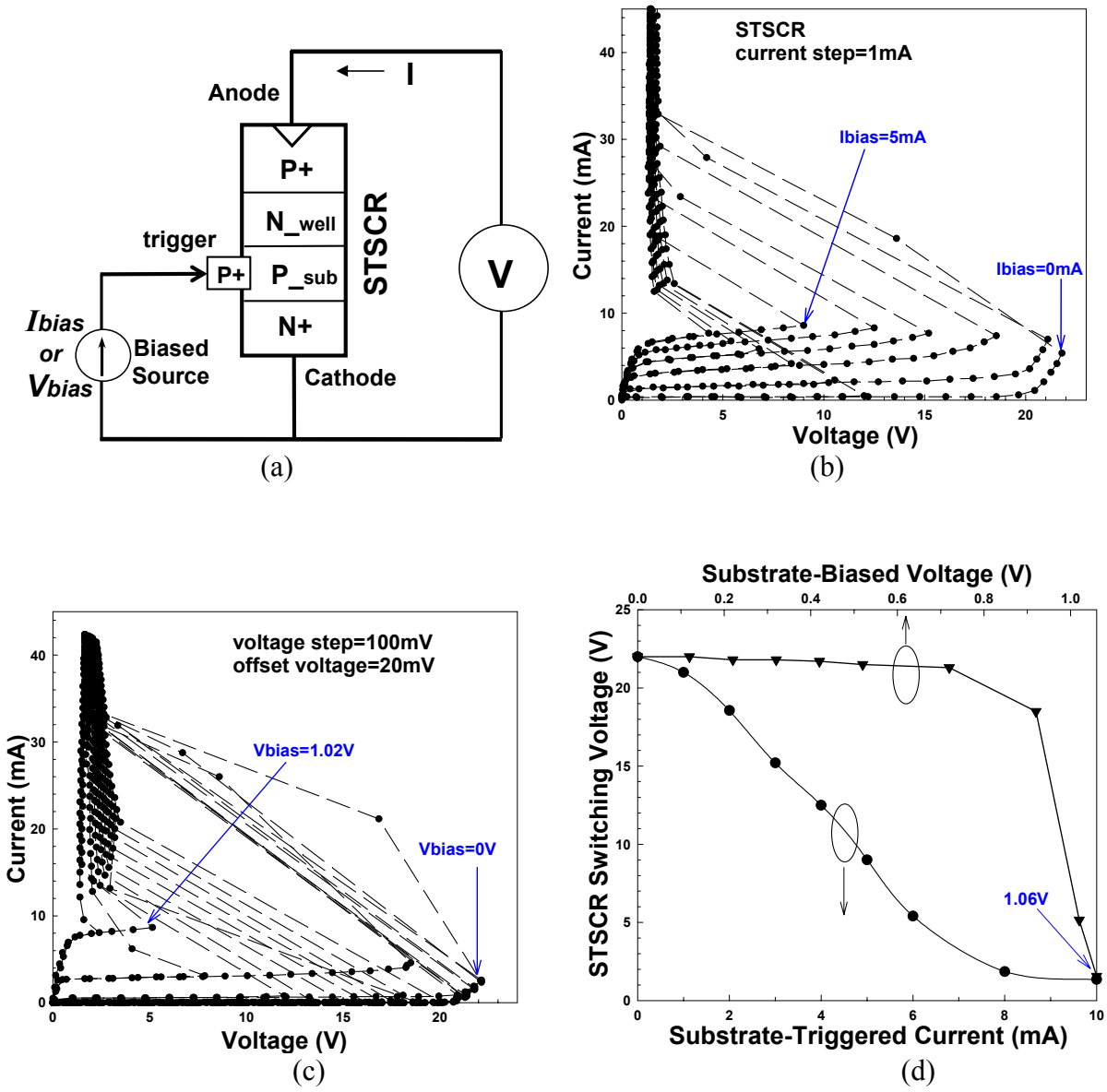
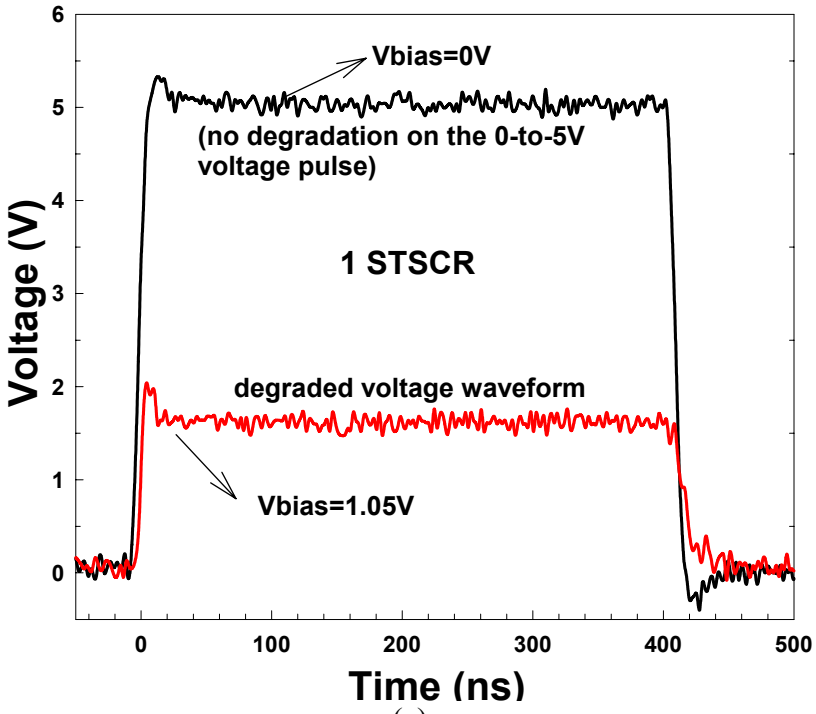
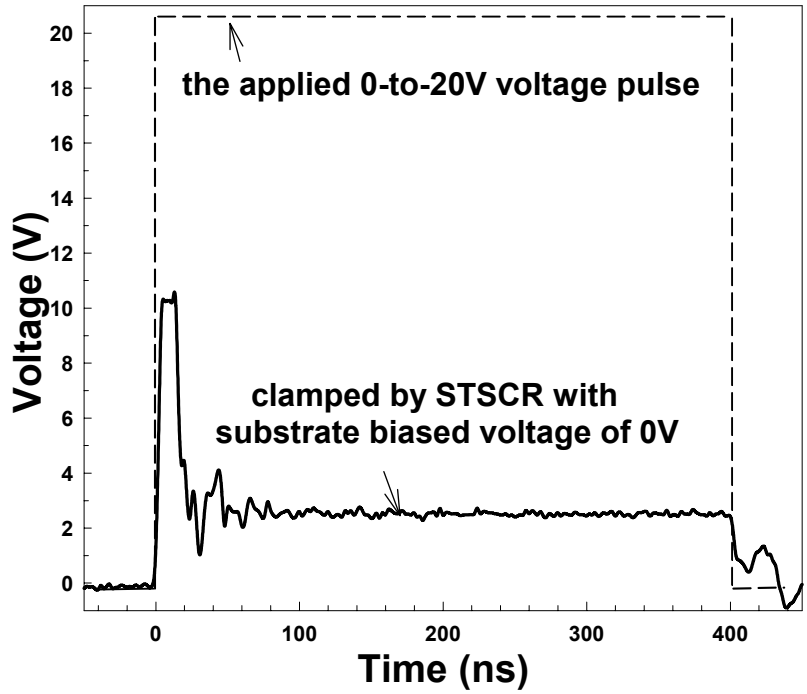


Fig. 2.2 (a) The experimental measurement setup used to measure the I-V curves of the STSCR device. The measured I-V curves of the STSCR device under (b) different substrate-triggered currents and (c) different substrate bias voltages. (d) The dependence of the switching voltage of the STSCR on the substrate-triggered current and substrate bias voltage in the STSCR device.



(a)



(b)

Fig. 2.3 (a) Under substrate bias of 0V and 1.05V, the measured voltage waveforms on the anode of STSCR device when a 0-to-5V voltage pulse is applied to the anode of the STSCR with the cathode grounded. (b) The measured voltage waveform on the anode, clamped by the stand-alone STSCR device when a 0-to-20V voltage pulse is applied to the anode with the cathode grounded.

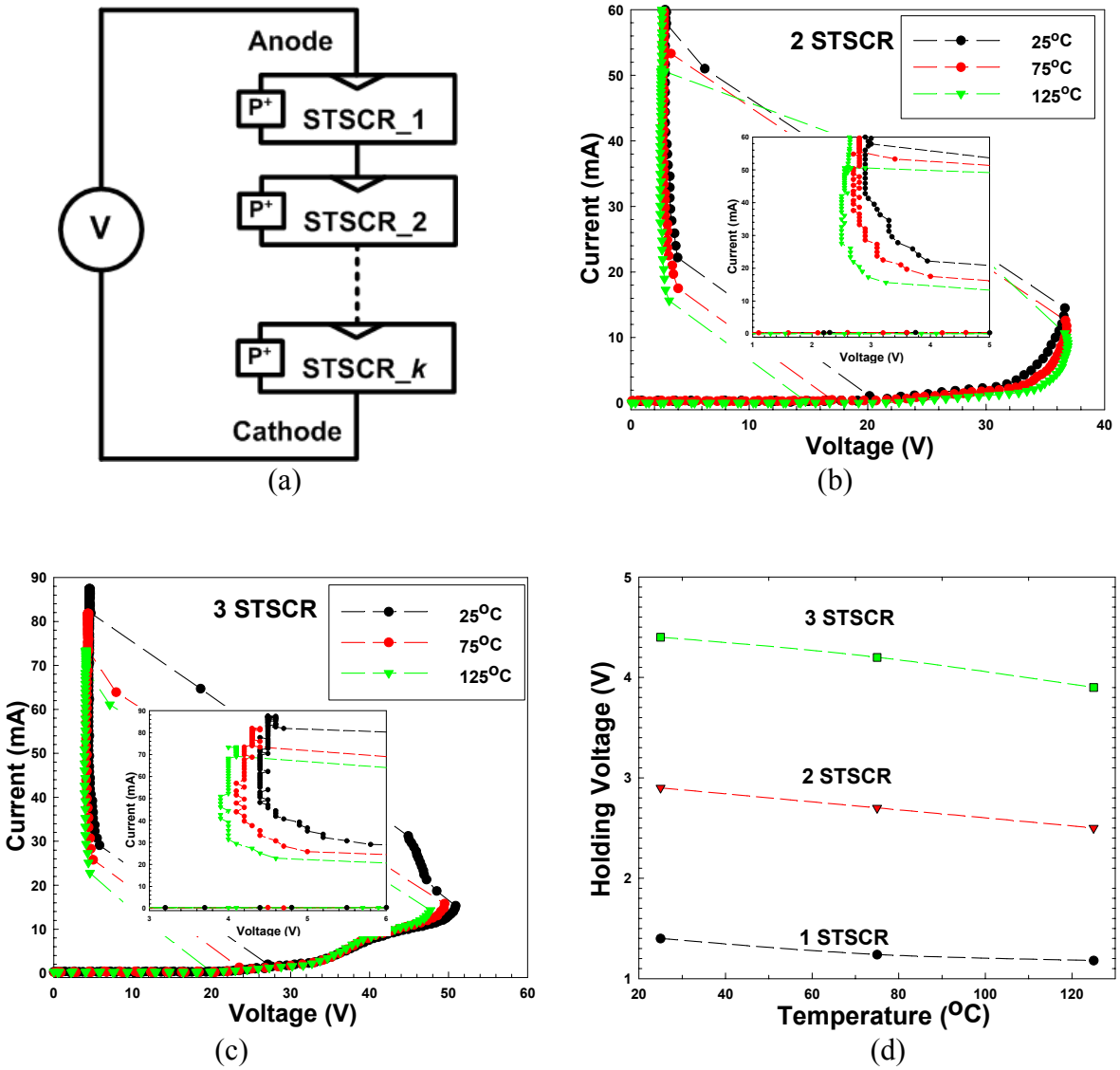
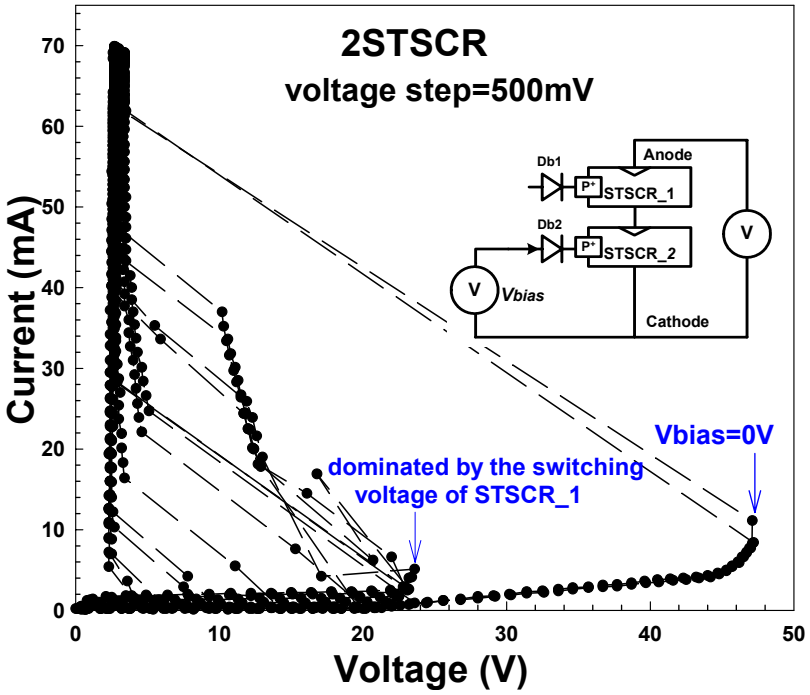
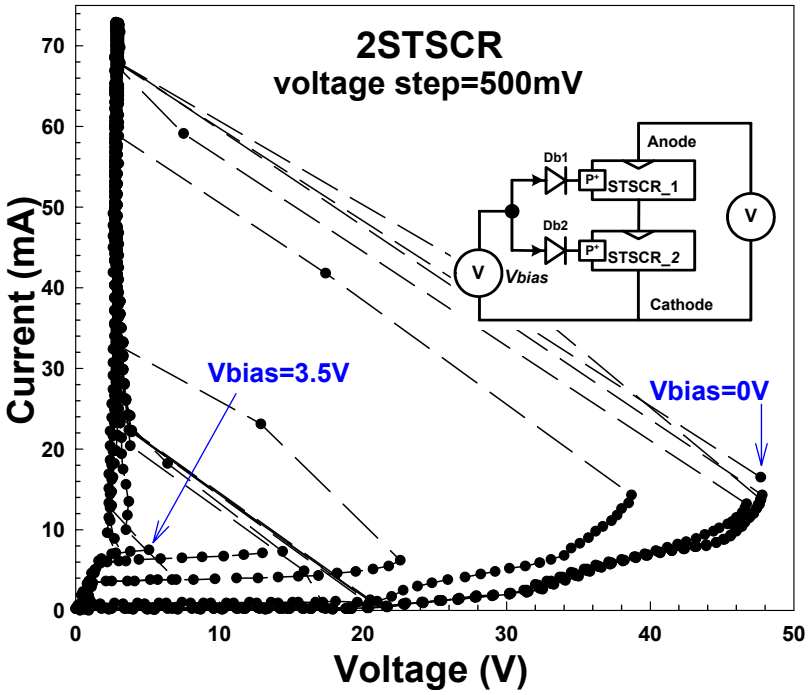


Fig. 2.4 The temperature dependence on the total holding voltage of the stacked STSCR devices with different stacked number. (a) Experimental measurement setup, (b) the measured I-V curves of two STSCR devices in stacked configuration (2STSCR), (c) the measured I-V curves of three STSCR devices in stacked configuration (3STSCR), and (d) the relation between the holding voltage and operating temperature under different number of stacked STSCR devices.

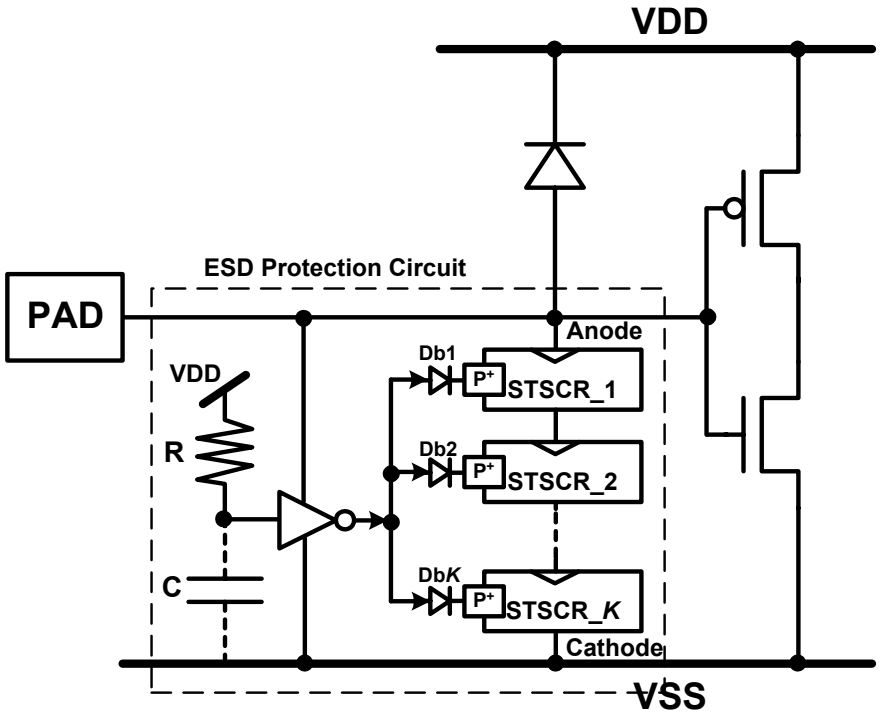


(a)

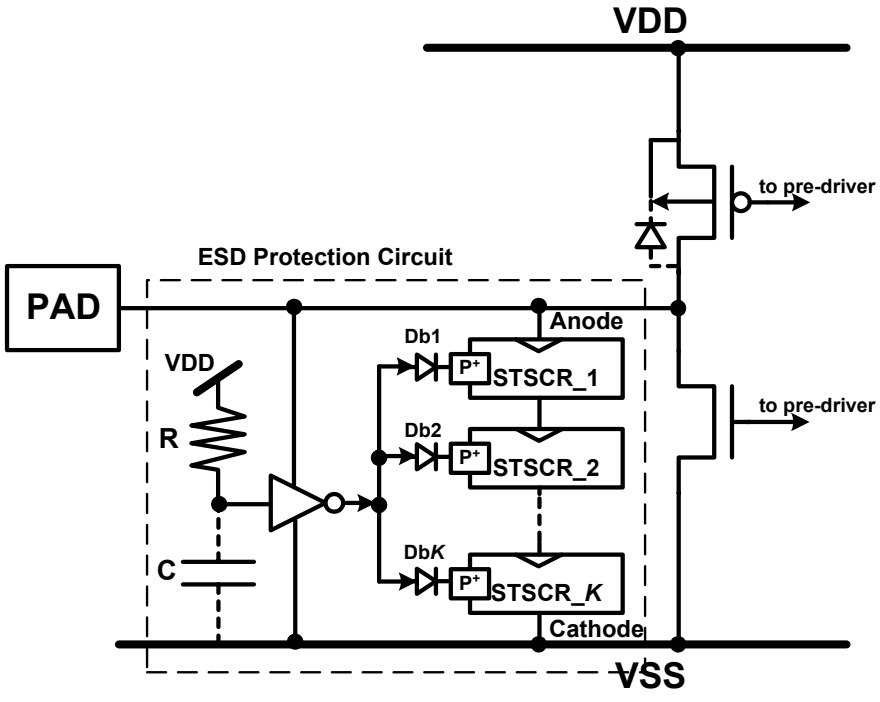


(b)

Fig. 2.5 The measured I-V curves of the two STSCR devices in stacked configuration (2STSCR) when the substrate bias voltages are applied to (a) only one trigger node, and (b) all trigger nodes.



(a)



(b)

Fig. 2.6 The ESD protection circuits for (a) the input pad, and (b) the output pad, by using the proposed STSCR devices in stacked configuration.

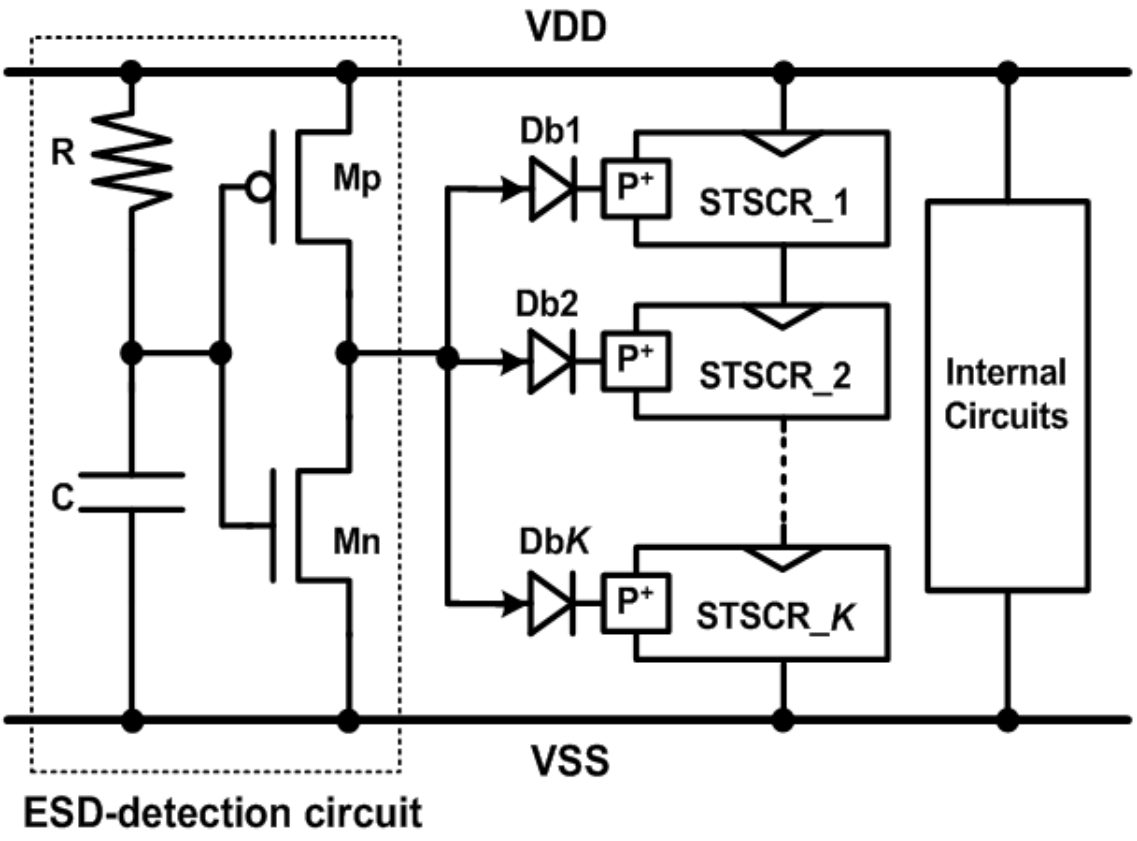


Fig. 2.7 The VDD-to-VSS ESD clamp circuit realized with the stacked STSCR devices.

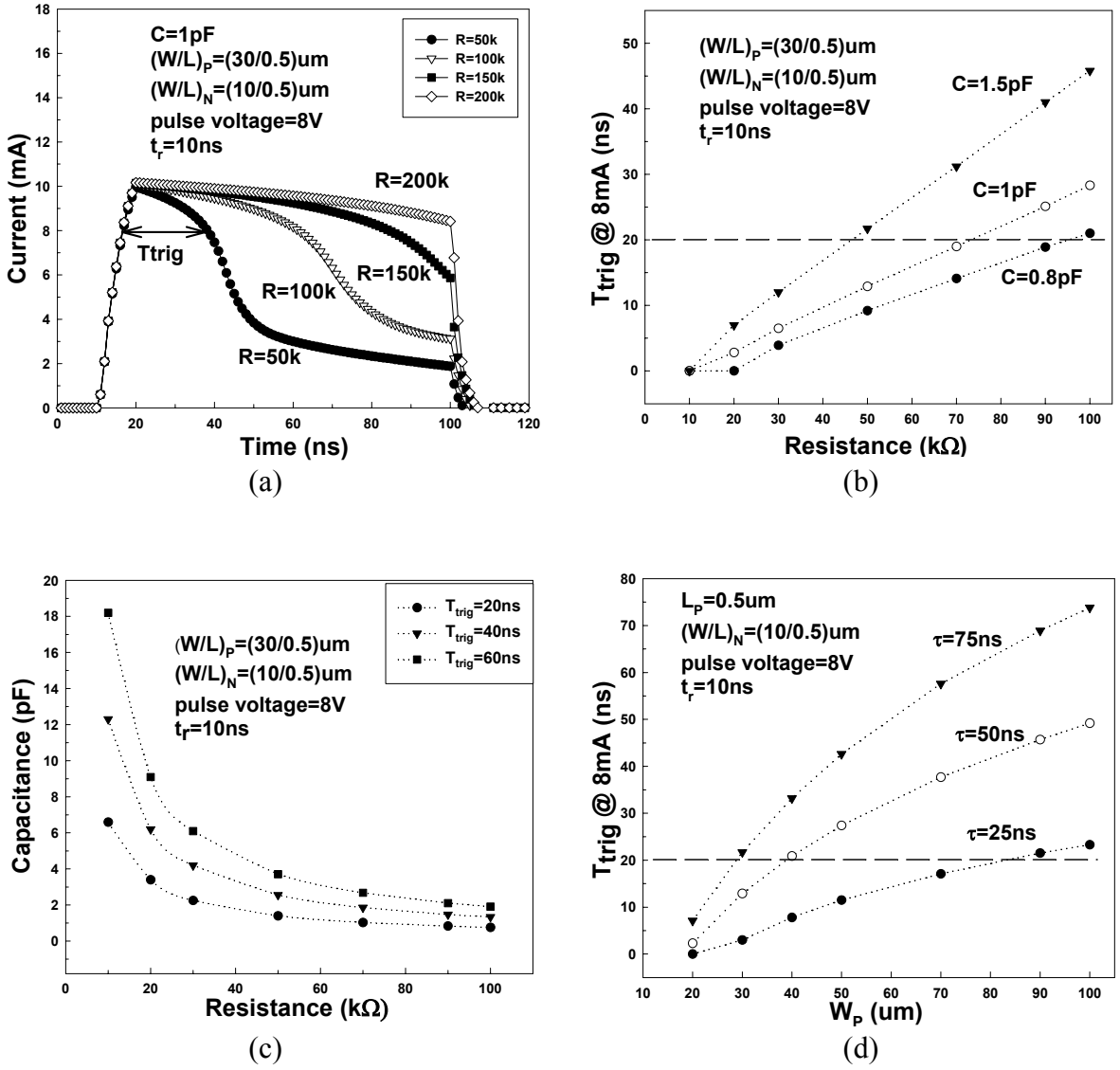
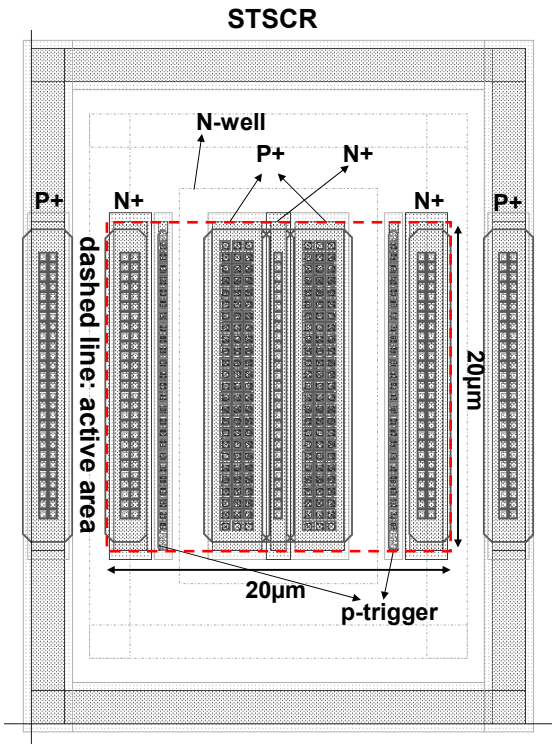
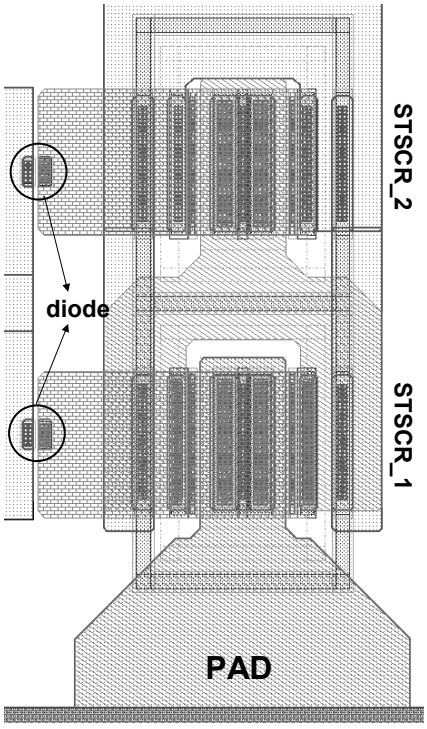


Fig. 2.8 HSPICE simulation. (a) The dependence of output current of ESD-detection circuit on time under different resistances. (b) The dependence of "Ttrig" on resistance under different capacitances. (c) The dependence of capacitance on resistance under different "Ttrigs". (d) The dependence of "Ttrig" on channel width of PMOS under different time constants.



(a)



(b)

Fig. 2.9 The layout views of (a) one substrate-triggered SCR (STSCR), and (b) two STSCR devices in stacked configuration (2STSCR) with blocking diodes.

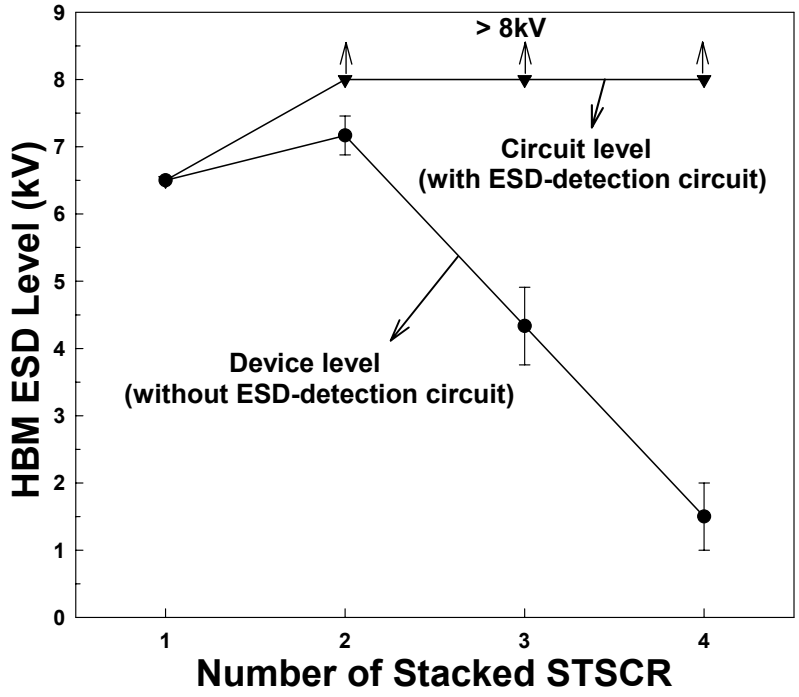


Fig. 2.10 Dependence of the HBM ESD levels of stacked STSCR configuration on the number of the stacked STSCR devices (Failure criterion: $I_{Leakage}$ > 1μA @ 2.5V bias).

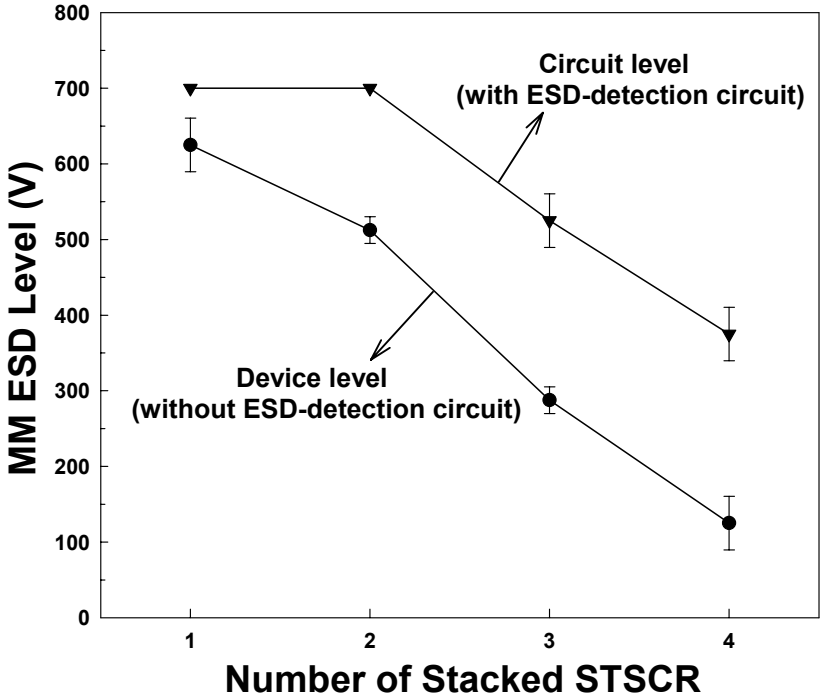


Fig. 2.11 Dependence of the MM ESD levels of stacked STSCR configuration on the number of the stacked STSCR devices (Failure criterion: $I_{Leakage}$ > 1μA @ 2.5V bias).

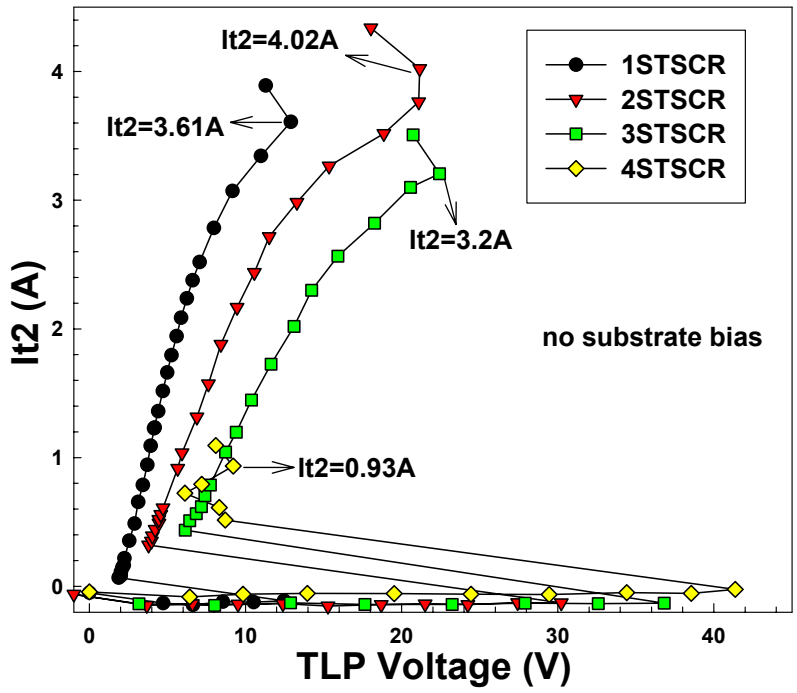


Fig. 2.12 The TLP-measured I-V curves of the stacked STSCR configuration without substrate bias under different numbers of the stacked STSCR devices.

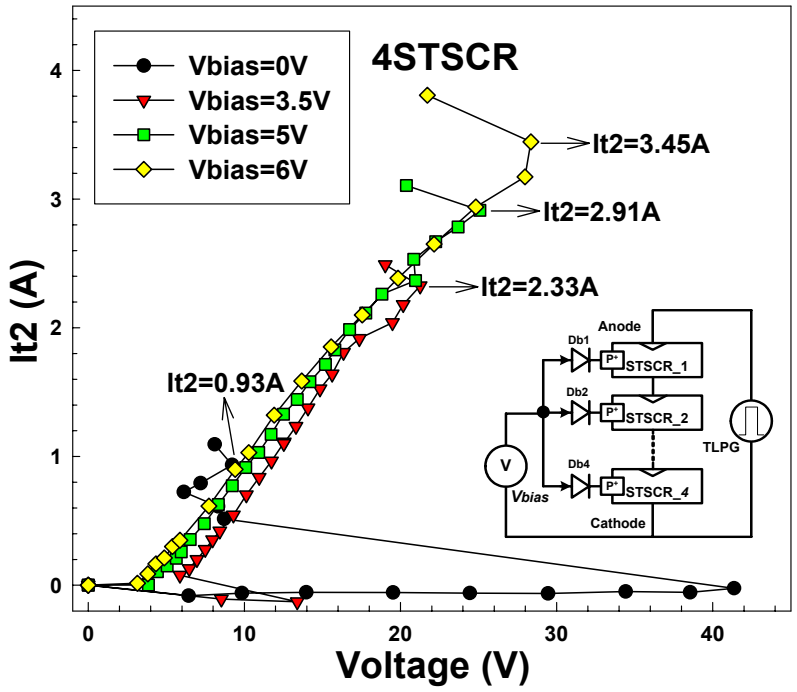


Fig. 2.13 The TLP-measured I-V curves of the four STSCR devices in stacked configuration (4STSCR) with different substrate bias voltages.

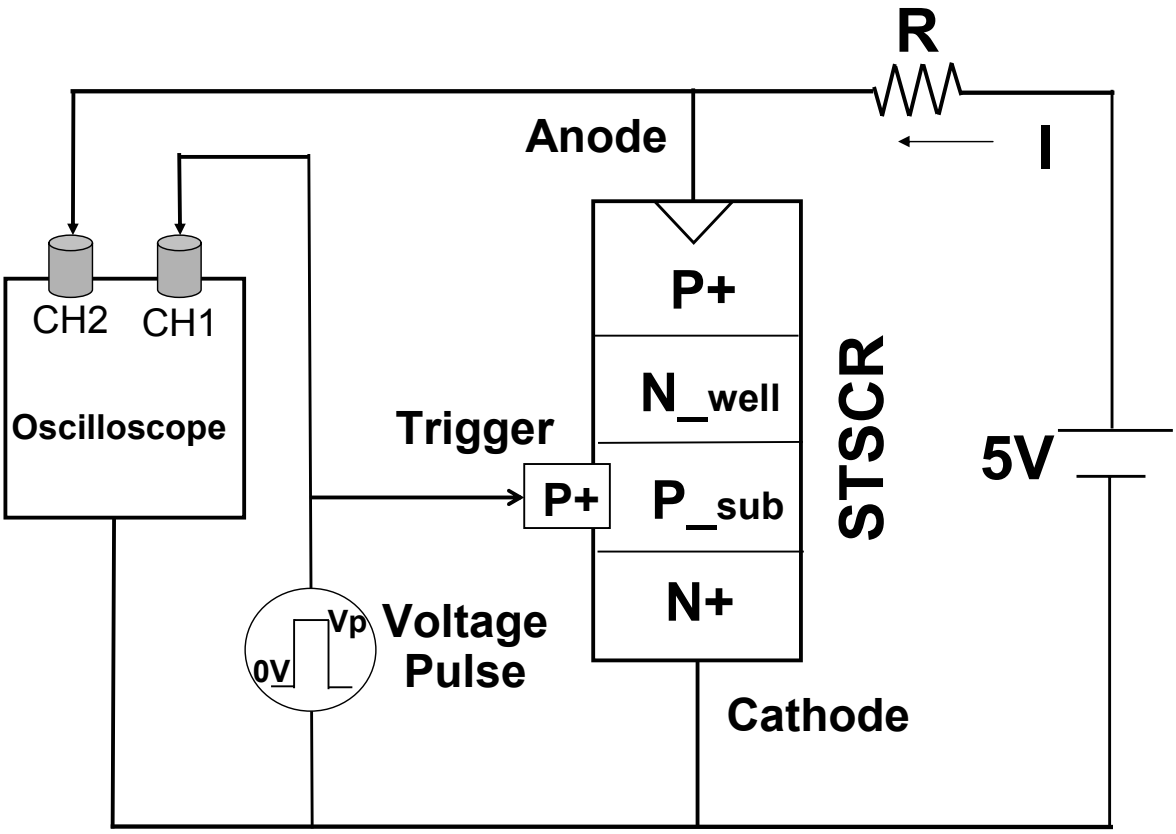


Fig. 2.14 Experimental setup to measure the turn-on time of one stand-alone STSCR device.

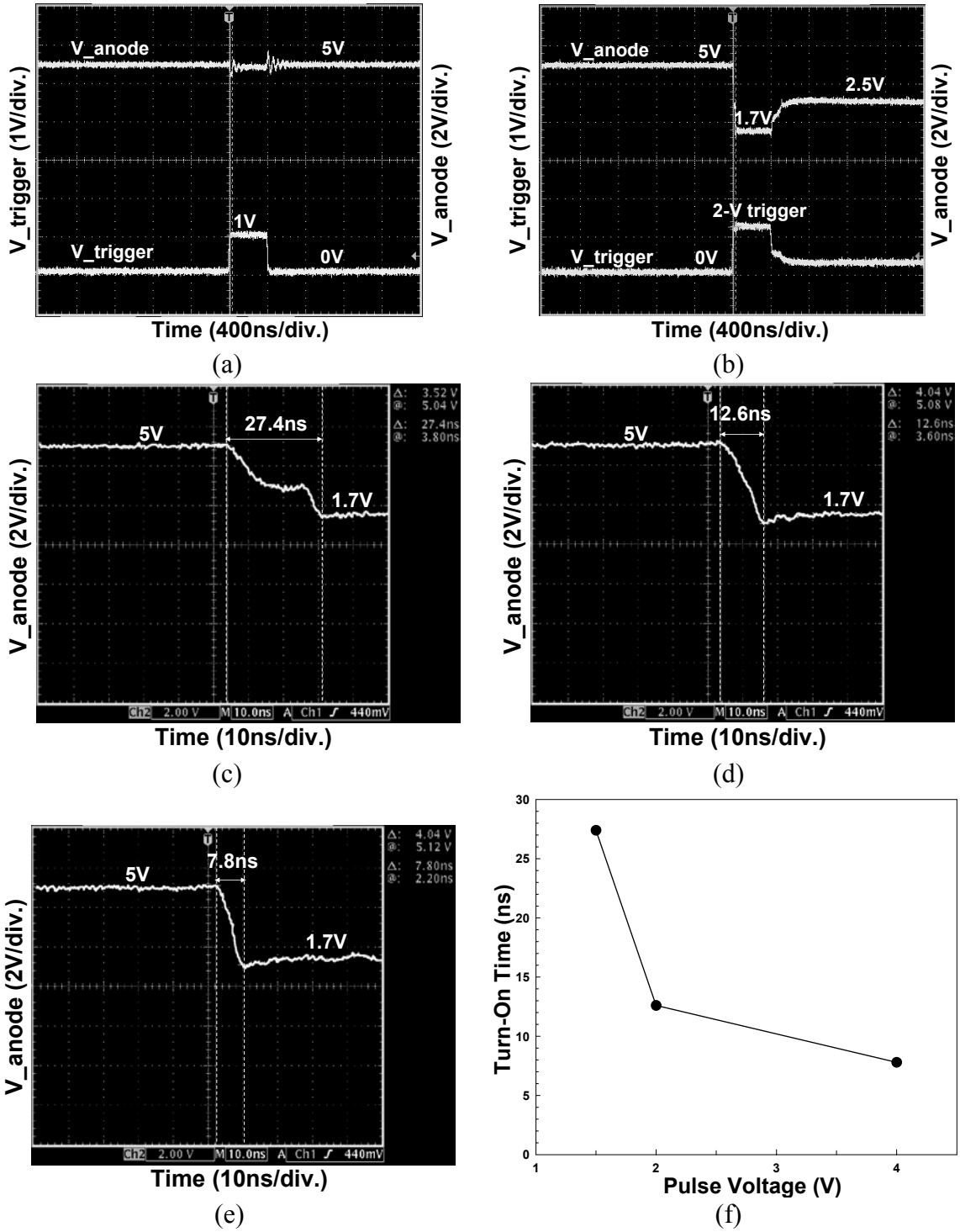


Fig. 2.15 The turn-on verification of STSCR device under different substrate biases. The measured voltage waveforms on the anode and trigger nodes of the STSCR device under (a) 1-V voltage triggering, and (b) 2-V voltage triggering. The close-up views of the V_anode at the falling edge while the STSCR is triggering by the voltage pulse of (c) 1.5V, (d) 2V, and (e) 4V into the P+ trigger node. (f) The relation between the turn-on time and the triggering pulse voltage.

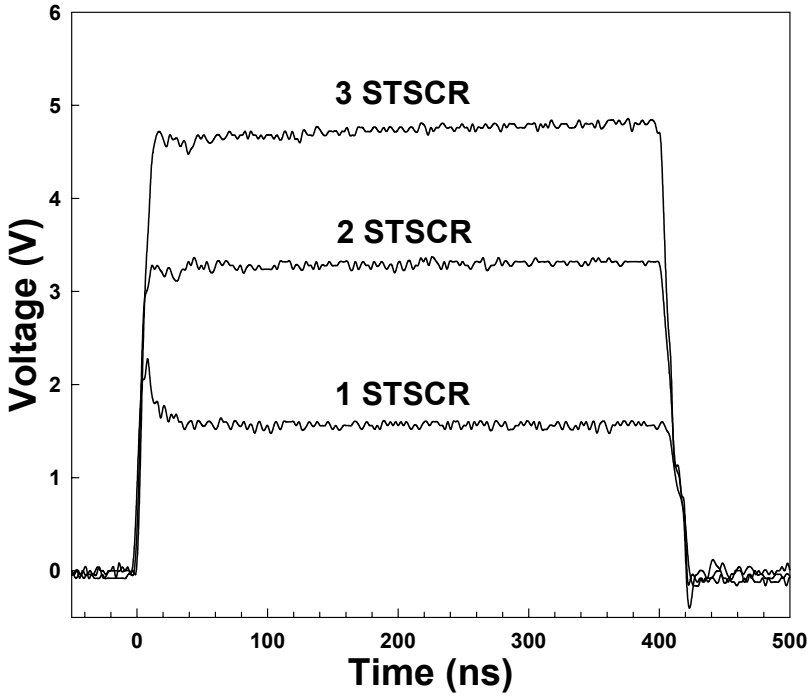


Fig. 2.16 The measured voltage waveforms on the VDD line, clamped by different stacked STSCR devices with ESD-detection circuit, when a 0-to-8V voltage pulse is applied to the VDD line of the VDD-to-VSS ESD clamp circuit with the VSS grounded.

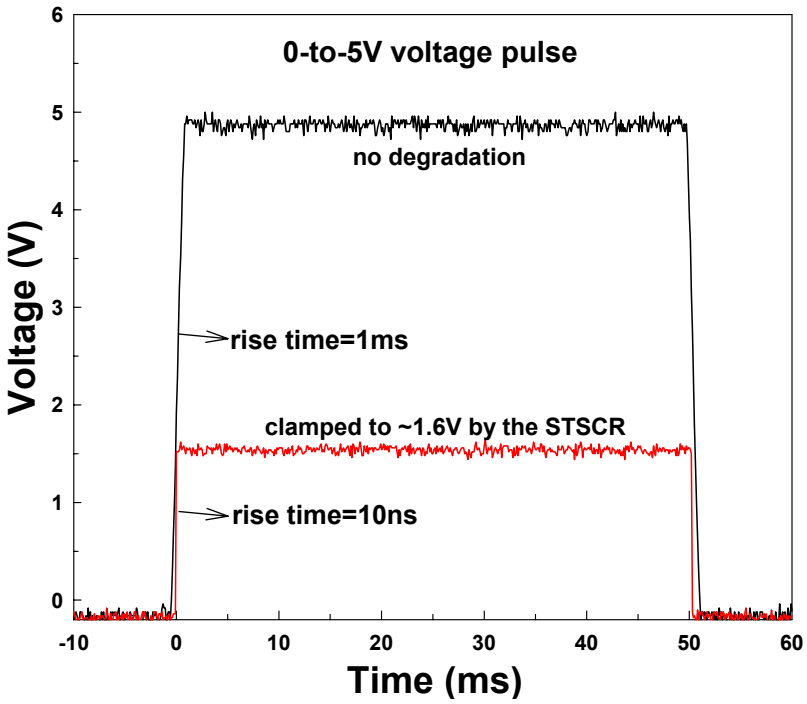


Fig. 2.17 The verification of ESD-detection function in the VDD-to-VSS ESD clamp circuit with one STSCR under the triggering of 0-to-5V voltage pulse with different rise time.

CHAPTER 3

DESIGN TECHNIQUE AND OPERATING PRINCIPLE OF ESD PROTECTION DESIGN WITH COMPLEMENTARY SUBSTRATE-TRIGGERED SCR DEVICES

In this chapter, latchup-free ESD protection circuits with complementary STSCR devices is designed to discharge both of the pad-to-VSS and pad-to-VDD ESD stresses. The design technique and the operating principles of the proposed ESD protection circuits with complementary STSCR devices are discussed. The real functions of these ESD protection circuits can be verified by the ESD-like voltage pulses generated from pulse generator. The latchup issue among the complementary STSCR devices can be successfully solved by increasing the total holding voltage with the stacked diode string. Such novel STSCR devices with stacked diode string are designed to be kept off during the normal circuit operating conditions, and to be quickly triggered on by substrate-triggered technique during the ESD-zapping conditions. The on-chip ESD protection circuits designed with such complementary STSCR devices and stacked diode string for input pad, output pad, and power rails have been successfully verified in a 0.25-μm salicided CMOS process [25], [26].

3.1 COMPLEMENTARY SUBSTRATE-TRIGGERED SCR DEVICES

3.1.1 Device Structure

The proposed device structures of P_STSCR and N_STSCR devices with stacked diode string are shown in Figs. 3.1(a) and 3.1(b), respectively. The SCR paths in the P_STSCR and N_STSCR devices are indicated by the dashed lines shown in Figs. 3.1(a) and 3.1(b), respectively. The purpose of the additional N-well region under the N+ diffusion at the end of the SCR path is used to further enhance the turn-on speed of the complementary STSCR devices for more effective ESD protection with the substrate-triggered technique, because

they increase the equivalent substrate resistance (Rsub) in these device structures.

The required number of diodes in the stacked diode string is dependent on the power supply voltage level of CMOS ICs in applications. To avoid the latchup issue, the total holding voltage must be designed greater than the maximum voltage level of VDD. The total holding voltage (Vh) of the P_STSCR or N_STSCR device with k-stacked diodes can be written as:

$$Vh = Vh_{\_SCR} + (k \times V_D), \tag{3.1}$$

where $Vh_{\_SCR}$ is the holding voltage (~1.5 V) of single P_STSCR (or N_STSCR) device and V_D is the cut-in voltage (~0.6 V) of a diode in forward-biased condition.

3.1.2 I-V Characteristics of the STSCR Devices

The P_STSCR and N_STSCR devices with different numbers of stacked diodes have been drawn in layout and fabricated in a 0.25-μm salicided CMOS process. The experimental setups to measure the DC I-V characteristics of the P_STSCR and N_STSCR devices are illustrated in Figs. 3.2(a) and 3.3(a), respectively. The measured DC I-V characteristics of stand-alone P_STSCR and N_STSCR devices are shown in Figs. 3.2(b) and 3.3(b), respectively. When the P_STSCR device has no substrate-triggered current (Ibias=0), the P_STSCR is turned on by its original N-well / P-substrate junction avalanche breakdown. In Fig. 3.2(b), the original switching voltage of the P_STSCR device is as high as 22 V, when the substrate-triggered current is zero. But, the switching voltage of the P_STSCR device is reduced to 9 V, when the substrate-triggered current is 5 mA. Furthermore, the switching voltage of the P_STSCR device can be reduced to only 1.85 V, when the substrate-triggered current is increased up to 8 mA. The DC I-V curves of N_STSCR device, as shown in Fig. 3.3(b), are similar to those of the P_STSCR device. The dependences of switching voltage of the P_STSCR and N_STSCR devices on the substrate-triggered / well-triggered current are shown in Figs. 3.4(a) and 3.4(b), respectively. The higher trigger current leads to a much lower switching voltage in the complementary STSCR devices. Without involving the avalanche breakdown mechanism, the P_STSCR and N_STSCR devices can be effectively triggered on by applying the substrate-triggered technique. With a much lower switching voltage, the turn-on speed of the P_STSCR / N_STSCR device can be further improved to quickly discharge ESD current. This is a very excellent feature for the proposed

complementary STSCR devices used to protect the thinner gate oxide of input circuits in sub-quarter-micron CMOS processes.

Due to the parasitic silicon controlled rectifier (SCR) path, transient-induced latchup phenomenon has been an inherent concern for bulk CMOS ICs when the IC is operating under normal circuit operations. To avoid the latchup issue, the total holding voltage of the ESD protection device must be designed greater than the maximum voltage level of VDD during the normal circuit operating conditions. This can be achieved by the complementary STSCR devices with stacked diode string in the ESD protection circuits. The DC I-V curves of the P_STSCR and N_STSCR devices with different numbers of stacked diodes are measured in Figs. 3.5(a) and 3.5(b), respectively. The corresponding measurement setups are inset into Figs. 3.5(a) and 3.5(b), respectively. The total holding voltages of the complementary STSCR devices with stacked diode string can be raised up by increasing the number of stacked diodes. The holding voltages of the complementary STSCR devices with 1, 2, 4, and 6 diodes at the temperature of 25^{o}C are 2.6, 3.2, 4.6, and 5.8 V, respectively. The switching voltages of complementary STSCR devices with stacked diode string shown in Fig. 3.5 have a little increase when increasing the number of stacked diodes, but they can be reduced by the substrate-triggered technique to provide the effective ESD protection. Figs. 3.6(a) and 3.6(b) show the I-V curves of the P_STSCR and N_STSCR with 6 diodes under different substrate or well triggered currents, respectively. With the substrate-triggered technique, the switching voltages of the P_STSCR and N_STSCR with 6 diodes can be significantly reduced. Thus, the proposed P_STSCR / N_STSCR with stacked diode string have the adjustable holding voltage and controllable switching voltage, so they can provide effective ESD protection for internal circuits as well as avoid the transient-induced latchup issue.

For the precise design of the ESD protection circuits, the device characteristics of complementary STSCR devices must be calibrated under different temperatures. The DC I-V curves of a P_STSCR with 4 diodes and an N_STSCR with 6 diodes under different temperatures are measured in Figs. 3.7(a) and 3.7(b), respectively. The insets in Figs. 3.7(a) and 3.7(b) are the enlarged views around the holding point for clearly observing. The holding voltages of the P_STSCR with 4 diodes at the temperatures of 25 ^{o}C, 75 ^{o}C, and 125 ^{o}C are 4.6, 4.1, and 3.85 V, respectively. The dependences of the total holding voltage of the P_STSCR and N_STSCR with stacked diode string on the number of stacked diodes under

different temperatures are shown in Figs. 3.8(a) and 3.8(b), respectively. With increase of the number of stacked diodes, the holding voltages of such ESD protection devices are increased. The total holding voltages slightly reduce when the temperature is increased, because the current gain (β) of the parasitic bipolar transistor in the SCR device is enhanced with the increase of temperature. For safe applications in 2.5-V CMOS ICs, two diodes are suggested to be stacked with the P_STSCR or N_STSCR devices in the ESD protection circuits to avoid the latchup issue under normal circuit operating conditions.

3.2 ON-CHIP ESD PROTECTION CIRCUITS WITH COMPLEMENTARY STSCR DEVICES

3.2.1 ESD Protection Circuit for the Input/Output Pads

Two kinds of ESD protection designs for I/O pad, realized with the complementary substrate-triggered SCR devices with stacked diode string, are shown in Figs. 3.9(a) and 3.9(b). In Fig. 3.9(a), the principle of RC delay is used to distinguish ESD-zapping events or the normal circuit operating conditions. In Fig. 3.9(b), the gate-coupled circuit technique is used to generate the trigger current to turn on the complementary STSCR devices during ESD-zapping conditions.

In Fig. 3.9(a), the p-trigger (n-trigger) node of the P_STSCR (N_STSCR) device is connected to the output of the inv_1 (inv_2). The input of the inv_1 (inv_2) is connected to VDD (VSS) through the resistor R1 (R2), which is better realized by the N+ diffusion resistance for the concern of antenna effect [55]. The resistors R1 and R2 can be shared with every I/O pad to save the layout area in the CMOS IC. A capacitor C1 (C2) is placed between the input of the inv_1 (inv_2) and VSS (VDD). These capacitors can be formed by the parasitic capacitors at the input node of the inverter. Besides, there are two parasitic diodes (Dp_1 and Dn_1) in this ESD protection circuits. The Dp_1 is the source-to-N-well (VDD) parasitic diode of PMOS in the inv_1. The Dn_1 is the source-to-P-sub (VSS) parasitic diode of NMOS in the inv_2.

In the normal circuit operating conditions with VDD and VSS power supplies, the input of inv_1 is biased at VDD. Therefore, the output of the inv_1 is biased at VSS due to the turn

on of NMOS in the inv_1, whenever the input signal is logic high (VDD) or logic low (VSS). The p-trigger node of the P_STSCR device is kept at VSS by the output of the inv_1, so the P_STSCR device is guaranteed to be kept off in the normal circuit operating conditions. The input node of inv_2 in the normal operating conditions is biased at VSS. Thus, the output of the inv_2 is kept at VDD due to the turn on of the PMOS in the inv_2, whenever the input signal is high or low. The n-trigger node of the N_STSCR device is biased at VDD by the output of the inv_2, so the N_STSCR is also guaranteed to be kept off in the normal circuit operating conditions. To avoid the noise transient-induced latchup issue on such P_STSCR or N_STSCR devices under normal circuit operating conditions, the total holding voltage of the ESD protection device must be designed greater than the power supply voltage or maximum voltage level of input signals. By changing the number of stacked diodes, the total holding voltage can be adjusted to meet different circuit applications.

An ESD energy applied on a pad may have the positive or negative voltage with reference to grounded VDD or VSS, so there are four modes of ESD stresses at each I/O pad of CMOS IC products. The four modes of ESD stresses are PS, NS, PD, and ND modes [18], [19]. To clearly comprehend the ESD current paths under these ESD stresses, the equivalent circuit of the ESD protection circuit designed by complementary STSCR devices and stacked diode string for I/O pads is illustrated in Fig. 3.10. The Dn_2 is the N-well to P-sub (VSS) parasitic diode in diode Db_*k* structure. The Dp_2 is the P+ to N-well parasitic diode in the P_STSCR device structure.

Under the PS-mode ESD-zapping condition (with grounded VSS but floating VDD), the input of the inv_1 is initially floating with a zero voltage level, thereby the PMOS of the inv_1 will be turned on due to the positive ESD voltage on the pad. So, the output of the inv_1 is charged up by the ESD energy to generate the trigger current into the p-trigger node of the P_STSCR device. Therefore, the P_STSCR device is triggered on and the ESD current is discharged from I/O pad to the grounded VSS pin through the P_STSCR device with stacked diode string. The RC time constant is designed to keep the input of the inv_1 at a relatively low voltage level during ESD stress condition, which can be finely tuned by HSPICE simulation.

Under the ND-mode ESD-zapping condition (with grounded VDD but floating VSS), the input of the inv_2 is initially floating with a zero voltage level, thereby the NMOS of the inv_2 will be turned on due to the negative ESD voltage on the pad. So, the output of the

inv_2 is pulled down by the negative ESD voltage to draw the trigger current out from the n-trigger node of the N_STSCR device. Therefore, the N_STSCR device is triggered on and the negative ESD current is discharged from I/O pad to the grounded VDD pin through the N_STSCR device with stacked diode string.

Under the NS-mode (PD-mode) ESD-zapping condition, the parasitic diodes Dn_1 and Dn_2 (Dp_1 and Dp_2) are forward biased and turned on to discharge the ESD current from I/O pad to the grounded VSS (VDD). Thus, the four modes (PS, NS, PD, and ND) of ESD stresses can be clamped to a very low voltage level by the P_STSCR with stacked diode string, Dn_1 and Dn_2, Dp_1 and Dp_2, and N_STSCR with stacked diode string, so the thin gate oxide in deep sub-quarter-micron CMOS technologies can be fully protected from any ESD stresses. In addition, the ESD level of an I/O pin is dominated by the weakest ESD current path, so the experimental measurements in the following are focused on the PS-mode and ND-mode ESD-zapping conditions.

Fig. 3.9(b) shows another ESD protection circuit designed with the complementary STSCR devices with stacked diode string for the I/O pad. When a PS-mode ESD zapping on the pad, the positive transient voltage on the pad is coupled through the capacitor C1 to the gate of NMOS Mn. The Mn with a positive coupled gate bias can be turned on first to conduct some ESD current from I/O pad into the p-trigger node of the P_STSCR device. Therefore, the P_STSCR is triggered on to discharge the ESD current from I/O pad to the grounded VSS line. When an ND-mode ESD zapping on the pad, the negative transient voltage on the pad is coupled through the capacitor C2 to the gate of PMOS Mp. The Mp with a negative coupled gate bias can be turned on first to draw some ESD current out from the n-trigger node of the N_STSCR device. Therefore, the N_STSCR is triggered on to discharge the negative ESD current from I/O pad to the grounded VDD line. When the NS-mode (PD-mode) ESD zapping on the pad, the ESD current can be bypassed through the forward-biased parasitic diodes Dn_2 and Dn_3 (Dp_2 and Dp_3) to grounded VSS (VDD). The Dn_3 (Dp_3) is the parasitic diode in the drain of Mn (Mp) to the P-sub (N-well). During normal circuit operating conditions, the gate of Mn (Mp) is biased at VSS (VDD) through the resistor R1 (R2). So, the Mn (Mp) is kept off and no trigger current will be applied to the trigger node of P_STSCR (N_STSCR). The proposed ESD protection circuits are designed to be inactive without interrupting the normal input or output signals during normal circuit operating conditions. The capacitance values of C1 and C2 in Fig. 3.9(b) must be tuned at

some value, where the coupled voltage under normal circuit operating conditions is smaller than the threshold voltage of Mn / Mp, but greater than the threshold voltage of Mn / Mp under ESD zapping conditions [38].

3.2.2 ESD Clamp Circuit between the Power Rails

The P_STSCR / N_STSCR devices can be also applied to design the power-rail ESD clamp circuits. The VDD-to-VSS ESD clamp circuits realized with the P_STSCR or N_STSCR device and the stacked diode string are shown in Figs. 11(a) and 11(b), respectively. The functions of the ESD-detection circuit, which is formed with resistor, capacitor, and inverter, is similar to that used in the I/O pad, but the RC value is designed with a time constant of about ~1μs to distinguish the VDD power-on event (with a rise time of ~ms) or ESD stress events (with a rise time of ~ns) [11]. During the normal VDD power-on transition (from low to high), the input of the inverter in Fig. 11(a) can follow up in time with the power-on VDD signal to keep the output of the inverter at zero. Hence, the P_STSCR device with stacked diode string are kept off, and do not interfere the functions of internal circuits.

When a positive ESD voltage is applied to VDD line with VSS line relatively grounded, the RC delay will keep the input of the inverter at a low voltage level for a relatively long time. Therefore, the output of the inverter will be pulled high by the ESD energy itself to trigger on the P_STSCR device. While the P_STSCR device is triggered on, the ESD current is discharged from VDD line to VSS line through the P_STSCR device and the stacked diode string. With such a suitable ESD-detection circuit, the P_STSCR device can be quickly triggered on to discharge the ESD current.

In Fig. 11(b), during the normal VDD power-on transition, the input of the inv_1 will be biased at VDD, so the output of the inv_1 (the input of the inv_2) will be biased at zero to keep the output of the inv_2 at VDD. Therefore, the N_STSCR device with stacked diode string are kept off and do not interfere the functions of internal circuits. However, when a positive ESD voltage is applied to VDD line with VSS line relatively grounded, the RC delay will keep the input of the inv_1 at a low voltage level for a relatively long time. The output of the inv_1 (the input of the inv_2) will become high, and then the output of the inv_2 will be kept at a low voltage level to trigger on the N_STSCR device. While the N_STSCR device is

triggered on, the ESD current is discharged from VDD line to VSS line through the N_STSCR device and the stacked diode string. When a negative ESD voltage is applied to VDD line with VSS line relatively grounded, the negative ESD current can be discharged from VDD line to VSS line through the forward-biased P-sub (VSS)-to-N-well (which is connected to VDD) parasitic diode. In addition, by adjusting the number of stacked diodes, such power-rail ESD clamp circuits can be designed free to latchup issue.

3.3 EXPERIMENTAL RESULTS

3.3.1 ESD Robustness

The proposed ESD protection devices and circuits for the I/O and the power pads have been fabricated in a 0.25-μm salicided CMOS process without using the additional silicide-blocking mask / process option. The layout examples of the P_STSCR device with two stacked diodes and the N_STSCR device with three stacked diodes are shown in Figs. 3.12(a) and 3.12(b), respectively. The device dimensions of the fully silicided P_STSCR and N_STSCR are drawn as 20 μm×20 μm, and each diode has a 30 μm×3 μm anode layout area. The human-body-model (HBM) and machine-model (MM) ESD stresses are used to verify the ESD levels of the proposed ESD protection circuits designed with the complementary STSCR devices and different numbers of the stacked diodes. The HBM and MM ESD test results of the P_ STSCR / N_STSCR with stacked diode string are compared in Figs. 3.13(a) and 3.13(b), respectively. In this ESD verification, the failure criterion is defined as the leakage current of the device after ESD zapping is greater than 1 μA under the normal operating voltage of 2.5 V. The HBM (MM) ESD levels of the P_STSCR / N_STSCR with stacked diode string have a little degradation while the number of stacked diodes is increased. The ESD-generated power across the ESD protection device can be calculated as power ≅ $I_{ESD} \times Vh$. Thus, the HBM and MM ESD levels are decreased in principle when the total holding voltage is increased. But, the stacked diode string with the parasitic vertical p-n-p BJT structures will also generate the extra current paths. These extra current paths can be also used to discharge the ESD current. So, the HBM and MM ESD levels of the P_STSCR / N_STSCR with stacked diode string can be almost kept at the same value. For IC

applications with power supply of 2.5 V, the ESD protection circuit can be designed free to latchup issue even if the operating temperature is up to 125 ^{o}C, when the number of stacked diodes is two. The complementary STSCR devices with two stacked diodes can still sustain the HBM (MM) ESD level of 7.25 kV (500 V). The ESD levels of substrate-triggered SCR devices are the same as that of the traditional SCR device under the same layout area. The aims of this design are to reduce the switching voltage, to avoid the transient-induced latchup issue, and to enhance the turn-on speed of the SCR device.

By comparison, a gate-grounded NMOS (GGNMOS) device with (W/L)=200/0.5 had been fabricated in the same CMOS process with additional silicide-blocking mask. Such GGNMOS occupied a layout area of 25.8 μm×60 μm can sustain the HBM ESD level of 3.5 kV. This has verified the excellent area efficiency of the ESD protection circuits realized with the proposed complementary STSCR devices (8 V/μm^2 for complementary STSCR with two stacked diodes, but 2.71 V/μm^2 for GGNMOS).

3.3.2 Turn-On Verification

The comparison of turn-on speed between P_STSCR and LVTSCR [17] under an applied 0-to-8 V voltage pulse is shown in Fig. 3.14. The device dimension W/L of inserted NMOS in LVTSCR structure is 40/0.25, and the device area of P_STSCR is the same as that shown in Fig. 3.12(a). The 8-V voltage pulse can be faster clamped to a stable low voltage level by the P_STSCR with 1.5-V substrate bias than by the LVTSCR. Therefore, the STSCR with enough substrate bias is more suitable to protect the ultra-thin gate oxide of input stage against ESD overstresses, as compared with LVTSCR device. In addition, the dependence of the turn-on time of STSCR device on the substrate bias is shown in Fig. 2.15.

The ESD protection circuits are kept “off” under normal circuit operating conditions and triggered “on” under ESD zapping conditions. In order to verify the functions of the ESD protection circuit for I/O pad, a 2.5-V voltage pulse with a pulse width of 400ns and a rise time of 10 ns is applied to the I/O pad in Fig. 3.9(a), where only one P_STSCR / N_STSCR device is placed between the I/O pad and VSS / VDD in this verification. In this experimental measurement, the ESD-detection circuit including R, C, and inverter is realized with R=100 kΩ, C=3 pF, PMOS dimension W/L=50/0.5, and NMOS dimension W/L=30/0.5. The channel length of NMOS / PMOS in the ESD-detection circuit can be reduced to gain the higher

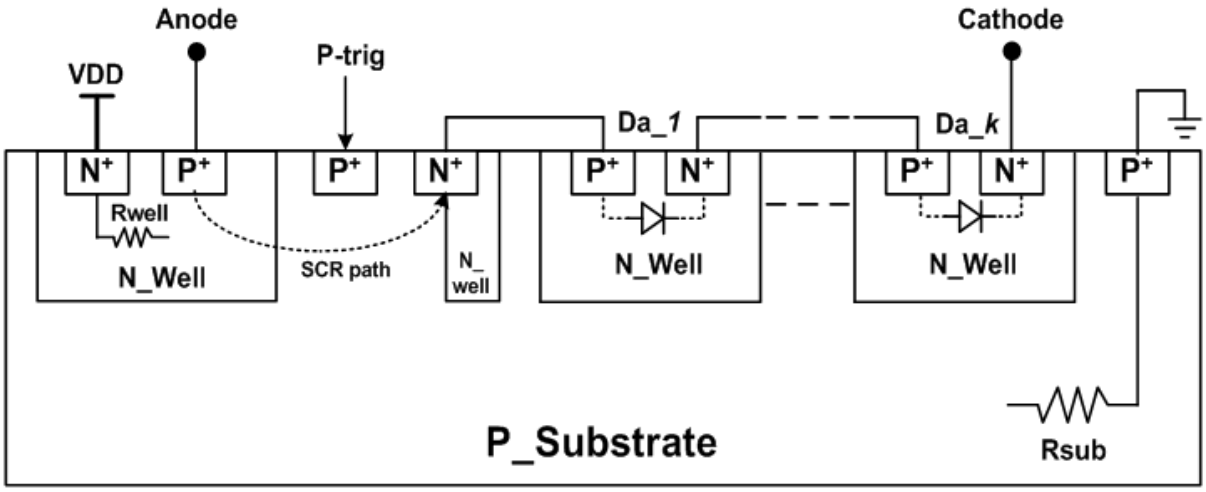
triggered currents. These device dimensions can be fine tuned by HSPICE simulator to fit different circuit applications, as shown in Fig. 2.8. During the normal circuit operating conditions, where the VDD is power-on and VSS is connected to ground, the input signal of 2.5 V has no degradation, as shown in Fig. 3.15(a). So, the ESD protection circuit do not interfere the input signal. However, during PS-mode ESD-zapping condition, the ESD-detection circuit is active, so the applied voltage pulse of 2.5V is clamped to ~1.2V by the turned-on P_STSCR, as shown in Fig. 3.15(b). During ND-mode ESD-zapping condition, a -2.5-V voltage pulse is clamped to ~ -1.26V by the turned-on N_STSCR, as shown in Fig. 3.15(c). By using this method, the turn-on characteristics of the ESD protection circuit for I/O pad shown in Fig. 3.9(b) can be also verified in Fig. 3.16. In this measurement, the ESD detection circuit including C, R, and NMOS / PMOS is realized with C=96 fF, R=10 kΩ, NMOS dimension W/L=30/0.5, and PMOS dimension W/L=50/0.5. When a positive 0-to-7V voltage pulse to simulate the PS-mode ESD-zapping condition is applied to the I/O pad of ESD protection circuit in Fig. 3.9(b), the voltage waveform on the I/O pad is clamped to a low voltage level measured in Fig. 3.16(a). In Fig. 3.16(a), the NMOS, Mn in the ESD protection circuit of Fig. 3.9(b), will be first turned on to conduct some ESD current to trigger on the P_STSCR device, and then the P_STSCR clamps the voltage to 1.8 V. If the pulse voltage is increased to 10 V shown in Fig. 3.16(b), the turn-on time of Mn can be shortened and the P_STSCR can be triggered on into latching state more quickly. In Fig. 3.16(c), when a negative 0-to-10 V voltage pulse to simulate the ND-mode ESD-zapping condition is applied to the I/O pad of ESD protection circuit in Fig. 3.9(b), the voltage waveform is clamped to a low voltage level (~ -1.8 V) by the turned-on N_STSCR device. The measured results can match the results shown in Fig. 2.15. The higher voltage pulse will generate the higher substrate bias through Mn or Mp. So, the P_STSCR and N_STSCR can be triggered on into latching state more quickly with increasing the pulse voltage. These have verified the effectiveness of the proposed ESD protection circuits designed with the substrate-triggered technique and the SCR devices. To achieve latchup-immunity, some diodes must be stacked with the substrate-triggered SCR devices in the ESD protection circuits.

To verify the property of latchup-immunity, another verification to measure the holding voltages of the complementary STSCR devices with stacked diode string is tested under transient conditions. The turn-on behavior of the power-rail ESD clamp circuit realized with the R, C, inverter, and P_STSCR with stacked diode string is shown in Fig. 3.17. In Fig. 3.17,

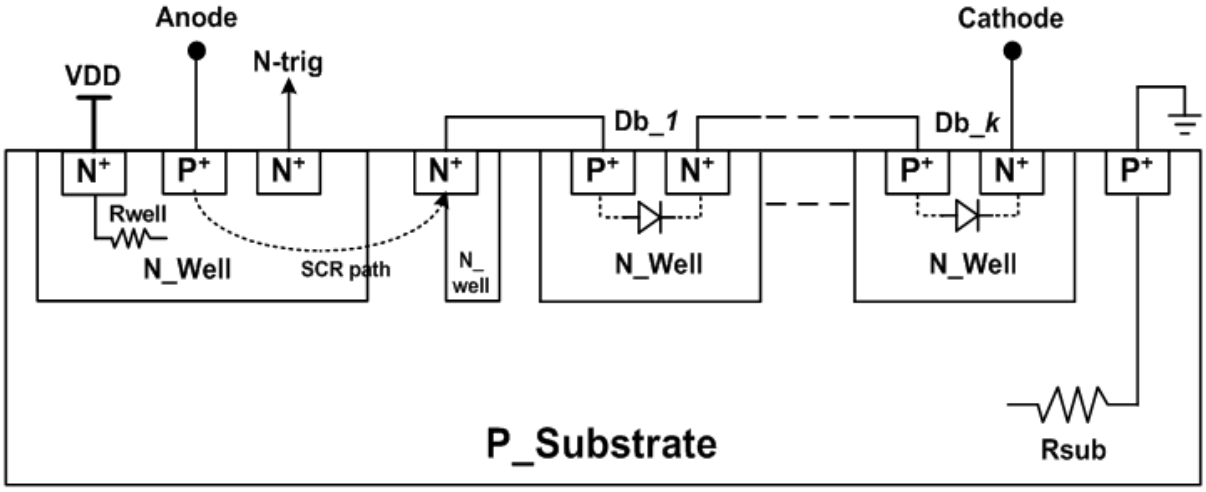
a 0-to-5 V voltage pulse with a pulse width of 400 ns and a rise time of 10 ns is applied to the VDD pin of Fig. 3.11(a) to simulate the PS-mode ESD-zapping condition. The voltage pulse applied on the VDD pin is clamped to 1.6, 2.4, 3, 4.3 V by the ESD protection circuit realized with ESD-detection circuit, P_STSCR, and 0, 1, 2, 4 diodes, respectively. When the voltage pulse is applied to the VDD pin, the voltage pulse is quickly clamped to a low voltage level within only several ns. The clamped voltage level of the ESD protection circuit can be linearly adjusted by changing the number of stacked diodes for practical applications in CMOS IC products with different VDD voltage levels. For IC applications with VDD of 2.5 V, the P_STSCR and two stacked diodes has a clamped voltage of about 3 V, so it can be free to latchup issue.

3.4 SUMMARY

A latchup-free on-chip ESD protection circuits realized with complementary substrate-triggered SCR devices have been successfully investigated in a 0.25-μm salicided CMOS process. By using the substrate-triggered technique, the ESD protection circuits with complementary-STSCR devices and stacked diodes have the advantages of controllable switching voltage, adjustable holding voltage, fast turn-on speed, high ESD robustness in a smaller layout area, and free to latchup issue. For the IC applications with VDD of 2.5 V, the ESD protection circuits designed with complementary-STSCR devices and two stacked diodes can sustain the HBM (MM) ESD level of ~7.25 kV (500 V) in a 0.25-μm fully salicided CMOS process without using extra process modification.

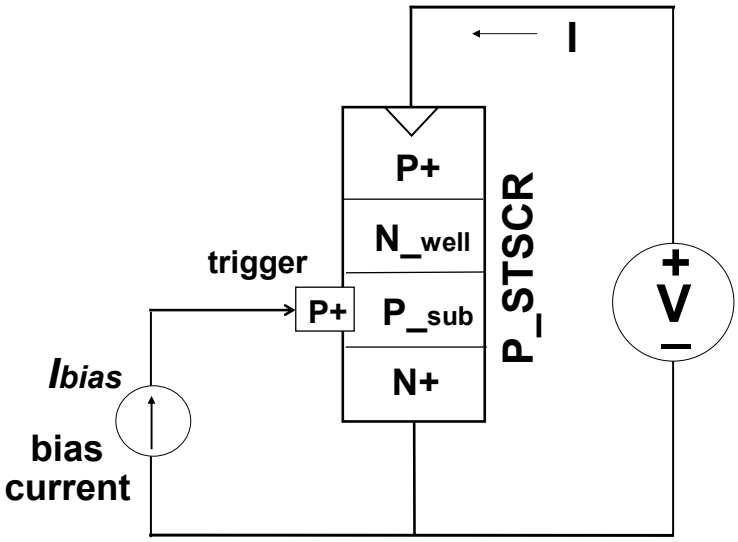


(a)

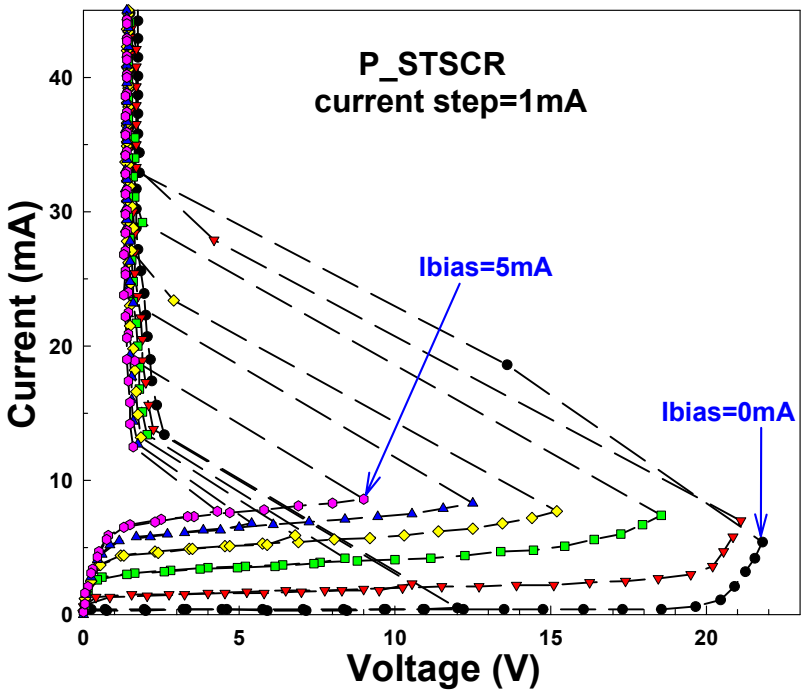


(b)

Fig. 3.1 Device structures of (a) the p-type substrate-triggered SCR device (P_STSCR), and (b) the n-type substrate-triggered SCR device (N_STSCR), with stacked diode string.

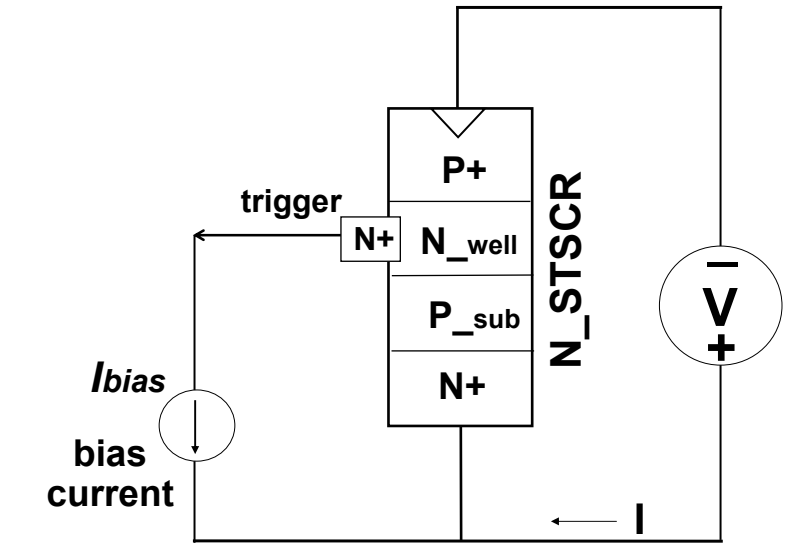


(a)

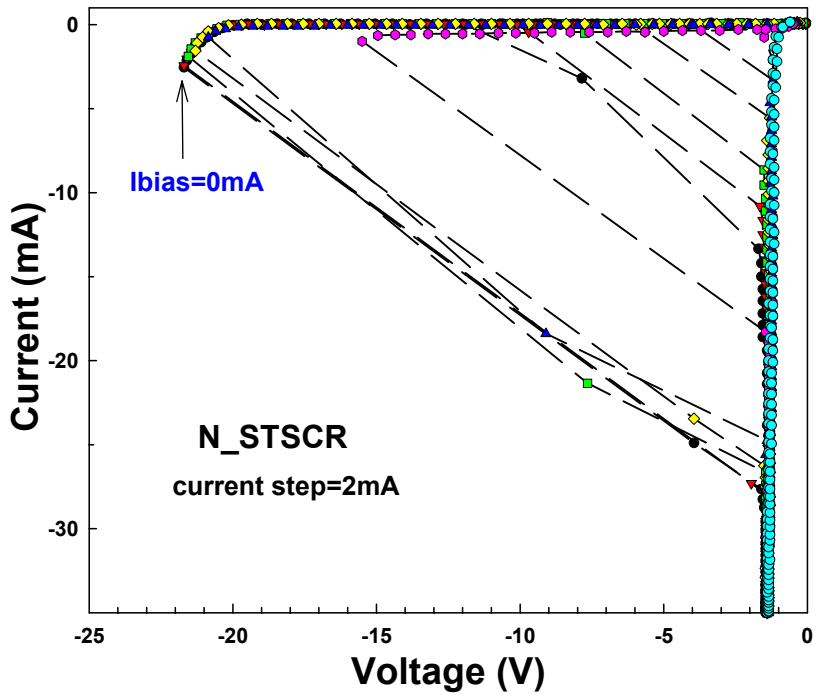


(b)

Fig. 3.2 (a) The experimental measurement setup to measure the I-V curves of the P_STSCR device, and (b) the measured I-V curves of the P_STSCR device under different substrate-triggered currents.

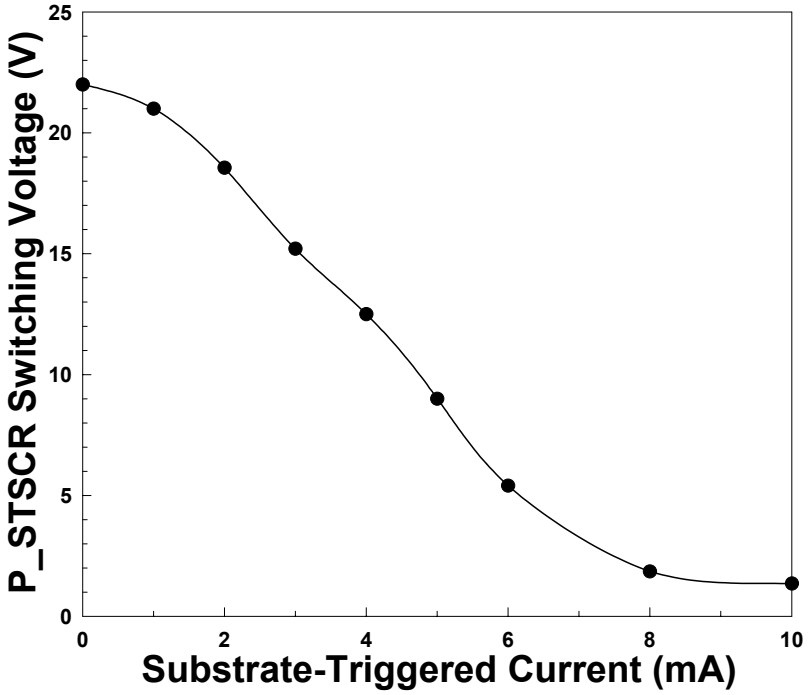


(a)

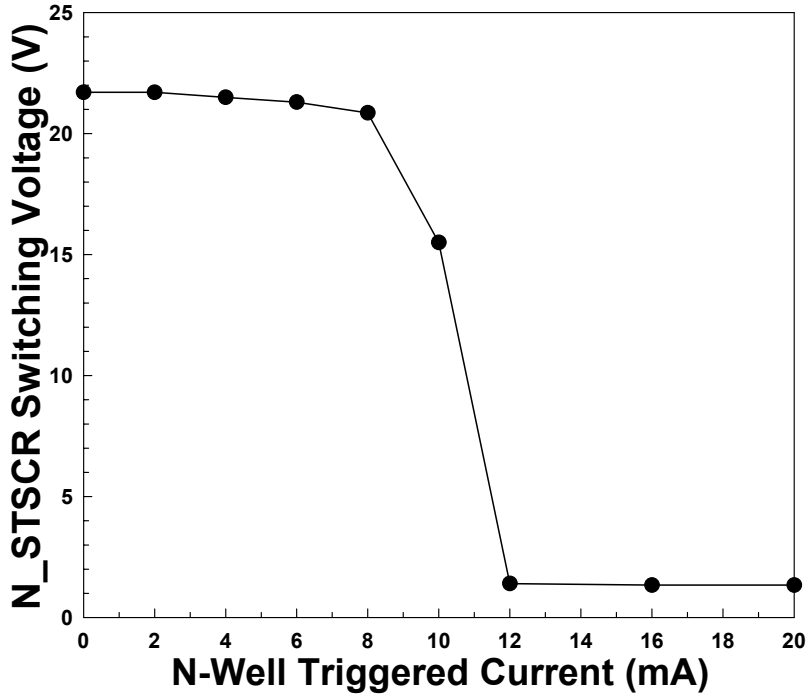


(b)

Fig. 3.3 (a) The experimental measurement setup to measure the I-V curves of the N_STSCR device, and (b) the measured I-V curves of the N_STSCR device under different well-triggered currents.

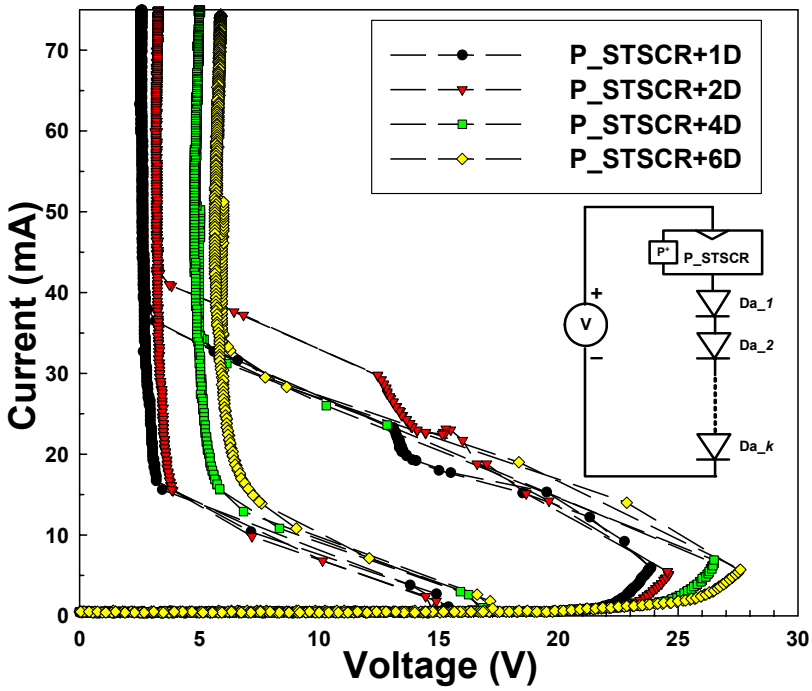


(a)

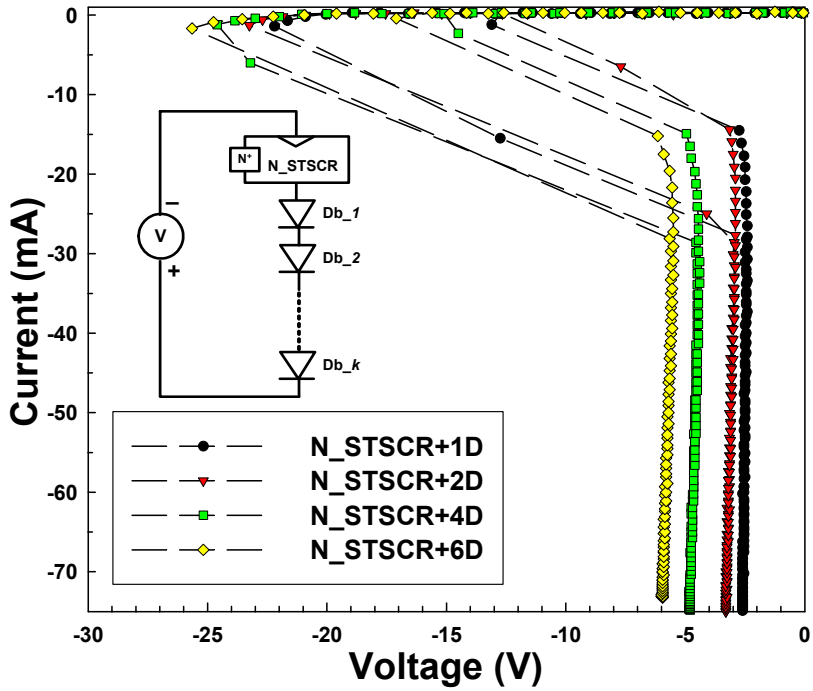


(b)

Fig. 3.4 Dependence of the switching voltage of (a) the P_STSCR, and (b) the N_STSCR, on the triggered current in P-substrate or in N-well.

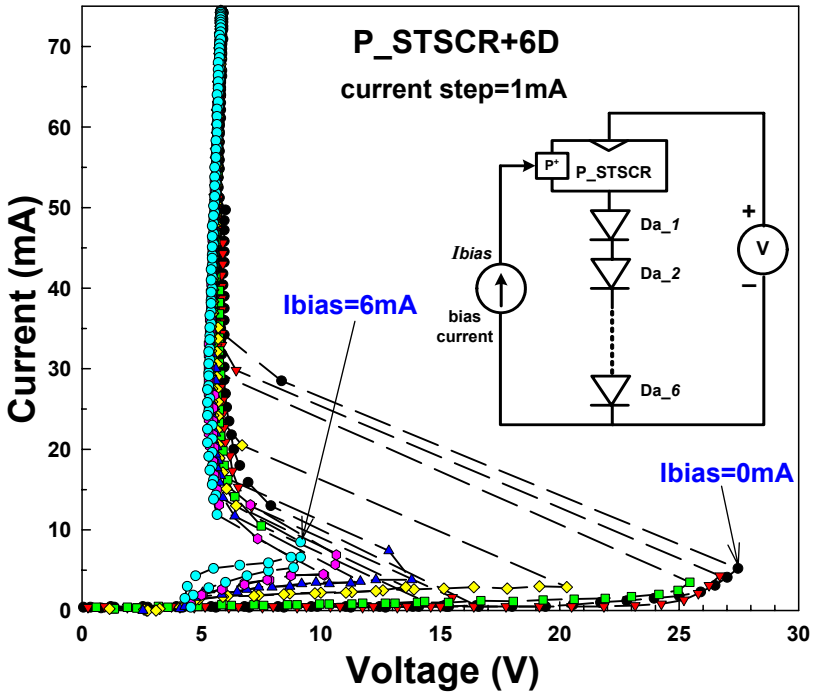


(a)

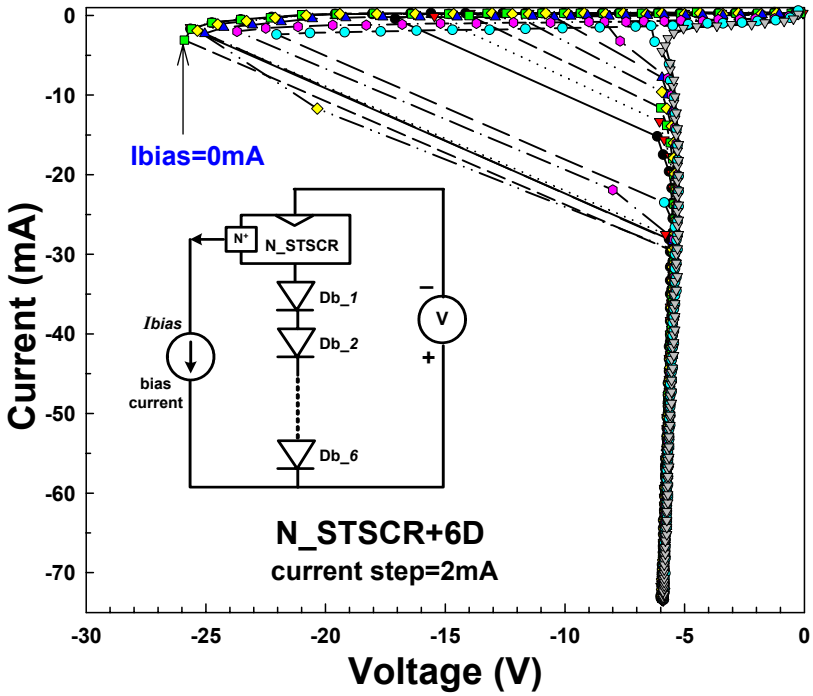


(b)

Fig. 3.5 The measured I-V curves of (a) the P_STSCR, and (b) the N_STSCR, with different numbers of stacked diodes under the temperature of 25°C.

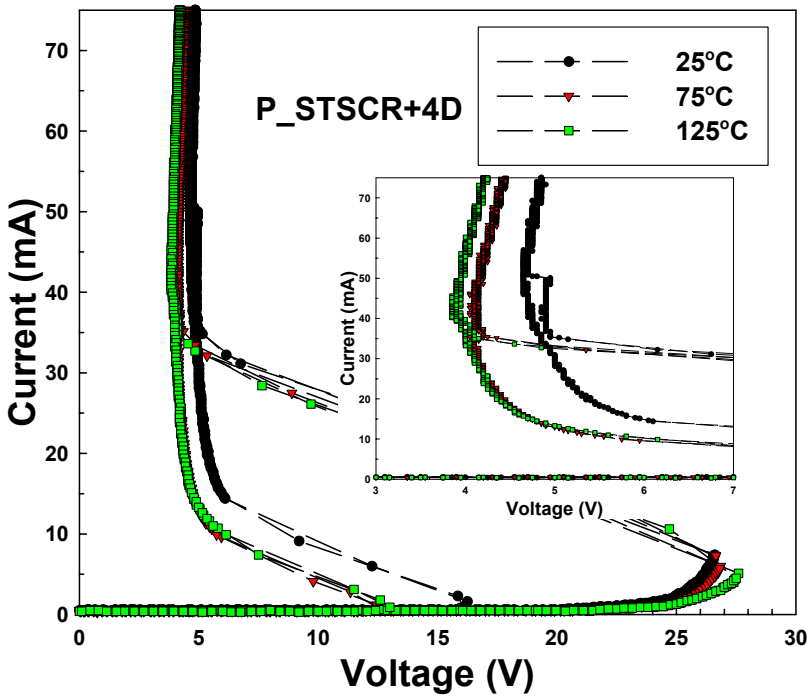


(a)



(b)

Fig. 3.6 The measured turn-on I-V curves of (a) the P_STSCR, and (b) the N_STSCR, with six stacked diodes under different triggered currents.



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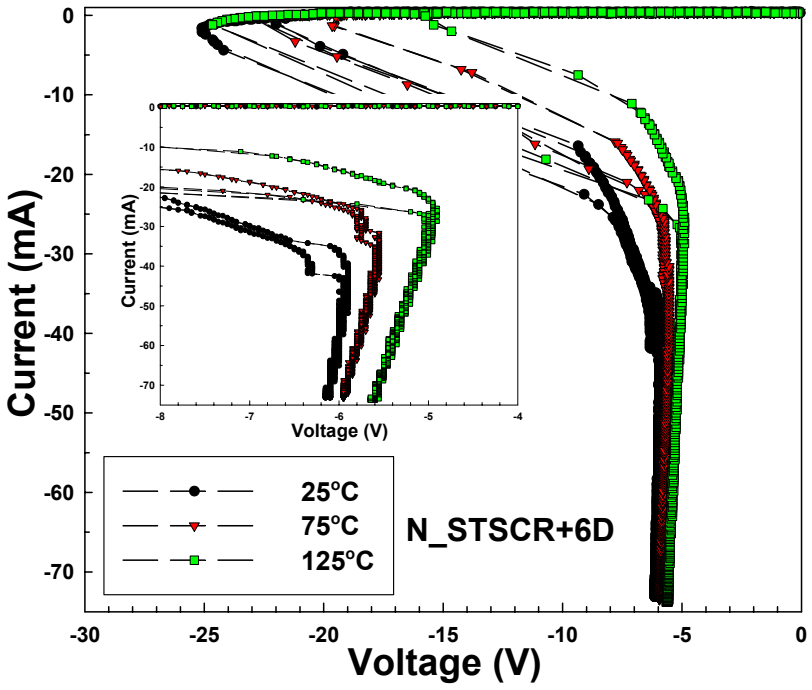
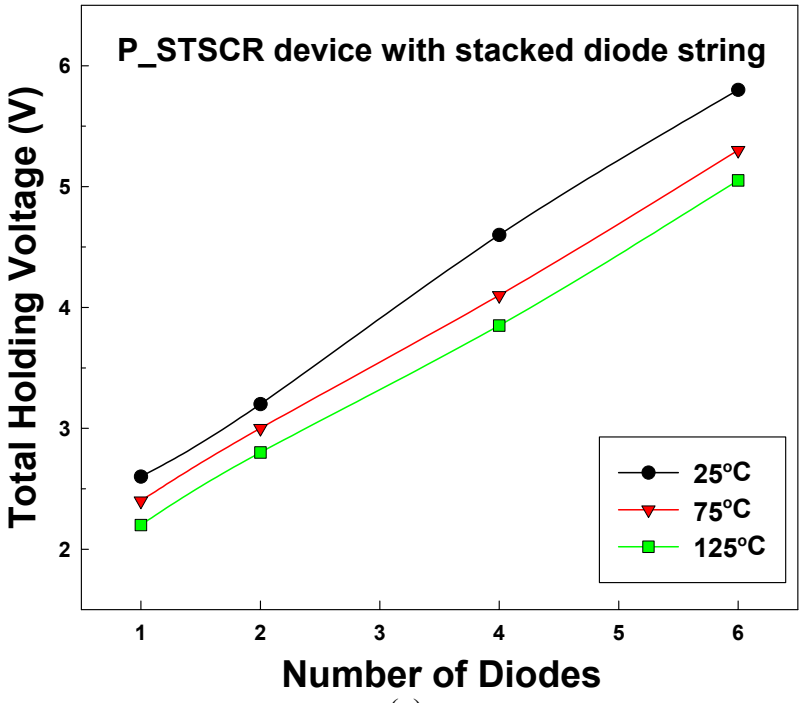
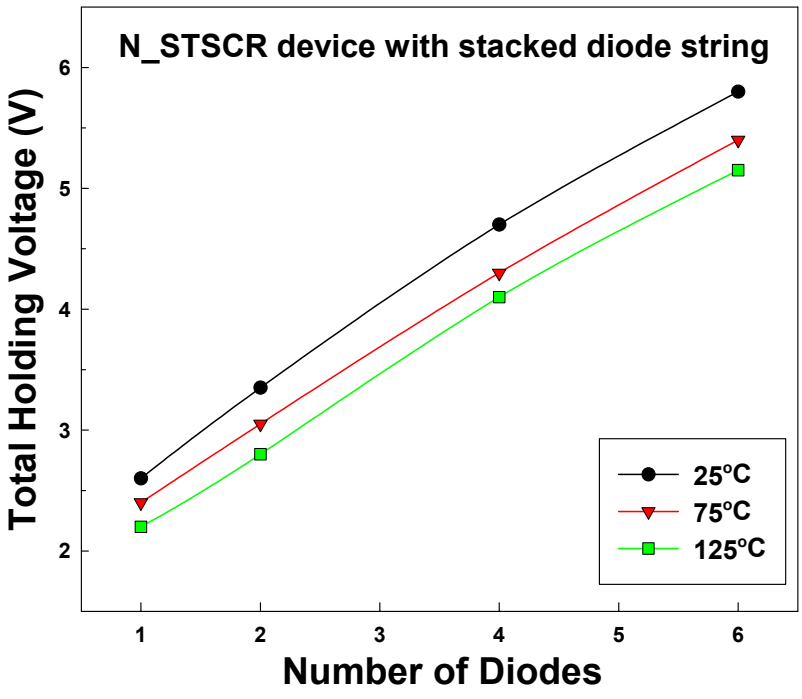


(b)

Fig. 3.7 The measured I-V curves of (a) the P_STSCR with four stacked diodes, and (b) the N_STSCR with six stacked diodes, under different temperatures.

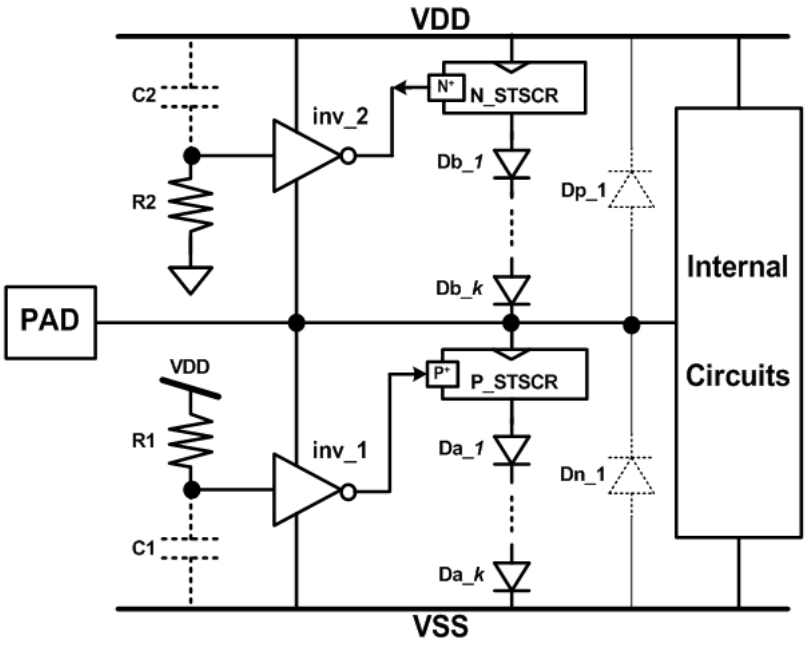


(a)

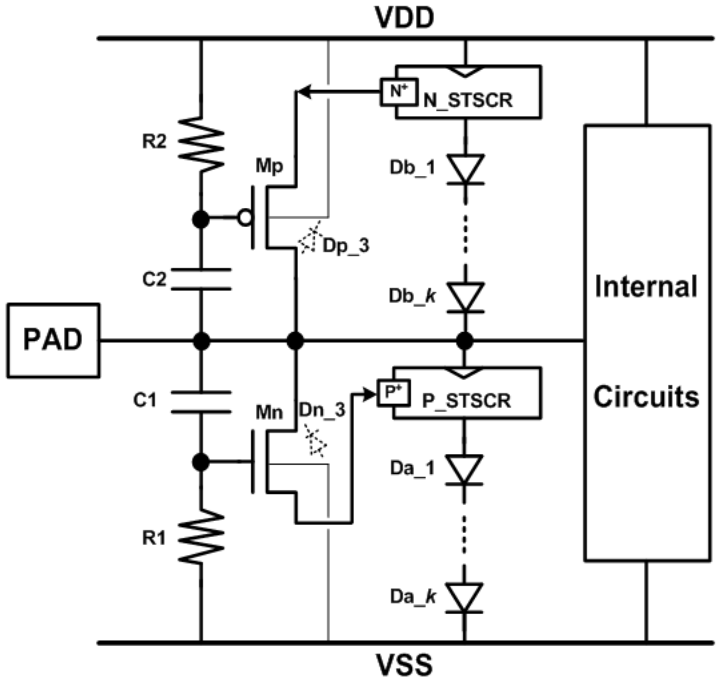


(b)

Fig. 3.8 Dependence of the total holding voltage of (a) the P_STSCR with stacked diode string, and (b) the N_STSCR with stacked diode string, on the number of stacked diodes under different temperatures.



(a)



(b)

Fig. 3.9 Design of ESD protection circuits for the input or output pads with the proposed complementary-STSCR devices and stacked diode string by using (a) RC delay, and (b) gate coupled, circuit techniques.

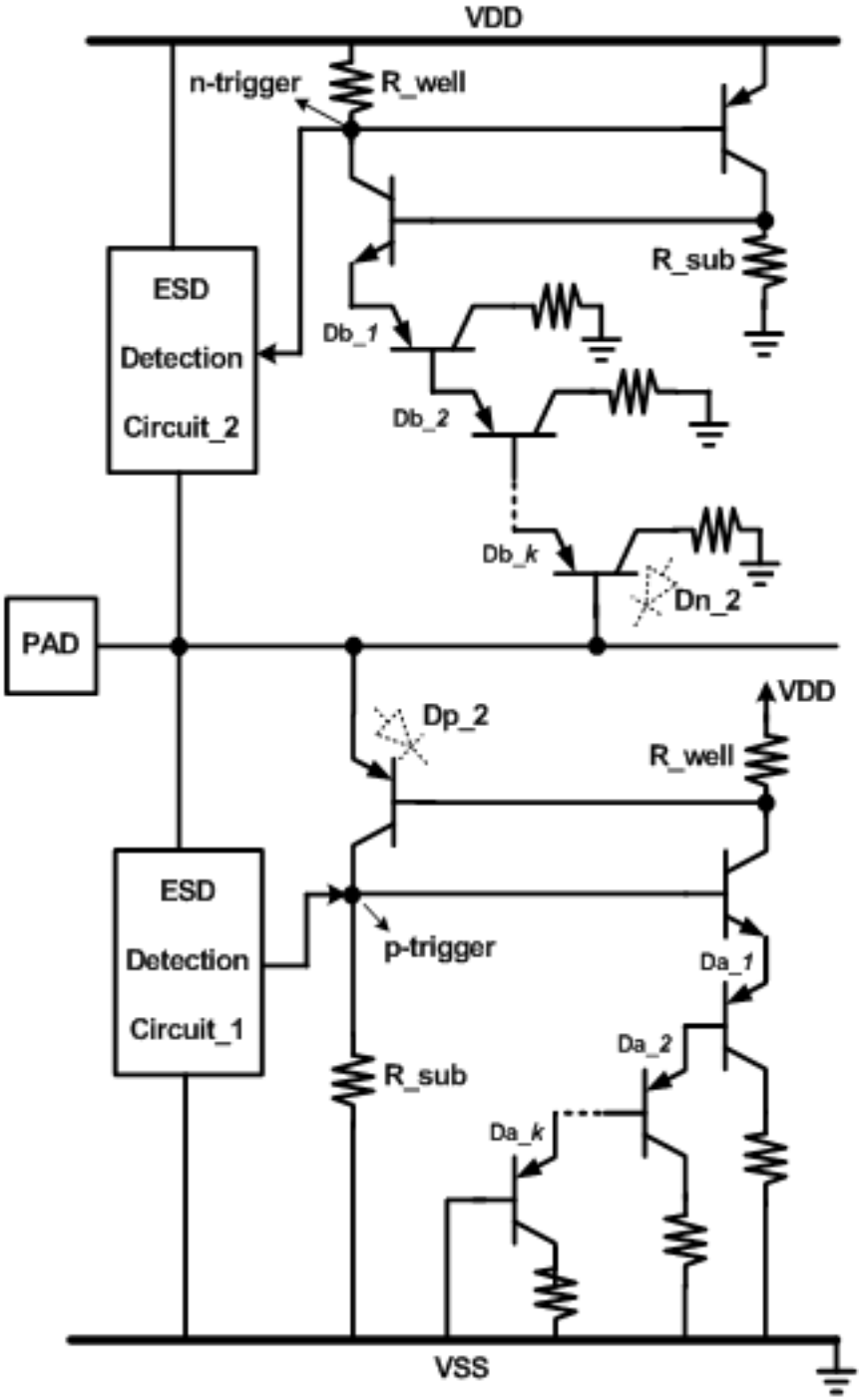
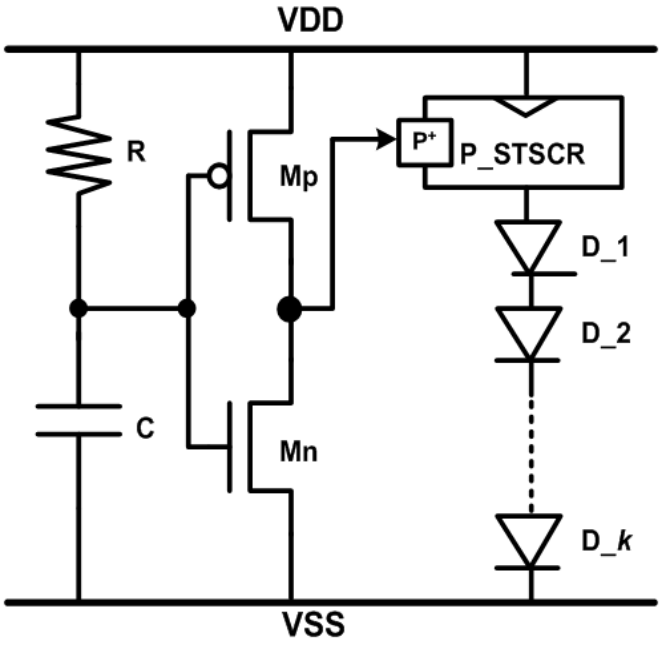


Fig. 3.10 The equivalent circuit of the complementary-STSCR devices with stacked diode string for the input and output pads.



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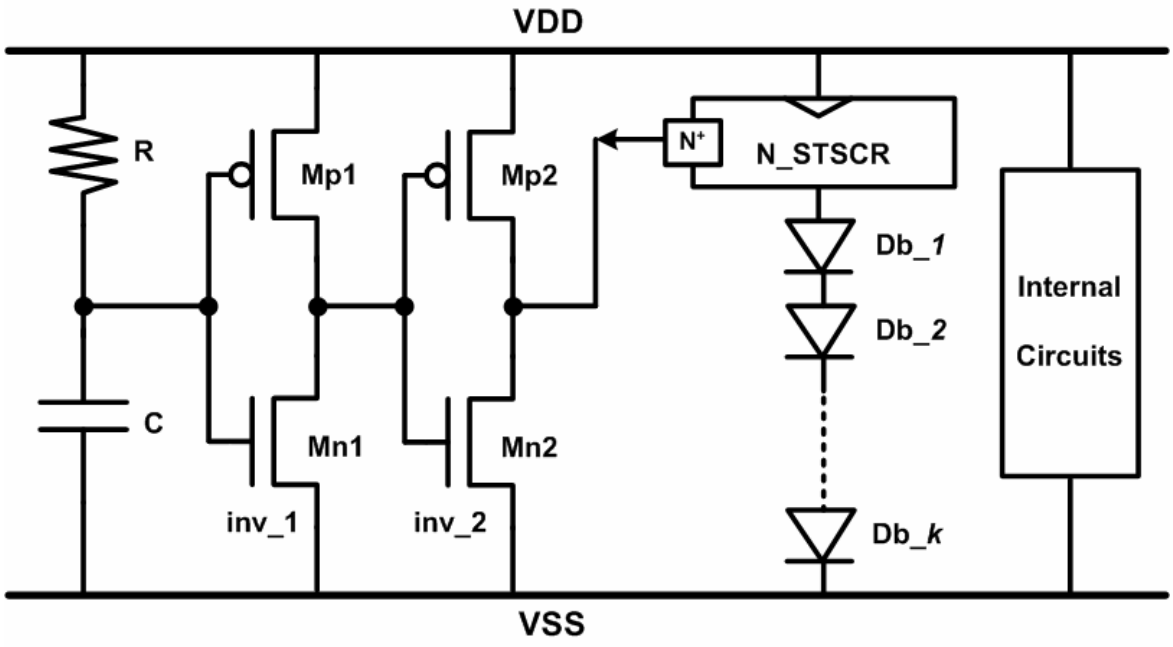
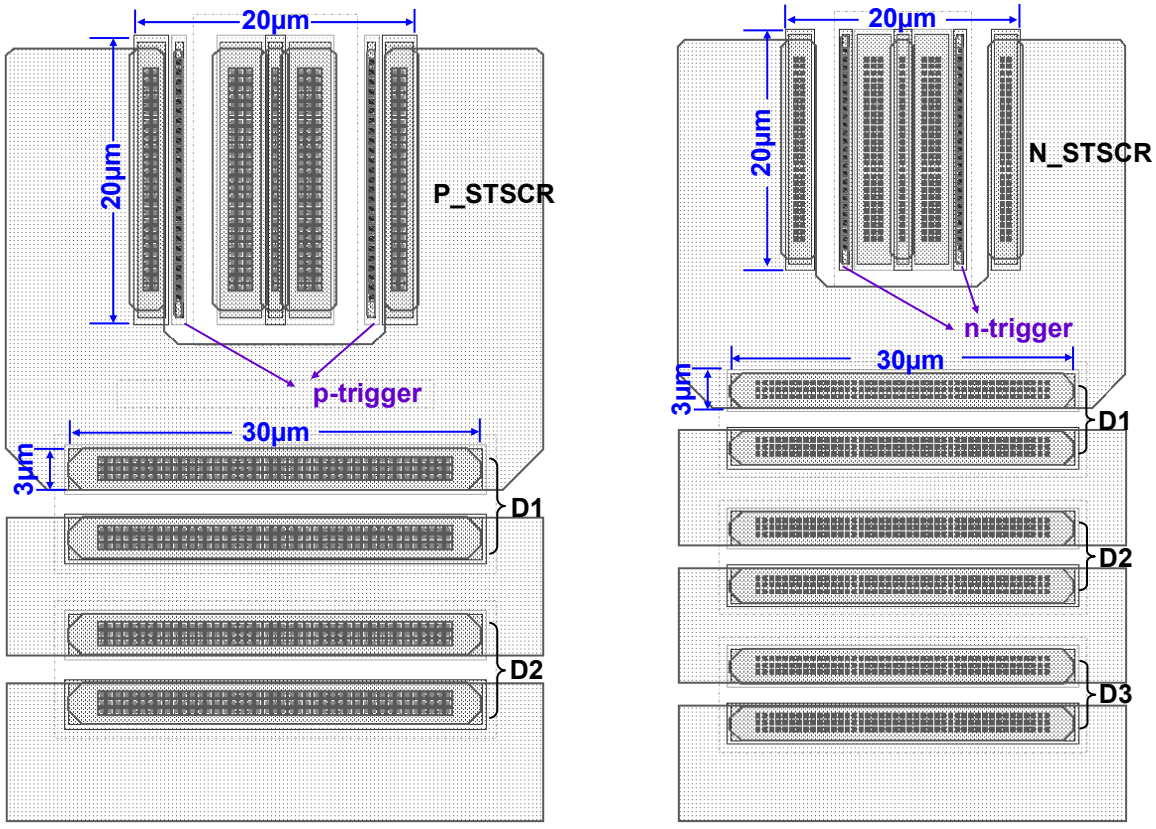


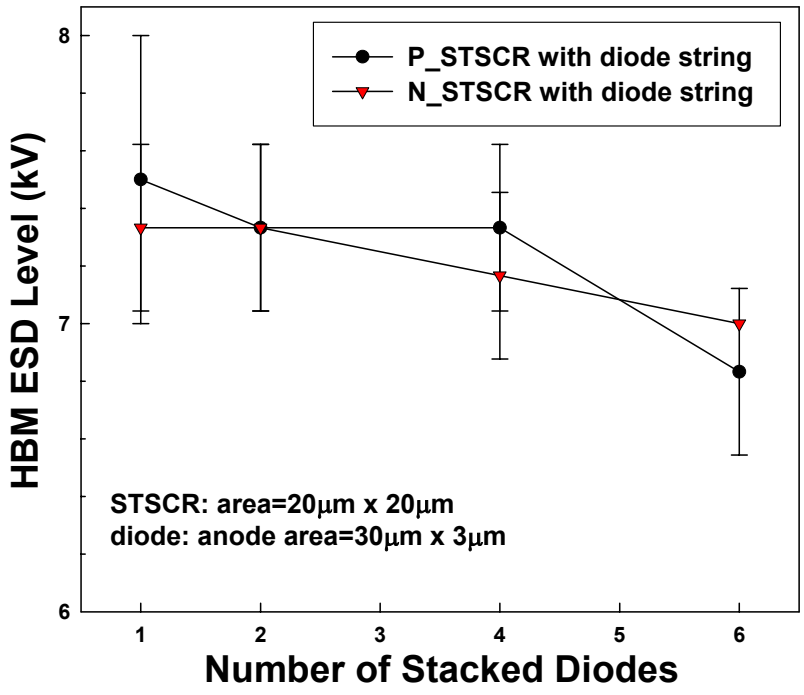
(b)

Fig. 3.11 The VDD-to-VSS ESD clamp circuits realized with (a) the P_STSCR, and (b) the N_STSCR, with stacked diode sting.

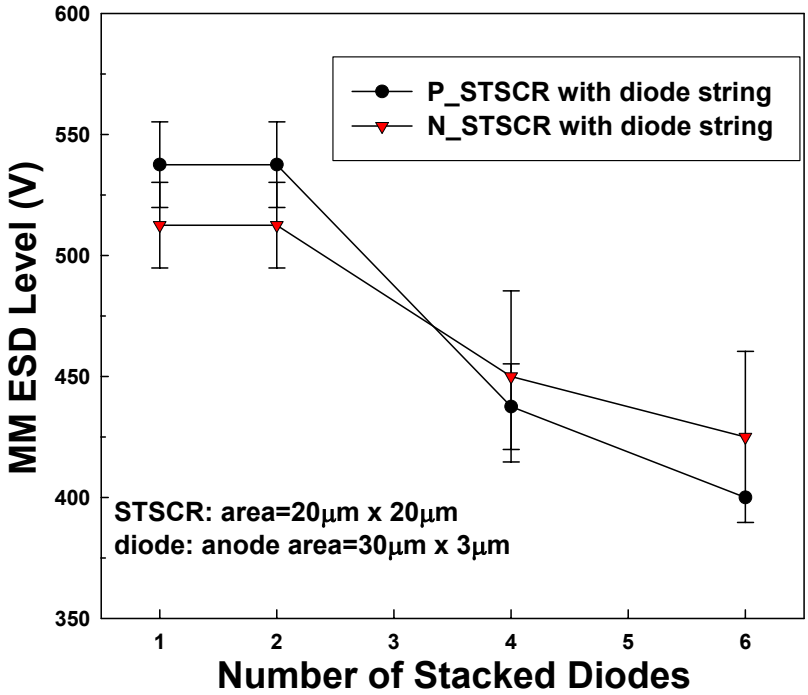


(a) (b)

Fig. 3.12 The layout top views of (a) the P_STSCR with two stacked diodes, and (b) the N_STSCR with three stacked diodes, in a 0.25-μm salicided CMOS process.



(a)



(b)

Fig. 3.13 Dependence of the (a) HBM, and (b) MM, ESD levels of the complementary STSCR devices with stacked diode sting on the number of the stacked diodes (Failure criterion: $I_{Leakage} > 1$ μA @ 2.5 V bias).

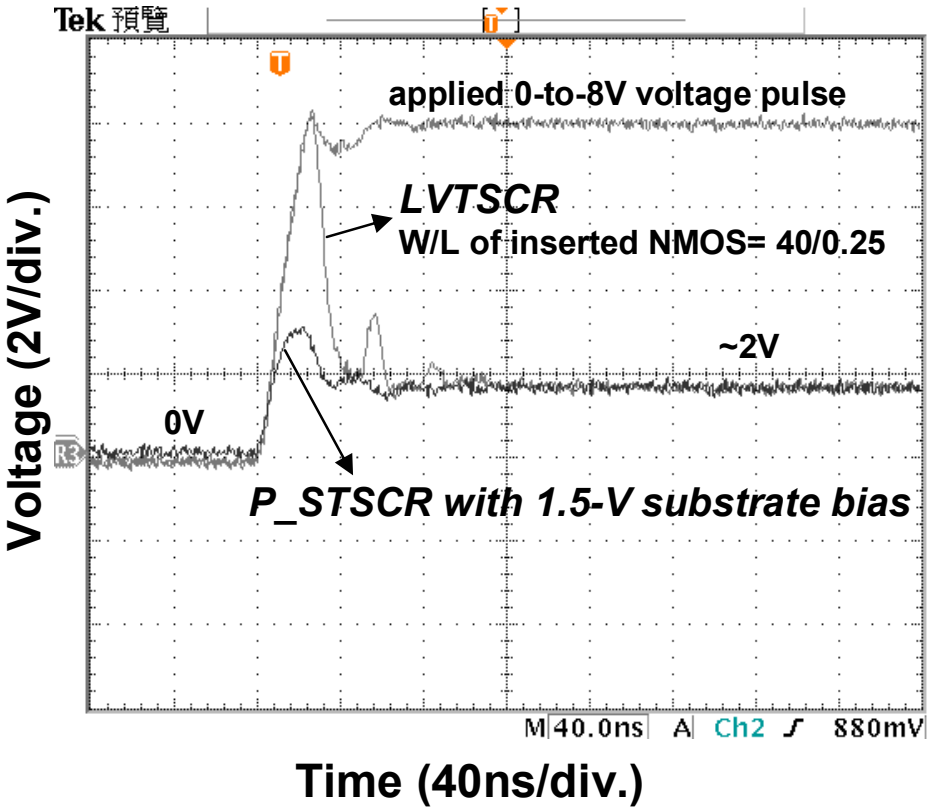
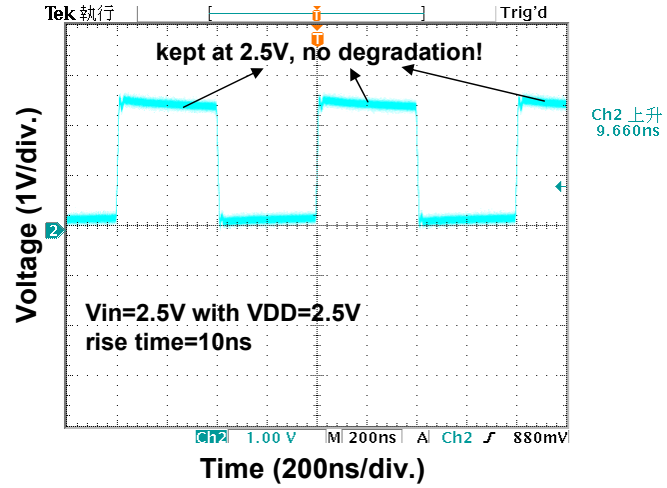
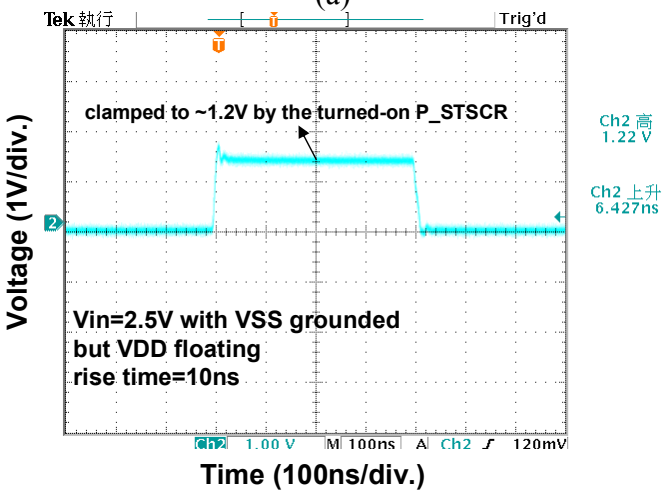


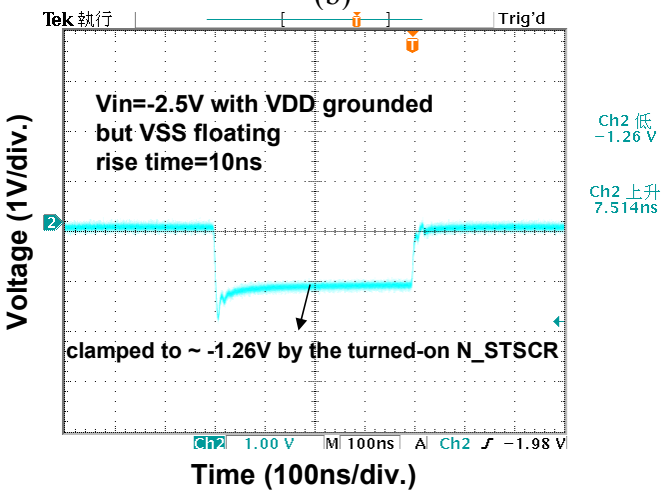
Fig. 3.14 The comparison of turn-on time between LVTSCR and P_STSCR with 1.5-V substrate bias under an applied 0-to-8 V voltage pulse.



(a)

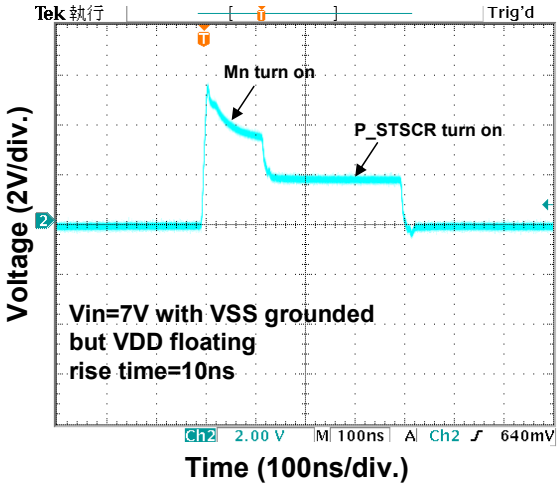


(b)

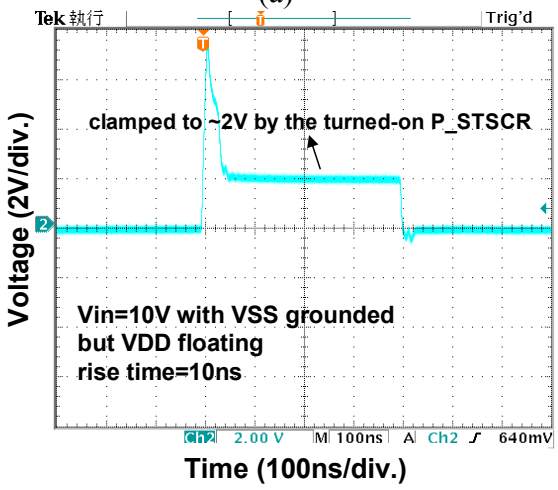


(c)

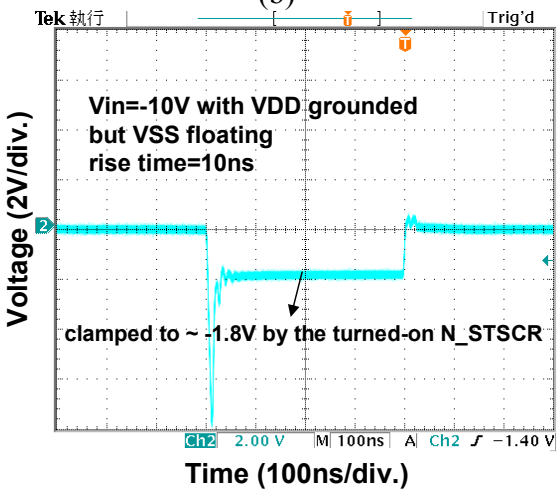
Fig. 3.15 The measured voltage waveforms on the I/O pad of Fig. 3.9(a) under (a) the normal circuit operating conditions, (b) the positive-to-VSS ESD zapping condition, when a 2.5-V voltage pulse is applied to the I/O pad, and (c) the negative-to-VDD ESD zapping condition when a -2.5-V voltage pulse is applied to the I/O pad.



(a)



(b)



(c)

Fig. 3.16 The measured voltage waveforms on the I/O pad of Fig. 3.9(b) under (a) the 7-V positive-to-VSS ESD zapping condition, (b) the 10-V positive-to-VSS ESD zapping condition, and (c) the -10V negative-to-VDD ESD zapping condition.

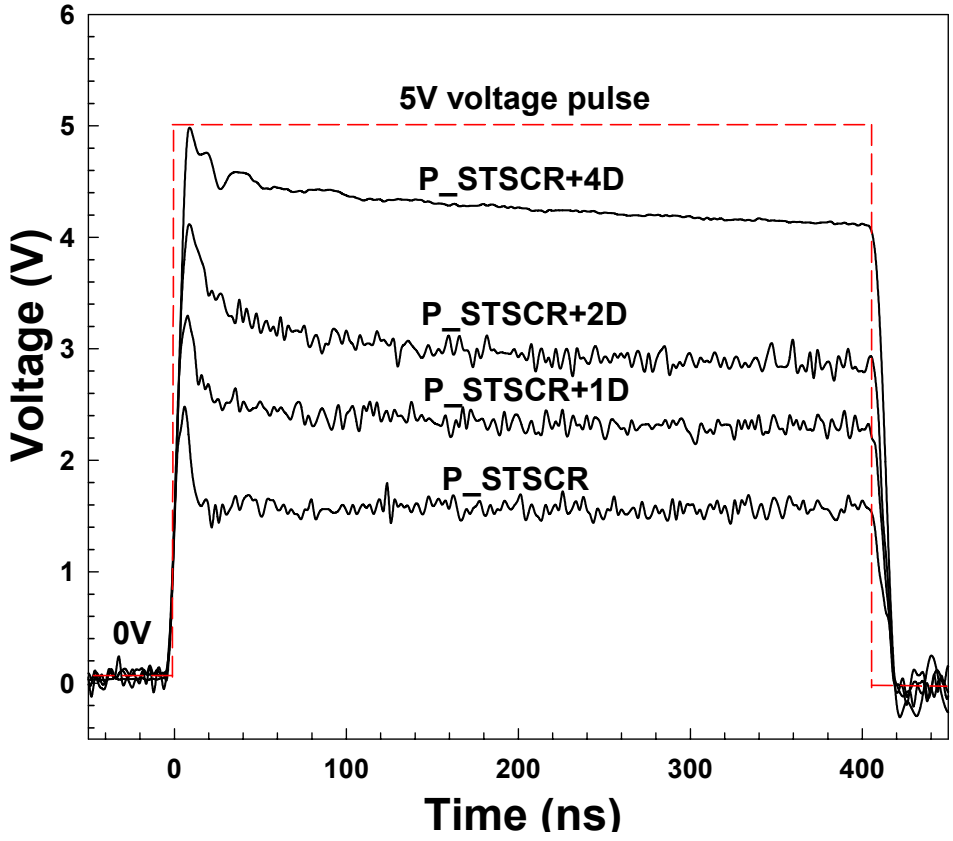


Fig. 3.17 The voltage waveforms clamped by the VDD-to-VSS ESD clamp circuit designed with the P_STSCR device and different numbers of stacked diodes, when a 0-to-5 V voltage pulse is applied.

CHAPTER 4

SCR DEVICE WITH DOUBLE-TRIGGERED TECHNIQUE FOR EFFECTIVE ON-CHIP ESD PROTECTION

SCR device consists of a lateral NPN and a vertical PNP bipolar transistors, which is inherent in the CMOS processes. In this chapter, a novel double-triggered technique, used to synchronously trigger the NPN and PNP transistors in the SCR structure, is also proposed to further improve the turn-on speed of SCR devices for using in on-chip ESD protection circuit to effectively protect the much thinner gate oxide in nanoscale CMOS processes [27]. The purpose of double-triggered technique is to reduce the switching and to enhance the turn-on speed of SCR device. The DTSCR device is designed to be triggered on without involving junction avalanche breakdown mechanism. With a suitable ESD-detection circuit, such DTSCR device is designed to be kept off during the normal circuit operating conditions, and to be quickly triggered on during the ESD-zapping conditions.

4.1 DOUBLE-TRIGGERED SCR (DTSCR) DEVICE

4.1.1 Device Structure

The proposed double-triggered SCR (DTSCR) device is shown in Fig. 4.1. The ESD current path in the DTSCR device is indicated by the dashed lines shown in Fig. 4.1. As compared with the traditional lateral SCR device structure [1], extra P+ and N+ diffusions are inserted into the P-substrate and N-well of the DTSCR device structure, respectively. The inserted P+ and N+ diffusions are connected out as the p-trigger and n-trigger nodes of the DTSCR device. When a trigger current is applied into p-trigger node, the NPN bipolar transistor in SCR structure is active, and the collector current of NPN is generated to bias the PNP bipolar transistor. When PNP transistor is turned on, the collector current of PNP is also generated to further bias NPN transistor. The positive-feedback regenerative mechanism [35],

[36] of latchup is initiated by the substrate-triggered current in SCR structure instead of avalanche breakdown mechanism, so the DTSCR will be triggered into its latching state. When a trigger current is drawn out from the n-trigger node, the DTSCR will be also triggered on into its latching state through the positive-feedback regenerative mechanism. In this chapter, two trigger currents can be synchronously applied to trigger on the DTSCR device.

4.1.2 Device I-V Characteristics

The fully-silicided DTSCR device in Fig. 4.1 has been fabricated in a 0.25-μm salicided CMOS process. The layout top view of the DTSCR device is shown in Fig. 4.2. The active area of the DTSCR device is 20 μm×20 μm. Fig. 4.3(a) shows the measured DC I-V curves of DTSCR, which is measured under different substrate-triggered currents into the p-trigger node of DTSCR but no N-well triggered current. The measurement setup is shown as the inset in Fig. 4.3(a). The switching voltage of such DTSCR is reduced with the increase of the substrate-triggered current. When the triggered current at the p-trigger node is increased from 0 to 6 mA, the switching voltage of DTSCR is reduced from ~22 to ~7 V. If the triggered current is continually increased, the switching voltage will be nearly reduced to its holding voltage. Moreover, in Fig. 4.3(b), the double-triggered solution is used to further reduce the switching voltage to a relatively lower voltage level. Based on the similar measurement of Fig. 4.3(a), an extra N-well current of 2 mA is drawn out from the n-trigger node of DTSCR, and the measured I-V curves under different substrate-triggered currents into the p-trigger node are shown in Fig. 4.3(b). The double-triggered measurement setup is also indicated in the inset of Fig. 4.3(b). The switching voltage of DTSCR under the substrate-triggered current of 6 mA is further reduced from ~7 to only ~2 V, when the N-well triggered current is increased from 0 to -2 mA. The negative sign on the current in this chapter is used to represent the current flowing out from the node. The dependence of switching voltage of DTSCR device on the substrate-triggered current under different N-well triggered currents is depicted in Fig. 4.3(c). The switching voltage of DTSCR device can be nearly reduced to the holding voltage (~1.5 V) more efficiently, when both the substrate-triggered and N-well triggered currents are applied to the DTSCR device. These results have proven that the switching voltage of DTSCR device can be significantly reduced by the proposed

double-triggered technique.

The measured DC I-V curves of DTSCR under a substrate-triggered current of 2 mA into the p-trigger node and different N-well triggered currents out from the n-trigger node are shown in Fig. 4.4(a). The measurement setup is also illustrated as the inset in Fig. 4.4(a). When the N-well triggered current is increased from 0 to -3 mA, the switching voltage of DTSCR under the substrate-triggered current of 2 mA is significantly reduced from ~15 to only ~1.5 V, which is near to its holding voltage. The dependence of switching voltage of the DTSCR on the N-well triggered current under different substrate-triggered currents is shown in Fig. 4.4(b). The switching voltage of DTSCR under the N-well triggered current of -3 mA is further reduced from ~21 to ~1.5 V, when the substrate-triggered current is increased from 0 to 2 mA. The characteristics of DTSCR in Fig. 4.4(b) are similar to that in Fig. 4.3(c). In the p-type substrate, because the current gain of NPN transistor is higher than that of PNP transistor, the substrate-triggered current (used to trigger the NPN transistor in the DTSCR device) seems to have more significant effect, than N-well triggered current (used to trigger the PNP transistor in the DTSCR device) to reduce switching voltage of the DTSCR and to quickly trigger on DTSCR [58]. The ESD protection device with lower switching voltage can be turned on more quickly to protect the internal circuits from ESD damage.

Another issue of using SCR device as the ESD protection device is the transient-induced latchup concern [32], when CMOS IC is operating under normal circuit operations. The total holding voltage of the ESD protection circuit with SCR devices must be designed greater than the maximum voltage level of VDD during the normal circuit operating conditions to avoid the latchup issue. This can be achieved by stacking the DTSCR devices in the ESD protection circuits. Fig. 4.5 shows the dependence of the total holding voltage of stacked DTSCR devices on the temperature under different numbers of stacked DTSCR devices. The measurement setup to measure the I-V curves of stacked DTSCR devices is depicted in Fig. 4.5(a). The I-V curves of two (three) DTSCR devices in stacked configuration, which is marked as 2DTSCR (3DTSCR), under different temperatures are measured in Fig. 4.5(b) (Fig. 4.5(c)). The insets in Figs. 4.5(b) and 4.5(c) are the enlarged views around the holding points. The total holding voltage has some degradation, when the temperature is increased, because the current gains (β) of the parasitic bipolar transistors in the SCR device are increased with the increase of temperature. The holding voltages of 1DTSCR, for example, are 1.4, 1.24, and 1.18 V under the temperatures of 25, 75, and 125 ^{o}C, respectively. The total holding voltage,

however, can be still raised up by increasing the number of the stacked DTSCR devices. The holding voltages of 1DTSCR, 2DTSCR, and 3DTSCR at the temperature of 125 ^{o}C are 1.18, 2.5, and 3.9 V, respectively. The dependence of holding voltage on temperature in the stacked DTSCR devices is compared in Fig. 4.5(d). Although the DTSCR devices in stacked configurations have the increased total switching voltage, such stacked DTSCR devices can be still quickly triggered on to provide effective ESD protection, when the double-triggered technique is synchronously applied to all stacked DTSCR devices.

4.1.3 Turn-On Speed

From the measured DC I-V curves of DTSCR, it has been verified that the switching voltage of DTSCR can be significantly reduced by the substrate and N-well triggered currents. The turn-on time of DTSCR, which is defined as the time for DTSCR entering into its latching state, will be verified in this section. Fig. 4.6(a) shows the measurement setup to find the turn-on time of DTSCR devices with double-triggered technique. The measured results in time domain for DTSCR are shown in Figs. 4.6(b) to 4.6(h), where the V_anode, V_p-trigger, and V_n-trigger are the voltage waveforms on the anode, p-trigger, and n-trigger nodes of the DTSCR shown in Fig. 4.6(a). The anode of the DTSCR device is biased at 5 V through the resistance of 10 Ω, which is used to limit the sudden large transient current from power supply, when the DTSCR is turned on.

The positive and negative voltage pulses with a fixed rise time (or fall time) of 10 ns, which are generated from pulse generators, are synchronously applied to the p-trigger and n-trigger nodes. The original voltage pulses generated synchronously from pulse generators are shown in Fig. 4.6(b). The pulse height and pulse width are changed in the experimental measurement to verify the required turn-on time of DTSCR. However, in order to avoid the loading effect of oscilloscope interfering the accuracy of measured waveform, only the V_p-trigger will be monitored. When a 0-to-1.5 V positive voltage pulse with a pulse width of 100 ns is applied into the p-trigger node of DTSCR and the n-trigger node is floating, the voltage waveform at the V_anode of the DTSCR which is triggered into latching state is shown in Fig. 4.6(c). After the triggering of 1.5-V voltage pulse at the p-trigger node, the V_anode is latched at a low voltage level of ~2.5 V and the V_p-trigger is kept at a voltage level of 0.8 V. If the pulse width of 1.5-V pulse at the p-trigger node is reduced to 30 ns, the

DTSCR device can not be triggered on by this 1.5-V voltage pulse. So, the V_anode is still kept at the same voltage level of 5 V as shown in Fig. 4.6(d). However, based on the same condition of Fig. 4.6(d), the DTSCR device can be triggered into latching state if an additional 5-to-0 V negative voltage pulse with pulse width of 30 ns is synchronously applied to the n-trigger node of DTSCR device, as that shown in Fig. 4.6(e). So, the required pulse width for DTSCR triggering into latching state can be shortened if both positive and negative voltage pulses are synchronously applied to the p-trigger and n-trigger nodes.

The turn-on time for DTSCR into its latching state is observed by the close-up view of the V_anode voltage waveform at the falling edge. The close-up views of the V_anode at the falling edge, while the DTSCR is synchronously triggered by the positive voltage pulse of 1.5 V at p-trigger node and the negative voltage pulse of floating, 5-to-2 V, and 5-to-0 V at n-trigger node, are compared in Figs. 4.6(f), 4.6(g), and 4.6(h), respectively. The pulse widths of the positive and negative voltage pulses in the measurements of Figs. 4.6(f)-4.6(h) are 200 ns. The turn-on time of DTSCR is 37.6 ns in Fig. 4.6(f) if only a 1.5-V positive voltage pulse is applied into the p-trigger node. Hence, the DTSCR can not be triggered on, if only a 1.5-V voltage pulse with a pulse width smaller than 37.6 ns is applied into the p-trigger node alone, which has been verified in Fig. 4.6(d). Moreover, from Figs. 4.6(f) to 4.6(h), under the positive voltage pulse of 1.5 V at p-trigger node, the turn-on time of DTSCR can be reduced from 37.6 to 11.8 ns, while the absolute pulse height of negative voltage pulse applied to the n-trigger node is increased from 0 to 5 V. These results infer that the turn-on speed of DTSCR device can be indeed speeded up by the proposed double-triggered technique. The dependence of turn-on time of DTSCR on the N-well bias under different substrate bias conditions with a fixed rise time of 10 ns is summarized in Fig. 4.7. The turn-on time of DTSCR can be shortened, when the substrate or/and N-well bias voltages are increased. In addition, the dependence of turn-on time of DTSCR on rise time of voltage pulse under different substrate bias conditions is also measured and shown in Fig. 4.8. With the reduction of rise time of applied voltage pulse, the turn-on time of DTSCR can be also shortened to trace the rise time of voltage pulse at the p-trigger node if the enough pulse voltage is applied to trigger nodes of DTSCR. For enhance the turn-on speed of DTSCR, both the pulse height and rise time must be well designed to trigger on the DTSCR device more efficiently.

4.2 APPLICATIONS FOR ON-CHIP ESD PROTECTION

4.2.1 ESD Protection Circuit for the Input/Output Pad

Based on above measured results, two kinds of ESD protection designs for I/O pad, realized with the stacked double-triggered SCR devices, are shown in Figs. 4.9(a) and 4.9(b). Two stacked DTSCR devices are used to avoid the latchup issue during normal circuit operating conditions for 2.5-V circuit applications. In Fig. 4.9(a), the RC delay is used to distinguish the ESD-zapping conditions or the normal circuit operating conditions. In Fig. 4.9(b), the gate-coupled circuit technique is used to generate the trigger currents to turn on the stacked DTSCR devices during ESD-zapping conditions.

In Fig. 4.9(a), the p-trigger (n-trigger) nodes of the two stacked DTSCR devices between I/O pad and VSS line are connected to the drain (source) of PMOS Mp1 (Mp2). The p-trigger (n-trigger) nodes of the two stacked DTSCR devices between I/O pad and VDD line are connected to the source (drain) of NMOS Mn1 (Mn2). The gates of the PMOS Mp1 and Mp2 (NMOS Mn1 and Mn2) are connected to VDD (VSS) through the resistor R1 (R2), which is better realized by the N+ diffusion resistor for the concern of antenna effect [55]. The resistors R1 and R2 can be shared with each I/O pad to save the layout area in the CMOS IC. A capacitor C1 (C2) is placed between the gates of PMOS (NMOS) and VSS (VDD). These capacitors can be formed by the parasitic capacitors at the gates of the PMOS (Mp1 and Mp2) or NMOS (Mn1 and Mn2). The blocking diodes, Db, are used to block the current flowing through the metals connected among the trigger nodes of the stacked DTSCR devices. Besides, there are two parasitic diodes (Dp_2 and Dn_2) in this ESD protection circuit. The Dp_2 is the source-to-N-well (VDD) parasitic diode in PMOS Mp1. The Dn_2 is the source-to-P-sub (VSS) parasitic diode in NMOS Mn2.

In the normal circuit operating conditions with VDD and VSS power supplies, the gates of Mp1 and Mp2 (Mn1 and Mn2) are biased at VDD (VSS). Therefore, the Mp1, Mp2, Mn1, and Mn2 are all in off state, whenever the input signal is logic high (VDD) or logic low (VSS). The p-trigger (n-trigger) nodes of the stacked DTSCR devices are kept at VSS (VDD) through the parasitic resistors (R_well and R_sub), so such stacked DTSCR devices are guaranteed to be kept off in the normal circuit operating conditions.

To clearly comprehend the ESD current paths under these ESD stresses, the equivalent

circuit of the ESD protection circuit designed by the stacked DTSCR devices for I/O pad is illustrated in Fig. 4.10. The Dn_1 is the N-well (under the N+ diffusion at the end of the SCR path) to P-sub (VSS) parasitic diode in DTSCR_4 and the Dp_1 is the P+ to N-well (connected to VDD) parasitic diode in the DTSCR_1.

Under the PS-mode ESD-zapping condition (with grounded VSS but floating VDD), the gates of Mp1 and Mp2 are initially floating with a zero voltage level, thereby the Mp1 and Mp2 will be turned on due to the positive ESD voltage on the pad. So, the Mp1 will conduct some initial ESD current into the p-trigger nodes of the two stacked DTSCR devices between I/O pad and VSS line. Synchronously, the Mp2 will draw some initial ESD current out from the n-trigger nodes of the stacked DTSCR devices. The switching voltages of the two stacked DTSCR devices will be reduced to a low voltage level, therefore the two stacked DTSCR devices can be quickly triggered on. So, the ESD current can be discharged from I/O pad to the grounded VSS through the stacked DTSCR devices. However, the gate voltages of Mp1 and Mp2 may be charged up by the ESD energy through the forward-biased diodes Dp_1 and Dp_2, so the R1C1 time constant is designed to keep the gates of Mp1 and Mp2 at a relatively low voltage level. Then, the voltage pulses can be generated at the p-trigger and n-trigger node to successfully trigger on the stacked DTSCR devices during ESD stress conditions. With the double-triggered technique, the required pulse width to trigger the DTSCR into latching state can be shortened, as that shown in Fig. 4.6, so the RC time constant can be design smaller to save the layout area.

Under the ND-mode ESD-zapping condition (with grounded VDD but floating VSS), the gates of Mn1 and Mn2 are initially floating with a zero voltage level, thereby the Mn1 and Mn2 will be turned on due to the negative ESD voltage on the pad. So, the Mn1 will conduct some initial ESD current into the p-trigger nodes of the two stacked DTSCR devices between I/O pad and VDD line. Synchronously, the Mn2 will draw some initial ESD current out from the n-trigger nodes of the stacked DTSCR devices. Therefore, the two stacked DTSCR devices will be triggered on, and the ESD current can be discharged from I/O pad to the grounded VDD through the stacked DTSCR devices. Furthermore, the R2C2 time constant is also designed to avoid the gate voltages of Mn1 and Mn2 being charged up quickly through the parasitic diodes Dn_1 and Dn_2.

Under the NS-mode (PD-mode) ESD-zapping condition, the parasitic diodes Dn_1 and Dn_2 (Dp_1 and Dp_2) will be forward biased and turned on to discharge the ESD current

from I/O pad to the grounded VSS (VDD). The four modes (PS, NS, PD, and ND) of ESD stresses can be clamped to a very low voltage level by the stacked DTSCR devices or the forward-biased parasitic diodes, so the thinner gate oxide in deep sub-quarter-micron CMOS technologies can be fully protected. The diode in forward-biased condition can often sustain a much high ESD level. The ESD level of an I/O pad is dominated by the weakest ESD current path, so the experimental measurements in the following will be focused on the PS-mode and ND-mode ESD-zapping conditions.

Fig. 4.9(b) shows another ESD protection circuit designed with the stacked DTSCR devices for the I/O pad. When a PS-mode ESD zapping on the pad, the positive transient voltage on the pad is coupled through the capacitor C1 to the gates of Mn1 and Mn2. The Mn1 with a positive coupled gate bias can be turned on to conduct some ESD current from I/O pad into the p-trigger nodes of the two stacked DTSCR devices between I/O pad and VSS line. Synchronously, the Mn2 can be turned on to draw some ESD current out from the n-trigger nodes of the stacked DTSCR devices. Therefore, the two stacked DTSCR devices will be triggered on to discharge the ESD current from I/O pad to the grounded VSS. When an ND-mode ESD zapping on the pad, the negative transient voltage on the pad is coupled through the capacitor C2 to the gates of Mp1 and Mp2. The Mp1 with a negative coupled gate bias can be turned on to conduct some ESD current into the p-trigger nodes of the two stacked DTSCR devices between I/O pad and VDD line. The Mp2 can be synchronously turned on to draw some ESD current out from the n-trigger nodes of the stacked DTSCR devices. Therefore, the stacked DTSCR devices will be triggered on to discharge the ESD current from I/O pad to the grounded VDD. When the NS-mode (PD-mode) ESD zapping on the pad, the ESD current can be discharged through the forward-biased parasitic diodes Dn_1 and Dn_3 (Dp_1 and Dp_3) to grounded VSS (VDD). The Dn_3 (Dp_3) is the parasitic diode in the drain of Mn1 (Mp2) to the P-sub (N-well). The parasitic Dn_1 and Dp_1 diodes in the stacked DTSCR have shown in Fig. 4.10.

During normal circuit operating conditions, the gates of Mn1 and Mn2 (Mp1 and Mp2) are biased at VSS (VDD) through the resistor R1 (R2) in Fig. 4.9(b). So, the Mn1, Mn2, Mp1, and Mp2 are all kept off, whenever the input signal is high or low at the pad in Fig. 4.9(b). The ESD protection circuits are designed to be inactive without interrupting the normal input or output signals. The C1 and C2 in Fig. 4.9(b) must be tuned at some suitable value, where the coupled voltage under normal circuit operating conditions is smaller than the threshold

voltage of NMOS / PMOS, but greater than the threshold voltage of NMOS / PMOS under ESD zapping conditions [38].

HSPICE is used to verify the functions of ESD-detection circuits on the ESD protection circuits for the I/O pad. The transient simulations on the ESD-detection circuit in Fig. 4.9(a) under PS-mode and ND-mode ESD zapping conditions are shown in Figs. 4.11(a) and 4.11(b), where R1=R2=100 kΩ, C1=C2=1 pF, and the device dimensions W/L of Mp1, Mp2, Mn1, and Mn2 are 10 μm/0.25 μm, 20 μm/0.25 μm, 10 μm/0.25 μm, and 5 μm/0.25 μm. Because the overdrive voltage (Vsg) of Mp2 is smaller than that of Mp1 under the same pad voltage, the Mp2 in Fig. 4.9(a) is designed with larger channel width than that of Mp1. In Fig. 4.11(a), when a 0-to-8 V voltage pulse with a rise time of 10 ns is applied to the I/O pad of Fig. 4.9(a), the substrate-triggered and well-triggered currents can be synchronously generated by the ESD-detection circuit, which is formed by R1, C1, Mp1, and Mp2, to trigger on the stacked DTSCR devices. In Fig. 4.11(b), the substrate-triggered and well-triggered currents can be also synchronously generated by the ESD-detection circuit, which is formed by R2, C2, Mn1, and Mn2, when a 0-to-(-8) V negative voltage pulse with a fall time of 10ns is applied to the I/O pad of Fig. 4.9(a). Because of the difference of the overdrive voltage between Mn1 and Mn2, the Mn1 in Fig. 4.9 is designed with larger channel width than that of Mn2. On the other hand, the transient simulations on the ESD-detection circuit in Fig. 4.9(b) under PS-mode and ND-mode ESD zapping condition are shown in Figs. 4.11(c) and 4.11(d), where R1=R2=50 kΩ, C1=C2=50 fF, and the device dimensions W/L of Mn1, Mn2, Mp1, and Mp2 are 30 μm/0.25 μm, 10 μm/0.25 μm, 30 μm/0.25 μm, and 50 μm/0.25 μm. Because of the difference of the overdrive voltage between Mn1 and Mn2 (Mp1 and Mp2), the Mn1 (Mp2) in Fig. 4.9(b) is designed with larger channel width than that of Mn2 (Mp1). When a 0V-to-8 (-8) V positive (negative) voltage pulse with a rise (fall) time of 10 ns is applied to the I/O pad of Fig. 4.9(b), the substrate-triggered and well-triggered currents can be also synchronously generated by the ESD-detection circuit, which is formed by R1, C1, Mn1, and Mn2 (R2, C2, Mp1, and Mp2), to trigger on the stacked DTSCR devices. From the simulation results in Fig. 4.11, the trigger currents at the p-trigger and n-trigger nodes can be generated almost following the voltage pulse on the I/O pad. The delay resulting from the ESD-detection circuit in Fig. 4.9 can be almost neglectable. The triggered currents, which are the functions of resistance (R1, R2), capacitance (C1, C2), and device dimensions of PMOS devices and NMOS devices, can be fine tuned by HSPICE simulator to fit the practical

applications in different CMOS processed.

4.2.2 ESD Clamp Circuit between the Power Rails

The stacked DTSCR devices can be also applied to design the power-rail ESD clamp circuit. The VDD-to-VSS ESD clamp circuit designed with the two stacked DTSCR devices is realized in Fig. 4.12 for the circuit applications of 2.5 V. The functions of the ESD-detection circuit, which is formed with resistor (R), capacitor (C), and inverters (inv_1 and inv_2), is to distinguish VDD power-on event (with a rise time of ~ms) or ESD-stress events (with a rise time of ~ns) [11]. During normal VDD power-on transition (from low to high), the input of the inv_1 can follow up in time with the power-on VDD waveform, so the output of the inv_1 (or the input of the inv_2) will be biased at zero. Therefore, the output of the inv_2 will be kept at VDD. The p-trigger / n-trigger nodes of stacked DTSCR devices are biased at VSS / VDD in this situation, so the two stacked DTSCR devices are kept off and do not interfere with the normal circuit operating functions.

When a positive ESD voltage is applied to VDD with VSS relatively grounded, the RC delay will keep the input of the inv_1 at a relatively low voltage level for a long time. Therefore, the output of the inv_1 (or the input of the inv_2) will become high, and then the output of the inv_2 will be kept at a low voltage level. Thus, the p-trigger current and n-trigger current voltage pulses can be synchronously generated to trigger on the two stacked DTSCR devices. ESD current is discharged from VDD to VSS through the stacked DTSCR devices. When a negative ESD voltage is applied to VDD with VSS relatively grounded, the negative ESD current can be discharged through the forward-biased P-sub (VSS)-to-N-well (which is connected to VDD) parasitic diode in the ESD protection circuit.

4.2.3 ESD Robustness

The human-body-model (HBM) and machine-model (MM) ESD stresses are applied to the ESD protection circuits to verify their ESD robustness. The HBM ESD test results on the stacked DTSCR devices in the device level (without ESD-detection circuit) and the circuit level (with ESD-detection circuit) are compared in Fig. 4.13. In these ESD verifications, the failure criterion is defined as the leakage current of the device or circuit after ESD stresses is greater than 1 μA under the voltage bias of 2.5 V. For device level, the HBM ESD levels of

the 2DTSCR, 3DTSCR, and 4DTSCR (without ESD-detection circuit) are 7, 4, and 1.5 kV, respectively. In the layout, each DTSCR device in the stacked configuration is close to save the layout area, so the power (thermal) dissipation among the stacked DTSCR devices will interact to reduce the ESD robustness of stacked DTSCR devices. From other aspect, because the total holding voltage of stacked DTSCR configuration is increased with the increase of the number of the stacked DTSCR devices, the HBM ESD robustness of the stacked DTSCR devices is decreased due to power = $I_{ESD} \times V_{hold}$. But, the ESD levels of the stacked DTSCR devices can be greatly improved for the 3DTSCR or 4DTSCR, if the desired ESD-detection circuit is used to trigger the stacked DTSCR devices on. From Fig. 4.13, the ESD levels of the stacked DTSCR devices with ESD-detection circuit are all boosted up to >8 kV. The measurement results on the MM ESD levels of the stacked DTSCR devices with or without ESD-detection circuit are shown in Fig. 4.14. The MM ESD level is also decreased when the number of stacked DTSCR devices is increased. However, the MM ESD levels of the stacked DTSCR devices can be also improved if the desired ESD-detection circuit is used to trigger the stacked DTSCR devices on. The MM ESD levels of the 2DTSCR, 3DTSCR, and 4DTSCR (with ESD-detection circuit) are 700, 525, and 375 V, respectively.

The TLP-measured I-V curves of the two stacked DTSCR devices with or without ESD-detection circuit depicted in Fig. 4.12 are shown in Fig. 4.15. The stacked DTSCR devices with ESD-detection circuit can be triggered on at a lower voltage level of ~2 V, however, the stacked DTSCR devices without ESD-detection circuit can not be triggered on until a higher voltage level of ~30 V. Moreover, the It2 of the stacked DTSCR device with ESD-detection circuit can be improved, which is in accordance with the results in Fig. 4.13. This has confirmed that the ESD-detection circuit proposed in this chapter can indeed reduce the switching voltage of DTSCR and enhance its ESD robustness.

4.2.4 Turn-On Verification

In order to verify the function of the ESD protection circuit in Fig. 4.12, a voltage pulse with a pulse width of 400 ns and rise time of 10 ns is applied to VDD of Fig. 4.12 with grounded VSS. In Fig. 4.16, a 0-to-5 V voltage pulse applied on the VDD line is clamped to ~3 V by the turned-on 2DTSCR. This implies that the ESD-detection circuit realized with the R, C, inv_1, and inv_2 can indeed generate the required double-triggered currents. The

stacked DTSCR devices can be successfully triggered into latching state without involving the junction avalanche breakdown mechanism. The clamped voltage of ~3 V has also verified that the proposed ESD protection circuits with two stacked DTSCR devices are free to latchup issue under normal operating conditions.

4.3 SUMMARY

The novel DTSCR device used for on-chip ESD protection circuits has been successfully investigated in a 0.25-μm salicided CMOS process. With both the substrate and N-well triggered currents, the switching voltage and turn-on time of DTSCR device can be successfully reduced to only ~1.5 V and ~10 ns, respectively. For IC applications with VDD of 2.5 V, the ESD protection circuits designed with two DTSCR devices in stacked configuration and ESD-detection circuits have a clamp voltage of ~3 V, which are free to latchup issue. Such ESD protection circuits can sustain the HBM (MM) ESD level per area of >10 V/μm^2 (0.88 V/μm^2) in a 0.25-μm fully salicided CMOS process without using extra process modification.

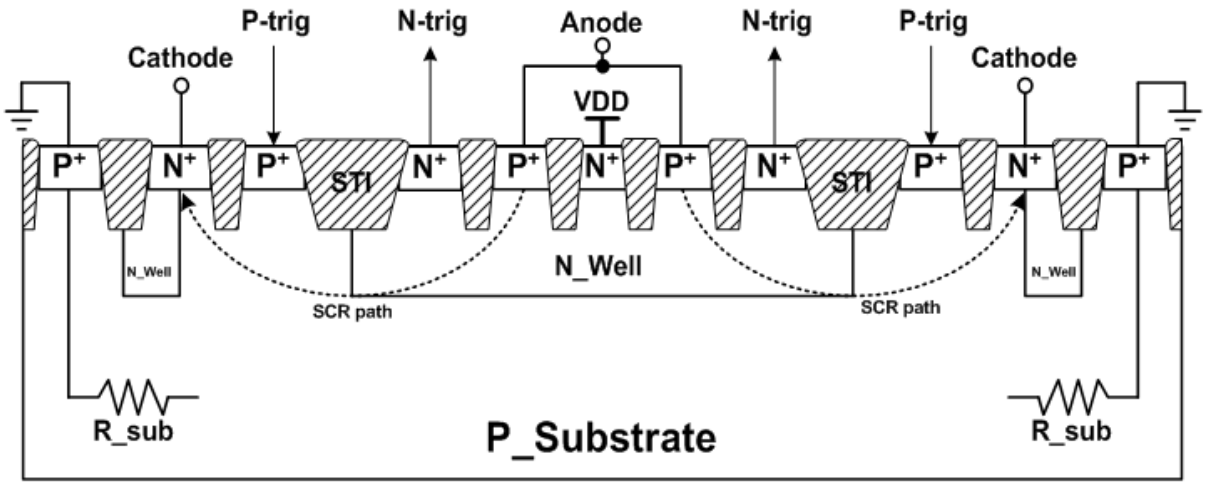


Fig. 4.1 Device structure of the double-trigger SCR (DTSCR) device.

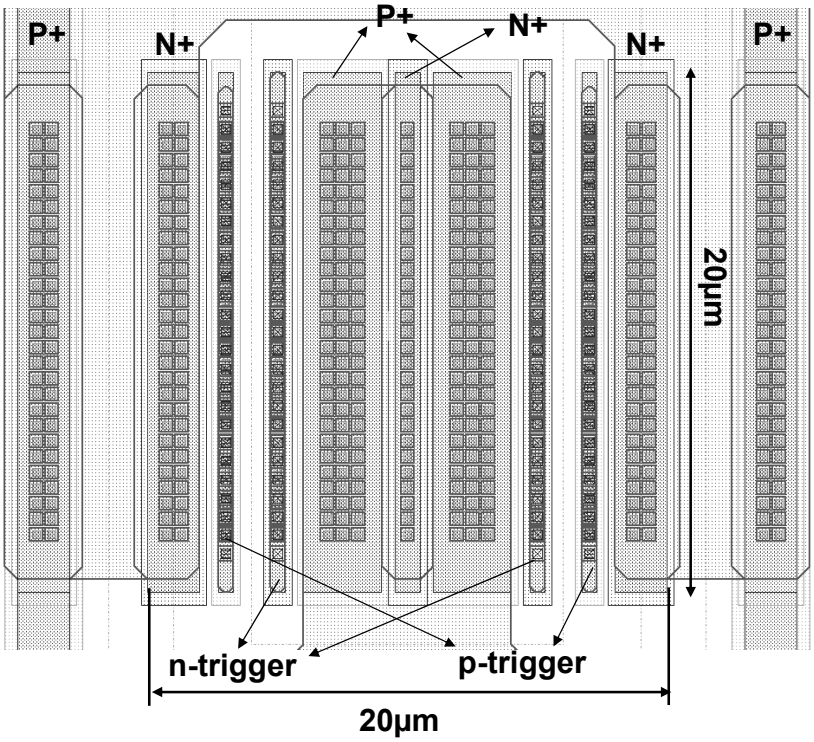


Fig. 4.2 The layout top view of the DTSCR device.

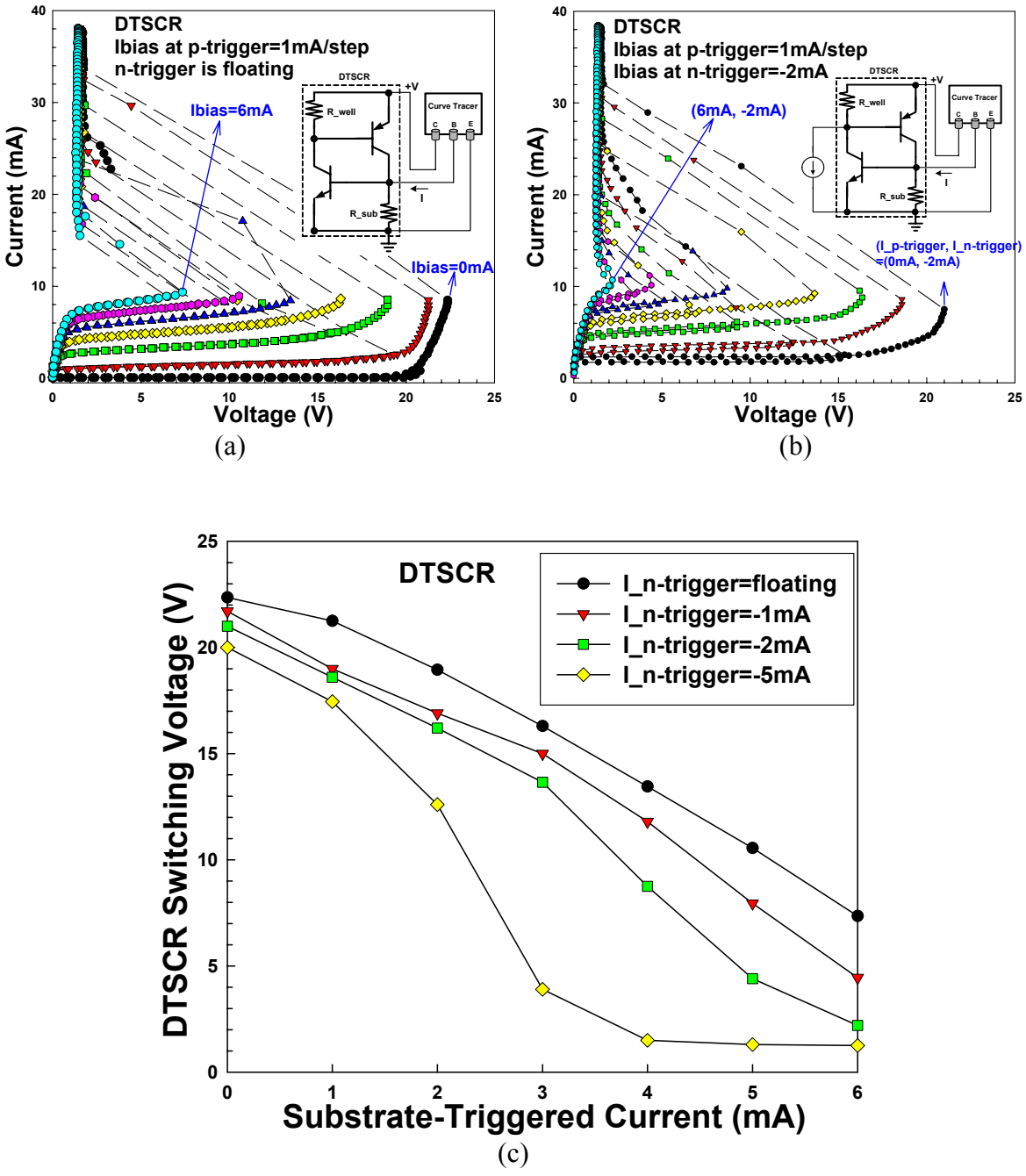
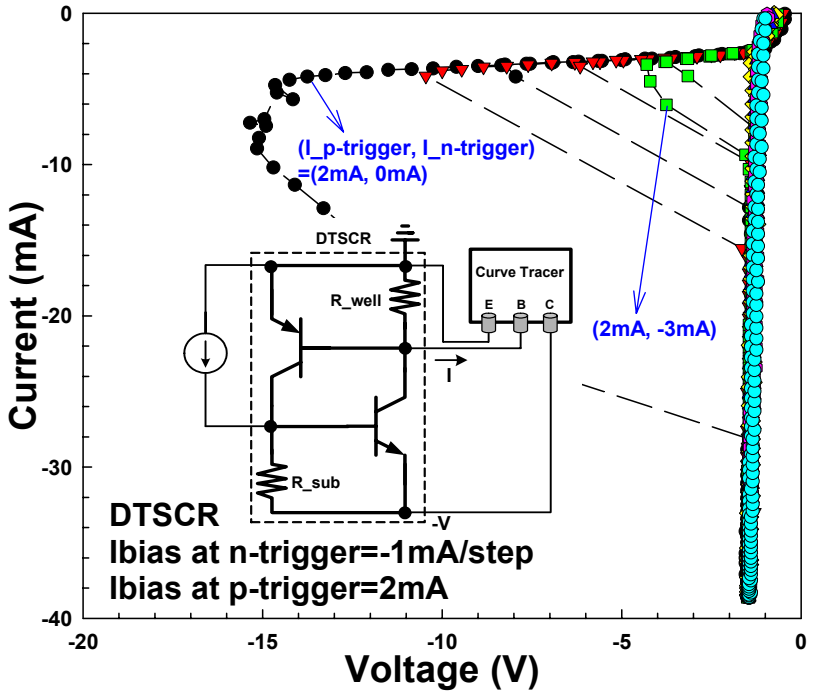
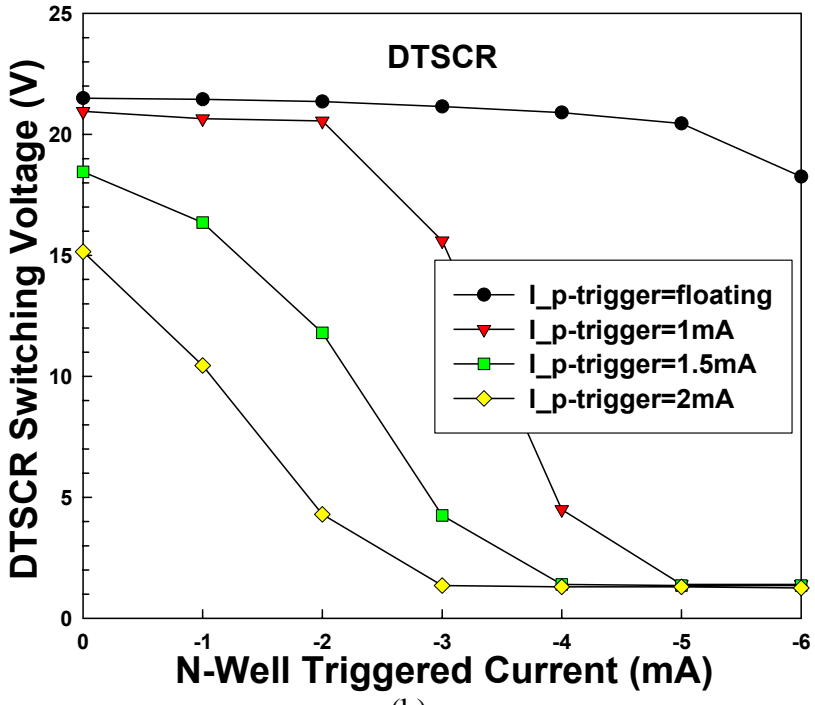


Fig. 4.3 (a) The measurement setup and measured DC I-V curves of DTSCR under different substrate-triggered currents but no N-well triggered current. (b) The measured DC I-V curves of DTSCR under different substrate-triggered currents and the additional N-well triggered current of -2 mA. (c) The dependence of switching voltage of DTSCR on substrate-triggered current under different N-well triggered currents.



(a)



(b)

Fig. 4.4 (a) The measurement setup and measured DC I-V curves of DTSCR under different n-trigger currents and the substrate-triggered current of 2 mA. (b) The dependence of switching voltage of DTSCR on the N-well triggered current under different substrate-triggered currents.

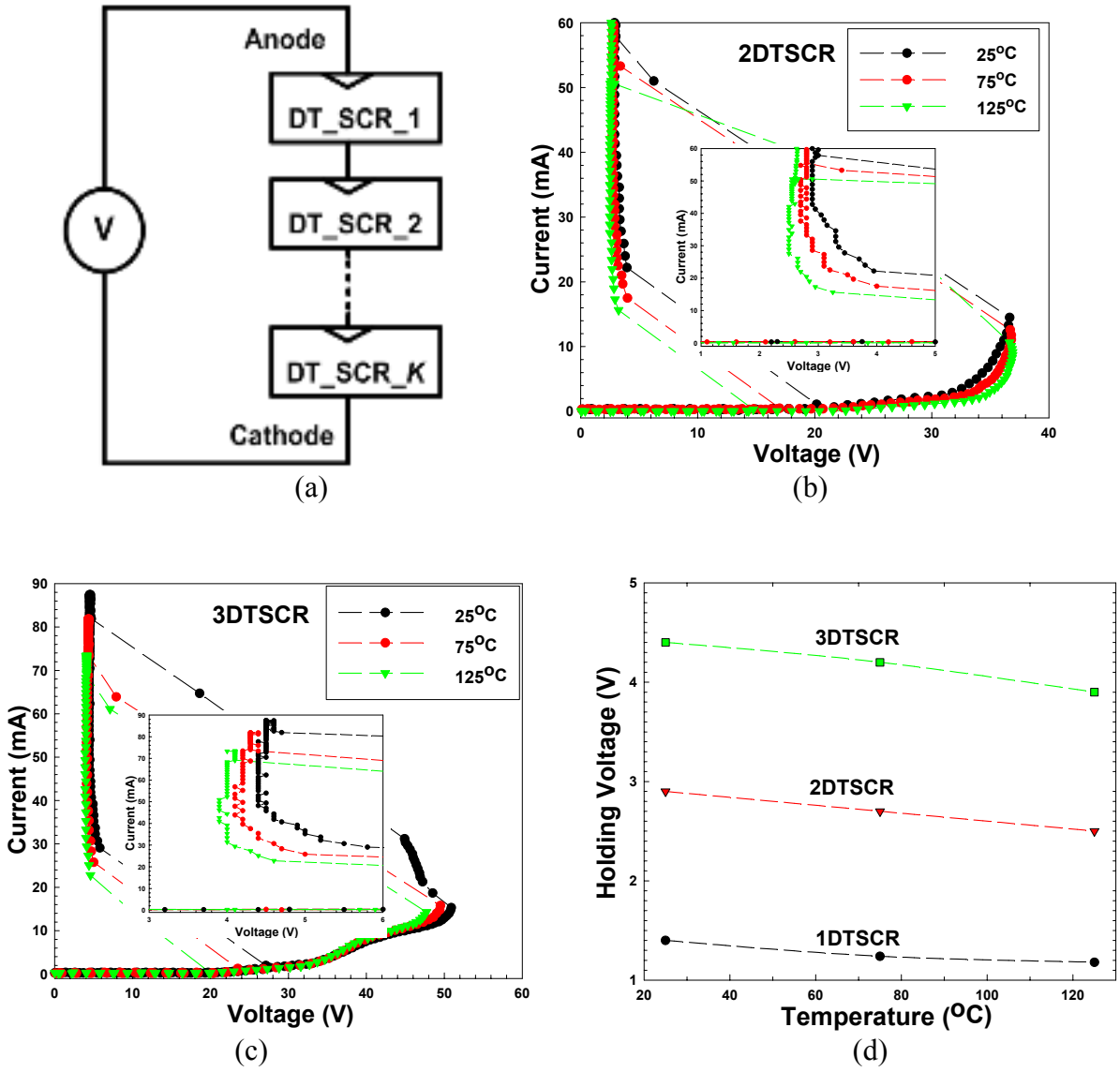
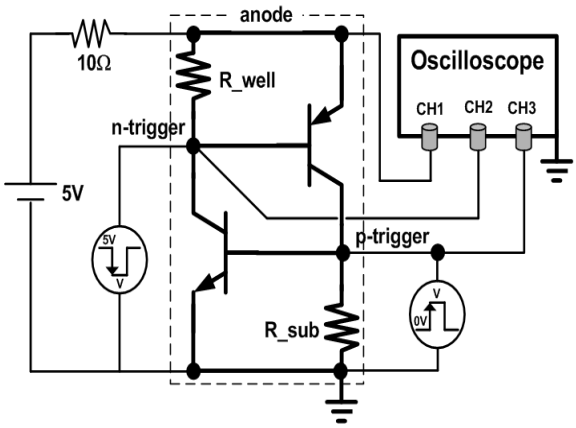
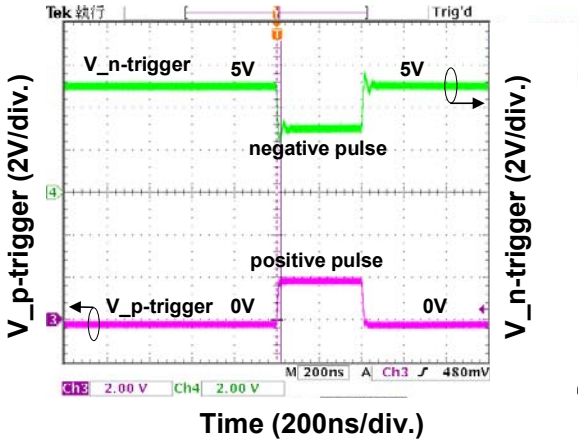


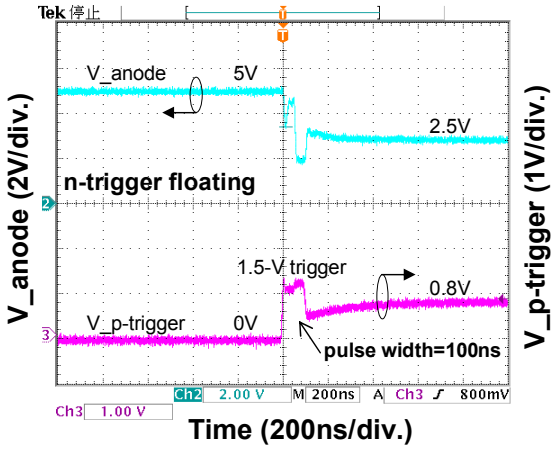
Fig. 4.5 The temperature dependence on the total holding voltage of the stacked DTSCR devices with different stacked numbers. (a) Experimental measurement setup, (b) the measured I-V curves of two DTSCR devices in stacked configuration (2DTSCR), (c) the measured I-V curves of three DTSCR devices in stacked configuration (3DTSCR), and (d) the relation between the holding voltage and the temperature under different numbers of stacked DTSCR devices.



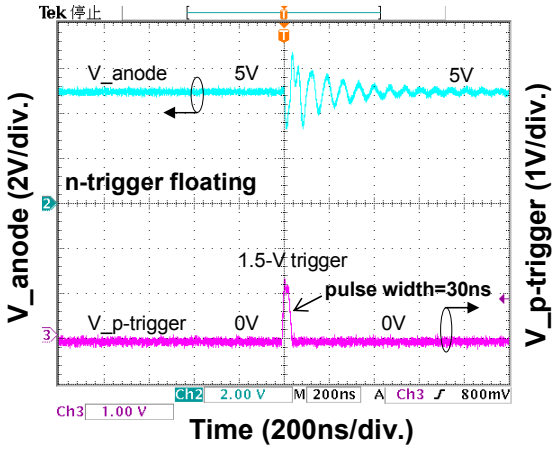
(a)



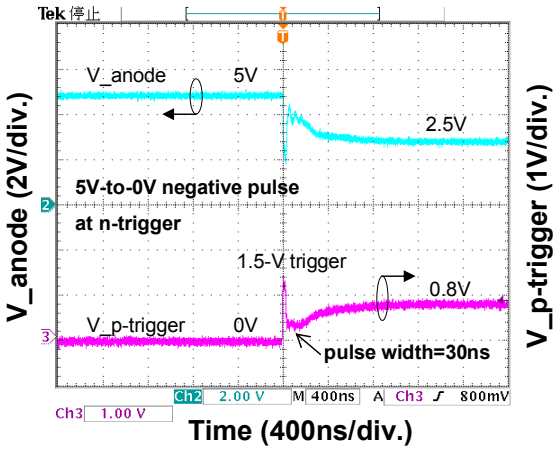
(b)



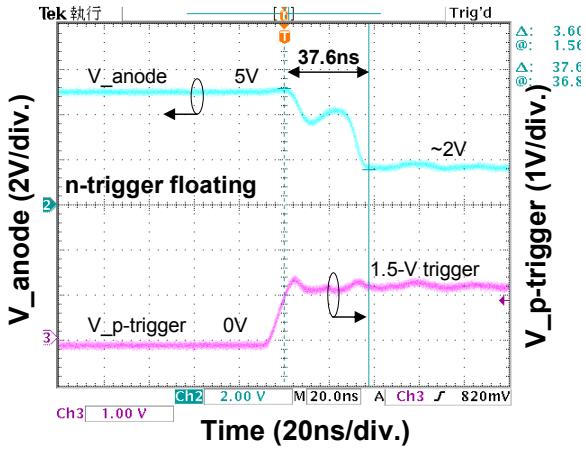
(c)



(d)

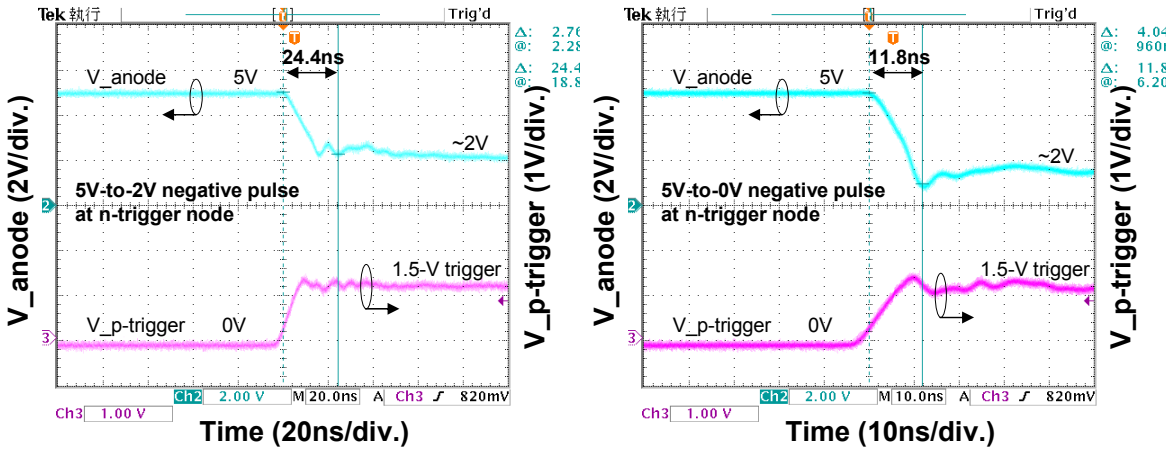


(e)



(f)

(continued to the next page for Fig. 4.6)



(g) (h)

Fig. 4.6 The turn-on verification of DTSCR under different voltage pulses. (a) The measurement setup. (b) Synchronous positive and negative voltage pulses. The measured voltage waveforms on the anode and p-trigger nodes of the DTSCR device under 1.5-V positive voltage pulse with pulse width of (c) 100 ns, (d) 30 ns, while n-trigger is floating, and (e) 30 ns while 5-to-0 V negative voltage pulse is applied to n-trigger. The close-up views of the V_anode at the falling edge while the DTSCR is synchronously triggering by the 1.5-V positive voltage pulse and under the negative voltage pulse of (f) floating, (g) 5-to-2 V, and (h) 5-to-0 V.

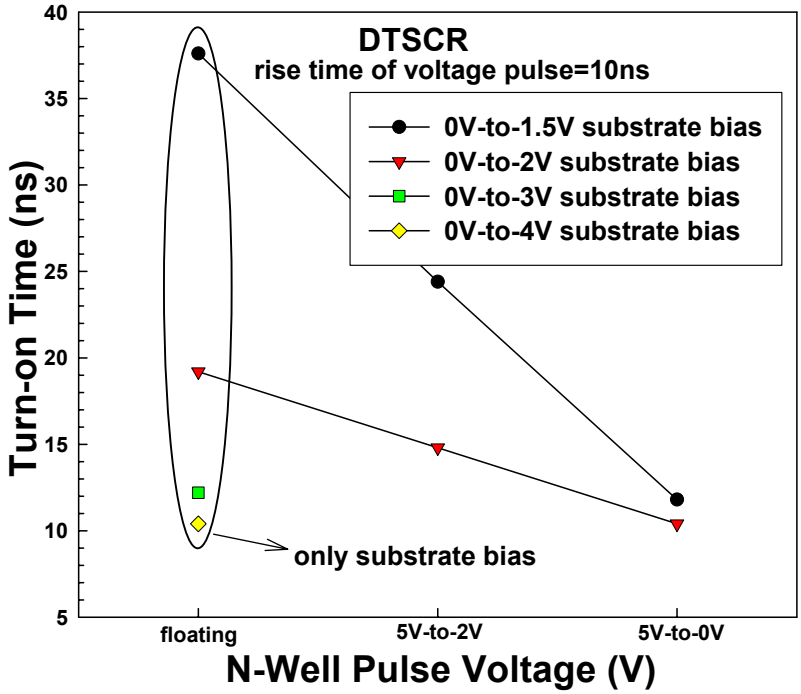


Fig. 4.7 The dependence of turn-on time of DTSCR on the N-well biases under different substrate bias conditions with a fixed rise time of 10 ns.

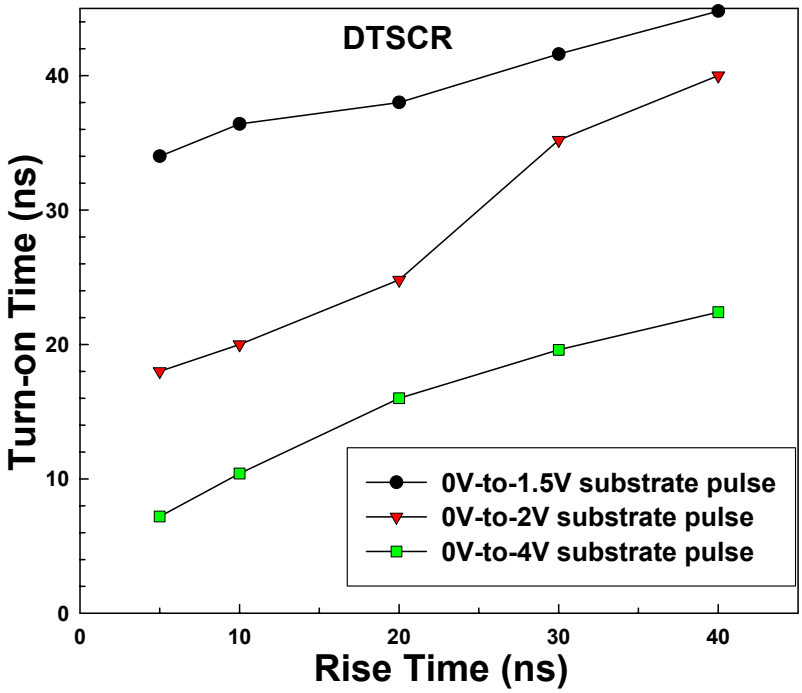
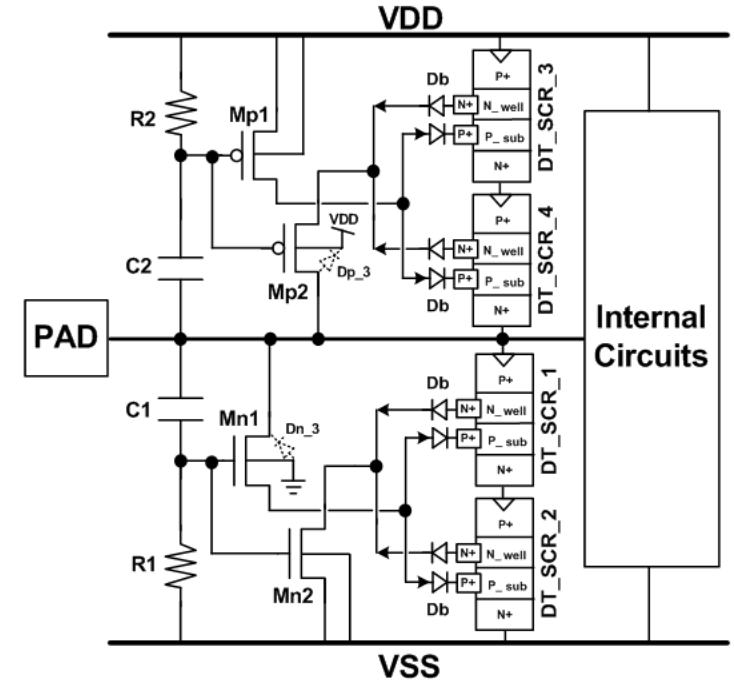
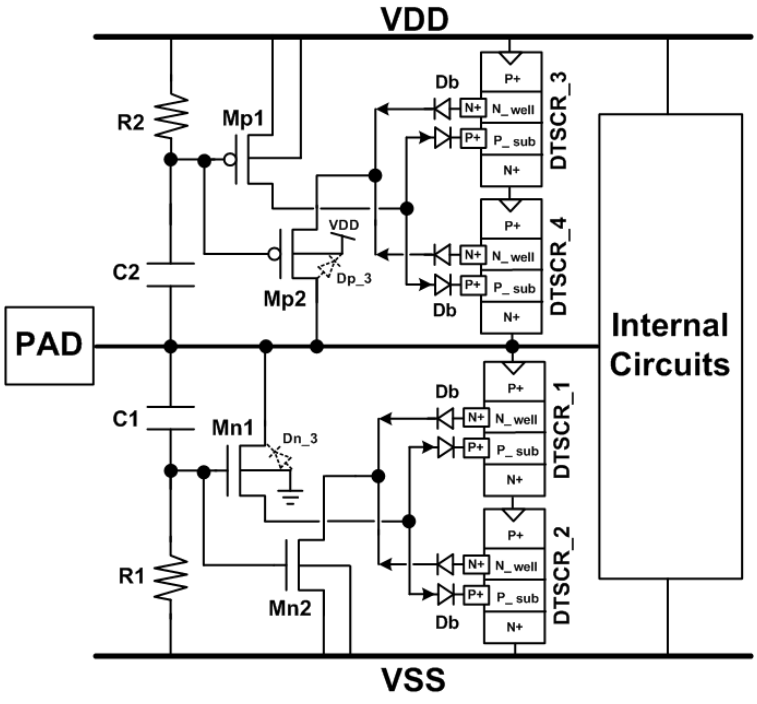


Fig. 4.8 The dependence of turn-on time of DTSCR on the rise time of voltage pulse under different substrate bias conditions.



(a)



(b)

Fig. 4.9 Design of ESD protection circuits for the input or output pad with the proposed DTSCR devices by using (a) RC delay, and (b) gate coupled, circuit techniques.

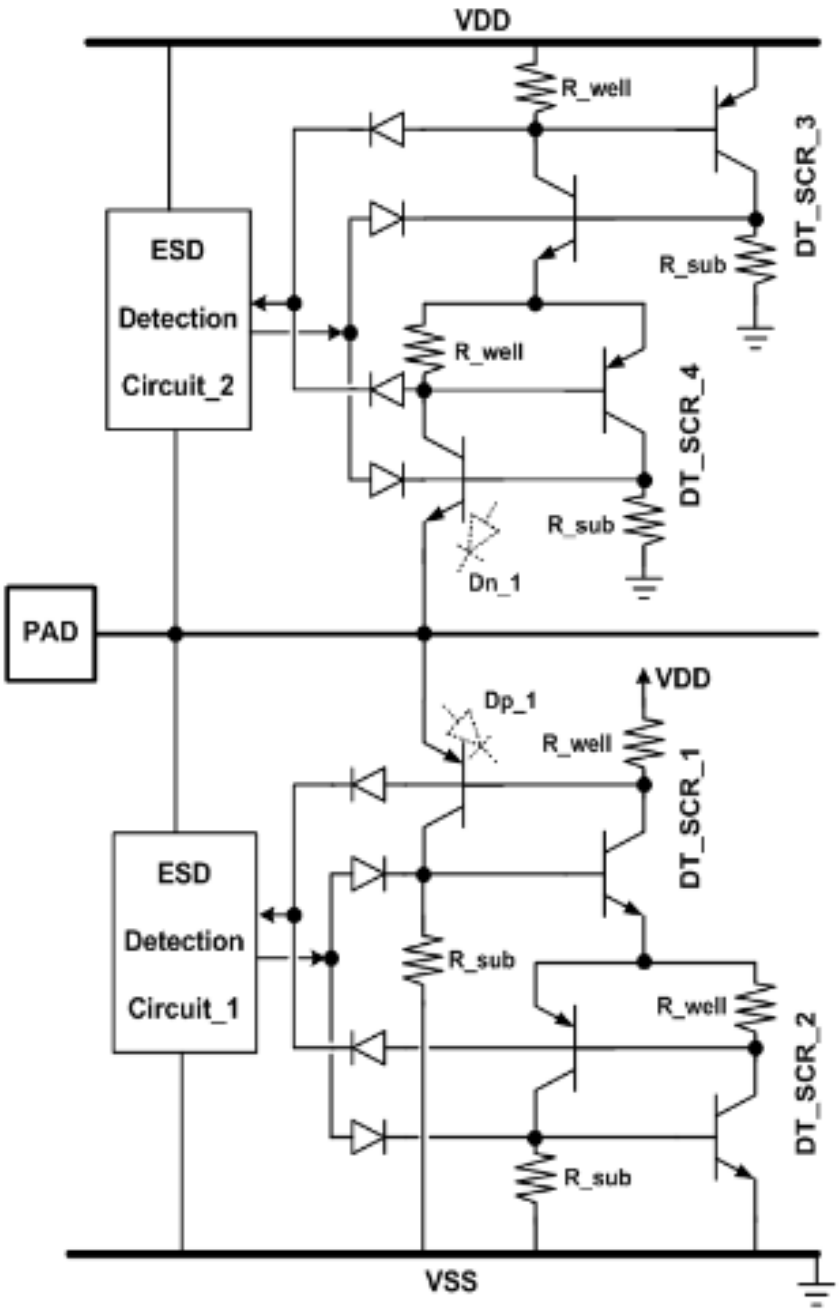


Fig. 4.10 The equivalent circuit of the stacked DTSCR devices for the input or output pad.

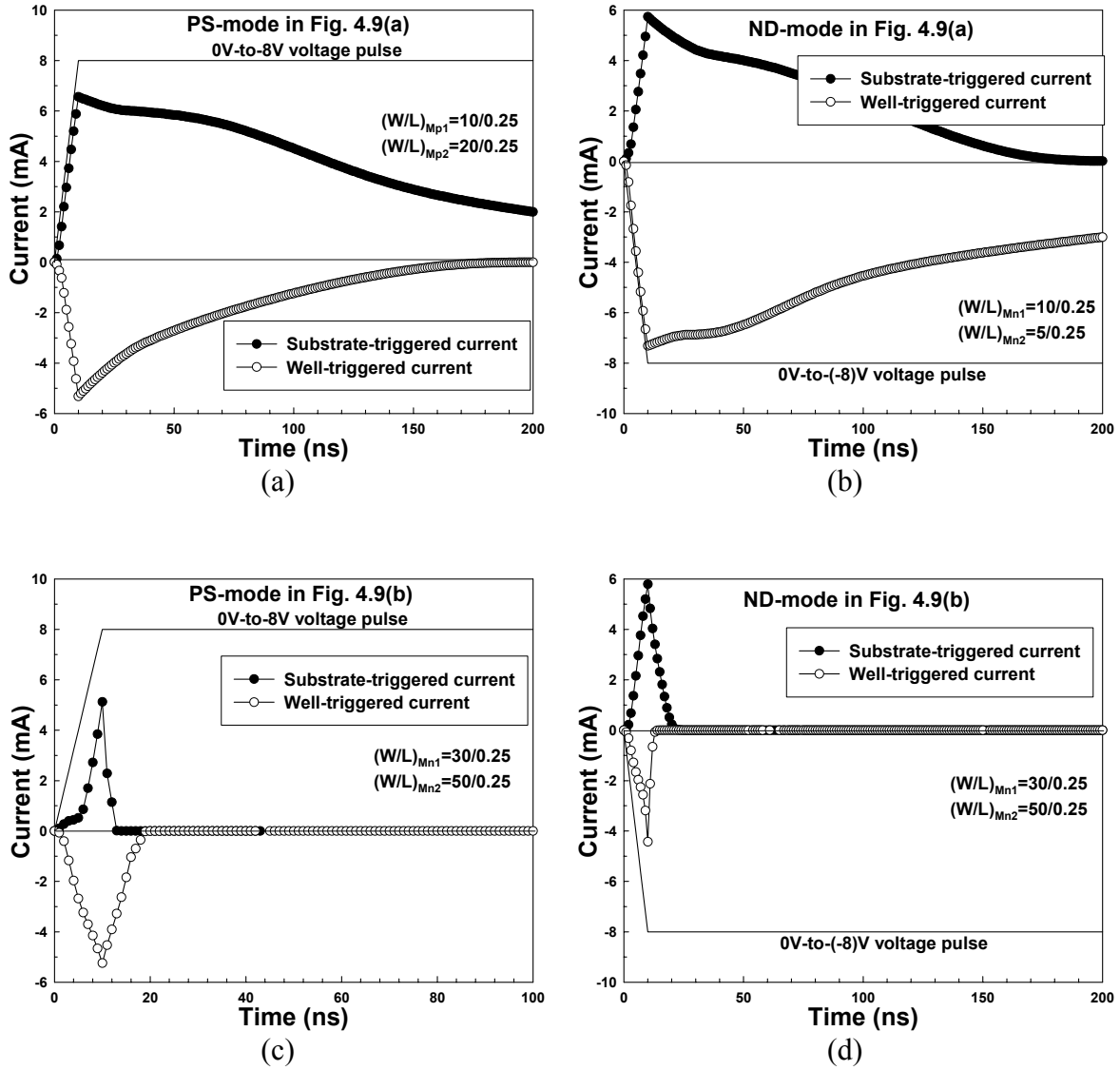


Fig. 4.11 HSPICE simulation. The transient simulation on the ESD-detection circuit in Fig. 4.9(a) under (a) PS-mode, and (b) ND-mode, ESD-zapping conditions and in Fig. 4.9(b) under (c) PS-mode, and (d) ND-mode, ESD-zapping conditions.

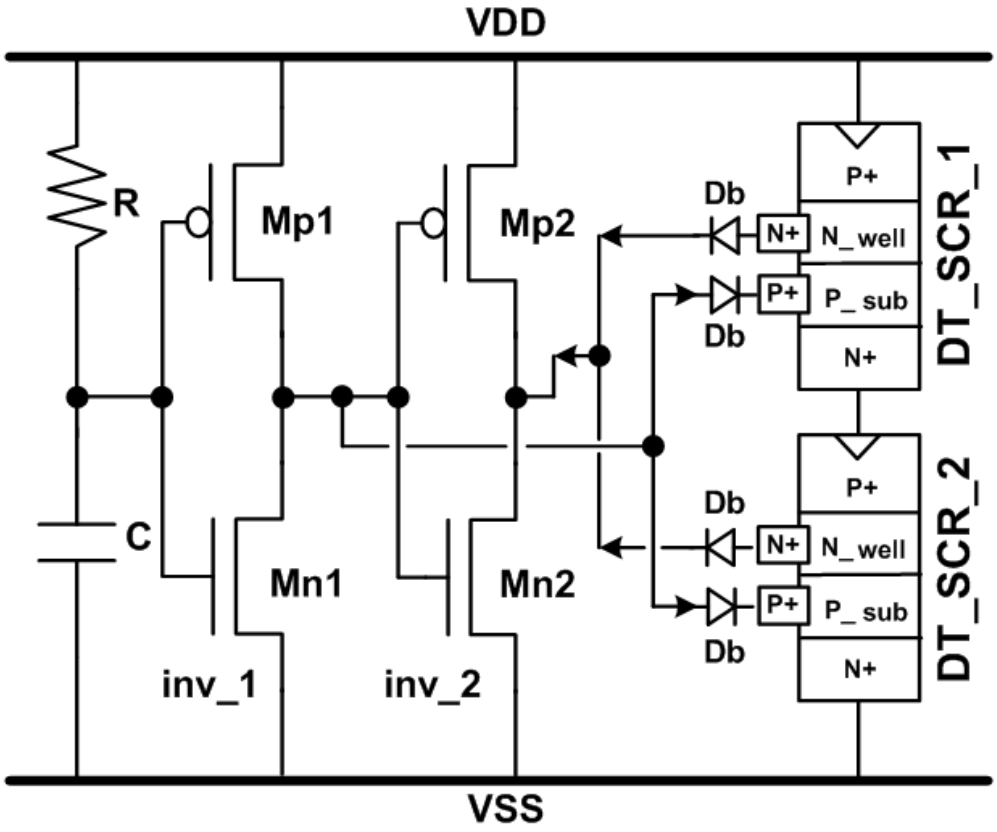


Fig. 4.12 The power-rail ESD clamp circuit designed with two stacked DTSCR devices and ESD-detection circuit.

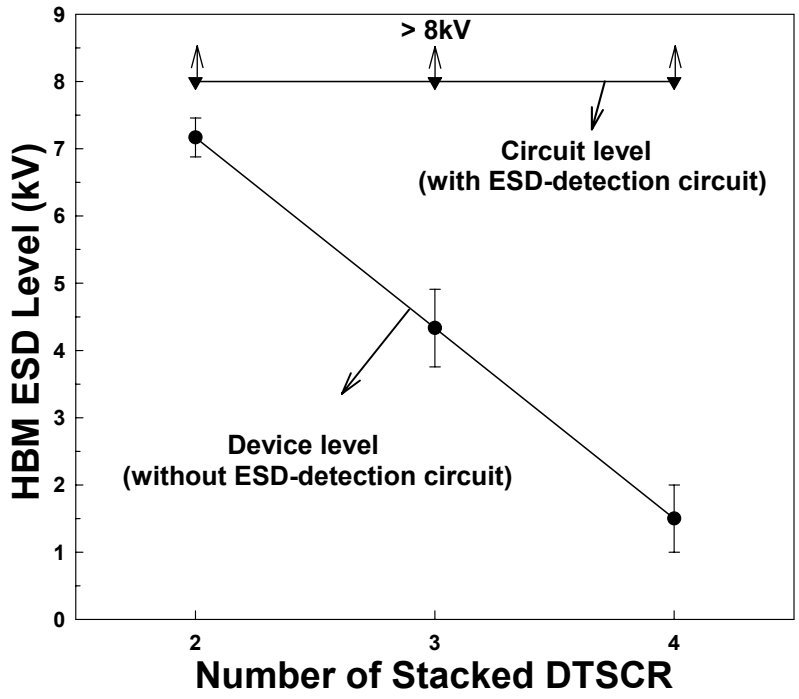


Fig. 4.13 Dependence of the HBM ESD levels of stacked DTSCR configuration on the number of the stacked DTSCR devices (Failure criterion: $I_{Leakage}$ > 1 μA @ 2.5 V bias).

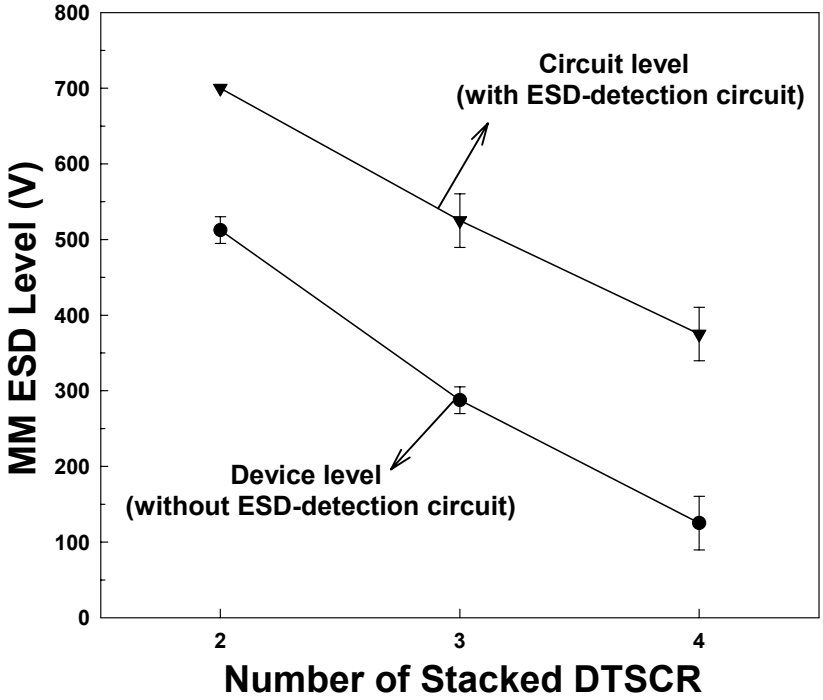


Fig. 4.14 Dependence of the MM ESD levels of stacked DTSCR configuration on the number of the stacked DTSCR devices (Failure criterion: $I_{Leakage}$ > 1 μA @ 2.5 V bias).

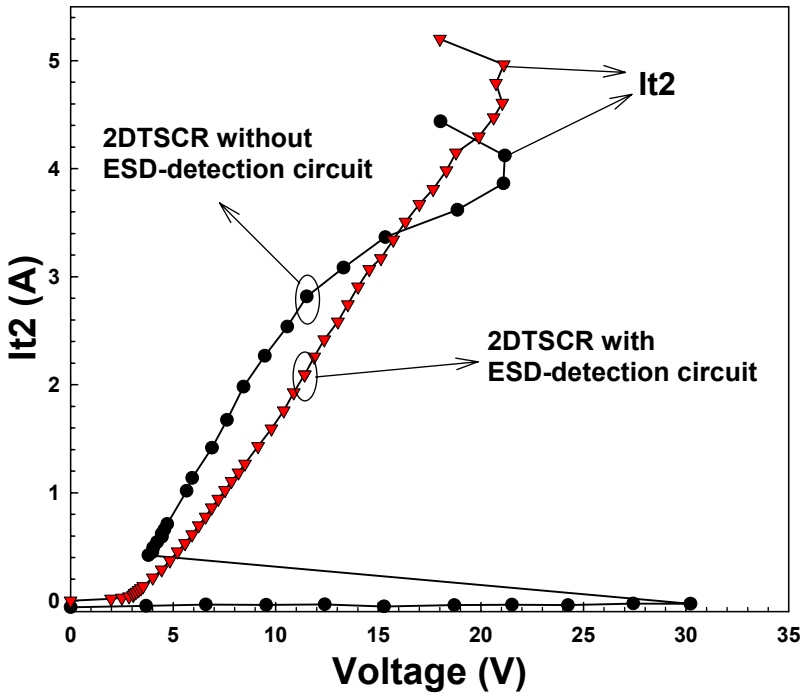


Fig. 4.15 The TLP-measured I-V curves of the two stacked DTSCR devices with or without ESD-detection circuit (Failure criterion: $I_{Leakage} > 1$ μA @ 2.5 V bias).

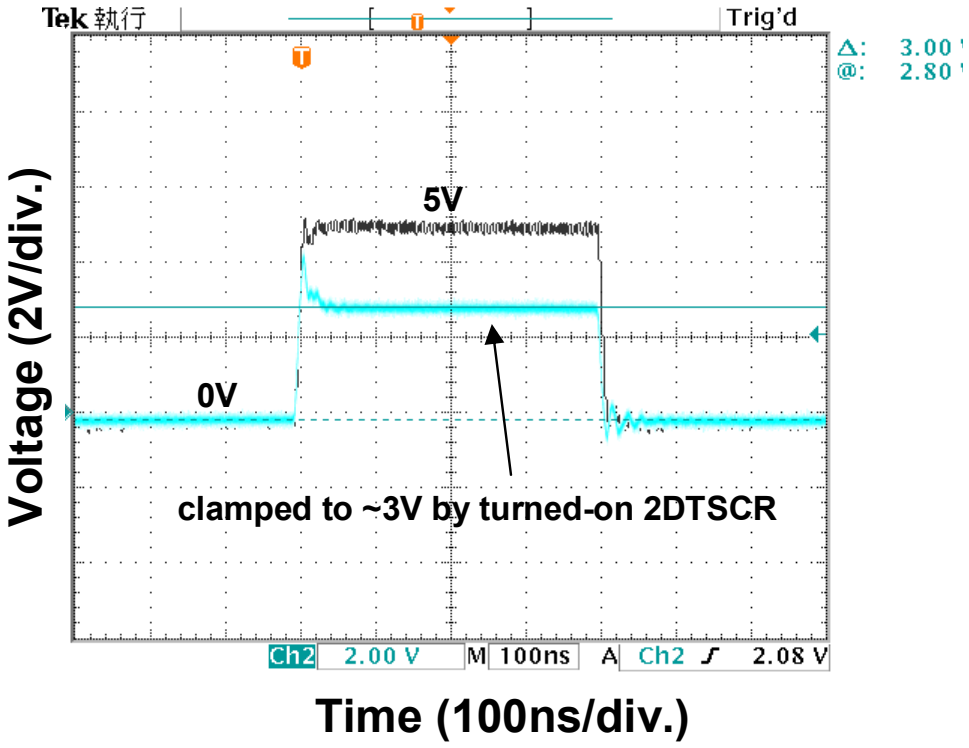


Fig. 4.16 The measured voltage waveforms to verify the turn-on efficiency of the power-rail ESD clamp circuit with two stacked DTSCR devices.

CHAPTER 5

SCR DEVICE FABRICATED WITH DUMMY-GATE STRUCTURE

In this chapter, a novel dummy-gate structure is used to block the shallow trench isolation (STI) and silicide between the diffusion regions in the SCR device, and therefore to further enhance its turn-on speed and CDM ESD levels [40]-[42]. The fabrication of the proposed SCR device with dummy-gate structure is fully process-compatible to general CMOS process, without using extra mask layer or increasing process step. The fully-silicided STSCR with dummy-gate structure has the advantages of lower switching voltage, lower clamping voltage, smaller turn-on resistance, and faster turn-on speed, as compared to the STSCR with STI. With suitable ESD-detection circuit, the STSCR with dummy-gate structure is designed to be kept off during the normal circuit operating conditions, and to be quickly triggered on during the ESD-zapping conditions. Therefore, the ultra-thin gate oxide in deep submicron CMOS processes can be effectively protected by the STSCR with dummy-gate structure. In the future nanoscale CMOS process with VDD below 1.2 V, the latchup concern will be eliminated, because the holding voltage of SCR device is greater than the maximum voltage level of VDD.

5.1 SCR DEVICE WITH DUMMY-GATE STRUCTURE

The normal fully-silicided substrate-triggered SCR (STSCR) device with STI structure [24] is shown in Fig. 5.1(a). In a typical 130-nm CMOS process, the depth of STI is about ~0.4 μm, but the junction depth of P+ / N+ diffusion is only about ~0.15 μm. The deeper STI region in SCR device causes a longer current path from the anode to the cathode, which also leads to a slower turn-on speed of SCR. In order to further enhance the turn-on speed of STSCR device, the STI structure must be blocked. In nanoscale CMOS processes, the STI region is defined by the active area (thin oxide) mask. Then, the P+ / N+ diffusions regions

will be formed through the definition of implantation masks. In such a typical process flow, the STI regions between diffusions in active area can be blocked. But, the extra silicide-blocking mask must be used to block the silicide between diffusions in the fully-silicided CMOS processes, otherwise the anode and the cathode of SCR device will become short circuit. The STSCR with silicide-blocking structure is shown in Fig. 5.1(b). To achieve more high performance of circuit operation, some advanced circuit designs did not wish to use the silicide-blocking mask in the I/O circuits. To increase the ESD robustness of I/O circuits but not using the silicide-blocking mask, some layout techniques had been invented to improve ESD levels of NMOS device [59]-[61]. Moreover, with the extra silicide-blocking mask, the process flows and total fabrication costs will be increased. In this work, a dummy-gate structure is proposed to block the silicide and STI between the diffusion regions in SCR device without adding extra process masks and increasing the fabrication costs.

The proposed STSCR device with dummy-gate structure is shown in Fig. 5.1(c). The ESD current paths in these STSCR devices are indicated by the dashed lines in Figs. 5.1(a)-5.1(c). The ESD current path in Fig. 5.1(c) is the shortest, because the spacing between the diffusion regions isolated by the dummy-gate structure is the smallest design rule in CMOS process, and the deeper STI regions do not exist in the ESD current path in Fig. 5.1(c). The turn-on speed of STSCR with dummy-gate structure will have the better benefits than that of STSCR with STI or silicide-blocking structure. Thus, in this chapter, the device characteristics and ESD performance of STSCR with dummy-gate structure will be investigated in detail. As compared with the traditional LSCR device structure, the extra P+ diffusions are inserted into the STSCR device structure. The inserted P+ diffusions are connected out as the p-trigger node of the STSCR. When a trigger current is applied into the trigger node, the base voltage of NPN will be raised up due to the substrate resistor (R_sub). As long as the base voltage of NPN is greater than 0.7 V, the NPN bipolar transistor in SCR structure is active. The collector current of NPN is generated to trigger on the PNP bipolar transistor. When the PNP transistor is turned on, the collector current of PNP is in turn generated to further bias the NPN transistor. The positive-feedback regenerative mechanism of SCR latching process [35], [36] is initiated by the substrate-triggered current. Finally, the STSCR will be successfully triggered on into its latching state to discharge ESD current.

For on-chip ESD protection purpose, the corresponding ESD-detection circuit [24]-[26]

has to be designed to control the turn-on of this STSCR with dummy-gate structure. The ESD-detection circuits can be designed according to the principle of RC delay (used to distinguish ESD-zapping events or the normal circuit operating conditions) or the gate-coupled circuit technique (used to generate the trigger current) to turn on this STSCR device during ESD-zapping conditions. With the suitable ESD-detection circuit, the STSCR with dummy-gate structure is designed to be kept off without interfering the I/O signals during the normal circuit operating conditions, and to be quickly triggered on to discharge ESD current during the ESD-zapping conditions. So, the STSCR with dummy-gate structure can be successfully used in the input, output, and power-rail ESD protection circuits. For avoiding the latchup issue in STSCR device, the voltage drop elements (such as diodes or STSCR devices) can be stacked with the dummy-gate blocking STSCR device to elevate its total holding voltage in the bulk CMOS process. As long as the total holding voltage of ESD protection device (including the STSCR and the voltage drop elements) is greater than the maximum voltage level of VDD, the latchup concern inherent in SCR structure can be eliminated during normal circuit operating conditions.

5.2 EXPERIMENTAL RESULTS

5.2.1 Device Characteristics

The two fully-silicided STSCR devices with STI and dummy-gate structures have been fabricated with the same layout area in a 0.25-μm CMOS process. The active areas (without including the guard rings) of these two STSCR devices in the test chip are 20 μm×20 μm. The measurement setup to find the DC I-V curves of the fabricated SCR devices under substrate-triggering technique is shown in Fig. 5.2(a). The DC I-V curves of STSCR with STI and dummy-gate structures under different substrate-triggered currents are shown in Figs. 5.2(b) and 5.2(c), respectively. When the substrate-triggered current applied at the p-trigger node is increased from 0 to 6 mA, the switching voltage of STSCR with STI is reduced from ~22 to ~7 V, whereas that of STSCR with dummy-gate structure is reduced from ~18 to ~3 V. With the substrate-triggered current, both of the STSCR with STI and dummy-gate structures can be triggered into latching state without involving the avalanche breakdown mechanism

[33], [34]. The dependences of the switching voltage of STSCR devices with STI and dummy-gate structures on the substrate-triggered current are compared in Fig. 5.3. If the trigger current is continually increased, the switching voltages of both STSCR devices will be nearly reduced to their holding voltages (~1.3 V). Moreover, the switching voltage of STSCR with dummy-gate structure can be further reduced lower than that of STSCR with STI under the same trigger current. This is related to the current gain (β) of parasitic bipolar transistor in SCR structure, which will be discussed later. The SCR device with lower switching voltage can clamp the ESD overstresses more quickly to effectively protect the thinner gate oxide of input circuits.

5.2.2 Turn-On Speed

The comparison of turn-on speed between a traditional LVTSCR [17] and the new STSCR with dummy-gate structure under an applied 0-to-8 V voltage pulse is shown in Fig. 5.4. The dummy-gate blocking STSCR with 0.9-V substrate bias is initially triggered on at ~2.5 V through the positive-feedback regenerative mechanism, but the LVTSCR is initially triggered on at a higher voltage level of 8 V through the drain avalanche breakdown of the inserted short-channel NMOS device. The 8-V voltage pulse is faster clamped to a stable low voltage level (~1.7 V) by the dummy-gate blocking STSCR with a 0.9-V substrate bias than by the traditional LVTSCR. The STSCR with dummy-gate structure has the lower switching voltage and faster turn-on speed than those of the LVTSCR device, if enough substrate bias is applied to STSCR device. Therefore, the new STSCR with dummy-gate structure is more suitable to protect the ultra-thin gate oxide of input stages against ESD overstresses.

In addition, the comparison of turn-on speed between the STSCR devices with STI and dummy-gate structures without any substrate bias applied at the p-trigger node is shown in Fig. 5.5. When a 0-to-10 V voltage pulse with 5-ns rise time is applied, the STSCR with dummy-gate structure can be triggered on to clamp the voltage pulse to a low voltage level, but the STSCR with STI can not be triggered on until a 0-to-11 V voltage pulse with 5-ns rise time is applied. Due to the dV/dt transient current, the dynamic switching voltages of STSCR devices are smaller than the static switching voltage of STSCR devices, as shown in Fig. 2. But, the dynamic switching voltage of STSCR with dummy-gate structure is still smaller than that of STSCR with STI. The STSCR with dummy-gate structure also has a lower clamping

voltage level (~1.9 V) that that (~2.4 V) of STSCR with STI. Moreover, the ESD-like voltage pulse can be faster clamped to a stable low voltage level by the STSCR with dummy-gate structure than by the STSCR with STI. This has proven that the turn-on speed of STSCR with dummy-gate structure is faster than that of STSCR with STI.

In order to further investigate the dependence of turn-on efficiency of the STSCR devices with STI and dummy-gate structures on substrate bias, the experimental setup to measure the required turn-on times of the STSCR devices is illustrated in Fig. 5.6(a). A 5-V voltage bias is connected to the anode of the STSCR device through a resistance of 10 Ω, which is used to limit the sudden large transient current from power supply when the STSCR is turned on. The turn-on time of STSCR is defined as the time for STSCR entering into its latching state. The measured turn-on times for STSCR devices with STI and dummy-gate structure are shown in Figs. 5.6(b) and 5.6(c), respectively. The V_anode is the voltage waveform on the anode of STSCR shown in Fig. 5.6(a). From Fig. 5.6(b), the turn-on time of STSCR with STI is reduced from 35, 20, to 11.2 ns, while the STSCR is triggering by the voltage pulse of 1.5, 2, and 4 V with 10-ns rise time into the p-trigger node, respectively. Moreover, from Fig. 5.6(c), the turn-on time of STSCR with dummy-gate structure is further reduced from 25.4, 13.6, to 9.8 ns under the same measurement conditions as those of Fig. 5.6(b). The comparison on the turn-on time between STSCR with STI and dummy-gate structures under different voltage pulses with 10-ns rise time applied at the p-trigger node is summarized in Fig. 5.7. With the increase of pulse voltage applied at the p-trigger node, the turn-on time of both STSCR devices with STI and dummy-gate structures will be reduced. Moreover, the turn-on time of STSCR with dummy-gate structure is further reduced shorter than that of STSCR with STI under the same substrate voltage pulse. The dependence of turn-on time of STSCR with dummy-gate structure on different rise times of voltage pulse under different substrate pulse conditions is shown in Fig. 5.8. With the reduction of pulse rise time, the turn-on time of STSCR with dummy-gate structure will be also shortened under the same substrate pulse voltage. When a 4-V substrate pulse with rise time of 5 ns is applied to the p-trigger node, the turn-on time of the STSCR with dummy-gate structure can be shortened to only 6.6 ns. So, the turn-on time of such STSCR with dummy-gate structure can trace the rise time of ESD event (even the CDM stress) to efficiently protect the ultra-thin gate oxide, if the high enough voltage pulse has been applied to the STSCR device. For CMOS IC applications with ultra-thin gate oxide, the dummy-gate blocking STSCR device

with faster turn-on speed can be designed to protect the core circuits from latent damages more efficiently than the STSCR with STI.

The dependence of current gains of NPN bipolar transistors in the STSCR with STI and dummy-gate structures on the collector current under the measured conditions of |VCE|=5 V and |VB|=0-2 V is shown in Fig. 5.9. The current gain of NPN in the STSCR with dummy-gate structure is higher than that of NPN in the STSCR with STI due to the shorter current path. The switching voltage of STSCR device is in inverse proportion to the current gain [62], so the STSCR with dummy-gate structure has the lower switching voltage. In addition, the substrate bias used to trigger the NPN transistor in the STSCR device has significant effect to further reduce the switching voltage and the turn-on time of STSCR with dummy-gate structure, as compared with the STSCR with STI.

5.2.3 ESD Robustness

The secondary breakdown current (It2) is the index for the HBM ESD robustness, which is indicated by the sudden increase of the leakage current under the voltage bias of 2.5 V in this work. The relation between secondary breakdown current (It2) and HBM ESD level (V_{ESD}) can be approximated as $V_{ESD} \cong It2 \times 1.5\ k\Omega$, where 1.5 kΩ is the equivalent resistance of human body. The TLP-measured I-V curves of STSCR with STI and dummy-gate structures and their measurement setup are shown in Fig. 5.10. The gate monitor device is a NMOS capacitor to verify the effectiveness of ESD protection device. The leakage currents of gate monitor device are the same before and after the TLP measurements. This implies that the thin gate oxide of NMOS can be fully protected by the STSCR with dummy-gate structure. The It2 of both STSCR devices are almost the same, but the turn-on resistance (~2.18 Ω) of STSCR with dummy-gate structure is smaller than that (~2.63 Ω) of STSCR with STI. The STSCR devices with STI and dummy-gate structures are designed with the same layout spacing to investigate the STI-blocked effect in this chapter. In fact, the layout spacing of STSCR with dummy-gate structure can be further reduced, so the current path and turn-on resistance of STSCR with dummy-gate structure can be also reduced. Under the breakdown limitation of the ultra-thin gate oxide of input stage, the STSCR with dummy-gate structure with a smaller turn-on resistance can sustain more ESD current than that of STSCR with STI with a larger turn-on resistance.

The human-body-model (HBM) [2], machine-model (MM) [3], and charged-device-model (CDM) [15] ESD tests are used to verify the ESD levels of STSCR devices with STI and dummy-gate structures. The comparison on the ESD robustness between the STSCR with STI and dummy-gate structures is shown in Table 5.1. In this ESD verification, the failure criterion is defined as the measured voltage after ESD zapping at the current level of 1 μA is shifted 30% from its original value. The HBM (MM) ESD levels of both STSCR devices with STI and dummy-gate structures are almost the same and equal to ~7 kV (~600 V). The comparison of leakage current between the STSCR with STI and dummy-gate structures before and after the 4-kV HBM ESD zapping is shown in Fig. 5.11. Although the proposed STSCR with dummy-gate structure has a larger leakage current (originating from the dummy-gate structures) than the STSCR with STI, the leakage current of STSCR with dummy-gate structure is still smaller than 3 pA at 2.5-V normal circuit operating condition even after 4-kV HBM ESD zapping. For reference, a gate-grounded NMOS (GGNMOS) device with (W/L) = 200 μm /0.5 μm has been fabricated in the same CMOS process with extra silicide-blocking mask. Such GGNMOS occupied a large active layout area of 25.8 μm×50 μm can only sustain the HBM ESD level of 3.5 kV. This has verified the excellent area efficiency of the STSCR device with dummy-gate structure (17.5 V/μm^2 for STSCR with dummy-gate structure, but only 2.71 V/μm^2 for GGNMOS).

Under the socket-mode CDM ESD test, the CDM ESD level of the STSCR with dummy-gate structure is significant higher than that of STSCR with STI structure. The dummy-gate blocking STSCR device with gate monitor device can sustain the positive (negative) CDM ESD level of 1500 (-900) V, but the STI STSCR device with gate monitor device can only sustain that of 800 (-650) V in the same 0.25-μm CMOS process. The gate monitor device is realized by the NMOS capacitor in these CDM ESD-zapping tests. The gate of the NMOS capacitor is connected to a pad, which is protected by the STSCR with STI or dummy-gate structures. The leakage currents of the gate monitor device are the same before and after the ESD zapping. From the CDM-zapping results, the STSCR with dummy-gate structure can be indeed triggered on faster to protect the ultra-thin gate oxide of input stage and to sustain higher CDM ESD robustness, as compared to the STSCR with STI. Therefore, blocking the STI region in STSCR device structure can reduce the switching voltage, enhance the turn-on speed, and increase the CDM ESD level of SCR device.

5.3 SUMMARY

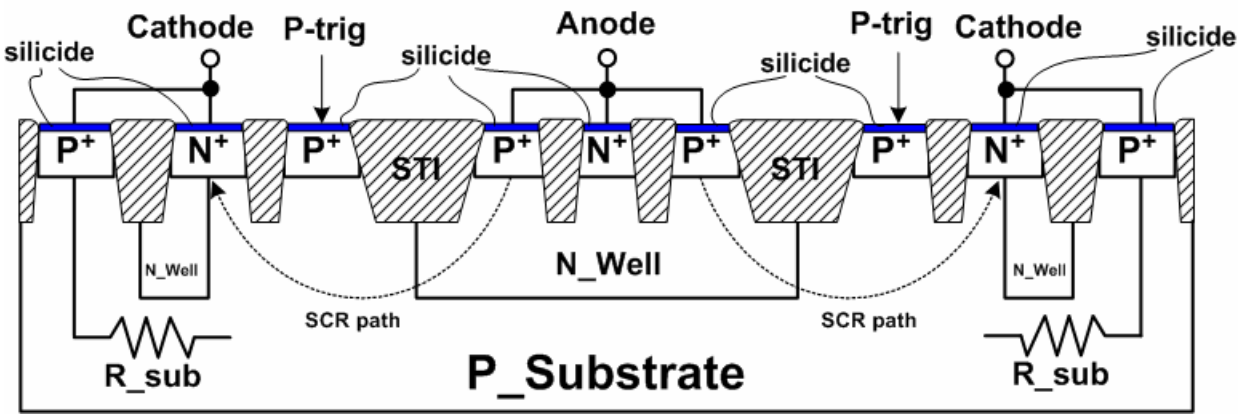
The novel dummy-gate structure to block STI region in SCR device with substrate-triggered design has been successfully investigated in a 0.25-μm salicided CMOS process. The proposed STSCR device with the dummy-gate structure is fully process-compatible to the general silicided CMOS processes without using extra silicide-blocking mask. As compared to the STSCR with STI structure, the STSCR with dummy-gate structure has the lower switching voltage, smaller turn-on resistance, lower clamping voltage, higher bipolar current gain, faster turn-on speed, and higher CDM ESD level to effectively protect the ultra-thin gate oxide against ESD stresses. The STSCR with dummy-gate structure can sustain the positive (negative) CDM ESD level of 1500 (-900) V, but the STSCR with STI can only sustain that of 800 (-650) V in the same 0.25-μm CMOS process. With a faster turn-on speed, the proposed STSCR with dummy-gate structure can effectively protect the ultra-thin gate oxide against ESD damage in the future nanoscale CMOS integrated circuits without latchup issue.

TABLE 5.1

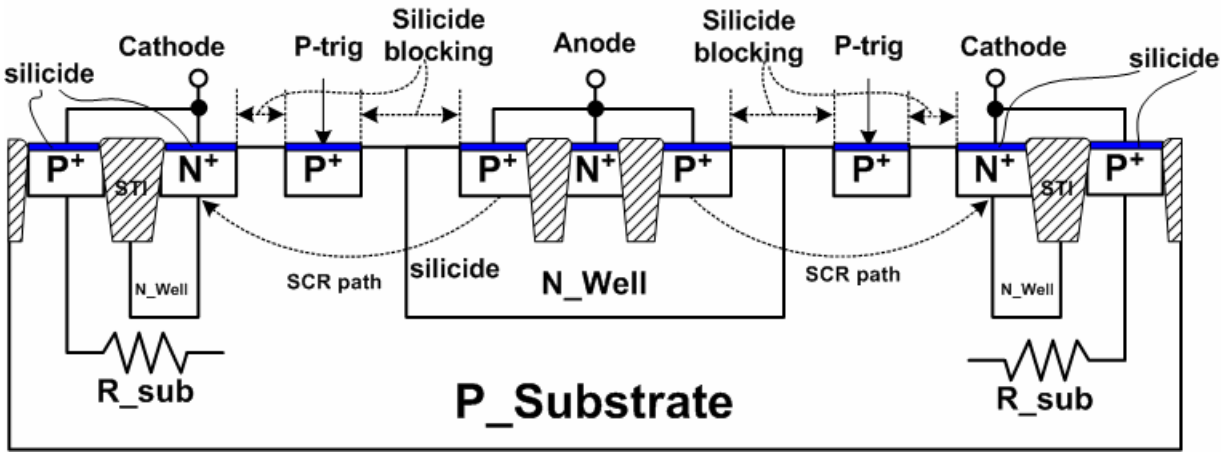
Comparison on the ESD robustness between the STSCR with STI and dummy-gate structures.

ESD stress / Device	HBM (kV)	MM (V)	CDM (+) (V)	CDM (-) (V)
STSCR with STI	~7	600	800	-650
STSCR with dummy-gate	~7	650	***1500***	***-900***

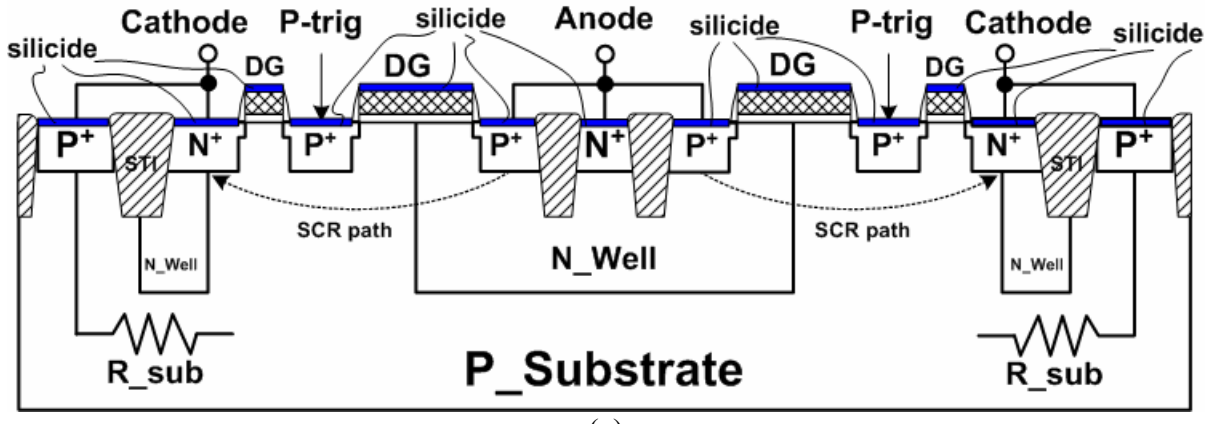
Active area: STSCR with STI or dummy-gate is drawn as 20 μm×20 μm.



(a)



(b)



(c)

Fig. 5.1 Device structures of (a) the substrate-triggered SCR (STSCR) device with shallow trench isolation (STI), (b) the STSCR device with extra silicide-blocking mask, and (c) the proposed STSCR device with dummy-gate structure.

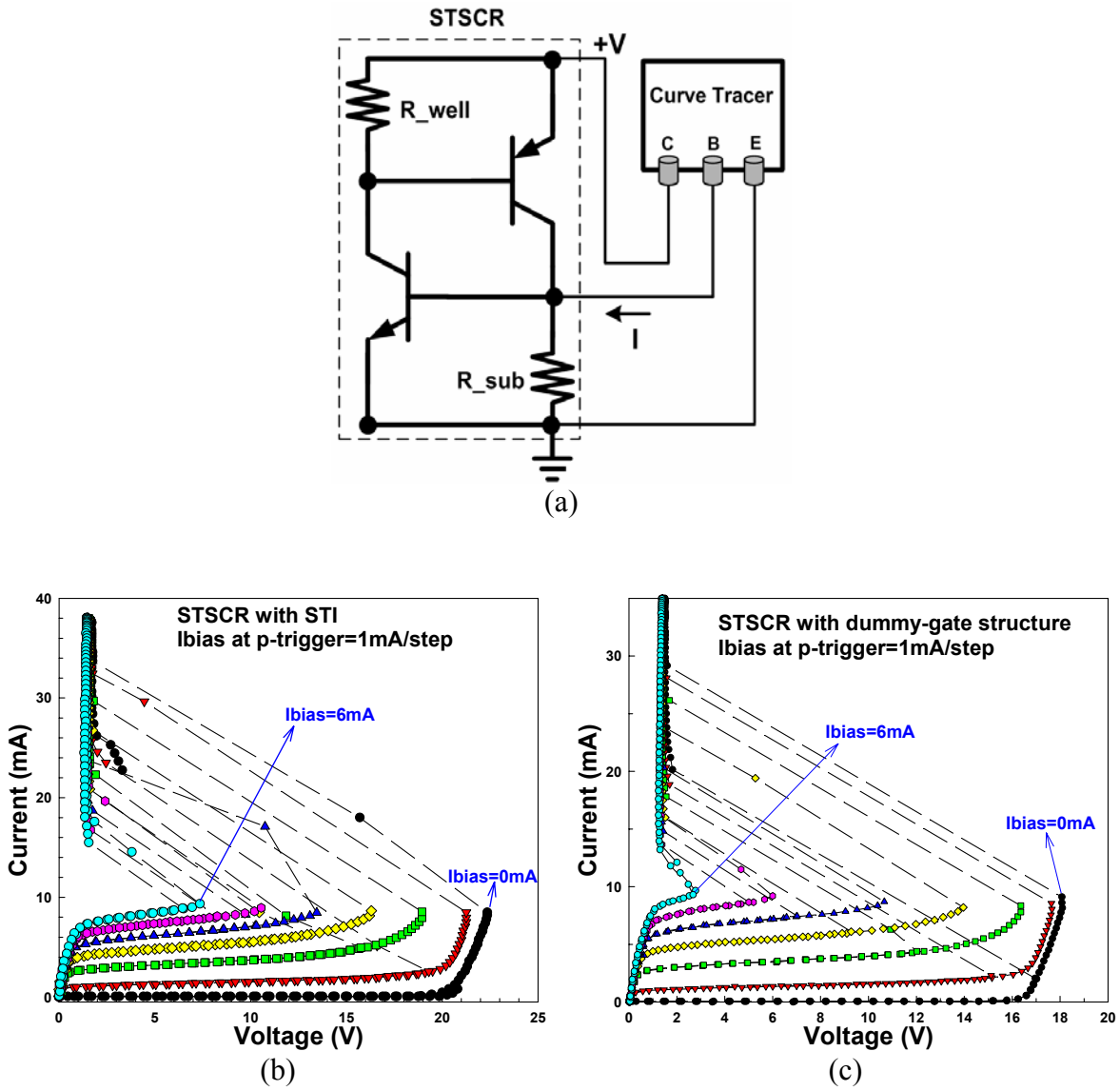


Fig. 5.2 (a) The measurement setup to find the DC I-V curves of STSCR devices. The DC I-V curves of STSCR with (b) STI, and (c) dummy-gate, structures under different substrate-triggered currents.

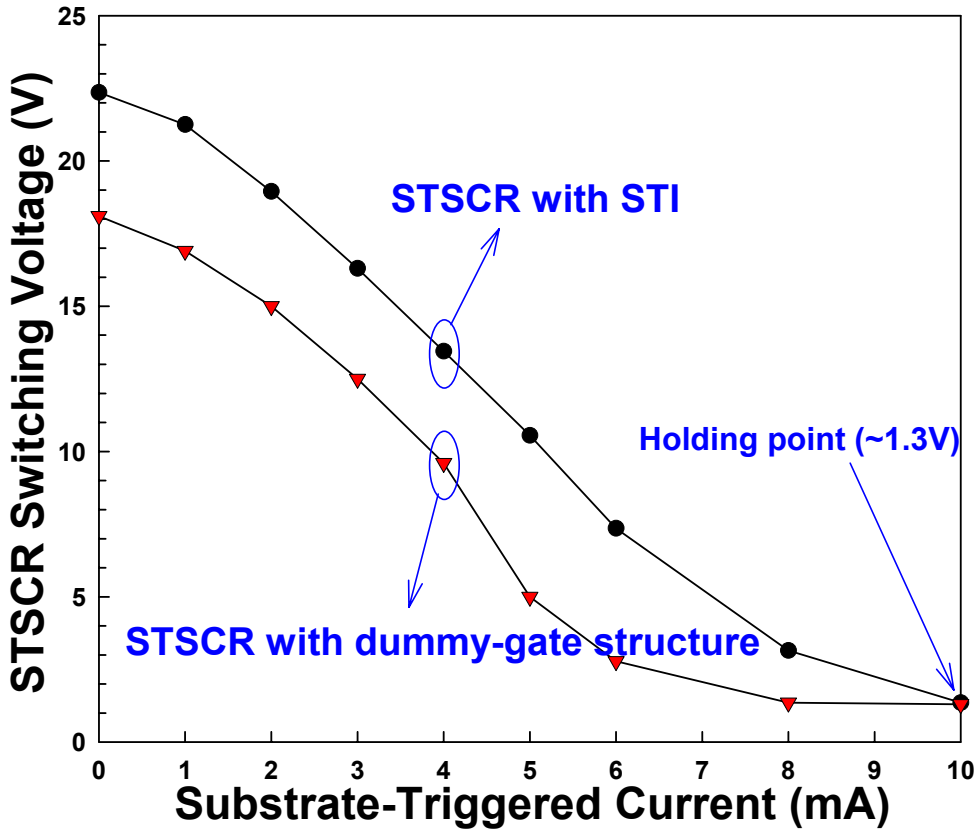


Fig. 5.3 The dependences of the switching voltages of STSCR devices with STI or dummy-gate structure on the substrate-triggered current.

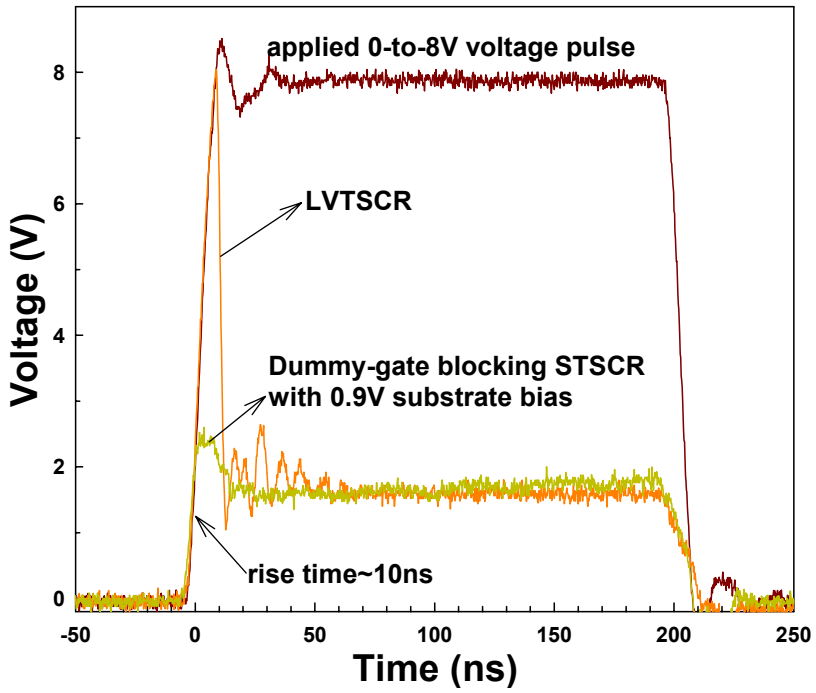


Fig. 5.4 The comparison of turn-on speed between the LVTSCR and the dummy-gate blocking STSCR with 0.9-V substrate bias under an applied 0-to-8 V voltage pulse.

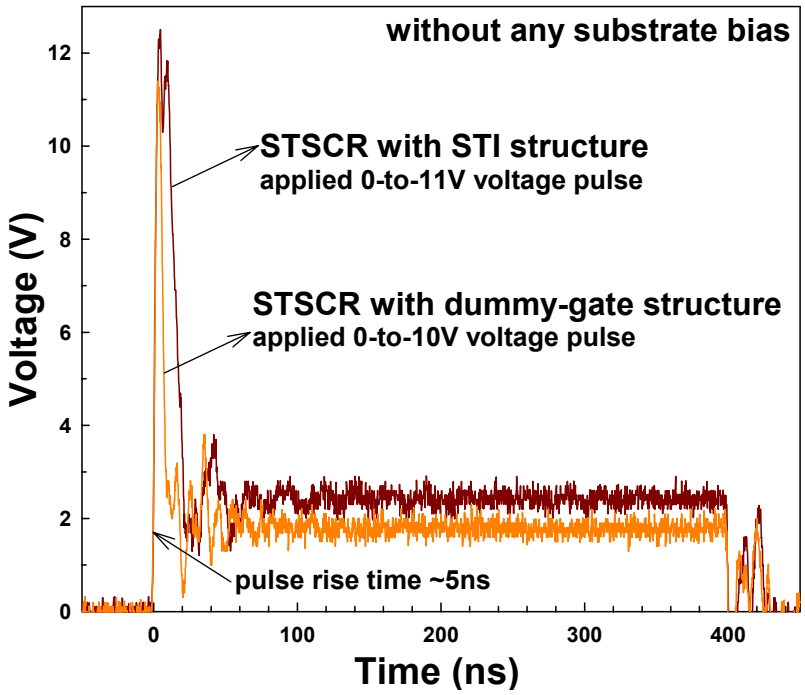


Fig. 5.5 The comparison of turn-on speed between the STSCR with STI and dummy-gate structures without any substrate bias applied at p-trigger node.

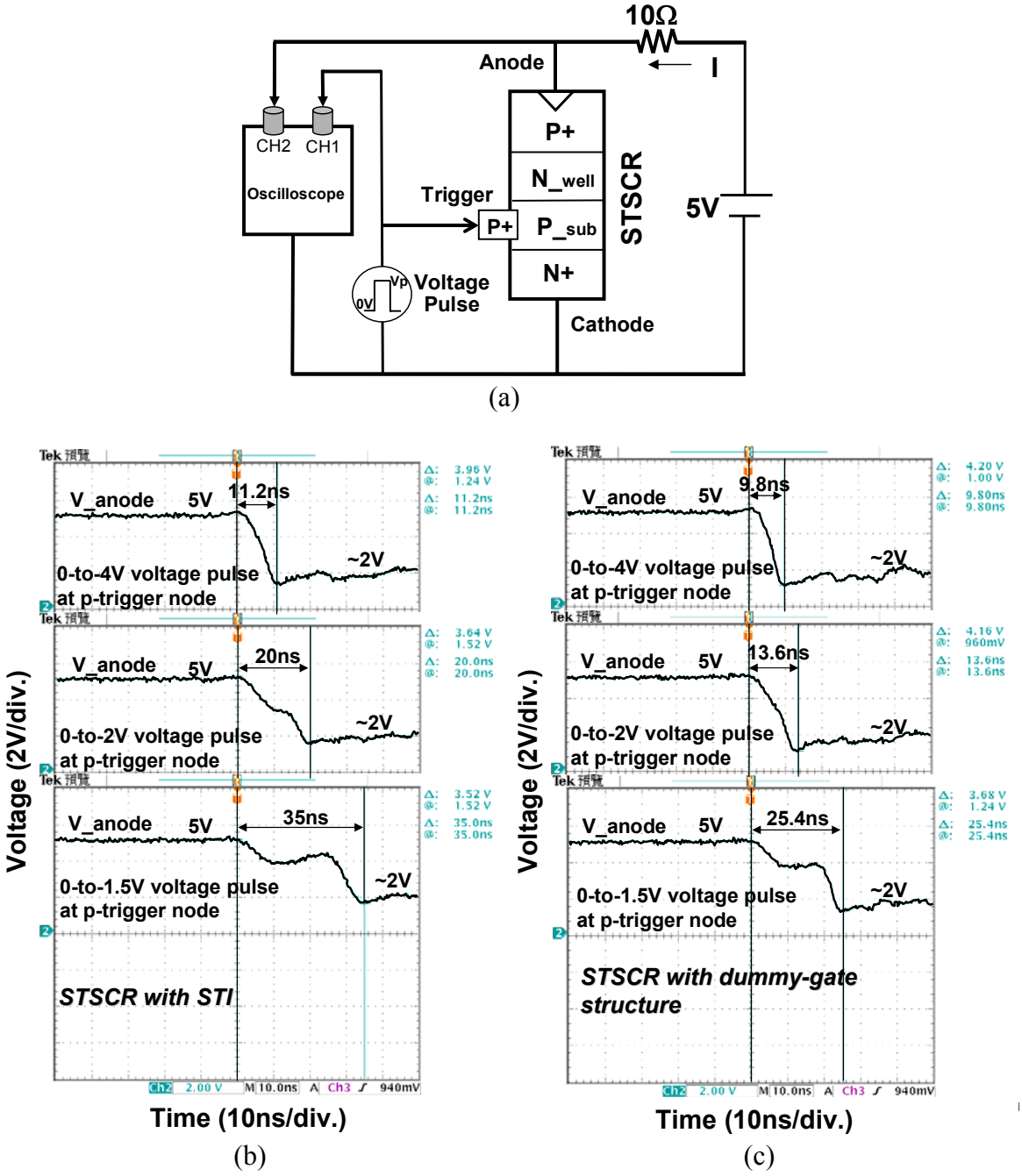


Fig. 5.6 Measurement on the turn-on time of STSCR with STI and dummy-gate structures under different voltage pulses. (a) The measurement setup. The measured voltage waveforms on the anode of the STSCR with (b) STI, and (c) dummy-gate structure, while the STSCR is triggering by the voltage pulse of 1.5V, 2V, and 4V into the trigger node.

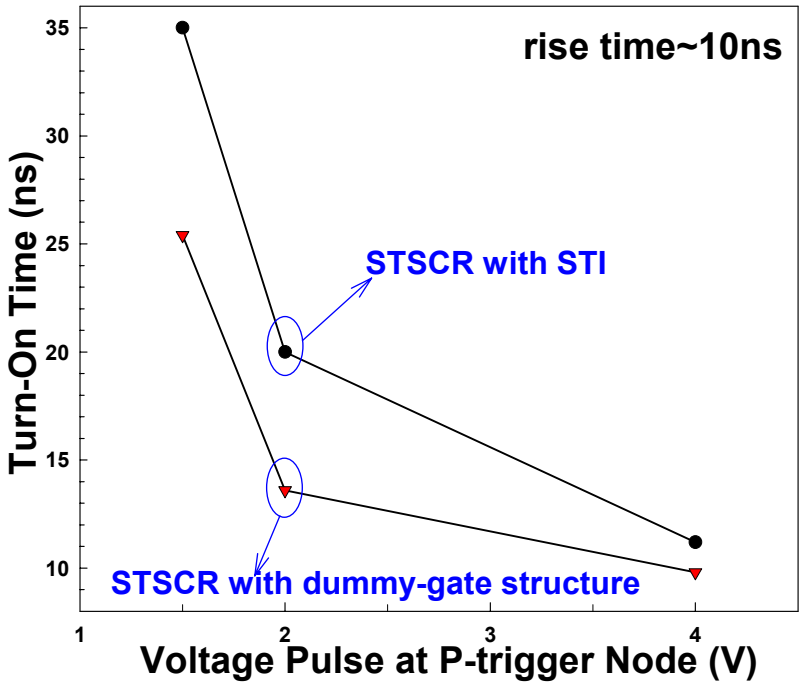


Fig. 5.7 The comparison on the turn-on time between STSCR with STI and dummy-gate structures under different voltage pulses with 10-ns rise time applied at the p-trigger node.

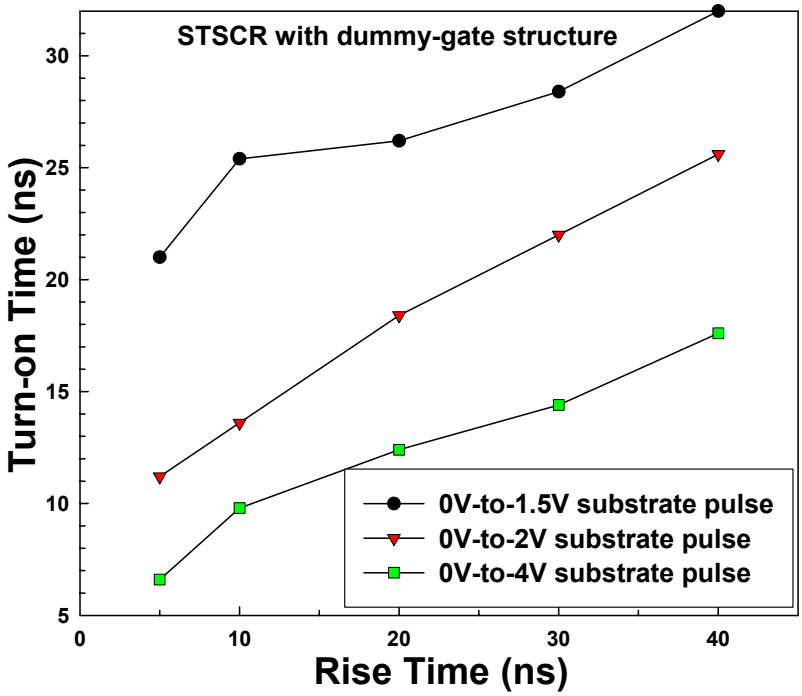


Fig. 5.8 The dependence of the turn-on time of STSCR with dummy-gate structure on the rise time of voltage pulse under different substrate bias conditions.

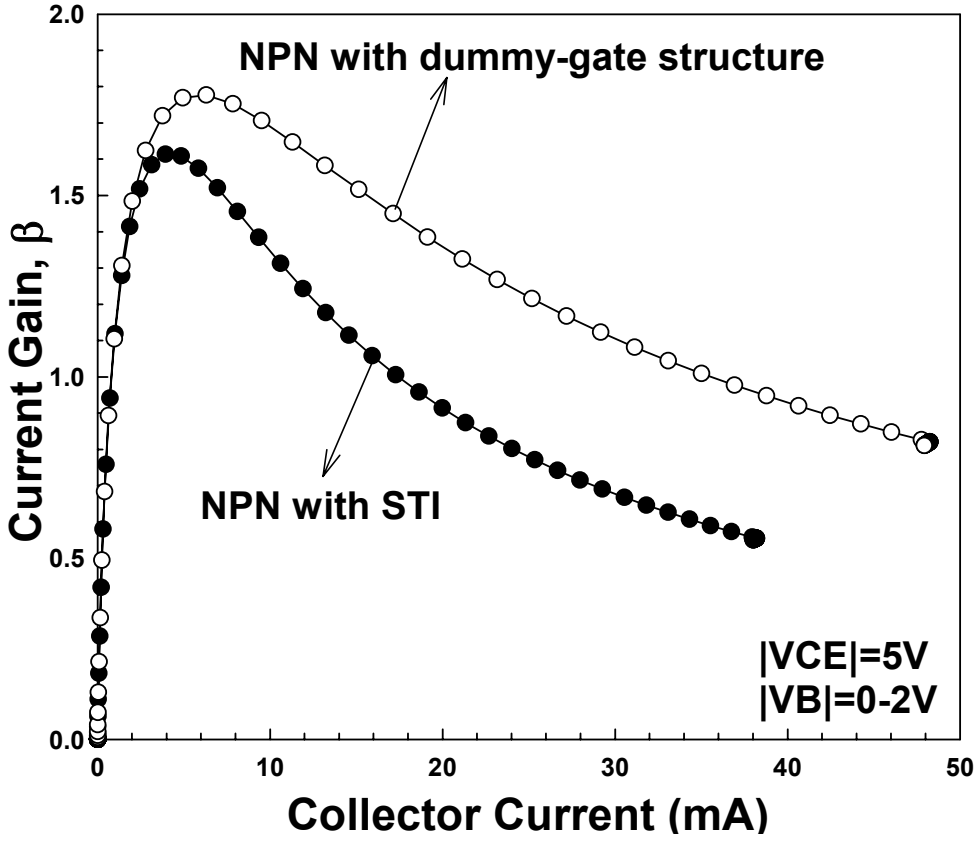


Fig. 5.9 The dependence of current gains of the NPN bipolar transistors in the STSCR devices with STI or dummy-gate structures on its collector current.

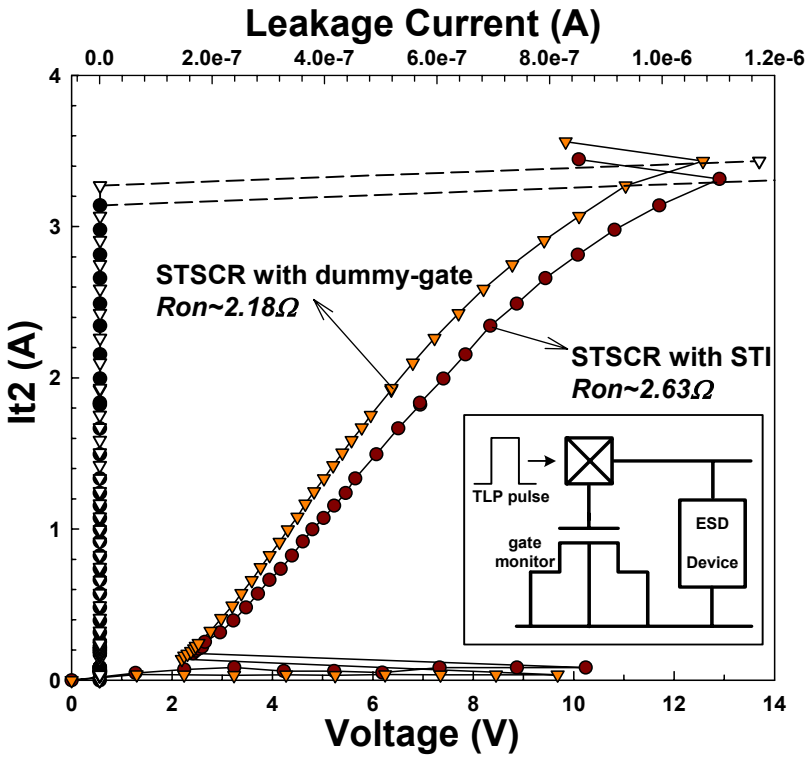


Fig. 5.10 The TLP-measured I-V curves of the STSCR with STI and dummy-gate structures.

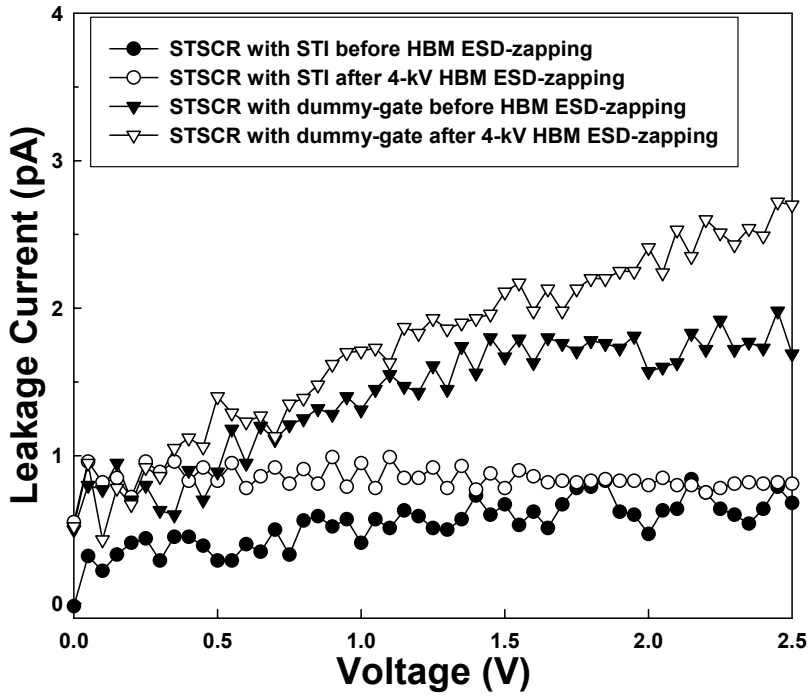


Fig. 5.11 The comparison of leakage current between the STSCR with STI and dummy-gate structures before and after 4-kV HBM ESD zapping.

CHAPTER 6

ON-CHIP ESD PROTECTION DESIGN WITH NATIVE-NMOS-TRIGGERED SCR

In this chapter, based on the substrate-triggered technique [23]-[27], a native NMOS with almost zero threshold voltage, which is an optional device in a 0.13-μm CMOS process without adding extra mask, is first used to trigger on SCR device during ESD events [28]. The novel native-NMOS-triggered SCR (NANSCR) has the lower switching voltage, smaller turn-on resistance, lower holding voltage, faster turn-on speed, and higher CDM ESD level than those of a traditional LVTSCR, therefore it is more suitable to protect the ultra-thin gate oxide. The emission microscope (EMMI) photographs are used to verify the turn-on process of NANSCR device under different ESD voltages. The NANSCR can be used in the input, output, power-rail, and whole-chip ESD protection circuits without latchup danger in CMOS IC applications with voltage supply of 1.2 V.

6.1 NATIVE-NMOS-TRIGGERED SCR (NANSCR) DEVICE

6.1.1 Device Structure

The native NMOS is directly built in a lightly-doped p-type substrate, whereas the normal NMOS (PMOS) is in a heavily-doped p-well (n-well) in a P-substrate twin-well CMOS technology, as shown in Fig. 6.1. The native NMOS is fully process-compatible with the standard CMOS process without adding extra mask. The threshold voltage of native NMOS is almost zero (~0.1 V), however, that of normal NMOS is about 0.34 V in a 0.13-μm CMOS process. The native NMOS and lateral SCR are merged together to be a novel ESD protection device, native-NMOS-triggered SCR (NANSCR), which is investigated in the chapter. The circuit schematics of NANSCR and LVTSCR are shown in Figs. 6.2(a) and 6.2(b), respectively. The drain of native NMOS in NANSCR is directly coupled to the pad of

anode, but the drain of NMOS in LVTSCR is located across the n-well/P-substrate junction of the SCR device. The gate of native NMOS is connected to a negative bias circuit (NBC) [63] to turn off the NANSCR, but the gate of NMOS in LVTSCR is connected to VSS to ensure that LVTSCR is off, under normal circuit operating conditions. The NBC is formed with clock generator, capacitors, and diodes. The output negative voltage of NBC can be tuned to fulfill various applications [63]. Under ESD event, the negative bias circuit is initially floating, so the native NMOS is an already-on device to draw some ESD current from the pad of anode to bias the SCR device. When a trigger current through the native NMOS is applied into the base (P-substrate) of NPN in Fig. 6.2(a), the base voltage of NPN will be raised up due to the substrate resistor (Rsub). As long as the base voltage of NPN is greater than 0.7 V, the NPN bipolar transistor in SCR structure is active. The collector current of NPN is generated to bias the PNP bipolar transistor. If the voltage drop across the well resistor (Rwell) is greater than 0.7 V, the PNP bipolar transistor in SCR structure is also active. When the PNP transistor is turned on, the collector current of PNP is in turn generated to further bias the NPN transistor. The positive-feedback regenerative mechanism of SCR latching process is initiated by the trigger current of the already-on native NMOS in the NANSCR structure. Finally, the NANSCR will be successfully triggered on into its latching state to discharge ESD current.

6.1.2 Characteristics of NANSCR

The new proposed NANSCR device and the traditional LVTSCR device have been fabricated in a 0.13-μm salicided CMOS process. Both of them are fully-silicided devices without extra silicide-blocking mask. In the experimental test chip, the active area (without including the guard rings) of SCR in NANSCR is drawn as 20 μm×8 μm. The active area of LVTSCR is drawn as 20 μm×7.5 μm, and the W/L of NMOS within LVTSCR is 20 μm/0.13 μm. The comparison of DC I-V curves between NANSCR and LVTSCR is shown in Fig. 6.3(a). The native NMOS in NANSCR structure has two different device dimensions of 20 μm/0.3 μm and 40 μm/0.3 μm for comparison. With the substrate-triggered technique, the switching voltage of NANSCR with native NMOS of 20-μm channel width is about ~4 V, which is smaller than that (~5 V) of LVTSCR. So, the NANSCR can be triggered on faster than the LVTSCR. Moreover, if the channel width of native NMOS in NANSCR is increased

from 20 to 40 μm, the switching voltage of NANSCR with native NMOS of 40-μm channel width can be further reduced to only ~2.5 V. The NANSCR with lower switching voltage can clamp ESD overstress voltage more quickly. The turn-on resistance and holding voltage of NANSCR are also smaller than those of LVTSCR in Fig. 6.3(a). Therefore, the voltage on the pad clamped by the NANSCR device will be lower than that clamped by the LVTSCR device under the same ESD stress. The holding voltage of NANSCR is about ~1.6 V, which is immune from latchup issue in CMOS IC applications with 1.2-V voltage supply. Such a holding voltage of NANSCR is still low enough to provide high ESD robustness, as compared with other ESD protection devices. Fig. 6.3(b) shows the leakage currents of LVTSCR and NANSCR under different gate biases. The W/L of native NMOS in NANSCR is 20 μm/0.3 μm in Fig. 6.3(b). The leakage current of NANSCR can be reduced under normal circuit operating conditions, when the gate of native NMOS is biased at -0.1 V.

6.2 ON-CHIP ESD PROTECTION DESIGN WITH NANSCR

6.2.1 ESD Protection Circuit for Input/Output Pads

The ESD protection circuit for input or output pads, which is realized with NANSCR devices, is shown in Fig. 6.4. The NANSCR devices are placed between I/O pad and VDD/VSS power lines. The n-well in NANSCR_1 is connected to VDD, but not connected to I/O pad. The gates of native NMOS in the NANSCR_1 and NANSCR_2 are connected to the same negative bias circuit (NBC). The parasitic diode Dp is the p+-to-n-well (VDD) diode in the NANSCR_1 structure. The parasitic diode Dn is the n+-to-P-substrate (VSS) diode in the NANSCR_2 structure.

Under normal circuit operating conditions, the gates of native NMOS in all NANSCR devices are biased by the same NBC to turn off the NANSCR devices. So, the NANSCR devices, NANSCR_1 and NANSCR_2, will not interfere with the functions of I/O circuits, whenever the input/output signals are logic high (VDD) or logic low (VSS). Because the holding voltage of NANSCR (~1.6 V) is greater than the maximum voltage level (1.2 V) of input/output signals, the transient-induced latchup issue in such NANSCR devices is vanished.

Under the positive-to-VSS (PS) ESD-zapping condition (with grounded VSS but floating VDD), the gate of native NMOS in the NANSCR_1 is floating. The NANSCR_1 is triggered on quickly by the substrate-triggering current generated from the native NMOS. So, the positive ESD current can be effectively discharged from the I/O pad through the NANSCR_1 to grounded VSS line. Under the negative-to-VDD (ND) ESD-zapping condition (with grounded VDD but floating VSS), the gate of native NMOS in the NANSCR_2 is floating but with an initial voltage level of 0 V. The negative ESD voltage at the I/O pad will pull down the source voltage of native NMOS through the base-emitter junction of NPN in the NANSCR_2 device. Therefore, the native NMOS in NANSCR_2 will be turned on first, resulting in the NANSCR_2 being triggered on quickly. The negative ESD current will be discharged from the I/O pad through the NANSCR_2 to grounded VDD line. For the negative-to-VSS (NS) (positive-to-VDD (PD)) ESD-zapping condition, the parasitic diode Dn (Dp) is forward biased to discharge the negative (positive) ESD current. Thus, the four modes (PS, NS, PD, and ND) of ESD stresses on the I/O pad can be clamped to a very low voltage level by the NANSCR_1, Dn, Dp, and NANSCR_2, respectively. The ultra-thin gate oxide of internal circuits can be fully protected by this design with the new proposed NANSCR devices.

6.2.2 ESD Clamp Circuit between Power Rails

The VDD-to-VSS ESD clamp circuit realized with the NANSCR device is shown in Fig. 6.5. Under normal circuit operating conditions, the NBC is active to turn off the NANSCR device. So, the NANSCR device between the power lines will neither degrade the VDD power-on transition nor interfere with the functions of internal circuit. Under ESD-stress conditions, the NBC is inactive. No negative bias is applied to the gate of native NMOS in the NANSCR. When a positive ESD pulse is applied on the VDD line with grounded VSS line, the NANSCR device will be quickly triggered on by the already-on native NMOS to discharge the positive ESD current to grounded VSS line. If a negative ESD pulse is applied on the VDD line with grounded VSS line, the parasitic diode (P-substrate/n-well junction) in the NANSCR structure will be forward biased to discharge the negative ESD current. With the power-rail ESD clamp circuit, the positive ESD current on the I/O pad in Fig. 6.4 can be partially discharged by another current path, which is from I/O pad, forward-biased diode

(Dp), through the power-rail ESD clamp circuit, to grounded VSS line under PS ESD-zapping condition. For the ND ESD-zapping condition, the negative ESD current on the I/O pad can be also partially discharged through the current path, which is from I/O pad, forward-biased diode (Dn), the power-rail ESD clamp circuit, to grounded VDD line. The ESD robustness can be greater improved and the layout area of NANSCR devices used in the I/O stages can be further reduced, while the power-rail ESD clamp circuit is added.

6.2.3 Whole-Chip ESD Protection Scheme

A new whole-chip ESD protection scheme with the proposed NANSCR devices is shown in Fig. 6.6. The anode terminals of NANSCR devices are all connected to the pads (including I/O, VDD, and VSS pads) and their cathode terminals are all connected to the ESD path. The ESD path indicated by the bold line in Fig. 6.6 can be realized with the wide and top metal line in the chip to efficiently discharge the ESD current of several amperes during ESD events. To further save layout area in the chip, such ESD path can be merged with the seal ring of the chip. The gates of native NMOS in the NANSCR devices are biased by an on-chip negative bias circuit (NBC) [63] to fully turn off all NANSCR devices under normal circuit operating conditions. During ESD-zapping condition, the NANSCR devices without negative bias in the whole-chip ESD protection scheme can be triggered on more quickly to effectively protect the internal circuits. Except the four modes of ESD stresses on the I/O pads with VDD or VSS grounded, all pin-to-pin ESD-zapping conditions (such as input-to-input, output-to-output, input-to-output, or VDD(VSS)-to-VDD(VSS)) can be fully protected by this whole-chip ESD protection scheme. For example, when an ESD pulse is zapping on an input pad (In_1) and another input pad (In_2) is relatively grounded, the ESD current will be conducted from the In_1 pad to the common ESD path through the NANSCR device. As long as the voltage level of ESD path is raised up, the parasitic diode (P-substrate/n-well junction) in another NANSCR structure connected to In_2 will be forward biased. So, the ESD current on the In_1 can be discharged from the In_1, through the NANSCR to the common ESD path, the parasitic diode in another NANSCR, to the grounded In_2. By using this new whole-chip ESD protection scheme, the pin-to-pin ESD stress can be discharged through only a NANSCR, the ESD path, and a parasitic diode between the zapping pin and the grounded pin. For ultra large-scale CMOS ICs with multiple power pins,

this new proposed whole-chip ESD protection scheme with the NANSCR devices and common ESD path is an overall solution to discharge all modes of ESD stresses quickly and efficiently.

6.3 EXPERIMENTAL RESULTS

6.3.1 Turn-On Verification

The measured voltage waveform of input signal on the pad with the NANSCR as ESD protection device under normal circuit operating condition is shown in Fig. 6.7. The voltage waveform has no any degradation, when a 1.2-V voltage signal is applied to the pad and the gate of native NMOS in NANSCR is biased at -0.1 V. So, the proposed NANSCR device does not interfere with the functions of I/O circuits or degrade the voltage level of input signals under normal circuit operating conditions. Another experimental setup to measure the turn-on speed or the emission microscope (EMMI) photograph of turn-on behavior among ESD devices under ESD-like transient conditions is shown in Fig. 6.8, where the Rs (50 Ω) is the output impedance of pulse generator. By changing the amplitude or rise time of voltage pulse, the turn-on behaviors of ESD devices under ESD events can be observed. The turn-on speeds between the gate-grounded NMOS (GGNMOS) and the gate-floated native NMOS under channel width of 360 μm but different channel lengths are compared in Fig. 6.9. Because the native NMOS is an already-on device under ESD events, the switching voltage (~2 V) of the gate-floated native NMOS is lower than that (~6 V) of the normal GGNMOS under the same device dimension, when a 0-to-6 V voltage pulse is applied. Even if the channel length of the gate-floated native NMOS is drawn as 0.3 μm, its switching voltage is still lower than that of the normal GGNMOS with channel length of 0.13 μm. So, the turn-on speed of the gate-floated native NMOS is significantly faster than that of the normal GGNMOS. Moreover, whatever the channel length of the gate-floated native NMOS is 0.13 μm or 0.3 μm, both of the gate-floated native NMOS devices have a lower clamping voltage (~2 V) than that (~3.5 V) of the normal GGNMOS with a channel length of 0.13 μm. The switching voltage and clamping voltage of the gate-floated native NMOS can be reduced with the shrinkage of channel length.

The comparisons of turn-on speeds between NANSCR and LVTSCR under 0-to-7 V voltage pulse with the pulse rise times of 10 and 5 ns are measured and shown in Figs. 6.10(a) and 6.10(b), respectively. The W/L of native NMOS in the NANSCR under this test is 20 μm/ 0.3 μm. In Fig. 6.10(a), the turn-on speed (~20 ns) of NANSCR is two-times faster than that (~40 ns) of LVTSCR. Furthermore, the turn-on speeds of NANSCR and LVTSCR can be improved with the reduction of pulse rise time. In Fig. 6.10(b), the turn-on speed (~10 ns) of NANSCR is still faster than that (~30 ns) of LVTSCR, when the rise time of 7-V voltage pulse is reduced from ~10 to ~5 ns. In addition, NANSCR can clamp the ESD-like voltage pulse to a lower voltage level than that of LVTSCR. From the experimental results, the NANSCR is more suitable than LVTSCR to quickly discharge ESD energy and to efficiently protect the ultra-thin gate oxide.

The dependence of turn-on speeds of NANSCR under different pulse rise times and pulse voltages are shown in Figs. 6.11(a)-6.11(c). When a 0-to-5 V voltage pulse is applied to the pad with NANSCR, the voltage waveform on the pad is clamped to a low voltage level, as shown in Fig. 6.11(a). The gate-floated native NMOS in NANSCR will be first turned on to clamp the ESD-like voltage pulse. Because the native NMOS is already on, it will conduct some ESD current to trigger on the SCR device and then the SCR clamps the voltage pulse to 1.6 V. Because of the output impedance of the pulse generator and the turn-on resistance of native NMOS, the clamping voltage (~4 V) of native NMOS with channel width of 20 μm in Fig. 6.11(a) is greater than that (~2 V) of native MMOS with channel width of 360 μm in Fig. 6.9. If the pulse voltage is increased to 6 V and the pulse rise time is kept at ~10 ns in Fig. 6.11(b), the NANSCR can be triggered into latching state more quickly due to the substrate-triggered technique. Moreover, the turn-on time of NANSCR is significantly reduced from ~30 to only ~10 ns, when the rise time of 6-V voltage pulse is reduced from ~10 to ~5 ns in Fig. 6.11(b). However, the turn-on speeds of NANSCR are the same in Fig. 6.11(c), when the 6-V or 8-V voltage pulses with a fixed 5-ns rise time are applied. Fig. 6.11(c) shows that the dominated factor on the turn-on speed of the proposed NANSCR is the pulse rise time, but not the overshoot transient voltage, if the high enough voltage pulse is applied. The turn-on time of NANSCR will trace the rise time of ESD event (even the CDM stress) to efficiently protect the ultra-thin gate oxide, if the high enough voltage pulse has been applied to the NANSCR device.

Fig. 6.12 verifies the turn-on waveforms of the whole-chip ESD protection scheme with

NANSCR in Fig. 6.6 under the positive-to-ESD path, negative-to-ESD path, and pin-to-pin ESD-zapping conditions. When a 0-to-8 V voltage pulse is applied to a pad and the ESD path is relatively grounded, the voltage waveform on the pad is clamped to ~2 V by the turned-on NANSCR device. Under the negative-to-ESD path ESD-zapping condition, the amplitude of clamped voltage waveform on the zapping pad is clamped to ~1 V by the forward-biased diode in the NANSCR device between the pad and ESD path. During the pin-to-pin ESD zapping, if the 0-to-8 V voltage pulse is applied to a pad_1 and a pad_2 is connected to ground, the turn-on waveform on the pad_1 can be quickly clamped to ~3 V by the turned-on NANSCR device and the forward-biased diode between the pad_1 and pad_2. The turn-on speed of NANSCR and forward-biased diode under the pin-to-pin ESD-zapping condition is almost the same as that of the stand-alone NANSCR under positive-to-ESD path ESD zapping. So, the new whole-chip ESD protection scheme in Fig. 6.6 can successfully protect the ultra-thin gate oxide of internal circuits against various ESD-zapping tests.

6.3.2 EMMI Photographs

The measured EMMI photographs on the turn-on behavior of NANSCR under different voltage pulses are shown in Figs. 6.13(a)-6.13(d). Fig. 6.13(a) shows the initial EMMI photograph of NANSCR under the voltage pulse of 0 V, where there is no hot spot in the NANSCR structure. When the pulse voltage is increased to 5 V, the hot spots are shown to locate at the native NMOS in Fig. 6.13(b), which indicates the turn-on of native NMOS. When a 5.8-V voltage pulse is applied to the pad, the hot spots are located at both of the native NMOS and the SCR device in Fig. 6.13(c), which means that SCR has been triggered on. Moreover, the intensity of hot spots on the native NMOS will become weaker in Fig. 6.13(c). If the pulse voltage is further increased to 6 V, all hot spots will be located at the SCR device and the hot spot in native NMOS will vanish in Fig. 6.13(d). The turn-on behaviors of NANSCR observed by these EMMI photographs are consistent with the results of Fig. 6.11 observed by the voltage waveforms in time domain. With the increase of pulse voltage, the ESD current path, as shown by the hot spots, is initially discharged from the native NMOS to trigger SCR into latching state, and then fully discharged through SCR device, as those shown in Figs. 6.13(b)-6.13(d).

6.3.3 TLP Measurement

By using the transmission line pulsing (TLP) measurement [56], [57], the secondary breakdown current (It2) of the ESD protection device can be found. It2 is another index for the HBM ESD robustness, which is indicated by the sudden increase of the leakage current at the voltage bias of 1.2 V in this work. The relation between secondary breakdown current (It2) and HBM ESD level (V_{ESD}) can be approximated as $V_{ESD} \cong It2 \times 1.5\ k\Omega$, where 1.5 kΩ is the equivalent resistance of human body. The TLP-measured I-V curves of the normal GGNMOS and the gate-floated native NMOS devices with silicide-blocking mask under channel width of 360 μm but different channel lengths are shown in Figs. 6.14(a) and 6.14(b), respectively. Because of involving the avalanche breakdown mechanism, significant snapback feature will exist in the normal GGNMOS in Fig. 6.14(a), but it can not be found in the gate-floated native NMOS in Fig. 6.14(b). The gate-floated native NMOS is an already-on device under ESD-zapping condition, so the required substrate current to trigger on the NPN bipolar transistor can be provided by the on current of native NMOS without involving the avalanche breakdown mechanism. So, the switching voltage of the gate-floated native NMOS in Fig. 6.14(b) is smaller than that of the normal GGNMOS (~5 V) in Fig. 6.14(a). The comparison of It2 between the normal GGNMOS and the gate-floated native NMOS under different channel lengths is summarized in Fig. 6.14(c). The It2 per channel width (micron) of the gate-floated native NMOS under different channel lengths are all greater than 7.5 mA/μm, however, those of GGNMOS under different channel lengths are all smaller than 6.5 mA/μm. The gate-floated native NMOS can sustain more ESD current than that of the normal GGNMOS under the same layout size.

The It2 of fully-silicided NANSCR and LVTSCR devices under the conditions with or without gate monitor device and the corresponding measurement setups are shown in Fig. 6.15. The gate monitor device is a NMOS capacitor to verify the effectiveness of ESD protective device. The It2 of NANSCR is almost the same as that of LVTSCR, but the turn-on resistance of NANSCR (~3 Ω) is smaller than that of LVTSCR (~5.1 Ω) under the TLP-measured conditions, which corresponds to the DC-measured result in Fig. 6.3(a). Under the breakdown limitation of ultra-thin gate oxide of input stage, the NANSCR with smaller turn-on resistance can sustain more ESD current than that of LVTSCR with larger turn-on resistance. In other words, the layout area of NANSCR can be reduced to sustain the

same ESD current as the LVTSCR with the larger layout area. The NANSCR devices have the same It2 per micron of ~80 mA/μm under the measured conditions with or without gate monitor device. The leakage currents of gate monitor device are the same before and after the TLP measurements. Therefore, the ultra-thin gate oxide of input stage can be fully protected by the new proposed NANSCR against ESD stress. Such It2 per micron of NANSCR with silicide is ten-times larger than that of normal GGNMOS without silicide shown in Fig. 6.14(c). This has verified that NANSCR has the highest ESD robustness in a smallest layout area than that of other ESD protection devices.

6.3.4 ESD Robustness

The human-body-model (HBM) [2], machine-model (MM) [3], and charged-device-model (CDM) [15] ESD tests are used to verify the ESD levels of NANSCR and LVTSCR devices. The comparison on the ESD robustness per layout area between NANSCR and LVTSCR is summarized in Table 6.1. In this ESD verification, the failure criterion is defined as the measured voltage at the current level of 1 μA is shifted 30% after ESD zapping. The HBM (MM) ESD levels per layout area of NANSCR and LVTSCR are almost the same and equal to ~16 (~1) V/μm^2. However, under the socket-mode CDM ESD testing, the CDM ESD level of the NANSCR is larger than that of LVTSCR. The NANSCR with gate monitor device can sustain the positive (negative) CDM ESD level per layout area of 5 (-3.75) V/μm^2, but the LVTSCR with gate monitor device can only sustain that of 2.33 (-2) V/μm^2 in the same 0.13-μm CMOS process. The gate monitor device is also used a NMOS capacitor in these measurements. The gate of the NMOS capacitor is connected to a pad and protected by NANSCR or LVTSCR. The leakage currents of gate monitor device are the same before and after the ESD-zapping measurements. From the CDM-zapping results, the NANSCR can be indeed triggered on faster to protect the ultra-thin gate oxide of input stage and to sustain the higher CDM ESD robustness, as compared with LVTSCR.

6.4 SUMMARY

The novel native-NMOS-trigger SCR (NANSCR) has been successfully investigated in a 0.13-μm CMOS process with 1.2-V voltage supply. The NANSCR with holding voltage of 1.6 V can be designed free to latchup issue for 1.2-V CMOS IC applications. As compared with the traditional LVTSCR, NANSCR has the lower switching voltage, smaller turn-on resistance (~3 Ω), lower clamping voltage, faster turn-on speed, and higher CDM ESD level to protect the ultra-thin gate oxide against ESD stresses. From the experimental results, the turn-on speed of NANSCR (~20 ns) has been improved two-times faster than that of traditional LVTSCR (~40 ns) under 7-V voltage pulse with 10-ns rise time. Moreover, the turn-on time of NANSCR is further reduced to only ~10 ns, when the pulse rise time is reduced from 10 to 5 ns under 6-V voltage pulse. The NANSCR can sustain the positive (negative) CDM ESD level per layout area of 5 (-3.75) V/μm^2, but the LVTSCR can only sustain that of 2.33 (-2) V/μm^2 in the same 0.13-μm CMOS process. For ultra large-scale CMOS ICs with multiple power pins, the proposed whole-chip ESD protection scheme with NANSCR and ESD path is an overall solution to quickly discharge all kinds of ESD stresses and to provide efficient protection for the internal circuits.

TABLE 6.1

Comparison on the ESD robustness between NANSCR and LVTSCR.

ESD stress / ESD device	HBM (V/μm²)	MM (V/μm²)	CDM (+) (V/μm²)	CDM (-) (V/μm²)
NANSCR	16.1	1.3	5	-3.75
LVTSCR	15.9	1.1	2.33	-2

Active area: NANSCR=20 μm×8 μm, LVTSCR=20 μm×7.5 μm.

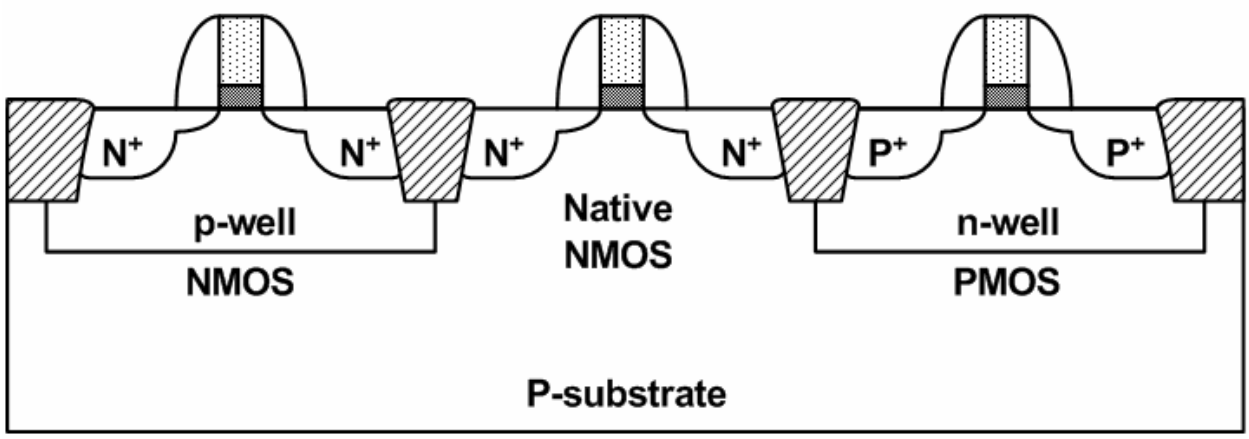


Fig. 6.1 The device cross-sectional views of the NMOS, PMOS, and native NMOS in a P-substrate twin-well CMOS technology.

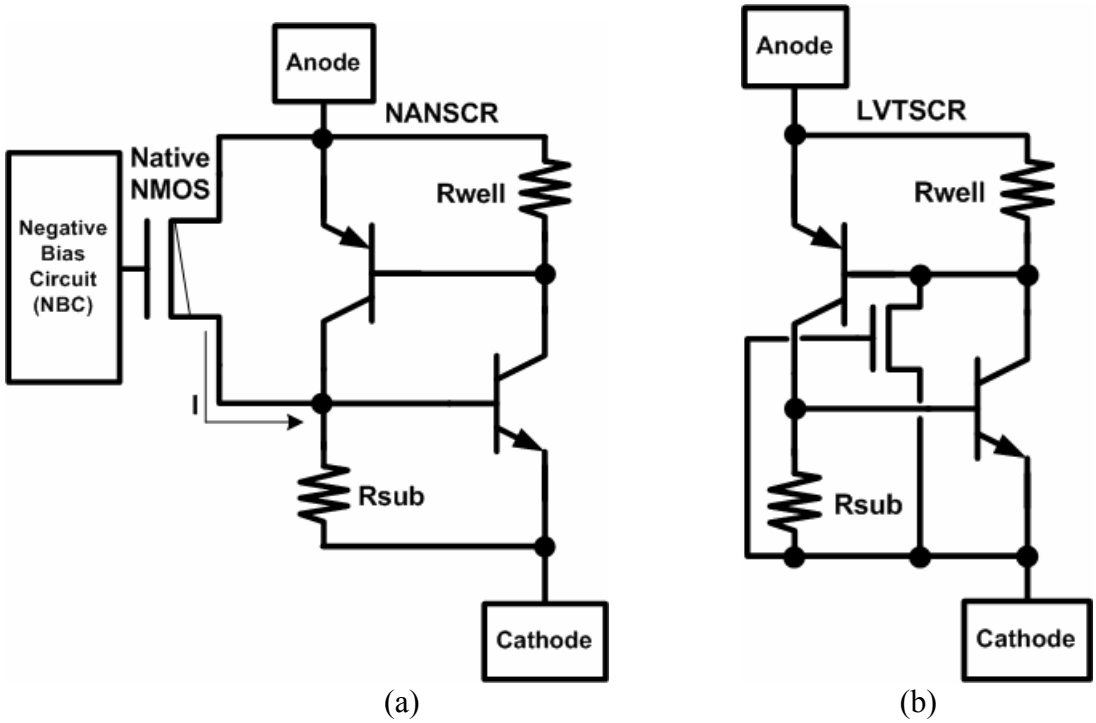
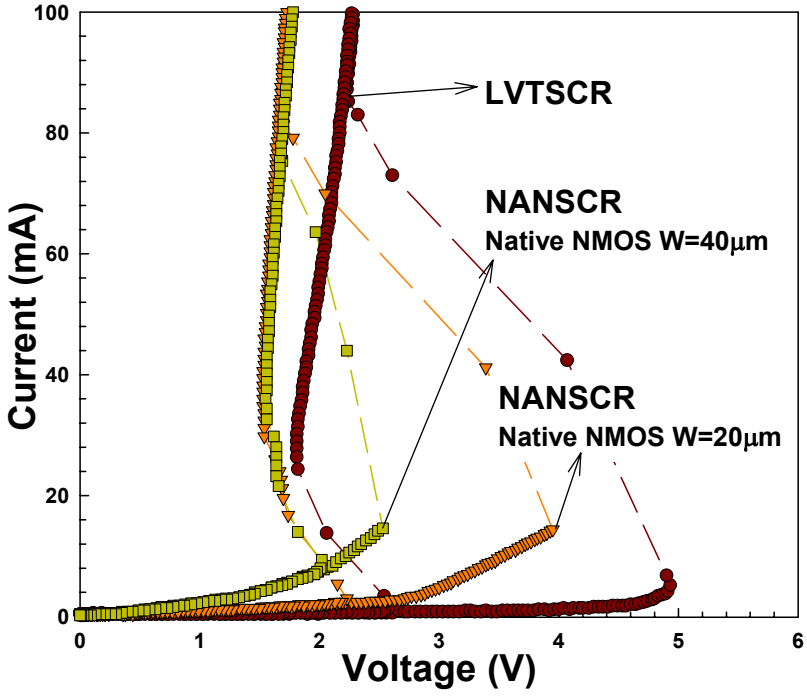
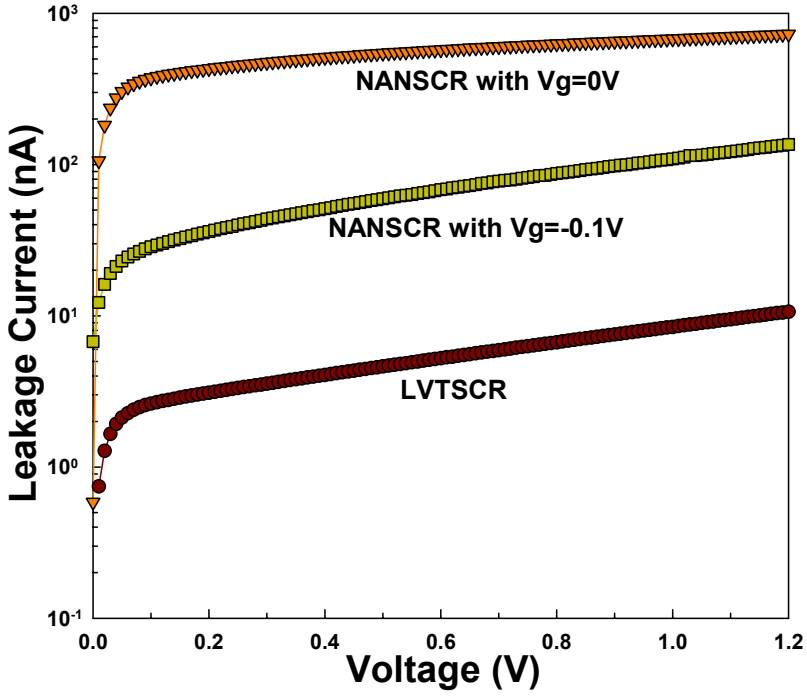


Fig. 6.2 The circuit schematics of (a) the proposed native-NMOS-triggered SCR (NANSCR) and (b) the traditional LVTSCR.



(a)



(b)

Fig. 6.3 (a) The DC I-V curves and (b) the leakage currents of the NANSCR and LVTSCR.

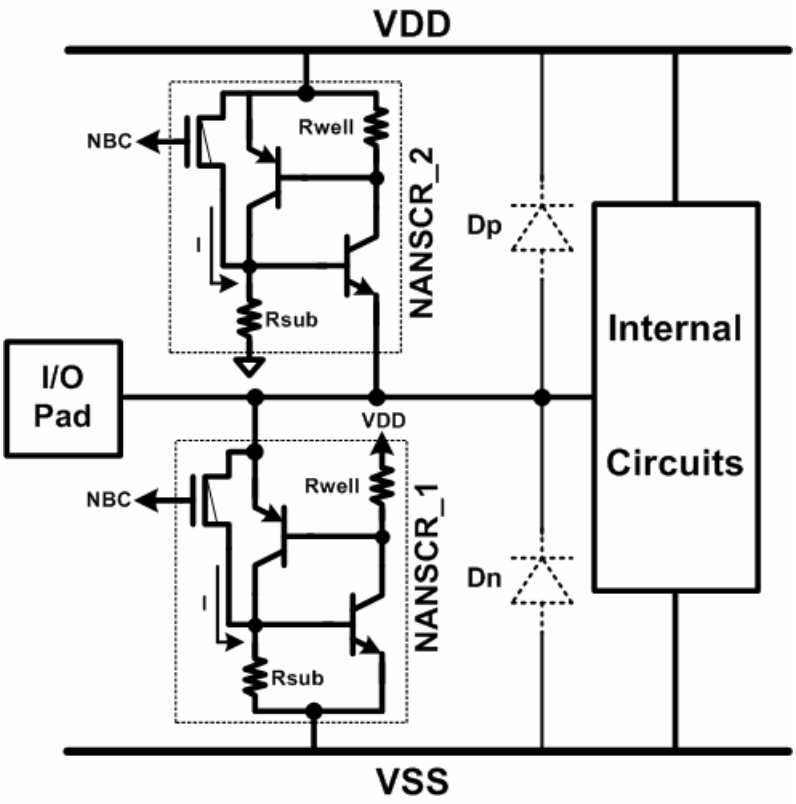


Fig. 6.4 Design of ESD protection circuit for the input or output pads with the proposed NANSCR devices.

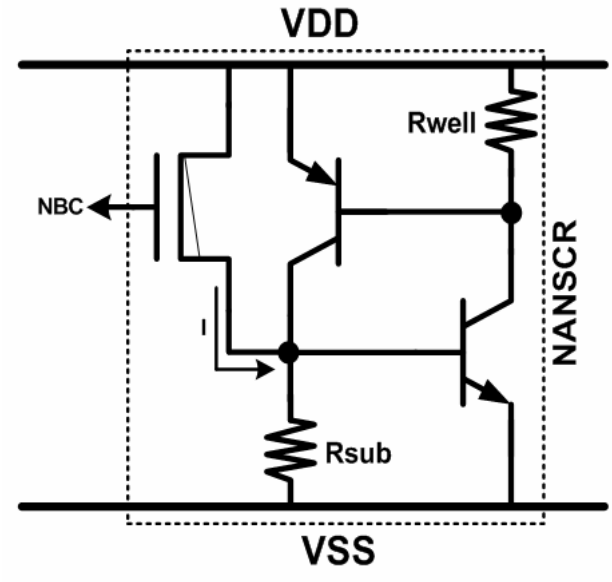


Fig. 6.5 The VDD-to-VSS ESD clamp circuit realized with the NANSCR device.

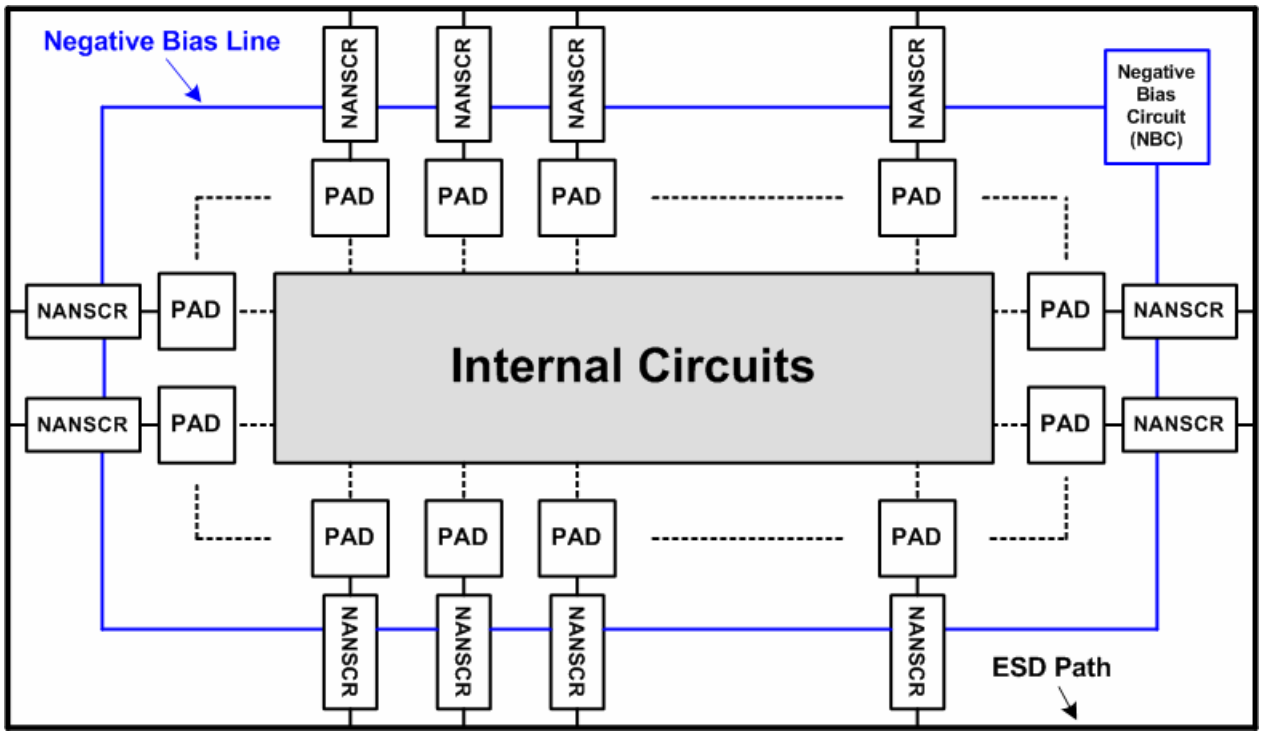


Fig. 6.6 The new whole-chip ESD protection scheme realized with the NANSCR devices.

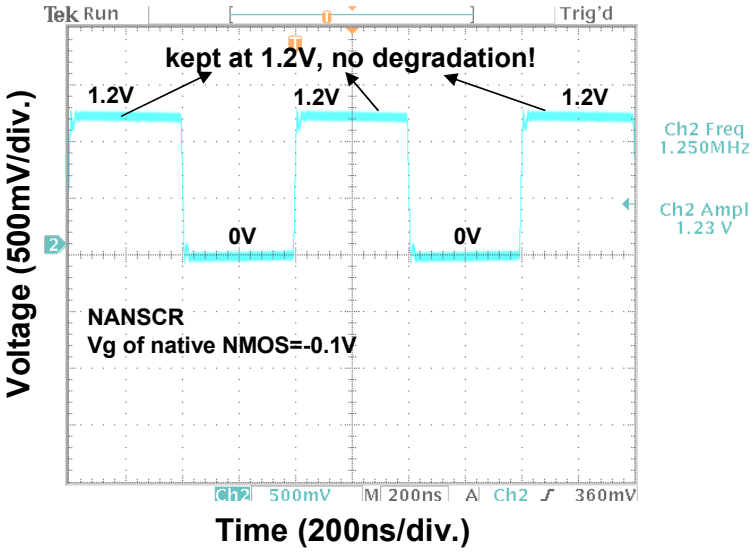


Fig. 6.7 The measured voltage waveform of input signal on the pad with the NANSCR device under normal circuit operating conditions, when a 1.2-V voltage signal is applied to the pad.

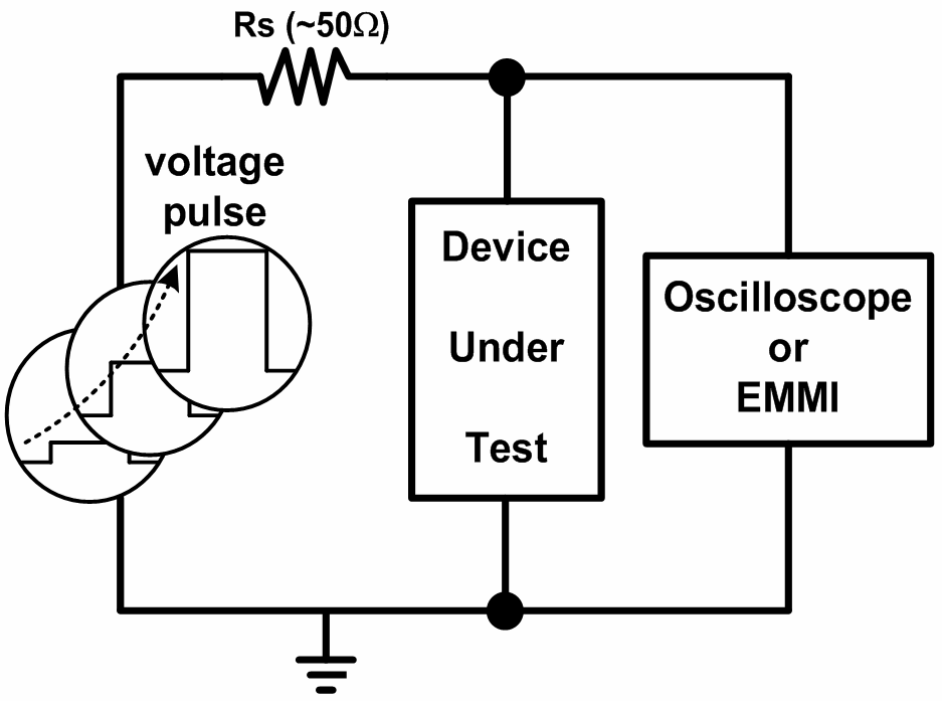


Fig. 6.8 Experimental setup to measure the turn-on speed or EMMI photograph of turn-on behavior among ESD devices.

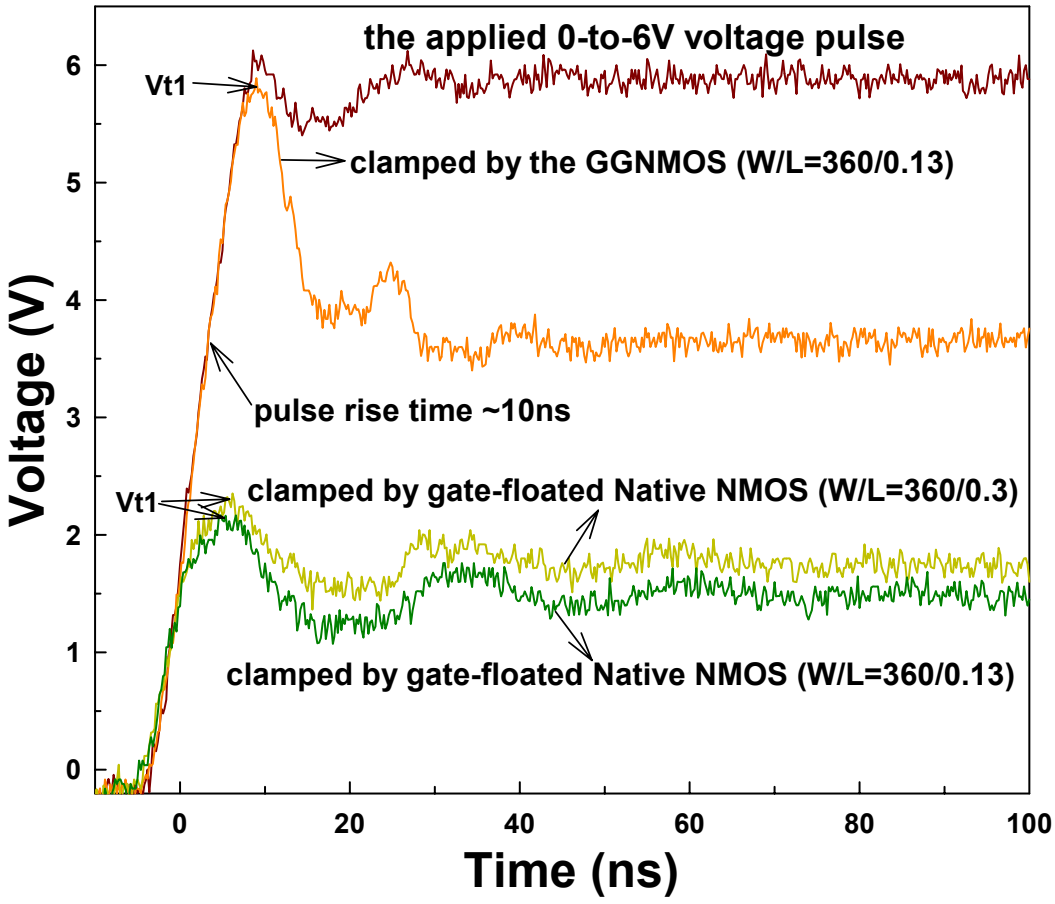
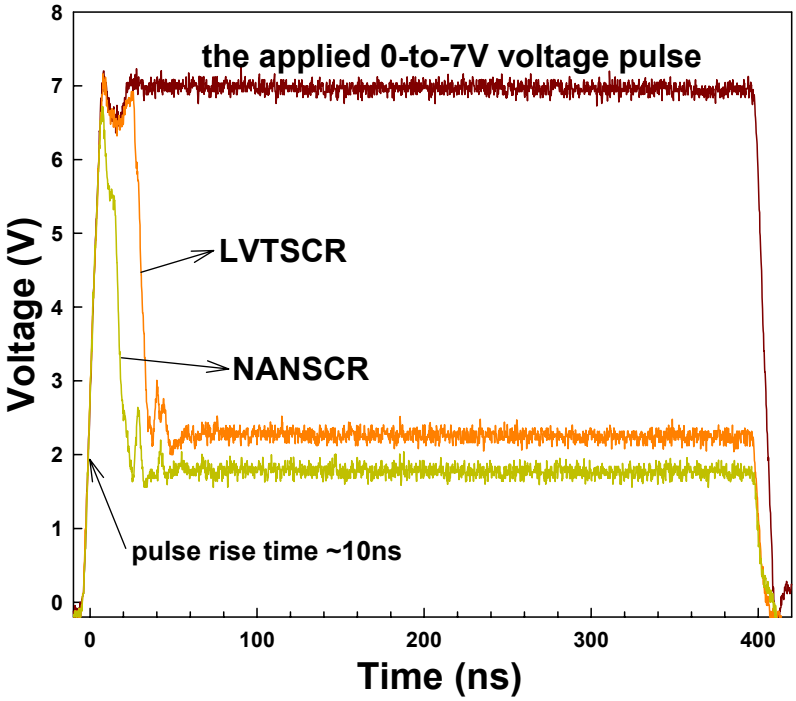
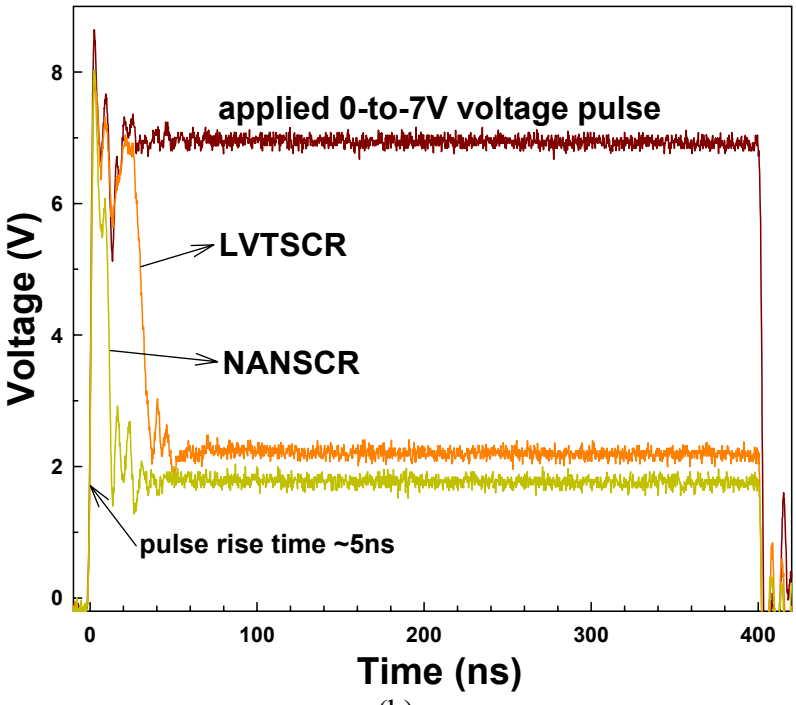


Fig. 6.9 The comparison of turn-on speeds between the GGNMOS and the gate-floated native NMOS under different channel lengths.



(a)



(b)

Fig. 6.10 The comparison of turn-on speeds between NANSCR and LVTSCR under 0-to-7 V voltage pulse with (a) 10-ns rise time and (b) 5-ns rise time.

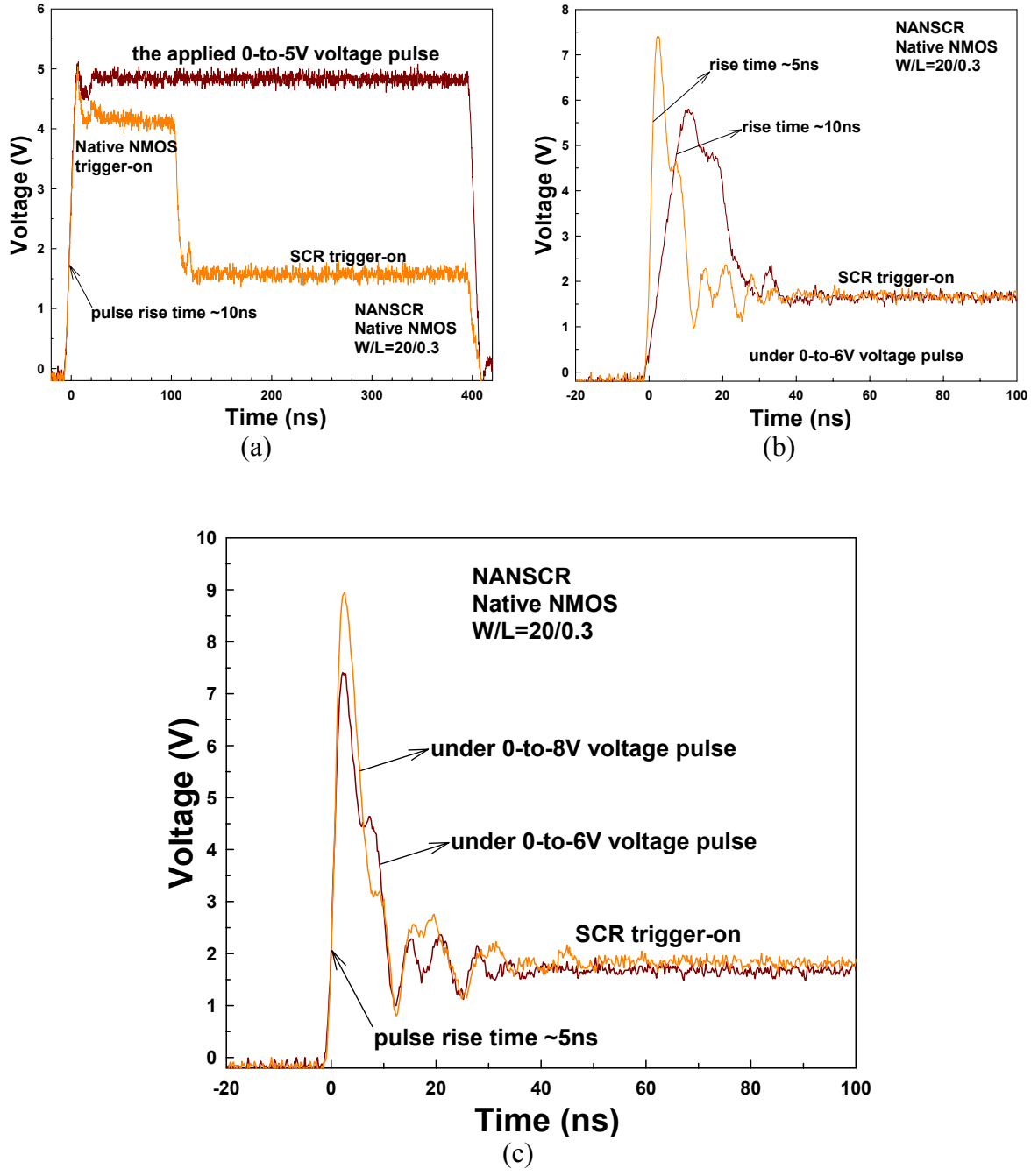


Fig. 6.11 (a) The turn-on waveform of NANSCR under 5-V voltage pulse with rise time of 10 ns. The comparison of turn-on speeds of NANSCR (b) under 6-V voltage pulse with different rise times and (c) under different pulse voltages with the same rise time of 5 ns.

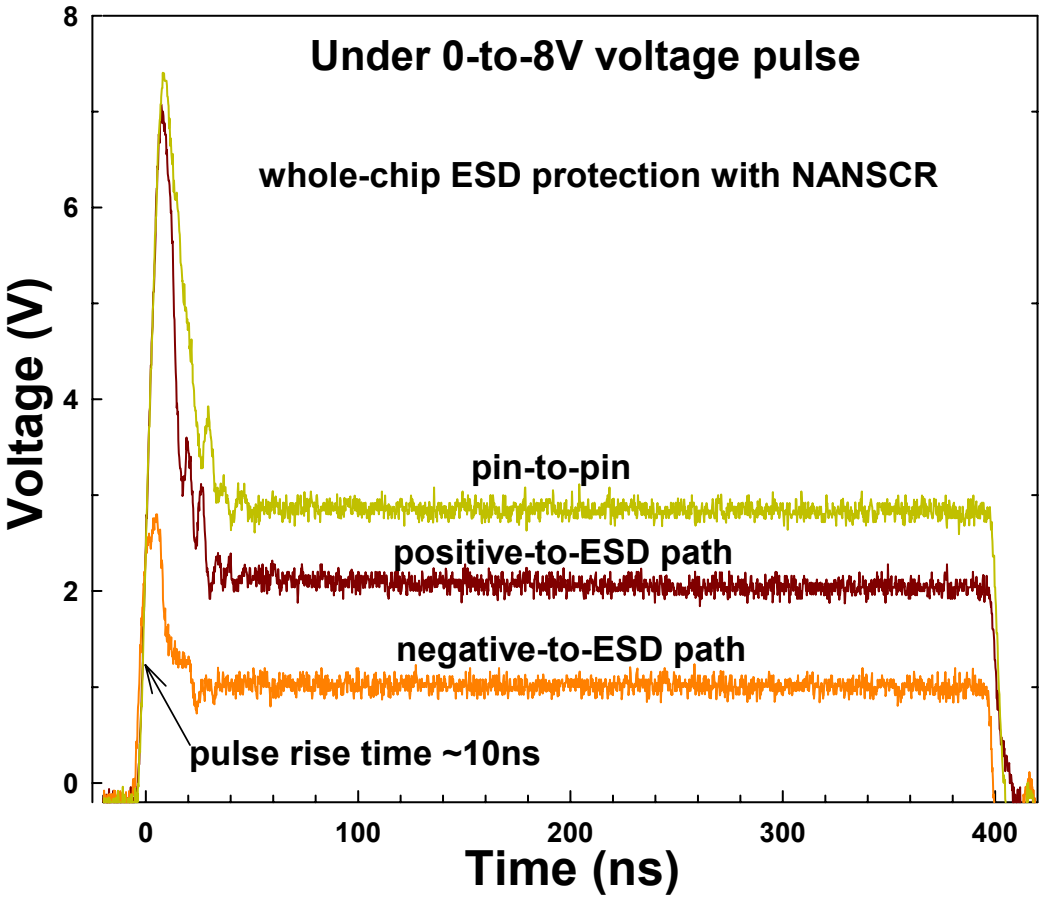


Fig. 6.12 The clamped voltage waveforms of the whole-chip ESD protection scheme with NANSCR under positive-to-ESD path, negative-to-ESD path, and pin-to-pin ESD-zapping conditions.

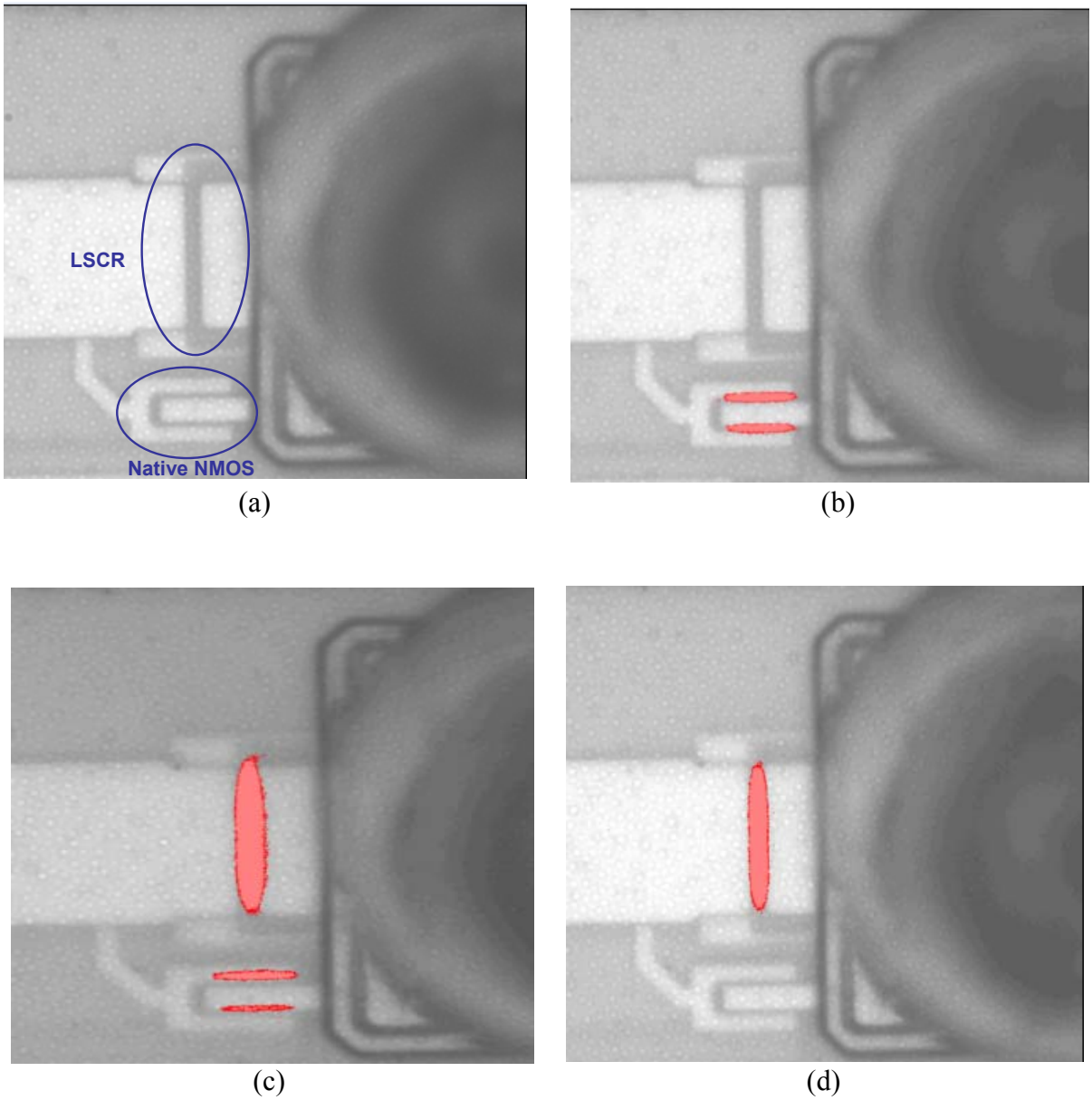


Fig. 6.13 The measured EMMI photographs on the turn-on behavior of NANSCR device under the pulsed voltage stresses of (a) 0 V, (b) 5 V, (c) 5.8 V, and (d) 6 V.

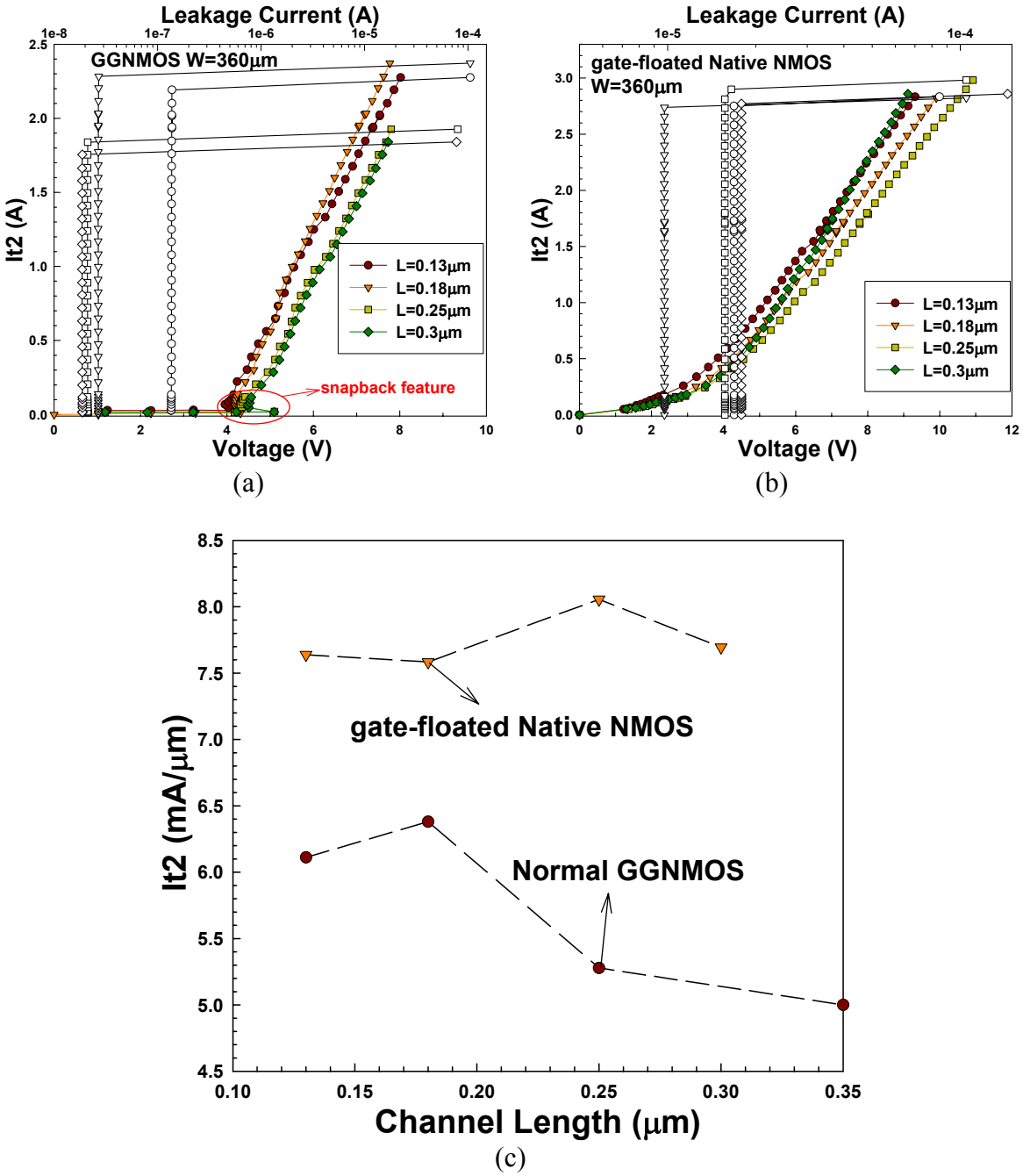


Fig. 6.14 The TLP-measured I-V curves of (a) the normal GGNMOS and (b) the gate-floated native NMOS under channel width of 360 μm and different channel lengths. (c) The comparison of It2 per micron between the normal GGNMOS and the gate-floated native NMOS under different channel lengths.

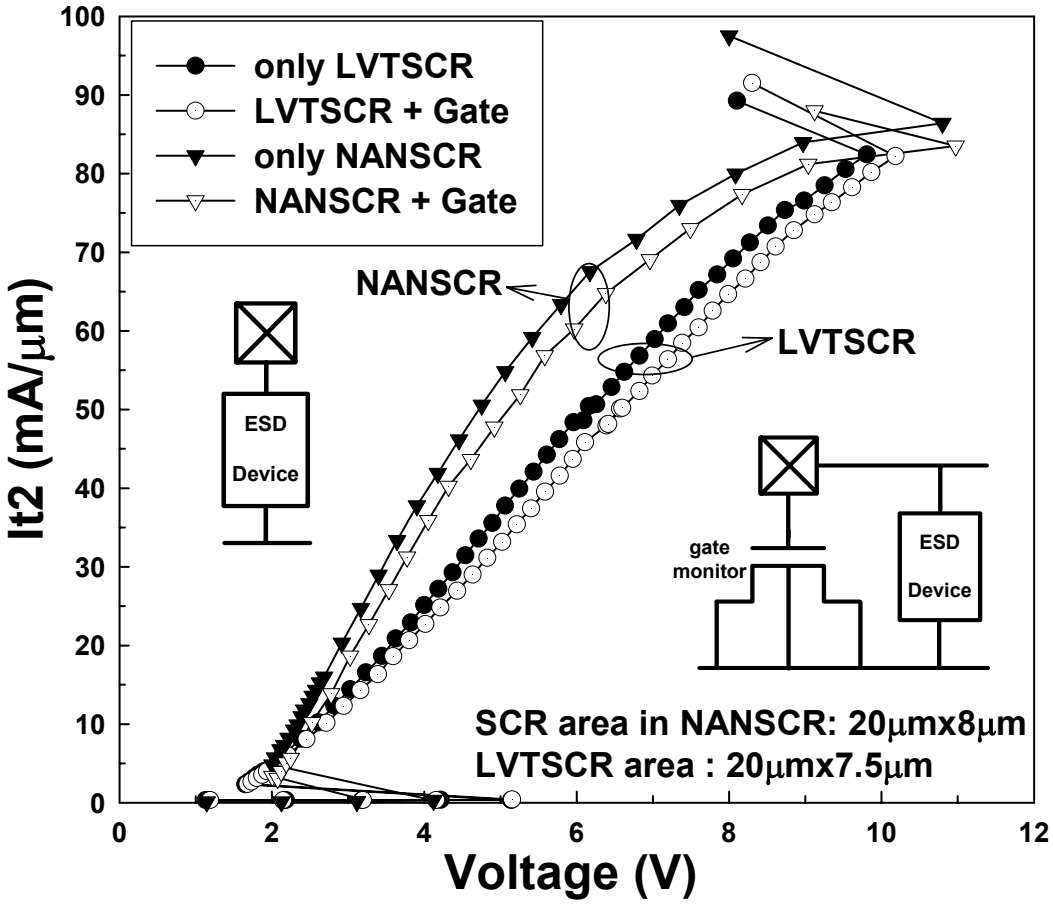


Fig. 6.15 The TLP-measured I-V curves of NANSCR and LVTSCR under the conditions with or without the gate monitor device.

CHAPTER 7

CONCLUSIONS AND FUTURE WORKS

7.1 MAIN RESULTS OF THIS THESIS

In this thesis, many kinds of low-voltage-trigger SCR devices has been proposed, p-type substrate-triggered SCR (P_STSCR), n-type substrate-triggered SCR (N_STSCR), double-triggered SCR (DTSCR), STSCR with dummy-gate structure, native-NMOS-triggered SCR (NANSCR). With the trigger technique, the positive-feedback regenerative mechanism of SCR device can be initiated without involving the avalanche breakdown mechanism. Therefore, the proposed SCR devices with trigger-assist circuits can be successfully used in the input, output, and power-rail ESD protection circuits to effectively protect the ultra-thin gate oxide of input stages. By using the substrate-triggered technique, the STSCR device has the advantages of controllable switching voltage (~1.85 V@8 mA or ~1.55 V@1.06 V) and high ESD robustness (~16 V/μm^2) in a smaller layout area. The turn-on time of STSCR can be reduced from 27.4 ns to 7.8 ns by the substrate-triggering technique. For the latchup-free IC applications with VDD of 2.5V, the ESD protection circuit designed with two STSCR devices in stacked configuration and ESD-detection circuit can sustain the HBM (MM) ESD level per area of >10V/μm^2 (0.88 V/μm^2). And, the ESD protection circuits designed with complementary-STSCR devices and two stacked diodes can sustain the HBM (MM) ESD level per area of ~8.8 V/μm^2 (0.61 V/μm^2) in a 0.25-μm fully salicided CMOS process without using extra process modification.

By applying the both substrate and N-well triggered currents to synchronously trigger the NPN and PNP bipolar transistors in SCR structure, the switching voltage and turn-on time of DTSCR device can be successfully reduced. The switching voltage of DTSCR under the N-well triggered current of -3 mA is further reduced from ~21 to ~1.5 V, when the substrate-triggered current is increased from 0 to 2 mA. Under the positive voltage pulse of 1.5 V at p-trigger node, the turn-on time of DTSCR can be reduced from 37.6 to 11.8 ns, while the absolute pulse height of negative voltage pulse applied to the n-trigger node is

increased from 0 to 5 V. With the double-triggered technique, the required pulse width to trigger the DTSCR into latching state can be shortened, so the layout areas of the ESD-detection circuits, used to synchronously generate the substrate and N-well triggered currents, can be design smaller to save the fabrication cost.

The proposed STSCR device with the dummy-gate structure is fully process-compatible to the general silicided CMOS processes without using extra silicide-blocking mask. As compared to the STSCR with STI structure, the STSCR with dummy-gate structure has the lower switching voltage, smaller turn-on resistance, lower clamping voltage, higher bipolar current gain, faster turn-on speed, and higher CDM ESD level to effectively protect the ultra-thin gate oxide against ESD stresses. The STSCR with dummy-gate structure can sustain the positive (negative) CDM ESD level of 1500 (-900) V, but the STSCR with STI can only sustain that of 800 (-650) V in the same 0.25-μm CMOS process. With a faster turn-on speed, the proposed STSCR with dummy-gate structure can effectively protect the ultra-thin gate oxide against ESD damage in the future nanoscale CMOS integrated circuits without latchup issue.

NANSCR has the lower switching voltage, smaller turn-on resistance (~3 Ω), lower clamping voltage, faster turn-on speed, and higher CDM ESD level to protect the ultra-thin gate oxide against ESD stresses, as compared with the traditional LVTSCR. From the experimental results, the turn-on speed of NANSCR (~20 ns) has been improved two-times faster than that of traditional LVTSCR (~40 ns) under 7-V voltage pulse with 10-ns rise time. Moreover, the turn-on time of NANSCR is further reduced to only ~10 ns, when the pulse rise time is reduced from 10 to 5 ns under 6-V voltage pulse. The NANSCR can sustain the positive (negative) CDM ESD level per layout area of 5 (-3.75) V/μm^2, but the LVTSCR can only sustain that of 2.33 (-2) V/μm^2 in the same 0.13-μm CMOS process. For ultra large-scale CMOS ICs with multiple power pins, the proposed whole-chip ESD protection scheme with NANSCR and ESD path is an overall solution to quickly discharge all kinds of ESD stresses and to provide efficient protection for the internal circuits.

The comparison among the proposed SCR-based devices in this thesis and the prior SCR-based devices in some papers for on-chip ESD protection has been summarized in Table 1.1. The HBM and MM ESD levels of SCR-based devices are always superior to other non-SCR ESD protection devices. The switching voltage and the turn-on speed of SCR-based

devices must be finely designed to fully and effectively protect the ultra-thin gate oxide of input stages, especially against the fast CDM ESD events. The switching voltage and turn-on speed of SCR-based devices will be the dominated factors on the overall performances of on-chip ESD protection circuits with SCR-based devices in nanoscale CMOS process with the maximum voltage supply smaller than 1.2 V. The NANSCR and the dummy-gate blocking SCR device with trigger-assist circuits will be a better choice to protect such an ultra-thinner gate oxide in nanoscale CMOS processes.

7.2 FUTURE WORKS

In the future nanoscale CMOS process with VDD below 1.2 V, the latchup concern inherent in SCR device will be eliminated, because the holding voltage of SCR device is greater than the maximum voltage level of VDD. The low-voltage-trigger SCR device with highest ESD robustness in a smaller layout area will be a suitable ESD protection solution. The fabrication cost of SCR-based device is usually lower than other ESD protection devices due to its best area efficiency. The device characteristics, turn-on waveforms, TLP measurements, and ESD robustness of the ESD protection circuits with the proposed low-voltage-trigger SCR-based devices have been clearly analyzed and discussed in this thesis. But, there are no simulation results for the current, temperature, and electric field distributions of the proposed SCR-based devices in this thesis because of the lack of efficient simulation tools and device process parameters. Those simulation results can help the evidence of the proposed turn-on mechanisms. Thus, the future work to simulate ESD robustness of the protection devices will focus on those physical simulation results, which are based on the proposed turn-on mechanisms in this thesis.

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論 文 名 稱：**具有基體觸發技術之矽控整流器及其在積體電路晶片靜電放電防護上之應用**

Silicon-Controlled Rectifier With Substrate-Triggered Technique for On-Chip ESD Protection in CMOS Integrated Circuits

PUBLICATIONS LIST

(A) Referred Journal Papers:

[1] Ming-Dou Ker and **Kuo-Chun Hsu**, "Substrate-triggered SCR device for on-chip ESD protection in fully silicided sub-0.25-um CMOS process," *IEEE Trans. Electron Devices*, vol. 50, pp. 397-405, Feb. 2003.

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(B) Local Journal Papers:

[1] **Kuo-Chun Hsu** and Ming-Dou Ker, "基體觸發之互補式矽控整流器及其在靜電放電防護電路上的應用," 電子月刊, 第92期, pp. 148-161, 2003.

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(E) Patents

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