國立交通大學

電機資訊學院　　電子與光電學程

碩 士 論 文

矽化金屬互補式金氧半導體製程之新型靜電放電防護元件

New ESD Protection Devices with Dummy-Gate Structure in a Fully-Salicided CMOS Technology

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中 華 民 國 九十三 年 六 月

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國 立 交 通 大 學

電機資訊學院　電子與光電學程

碩 士 論 文

A Thesis

Submitted to Degree Program of Electrical Engineering and Computer Science

College of Electrical Engineering and Computer Science

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Electronics and Electro-Optical Engineering

June 2004

Hsinchu, Taiwan, Republic of China

中華民國九十三年六月

授權書

(博碩士論文)

本授權書所授權之論文為本人在交通大學(學院)電機資訊學院電子與光電學程系所

九十二學年度第二學期取得碩士學位之論文。

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矽化金屬互補式半導體製程之
新型靜電放電防護元件

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摘要

矽化金屬沉積(salicidation)是高速互補式金氧半導體的重要製程技術，然而當此項技術應用在 N 型金氧半導體靜電放電保護元件上便有幾項問題存在，其中最重要的問題是 N 型金氧半導體元件的靜電放電保護準位過低。因為矽化金屬沉積降低汲極端的平穩電阻，使得電流集中在表面，因此產生多手指機制均勻啟動失效的問題以致於降低半導體靜電放電保護元件的 ESD 準位。所以如何在汲極與閘極之間形成一個適當平穩的電阻便是一個重要的課題。一般有幾種解決方式如汲極端的阻絕(salicide blocking of drain side)，使用額外的 N-well 平穩電阻(external N-well ballast resistors)，靜電放電防護元件植佈方法(ESD implantation methods)。然而汲極端的阻絕因為使用較多道製程，成本較高，而且存在因為蝕刻阻絕材料造成的漏電流的問題。而靜電放電保護元件植佈方法則有成本高及例如熱載子的可靠性問題，本篇論文中利用 N-well 電阻加在 N 型金氧半導體元件的汲極端，同時在 N-Well 電阻上方形成 Field Oxide (FOX)，假性閘極(dummy-gate)。如此分別在 FOX, 假性閘極下方的 N-Well 電阻解決了 ESD 準位過低的問題，這些 N 型金氧半導體元件不需要額外的製程便可以被製造出來。

為了與新型元件做比較，傳統的矽化金屬沉積 N 型金氧半導體元件，以及使用矽化金屬阻絕(salicide blocking)的元件將一併被製造，而這四種靜電放電防護 N 型金氧半導體元件將被提出來討論比較。

New ESD Protection Devices with Dummy-Gate Structure in a Fully-Salicided CMOS Technology

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ABSTRACT

Salicidation is one of the key processes for high performance quarter-micron CMOS devices. However, several problems occur when salicide technology is implemented in ESD protection NMOS transistors. The most difficult problem is the low ESD robustness of output NMOS transistors. A salicided drain may reduce the desired ballast resistance at the drain junction, which results in current localization and failure of multi-finger uniform turn-on, thus the ESD characteristics will be degraded very much. It's very important to make a ballast resistance between drain contact and gate edge for ESD robustness.

There are several solutions such as salicide blocking of the drain area, using external N-well ballast resistors, and ESD implantation method to improve ESD robustness. However, salicide blocking method is expensive because it needs several extra process steps, and has the problem that larger leakage current can be caused by the etching of blocking materials. ESD implantation method can improve ESD

robustness but it results in extra cost and other hot carriers reliability issue. In this thesis, we proposed two novel ESD protection NMOS transistors, FOX structure transistor with external N-well resistors, and dummy-gate structure transistor with external N-well resistors to form ballast resistors between drain contact and gate edge. To compare with the novel ESD protection NMOS transistors, transistors with fully-salicided and salicide blocking structures are also fabricated. Those four ESD protection NMOS transistors are compared and discussed in this thesis.

誌謝

首先我要對我的指導教授 柯明道教授獻上最誠摯的謝意，感謝老師在電路上的許多建議與指導，並教導我許多報告與書寫論文的技巧。 柯明道教授也為我爭取到許多下晶片的機會，使我們能將設計的元件做實際上的驗證。感謝林坤賢學長、張智毅學長、徐國鈞學長、楊明達學長、徐新智學長、鄧至剛學長以及張瑋仁、陳榮昇、許勝福，在我遭遇到問題的時候，耐心的幫我找出問題的所在。我也要感謝他們，在我遇到瓶頸的時候，能夠適時的給予協助。還有我的同學，在我們日常生活的討論中，讓我學習到許多東西。同時我也要感謝實驗室的所有人，有了大家的幫忙，我才有辦法開心及順利的完成碩士課程。

最後我也要由衷的感謝我的父親、母親，因為你們從小的栽培，我才能夠順順利利的達成現在的成就；還有太太，謝謝你的支持。

陳 啟 銘

西元 2004 年 6 月

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CHAPTER 1

INTRODUCTION

1.1 Background

Electrostatic discharge (ESD) issue of semiconductor products are not only revealed by the low yield issue during manufacturing, but also by the other reliability issues, especially in the devices with the thinner gate oxide, shorter channel length, shallower drain/source junction, lightly-doped drain (LDD) structure and salicided process in deep sub-micron CMOS technology. To enhance the ESD robustness of CMOS ICs, the efficient on-chip ESD protection circuit is required to be designed and placed in each I/O cell to prevent the damage on the silicon die. For general industrial specification, IC products have to sustain at least 2 kV of Human-Body-Model (HBM) ESD event, 200 V of Machine-Model (MM) ESD event. Therefore, the ESD protection circuits must be placed around the input and output pads of ICs for protecting them from the ESD events. Gate-grounded NMOS (GGNMOS) transistors are placed nearby output pads for output driving options and ESD protection considerations.

A GGNMOS device is formed by shorting the gate to the source as shown in Fig. 1.1 The gate-grounded ensures that the device is never turned on during normal operation. Under an ESD zapping, the NPN BJT of the GGNMOS is turned on to discharge the ESD current. The I-V curve of gate-grounded NMOS transistor is shown in Fig. 1.2. Salicidation is one of the key processes for high performance quarter micron CMOS devices. Salicidation process not only reduces sheet resistance, but also reduces its ESD performance of GGNMOS dramatically [1]. ESD robustness

of salicided GGNMOS is only 30% of that of unsalicided GGNMOS. ESD robustness of salicided NMOS also drops dramatically with increasing TiSi2 thickness. This is primarily due to non-uniform distribution of current in the ESD device and current crowding within the salicided layer. Besides, shallow junction and LDD structure in deep-submicron CMOS technology lead to higher current density during ESD event, and hence more lower failure threshold [2], [3].

Because the GGNMOS transistors with salicidation have the non-uniform current distribution problem, only a few fingers turn on to discharge the ESD current, while others fingers do not share the current. That leads to lower ESD robustness. There are several solutions, such as salicide blocking [4], using external N-well ballast resistors [5], [6], ESD implantation methods [7]-[9] to improve ESD robustness in deep sub-micron CMOS process. However, the salicide blocking method, ESD implant methods are expensive because they need several extra mask and procedures.

In this work, we proposed two novel ESD protection NMOS transistors using FOX or dummy-gate structure with N-well ballast resistors to improve ESD robustness, without extra mask and process [10]. Moreover, the conventional devices with fully-salicided and salicide blocking structures are also compared with these two novel ESD protection devices.

1.2 Some Solutions for Conventional Fully-salicided GGNMOS

It is very important to make a ballast resistance between drain contact to gate edge of the multi-finger NMOS devices for uniform turn-on consideration. There are two solutions such as blocking salicidation of drain side and source side, using external N-well ballast resistors. The detail discussions will be shown as below.

1.2.1 Blocking Salicidation of the Drain Side and Source Side

Salicidation is now a regular feature of deep sub-micron CMOS process. With this option, the sheet resistance is reduced by more than an order of magnitude and thus improve circuit speed. However, the ESD robustness is dramatically degraded to about 30 percent compared with the ESD protection devices without salicidation. [1], [2], [11]. This is because the small resistance of salicidation would induce to non-uniform turn-on and current localization issues. Fig. 1.3 shows the cross-sectional view of NMOS transistors with salicidation, and salicide blocking structure. Fig. 1.4 shows the top view of NMOS transistor with salicide blocking structure. If salicide blocking process is applied, the ESD current flow lines will be much deeper instead of crowding within the salicidation layer. Thus, the ballast resistance of drain area will be increased to make multi-fingers of ESD protection devices uniform turn-on and solve the current localization issue. Compared to fully-salicided NMOS transistor, NMOS transistor with salicide blocking structure has higher ESD robustness. So, the ESD robustness of ESD protection devices can be improved by the salicide blocking method.

1.2.2 Using External N-well Resistors

Grounded-gate NMOS transistors are generally used as ESD protection devices in CMOS circuits. The transistor is often laid out as a multi-finger structure to save layout area. Under ESD stress condition, only a few fingers of the GGNMOS may be triggered on, and only a few parasitic NPN BJT can be turned on to discharge ESD current. This is because snapback phenomenon of BJT in the GGNMOS transistors, the voltage across the GGNMOS devices is pulled down too low to trigger on other fingers of GGNMOS devices. So, only a few fingers turn on to sustain the whole ESD

current and cause lower ESD robustness. One way to solve this problem is adding series resistance to each fingers, for instance by salicide blocking method, but it is too expensive to add an extra mask. In order to solve this problem without extra cost and improve ESD robustness, two novel NMOS with N-well resistors are proposed. A cross-sectional view of the FOX structure GGNMOS device with proposed N-well resistors is shown in Fig.1.5. In the figure, N-well resistor is formed only in drain area. The un-salicided N-well resistors may make a series resistance to ensure simultaneous triggering of multiple fingers, and to uniformly dissipate the electrostatic charge from ESD source and prevent current localization within salicided layer. The current flow lines of dummy-gate structure transistors with N-well resistors and that with conventional fully-salicided structure are compared as shown in Fig. 1.6 [12]. The current flow lines of dummy-gate structure transistors with N-well resistors will flow more deeper and uniform than that with conventional fully-salicided structure. The I-V curve of FOX structure GGNMOS transistor with external N-well resistors is also shown in Fig. 1.7. The slope of I-V curve of FOX structure GGNMOS with external N-well is lower than that with fully-salicided structure. As we know, slope of I-V curve is inverse proportional to turn-on resistance. So, the increased turn-on resistance of FOX structure GGNMOS with external N-well resistors would make simultaneous triggering of multiple fingers, thus contribute to ESD robustness. So, the multiple fingers of FOX structure GGNMOS transistors with external N-well resistors can be uniform turned on by this method, and it has better ESD robustness.

1.3 Thesis Organization

In Chapter 1, the ESD protection device using conventional gate-grounded NMOS (GGNMOS) is introduced. A discussion about the non-uniform turn-on and current localization problems of gate-grounded NMOS transistor utilizing salicidation

process is addressed. Two novel GGNMOS solutions, FOX and dummy-gate structure with external N-well ballast resistors are provided and discussed. We have a simple explanation for the thesis of the two novel solutions.

In chapter 2, two types of novel GGNOS devices, FOX structure transistor with external N-well resistors, dummy-gate structure transistor with external N-well resistors, are proposed, and the other two conventional devices, transistor with fully-salicided structure, transistor with salicide-blocking structure are also compared. These four types of GGNMOS devices are implemented in several experiments. Then we have a design methodology of experiment to clarify the influence of layout parameters. Channel length, channel width, fingers number and DCGS (Drain contact to gate spacing) of the ESD protection devices have been drawn and investigated. For more detail analysis, we also have an experiment design to test the influence of detailed layout parameters. The split items of layout parameters are salicide blocking region to gate spacing, separated N-well to N-well spacing, and N-well to gate spacing.

In chapter 3, the measured experimental results are given and investigated. The Human-Body-Model (HBM), Machine-Model (MM) ESD levels and Transmission Line Pulsing (TLP) It2 of different GGNMOS transistors with different dimensions of channel length, channel width, fingers number, DCGS, salicide blocking region to gate spacing, separated N-well to N-well spacing, N-well to gate spacing are investigated and compared. Some discussions of measured results of these four types of GGNMOS transistors are provided.

In chapter 4, failure analysis pictures are given and investigated. The difference of failure locations of these four types ESD protection devices (fully-salicided transistor, salicide blocking transistor, FOX structure transistor with external N-well resistors, and dummy-gate structure transistor with external N-well resistors) zapped

by HBM and MM ESD stress are compared and discussed.

Finally, the results and conclusions will be summarized in Chapter 5. A discussion of experimental and failure analysis results are given. Moreover, the future work about the effective GGNMOS transistors are addressed in Chapter 5.

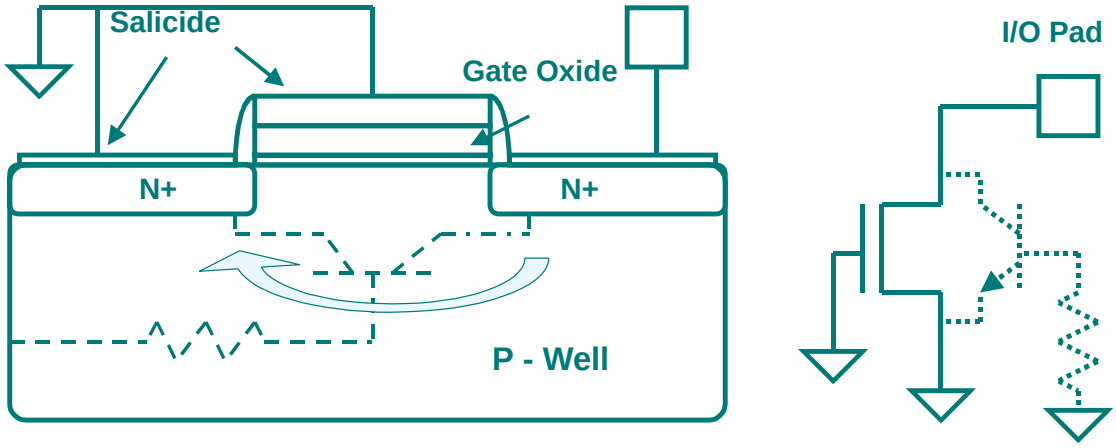


Fig. 1.1 A cross-sectional view of GGNMOS device showing the gate shorted to the source, and it's current dissipate path under ESD zapping.

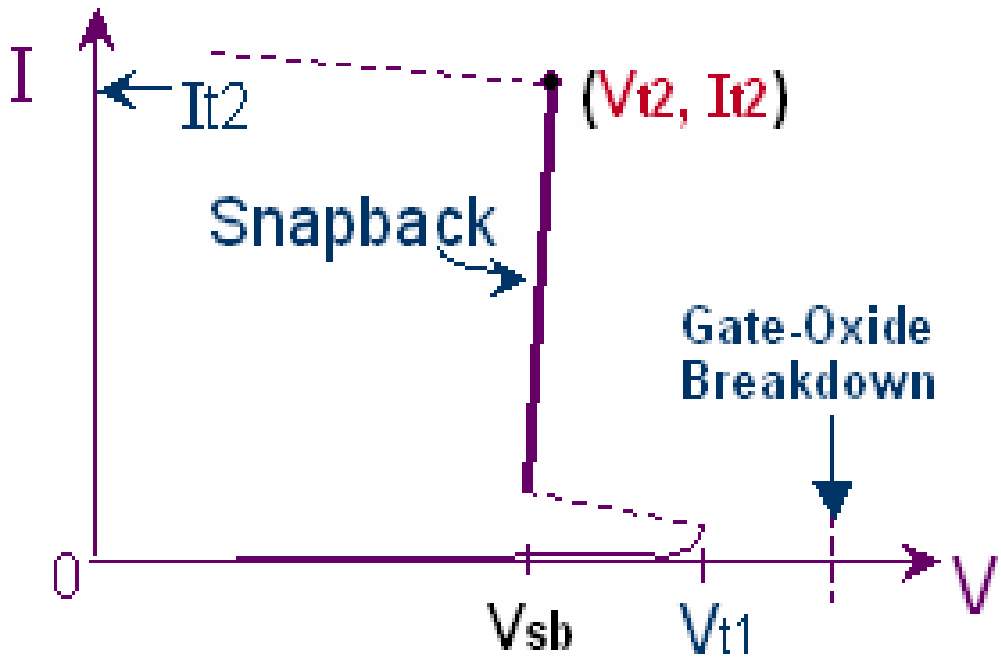
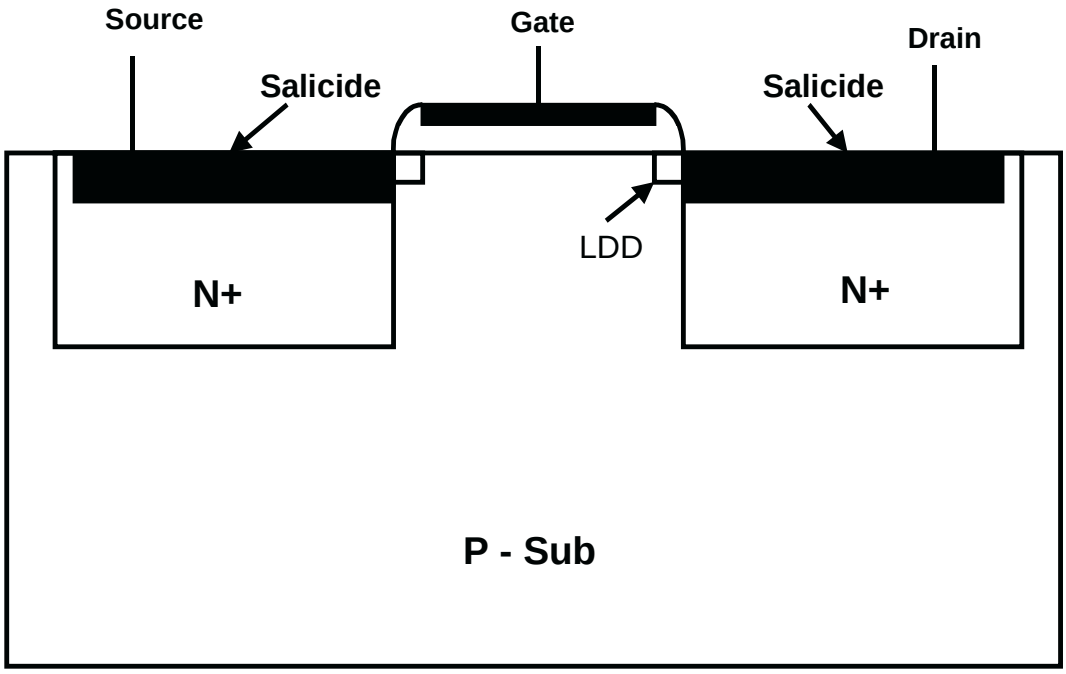
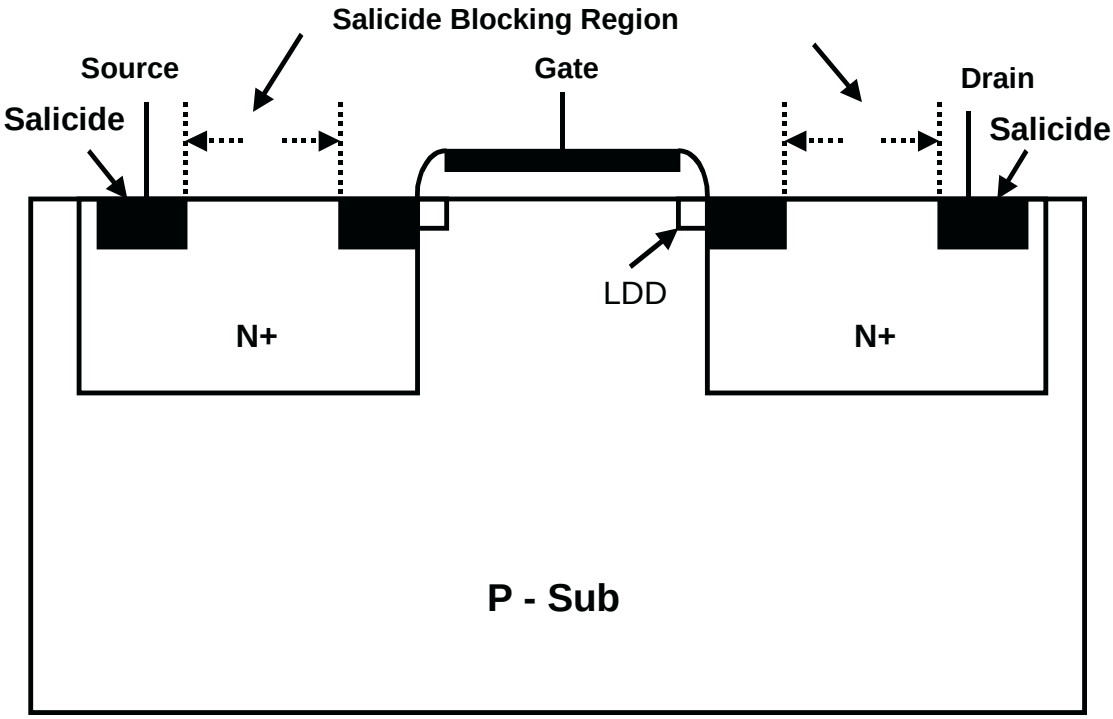


Fig. 1.2 The I-V curve of a gate-grounded NMOS.



(a)



(b)

Fig. 1.3 A cross-sectional view of NMOS transistors with (a) fully-salicided Structure, (b) salicide blocking structure.

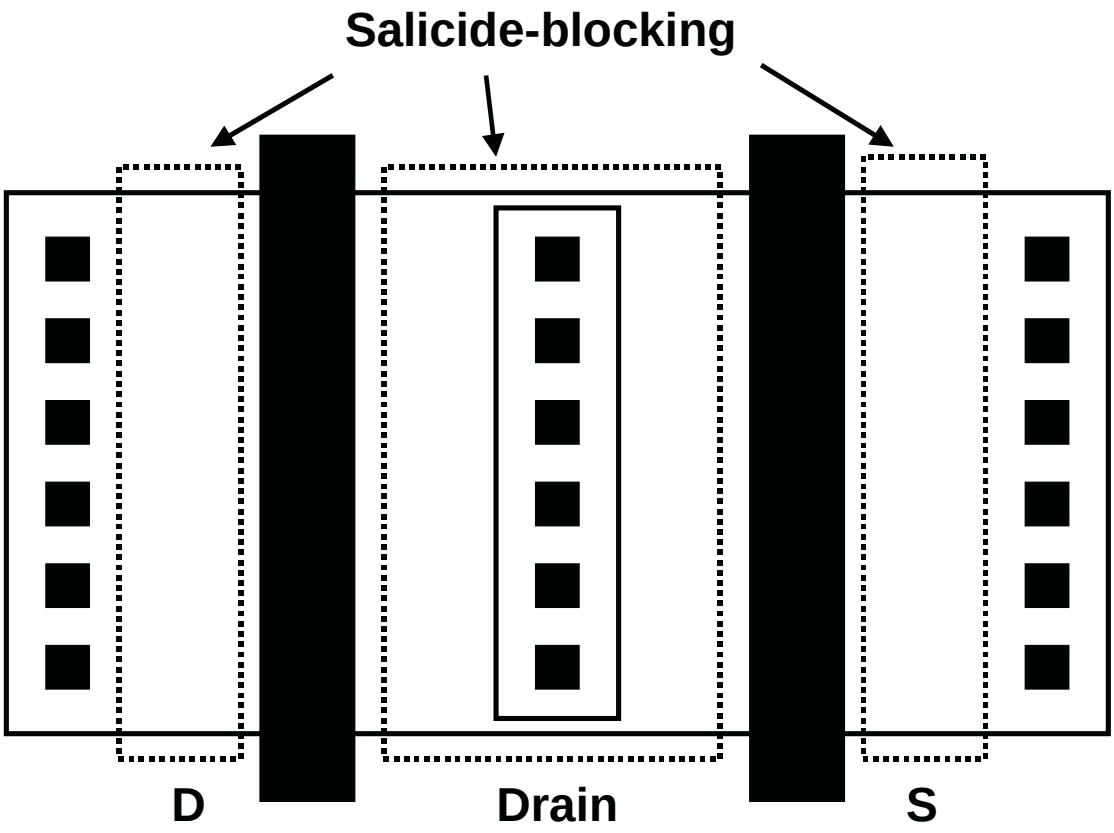


Fig. 1.4 A top view of NMOS transistor with salicide blocking.

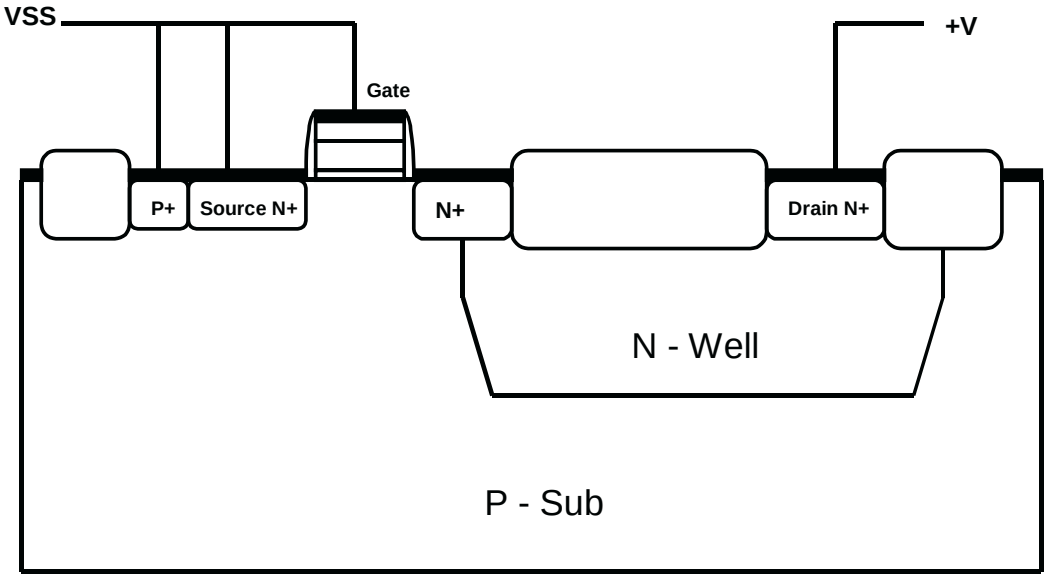
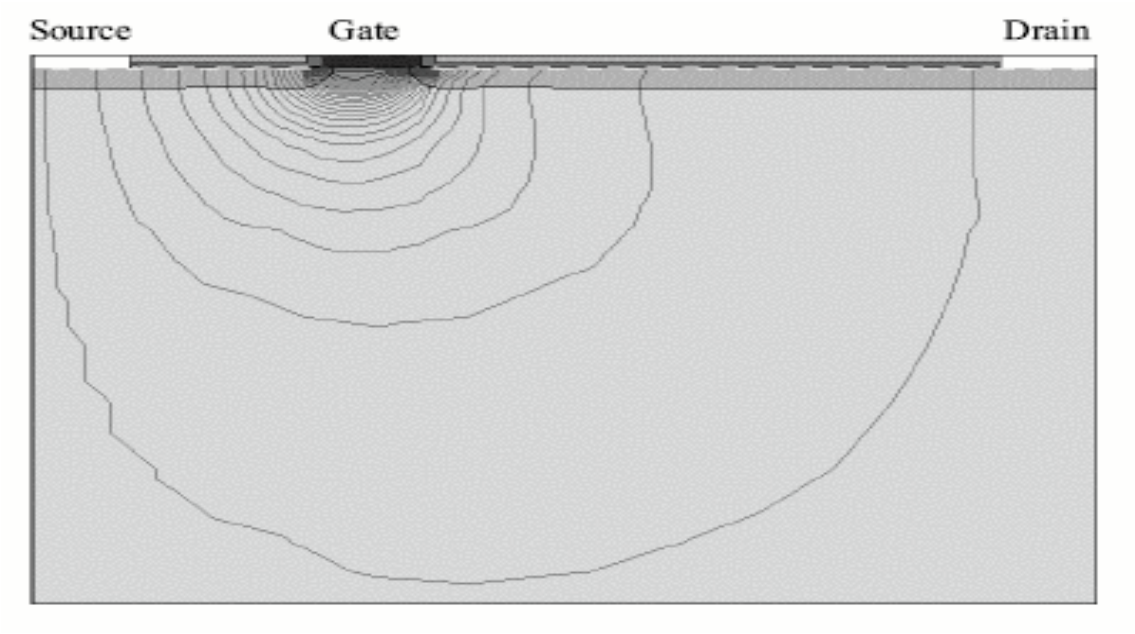
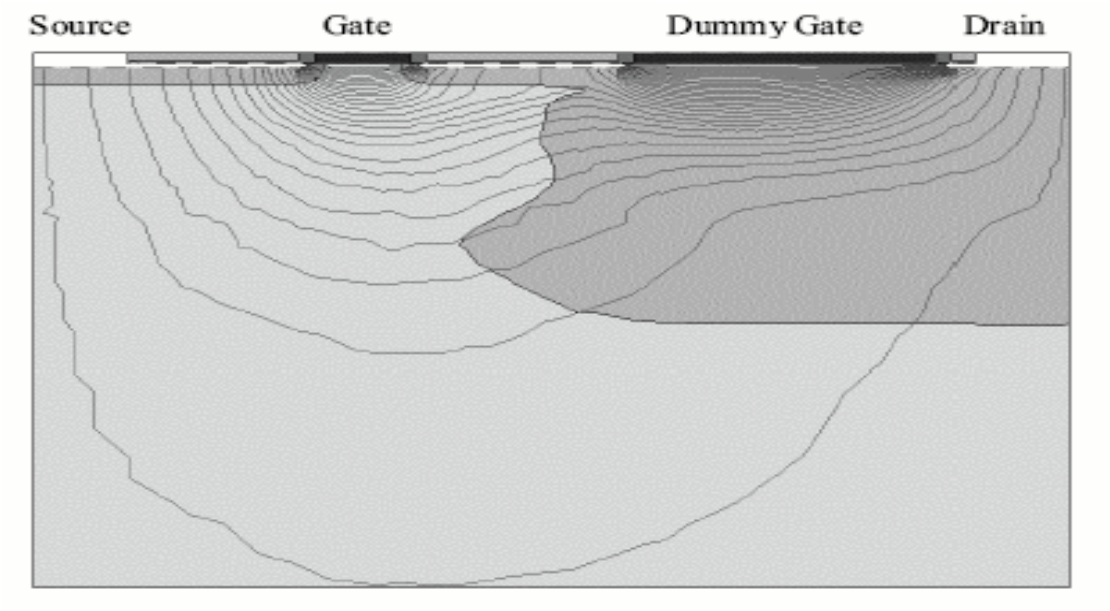


Fig. 1.5 A cross-sectional view of FOX structure GGNMOS transistor with external N-well resistors.



(a)



(b)

Fig. 1.6 Current flow lines of (a) fully-salicided structure NMOS transistor (b) dummy gate structure NMOS transistors with extrnal N-well resistors.

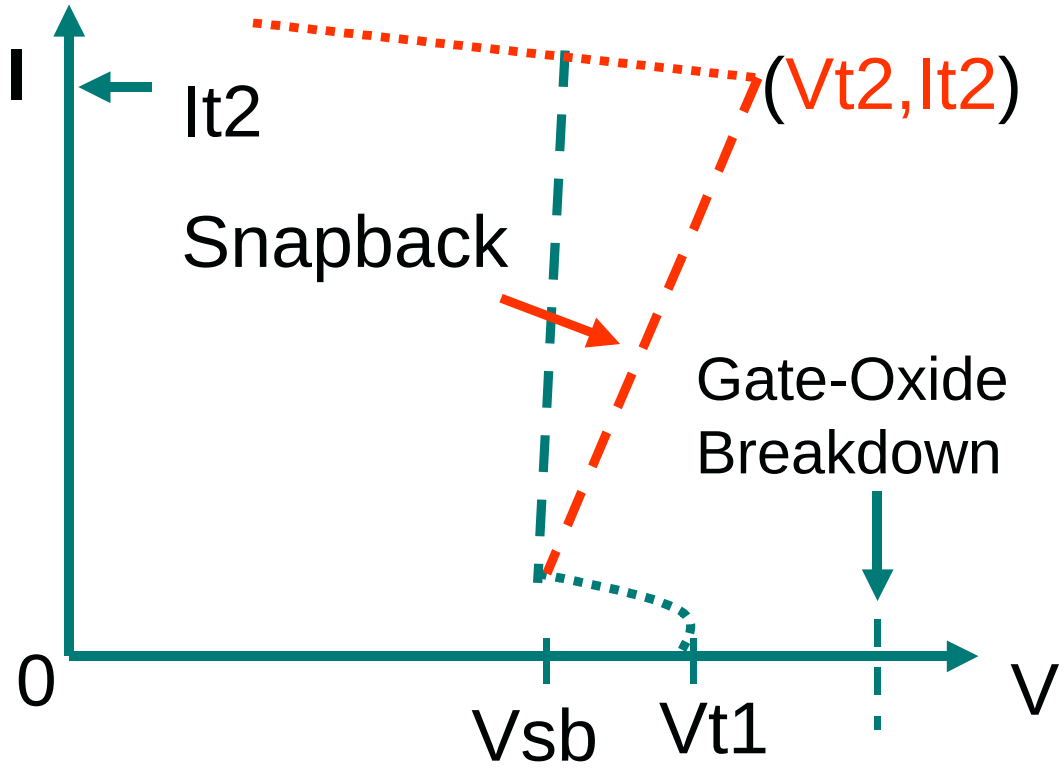


Fig. 1.7 I-V curve of FOX structure GGNMOS transistor with external N-well resistors.

CHAPTER 2

Robustness Design for GGNMOS Transistors

To ensure the multiple fingers uniform turn-on, adding series resistors is the major consideration. In this paper, we propose two novel salicided NMOS transistors in a 0.25 μm CMOS technology. Those two proposed NMOS transistors include FOX structure NMOS transistor with external N-well ballast resistors and dummy gate structure NMOS transistor with external N-well ballast resistor. Moreover, conventional NMOS transistors with fully-salicided structure and salicide blocking structure are also compared. Test structures were designed to quantify the influence of layout parameters on the ESD robustness of those four different types of GGNMOS transistors.

2.1 Proposed Two Types of Salicided GGNMOS Transistors

Fig. 2.1 shows the cross-sectional view of the conventional fully-salicided NMOS transistors. The series resistance between drain contact to gate is too small for multi-fingers to uniformly turn on. Fig. 2.2 shows the cross-sectional view of GGNMOS transistor fabricated with salicide blocking structure. In this structure, series resistance is bigger than that of fully-salicided GGNMOS. It is reported that ESD robustness of transistor with salicide blocking structure will be better than that with fully-salicided structure [4]. Fig. 2.3. shows the cross-sectional view of FOX structure GGNMOS transistor with external N-well resistors. In this structure, a gate layer named ‘FOX’ is formed in the drain area for salicide blocking. A high resistive drain area is formed by FOX without any extra process. Fig. 2.4. shows the cross-sectional view of dummy-gate structure GGNMOS transistor with external

resistors. In this structure, a gate layer named ‘dummy gate’ is formed between the drain contact to poly edge to block salicidation without any extra process. We have designed several test structures to investigate the influences of layout parameters on the ESD robustness of these modified NMOS transistors.

The fabrication flowchart of NMOS transistors with salicide blocking and dummy-gate structure NMOS transistors with external N-well resistors are shown in Fig. 2.5. Without applying PR and mask to block salicidation and without removing PR, dummy-gate structure transistors with external N-well resistors have the advantage of low-cost.

2.2 Experiment Design

For devices with salicide blocking process, current always flows in the N+ diffusion as path 1 in Fig. 2.6. If we adjust the clearance from salicide-blocking region to gate of transistors, current could flow more deeper as path 2 in Fig. 2.6. Thus, there will be more space for current flow and heat dissipation under ESD zapping. The split conditions of salicide-blocking region to gate spacing are -0.2 μm to 0.4 μm.

Fig. 2.7 shows the cross-sectional view of dummy-gate structure NMOS transistor with varied separated N-well to N-well spacing. If we separate N-well of different fingers as shown in Fig. 2.7. The breakdown voltage of N+ to P-sub junction is smaller than that of N-well to P-sub junction. The lower breakdown junction provide another dissipation path for ESD event. The new dissipation path is expected to increase ESD robustness of dummy-gate structure GGNMOS transistor. We make an experiment to see the influence of N-well to N-well spacing variations on the ESD robustness of the GGNMOS. The split conditions of N-well to N-well spacing variations are 0 μm to 2.4 μm.

Fig. 2.8 and Fig. 2.9 show the cross-sectional view of FOX structure and dummy gate structure NMOS transistor with varied N-well to gate spacing. If N-well boundary is moved more closer to gate as shown in Fig. 2.8, and Fig. 2.9, the breakdown voltage will be increased with decreasing N-well to gate spacing. ESD robustness will be suffered for increased breakdown voltage. For channel length is decreased, the leakage current will be enlarged due to short channel effect. To investigate the influence of N-well to N-well spacing on ESD robustness of these GGNMOS, the split conditions of clearance from N-well to N-well spacing are 0 μm to 2.4 μm.

Test structures were designed to quantify the influence of layout parameters on the ESD robustness of the proposed novel NMOS transistors. For those NMOS transistors, the split items are channel length, drain contact-to-gate spacing (DCGS), and the number of fingers, salicide blocking region to gate spacing, separated N-well to N-well spacing and N-well to gate spacing. The top view of test structure and its channel length, DCGS, SCGS definitions are shown in Fig. 2.10.

Fig. 2.11 shows the layout floor plane of test chips fabricated in a 0.25 μm CMOS process. There are two chips including Chip 2 and Chip 3 are fabricated. Two banks are designed in each chip. The number of NMOS transistors is 15 for each type of structures. The package type is 64TSOP in ceramics material. The discrete test transistor has four pads. One is for the gate, one is for source, the others are for p-substrate and drain, respectively.

2.3 Summary

To compare the robustness of different types of GGNMOS transistors, some split items are investigated. The split items include channel length, channel width, drain

contact-to-gate spacing (DCGS), and the number of fingers. For ESD robustness optimization, salicide blocking region to gate spacing, separated N-well to N-well spacing, N-well to gate spacing are also implemented in this experiment design.

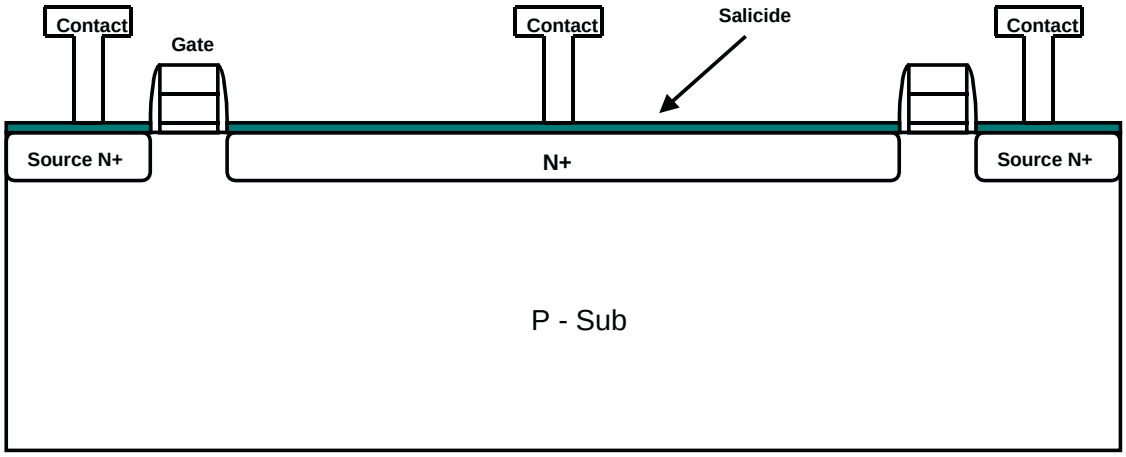


Fig. 2.1 Cross-sectional view of fully-salicided NMOS transistor.

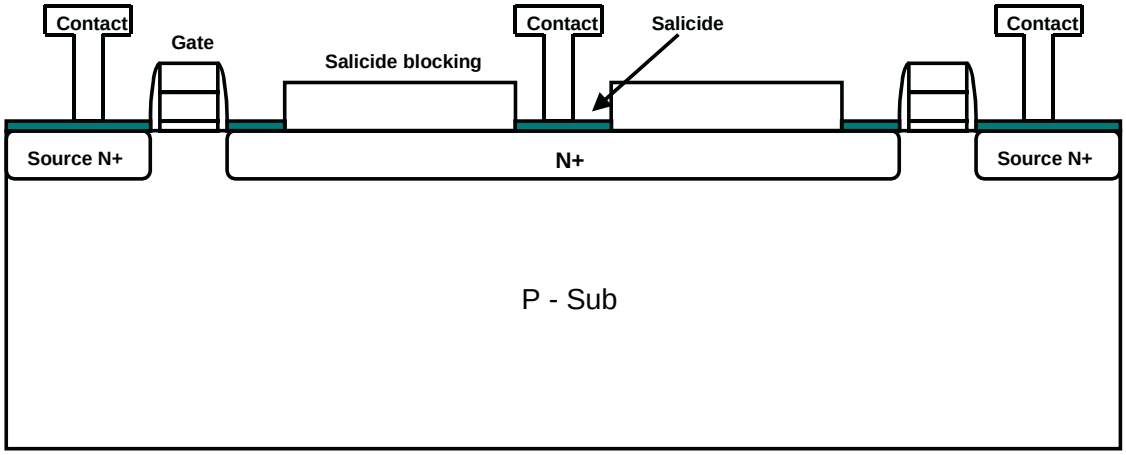


Fig. 2.2 Cross-sectional view of NMOS transistor with salicide blocking structure.

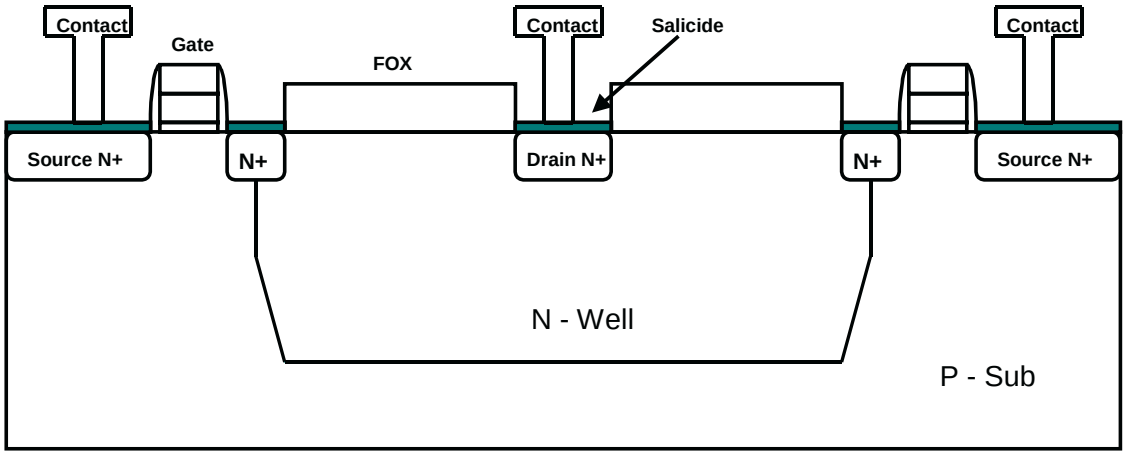


Fig. 2.3 Cross-sectional view of FOX structure NMOS transistor with external N-well resistors.

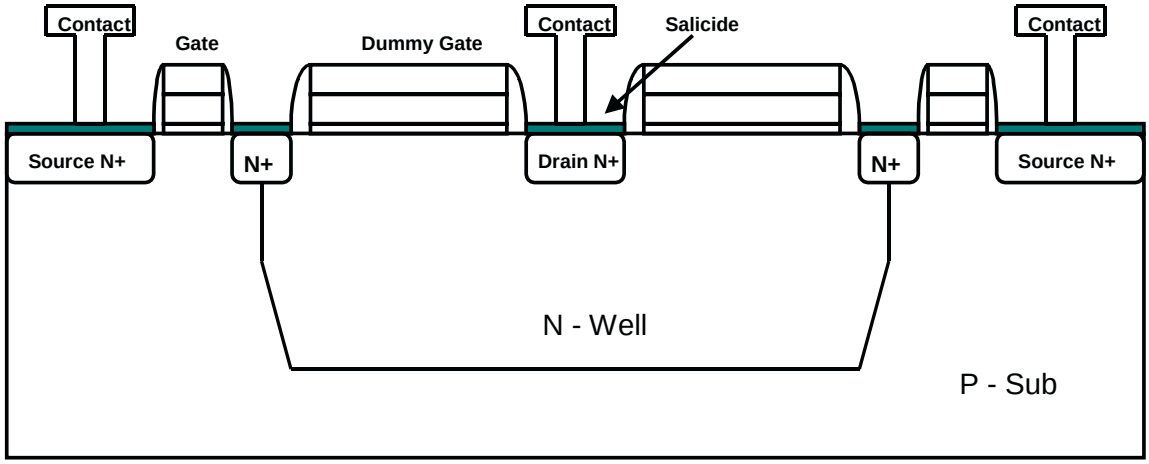


Fig. 2.4 Cross-sectional view of dummy-gate structure NMOS transistor with external N-well resistors.

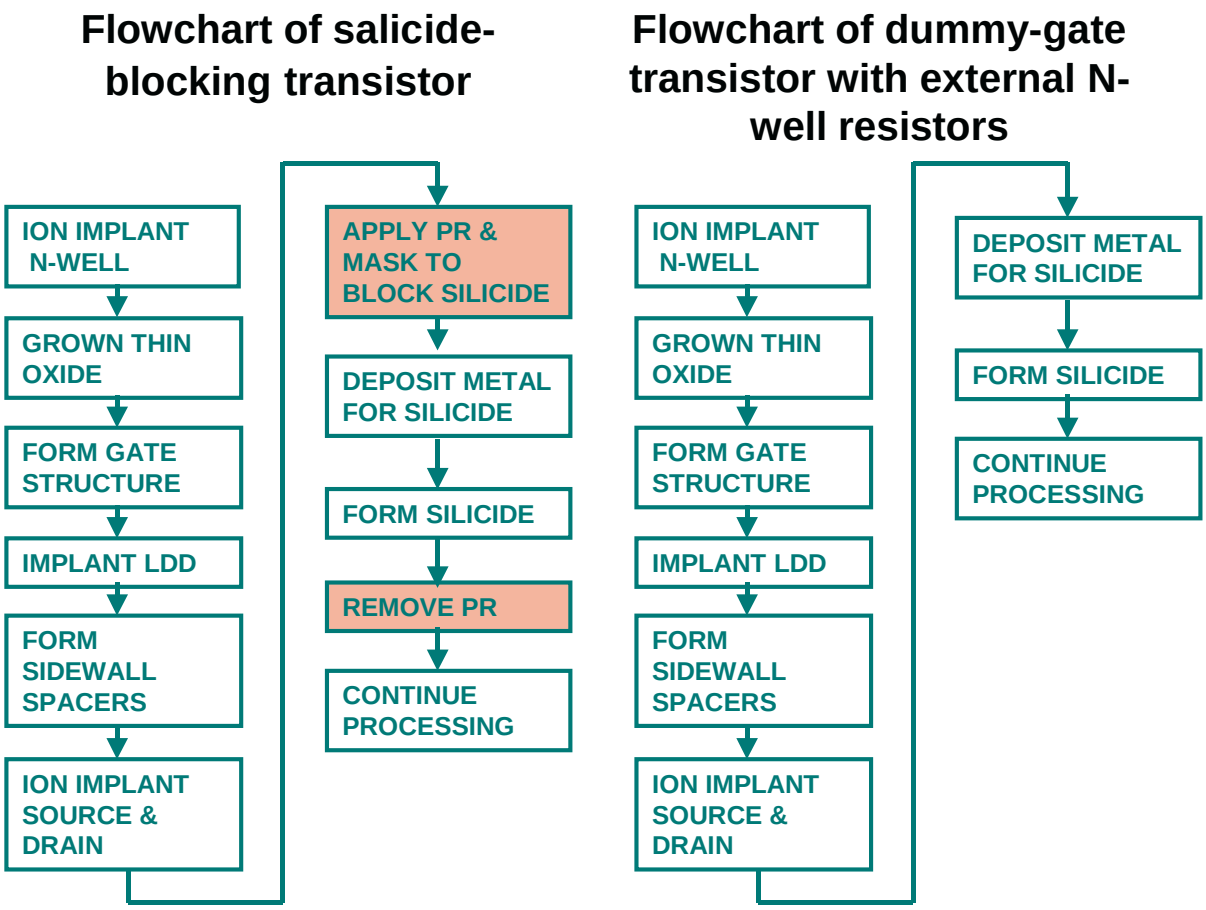


Fig. 2.5 Flowchart of salicide blocking structure transistor and dummy-gate structure transistor with external N-well resistors.

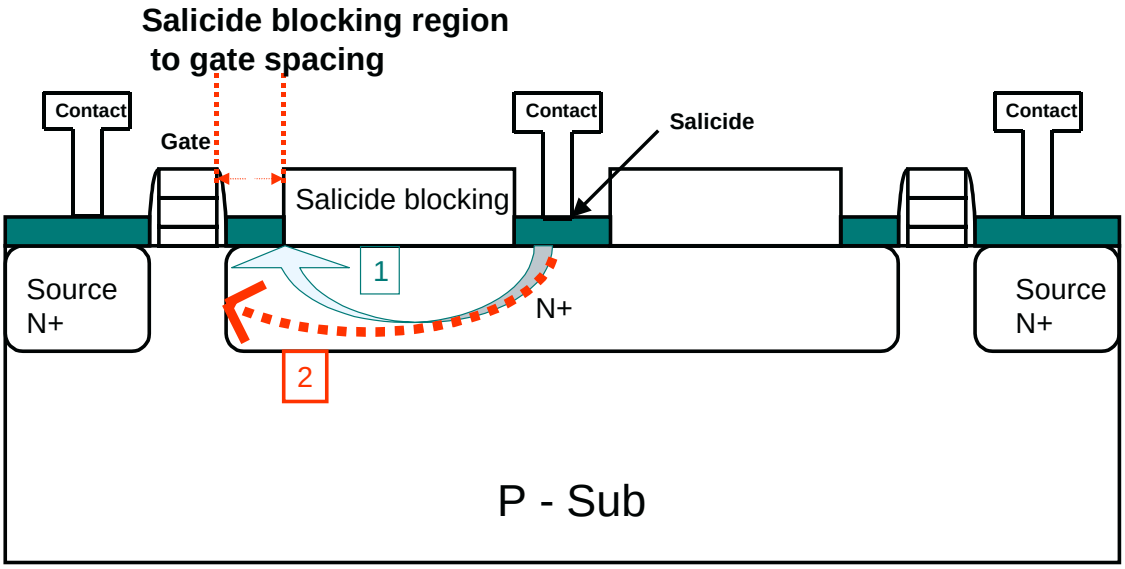


Fig. 2.6 Cross-sectional view of salicide blocking structure NMOS transistor with varied salicide blocking region to gate spacing.

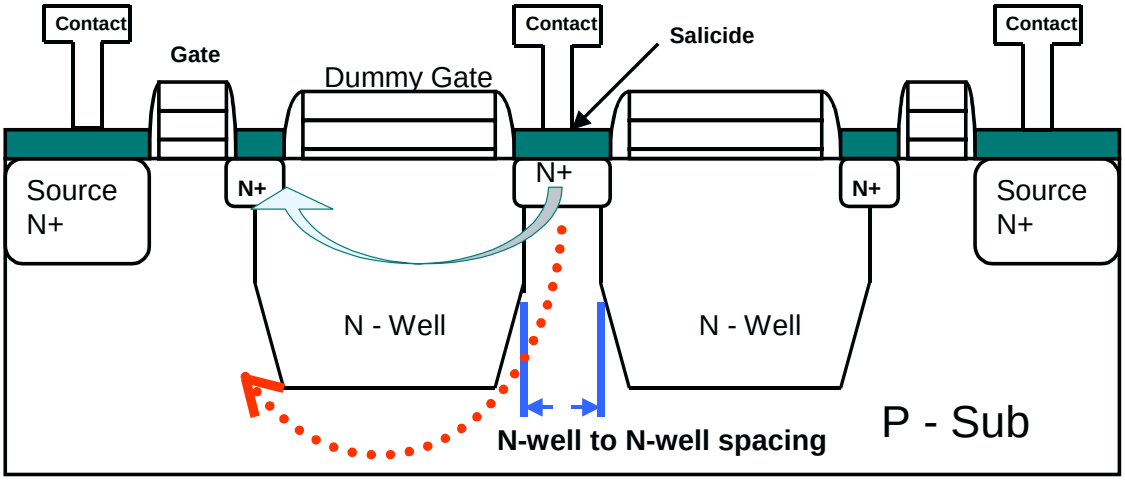


Fig. 2.7 Cross-sectional view of dummy-gate structure NMOS transistor with varied separated N-well to N-well spacing.

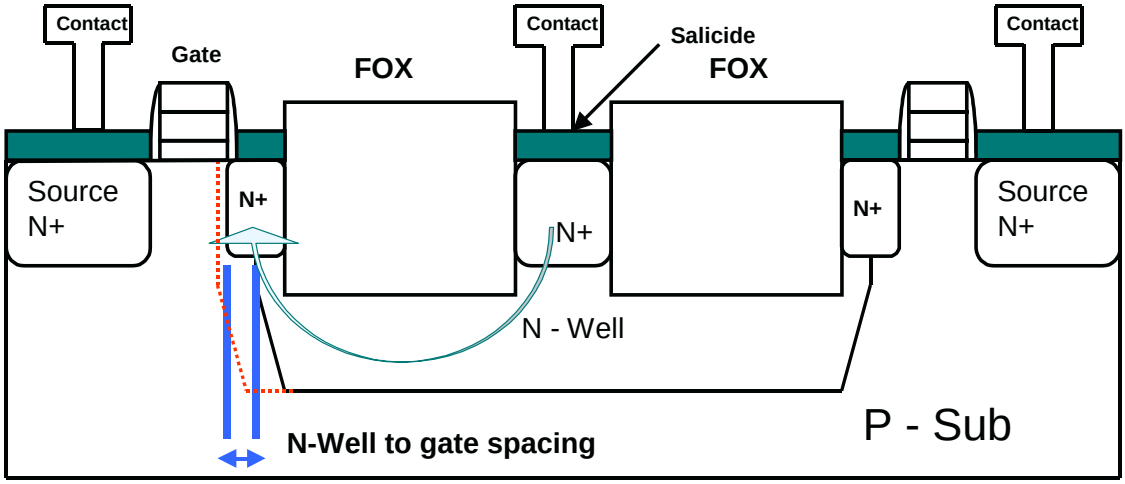


Fig. 2.8 Cross-sectional view of FOX structure NMOS transistor with varied N-well to gate spacing.

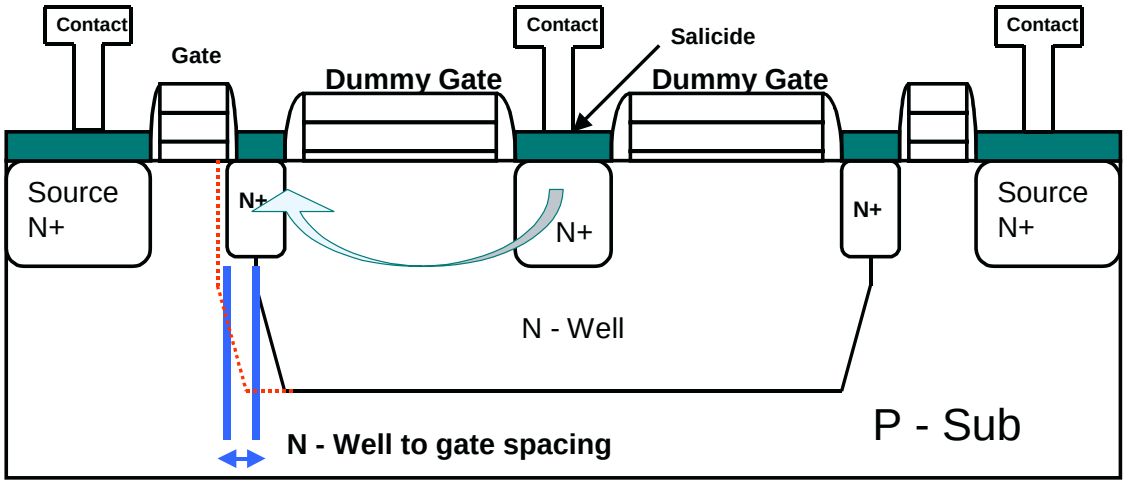


Fig. 2.9 Cross-sectional view of dummy-gate structure NMOS transistor with varied N-well to gate spacing.

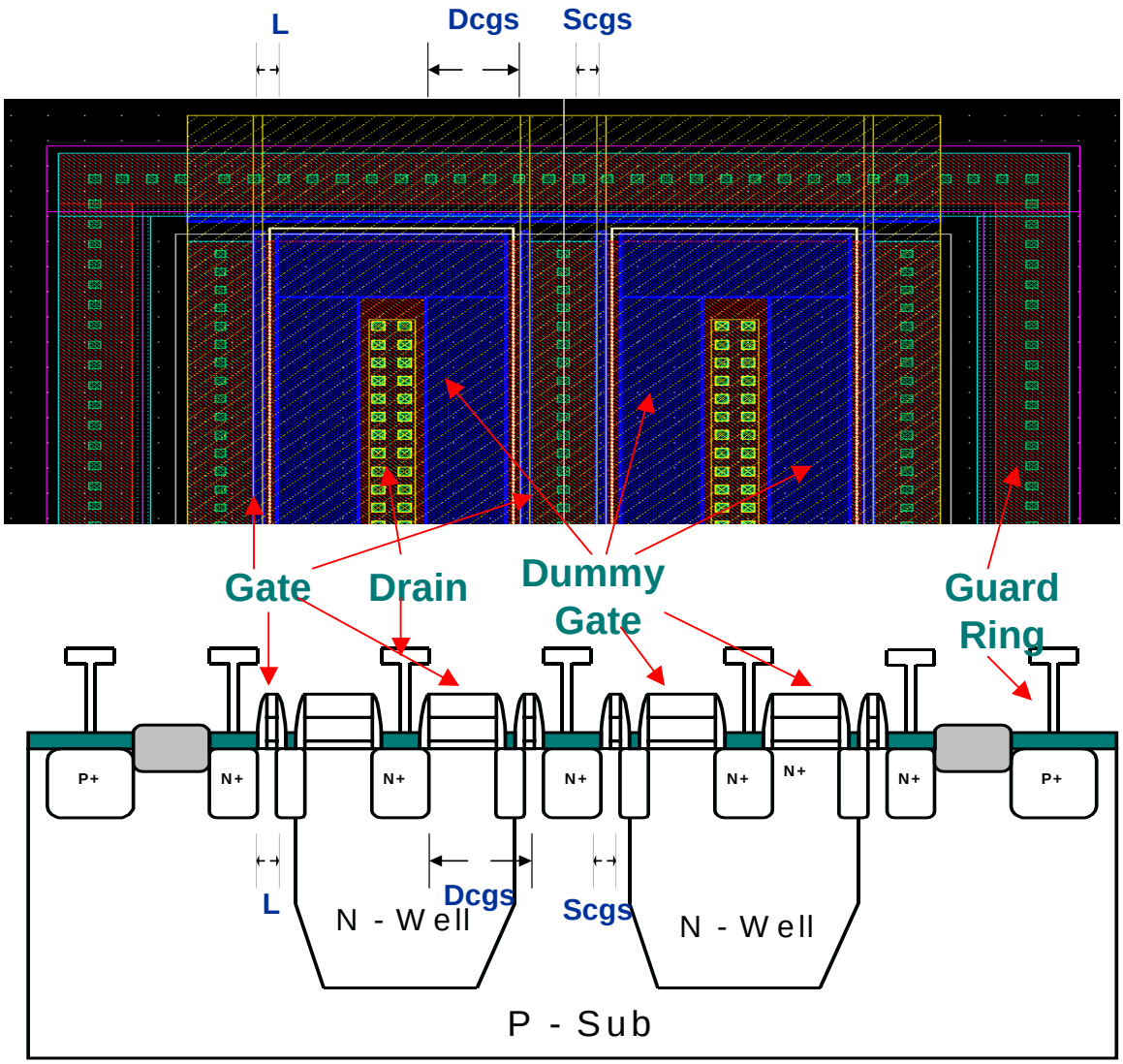


Fig. 2.10 The layout pattern and corresponding devices structure of dummy-gate structure NMOS transistor in 0.25 μm salicided CMOS process.

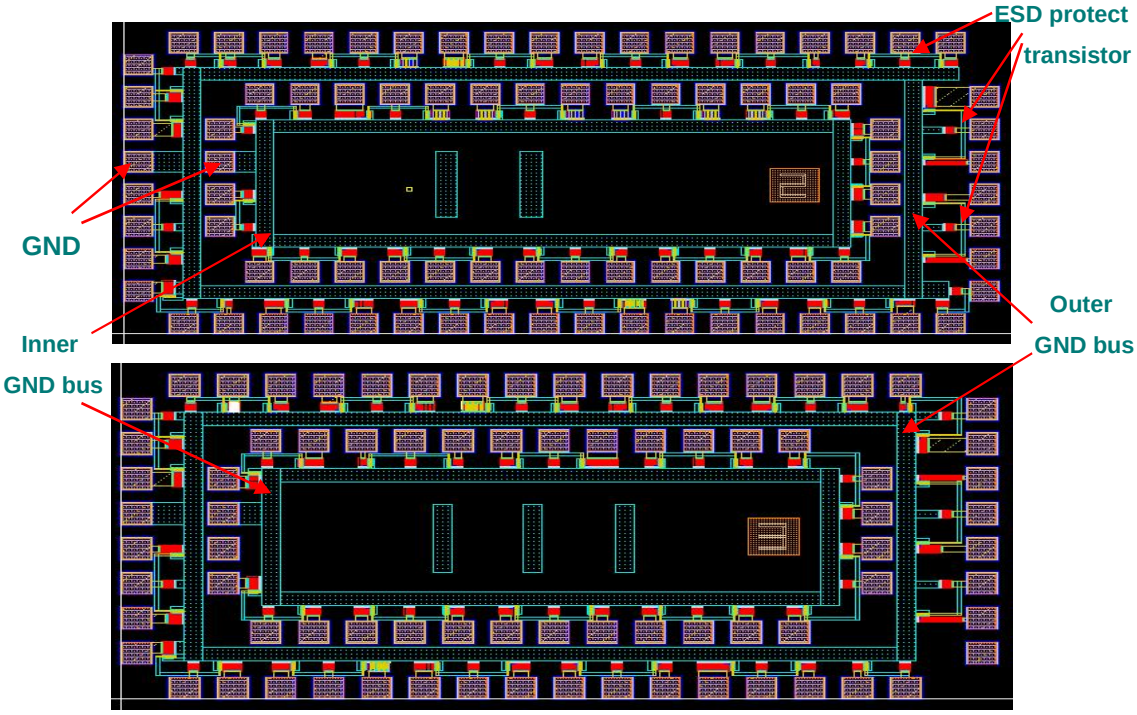


Fig. 2.11 Layout floor plane of test chips in 0.25 μm CMOS process.

CHAPTER 3

Experiment Results

The I-V characteristics of the four types GGNMOS transistors mentioned above are measured by the Tektronix 370A I-V curve tracer. The HP4155C parameter analyzer is used to measure the device I-V curves and leakage current. The ESD robustness of fully-salicided GGNMOS transistor, salicide-blocking GGNMOS transistor, salicide blocking structure GGNMOS transistor with external N-well resistors, and dummy gate structure GGNMOS transistor with external N-well resistors under the Human Body Model (HBM) ESD stress and Machine Model (MM) ESD stress are measured by the ZapMaster ESD tester, produced by KeyTek Instrument Corp. The transmission line pulsing (TLP) system is used to measure the device turn-on behavior and second breakdown characteristics (It2, Vt2) for double confirm the ESD robustness.

3.1 TLP I-V Curve Measurement Results

The transmission line pulsing (TLP) system has been used to measure the device turn-on behavior and second breakdown characteristics (It2,Vt2) under ESD stress condition. I-V curves measured by TLP system show the parasitic NPN bipolar trigger voltage (Vt1), holding voltage (Vh), second breakdown voltage (Vt2), and second breakdown current (It2) of NMOS transistor. Fig. 3.1(a), Fig. 3.1(b), Fig. 3.2(a) and Fig. 3.2(b) show the four type GGNMOS measured by TLP system respectively. The gate length and width of four different types of transistors are 0.25 μm and 30 μm, respectively, DCGS/SCGS are 3 μm/0.4 μm, and unit finger width is 30 μm.

TLP measured I-V curves of NMOS transistors with fully-salicided structure,

NMOS transistors with salicide-blocking structure, FOX structure NMOS transistor with external N-well resistors and dummy-gate structure NMOS transistor with external N-well resistors are compared as shown in Fig. 3.3 In this figure, slopes of FOX structure NMOS transistor with external N-well resistors and dummy-gate structure NMOS transistor with external N-well resistors are much greater than those of fully-salicided and salicide-blocking structure transistors because of the external N-well resistors. Due to the application of STI, turn-on resistance of transistor with FOX structure is greater than that with dummy-gate structure. So, I-V slope of FOX structure NMOS transistor with external N-well resistors is greater than that of dummy-gate structure NMOS transistor. Due to the N+ resistor under salicide-blocking area, I-V slope of transistors with salicide-blocking structure is greater than that with fully-salicided structure. From the experimental results, the It2 levels are 2.135 A, 3.669 A, 0.773 A, 0.698 A, for fully-salicided NMOS transistor, salicide-blocking NMOS transistor, FOX structure NMOS transistor with external N-well resistors and dummy-gate structure NMOS with external N-well ballast resistors, respectively. The ESD robustness of fully-salicided transistor is greater than that of transistors with FOX, dummy-gate structures.

3.2 TLP, HBM, and MM Results of GGNMOS Transistors with Different DCGS

There are four different ESD testing pin combinations with positive or negative voltage at each input or output pin respect to the grounded VDD or VSS pins are usually used to measure the ESD robustness as shown in Fig. 4. The industrial HBM and MM ESD testing standards are used to find the ESD robustness of the fabricated ESD protection circuits in a 0.25 μm CMOS process. The testing steps of HBM is

started from 500 V with step of 100 V increasing until failure (maximum range is 8 kV), and the MM testing is started from 50 V with step of 25 V increasing until failure. The failure criterion is generally defined as voltage shift 30% at 1 μA.

TLP measured It2, HBM ESD level and MM ESD level with varied channel length, channel width, finger numbers, DCGS, N-well to N-well spacing and salicide blocking region to gate spacing are shown in Table 3.1, Table 3.2, and Table 3.3. Fig. 3.5 show the TLP measured It2 of GGNOS transistors with varied DCGS. In the figure, the TLP measured It2 of transistor with FOX structures increase with increasing DCGS. For the other three types of transistors, there are no dependence between DCGS and TLP measures It2. Fig. 3.6 shows the measured HBM ESD level of GGNOS transistors with varied DCGS. In the figure, HBM ESD robustness of both the FOX and dummy-gate structure transistors increase with the increasing DCGS, and HBM ESD robustness of FOX and dummy-gate structure transistors are almost the same with that of fully-salicided transistor when DCGS is greater than 5μm. Fig. 3.7 show the measured MM ESD level of GGNMOS transistors with varied DCGS. In the figure, MM ESD robustness of transistor with dummy-gate structure is better than that of transistor with fully-salicided structure when DCGS is greater than 3.6 μm. The MM results are dramatically different with that of TLP and HBM measured results.

3.3 TLP, HBM, and MM Results of GGNMOS Transistors with Different Gate Length

Fig. 3.8, Fig. 3.9 and Fig. 3.10 show the TLP measured It2, HBM, and MM ESD levels of GGNMOS transistors with varied gate length, respectively. TLP measured It2, HBM and MM ESD robustness of transistor with fully-salicided structure, transistor with salicide-blocking structure, transistor with FOX structure, and

transistor with dummy-gate structure have no dependence with gate length. MM ESD robustness of dummy-gate structure GGNMOS transistor is better than that of fully-salicided structure transistor. The result is different with TLP and HBM measured results.

3.4 TLP, HBM, and MM Results of GGNMOS Transistors with Different Number of Fingers

Fig. 3.11, Fig. 3.12, and Fig. 3.13 show the TLP measured It2, HBM, MM ESD levels of GGNMOS transistors with varied fingers number, respectively. TLP measured It2, HBM and MM ESD robustness of transistors with dummy-gate structure slightly increase with increasing fingers number. However, MM ESD robustness of dummy-gate structure GGNMOS transistor is better than that of fully-salicided structure transistor. That result is quite different with TLP and HBM measured results, and it is the same with that mentioned in Chapter 3.2 and Chapter 3.3.

3.5 TLP, HBM, and MM Results of GGNMOS Transistors with Different Channel Width

Fig. 3.14, Fig. 3.15, and Fig. 3.16 show the TLP measured It2, HBM, MM ESD levels of GGNMOS transistors with varied channel width, respectively. In the figures, TLP measured It2, HBM and MM ESD robustness of all types of GGNMOS transistors increase with increasing channel width. MM ESD robustness of dummy-gate structure GGNMOS transistor is better than that with fully-salicided structure. The result is also different with TLP and HBM measured results. That result is the same with that mentioned in Chapter 3.2, Chapter 3.3 and Chapter 3.4.

3.6 TLP, HBM, and MM Results of GGNMOS Transistors with Different Salicide Blocking Region to Gate Spacing

Fig. 3.17, Fig. 3.18, and Fig. 3.19 show the TLP measured It2, HBM, MM ESD levels of GGNMOS transistors with varied salicide-blocking region to gate spacing. In the figures, varied salicide-blocking region to gate spacing is independent with ESD robustness of NMOS transistor with salicide-blocking structure. So, varied salicide-blocking region to gate spacing is not the effective factor for ESD robustness level.

3.7 TLP, HBM, and MM results of GGNMOS transistors with different separated N-well to N-well spacing

Fig. 3.20, Fig. 3.21, and Fig. 3.22 show the TLP measured It2, HBM, MM ESD levels of GGNMOS transistors with varied N-well to N-well spacing, respectively. In the figures, varied N-well to N-well spacing is independent with ESD robustness for NMOS transistors with dummy-gate structure. So, varied N-well to N-well spacing is not the effective factor for ESD robustness level.

3.8 TLP, HBM, and MM Results of GGNMOS Transistors with Different N-well to Gate Spacing

Fig. 3.22 shows the TLP measured It2, HBM, MM ESD levels of GGNMOS transistors with varied N-well to gate spacing. In the Figure, the leakage current of GGNMOS transistors both with FOX, and dummy-gate structures dramatically increase with decreasing N-well to gate spacing. In the Figure, leakage current of device is greater than failure criterion before ESD zapping as N-well to gate spacing

is less than 0.25 μm. As mentioned in Chap. 2.2, if N-well boundary is moved more closer to gate, the leakage will be enlarged due to short channel effect. If N-well to gate space is less than 0.25 μm, short channel effect will lead to great leakage through channel. So, devices fail before ESD zapping if N-well to gate space is less than 0.25 μm.

3.9 Discussion

We fixed gate width, gate length, DCGS, fingers number of test dummy-gate structure devices to 240 μm, 0.25 μm, 3 μm, 8, respectively, except for drain contact to dummy-gate spacing. Drain contact to dummy-gate space is found to be sensitive to HBM ESD robustness. The average HBM robustness of dummy-gate structure transistors with drain contact to dummy-gate spacing of S = 1 μm is 4 kV in Fig. 3.18, while that with drain contact to dummy-gate spacing of S = 0.4 μm is only 2 kV in Fig. 3.6.

Based on the experiment results, the ESD robustness of dummy gate structure GGNMOS under MM zapping has better performance compared with other structure GGNMOS under TLP measurement and HBM zapping. Mechanisms under MM and HBM stress are not clear right now. To realize the mechanism under MM and HBM stress, further failure analysis will be done.

3.10 Summary

MM ESD robustness of proposed dummy-gate structure GGNMOS transistors is better than that of conventional transistor with fully-salicided structure. However, HBM ESD robustness of dummy-gate structure devices is sensitive to drain contact to gate spacing and drain contact to dummy-gate spacing. ESD robustness of transistors increases with increasing drain contact to gate spacing and drain contact to

dummy-gate spacing. HBM, MM ESDlevels are independent of separated N-well to N-well spacing for dummy-gate structure transistors. HBM, MM ESD levels are independent of salicide-blocking region to gate spacing for salicide-blocking transistors. Due to short channel effect induced leakage current, transistors with FOX and dummy-gate structures in N-well to N-well spacing experiment fail before ESD zapping if N-well to N-well spacing is less than 0.25 μm.

Table 3.1 The TLP measured It2, HBM ESD levels, and MM ESD levels of GGNMOS transistors with varied channel length, DCGS in 0.25 μm salicided CMOS process.

	TLP Current(A), PS-mode					HBM ESD Level(kV), PS-mode			
DCGS	S=1.4μm	S=2μm	S=3μm	S=3.6μm	S=5μm	S=1.4μm	S=2μm	S=3μm	S=3.6μm
Fully Salicided	2.26	2.28	2.27	2.25	1.81	4.58	4.79	4.95	4.15
RPO		3.51	4.07	3.76	3.47		7.43	7.40	7.24
FOX	0.38	0.36	0.84	1.36	2.35	0.63	0.70	1.38	2.38
Dummy Gate	0.65	0.80	0.86	0.88	0.84	1.18	1.60	2.18	2.20

		MM ESD Level(V), PS-mode				
DCGS	S=5μm	S=1.4μm	S=2μm	S=3μm	S=3.6μm	S=5μm
Fully Salicided	3.53	225.00	225.00	225.00	181.25	150.00
RPO	6.70		575.00	556.25	512.50	443.75
FOX	3.63	50.00	81.25	193.75	262.50	231.25
Dummy Gate	3.30	168.75	350.00	462.50	425.00	393.75

	TLP Current(A), PS-mode						HBM ESD Level(kV),PS-mode		
Gate Length	L=0.25μm	L=0.4μm	L=0.5μm	L=0.6μm	L=0.8μm	L=1.0μm	L=0.25μm	L=0.4μm	L=0.5μm
Fully Salicided	2.27	2.62	2.74	2.81	3.24	3.19	4.95	5.05	5.3625
RPO	4.07	4.05	3.73	3.89	3.85	3.69	7.55	7.2625	7.5875
FOX	0.84	0.81	1.05	0.91	0.95	0.86	1.375	1.55	1.775
Dummy Gate	0.86	0.87	0.88	0.88	0.97	0.87	2.175	2.275	1.75

				MM ESD Level(V), PS-mode					
Gate Length	L=0.6μm	L=0.8μm	L=1.0μm	L=0.25μm	L=0.4μm	L=0.5μm	L=0.6μm	L=0.8μm	L=1.0μm
Fully Salicided	5.475	5.625	5.675	225	231.25	243.75	262.5	275	275
RPO	7.4125	7.275	7.1625	556.25	543.75	525	525	512.5	525
FOX	1.725	1.85	1.5	193.75	200	200	231.25	256.25	250
Dummy Gate	1.725	1.675	1.625	462.5	375	400	368.75	381.25	437.5

Table 3.2 The TLP measured It2, HBM ESD levels, and MM ESD levels of GGNMOS transistors with varied fingers number, gate width in 0.25 μm salicided CMOS process.

No of Fingers	No=2	No=4	No=6	No=8	No=10	No=2	No=4	No=6	No=8
Fully Salicided	1.76	2.25	2.40	2.27	2.34	3.43	4.64	4.95	4.95
RPO	3.75	4.52	2.47	4.07	3.75	6.36	7.36	4.95	7.55
FOX	0.73	0.72	0.72	0.90	0.85	1.08	1.25	1.38	1.38
Dummy Gate	0.73	0.79	0.77	0.79	0.87	1.58	1.58	1.68	2.18

		MM ESD Level(V), PS-mode				
No of Fingers	No=10	No=2	No=4	No=6	No=8	No=10
Fully Salicided	4.69	100	225	212.5	225	200
RPO	7.11	500	556.25	225	556.25	512.5
FOX	1.75	118.75	137.5	175	193.75	193.75
Dummy Gate	2.33	287.5	418.75	437.5	462.5	462.5

	TLP Currnt(A), PS-mode					HBM ESD Level(kV), PS-mode			
Gate Width	W=60μm	W=120μm	W=180μm	W=240μm	W=480μm	W=60μm	W=120μm	W=180μm	W=240μm
Fully Salicided	0.48	1.12	1.79	2.27	4.34	1.13	2.26	3.36	4.95
RPO	1.68	2.73	3.18	4.87	6.00	2.00	3.64	5.31	7.55
FOX	0.58	0.60	0.71	0.84	0.78	0.95	1.20	1.30	1.38
Dummy Gate	0.65	0.75	0.87	0.86	1.17	1.30	1.70	1.50	2.18

		MM ESD Level(V), PS-mode				
Gate Width	W=480μm	W=60μm	W=120μm	W=180μm	W=240μm	W=480μm
Fully Salicided	8.00	50	118.75	150	225	393.75
RPO	7.70	181.25	286.75	406.25	556.25	981.25
FOX	1.30	125	168.75	212.5	193.75	281.25
Dummy Gate	2.93	200	337.5	393.75	462.5	631.25

Table 3.3 The TLP measured It2, HBM ESD levels, and MM ESD levels of GGNMOS transistor with varied N-well to N-well spacing, mask to gate spacing in 0.25 μm salicided CMOS process.

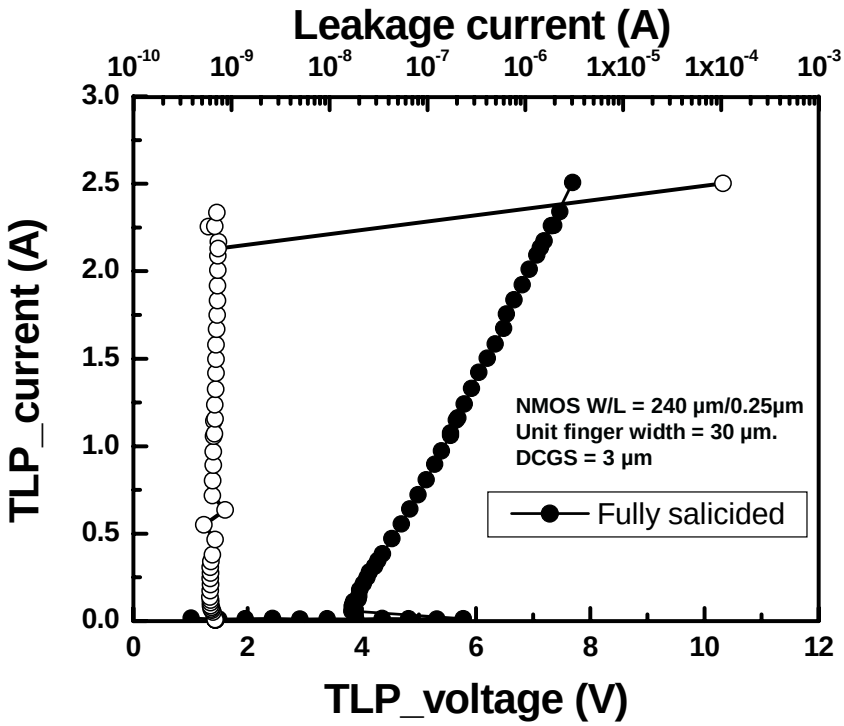
	TLP Current(A), PS-mode						HBM ESD Level(kV),PS-mode		
N-WellSpace Skew	S=0μm	S=0.3μm	S=0.6μm	S=1.2μm	S=1.8μm	S=2.4μm	S=0μm	S=0.3μm	S=0.6μm
DG Width=2.2	1.09	1.06	1.22	0.96	1.00	1.13	3.74	4.06	4.45
DG Width=0.5	0.71	0.71	0.71	0.80	0.94	0.78	1.20	1.20	1.18

				MM ESD Level(V), PS-mode					
N-WellSpace Skew	S=1.2μm	S=1.8μm	S=2.4μm	S=0μm	S=0.3μm	S=0.6μm	S=1.2μm	S=1.8μm	S=2.4μm
DG Width=2.2	3.74	2.46	2.74	568.75	537.5	493.75	500	481.25	331.25
DG Width=0.5	1.25	1.60	1.00	168.75	193.75	193.75	250	281.25	237.5

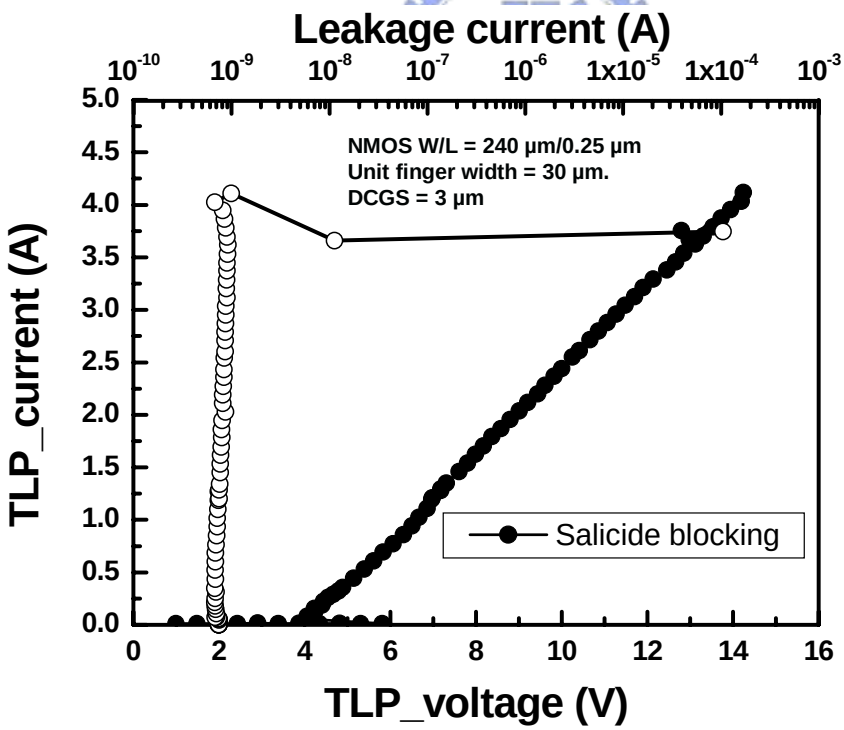
	TLP Currnt(A), PS-mode							HBM ESD Level(kV)	
RPO Sapce Skew	S=-0.2μm	S=-0.1μm	S=0μm	S=0.1μm	S=0.2μm	S=0.3μm	S=0.4μm	S=-0.2μm	S=-0.1μm
	4.19	4.08	3.92	4.15	4.13	5.01	4.07	7.05	7.23

	HBM ESD Level(kV), PS-mode					MM ESD Level(V), PS-mode			
RPO Sapce Skew	S=0μm	S=0.1μm	S=0.2μm	S=0.3μm	S=0.4μm	S=-0.2μm	S=-0.1μm	S=0μm	S=0.1μm
	7.10	6.80	7.33	186.63	7.55	587.5	556.25	556.25	550

	MM ESD Level(V), PS-mode		
RPO Sapce Skew	S=0.2μm	S=0.3μm	S=0.4μm
	550	543.75	556.25

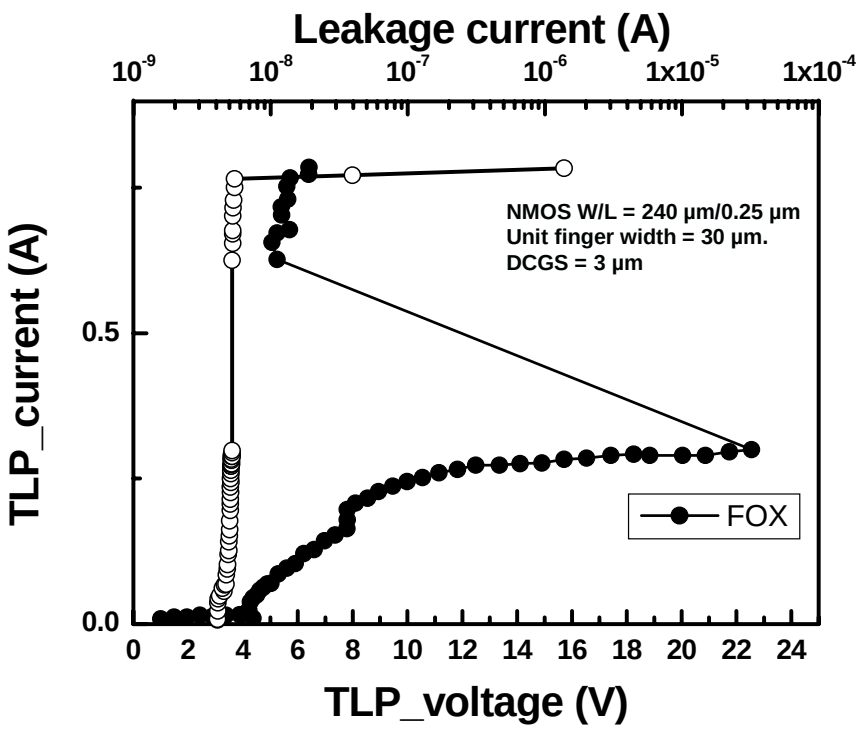


(a)

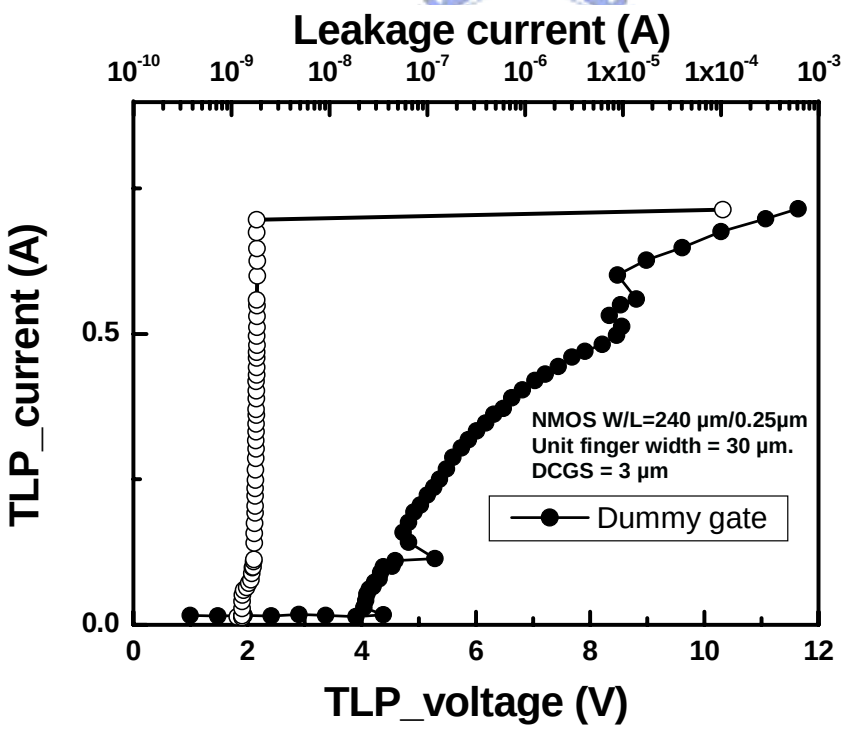


(b)

Fig. 3.1 The TLP measured I-V curve of (a) GGNMOS transistor with fully-salicided structure, (b) GGNMOS transistor with salicide blocking structure. NMOS = 240 μm/0.25 μm in 0.25 μm salicided CMOS process.



(a)



(b)

Fig. 3.2 The TLP measured I-V curve of (a) FOX structure GGNMOS transistor with external N-well resistors, (b) dummy-gate structure GGNMOS transistor with external N-well resistors. NMOS = 240 μm/0.25 μm in 0.25 μm salicided CMOS process.

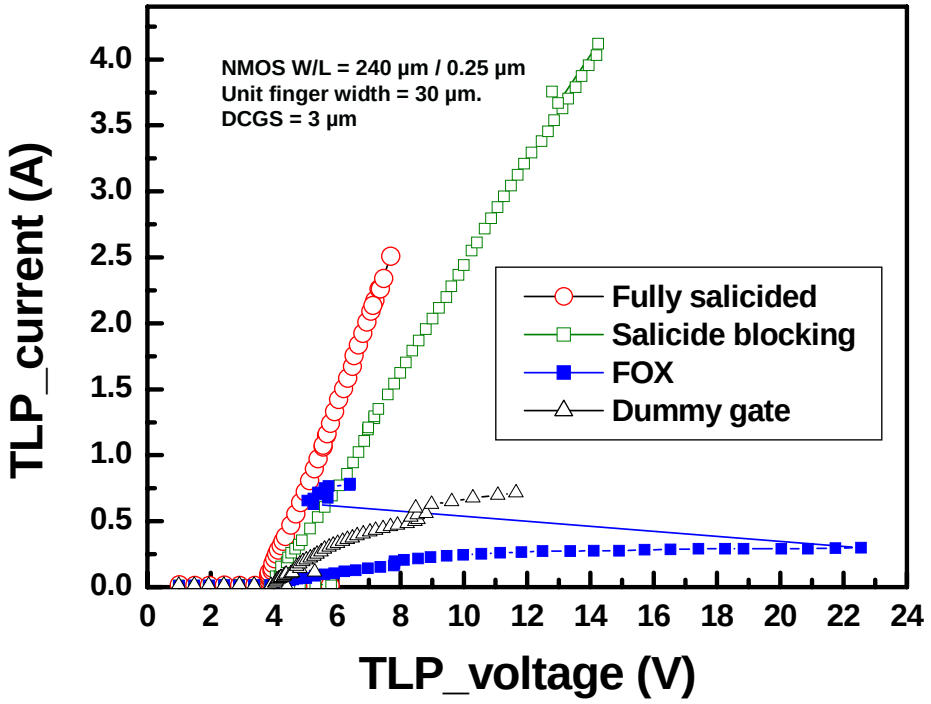


Fig. 3.3 The TLP measured I-V curves of GGNMOS transistor with fully-salicided structure, GGNMOS transistor with salicide-blocking structure, FOX structure GGNMOS transistor with external N-well resistor, dummy-gate structure GGNMOS transistor with external N-well resistor. NMOS = 240 μm/0.25 μm in 0.25 μm salicided CMOS process.

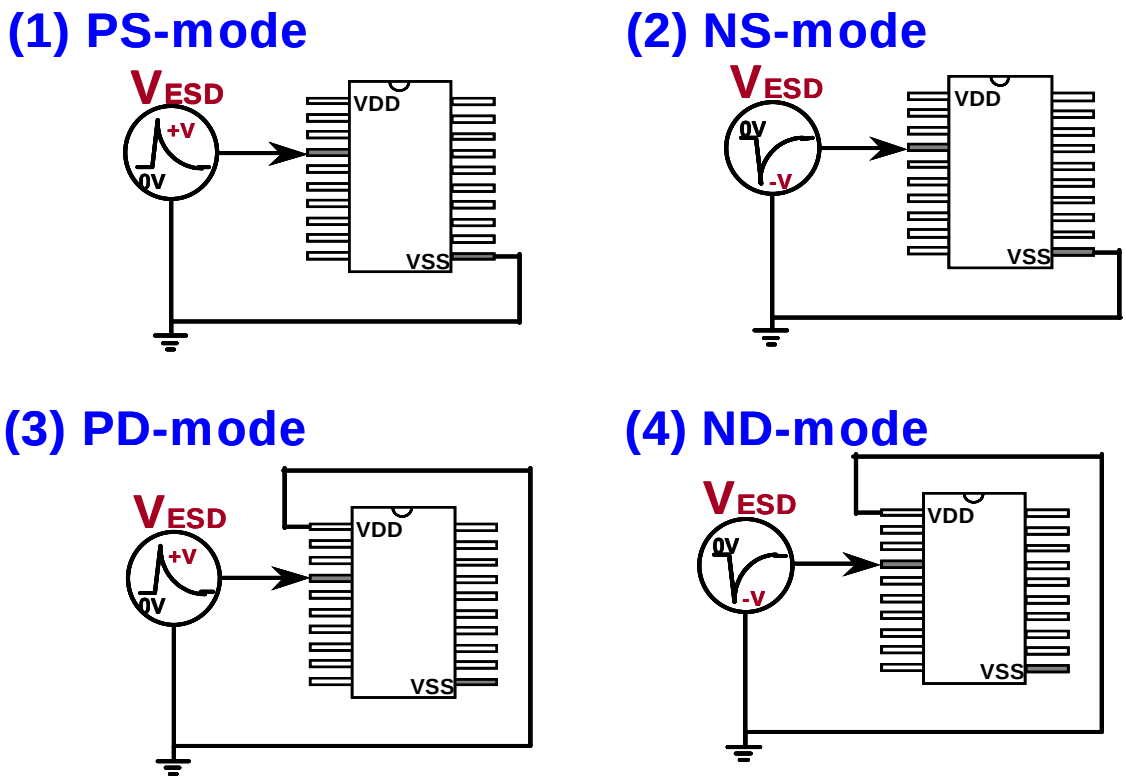


Fig. 3.4 Positive and negative ESD-stress on an input or output pin of an IC with respect to the ground VDD or VSS.

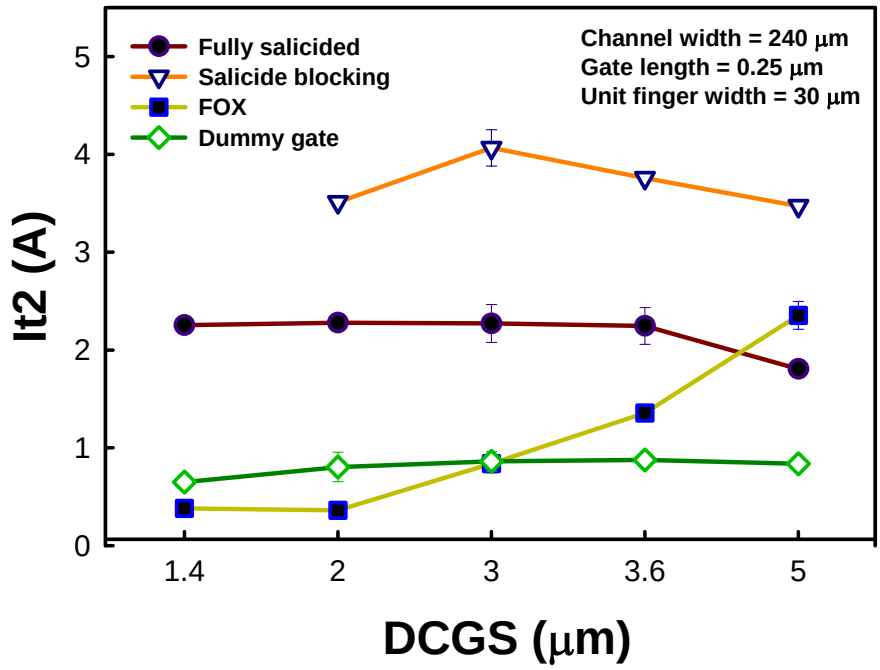


Fig. 3.5 The TLP measured It2 currents of GGNMOS transistors with varied DCGS in 0.25 μm salicided CMOS process.

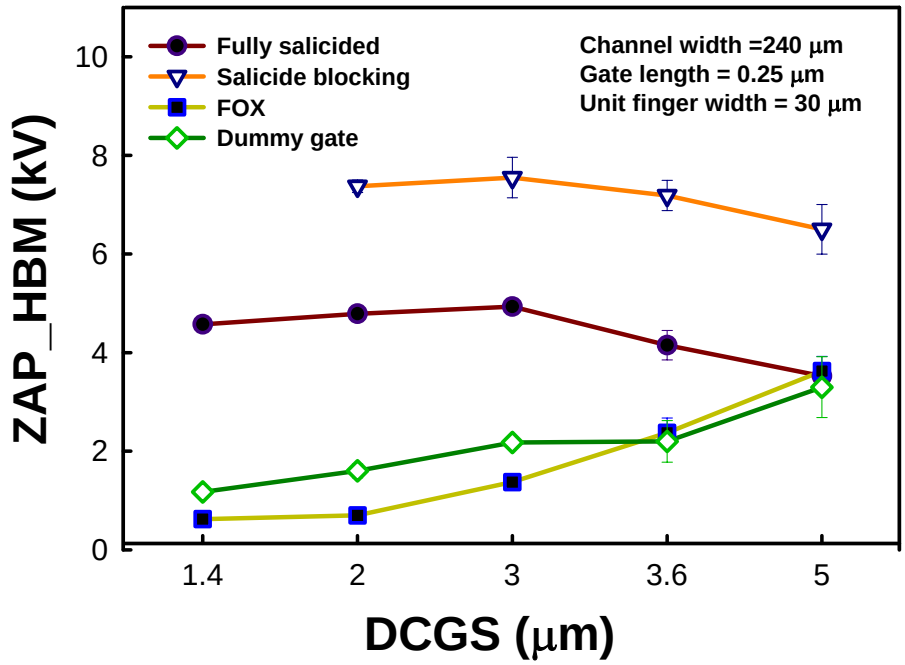


Fig. 3.6 The measured HBM ESD levels of GGNMOS transistors with varied DCGS in 0.25 μm salicided CMOS process.

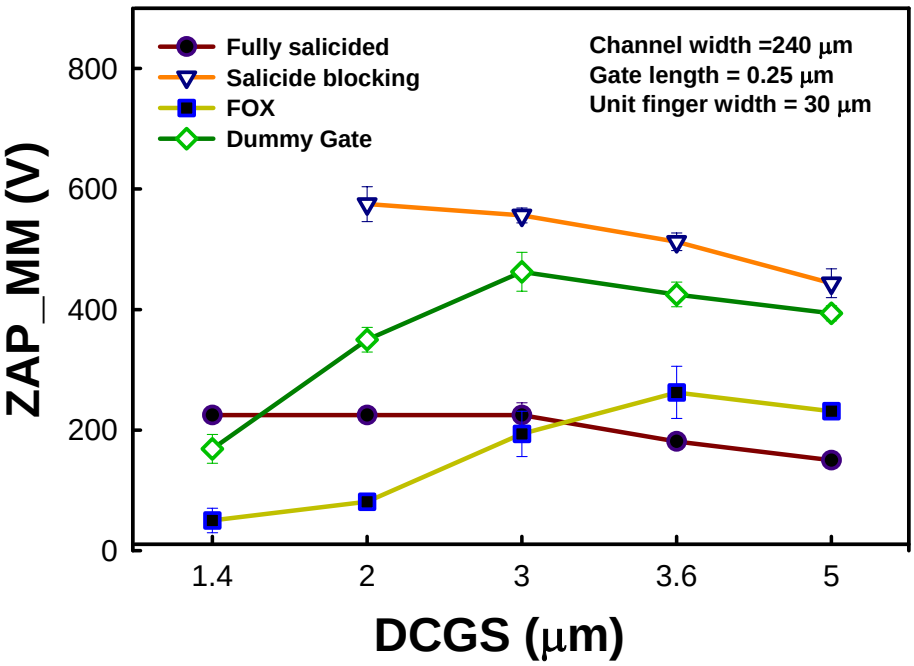


Fig. 3.7 The measured HBM ESD levels of GGNMOS transistors with varied DCGS in 0.25 μm salicided CMOS process.

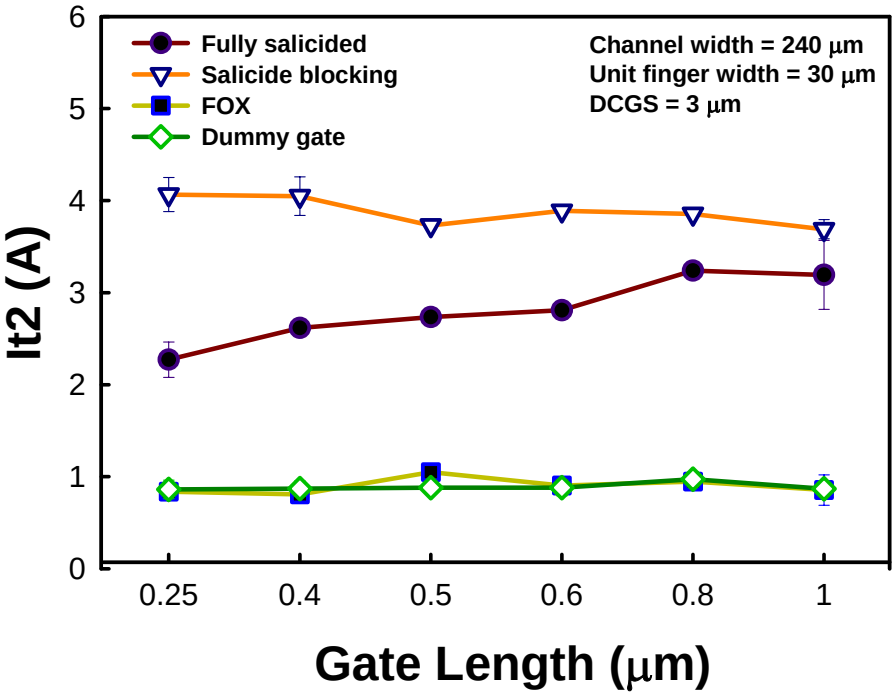


Fig. 3.8 The TLP measured It2 currents of GGNMOS transistors with varied gate length in 0.25 μm salicided CMOS process.

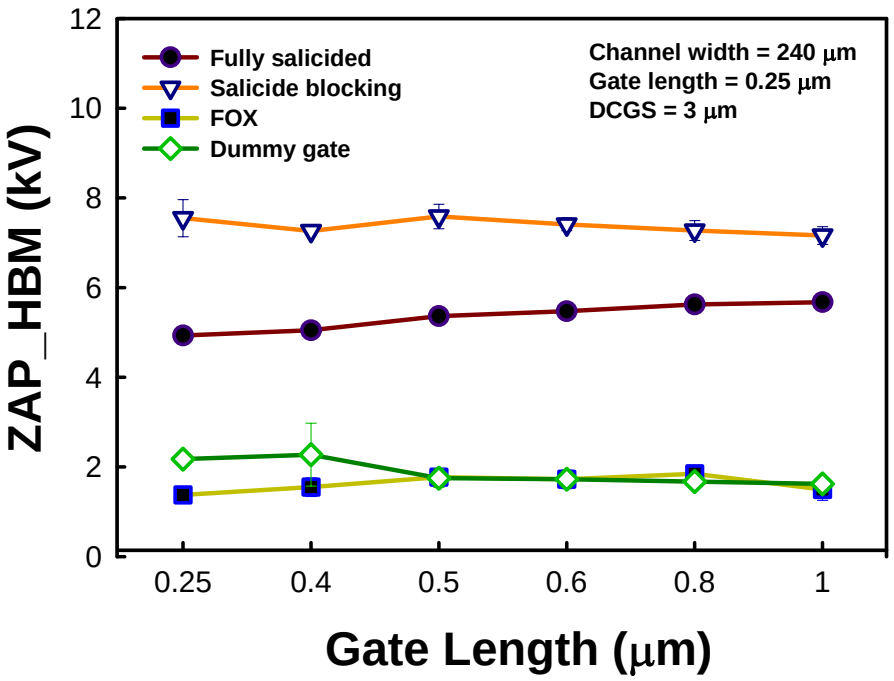


Fig. 3.9 The measured HBM ESD levels of GGNMOS transistors with varied gate length in 0.25 μm salicided CMOS process.

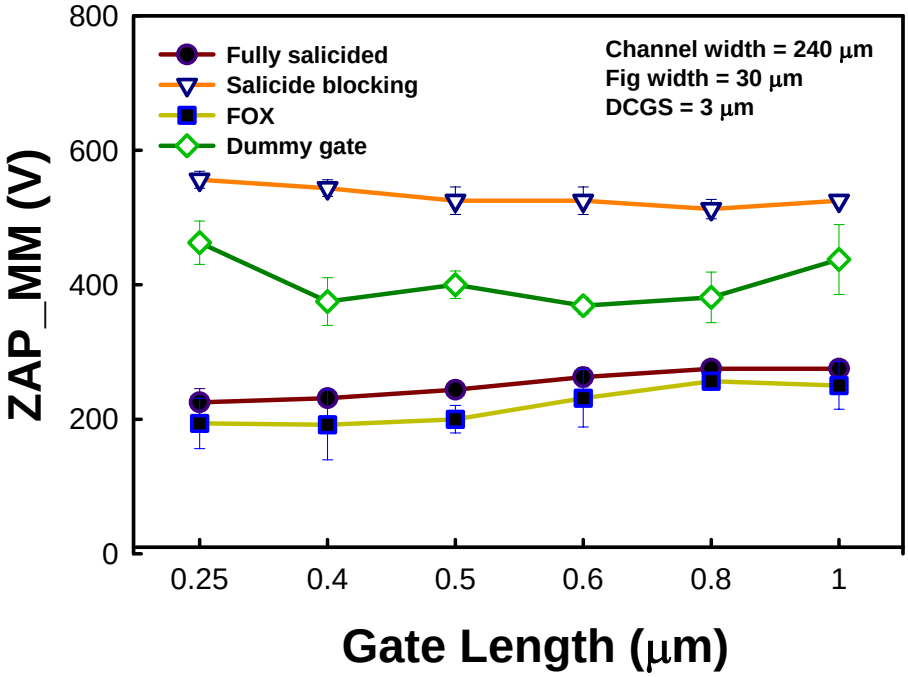


Fig. 3.10 The measured MM ESD levels of GGNMOS transistor with varied gate length in 0.25 μm salicided CMOS process.

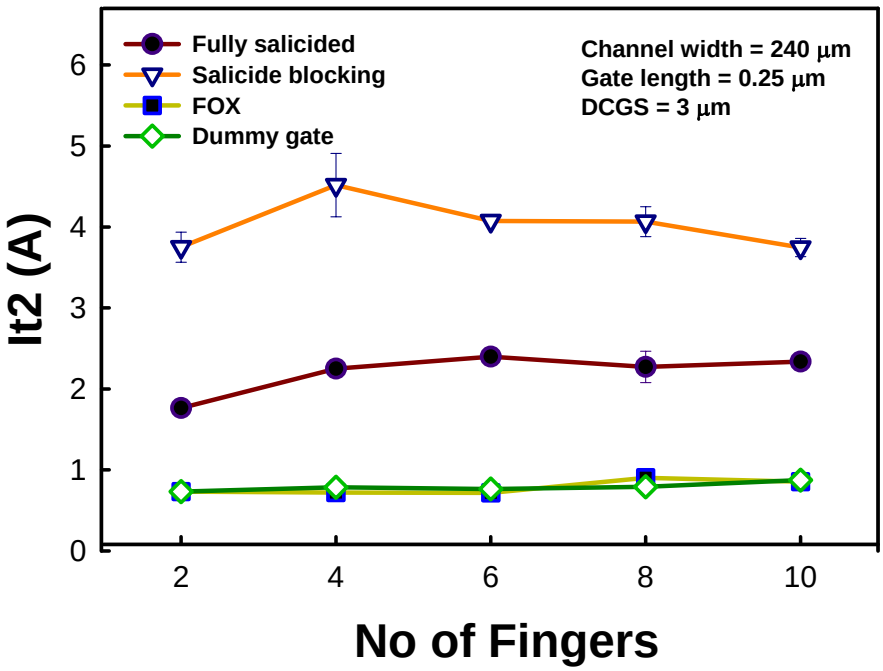


Fig. 3.11 The TLP measured It2 currents of GGNMOS transistors with varied fingers number in 0.25 μm salicided CMOS process.

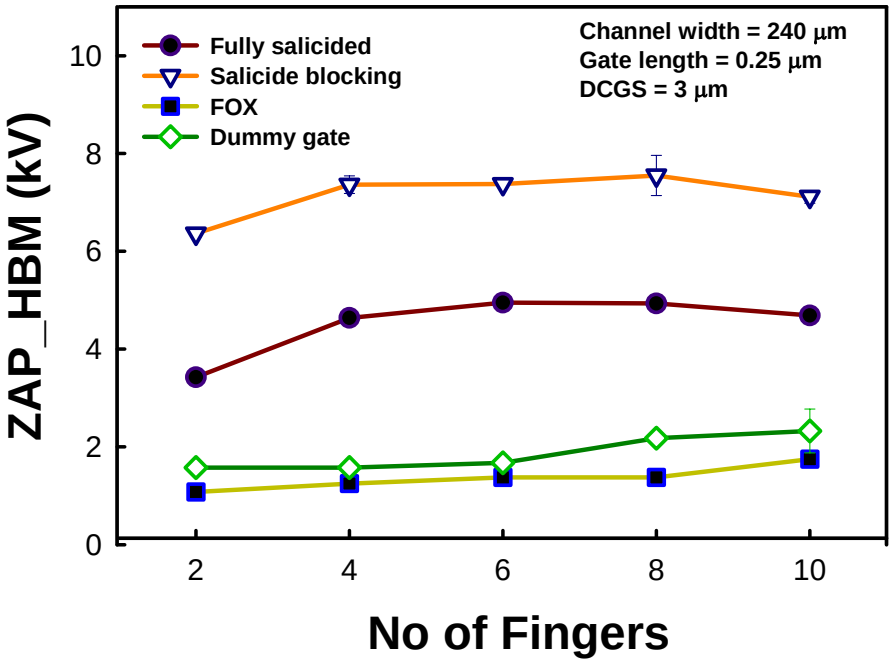


Fig. 3.12 The measured HBM ESD levels of GGNMOS transistors with varied fingers number in 0.25 μm salicided CMOS process.

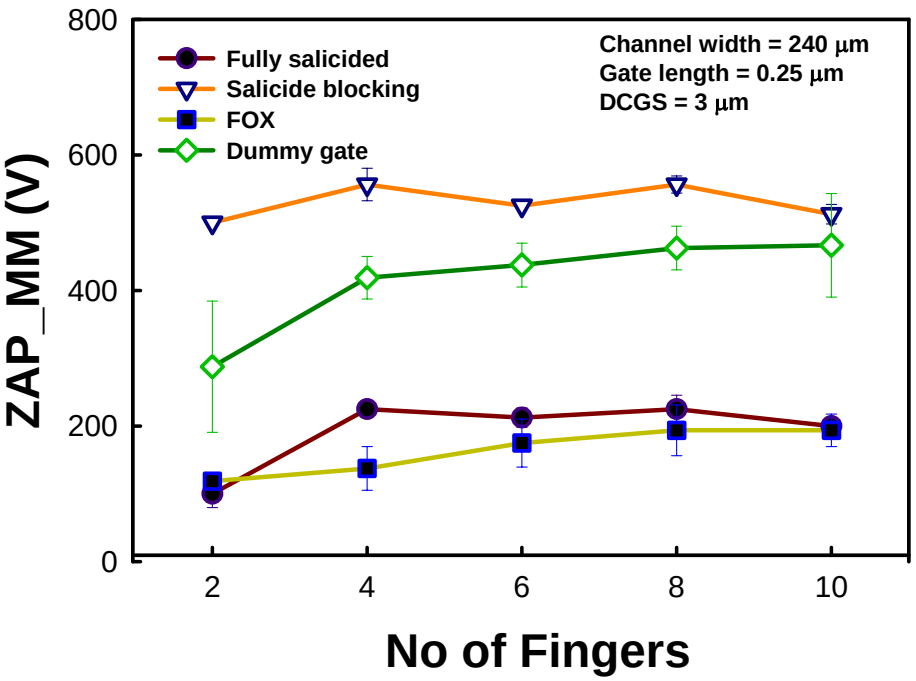


Fig. 3.13 The measured HBM ESD levels of GGNMOS transistors with varied fingers number in 0.25 μm salicided CMOS process.

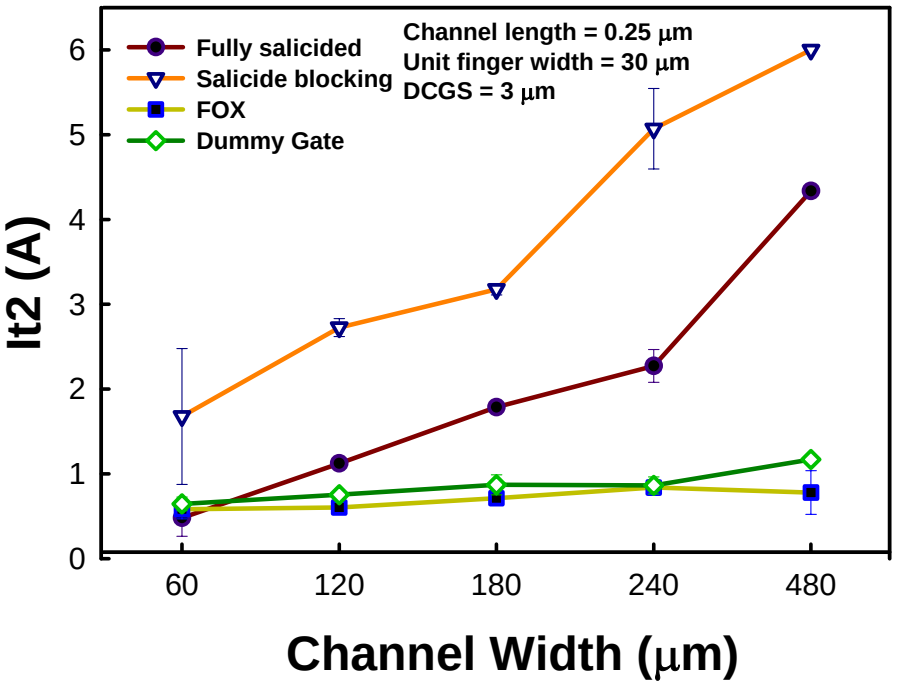


Fig. 3.14 The TLP measured It2 currents of GGNMOS transistors with varied channel width in 0.25 μm salicided CMOS process.

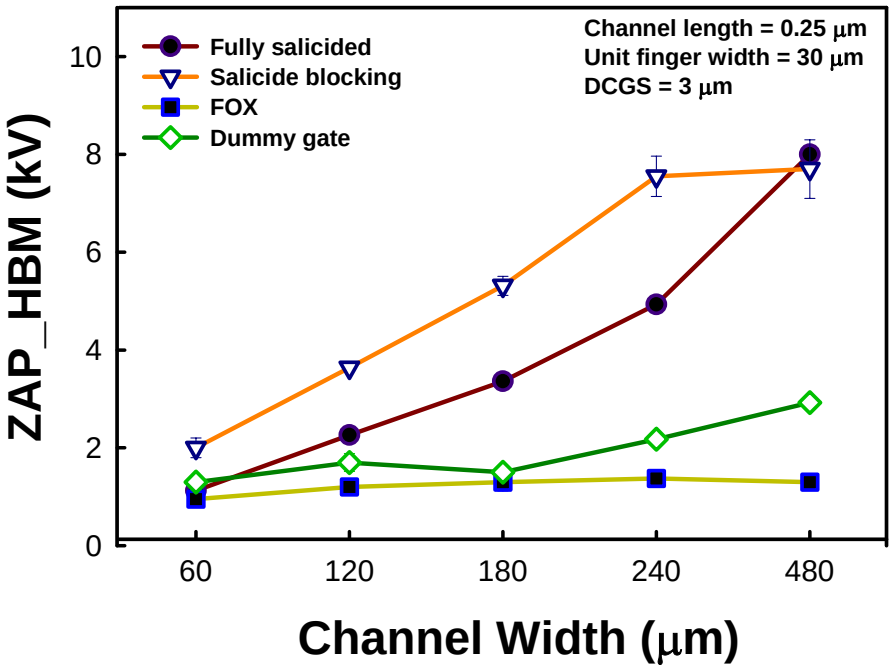


Fig. 3.15 The measured HBM ESD levels of GGNMOS transistors with varied channel width in 0.25 μm salicided CMOS process.

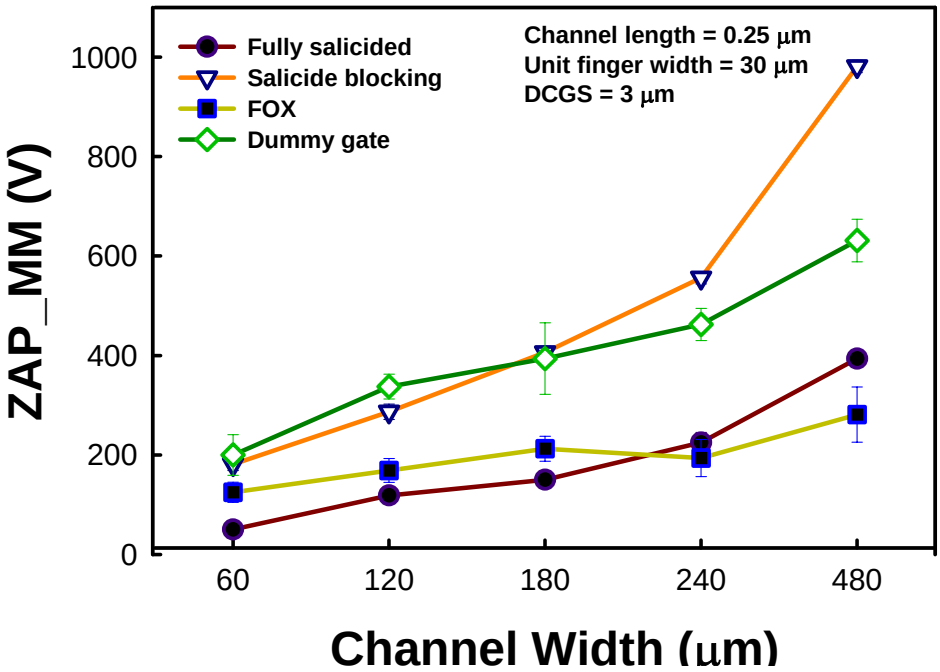


Fig. 3.16 The measured MM ESD levels of GGNMOS transistors with varied channel width in 0.25 μm salicided CMOS process.

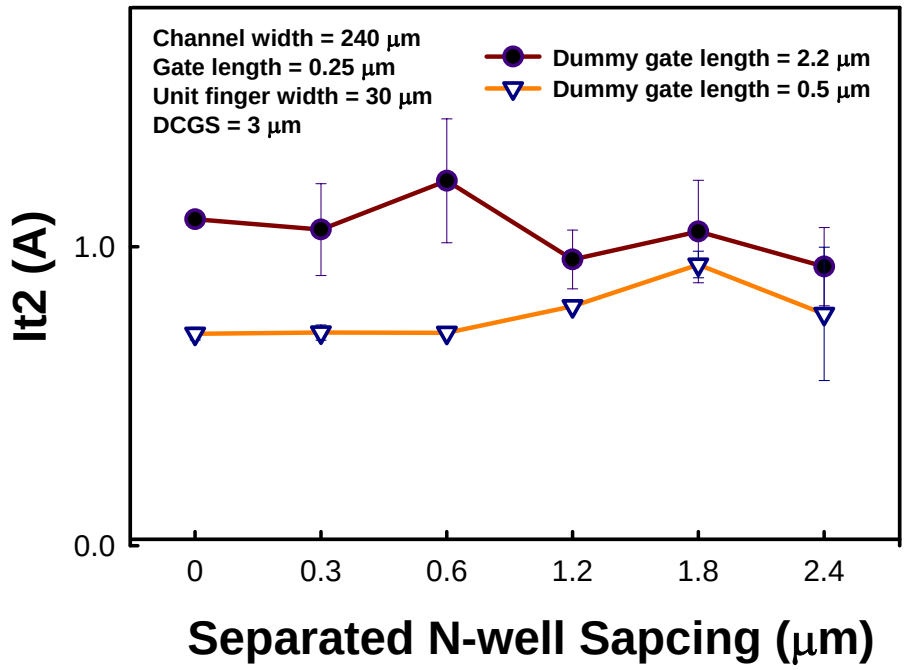


Fig. 3.17 The TLP measured It2 currents of dummy-gate structure GGNMOS transistors with varied separated N-well to N-well spacing in 0.25 μm salicided CMOS process.

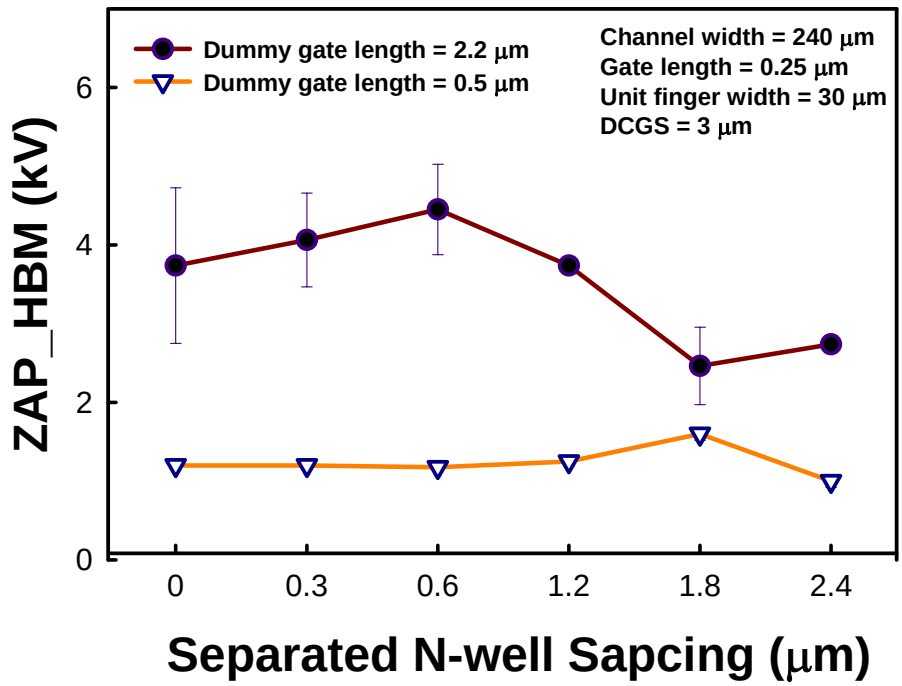


Fig. 3.18 The measured HBM ESD levels of dummy-gate structure GGNMOS transistors with varied separated N-well to N-well spacing in 0.25 μm salicided CMOS process.

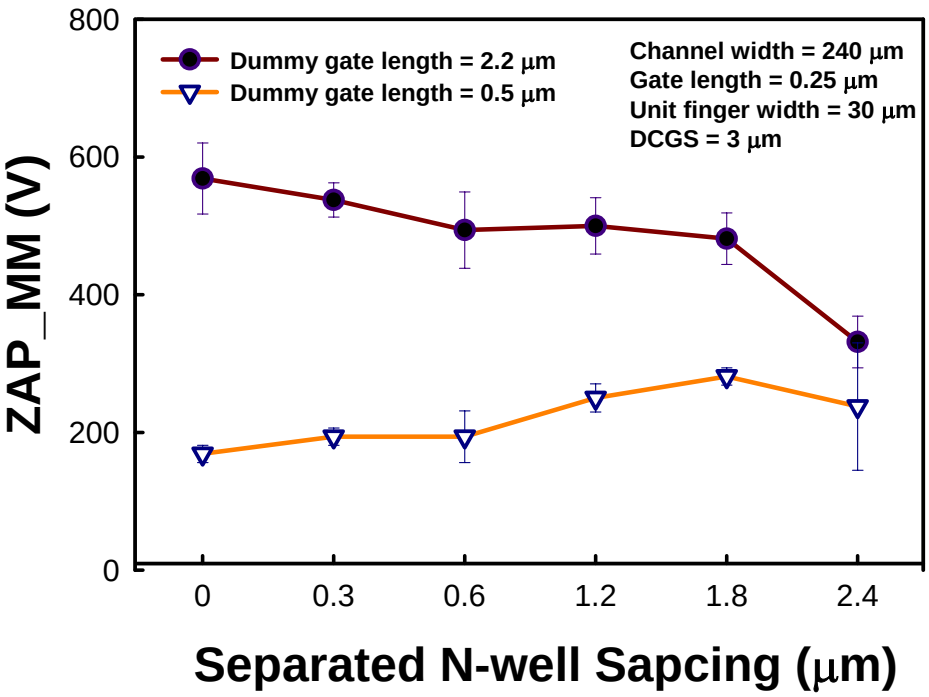


Fig. 3.19 The measured MM ESD levels of dummy-gate structure GGNMOS transistors with varied separated N-well to N-well spacing in 0.25 μm salicided CMOS process.

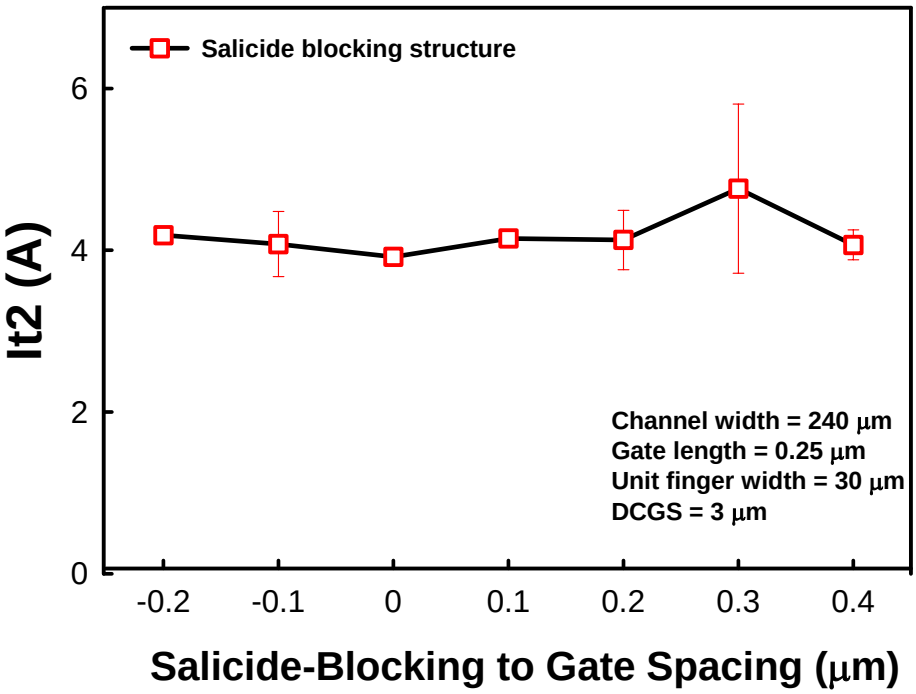


Fig. 3.20 The TLP measured It2 currents of salicide-blocking GGNMOS transistors with varied salicide-blocking region to gate spacing in 0.25 μm salicided CMOS process.

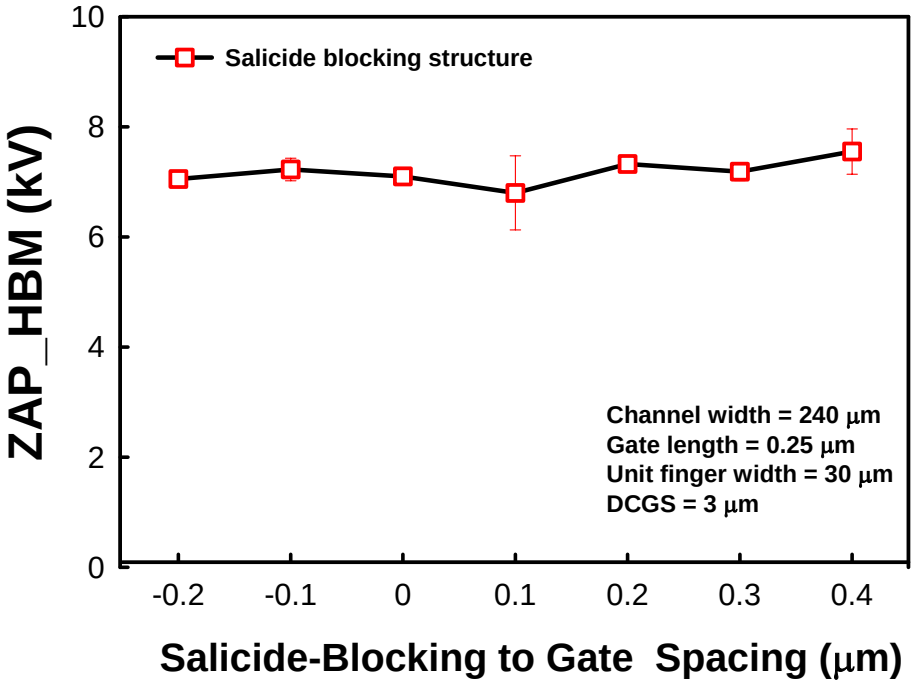


Fig. 3.21 The measured HBM ESD levels of salicide-blocking GGNMOS transistors with varied salicide-blocking region to gate spacing in 0.25 μm salicided CMOS process.

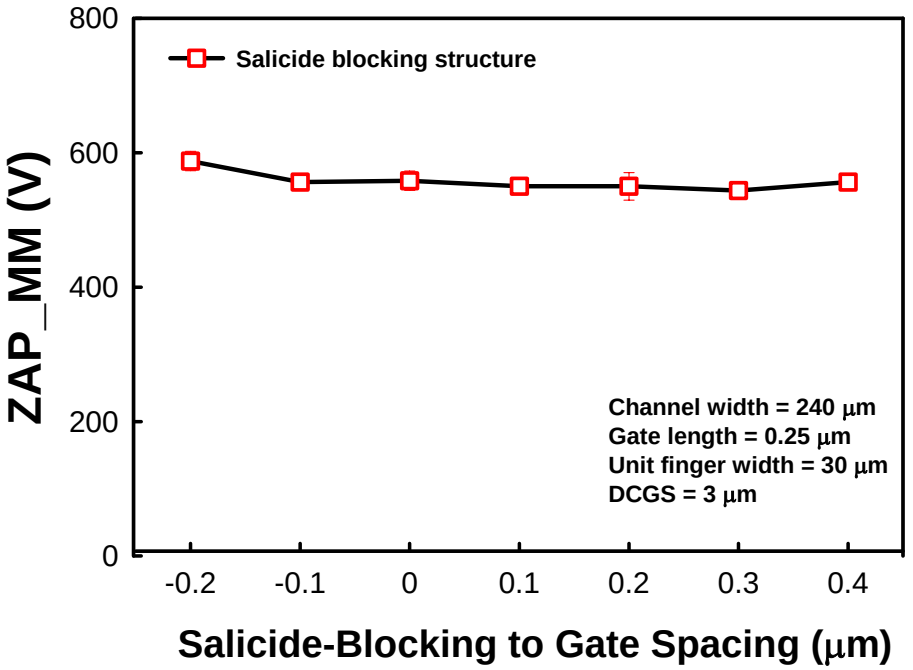


Fig. 3.22 The measured MM ESD levels of salicide-blocking GGNMOS transistors with varied salicide-blocking region to gate spacing in 0.25 μm salicided CMOS process.

CHAPTER 4

Failure Analysis

Based on the HBM and MM ESD robustness experimental results mentioned in chap 3, some results are analyzed and concluded but some results are not clear. In order to clarify the failure current paths and failure locations for reasonable explanation, we do some further failure analysis of these zapped ICs.

4.1 Failure Analysis Procedure

Once all experimental devices have been tested, the devices failing the electrical testing acceptance criteria were submitted for failure analysis. So the failed packages are decapitated, and then top layers including BPSG, metal, poly, and oxidation layer are removed to substrate layer with chemical processes. The failure locations are verified using optical microscopy, and scanning electron microscopy (SEM).

4.2 HBM Results and Discussion

The SEM failure pictures of dummy-gate structure transistors with drain contact to dummy-gate spacing of S = 0.4 μm, and drain contact to dummy-gate spacing of S = 1 μm after HBM ESD zapping are shown in Fig. 4.1, and Fig. 4.2. The failure pattern of dummy-gate structure transistors with drain contact to dummy-gate space of S = 1 μm is uniform, but that of dummy-gate structure transistors with drain contact to dummy-gate space of S = 0.4 μm is relatively non-uniform. So, the failure mechanism is attributed by small drain contact to dummy-gate spacing, which is matched with the data in Chap 3.

The SEM failure pictures of dummy-gate structure transistors with dummy-gate

length of L = 0.5 μm under HBM ESD zapping is shown in Fig. 4.3. Compared to dummy-gate structure transistor with dummy-gate length of L = 2.2 μm, the failure pattern of dummy-gate structure transistor with dummy-gate length of L = 0.5 μm is non-uniform and crowed in spots. The HBM ESD robustness of dummy-gate structure transistor with dummy-gate length of 2.2 μm is 2.1 kV. However, the HBM robustness of dummy-gate structure transistor with dummy-gate length of 0.5 μm is 1.2 kV.

The SEM failure pictures of transistors with FOX structure, fully-salicided structure, and salicide blocking structure under HBM stress are shown in Fig. 4.4, Fig. 4.5, and Fig. 4.6. The failure locations of NMOS transistors with FOX structure and fully-salicided structure are non-uniform but failure locations of NMOS transistor with salicide-blocking structure is relatively uniform. So, that's the reason why the ESD robustness of GGNMOS with salicide-blocking structure is higher than that of conventional fully-salicided structure and FOX structure transistors.

4.3 MM Results and Discussion

The SEM failure pictures of dummy-gate structure transistors with drain contact to dummy-gate space of S = 0.4 μm and drain contact to dummy-gate space of S = 1 μm under MM ESD stress are shown in Fig. 4.7 and Fig. 4.8, respectively. The failure patterns of dummy-gate structure transistors with drain contact to dummy-gate space of S = 1 μm under MM ESD stress is slightly more uniform than that with drain contact to dummy-gate space of S = 0.4 μm. So, MM ESD robustness levels of dummy-gate structure transistors with drain contact to dummy-gate spacing of S = 1 μm and transistors with drain contact to dummy-gate spacing of S = 0.4 μm are 500 V, 575 V, respectively.

The SEM pictures of dummy-gate structure transistors with dummy-gate length of L = 0.5 μm under MM ESD stress is shown in Fig. 4.9. The failure patterns on

SEM pictures of transistor with dummy-gate length of L = 0.5 μm is non-uniform and crowed in spots. The MM ESD robustness of dummy-gate structure transistor with dummy-gate length of 2.2 μm is 575 V. However, the MM ESD robustness of dummy-gate structure transistor with dummy-gate length of 0.5 μm is 175 V.

The SEM failure pictures of transistors with FOX structure, fully-salicided structure and salicide blocking structure under MM ESD stress are shown in Fig. 4.10, Fig. 4.11, and Fig. 4.12, respectively. The failure patterns of NMOS transistors with FOX structure and fully-salicided structure are non-uniform, and failure pattern of NMOS transistor with salicide-blocking structure is relatively uniform. So, that's why the ESD robustness of GGNMOS with salicide-blocking structure is higher than that of conventional fully-salicided structure and FOX structure transistors.

Comparing SEM failure pictures of dummy-gate structure and FOX structure transistors under MM ESD stress with those under HBM ESD stress shown in Fig. 4.2 ~ Fig. 4.12, the failure locations of transistors under MM ESD stress are more uniform than that of transistors under HBM stress. Relatively, failure locations of transistors with fully-salicided and salicide-blocking structures under MM ESD stress are similar with that of transistors under HBM stress. So, That's why MM ESD robustness of transistors with dummy-gate and FOX structures have better performance compared with that using fully-salicided structure. But HBM ESD robustness of transistors with dummy-gate and FOX structures are lower than that of transistor with fully-salicided structure. Summary of SEM failure locations of different structure of GGNMOS transistors are shown in Table 4.1.

4.4 Discussion

The SEM failure pictures of transistors with salicide-blocking structure, and fully-salicided structure under MM and HBM ESD stress show that the current paths

of transistors with fully-salicided structure are underneath the channel. Because the failure patterns of transistors with salicide blocking are crowed in top and bottom sides of fingers, failures of transistor with salicide blocking structures are caused by N+ to P-sub current path stress.

Failure patterns of devices with dummy-gate and FOX structures under MM ESD stress are relatively uniform compared with those of devices under HBM ESD stress. Fig. 4.13, and Fig. 4.14 show the waveforms of fully-salicided structure transistor and dummy-gate structure transistor under 1.1 kV HBM ESD zapping, and the peak voltages are 12.4 V and 12.3 V, respectively. Because the transformation ratio of current probe is 5 mV-to-1 mA, the corresponding currents are 2.48 A, 2.46 A, respectively. Because the resistance of HBM equivalent circuit is 1.5 kV, the turn-on resistances of all types of devices are much smaller than total resistance. So the ESD currents of different types of devices are almost the same. However, the turn-on resistance of transistors with dummy-gate and FOX structures are greater than that of fully-salicided structure transistor and salicide-blocking structure transistor. The power dissipations of those devices are proportional to turn-on resistance. That's why HBM ESD robustness of devices with dummy-gate and FOX structures are smaller than those with fully-salicided structure and silicide-blocking structure.

Fig. 4.15, and Fig. 4.16 show the discharge waveforms of fully-salicided structure transistor and dummy-gate structure transistor under 130 V MM ESD zapping. The peak voltages of fully-salicided structure transistor and dummy-gate structure transistor are 14 V and 11 V, respectively. Because the transformation ratio of current probe is 5 mV-to-1 mA, the corresponding currents are 2.8 A, 2.2 A, respectively. Because resistance of MM equivalent circuit is 0, the turn-on resistances of all types of devices are much greater than that of wires. So the ESD currents of different types devices are inverse proportional to their own turn-on resistances. The

stress voltages across devices are almost constant due to the smaller wire resistance of system. So, the power dissipation of device decreases with increasing resistance. That's why MM ESD robustness of devices with dummy-gate structure is greater than that with fully-salicided structure.

4.5 Conclusion

Failure patterns of MM ESD zapped devices with dummy-gate and FOX structure are relatively uniform compared with those of HBM ESD zapped devices. Failure pattern of devices with drain contact to dummy-gate spacing of S = 1 μm is relatively uniform comparing with those with drain contact to dummy-gate space of S = 0.4 μm. On the whole, the SEM failure pictures of ESD zapped devices are coincided with TLP, HBM and MM measured results.

Table 4.1. Summary of SEM failure locations of different structures of NMOS transistors under HBM and MM ESD zapping**.**

	HBM PS-mode	MM PS-mode
Failure locations of GGNMOS with dummy-gate structure after ESD stress (W/L = 240 μm/0.25 μm, drain contact to dummy-gate spacing = 0.4 μm, and dummy gate length = 2.2 μm)	HBM ESD robustness is 2.1 kV, Failure locations are top and bottom of drain sides.	MM ESD robustness is 500 V, failure locations are uniform in drain sides of fingers.
Failure locations of GGNMOS with dummy-gate structure after ESD stress (W/L = 240 μm/0.25 μm, drain contact to dummy-gate spacing = 1 μm, and dummy gate length = 2.2 μm)	HBM ESD robustness is 4 kV, failure locations are uniform in drain sides of fingers.	MM ESD robustness is 575 V, failure locations are uniform in drain sides of fingers.
Failure locations of GGNMOS with dummy-gate structure after ESD stress (W/L = 240 μm/0.25 μm, drain contact to dummy-gate spacing = 0.4 um, and dummy gate length = 0.5 μm)	HBM ESD robustness is 1.2 kV, failure locations are in gates and dummy gates.	MM ESD robustness is 175 V, failure locations are in gates and dummy gates.
Failure locations of GGNMOS with FOX structure after ESD stress (W/L = 240 μm/0.25 μm, drain contact to FOX spacing = 0.4 μm , FOX length = 2.2 μm)	HBM ESD robustness is 1.2 kV, failure locations are through gates.	MM ESD robustness is 175 kV, failure locations are located in some drain sides of fingers.
Failure locations of GGNMOS with fully-salicided structure after ESD stress (W/L = 240 μm/0.25 μm)	HBM ESD robustness is 5 kV, failure locations are uniform in drain and source sides of fingers.	MM ESD robustness is 225 V, failure locations are in gates.
Failure locations of GGNMOS with salicide blocking structure after ESD stress (W/L = 240 μm/0.25 μm, drain contact to salicide blocking = 0.4 μm and salicide blocking length = 2.2 μm)	HBM ESD robustness is 7.8 kV, Failure locations are top and bottom of drain sides.	MM ESD robustness is 550 V, failure locations are top and bottom of drain sides.

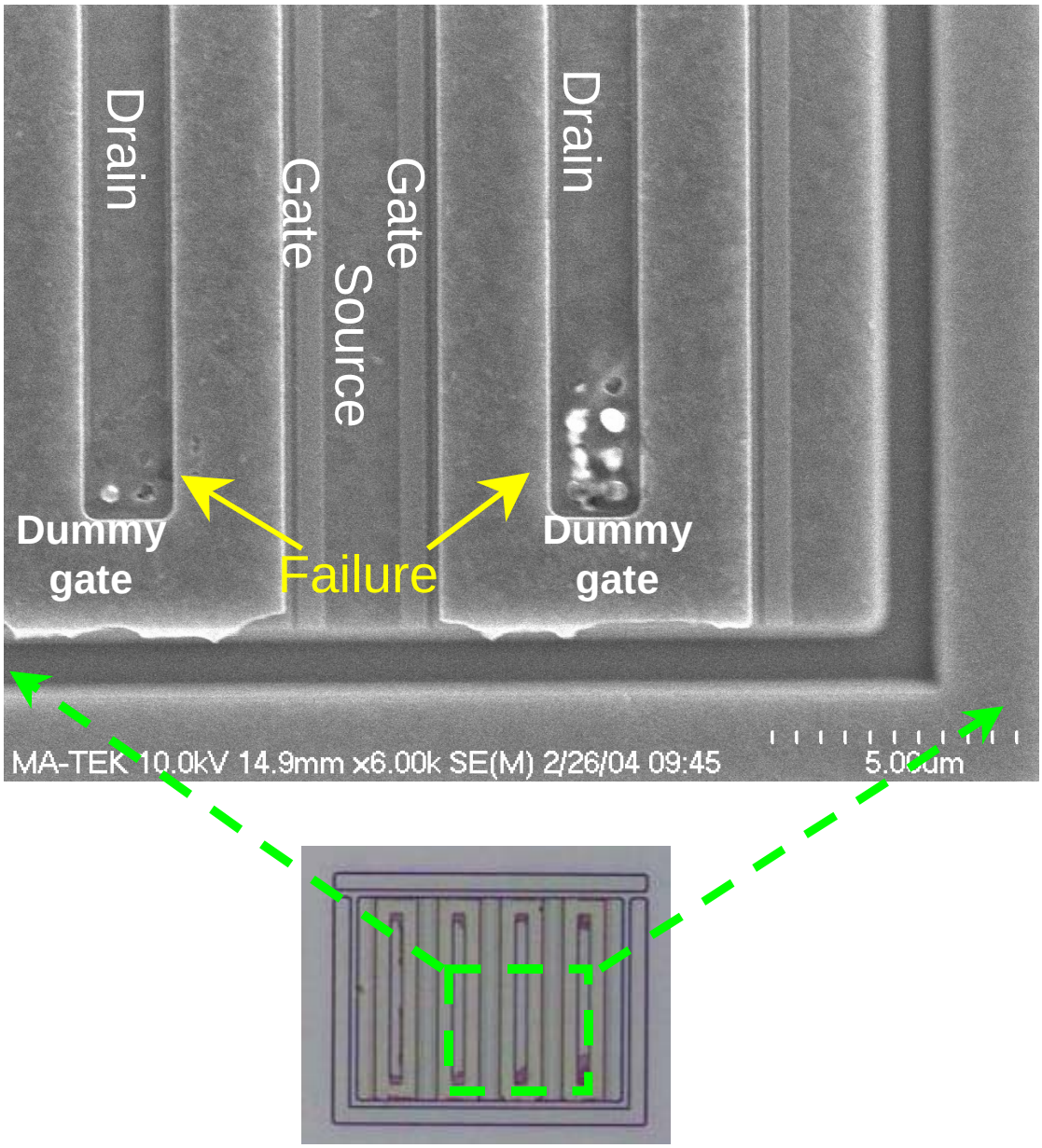


Fig. 4.1 SEM failure picture of dummy-gate structure NMOS transistor with drain contact to dummy-gate spacing of S = 0.4 μm under HBM ESD zapping. (HBM ESD robustness = 2.2 kV, W/L = 240 μm/0.25 μm, dummy-gate length = 2.2 μm)

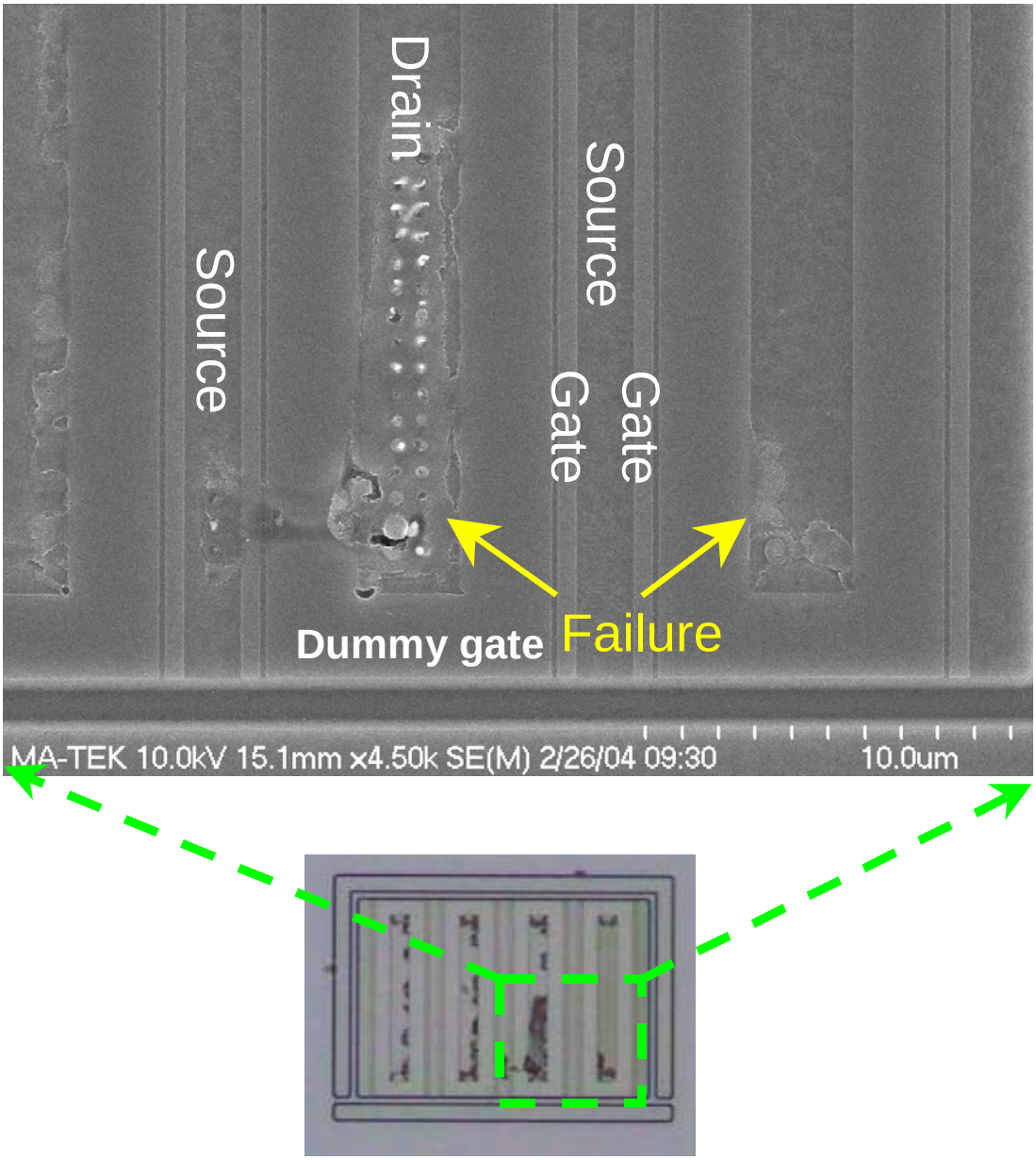


Fig. 4.2 SEM failure picture of dummy-gate structure NMOS transistor with drain contact to dummy-gate spacing of S = 1 μm under HBM ESD zapping. (HBM ESD robustness = 4 kV, W/L = 240 μm/0.25 μm, dummy-gate length = 2.2 μm)

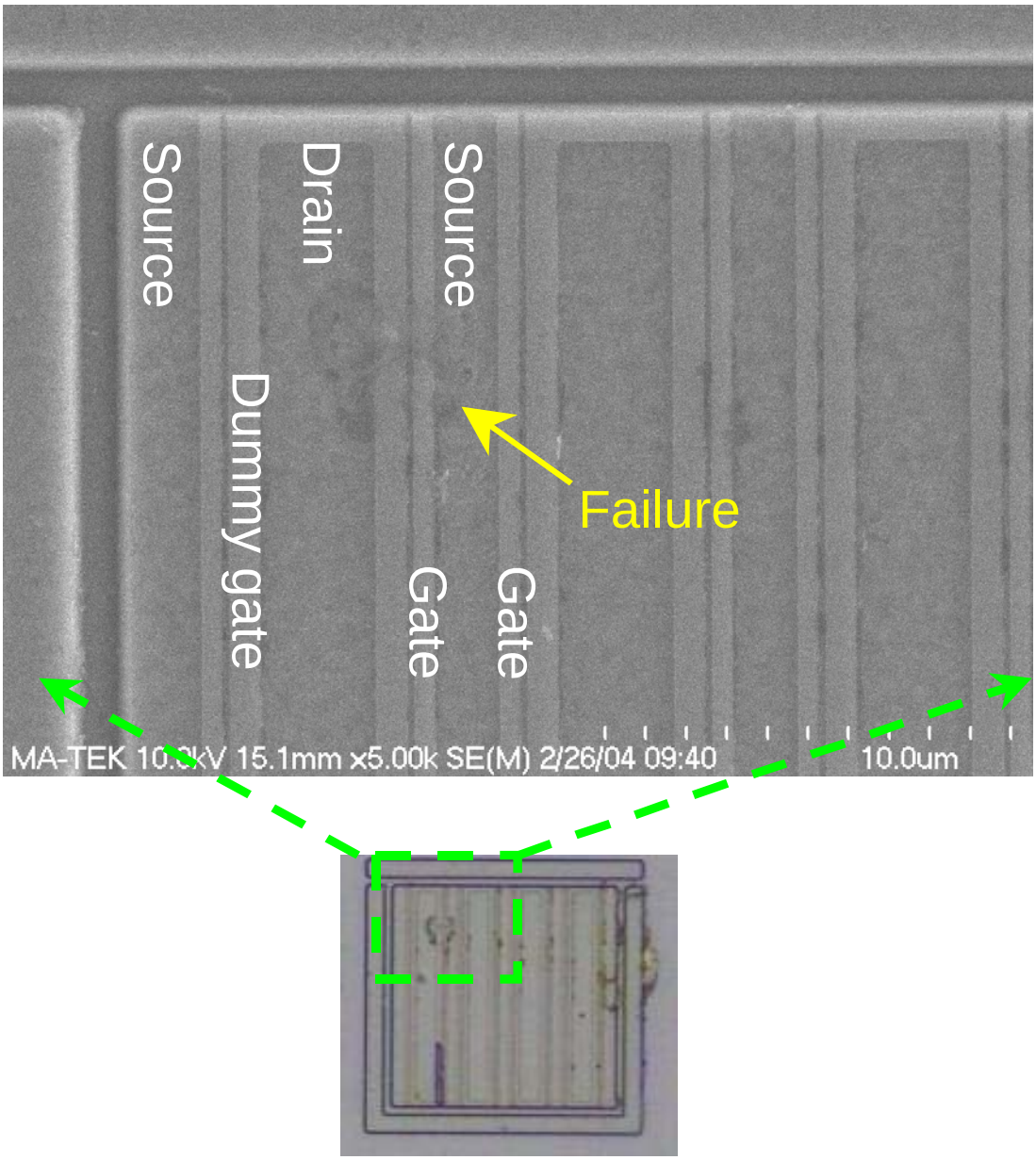


Fig. 4.3 SEM failure picture of dummy-gate structure NMOS transistor under HBM ESD zapping. (HBM ESD robustness = 1.2 kV, W/L = 240 μm/0.25 μm, dummy-gate length = 0.5 μm)

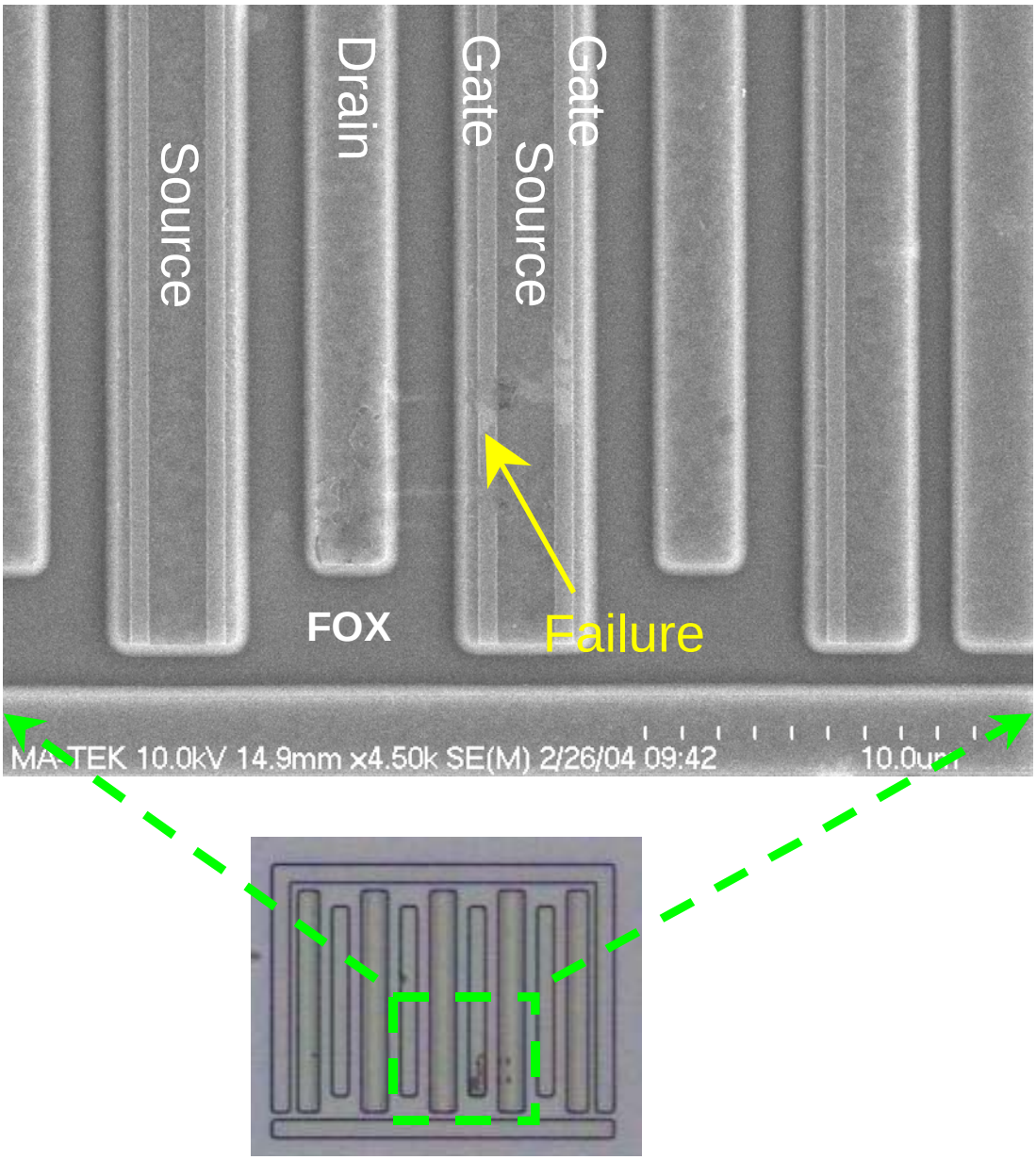


Fig. 4.4 SEM failure picture of FOX structure NMOS transistor under HBM ESD zapping. (HBM ESD robustness = 1.2 kV, W/L = 240 μm/0.25 μm)

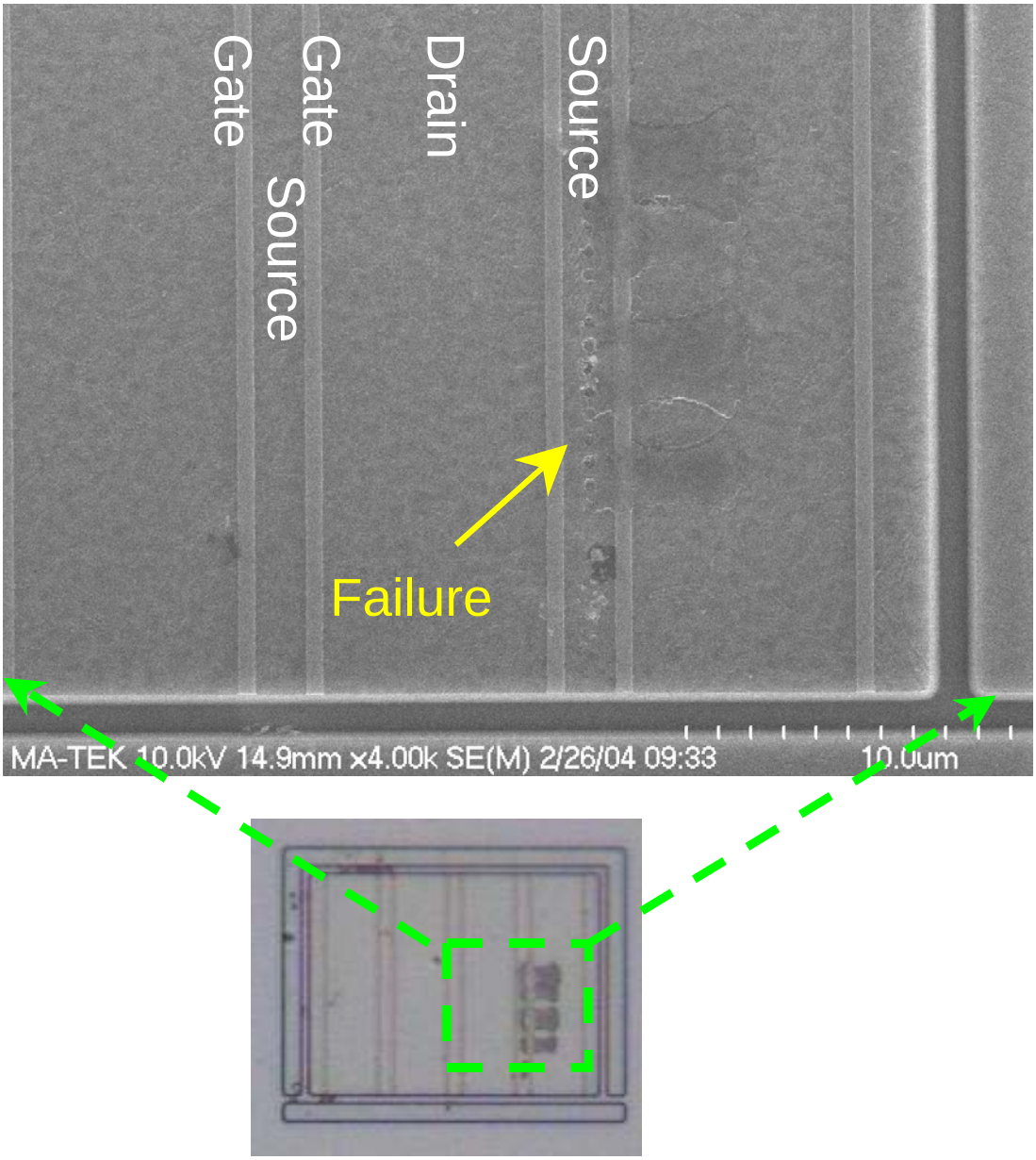


Fig. 4.5 SEM failure picture of fully-salicided structure NMOS transistor under HBM ESD zapping. (HBM ESD robustness = 5 kV, W/L = 240 μm/0.25 μm)

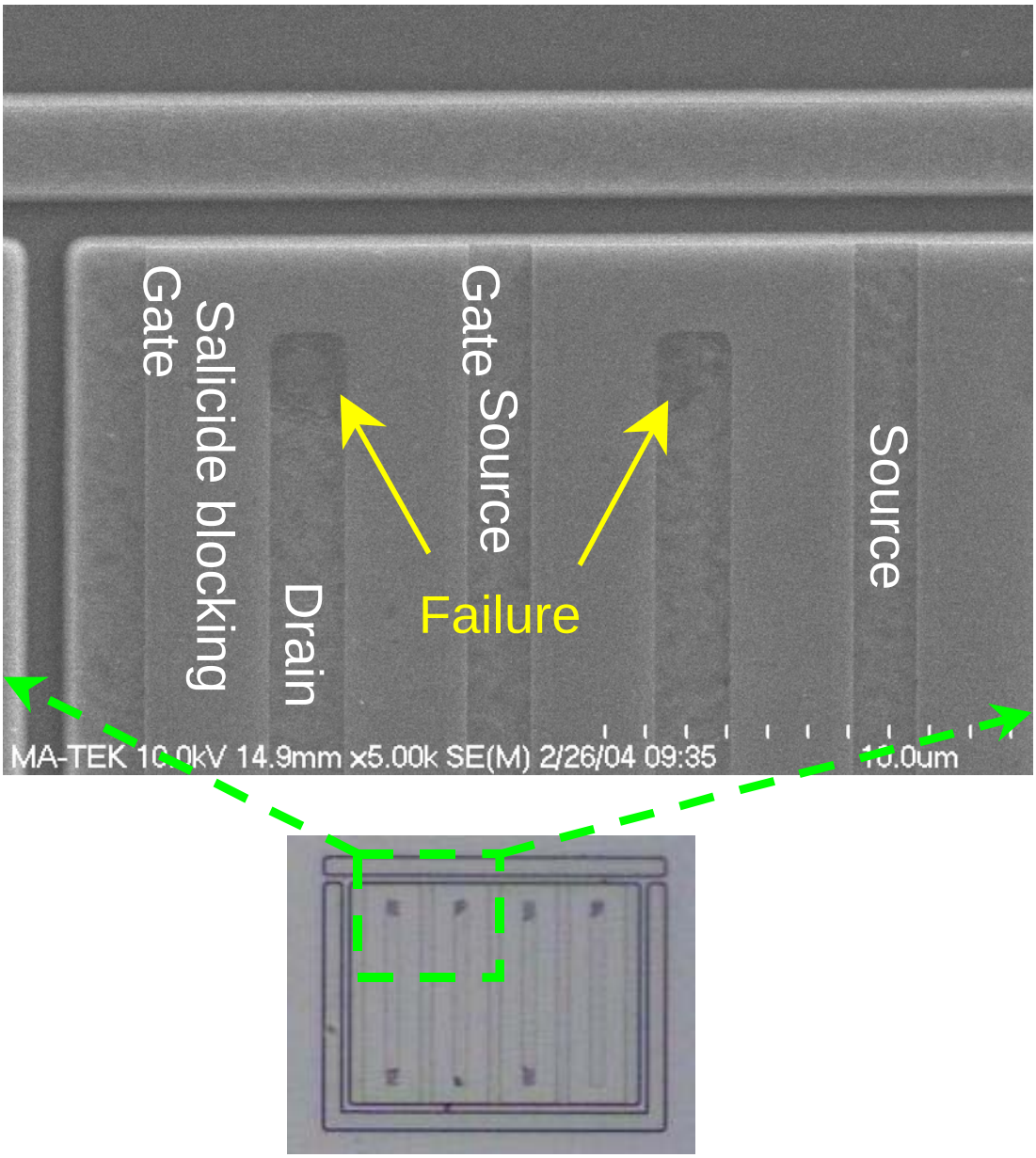


Fig. 4.6 SEM failure picture of salicide-blocking structure NMOS transistor under HBM ESD zapping. (HBM ESD robustness = 7.8 kV, W/L = 240 μm/0.25 μm)

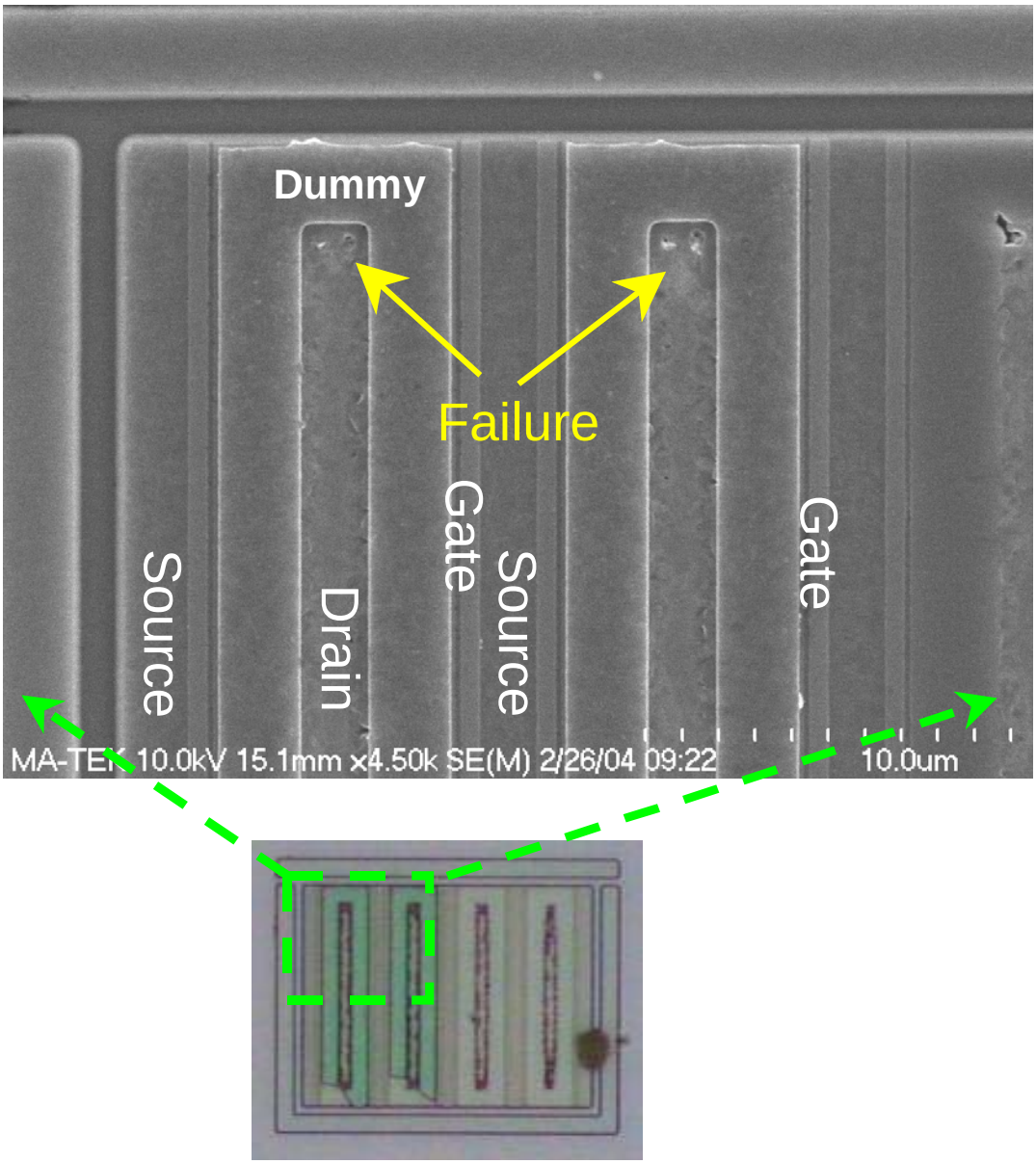


Fig. 4.7 SEM failure picture of dummy-gate transistor with drain contact to salicide block spacing of S = 0.4 μm under MM ESD zapping. (MM ESD robustness = 500 V, W/L = 240 μm/0.25 μm, dummy-gate length = 2.2 μm)

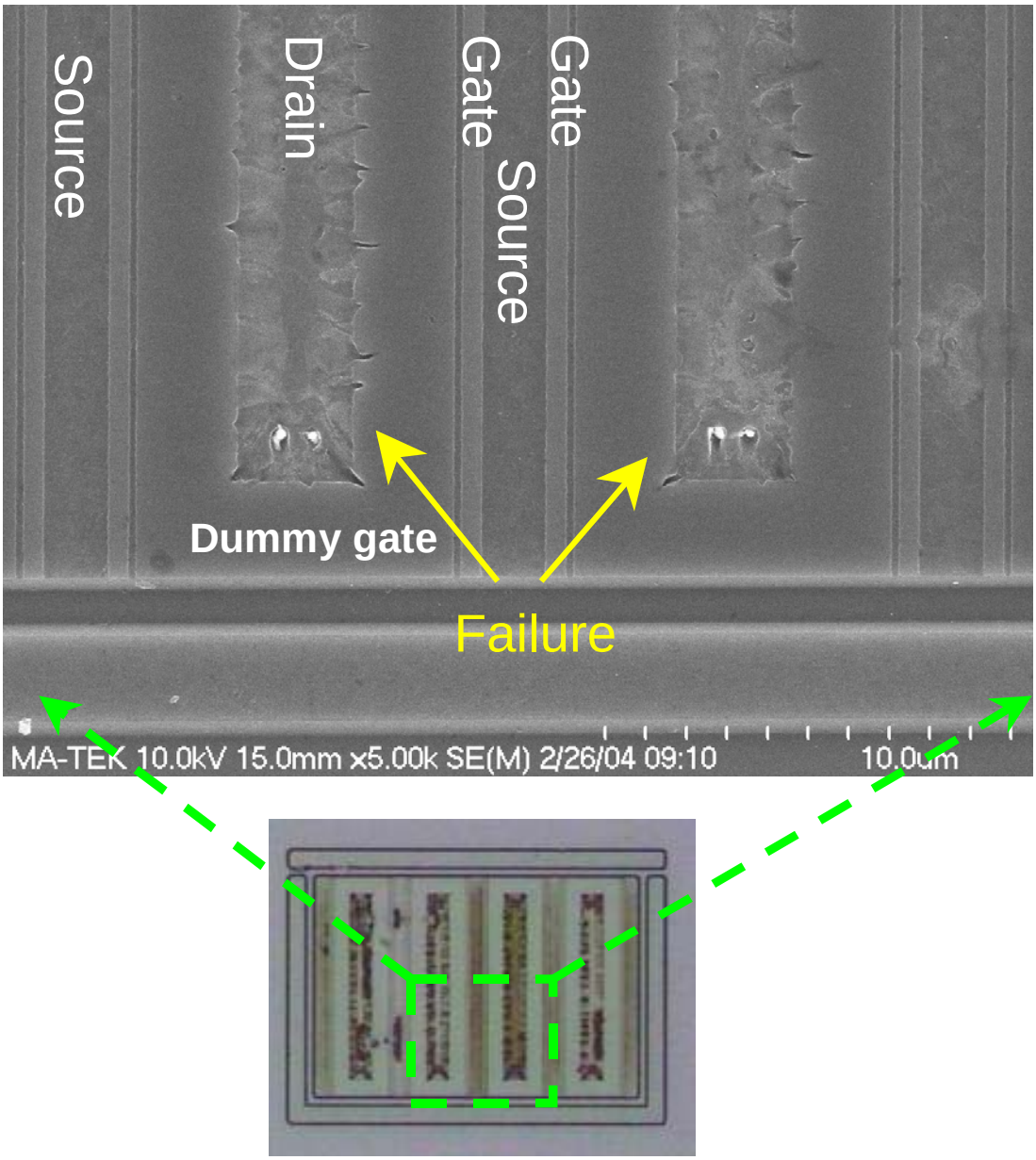


Fig. 4.8 SEM failure picture of dummy-gate transistor with drain contact to dummy-gate spacing of S = 1 μm under MM ESD zapping. (MM ESD robustness = 575V, W/L = 240 μm/0.25 μm, dummy-gate length = 2.2 μm)

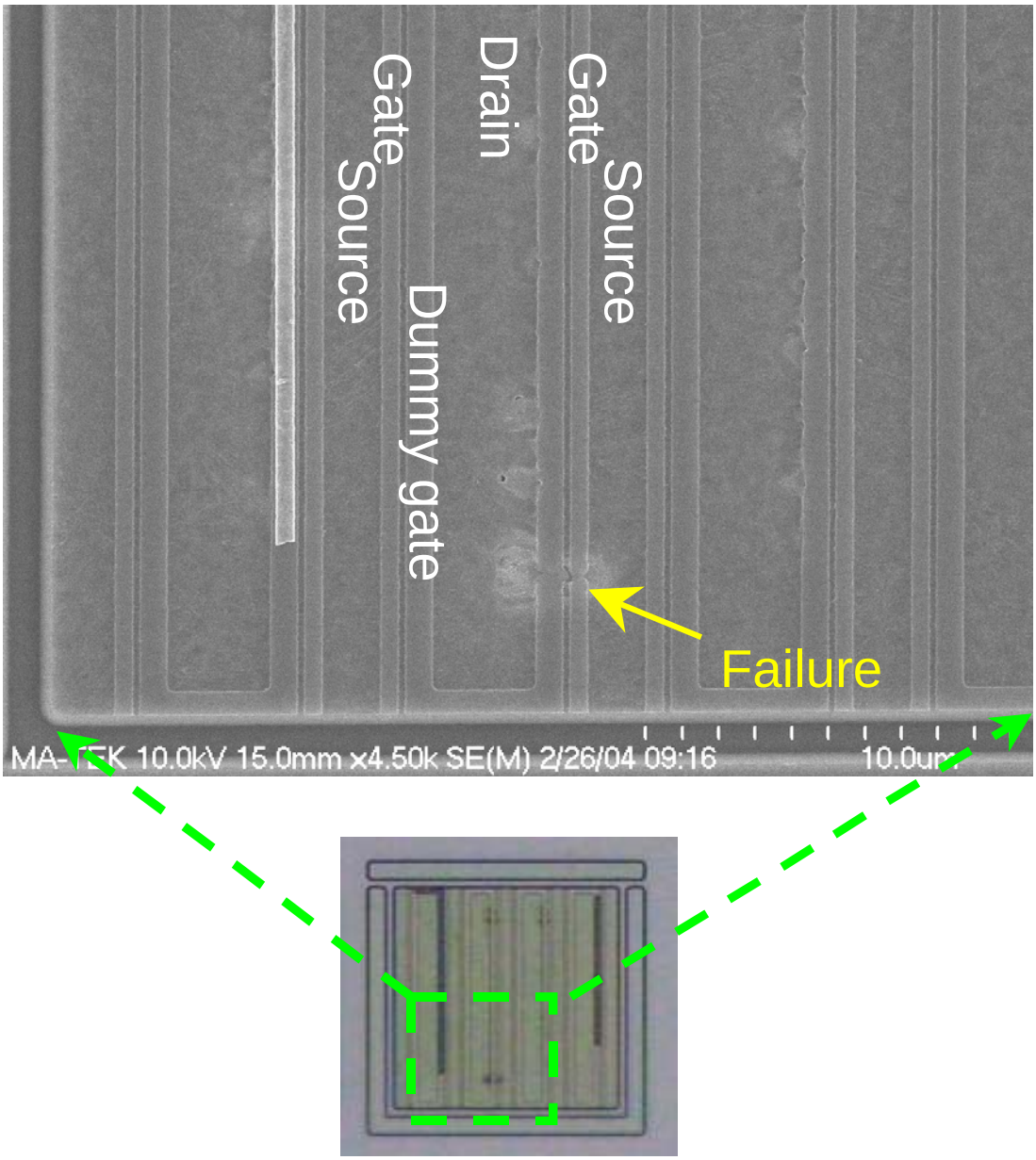


Fig. 4.9 SEM failure picture of dummy gate structure transistor under MM ESD zapping. (MM ESD robustness = 175 V, W/L = 240 μm/0.25 μm, dummy-gate length = 0.5 μm)

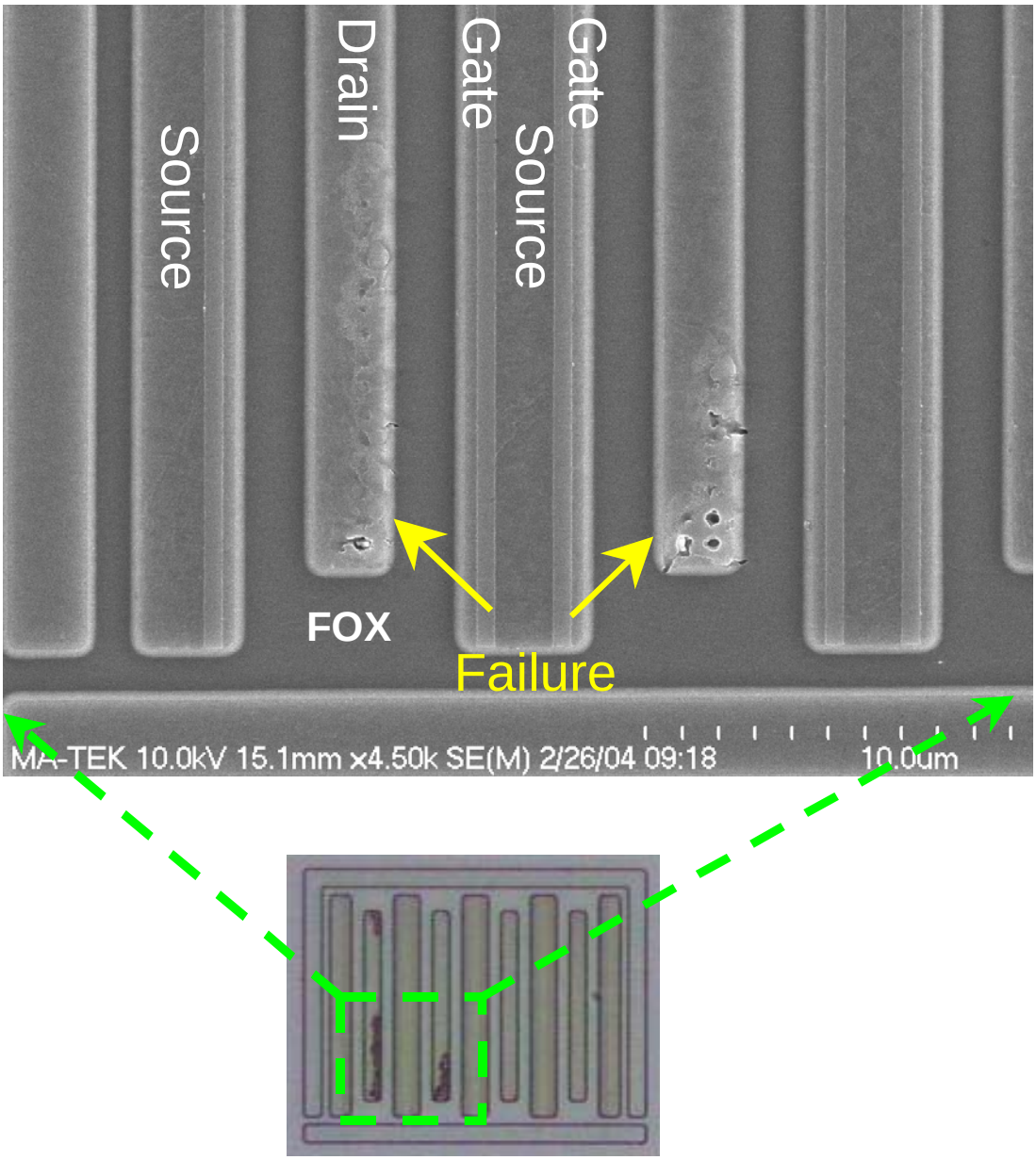


Fig. 4.10 SEM failure picture of FOX structure NMOS transistor under MM ESD zapping. (MM ESD robustness = 175 V, W/L = 240 μm/0.25 μm)

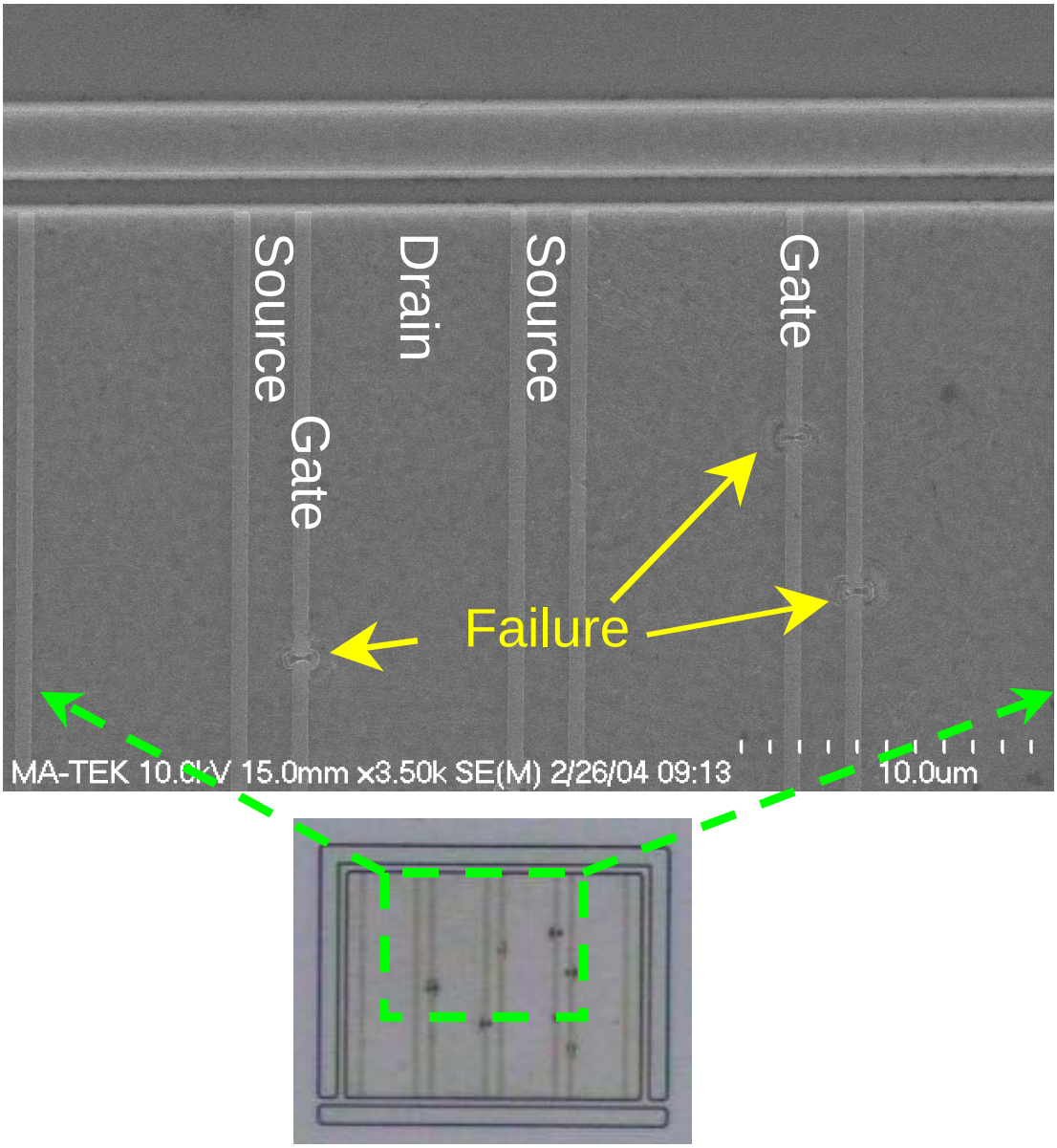


Fig. 4.11 SEM failure picture of fully-salicided structure NMOS transistor under MM ESD zapping. (MM ESD robustness = 225 V, W/L = 240 μm/0.25 μm)

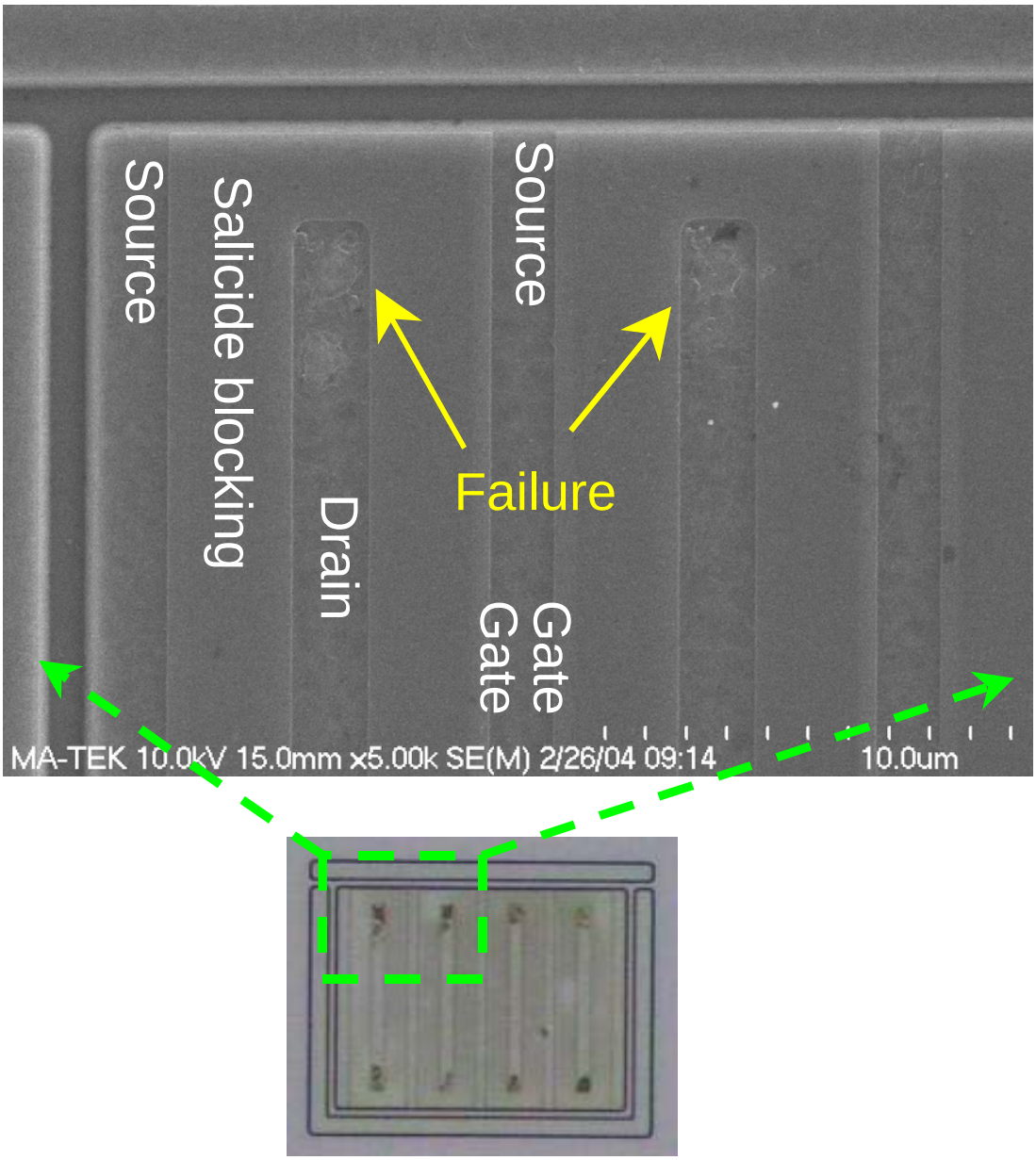


Fig. 4.12 SEM failure picture of salicide-blocking structure NMOS transistor under MM ESD zapping. (MM ESD robustness = 550 V, W/L = 240 μm/0.25 μm)

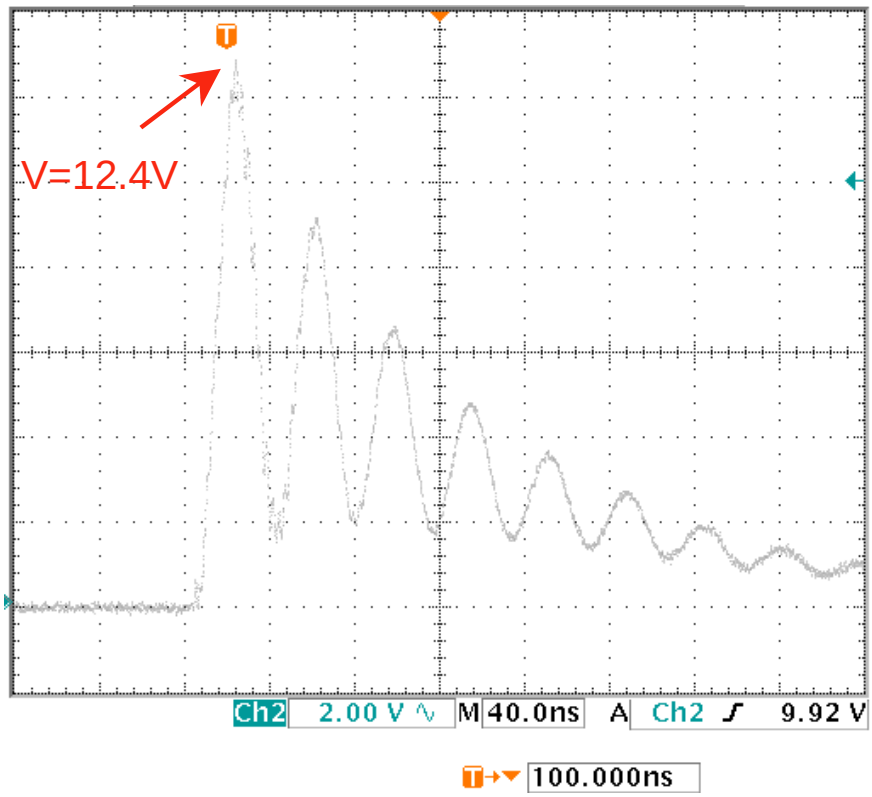


Fig. 4.13 The waveform of fully-salicided structure GGNMOS transistor under 1.1 kV HBM ESD zapping. (W/L = 240 μm/0.4 μm)

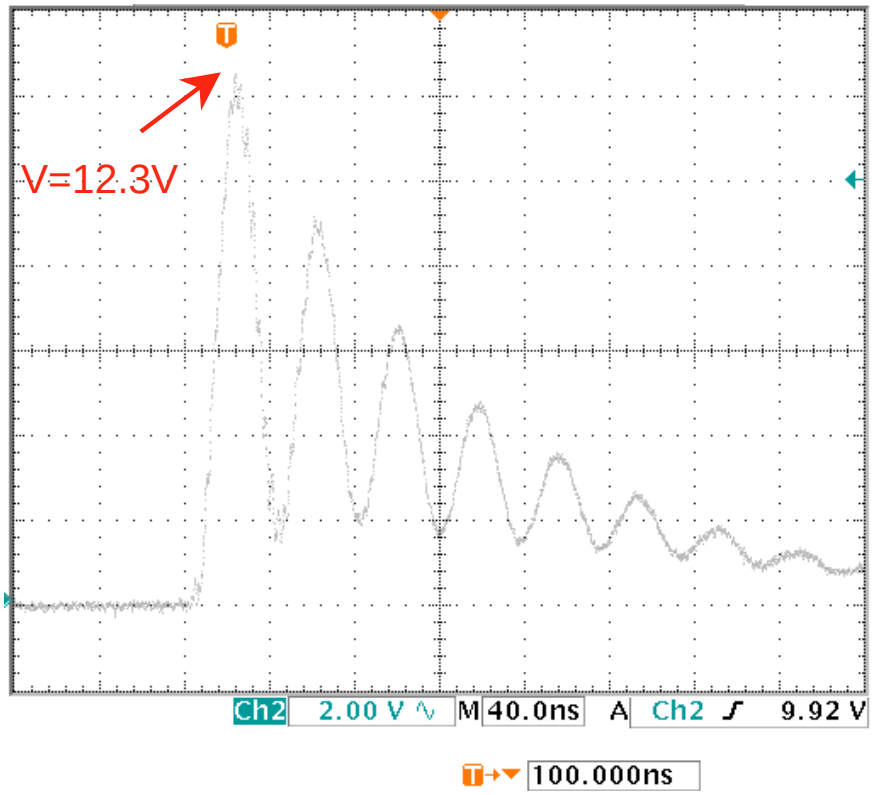


Fig. 4.14 The waveform of dummy-gate structure GGNMOS transistor under 1.1 kV HBM ESD zapping. (W/L = 240 μm/0.4 μm)

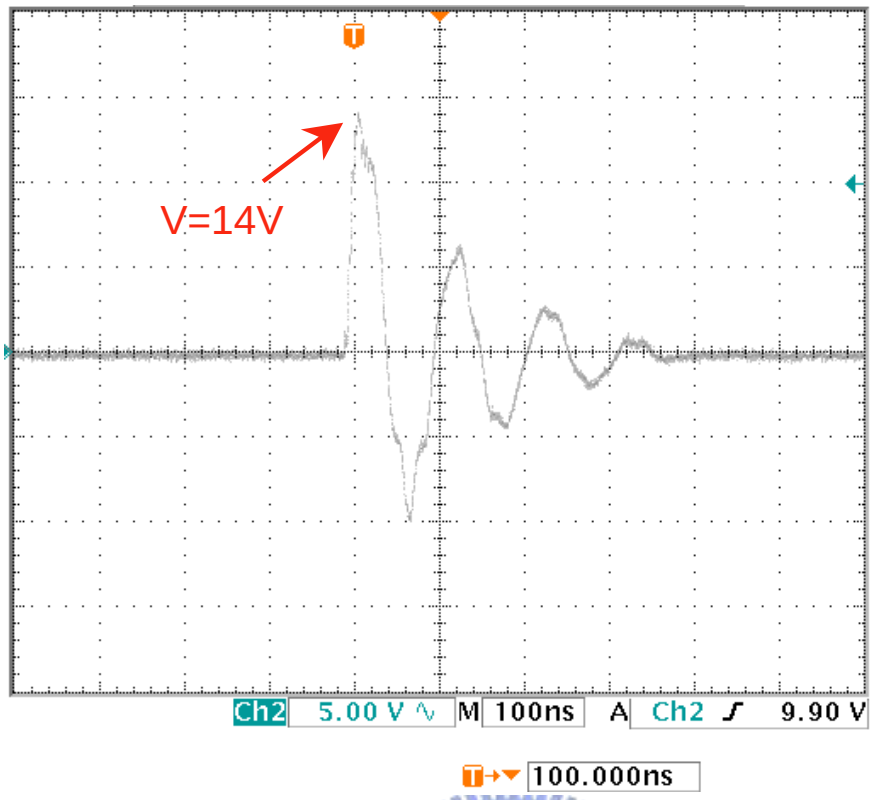


Fig. 4.15 The waveform of fully-salicided structure GGNMOS transistor under 130 V MM ESD zapping. (W/L = 240 μm/0.4 μm)

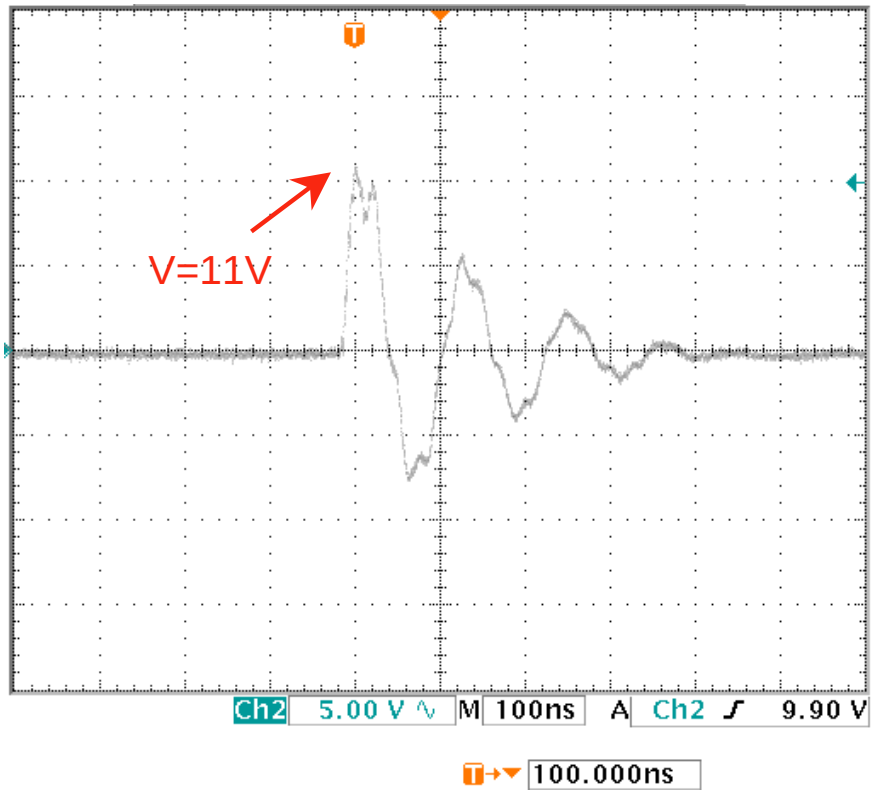


Fig. 4.16 The waveform of dummy-gate structure GGNMOS transistor under 130 V MM ESD zapping. (W/L = 240 μm/0.4 μm)

CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

5.1 Conclusions

To improve the non-uniform turn-on issue and current localization in salicide CMOS technology, four different types of transistors are fabricated and compared previously. A novel dummy-gate structure NMOS transistor proposed to significantly improve machine-mode ESD robustness has been practically verified in 0.25 μm CMOS process in this work. The MM level of proposed dummy-gate structure NMOS transistor with dimension of W/L = 240 μm/0.25 μm is greater than 400 V. However, HBM ESD robustness of this kind GGNMOS is not better than that of conventional structure. The HBM ESD robustness of transistors is clamped by DCGS and drain contact to dummy-gate spacing discussed in Chapter 3 and Chapter 4. On the whole, the proposed novel dummy-gate structure NMOS transistor is process compatible with general CMOS process without any extra process to improve MM ESD robustness.

5.2 Future Works

According to the experimental results in Chapter 3 and Chapter 4, the MM ESD robustness of GGNMOS has been improved by applying novel dummy-gate structure. However, HBM ESD robustness of GGNMOS with dummy gate structure is not better than that with conventional structure. This is because HBM ESD robustness of transistors is limited by drain contact to dummy-gate spacing. So, the result is quite different with the expected goal. So, the drain contact to dummy gate spacing needs to be optimized to get a good ESD result.

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論文名稱：**矽化金屬互補式半導體製程之新型靜電放電防護元件**

New ESD protection devices with dummy-gate structure in a fully salicided CMOS technology