國立交通大學

電子工程學系　電子研究所碩士班

碩　士　論　文

應用於薄膜電晶體之平面顯示器玻璃基底上的類比電路設計

Analog Circuits Design on Glass Substrate for TFT Panel Applications

研 究 生　：　李宇軒

指導教授　：　柯明道　教授

中華民國九十六年六月

應用於薄膜電晶體之平面顯示器
玻璃基底上的類比電路設計

Analog Circuits Design on Glass Substrate for TFT Panel Applications

研 究 生： 李宇軒　　Student ：Yu-Hsuan Li

指導教授： 柯明道 教授　　Advisor ：Prof. Ming-Dou Ker

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao-Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master

in

Electronics Engineering

June 2007

Hsin-Chu, Taiwan, Republic of China

中華民國九十六年六月

應用於薄膜電晶體之平面顯示器
玻璃基底上的類比電路設計

學生: 李 宇 軒　　指導教授: 柯 明 道 教授

國立交通大學

電子工程學系　電子研究所碩士班

摘要

低溫複晶矽 (low temperature poly-silicon) 薄膜電晶體 (thin-film transistors)已被視為一種材料廣泛地研究於可攜帶式系統產品中，例如數位相機、行動電話、個人數位助理 (PDA) 、筆記型電腦等等，這是由於低溫複晶矽薄膜電晶體的電子遷移率約是傳統非晶矽 (amorphous silicon) 薄膜電晶體的一百倍大。此外，低溫複晶矽技術可藉由將驅動電路整合於顯示器之週邊區域來達到輕薄、巧小且高解析度的顯示器。這樣的技術也將越來越適合於系統面板 (system-on-panel) 應用之實現。

近年來，低溫複晶矽技術具有朝向將所有控制和驅動電路整合進玻璃基板的趨勢。一般而言，液晶顯示器驅動電路包含閘極驅動電路、資料驅動電路以及直流對直流轉換電路。資料驅動電路則是由移位暫存器、閂鎖器、電位移轉器、數位類比轉換器以及類比輸出緩衝器所組成。然而，由於使用狹小雷射製程窗口來產生大顆粒的複晶矽薄膜電晶體，這會使得複晶矽薄膜電晶體因為巨大的元件特性變化而具有較差的一致性。元件特性的變化對於在液晶顯示面板上的類比電路設計已經逐漸成為一個很嚴重的問題。也由於這個原因，在本論文中將著重於資料驅動電路中的類比電路設計。

在本篇論文當中，提出了一個適用於面板資料驅動電路且同時具有珈瑪校正功能的新型數位類比轉換器以及一個著重在元件特性變化之考量用於資料驅動電路上之類比輸出緩衝器，此兩電路均以 8-μm LTPS 製程技術實現。此一新型數位類比轉換器由於是採用電阻串的架構，所以非常適合珈瑪校正的設計。藉由此提出之新型架構其面積與複雜度也都能大大地被降低。此一新型的數位類比轉換器非常有利於將資料驅動電路整合至液晶顯示器的週邊區域。而所提出具有 P 型差動輸入對之類比輸出緩衝器則能操作在 50 kHz 下並具有至少 1 至 9 V 的輸出範圍。藉著使用 P 型差動輸入對來抑制元件特性變化的方法除了能夠保持電路原有之效能外，還能夠提昇整體電路的製程良率。這樣的一個類比輸出緩衝器更加適用於資料驅動電路的輸出端來提供顯示器一個均勻的亮度以及較高的解析度。

最後，此具有珈瑪校正功能之新型折疊電阻串數位類比轉換器已在 8-μm 以及 3-μm LTPS 製程下成功驗證。而擁有抑制元件特性變化之類比輸出緩衝器也已經在 8-μm LTPS 製程下成功地被設計並製造出。此外，關於其它的數位類比轉換器電路之分析與比較也將會在此篇論文中做討論及整理。

Analog Circuits Design on Glass Substrate for TFT Panel Applications

Student: Yu-Hsuan Li Advisor: Prof. Ming-Dou Ker

Department of Electronics Engineering & Institute of Electronics
National Chiao-Tung University

ABSTRACT

Low temperature poly-silicon (LTPS) thin-film transistors (TFTs) have been widely investigated as a material for portable systems, such as digital camera, mobile phone, personal digital assistants (PDAs), notebook, and so on, because the electron mobility of LTPS TFTs is about 100 times larger than that of the conventional amorphous silicon TFTs. Furthermore, LTPS technology can achieve slim, compact, and high-resolution display by integrating the driving circuits on peripheral area of display. This technology will also become more suitable for realization of system-on-panel (SOP) applications.

Currently, LTPS technology has a tendency towards integrating all control circuits and driver circuits on the glass substrate. In general, the liquid-crystal display (LCD) driver contains gate driver, data driver, and DC-DC converter. The data driver is composed of shifter registers, latch, level shifters, digital-to-analog converters (DACs), and analog output buffer. However, the poly-Si TFTs suffered poor

uniformity with large variations on the device characteristics due to the narrow laser process window for producing large-grained poly-Si TFTs. The device variation becomes a very serious problem for the analog circuit design on the LCD panel. For this reason, the analog circuits of the data driver are the focus in my works.

In this thesis, a novel DAC with gamma correction for on-panel data driver and an on-panel analog output buffer for data driver with consideration of device characteristic variation are proposed in 8-μm LTPS technology. This new proposed architecture of the DAC is more suitable for gamma correction design due to the resistor string type of this DAC circuit. The area and complexity of the DAC also can be reduced greatly by this proposed architecture. This new DAC architecture is beneficial for data driver to be integrated in the peripheral area of the TFT-LCD panel in LTPS process. The proposed analog output buffer with P-TFTs input differential pair can be operated at 50-kHz operation frequency with at least a 1-to-9 V output swing. The device variation suppression method by using P-TFTs input differential pair can effectively maintain the performance of on-panel analog output buffer and increase the manufacturing yield of the circuit. This analog output buffer with suppressing device variation is more suitable for using in the on-panel data drivers to provide a uniform brightness and high resolution display

Furthermore, the novel folded R-string DAC with gamma correction has been verified in 8-μm and 3-μm LTPS technology. The analog output buffer with suppressing device variation also has been designed and fabricated in 8-μm LTPS technology. The analysis and comparison of the other DAC circuits are also included in this thesis.

誌謝

碩士二年，轉眼間就要畢業了，在這二年之中，首先最要感謝的是我的指導教授，柯明道教授的殷殷教誨，在於研究上他給予我許多的自由、指導與建議，還提供我相當多的資源，讓我能不斷地的充實自己；教導我們做事情要抱持嚴謹的態度，待人處事要圓融等，平常也會關心我們的生活狀況，亦師亦友，讓我獲益良多。此外，由於老師的努力，讓我能有與業界合作與接觸的機會，也因此擁有了許多晶片驗證的機會，在研究上不會有後顧之憂，另外，老師也常常為了修改我們的論文而廢寢忘食。在此，我要向柯明道教授致上我最深的謝意，謝謝您讓我有今天的成長。

在這段求學的過程中，『中華映管股份有限公司』以及『友達光電股份有限公司』，給予我許多的研究的資源與幫助，使我的電路能夠順利完成。在此特別感謝黃俊堯經理、邱振倫、廖偉見、許峻源、李純懷經理、郭俊宏副理等諸位長官以及『工研院系統晶片技術發展中心』的陳世宏學長、熊櫻霞女士，在實驗與量測設備上，所給予我的幫忙。

此外，我也要感謝『奈米晶片與系統實驗室』的陳世倫、許勝福、陳榮昇、顏承正、張瑋仁、蕭淵文、陳世宏、胡芳綾、陳佳惠、賴泰翔、王資閔、王暢資、莊介堯、羅怡凱等諸位實驗室學長姐以及學弟們，在各方面給予我許多幫助使我能順利完成碩士論文。感謝『奈米晶片與系統實驗室』及助理卓慧貞小姐給予我在研究上的資源及行政上的幫助，讓我完成學業。

接著要感謝的是一起打拼的同學們，小王、暢資、松諭、巧玲、黃董、宗裕、Hakko、野獸、神童、維德、國忠以及順哥，大家一起修課、熬夜，出遊、拍照玩鬧，讓我的碩士生活充滿歡樂；互相扶持，加油打氣讓我能充電再繼續努力。也謝謝國光新竹幫的學長姐們，Attila、Pluck、小白兔、大頭、魯巴、鳥逸、前野、大過和阿發，謝謝你們一直以來的陪伴與關懷。

最後我要致上萬分的感謝給予我的父親 李春淋先生，以及我的母親 蔡錦桃女士，由於他們一直以來的關心、支持與無微不至的照顧，並細心的栽培我讀書，進而讓我擁有了今天的成就。當然，也要謝謝我的女友-小豬，感謝她總是在我在沮喪無助時給於我最好的鼓勵、支持與建議，最後祝福我的師長、家人、朋友及學弟妹們事事順心、身體健康。我在撰寫的過程中，雖力求嚴謹，然誤謬之處，在所難免，尚祈各位讀者賜予寶貴意見，使本論文能更加完善。

李　宇　軒

僅誌於竹塹交大

九十六年　六月

CONTENTS

TABLE CAPTIONS

FIGURE CAPTIONS

Chapter 1

Introduction

1.1 MOTIVATION

1.1.1 LCD Industry and LTPS Technology [1], [2]

The liquid-crystal display (LCD) industry has shown rapid growth in five market areas, namely, notebook computers, monitors, mobile equipment, mobile telephones, and televisions. For high-speed communication networks, the emerging portable information tools are expected to grow in following on the rapid development of display technologies. Thus, the development of higher specification is demanded for LCD as an information display device. Moreover, the continual growth in network infrastructures will drive the demand for displays in mobile applications and flat panels for computer monitors and TVs. The specifications of these applications will require high-quality displays that are inexpensive, energy-efficient, lightweight, and thin.

Amorphous silicon (a-Si) thin-film transistors (TFTs) are widely used for flat-panel displays. However, the low field-effect mobility (ability to conduct current) of a-Si TFTs allows their application only as pixel switching devices; they cannot be used for complex circuits. In contrast, the high driving ability of polycrystalline Si (p-Si) TFTs allows the integration of various circuits such as display drivers. Eliminating LSI (large-scale integration) chips for display drivers will decrease the cost and thickness of displays for various applications.

There are high-temperature and low-temperature poly-Si TFTs, defined by the maximum process temperature they can withstand. The process temperature for

high-temperature poly-Si can be as high as 900°C. Hence, expensive quartz substrates are required, and the profitable substrate size is limited to around 6 in. (diagonal). Typical applications are limited to small displays. The process temperature for low-temperature poly-Si (LTPS) TFTs, on the other hand, is less than 600°C, which would allow the use of low-cost glass substrates. This makes possible direct-view large-area displays—for example, UXGA (ultra extended graphics array) monitors of up to 15.1 in. (diagonal) with a resolution of 1600 x 1200 pixels. For this reason, LTPS technology has been applied successfully to not only small-sized displays, but also medium- and large-screen products.

1.1.2 System-on-Panel Displays

LTPS TFT-LCD technology has some features of system integration within a display. It can make a compact, high reliable, high resolution display. Because of this property, LTPS TFT-LCD technology is widely used for mobile displays. Fig. 1.1 shows the system integration roadmap of LTPS TFT-LCD [3], [4].

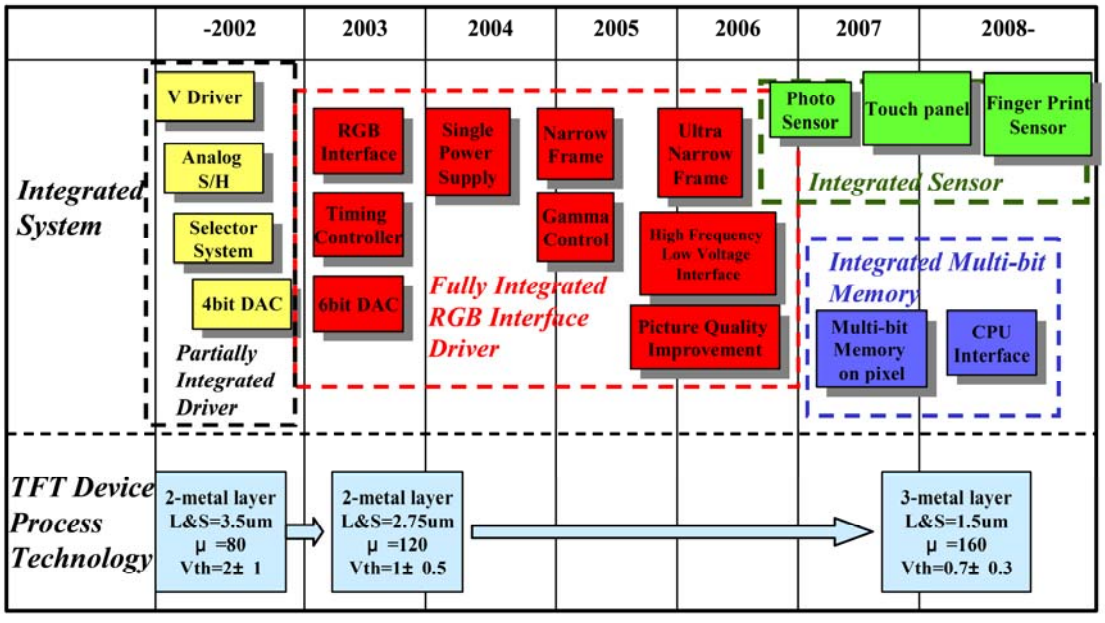


Fig. 1.1 System integration roadmap of LTPS TFT-LCD.

System-on-panel (SOP) displays are value-added displays with various functional circuits, including static random access memory (SRAM) in each pixel, integrated on the glass substrate [3]. Fig. 1.2 shows the basic concept of pixel memory technology. When SRAMs and a liquid crystal AC driver are integrated in a pixel area under the reflective pixel electrode, the LCD is driven by only the pixel circuit to display a still image. It means that no charging current to the data line for a still image. This result is more suitable for ultra low power operation. Eventually, it may be possible to combine the keyboard, CPU, memory, and display into a single "sheet computer". The schematic illustration of the "sheet computer" concept and a CPU with an instruction set of 1-4 bytes and an 8b data bus on glass substrate are shown in Fig. 1.3, respectively [1], [5]. Fig. 1.4 shows the roadmap of LTPS technologies leading toward the realization of sheet computers. Finally, all of the necessary function will be integrated in LTPS TFT-LCD. Although the level of LTPS is as almost the same as the level of the crystal Si of 20 years ago, actual operation of 50MHz with 1μm design will be realized near future [6].

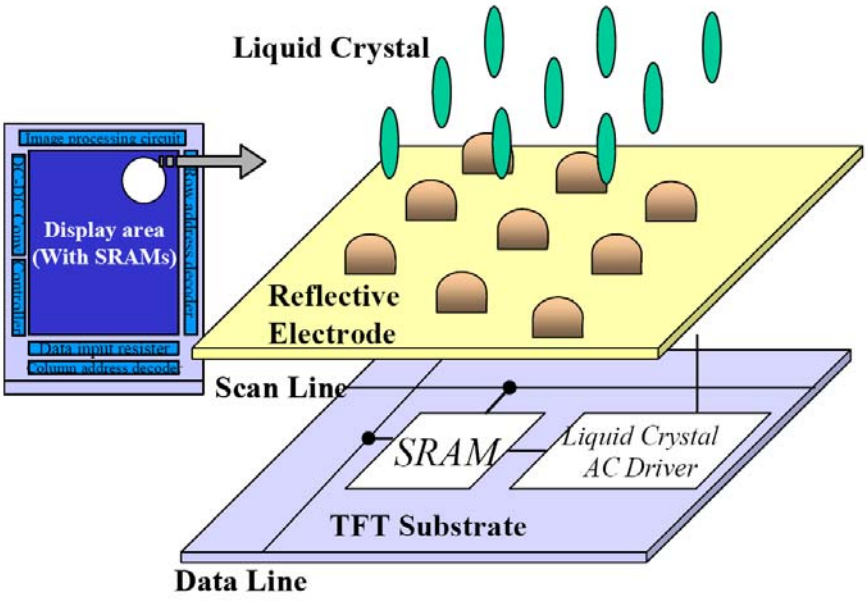
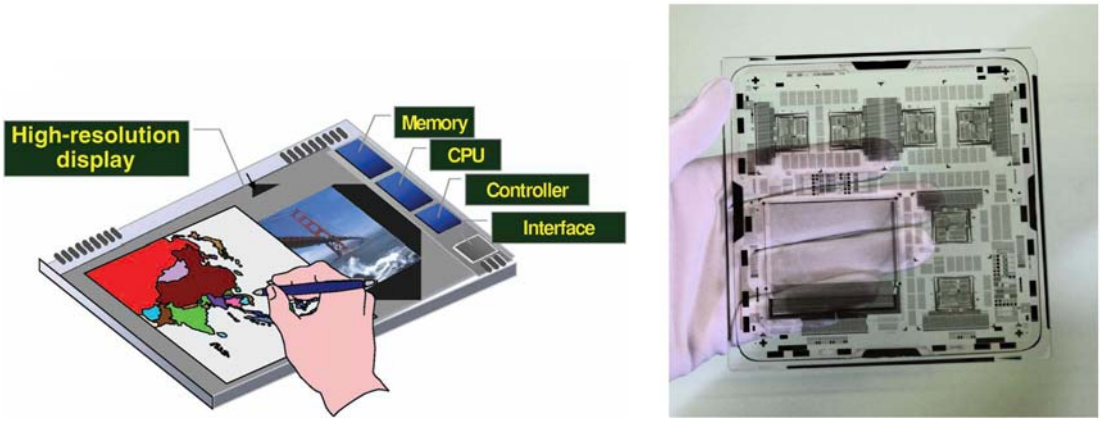
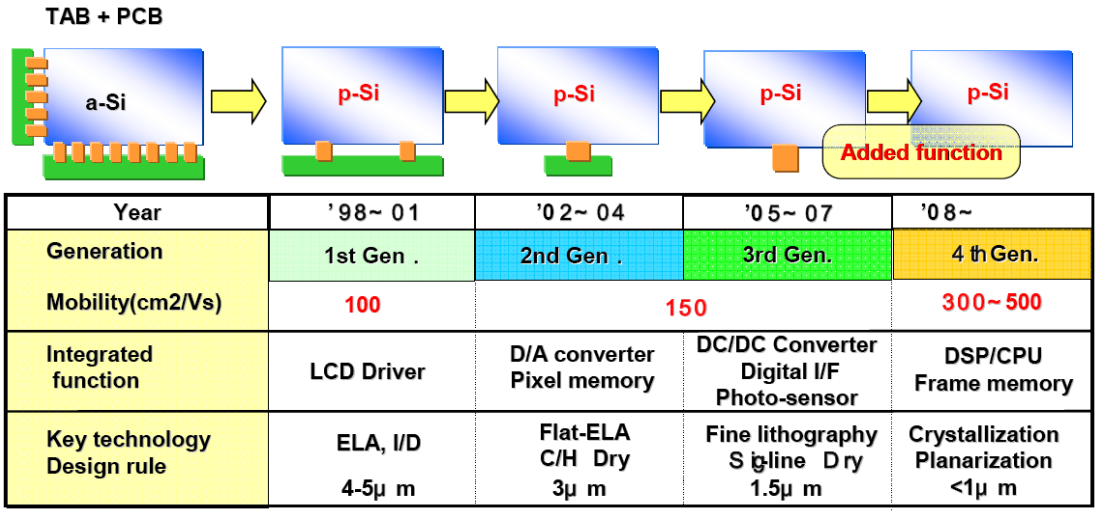


Fig. 1.2 Basic concept of pixel memory technology.



(a) (b)

Fig. 1.3 (a) The schematic illustration of the "sheet computer" concept and (b) a CPU with an instruction set of 1-4 bytes and an 8b data bus on glass substrate.



Year	'98~ 01	'02~ 04	'05~ 07	'08~
Generation	1st Gen .	2nd Gen .	3rd Gen.	4 th Gen.
Mobility(cm2/Vs)	100	150		300~500
Integrated function	LCD Driver	D/A converter Pixel memory	DC/DC Converter Digital I/F Photo-sensor	DSP/CPU Frame memory
Key technology Design rule	ELA, I/D 4-5μ m	Flat-ELA C/H Dry 3μ m	Fine lithography S tepper i-line Dry 1.5μ m	Crystallization Planarization <1μ m

Fig. 1.4 The roadmap of LTPS technologies leading toward the realization of sheet computers.

1.1.3 The Advantages of the SOP LTPS TFT-LCD Displays

The distinctive feature of the LTPS TFT-LCD is the elimination of TAB-ICs (integrated circuits formed by means of an interconnect technology known as tape-automated bonding). LTPS TFTs can be used to manufacture complementary metal oxide semiconductors (CMOSs) in the same way as in crystalline silicon metal oxide semiconductor field-effect transistors (MOSFETs). Fig. 1.5 shows the cross sectional structure of a LTPS TFT CMOS. For a-Si TFT-LCDs, TAB-ICs are

connected to the left and bottom side as the Y driver and the X driver, respectively. Integration of the Y and X drivers with LTPS TFTs requires PCB (printed circuit board) connections on the bottom of the panel only. The PCB connection pads are thus reduced to one-twentieth the size of those in a-Si TFT-LCDs. The most common failure mechanism of TFT-LCDs, disconnection of the TAB-ICs, is therefore decreased significantly. For this reason, the reliability and yield of the manufacturing can be improved. Decreasing the number of TAB-IC connections also achieves a high-resolution display because the TAB-IC pitch (spacing between connection pads) limits display resolution to 130 ppi (pixels per inch). A higher resolution of up to 200 ppi can be achieved by LTPS TFT-LCDs. Therefore, the SOP technology can effectively relax the limit on the pitch between connection terminals to be suitable for high-resolution display. Furthermore, eliminating TAB-ICs allows more flexibility in the design of the display system because three sides of the display are now free of TAB-ICs [1]. Fig. 1.6 shows a comparison of a-Si and LTPS TFT-LCD modules. The 3.8" SOP LTPS TFT-LCD panel has been manufactured successfully and it is shown in Fig. 1.7.

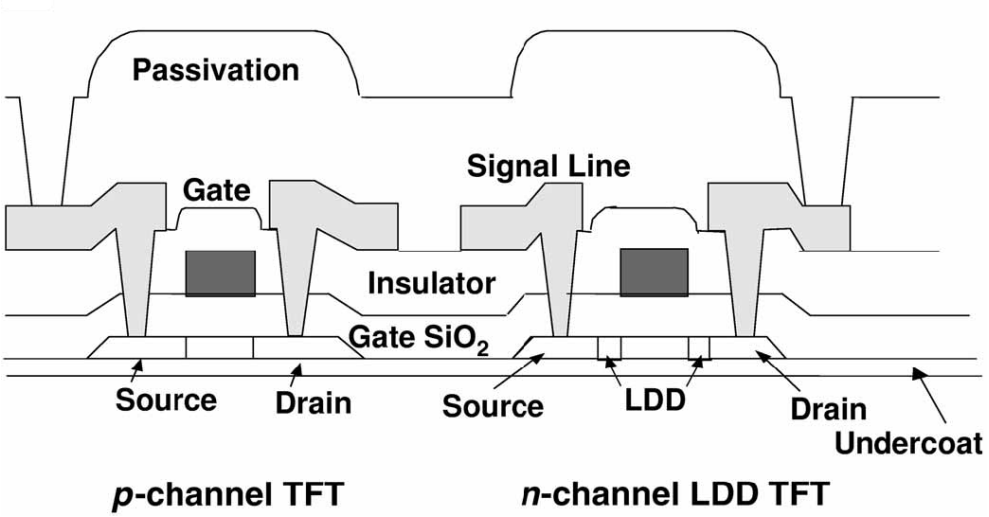
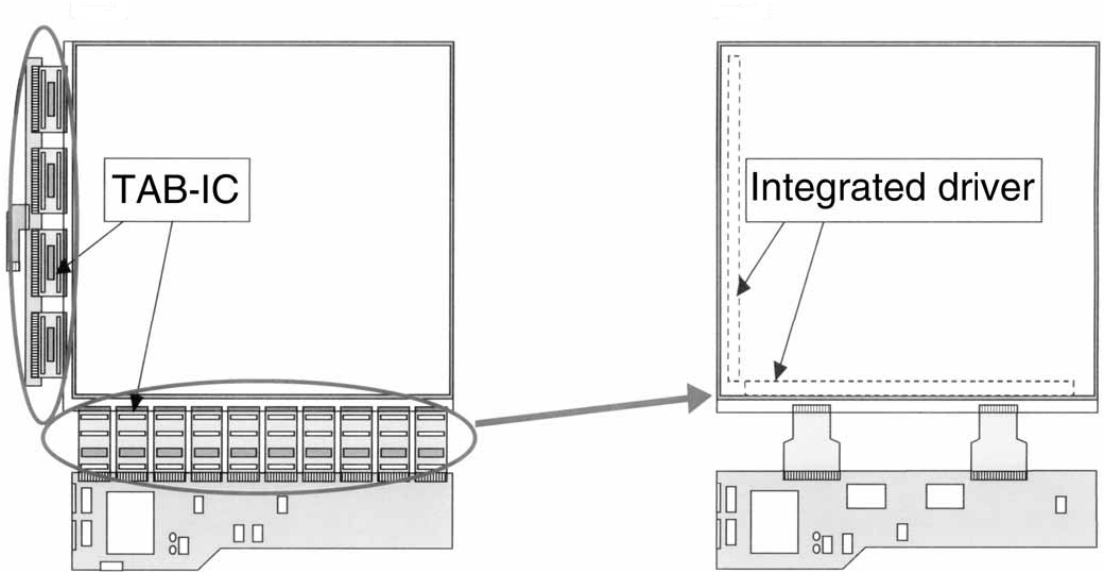


Fig. 1.5 Schematic cross-section view of the structure of a LTPS complementary metal oxide semiconductor (CMOS). LDD = lightly doped drain.



(a) (b)

Fig. 1.6 (a) Comparison of an amorphous silicon TFT-LCD module and (b) a low-temperature polycrystalline silicon TFT-LCD module.

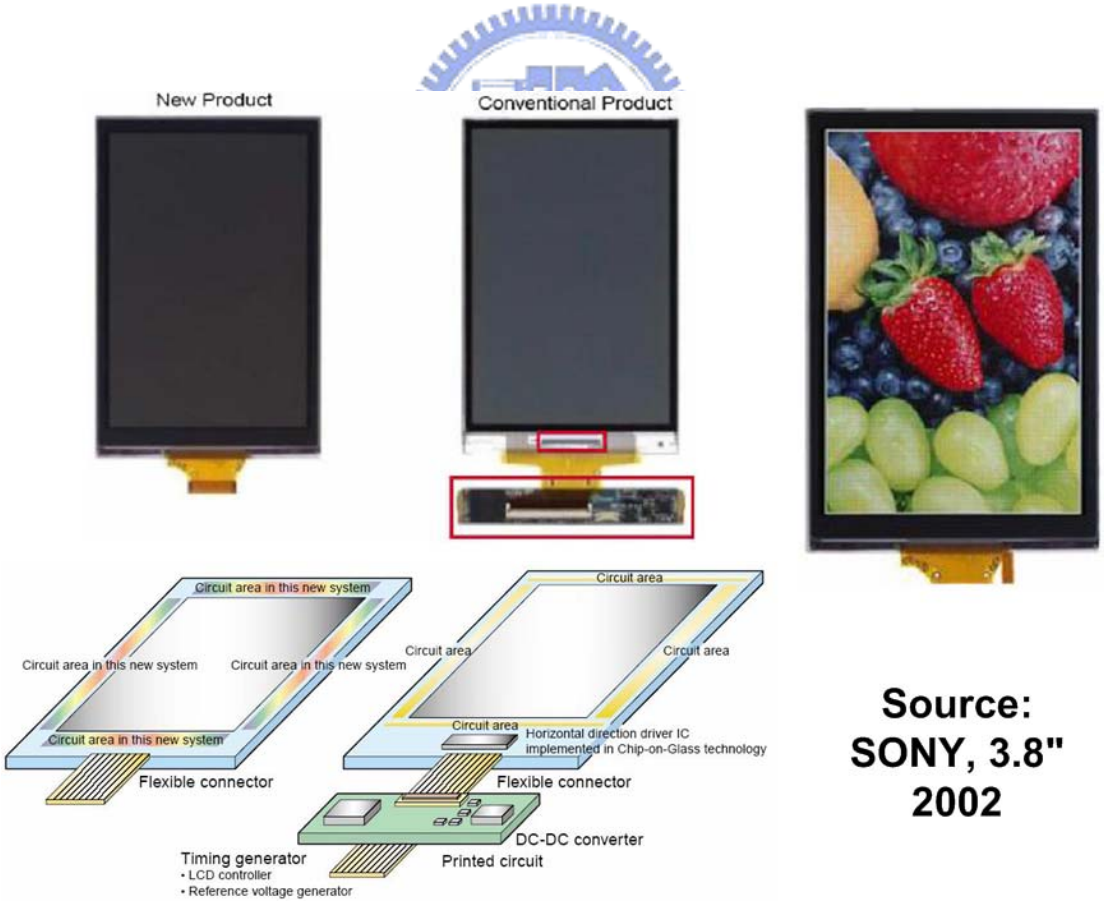


Fig. 1.7 The comparison of new SOP technology product and conventional product. The new 3.8” SOP LTPS TFT-LCD panel has been manufactured by SONY corp. in 2002.

1.1.4 Future Application of "Input Display" [6]

SOP technology also has a potential of integration of input function other than output function of display, which will pave the way for future displays. These various ways of integration are totally expressed by SOP technology. The input display technology opens opportunities for new applications for personal and business use. The new technology is scalable up and down, and can be applied to diverse products, from cellular phones to personal computers. The full scope to our imagination concerning future use of "Input Display" is shown in Fig. 1.8. Its wide range of usage will include recording of text or images for on-line shopping and the like, without a scanner device saving personal data and images to a computer, and personal identification, auto-power control with photo-sensor (or ambient light sensor, shown in Fig. 1.9) suitable for extremely low power cellular phone, detecting the position of finger or pen for some touch-sensing (a new touch-panel is shown in Fig. 1.10), and so on.

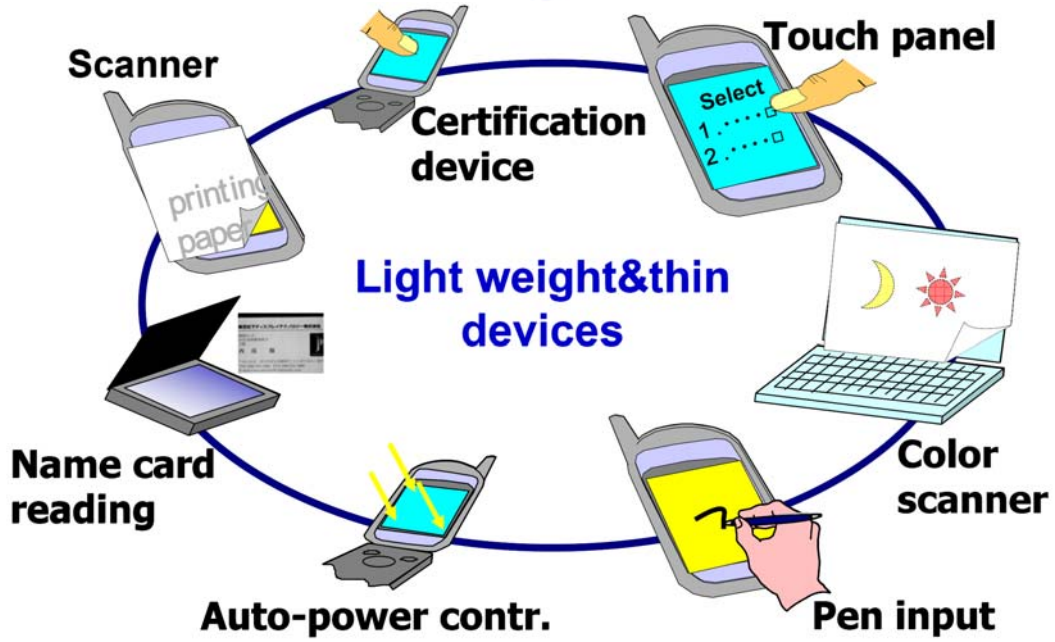


Fig. 1.8 Future application of "Input Display".

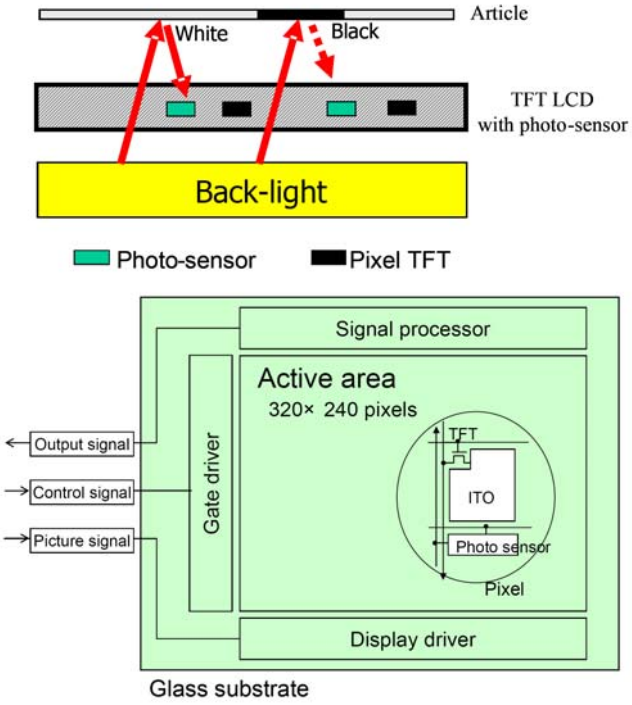


Fig. 1.9 The principle and structure of the photo-sensing display.

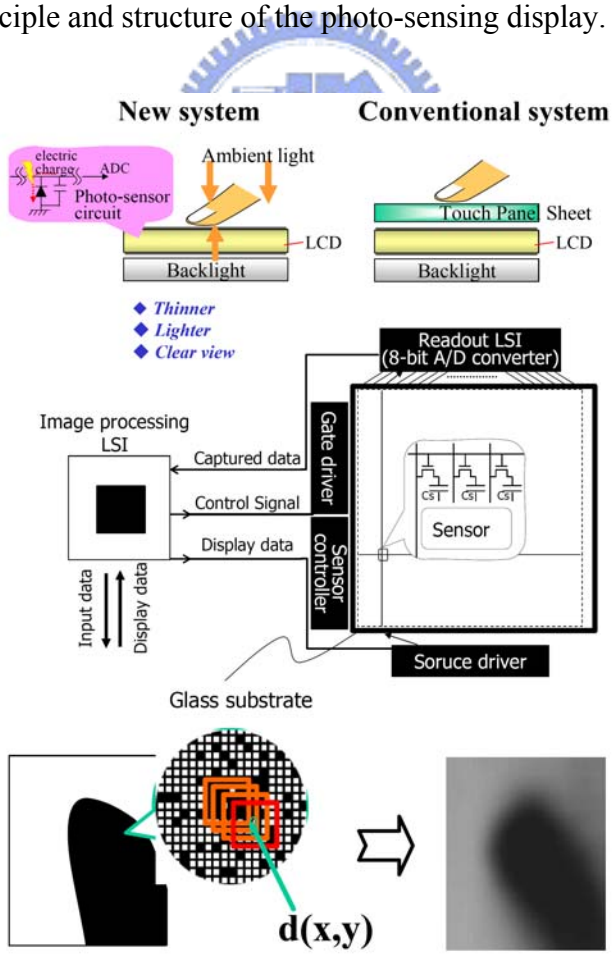


Fig. 1.10 The system architecture and image-capturing finger of this new touch-panel.

According to above discussion, it can see that the fabrication cost will gradually be lowed and SOP (system on panel) will be implemented step by step in the future. Such integration technology contributes to shorten the product lead-time because lengthy development time of ICs can be eliminated. Actually, this integration level has been proceeding from simple digital circuits to the sophisticated ones such as digital-to-analog converters (DACs) [6]. Moreover, LTPS technology is compatible with OLED, which is another promising display device [1]. Therefore, design of driving circuits for TFT-LCD in LTPS technology is worthy expecting in the future. In this thesis, a novel 6-bit folded R-string DAC with gamma correction for on-panel data driver and an on-panel analog output buffer for data driver with suppressing device characteristic variation technique have been proposed in LTPS technology.

1.2 THESIS ORGANIZATION

In chapter 2, some background knowledge of thin-film transistor liquid crystal displays, like liquid crystal display structure, driving method in TFT-LCD panel and periphery circuit block, will be introduced. The nonlinearity relationship between luminance and human visual system (HVS) and gamma correction will also be discussed in chapter 2. A novel DAC with gamma correction for on-panel data driver will be proposed and verified in chapter 3. Moreover, the analysis and comparison of the many kinds of DAC circuits will also be introduced in this chapter particularly. In chapter 4, an on-panel analog output buffer for data driver with consideration of device characteristic variation will be proposed. Besides, the simulation and measurement results of this proposed analog output buffer will be discussed in this chapter. The last chapter recapitulates the major consideration of this thesis and concludes with suggestions for future investigation.

Chapter 2

Background Knowledge of Thin-Film Transistor Liquid Crystal Displays

2.1 LIQUID CRYSTAL DISPLAY STRUCTURE

2.1.1 Material and Display Theory of Liquid Crystal [7], [8]

Most liquid crystals consist of molecules shaped like the rod. The direction of long axis is called the *director*, given by the vector $\vec{n}$, which is an apolar vector as $\vec{n}$ and $-\vec{n}$ are equivalent. Rod-shaped molecules are also termed *calamitic*.

We focus on calamitic (Bahadur, 1990; Demus *et al*., 1998a,b) liquid crystals as they are important for applications. One characteristic of the phase variation of liquid crystal materials is "the twice melting" showing in Fig. 2.1. Below the melting point (T_m) they are solid, crystalline and anisotropic, when above the clearing point (T_c) they are a clear and isotropic liquid. The material has the appearance of a milky liquid between T_c and T_m but still exhibit the ordered phases.

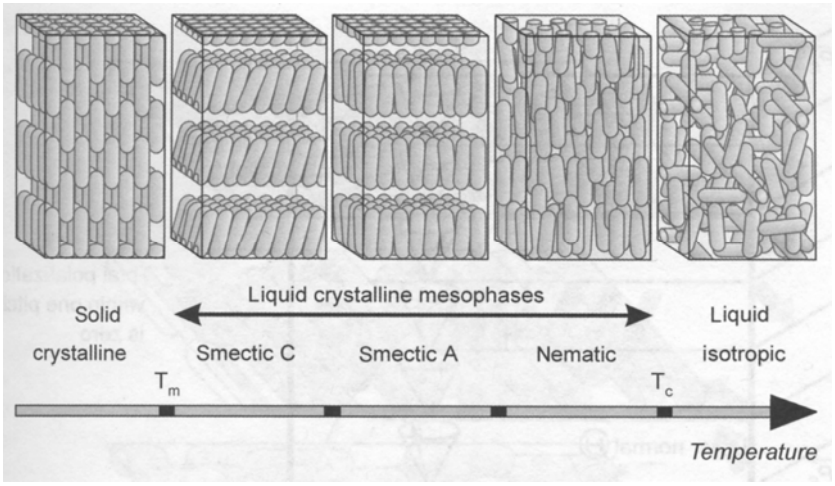
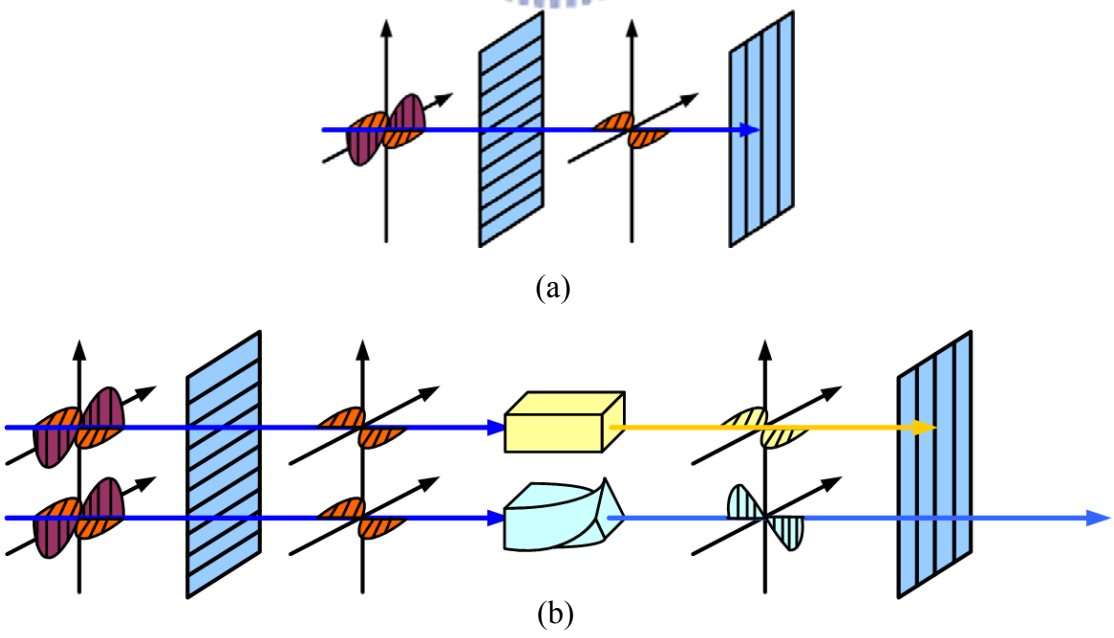


Fig. 2.1 Phases of liquid crystal materials versus temperature.

The phases during T_c and T_m can roughly be divided into smectic phase and nematic phase by its molecules arrangement. The molecules are ordered in two dimensions in smectic phase and appeared with only a one-dimensional order in nematic order. Most LCD materials' nematic phase is the basis and widely used as Twisted Nematic (TN) cell with active matrix addressing. Because the twist of liquid crystals can be controlled by the electric field that is applied across it, liquid crystals are used as a switch that passes or blocks the light.

The polarizer can block or pass the specific light by changing the phase of the polarizer. In general, the first polarizer of a couple of polarizers is called *polarizer* and the second polarizer of these is called *analyzer*. The light can be blocked by a couple of polarizers with 90° phase error, is shown in Fig. 2.2 (a). If we twist the liquid crystal molecule by applying the specific electric field across it, the light still can pass the polarizer. This is because the direction of liquid crystal molecules varies with electric field and it can guide the light along the long axis, shown in Fig. 2.2 (b).



(a)

(b)

Fig. 2.2 (a) A couple of polarizers with 90° phase error. (b) A couple of polarizers with liquid crystals.

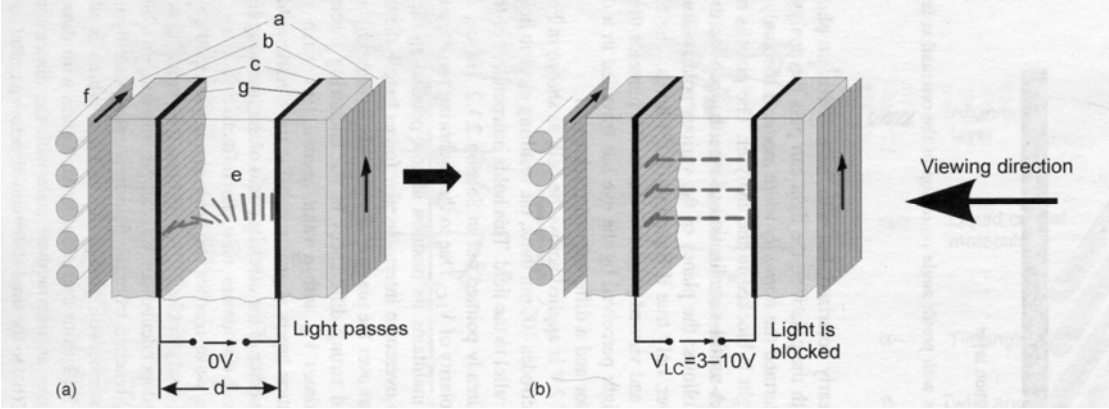


Fig. 2.3 The structure of a TN-LCD (a) while light is passing, and (b) while light is blocked. a: polarizer; b: glass substrate; c: transparent electrode; g: orientation layer; e: liquid crystal; f: illumination.

Fig. 2.3 (a) shows a pixel of a transmissive twisted nematic LC-cell with no voltage applied. The white backlight *f* passes the polarizer *a*. The light leaves it linearly polarized in the direction of the lines in the polarizer, and passes the glass substrate *b*, the transparent electrode *c* out of Indium-Tin-Oxide (ITO) and the transparent orientation layer *g*. In this case, the analyzer is crossed with polarizer. The light can pass the analyzer without applied voltage due to the twisted nematic LC-cell and the pixel appears white. If a voltage V_{LC} of the order of 10 V is applied across the cell, as shown in Fig. 2.3 (b), all molecules aligned parallel to the electric field. In this state, the wave that reaches the crossed analyzer is polarized in the same direction as at the input. Therefore, the analyzer blocks the light and the pixel appears black. This operation is termed the *normally white* (NW) *mode*. On the contrary, if the analyzer is rotated by 90°, paralleled with polarizer, the light is blocked in the analyzer. The pixel is black. This is called the *normally black* (NB) *mode*. The transmitted luminance, also termed *transmittance*, of the light. Fig. 2.4 shows the transmitted luminance versus the normalized voltage (V_{LC}/V_0) across the LC cell for the normally white mode and the normally black mode, respectively.

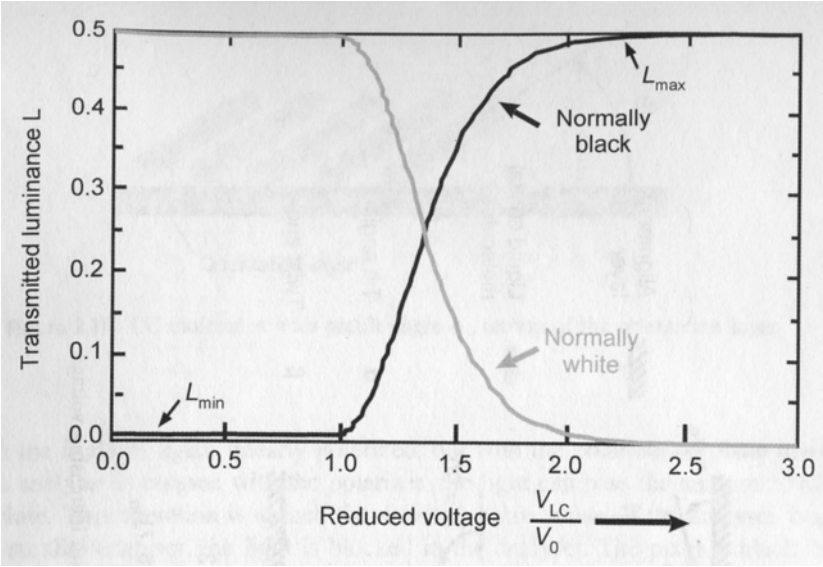


Fig. 2.4 The transmitted luminance versus the normalized voltage (V_{LC}/V_0) across the LC cell for the normally white mode and the normally black mode.

2.1.2 Liquid Crystal Display Module Structure

The cross section structure of TFT-LCD panel is shown in Fig. 2.5 particularly. It can be roughly divided into two part, TFT array substrate and color filter substrate, by liquid crystal filled in the center of LCD panel. We still need a backlight module including an illuminator and a light guilder since liquid crystal molecule cannot light by itself. However it usually consumes the most power of the system, some applications such as mobile communications try to exclude or replace it from the system. In TFT array substrate, we need a polarizer, a glass substrate, a transparent electrode and an orientation layer. In color filter substrate, we also need an orientation layer, a transparent electrode, color filters, a glass substrate and a polarizer. Most transparent electrodes are made by ITO, and they can control the directions of liquid crystal molecules in each pixel by voltage supplied from TFT on the glass substrate. Color filters contain three original colors, red, green, and blue (RGB). As the degree of light, named “gray level”, can be well controlled in each pixel covered by color filer, we will get more than million kinds of colors.

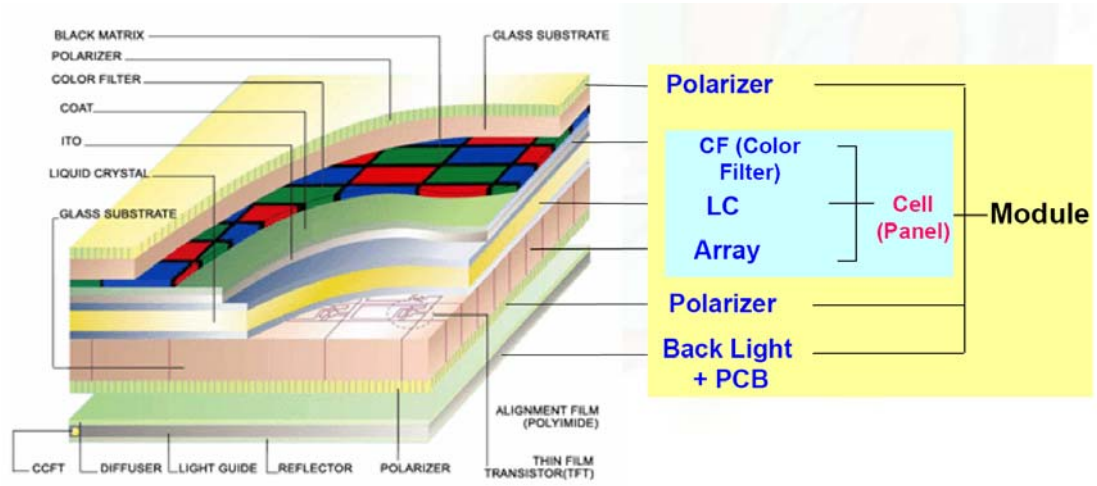


Fig. 2.5 The cross section structure of TFT-LCD panel.

2.1.3 Equivalent Model of Dot in each Pixel Cell

One dot is the most fundamental unit of LCD panel and each dot can express one kind of original color. Because one full color should be mixed with three original colors, each pixel contains three dots. As a result, if the resolution of gray level of each dot is 8 bits, then the whole panel can show 16,777,216 (2^8x2^8x2^8) kinds of colors at all. Fig. 2.6 shows the basic layout and cross section of an AMLCD sub-pixel. The equivalent circuit of a TFT in the sub-pixel with voltages, currents, and parasitic capacitances is shown in Fig. 2.7 [7].

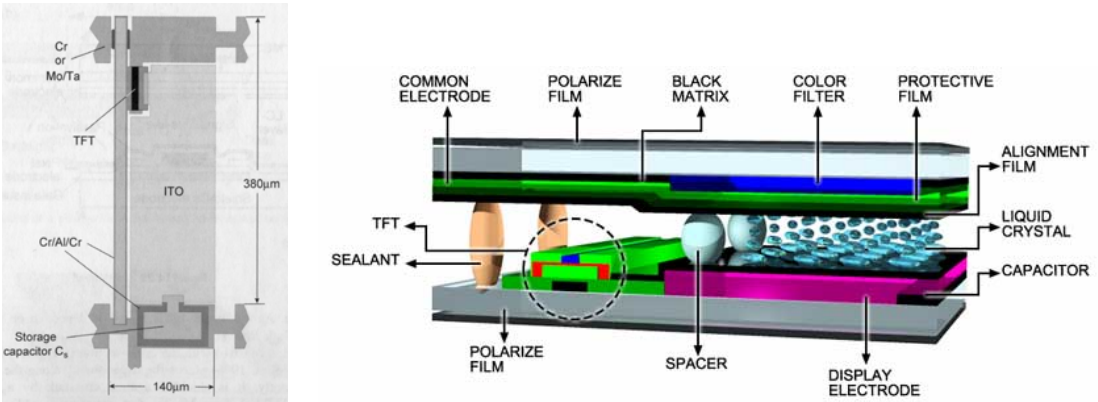


Fig. 2.6 The basic layout and cross section of an AMLCD sub-pixel.

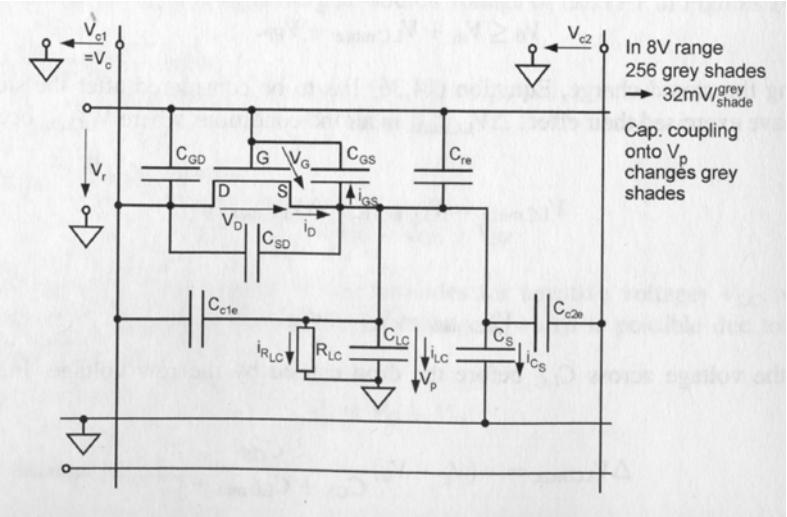


Fig. 2.7 The equivalent circuit of a TFT in the sub-pixel with voltages, currents, and parasitic capacitances.

Fig. 2.8 and Fig. 2.9 show the layout and equivalent circuit of each sub-pixel, including two major structures, the C_S on common mode and C_S on gate mode. The right-down region of the sub-pixel layout is the TFT switch, and the region of each sub-pixel area excluding TFT switch and storage capacitor (C_S) is called aperture region, which is the largest window for light passing. So the larger ratio of aperture region to pixel area is the better performance of the TFT-LCD panel. In Fig. 2.9, the M_S is a thin film transistor as a switch. The C_{lc} is the effective capacitor of liquid crystals, and C_S is the storage capacitor used to maintain the voltage level of liquid crystals during the hold time of frame transitions. The C_{gd} is the parasitic capacitor between gate line and effective liquid crystal capacitor. The structure, C_S on gate, which connects the bottom of the storage capacitor to the previous row of the gate line has some benefits. By this structure, we can compensate the unstableness of voltage level due to the clock feed-through effect from C_{gd}. Furthermore, this structure also has larger aperture ratio. But the trade-off with the C_S on gate method is an increase in the RC time constant of the gate line, which reduces the TFT switching performance.

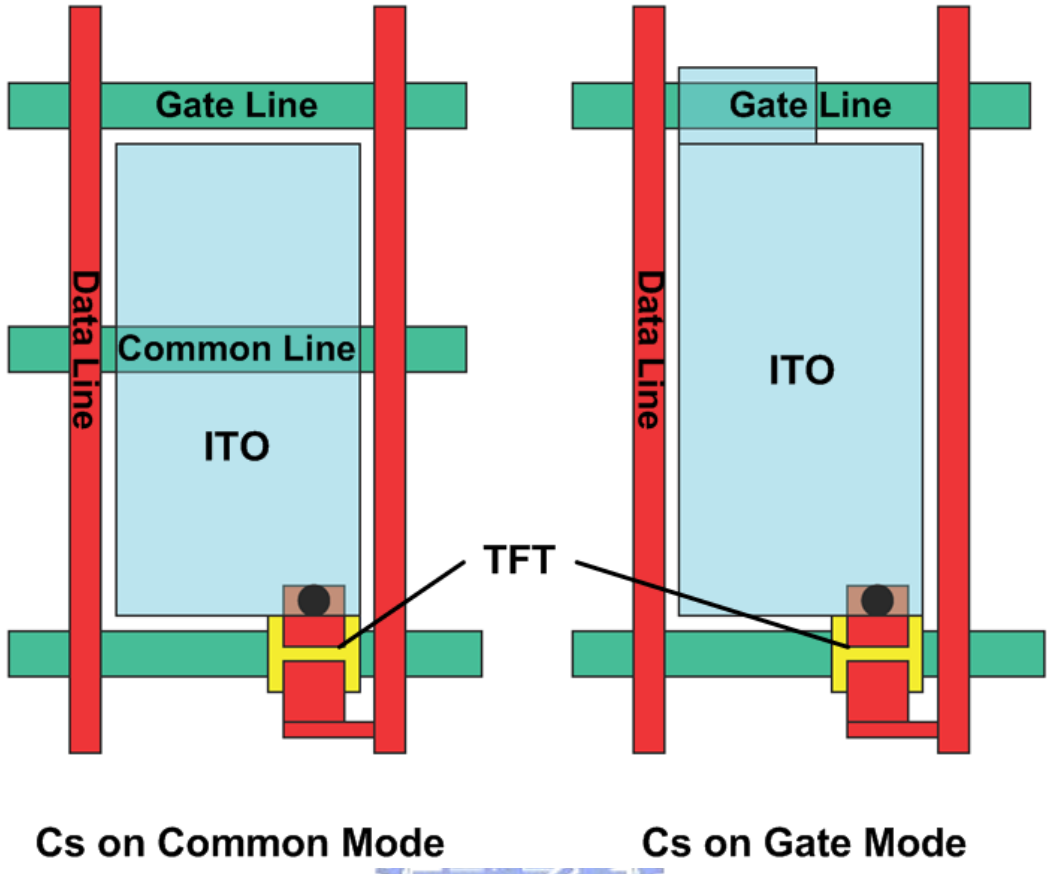


Fig. 2.8 The layout view of a TFT-LCD sub-pixel: (a) C_S on common mode and (b) C_S on gate mode.

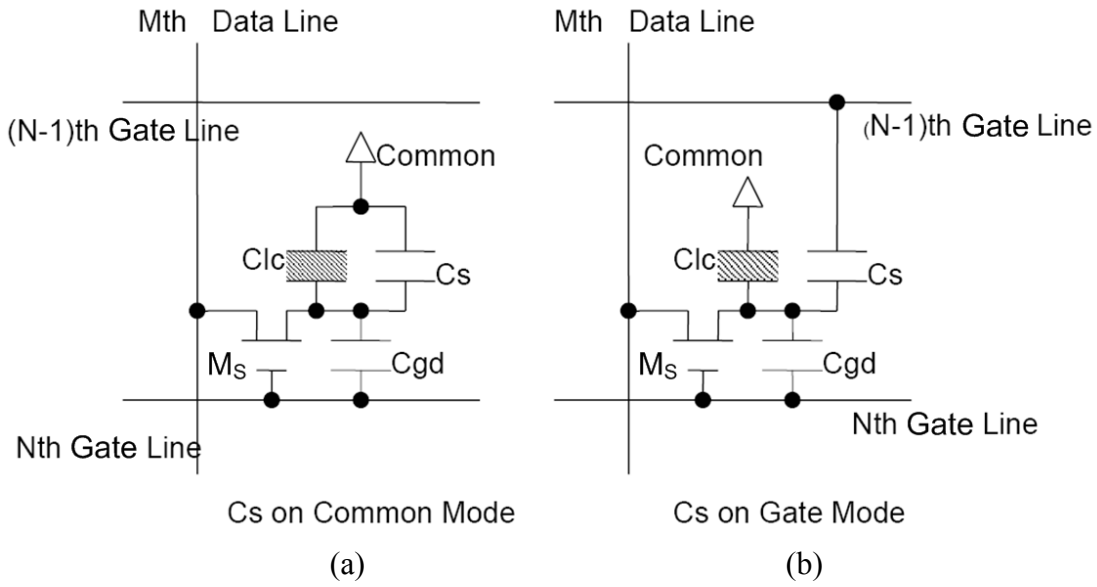
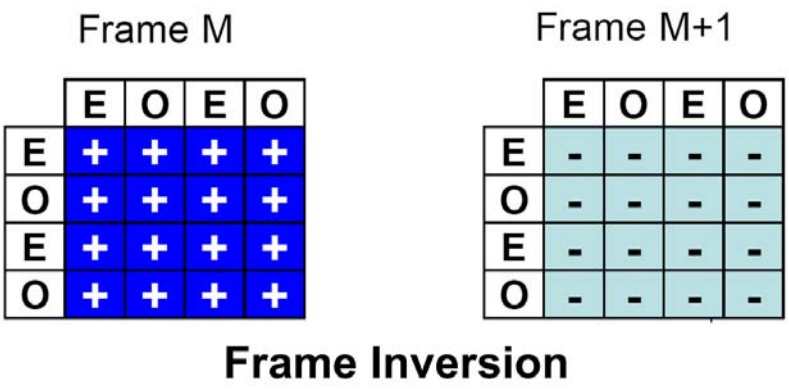


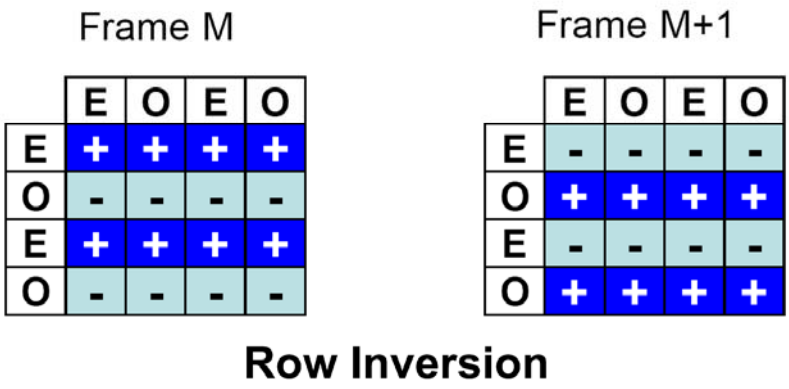
Fig. 2.9 The equivalent circuit of a TFT-LCD sub-pixel: (a) C_S on common mode and (b) C_S on gate mode.

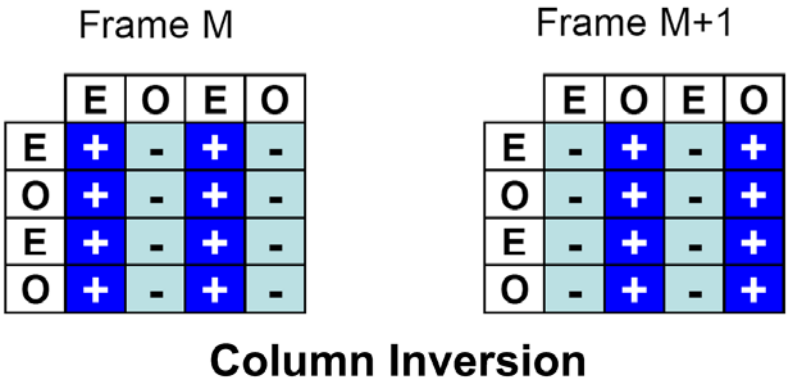
2.2 DRIVING METHOD IN TFT-LCD PANEL

2.2.1 Driving Method

Liquid crystal molecules can't be under a fixed voltage in the long period. The DC blocking effect and the DC residue (stick image) will be appeared under this condition. Therefore, the electric field polarity should be inversed every period to avoid the destruction of liquid crystals. The torque caused by electric filed is dependent on the magnitude of electric filed, not dependent on the polarity of electric filed. Therefore, the polarity of electric filed would not affect the twisting of the liquid crystal molecules. When the frame picture will be kept on the same gray level, the electric field across liquid crystals is changed into two polarities (positive and negative), alternately. As electric field is higher than common mode voltage the polarity is called positive polarity, otherwise it is called negative polarity. By this way, the liquid crystal molecules will avoid defection in the fixed applied voltage. In term of above description, the polarity inversions of LCD panel can be principally divided into four general types: frame inversion, row inversion, column inversion, and dot inversion [9]. They are listed in Fig. 2.10. Frame inversion is that all the adjacent pixels of the LCD panel have the same polarity. Row inversion (column inversion) is that each adjacent row pixels (adjacent column pixels) have different polarity. Finally, all the adjacent pixels of LCD panel have different polarity is called dot inversion. Dot inversion is the major driving method of LCD panel. This polarity inversion method has some benefits. By this method, we can achieve to higher quality image due to the reduction in both horizontal and vertical cross-talk. The flicker of image also can be reduced due to the spatial averaging of pixels. But the penalty of dot inversion method is an increase of the power consumption due to the line inversion component. This method is also incompatible with common voltage modulation.







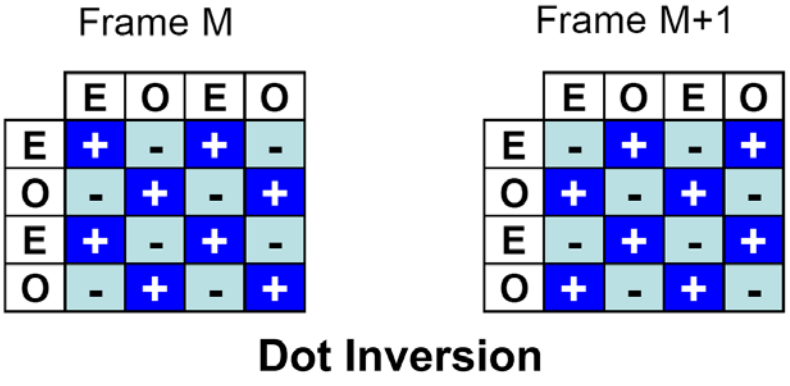


Fig. 2.10 The polarity inversions of TFT-LCD panel.

Based on the operational type of common mode voltage, the driving method can also be classified into direct driving and AC modulation driving. They are shown in Fig. 2.11 and Fig. 2.12, respectively. Direct driving method would keep its common voltage on a constant level. However, the common mode voltage of AC modulation driving method is not a constant level, is a period voltage. The characteristics of two driving methods are listed below:

- Direct driving method:
  - – Frame, row, column, and dot inversion are all available.
  - – Crosstalk and flicker can be eliminated.
- AC modulation driving method:
  - – Frame and row inversion are available.
  - – Low power dissipation in data driver.

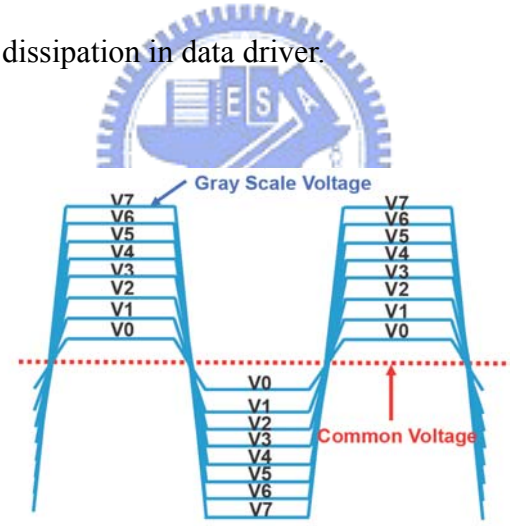


Fig. 2.11 The operation waveform of direct driving method.

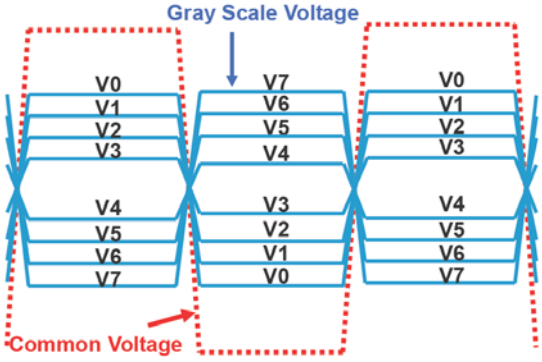


Fig. 2.12 The operation waveform of AC modulation driving method.

2.2.2 Gamma Correction

Gamma correction of liquid crystal displays is involved due to the nonlinearity between luminance and human visual system (HVS). This is because the pupils of the human's eyes would vary automatically for the change of the ambient light. For this reason, a data driver with gamma correction is necessary in TFT-LCD panel. The data driver often is required to compensate for the human visual system's transfer function. Moreover, it must also compensate for the LCD transfer function [9]. Fig. 2.13 shows the operation of the gamma correction for the normally white TN type LCD panel. The gamma correction system is composed of three relationships: luminance vs. HVS brightness, input digital code vs. pixel voltage, and the V-T curve of the NW-TN type liquid crystal. By this system, the relationship between input media codes and brightness in human eye will be more linear.

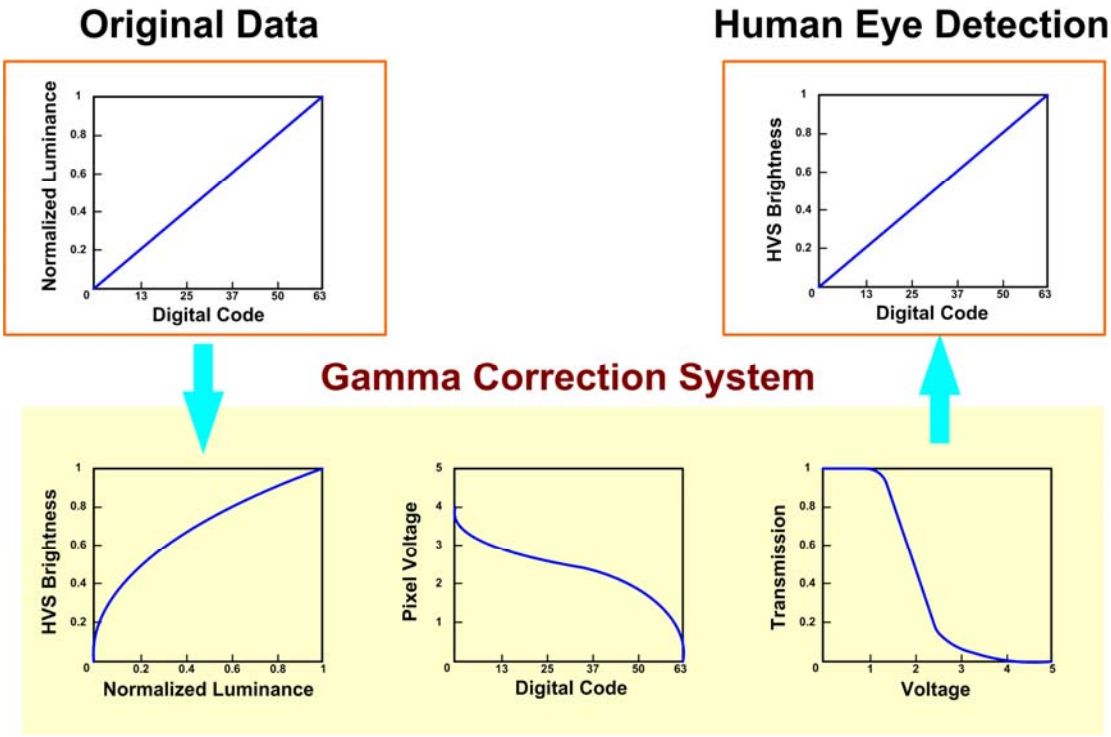


Fig. 2.13 The operation of the gamma correction for the normally white TN type LCD panel. HVS: human visual system.

Furthermore, there are something should be emphasized. In general, the input digital code vs. pixel voltage curve of data driver, in Fig. 2.14, is symmetrical to the common voltage (Vcom) axis. This is because that the permanent deflections of liquid crystal molecules will occur if the DC stress given on the LCD panel sustains a long period. As a result, the LCD panel should be driven by AC (alternating polarity) signal to eliminate the defect on LCD panel.

From previous description, we can get a linear relationship between input media codes and brightness in human eye through a “Gamma Correction Digital to Analog Converter”, which will be particularly discussed in the next chapter.

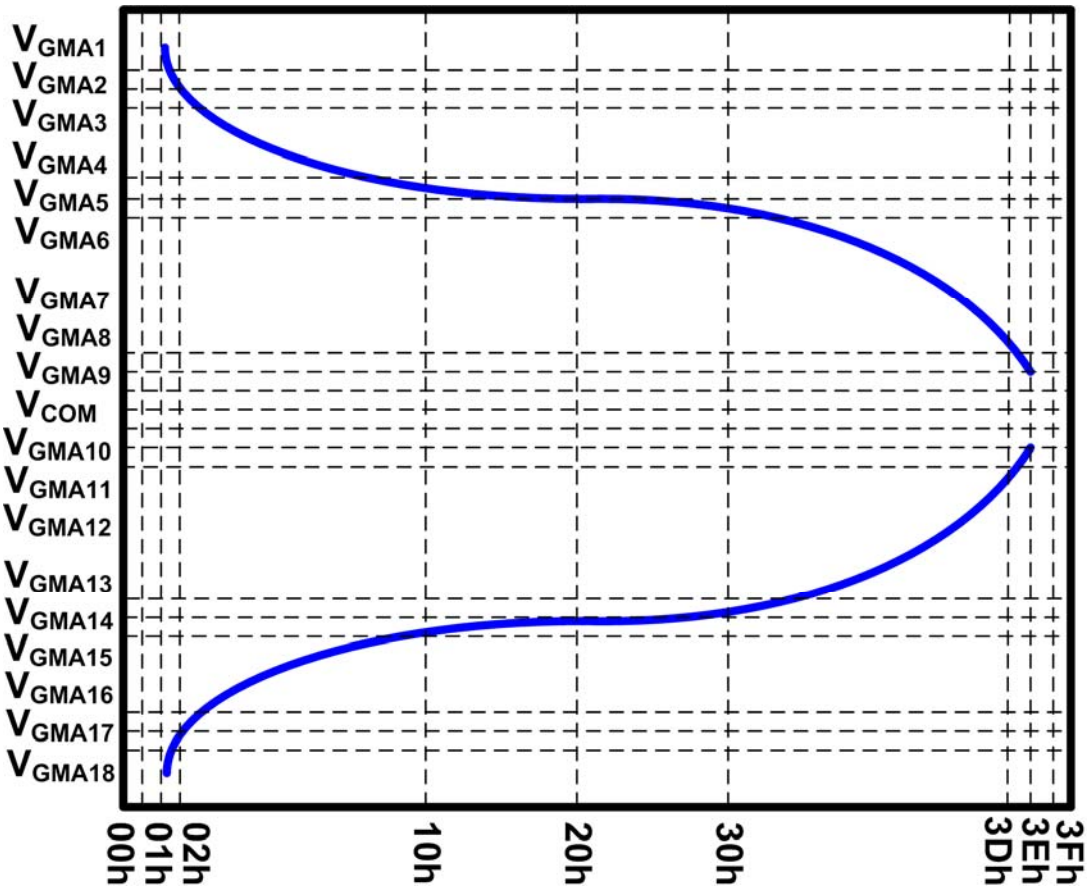


Fig. 2.14 The input digital code vs. pixel voltage curve of data driver in TFT-LCD panel.

2.3 PERIPHERY CIRCUIT BLOCK

The periphery circuit blocks of LCD panel are roughly composed of four parts — display panel, timing control circuit, scan driver circuit and data driver circuit [10]. In Fig. 2.15 is the block diagram of the entire TFT-LCD panel circuits. Display panel is constructed of the active matrix liquid crystals. The operation of the active matrixes is similar to DRAM (dynamic random access memory) which is used to charge and discharge the capacitor of the pixel. Timing controller is responsible for transiting RGB (red, green, and blue) signals to the data driver and controlling the behavior of scan driver. As soon as one voltage level of the scan lines rises, the RGB signals will be transited through the data driver. After a period, the voltage level of this scan line will be disabled and next scan line will be turned on. All voltage levels of those scan lines will be raised in turn. Addressing system, in Fig. 2.16, is composed of scan driver and data driver [7]. These two driver circuits will be further discussed in the following sections.

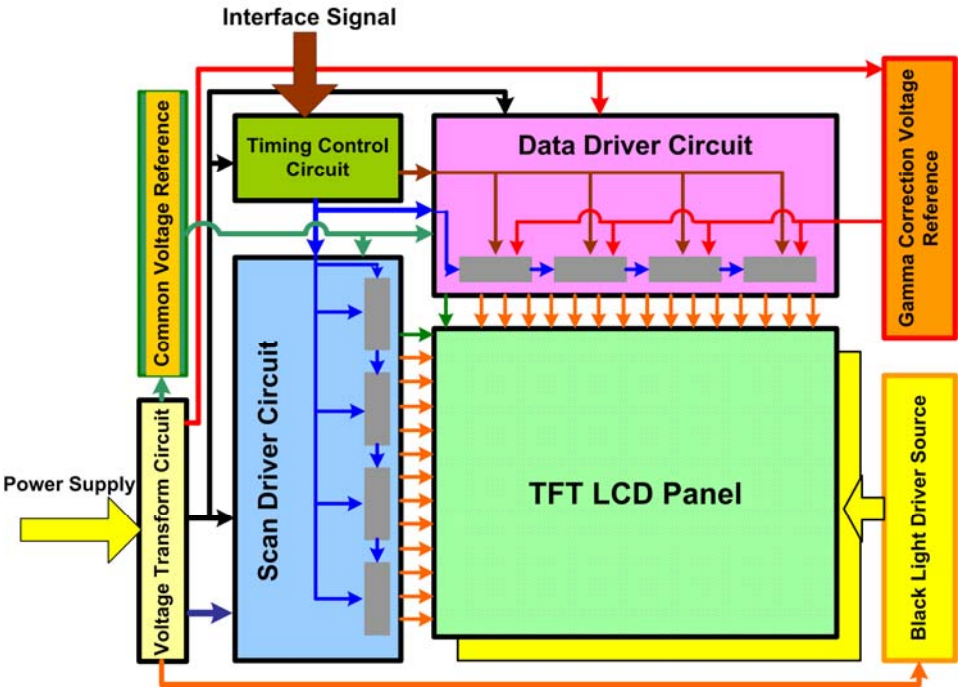


Fig. 2.15 The block diagram of the entire TFT-LCD panel circuits.

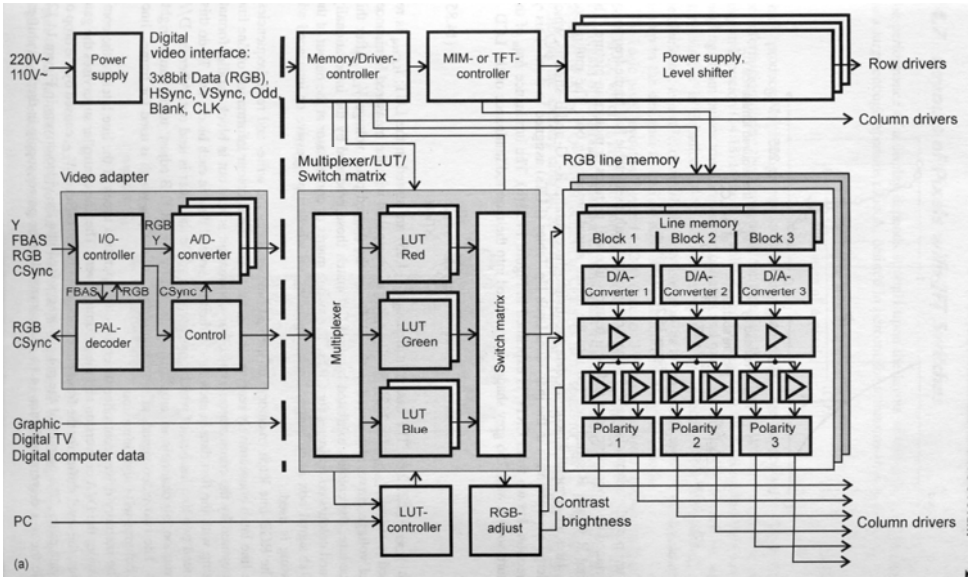


Fig. 2.16 The entire addressing system in detail.

2.3.1 Scan Driver Circuit

Scan driver, shown in Fig. 2.17, consists of shifter register, level shifter, and digital output buffer. Shifter register is used to store digital input signals and transit them to the next stage according to timing clock. Because the turn-on voltage of active matrixes is higher, scan driver should drive the active pixels with a high voltage. The purpose of the level shifter is just to convert the digital signals to a higher level voltage. Finally, since the scan lines can be modeled as RC (resister and capacitor) ladder, the digital output buffer should be used in the last stage for driving the large load [10].

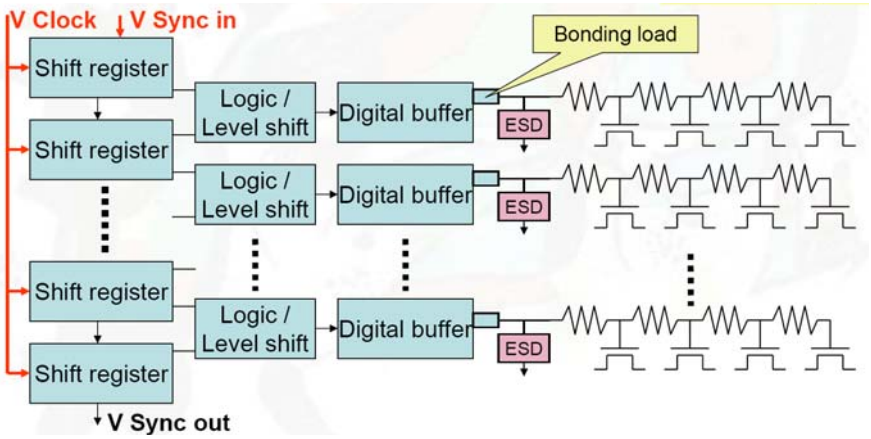


Fig. 2.17 The basic diagram of scan driver circuit.

2.3.2 Data Driver Circuit

Data driver, shown in Fig. 2.18, mainly contains shifter register, data latch, level shifter, digital-to-analog converter (DAC) and analog output buffer [10]. Furthermore, the first three parts classify as digital architectures. The other two parts belong to analog architectures. Shifter register and data latch manage to transit and store the RGB signals. Also, the purpose of level shifter is the same as the one in scan driver. It is applied to translate the RGB signal to a higher level voltage. As implied by the name, digital-to-analog converter is used to convert the digital RGB signal to analog gray level. Its structures can be divided into many types, and there will be much more detailed discussion in the next chapter. As for analog output buffer, its purpose is applied to drive active pixels into a desired gray level. However, The LCD panel usually has large loading, especially in larger panel display or higher resolution display. For this reason, the analog output buffer should enhance the driving capability of the data driver. The corresponding analog output buffer circuit will be described in the later chapter.

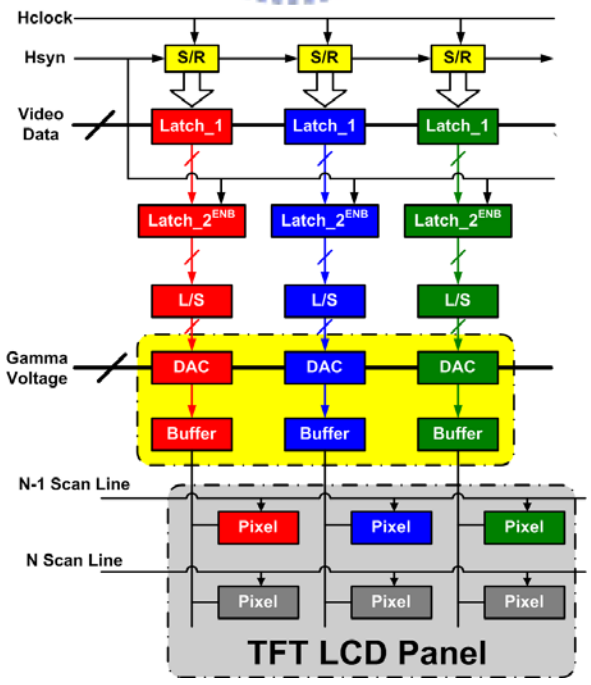


Fig. 2.18 The basic diagram of data driver circuit.

Chapter 3

Novel Digital-to-Analog Converter with Gamma Correction for On-Panel Data Driver

3.1 INTRODUCTION

As last chapter description, we know that there is a nonlinearity relationship between luminance and human visual system. For this reason, a data driver with gamma correction is necessary in TFT-LCD panel. The Data driver mainly contains shifter register, data latch, level shifter, digital-to-analog converter (DAC) and analog output buffer. DAC is used convert the digital RGB signal to analog gray level. It is an important and essential part in the driving system of TFT-LCD panel. In this chapter, the analysis and comparison of the many kinds of DAC circuits will be introduced particularly. Moreover, a novel DAC with gamma correction for on-panel data driver will be proposed and verified in this chapter.

3.2 DIGITAL-TO-ANALOG CONVERTERS [11]-[14]

3.2.1 R-String DAC with Switch Array Decoding

Fig. 3.1 shows a 6-bit R-string DAC circuit. The architecture of this DAC requires no digital decoders. This conventional R-string DAC is familiar in general LCD data drivers, because this architecture is simple and suitable for gamma correction design. However, the area of switch array is becoming larger and larger due to the high resolution DAC. The loading at the output node (Vout) is also becoming larger due to the huge switch array.

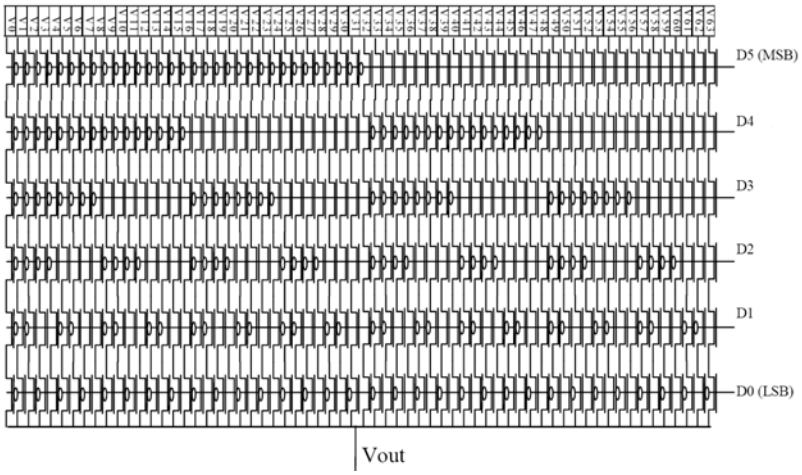


Fig. 3.1 A 6-bit R-string DAC with switch array decoding.

3.2.2 R-String DAC with Binary-Tree Decoding

Fig. 3.2 is a 6-bit R-string DAC with binary-tree decoding. This architecture also requires no digital decoders. In opposition to the R-string DAC with switch array decoding, this R-string DAC with binary-tree decoding has less transistors in the decoding circuits. Nevertheless, the speed of this circuit is limited by the delay through the switch network. The timing skew among the switch-controlling signals can cause large glitches at Vout. This circuit also has larger RC-type loading at the output node (Vout) due to the binary-tree switches.

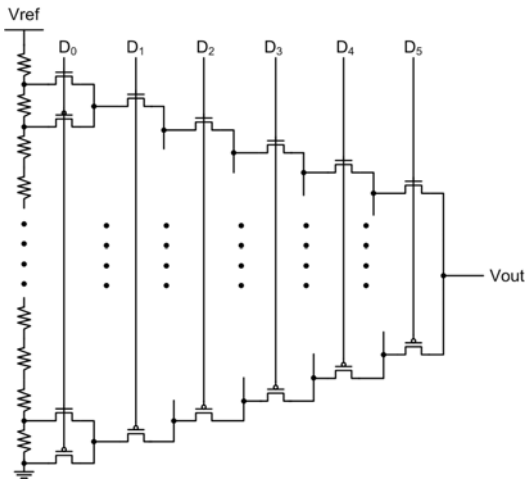


Fig. 3.2 A 6-bit R-string DAC with binary-tree decoding.

3.2.3 R-String DAC with Digital Decoding

In a higher-speed implementation, logic can be used for the decoder. Fig. 3.3 is a 6-bit R-string DAC with digital decoding. The loading of the output node can be reduced by the digital decoder, because the output node is only connected to one column of analog switches. Therefore, the operational speed of DAC using digital decoding is faster than DAC using binary-tree decoding. This architecture is also more suitable for gamma correction design because it is easy to produce different sections in resistor string. However, the area and complexity of decoder are larger and larger due to the high resolution DAC. For this reason, this R-string DAC with digital decoding is not suitable for integrating the data driver in the high resolution TFT-LCD panels.

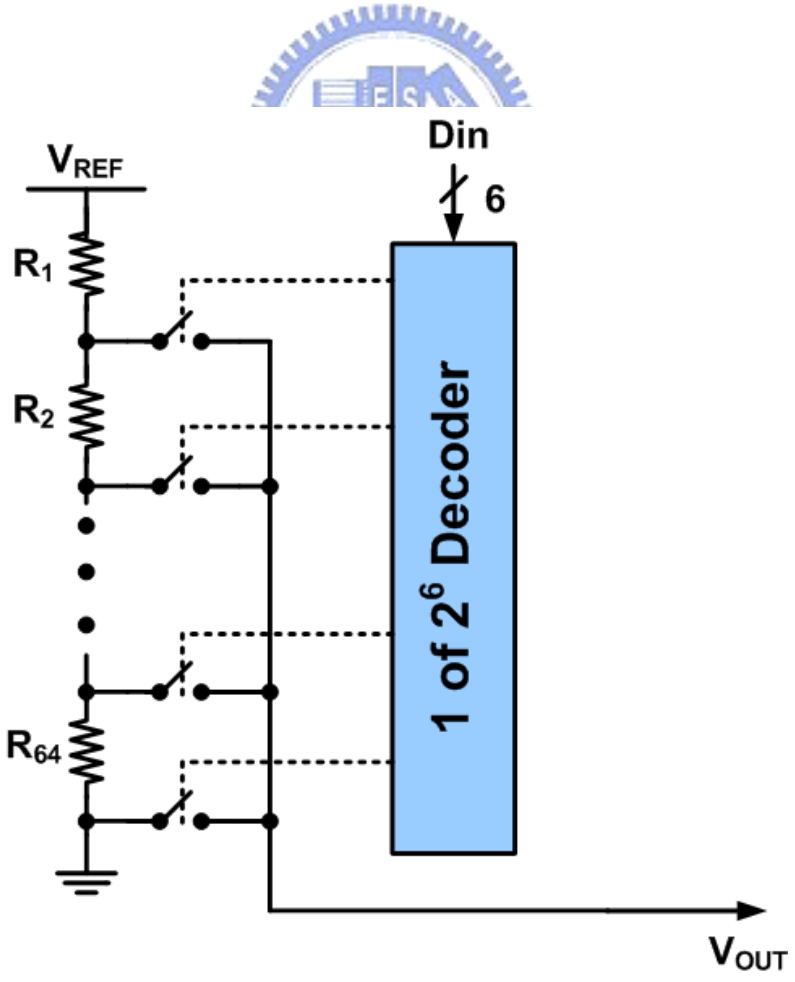


Fig. 3.3 A 6-bit R-string DAC with digital decoding.

3.2.4 Charge-Redistribution DAC

As shown in Fig. 3.4, it is a charge-redistribution DAC. The basic idea here is to simply replace the input capacitor of a switched-capacitor (SC) gain amplifier by programmable capacitor array (PCA) of binary-weighted capacitors. In this circuit, it has two phases. In first phase (ϕ_1), all capacitor bottom plates are connected to a reference voltage and top plates are connected to ground. During second phase (ϕ_2), capacitor bottom plates are connected to a reference voltage or ground according to logic high or logic low in codes. By this operation, the voltage level in output terminal can be determined by a formula which is shown in follow:

$$V_o = V_{ref} \times \frac{C}{2^N C + C_p} \times \sum_{i=0}^{N-1} b_i 2^i \qquad (3 - 1)$$

Where b_i is the bit number in input code, N is the total bit number and C_p is top plate parasitic capacitance. This circuit structure has some advantages better than the resistor-string DAC. First, the process matching for capacitor is better than resistor string. Second, charge-redistribution DAC can save more power because it has no DC path in the circuit. However, it has a big problem in LCD panel application. That is, this method is very difficult to achieve gamma correction. In other word it cannot compensate the inherent characteristic of liquid crystal.

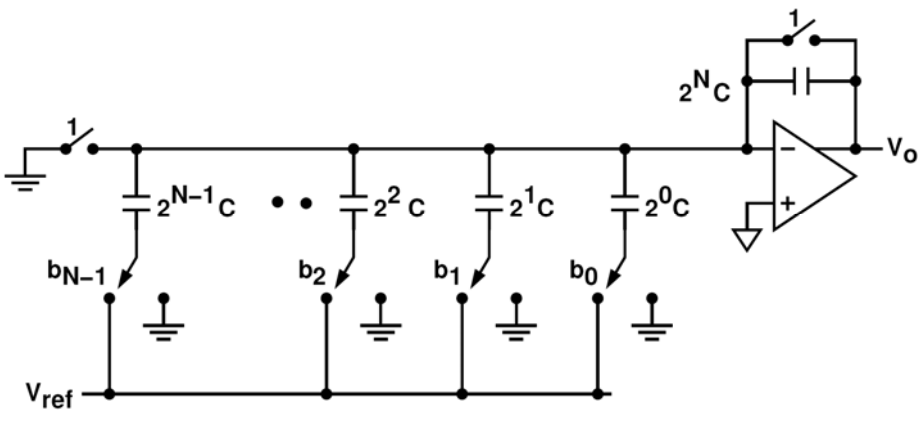


Fig. 3.4 The charge-redistribution DAC.

3.2.5 Multiple R-String DAC [15]

In this variation, a second tapped resistor string is connected between two adjacent nodes of the first resistor string (voltage reference), as shown in Fig. 3.5. In the shown 6-bit example, the three MSBs determine which two adjacent nodes of the first resistor string. The second resistor string linearly interpolates between the two adjacent voltages from the first resistor string. Finally, the output is determined by the lower LSBs. This approach requires only $2x2^{N/2}$ resistors, making it suitable for higher-resolution, low-power applications. This approach also has guaranteed monotonicity. During the signal transformation process, the spikes generated in the DAC (as shown in Fig. 3.6 (a)) are significantly related to the quality of display because the spikes would lead to the unstable displaying and redundant power consumption. Therefore, effective spikes reduction in the DAC becomes a critical topic for display systems. In this architecture, the bit with least signal variation (the higher bits) is arranged closely to output node. By this method, the spikes of the DAC can be reduced obviously, shown in Fig. 3.6 (b).

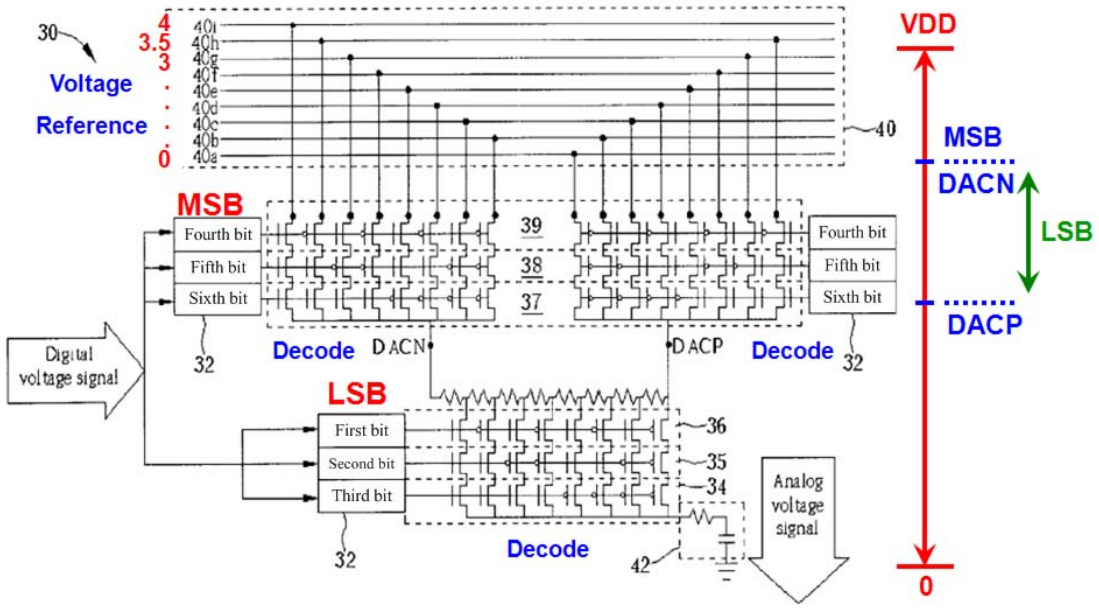
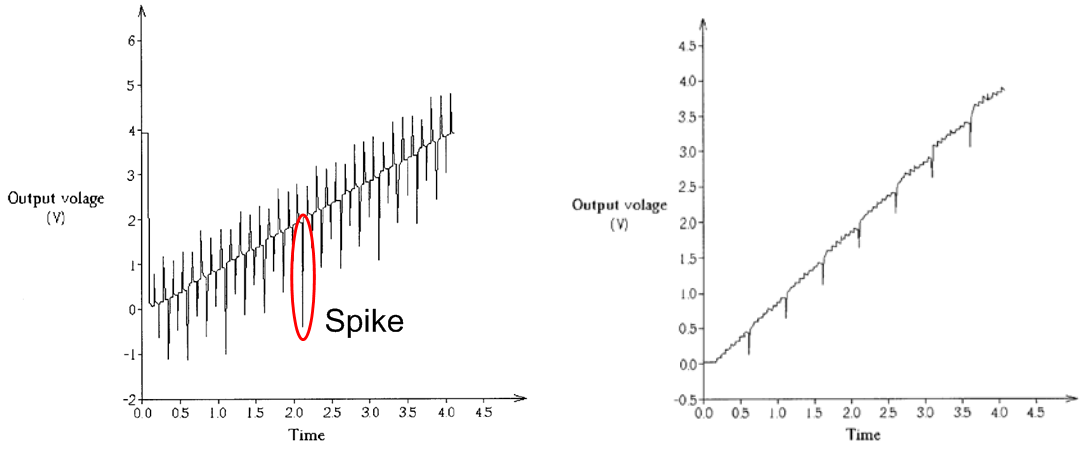


Fig. 3.5 A 6-bit multiple R-string DAC.



(a) (b)

Fig. 3.6 (a) The spikes of the DAC, and (b) the output waveform of the DAC with spikes reduction method.

3.2.6 Resistor-Capacitor Hybrid DAC

The benefits and drawbacks of resistor-string DAC and charge-redistribution DAC have been discussed previously. In order to get their benefits and exclude the drawbacks in the DAC, a hybrid structure has been proposed in Fig. 3.7. In this circuit, the upper bits are adopted in resistor-string architecture and the lower bits are employed the charge-redistribution structure. There are two phases in this circuit operation. In first phase (ϕ_1), all capacitor bottom plates are connected to ground. During second phase (ϕ_2), capacitor bottom plates are connected to a reference voltage V_1 or connected to the other reference voltage V_2 which is according to logic high or logic low in input codes. Furthermore, a formula about this circuit is shown in below:

$$V_o = \frac{V_{ref}}{2^M} \times \sum_{i=0}^{M-1} b_{i+L} 2^i + \frac{1}{2^M} \times \frac{V_{ref}}{2^L} \times \sum_{j=0}^{L-1} b_j 2^j = \frac{V_{ref}}{2^N} \times \sum_{i=0}^{N-1} b_i 2^i \qquad (3 - 2)$$

Where M is the total bit number in resistor-string DAC, L is the total bit number in charge-redistribution DAC and N is the total bit number in this DAC (N = M + L).

This hybrid structure can achieve high performance in operational speed, die area, and power consumption. Besides, it is also suitable in gamma correction DAC.

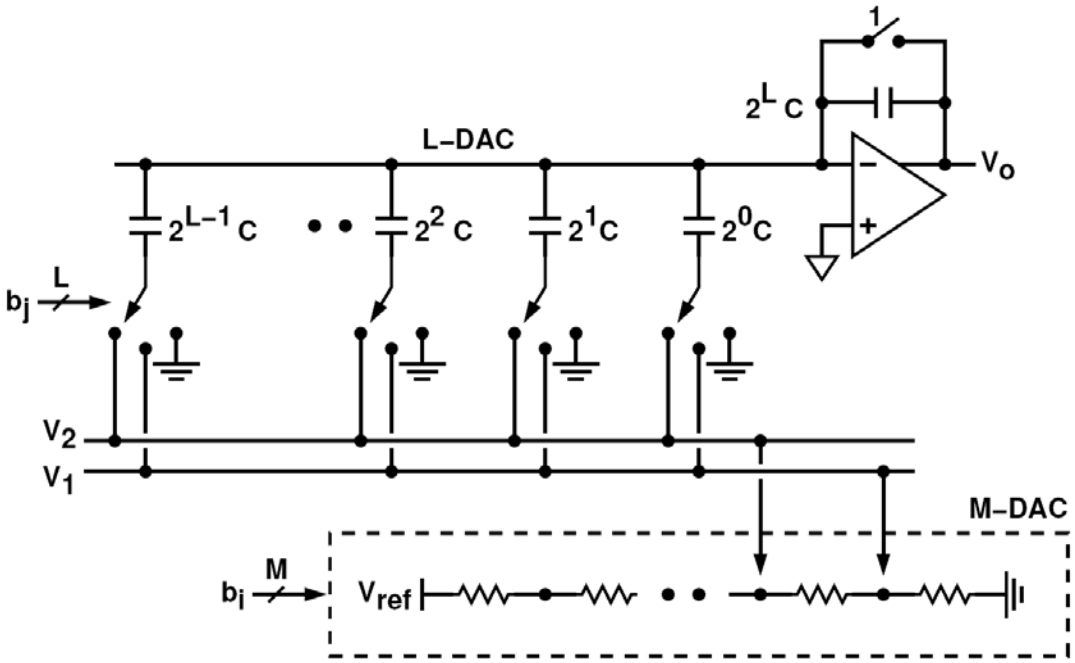


Fig. 3.7 The resistor-capacitor hybrid DAC.

3.2.7 Current-Steering DAC

Current-steering DAC is very similar to resistor-based converter, but is intended for higher-speed application due to the current type. The basic idea is to switch currents to either the output or to ground, as shown in Fig. 3.8. Here, the total output current is sum of the currents which are selected, as shown below:

$$I_o = I \times (b_{N-1} \cdot 2^{N-1} + b_{N-2} \cdot 2^{N-2} + \cdots + b_1 \cdot 2^1 + b_0 \cdot 2^0) \qquad (3 - 3)$$

This output current is converted to a voltage through a resistor (R_F). Although, this circuit has potentially large glitches due to timing skews and the monotonicity in this DAC is not guaranteed. But, we can reduce the glitches and provide the guaranteed monotonicity by using the thermometer decoding method.

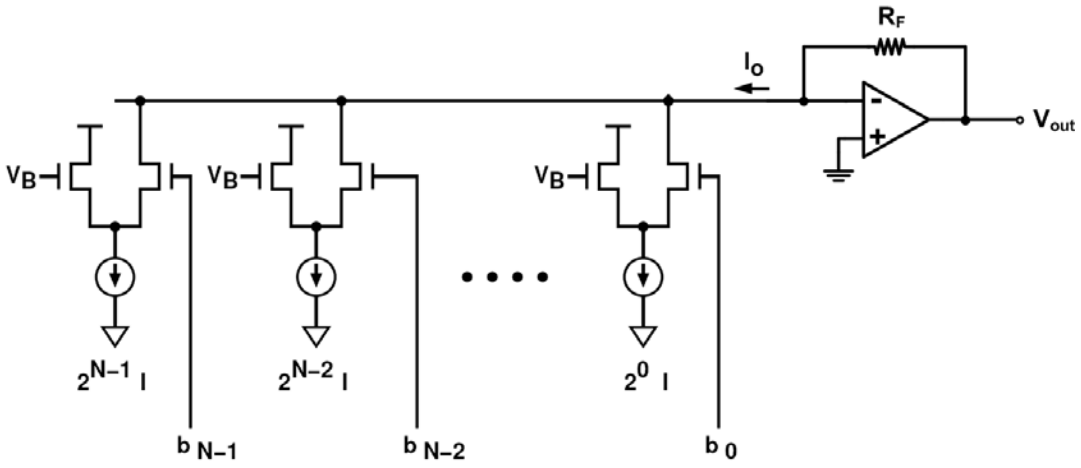


Fig. 3.8 The current-steering DAC.

From previous description and analysis, we can summarize a table about many kinds of the DAC circuits, as shown in Table 3.1. In this table, we can clearly find the characteristics of those DAC, like: suitable for gamma correction design, operation speed, power consumption, area, and the complexity of design and layout.

Table 3.1

The comparisons of many kinds of the digital-to-analog converter circuits.

Circuit Type	γ Correction	Speed	Power	Area	Complexity
R-DAC with switch array decoder	Best	Poor	Normal	Poor	Easy
R-DAC with binary-tree decoder	Best	Normal	Normal	Normal	Easy
R-DAC with digital decoder	Best	Good	Normal	Normal	Medium
Charge-redistribution DAC	Poor	Good	Best	Normal	Medium
Multiple R-DAC	Good	Good	Poor	Best	Medium
Hybrid R-C DAC	Good	Good	Good	Good	Hard
Current-steering DAC	Poor	Best	Poor	Normal	Hard

3.3 NOVEL FOLDED R-STRING DAC WITH GAMMA CORRECTION

3.3.1 Design of Gamma Correction

From previous chapters, we know that there is a nonlinearity relationship between luminance and human visual system. For this reason, the gamma correction design is necessary in TFT-LCD panel. The display transfer function is shown in Fig. 3.9. The nonlinearity between gray level domain and luminance domain can be corrected by gamma correction design. For a 6-bit gamma correction design, the transform function about this system can be express as following:

$$\frac{T(GL)-T_{\min}}{T_{\max}-T_{\min}}=(GL/63)^{\gamma} \tag{3 - 4}$$

$$T(GL)=(T_{\max}-T_{\min})(GL/63)^{\gamma}+T_{\min} \tag{3 - 5}$$

$$L(GL)=T(GL)\cdot K_{backlight} \tag{3 - 6}$$

$$L(GL)=(L_{\max}-L_{\min})(GL/63)^{\gamma}+L_{\min} \tag{3 - 7}$$

From above formula, the transform function between transmission and gray level is shown in equation (3 - 5).

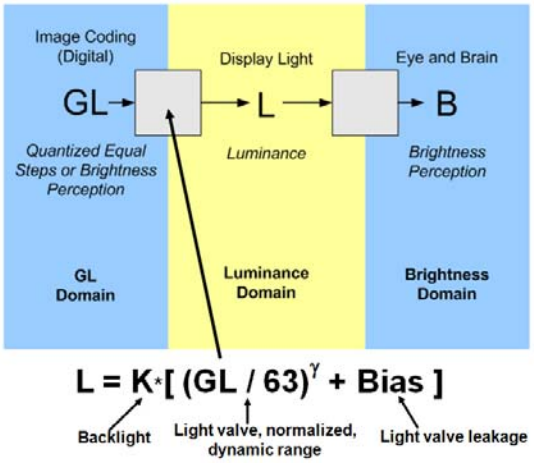


Fig. 3.9 The transform function of display system.

Fig. 3.10 shows a voltage versus transmission curve of the liquid crystal in CPT process. From this figure, we can know this liquid crystal is a normally white TN-type liquid crystal. We can calculate the pixel voltage with gamma value of 2.2 by using the transform function in equation (3 - 5) and the V-T curve of this liquid crystal. The pixel voltage corresponded to each gray level is shown in Table 3.2.

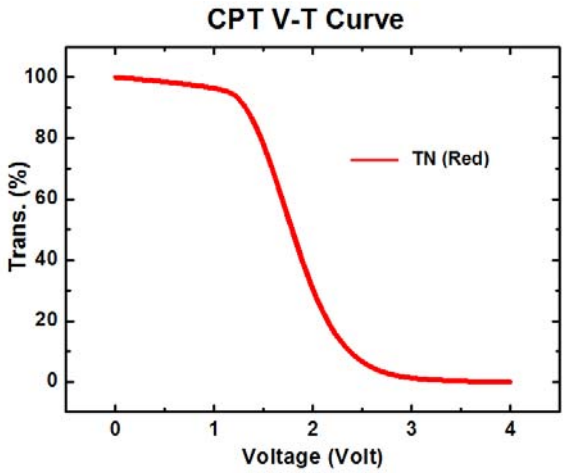


Fig. 3.10 The voltage vs. transmission curve of the liquid crystal in CPT process.

Table 3.2

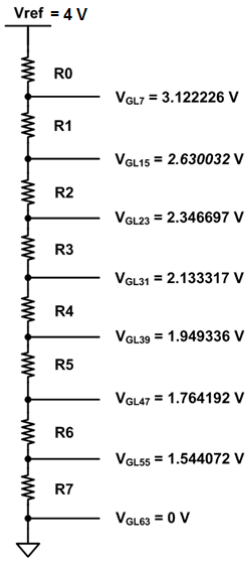
The pixel voltage corresponded to each gray level with gamma of 2.2.

GL	T%	Vp (V)	GL	T%	Vp (V)	GL	T%	Vp (V)	GL	T%	Vp (V)
0	0	***4***	16	4.903597	***2.5879***	32	22.53101	***2.109766***	48	54.97706	***1.74***
1	0.011001	***3.9***	17	5.60323	***2.548154***	33	24.10913	***2.086728***	49	57.52838	***1.71465***
2	0.050549	***3.758902***	18	6.354045	***2.510975***	34	25.74568	***2.063205***	50	60.14296	***1.688701***
3	0.123344	***3.613312***	19	7.156632	***2.47524***	35	27.44104	***2.04***	51	62.82105	***1.66249***
4	0.232264	***3.457736***	20	8.011554	***2.441479***	36	29.19553	***2.017145***	52	65.5629	***1.635021***
5	0.379476	***3.327016***	21	8.919351	***2.408688***	37	31.00949	***1.994362***	53	68.36876	***1.606405***
6	0.56674	***3.217753***	22	9.88054	***2.376906***	38	32.88325	***1.971823***	54	71.23888	***1.576317***
7	0.795548	***3.122226***	23	10.89562	***2.346697***	39	34.81713	***1.949336***	55	74.17349	***1.544072***
8	1.067207	***3.035698***	24	11.96508	***2.317437***	40	36.81144	***1.926691***	56	77.17283	***1.50949***
9	1.382879	***2.959477***	25	13.08937	***2.289892***	41	38.86649	***1.90363***	57	80.23715	***1.471855***
10	1.743616	***2.892731***	26	14.26895	***2.261672***	42	40.98257	***1.881031***	58	83.36666	***1.42963***
11	2.150377	***2.83195***	27	15.50426	***2.234607***	43	43.16	***1.858031***	59	86.56159	***1.382006***
12	2.604051	***2.774818***	28	16.79571	***2.208712***	44	45.39904	***1.834985***	60	89.82217	***1.324149***
13	3.105462	***2.723289***	29	18.14372	***2.182949***	45	47.69999	***1.81194***	61	93.14862	***1.249646***
14	3.655379	***2.675385***	30	19.54869	***2.157501***	46	50.06313	***1.788369***	62	96.54116	***1.1297***
15	4.25453	***2.630032***	31	21.01099	***2.133317***	47	52.48873	***1.764192***	63	100	***0***

As shown in the Table 3.2, we can find each target pixel value. The voltage-dividing method of the resistor string is adopted. First, we divide this R-string ladder into 8 interval values fitting to the target pixel value. Then, we divide each section of R-string into 8 the same sub-interval R-string. The value of each resistor in this R-string is designed in the Table 3.3 and the simulation result of the voltage divider of R-string is shown in Fig. 3.11.

Table 3.3

The resistance values of R-string for gamma correction design.



R0	*43.9k*	R1	*24.6k*	R2	*14.15k*	R3	*10.65k*
R00	5.4875k	R10	3.075k	R20	1.76875k	R30	1.33125k
R01	5.4875k	R11	3.075k	R21	1.76875k	R31	1.33125k
R02	5.4875k	R12	3.075k	R22	1.76875k	R32	1.33125k
R03	5.4875k	R13	3.075k	R23	1.76875k	R33	1.33125k
R04	5.4875k	R14	3.075k	R24	1.76875k	R34	1.33125k
R05	5.4875k	R15	3.075k	R25	1.76875k	R35	1.33125k
R06	5.4875k	R16	3.075k	R26	1.76875k	R36	1.33125k
R07	5.4875k	R17	3.075k	R27	1.76875k	R37	1.33125k
R4	*9.2k*	R5	*9.25k*	R6	*11k*	R7	*77.2k*
R40	1.15k	R50	1.15625k	R60	1.375k	R70	9.65k
R41	1.15k	R51	1.15625k	R61	1.375k	R71	9.65k
R42	1.15k	R52	1.15625k	R62	1.375k	R72	9.65k
R43	1.15k	R53	1.15625k	R63	1.375k	R73	9.65k
R44	1.15k	R54	1.15625k	R64	1.375k	R74	9.65k
R45	1.15k	R55	1.15625k	R65	1.375k	R75	9.65k
R46	1.15k	R56	1.15625k	R66	1.375k	R76	9.65k
R47	1.15k	R57	1.15625k	R67	1.375k	R77	9.65k

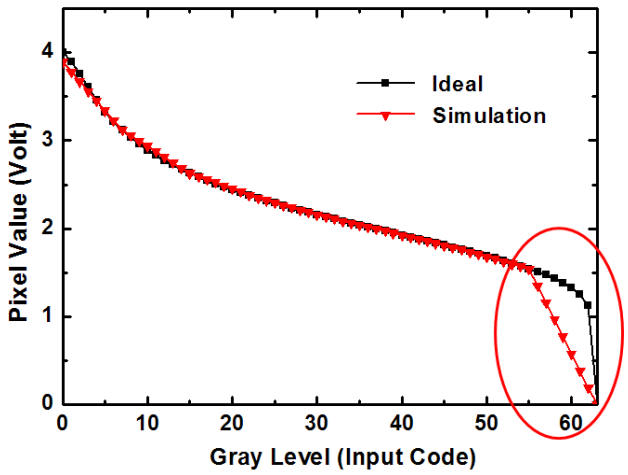
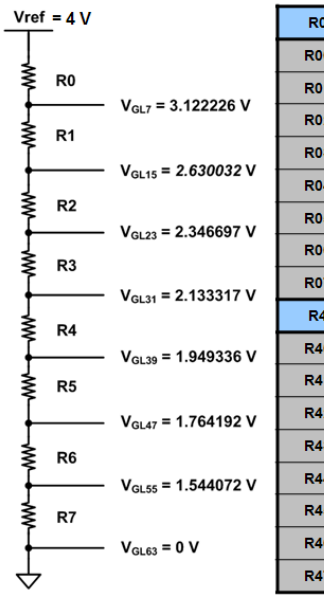


Fig. 3.11 The gray level vs. pixel value curve in the voltage divider of R-string.

From above simulation result, we can see that the pixel values of last 8 bits are not fit to the ideal values. This is because of the same interval in the last 8-bit section is not suitable for this design. The modified R-string ladder is designed in Table 3.4 and the simulation result of the voltage divider of R-string is shown in Fig. 3.12. As shown in the simulation result, we can find that all pixel values are fitter to the ideal values due to the modified R-string ladder.

Table 3.4

The modified resistance values of R-string for gamma correction design.



R0	43.9k	R1	24.6k	R2	14.15k	R3	10.65k
R00	5.4875k	R10	3.075k	R20	1.76875k	R30	1.33125k
R01	5.4875k	R11	3.075k	R21	1.76875k	R31	1.33125k
R02	5.4875k	R12	3.075k	R22	1.76875k	R32	1.33125k
R03	5.4875k	R13	3.075k	R23	1.76875k	R33	1.33125k
R04	5.4875k	R14	3.075k	R24	1.76875k	R34	1.33125k
R05	5.4875k	R15	3.075k	R25	1.76875k	R35	1.33125k
R06	5.4875k	R16	3.075k	R26	1.76875k	R36	1.33125k
R07	5.4875k	R17	3.075k	R27	1.76875k	R37	1.33125k
R4	9.2k	R5	9.25k	R6	11k	R7	77.2k
R40	1.15k	R50	1.15625k	R60	1.375k	R70	2.96k
R41	1.15k	R51	1.15625k	R61	1.375k	R71	2.96k
R42	1.15k	R52	1.15625k	R62	1.375k	R72	2.96k
R43	1.15k	R53	1.15625k	R63	1.375k	R73	2.96k
R44	1.15k	R54	1.15625k	R64	1.375k	R74	2.96k
R45	1.15k	R55	1.15625k	R65	1.375k	R75	2.96k
R46	1.15k	R56	1.15625k	R66	1.375k	R76	2.96k
R47	1.15k	R57	1.15625k	R67	1.375k	R77	56.48k

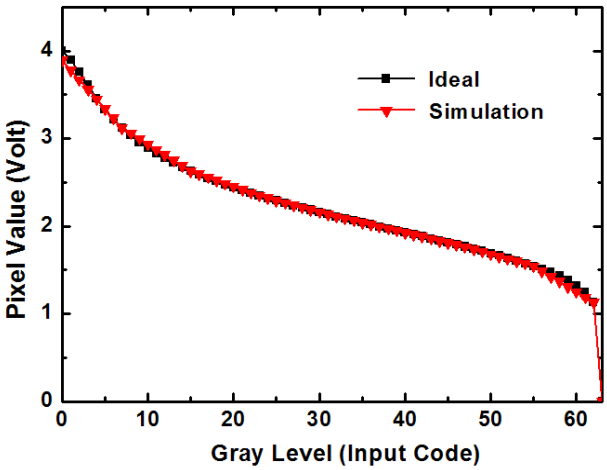


Fig. 3.12 The GL vs. pixel value curve in the modified voltage divider of R-string.

3.3.2 Circuit Description

From above discussions, we know that the R-string DAC with digital decoding is a valid technique for reducing the loading of the output node. It also has a simple structure for layout floorplan and suitable for gamma correction design. But this architecture has too large area of the decoder in high resolution DAC. For this reason, we have proposed a new architecture to reduce the area of the decoder. The transistor number of the decoder is not linearly increased but exponentially increased with the growing of the bit number. Therefore, we divided a decoder into two decoders to reduce the area of the decoder. The folded R-string DAC with segmented digital decoders is shown in Fig. 3.13. The area of the decoders in the 6-bit DAC can be reduced to about one sixth by using this segmented architecture.

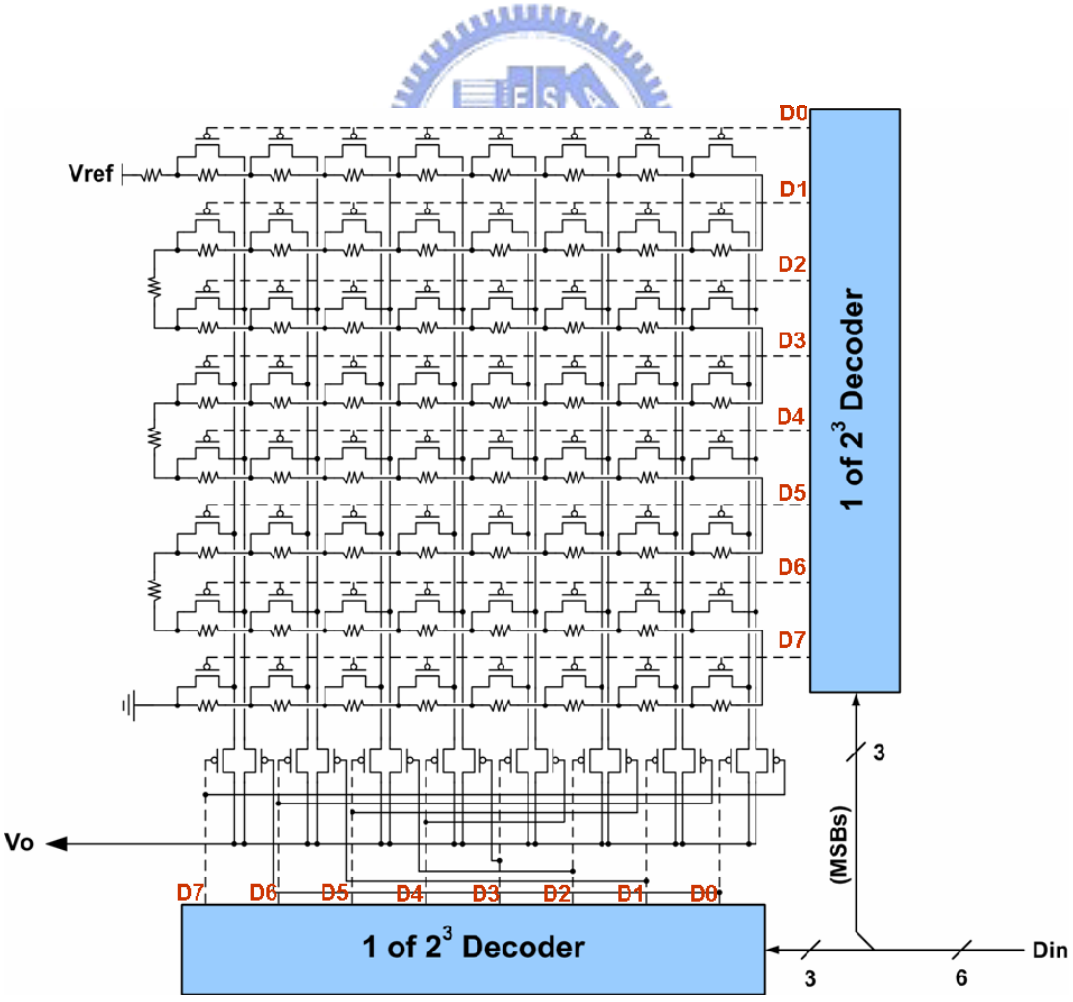


Fig. 3.13 The folded R-string DAC with segmented digital decoders.

In this work, we propose a novel digital-to-analog converter with gamma correction for on-panel data driver in LTPS technology. The purpose of low dimension and low complexity can be achieved by this architecture of the folded R-string DAC with segmented digital decoders. This DAC is composed of folded R-string, switch array, two segmented decoders, and reordering decoding circuit. The operating illustration of this 6-bit folded R-string DAC with segmented digital decoders is shown in Fig. 3.14. For example, when the input signal Din is 000000, this input signal will be segmented into two parts (MSBs and LSBs). The MSBs (000) and the LSBs (000) of the input signal are assigned to high-bit decoder and low-bit decoder, respectively. The output signal (D0) of the low-bit decoder will turn on the switches Ms08, Ms18, and their signal paths because its input is 000. In the same way, the output of high-bit decoder will turn on the top row of the switch array.

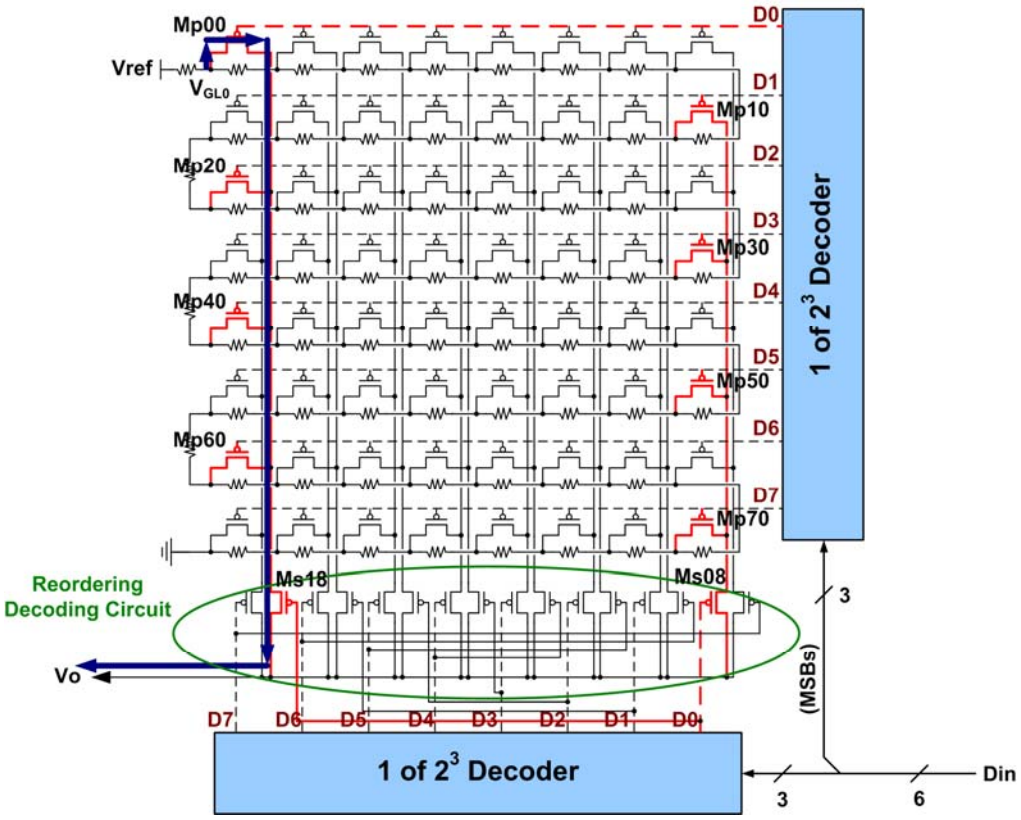


Fig. 3.14 The operation illustration of the 6-bit folded R-string DAC with segmented digital decoders.

With a resistor-string approach, the DAC has guaranteed monotonicity since any section on the resistor string must has a low voltage than its upper, neighbor section. It also has higher accuracy because the accuracy of the R-string DAC is dependent on the ratio of resistors, not dependent on absolute resistor values [16]. Furthermore, the area of the R-string DAC can be reduced by using the folded R-string and the segmented digital decoders. The reordering decoding circuit can simplify the decoder circuit. The partial decoding function is replaced by the signal paths routing of the reordering decoding circuit. For this reason, the fundamental decoders can be used for the segmented digital decoders. Fig. 3.15 is shown that the transistors of the decoders can be decreased from 780 to 124 in 6-bit DACs. The area of the R-string DAC can be effectively reduced to about one sixth by using this proposed architecture. This proposed 6-bit folded R-string DAC with segmented digital decoders is also more suitable for gamma correction design in TFT-LCD panel.

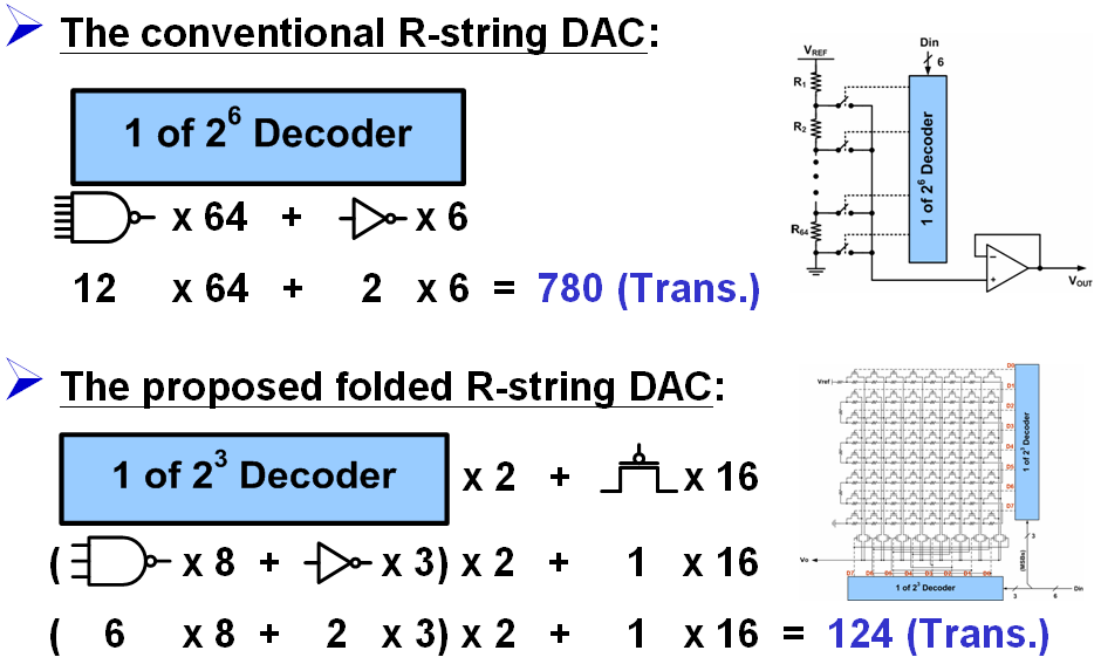


Fig. 3.15 The comparison of the transistors number of the decoders between the conventional and proposed 6-bit R-string DAC.

3.3.3 Simulation and Verification

According to previous sections in this chapter, we can get whole architecture of this 6-bit R-string DAC (as shown in Fig. 3.13) and all resistance values of R-string for gamma correction design (as shown in Table 3.4). This proposed 6-bit folded R-string DAC with segmented digital decoders has four voltage sources: V_{DD} = 6 V, V_{SS} = -2 V, V_{ref} = 4 V, and GND = 0 V. The first two voltage sources are used for digital decoders. The rest of voltage sources are used for R-string ladder. This proposed DAC has been successfully verified in 8-μm LTPS technology. The simulation result of this DAC, assigned a series of digital input codes from 000000 (0) to 111111 (63) at 100-kHz operation frequency, is shown in Fig. 3.16. The average power consumption of the proposed DAC is 82.047 μW and the average current through R-string is 20.007 μA. From above results, we know that the power consumption is dominated by the R-string ladder in this proposed 6-bit DAC.

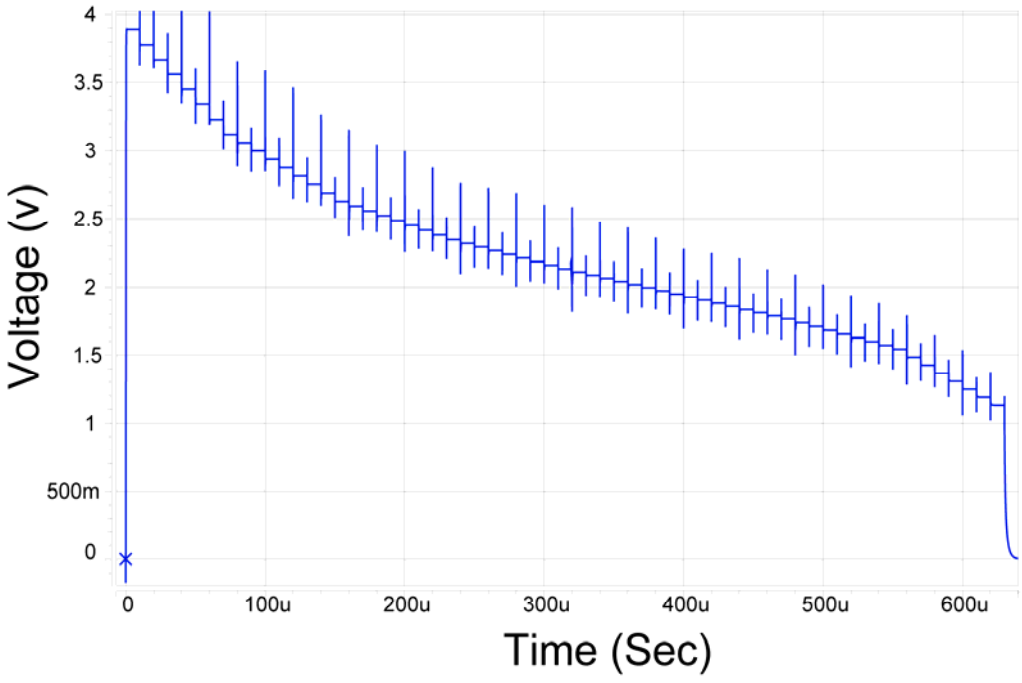


Fig. 3.16 The simulation result of this 6-bit folded R-string DAC with segmented digital decoders in 8-μm technology.

Table 3.5 and Fig. 3.17 show the voltage values and the GL vs. output voltage curves in ideal condition, R-string ladder, and this proposed DAC.

Table 3.5
The voltage values in ideal condition, R-string ladder, and this proposed DAC corresponded to each gray level. Unit: volt.

GL	Ideal	R-String	R-DAC	GL	Ideal	R-String	R-DAC	GL	Ideal	R-String	R-DAC	GL	Ideal	R-String	R-DAC
0	4	3.89	3.89	16	2.588	2.594	2.594	32	2.11	2.111	2.111	48	1.74	1.737	1.737
1	3.9	3.78	3.781	17	2.548	2.559	2.559	33	2.087	2.088	2.088	49	1.715	1.709	1.71
2	3.759	3.671	3.671	18	2.511	2.524	2.524	34	2.063	2.065	2.065	50	1.689	1.682	1.682
3	3.613	3.561	3.561	19	2.475	2.488	2.488	35	2.04	2.042	2.042	51	1.662	1.654	1.654
4	3.458	3.451	3.451	20	2.441	2.453	2.453	36	2.017	2.019	2.019	52	1.635	1.627	1.627
5	3.327	3.341	3.341	21	2.409	2.417	2.417	37	1.994	1.996	1.996	53	1.606	1.599	1.599
6	3.218	3.232	3.232	22	2.377	2.382	2.382	38	1.972	1.973	1.973	54	1.576	1.572	1.572
7	3.122	3.122	3.122	23	2.347	2.347	2.347	39	1.949	1.95	1.95	55	1.544	1.544	1.544
8	3.036	3.06	3.06	24	2.317	2.32	2.32	40	1.927	1.926	1.926	56	1.509	1.485	1.485
9	2.959	2.999	2.999	25	2.29	2.293	2.293	41	1.904	1.903	1.903	57	1.472	1.426	1.426
10	2.893	2.937	2.937	26	2.262	2.267	2.267	42	1.881	1.88	1.88	58	1.43	1.367	1.367
11	2.832	2.876	2.876	27	2.235	2.24	2.24	43	1.858	1.857	1.857	59	1.382	1.308	1.308
12	2.775	2.814	2.814	28	2.209	2.213	2.213	44	1.835	1.834	1.834	60	1.324	1.248	1.248
13	2.723	2.753	2.753	29	2.183	2.187	2.187	45	1.812	1.811	1.811	61	1.25	1.189	1.189
14	2.675	2.691	2.691	30	2.158	2.16	2.16	46	1.788	1.788	1.788	62	1.13	1.13	1.13
15	2.63	2.63	2.63	31	2.133	2.134	2.134	47	1.764	1.764	1.765	63	0	0	0.0052

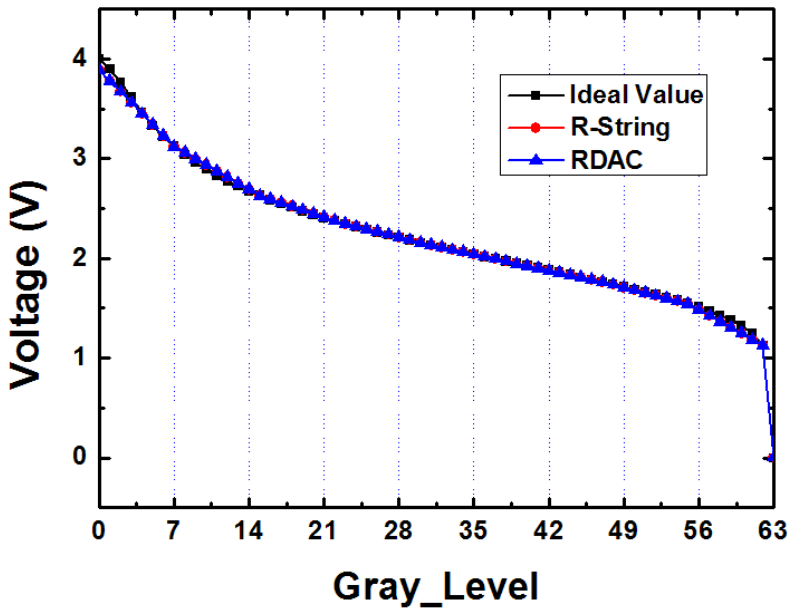
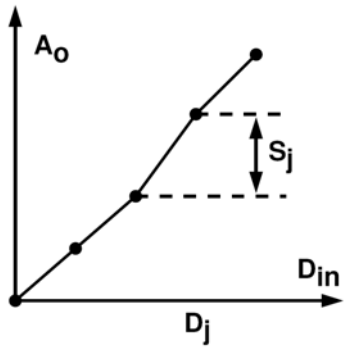


Fig. 3.17 The GL vs. output voltage curves in ideal condition, R-string ladder, and this proposed DAC.

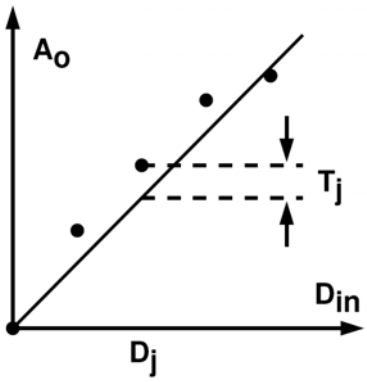
The differential non-linearity (DNL) and integral non-linearity (INL) are important specification of the data converter circuits except offset error and gain error. The definitions of DNL and INL are shown in Fig. 3.18 and Fig. 3.19 [17]. "Δ" is defined as least significant bit (LSB) in the data converter. However, there is a thing should be emphasized. The LSB is not a constant value in the nonlinear system, like this proposed DAC with gamma correction design. For this reason, if the difference between the bit itself and adjacent upper bit is named Diff (N+1) and that between the bit itself and adjacent lower bit is named Diff (N-1), the LSB in nonlinear system is defined as the less one among Diff (N+1) and Diff (N-1). From the simulation result in Table 3.5, we can find that the DNL and INL in this proposed 6-bit DAC almost equal to 0.



$$DNL(D_j) = \frac{S_j - \Delta}{\Delta} \quad (LSB)$$

$$\Delta = \frac{A_{FS}}{2^N}$$

Fig. 3.18 The definition of the differential non-linearity.



$$INL(D_j) = \frac{T_j}{\Delta} \quad (LSB)$$

$$\Delta = \frac{A_{FS}}{2^N}$$

Fig. 3.19 The definition of the integral non-linearity.

This proposed architecture also has been successfully verified in 3-μm LTPS technology. The simulation results are shown in Fig. 3.20 and Fig. 3.21. Based on Fig. 3.20, we can find that the spikes of this DAC can be obviously reduced by the advanced technology. This is because the clock feed-through can be greatly reduced due to the shorter length dimension of transistor.

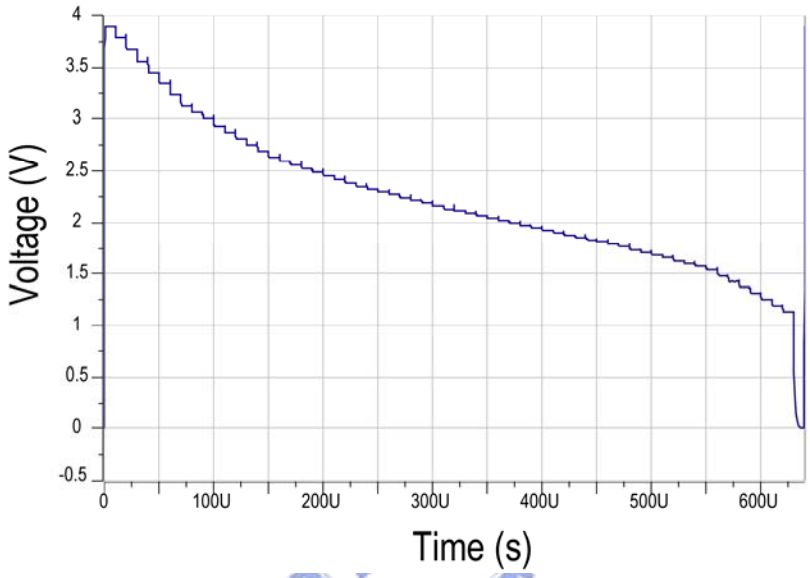


Fig. 3.20 The simulation result of this 6-bit folded R-string DAC with segmented digital decoders in 3-μm technology.

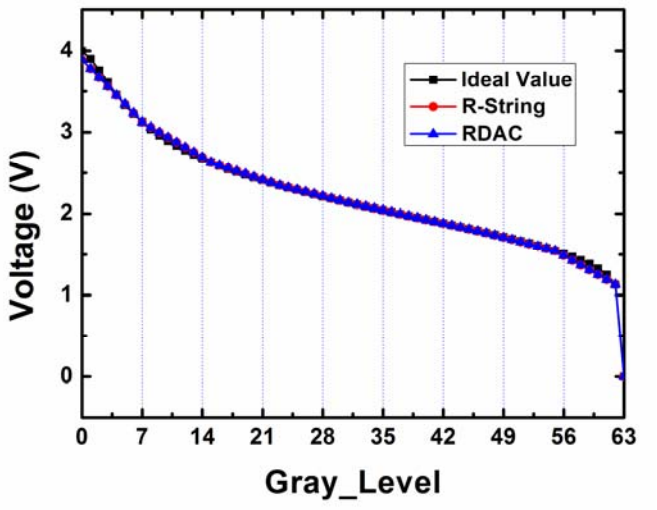


Fig. 3.21 The GL vs. output voltage curves in ideal condition, R-string ladder, and this proposed DAC in 3-μm technology.

In summary, a novel 6-bit folded R-string DAC with gamma correction has been successfully verified in 8-μm and 3-μm LTPS technology. By using the folded R-string and segmented digital decoders, the area of the R-string DAC can be effectively reduced to about one sixth. Furthermore, this architecture is also more suitable for gamma correction design and many kinds of LTPS process. Although, there is only a discussion for normally white TN-type liquid crystal in this chapter. This proposed architecture is also suitable for many kinds of gamma value and normally white (or black) TFT-LCD panel by modifying the R-string value and the decoder architecture.

Chapter 4
On-Panel Analog Output Buffer for Data Driver with Consideration of Device Characteristic Variation

4.1 INTRODUCTION

Based on chapter 1, we know that the LTPS TFTs have been widely investigated as a material for portable systems, such as digital camera, mobile phone, personal digital assistants (PDAs), notebook, and so on, because the electron mobility of LTPS TFTs is about 100 times larger than that of the conventional amorphous silicon TFTs. Furthermore, LTPS can achieve slim, compact, and high-resolution display by integrating the driving circuits on peripheral area of display. If the mobility of poly-Si TFTs is further increased, this technology will become more suitable for realization of SoP applications that will integrate with memory, CPU, and display [18], [19].

At present, LTPS technology has a tendency towards integrating all control circuits and driver circuits on the glass substrate [20], [21]. In general, the LCD driver contains gate driver, data driver, and DC-DC converter. The data driver is composed of shifter registers, latch, level shifters, D/A converters, and analog output buffer. The last two components belong to the analog circuit region. A novel 6-bit DAC has been proposed in last chapter. However, the analog output buffer is also a critical design to achieve the low power dissipation, high resolution, and large output swing on LCD panel. For this reason, an on-panel analog output buffer for data driver with consideration of device characteristic variation will be proposed in this chapter.

4.2 DEVICE CHARACTERISTIC VARIATION IN LTPS TECHNOLOGY

Although using LTPS process can enlarge poly-grain size to improve the device performance, it usually accompanies a random device-to-device variation on LCD panel. The harmful effects of irregular grain boundaries, gate-insulator interface defects, and incomplete ion-doping activation in thin poly-silicon channels result in the variation on electrical characteristics of LTPS TFTs. Fig. 4.1 shows the variation on threshold voltage (V_{TH}) of 120 LTPS n-type TFTs in different locations on LCD panel. The V_{TH} of LTPS n-type TFTs in different panel locations has wide distribution from 0.75 V to 2.15 V [22]. The device characteristic variations of LTPS p-type TFTs in different gate bias are shown in Fig. 4.2 [23]. Based on these two figures, the device characteristic variations in LTPS technology are quite large compared with CMOS technology.

However, in spite of many advantages of LTPS technology, main applications are still limited to small size displays. The reason is that the poly-Si TFTs have poor uniformity and suffer from large variations on the device characteristics due to the narrow laser process window for producing large-grained poly-Si thin film. The random grain boundaries and trap density exist in the channel region. This leads to some problems in real product applications such as non-uniformity brightness in panel, error reading in digital circuits, current gain mismatching in analog circuits, and so on [24]. As a result, the device characteristic variation becomes a very serious problem for analog circuit design in LTPS technology [25].

In this work, a class-A analog output buffer with suppressing device variation method has been proposed. By this proposed method, the manufacturing yield of the circuit can be increased and the performance of the on-panel analog output buffer also can be maintained effectively.

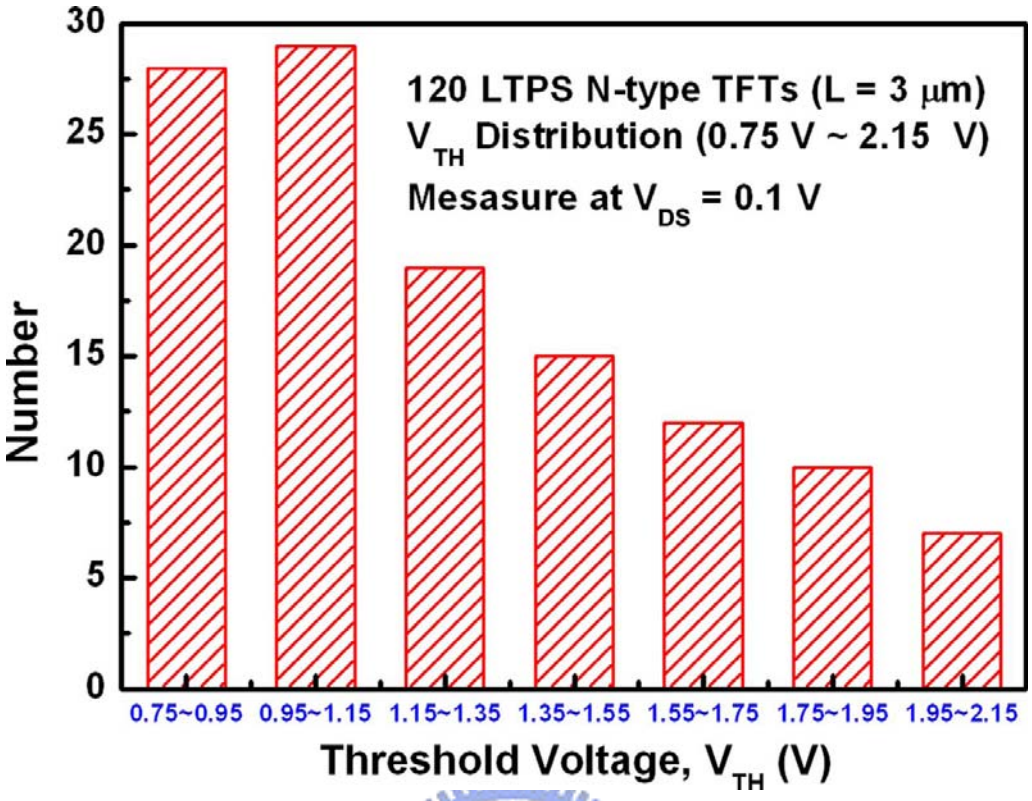


Fig. 4.1 Variation on threshold voltage (V_{TH}) of 120 LTPS n-type TFTs in different locations on LCD panel.

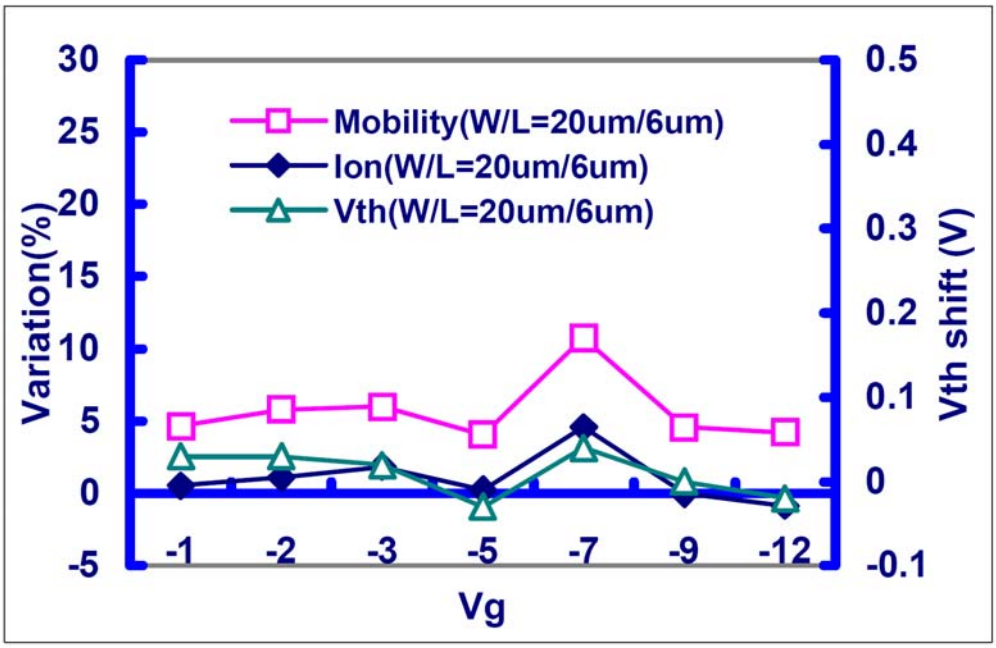


Fig. 4.2 The device characteristic variations of LTPS p-type TFTs in different gate bias.

4.3 ON-PANEL ANALOG OUTPUT BUFFER

4.3.1 Source Follower Analog Output Buffer [26]

The conventional source follower output buffer has been integrated on the glass substrate for data driver. However, there are some drawbacks in such output buffer including the lower output swing and the higher input offset voltage. Fig. 4.3 shows the circuit of the conventional source follower output buffer and its output waveforms at different input voltages. From this figure, we can find that the output swing of the source follower output buffer is limited to V_{DD}–V_{th}. Besides, there is always an input offset voltage in the source follower output buffer due to the threshold voltage of the TFT. The output swing and input offset voltage of source follower output buffer are not constant values, because these are both related to the various threshold voltages of the TFTs in different panel locations. The Monte Carlo simulation results of source follower output buffer is shown in Fig. 4.4.

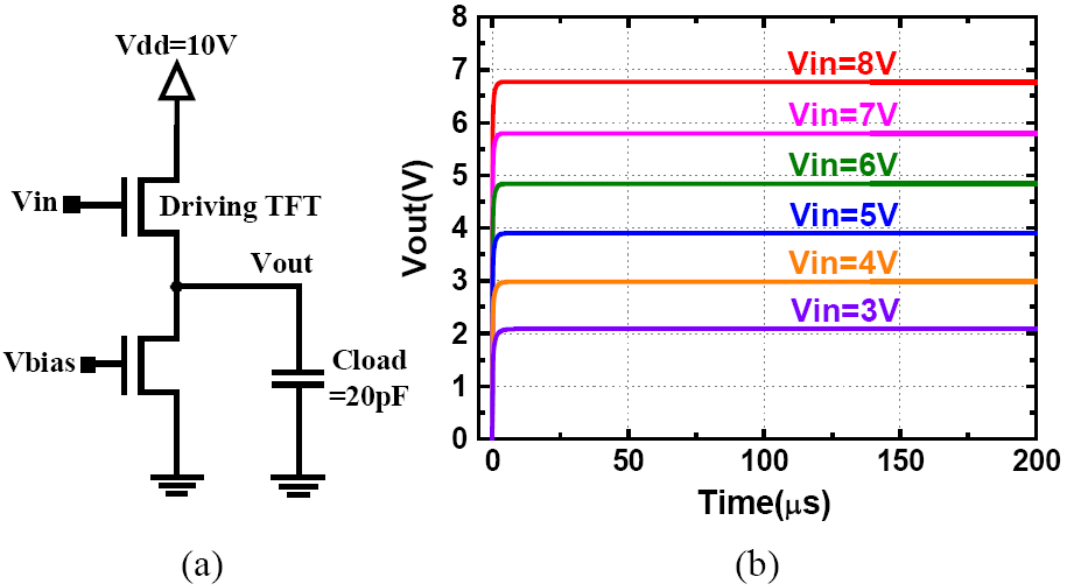


Fig. 4.3 (a) The conventional source follower output buffer and (b) its output waveforms at different input voltages.

Although the source follower output buffer has a huge input offset voltage, the input offset voltage can be reduced by using some compensation technique, like Fig. 4.5 shown. The additional switch devices, capacitors, and control signals are necessary for these methods. The power consumption of this output buffer will become an important issue due to the extra V_{bias} voltage and the DC current path.

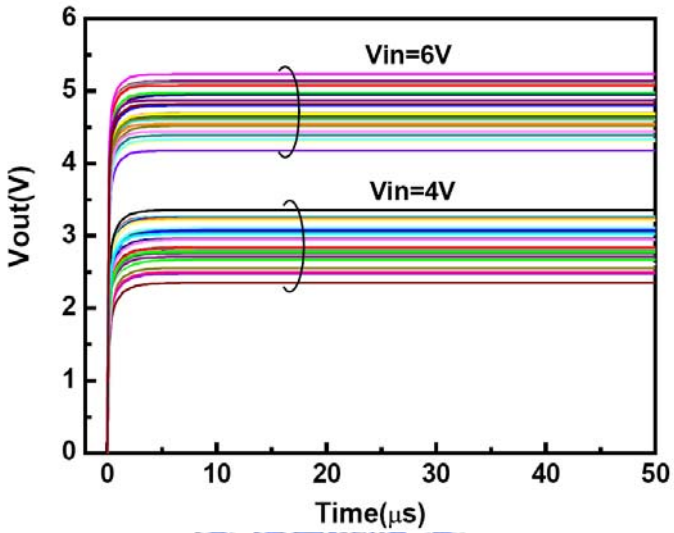
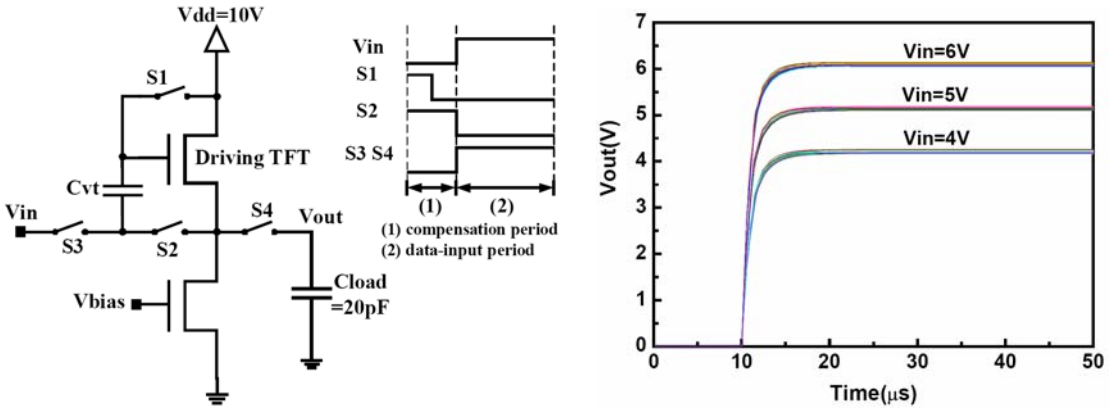


Fig. 4.4 The Monte Carlo simulation results of the conventional source follower output buffer.



(a) (b)

Fig. 4.5 (a) The source follower output buffer with V_{TH} compensation method and (b) Monte Carlo simulation results of this source follower output buffer.

4.3.2 Unity-Gain Output Buffer with an OPAmp

The conventional source follower output buffer has lower output swing and larger input offset voltage. In opposition to the source follower output buffer, the unity-gain output buffer with an OP amp has lower input offset voltage. The relation function between the input and output of this output buffer is

$$V_o = \frac{A}{1+A} V_{in} \qquad (4 - 1)$$

For this reason, the input offset voltage can be reduced by the large open-loop gain (A) of the unity-gain output buffer with an OP amp. In this work, the two-stage OP amp is adopted as a unit-gain output buffer, since the two-stage OP amp has higher open-loop gain, as well as the OP amp has high immunity to noise. Furthermore, the unity-gain output buffer with an OP amp has a larger slew rate for driving the capacitance load of the data bus on panel than that of source follower output buffer at the same operation frequency.

The circuit diagram of the class-A analog output buffer with N-TFTs input stage is shown in Fig. 4.6. As a unity-gain buffer, the output node (Vo) is connected to the negative input node (Vi-) and the input signal is applied to the positive input node (Vi+). This output buffer comprises four parts as following. The first part consists of an n-channel differential pair (M1-M2) with a p-channel current mirror load (M3-M4) and an n-channel tail current source (M5). The second part is a common-source amplifier stage (M6-M7), which can improve the open-loop gain and reduce the input offset voltage for this output buffer. The bias generator part is a constant g_m bias circuit (M11-M16 and R_B), which can provide the bias voltages for this output buffer. By using constant g_m bias method, a more steady reference voltage can be generated due to the constant g_m value.

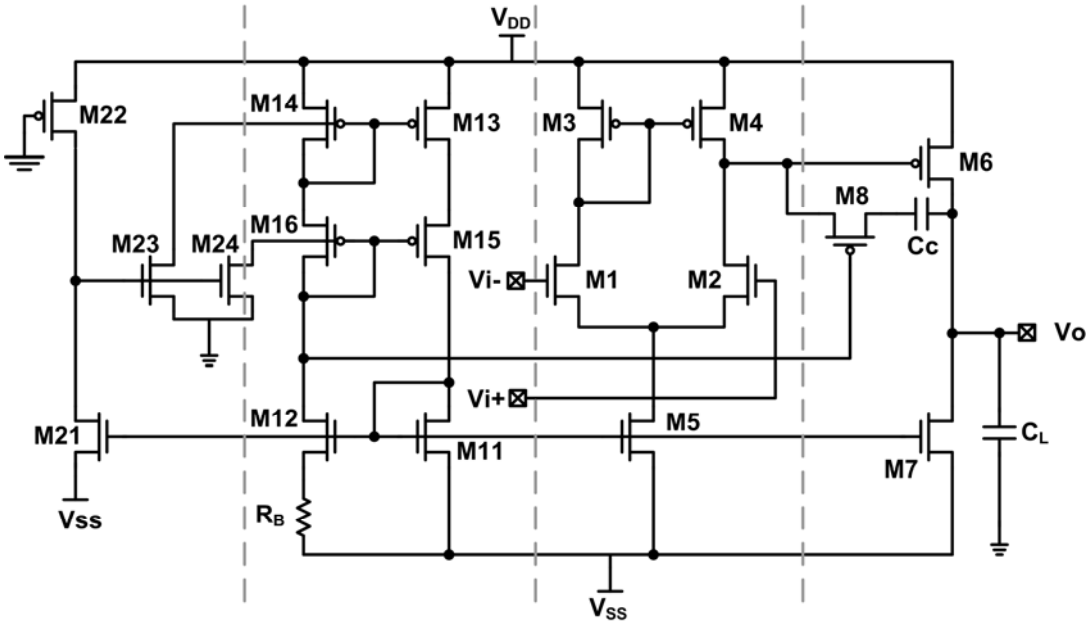


Fig. 4.6 The class-A analog output buffer with N-TFTs input stage.

However, the bias circuit is a self-biasing circuit, it needs a start-up circuit (M21-M24) that turns on the bias circuit in the beginning and automatically be turned off after bias circuit working.

Since there are two poles in this unity-gain output buffer circuit, the OP amp circuit needs frequency compensation to improve the phase margin and stability of the OP amp. In this work, the Miller compensation technique with nulling resistor (M8 and C_C) is adopted as frequency compensation circuit, which can provide a negative zero as

$$z = \frac{1}{(1/g_{m6} - R_C)C_C} \qquad (4 - 2)$$

where the resistor R_C is implemented by using a P-type TFT (M8) biased in the triode region. Making the resistance (R_C) greater than $1/g_{m6}$ moves the zero into the left half-plane (LHP), which can be used to provide positive phase shift at high frequency region and consequently to improve the phase margin of this output buffer.

The simulated frequency response and circuit performances of this output buffer are shown in Fig. 4.7 and Table 4.1, respectively.

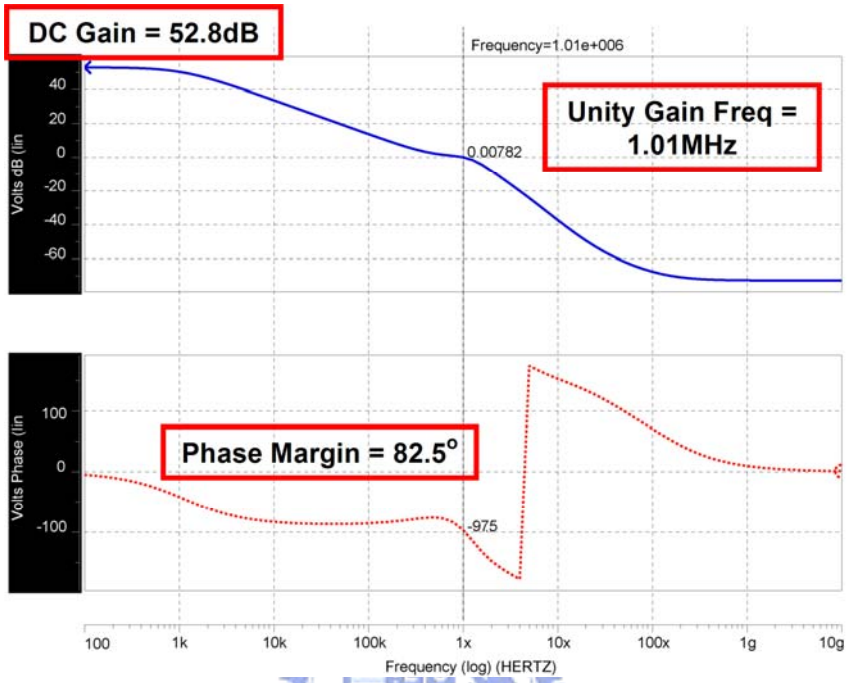


Fig. 4.7 The simulated frequency response of the class-A analog output buffer with N-TFTs input stage in open-loop condition.

Table 4.1

Summary of the simulated circuit performances of the output buffer in Fig. 4.6.

Open-Loop Characteristics	
Differential Gain	52.8 dB
Phase Margin	82.5 °
Unity Gain Bandwidth	1.01 MHz
CMRR	57.81 dB
PSRR + (–)	58.7 (62.2) dB
Close-Loop Characteristics	
Output Swing	1.8 ~ 9.2 V
Slew Rate	1.510 V/μs
Average Power Dissipation	1.386 mW
Power Supply	V_{DD} = 10 V, V_{SS} = 0 V

4.3.3 Proposed Output Buffer with Suppressing Device Variation

Based on section 4.2, we can find that the threshold voltages of the N-type TFT devices in different panel locations vary from 0.75 V to 2.15 V, whose variation is quite large compared with CMOS technology [22]. Besides, the device characteristic variation of the N-type TFT is more serious than that of P-type TFT [27]. For example, the mobility variation of N-type TFT and P-type TFT under the hot-carrier stress are -38.627% and +7.054%, respectively [28]. The average of mobility variation for n-channel and p-channel TFTs at different stress conditions are shown in Table 4.2.

For this reason, replacing the critical part of the analog circuit by P-TFTs is a valid technique for suppressing device characteristic variation and improving the manufacturing yield of the analog circuit. In this unity-gain output buffer, the differential pair of the OP amp is the critical part. Therefore, the output buffer with P-TFTs input differential pair is proposed to suppress the device variation in this work. This proposed output buffer with P-TFTs input stage can be operated at 50-kHz operation frequency with an output voltage swing of 1-to-9 V

Table 4.2
Mobility variation for n-channel and p-channel TFTs at different stress conditions.

		Average Variation (%)	**Std. Dev**
Hot-Carrier Stress Condition	***N-Channel***	-38.627	6.65
	P-Channel	+7.054	2.72
On-Current Stress Condition	***N-Channel***	+11.828	3.28
	P-Channel	+2.251	0.6525

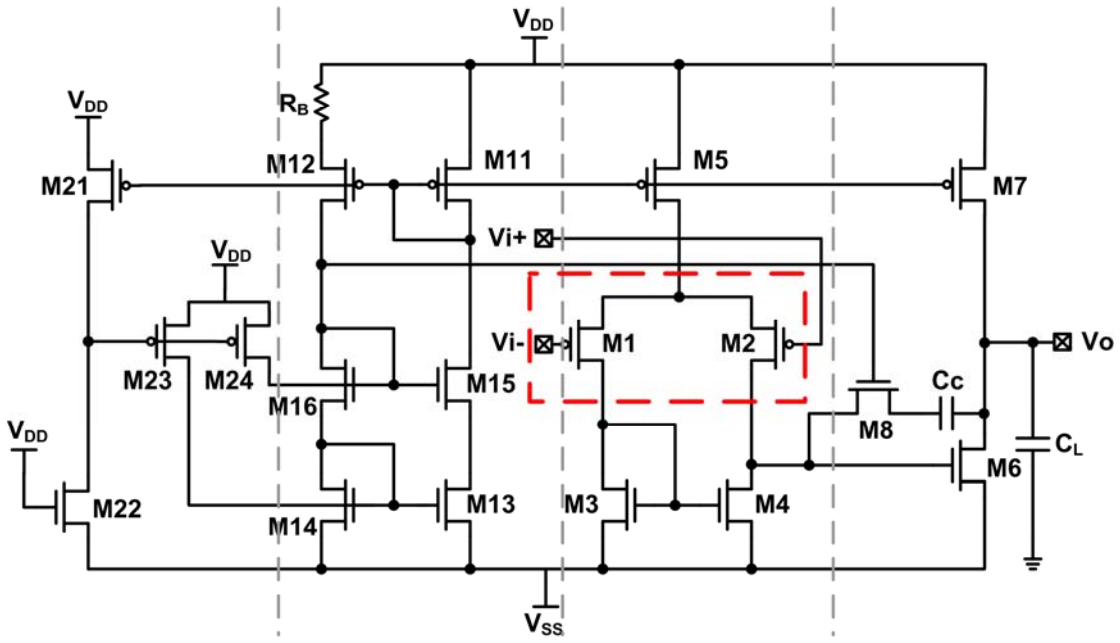


Fig. 4.8 The class-A analog output buffer with P-TFTs input stage.

The proposed analog output buffer with P-TFTs input stage is shown in Fig. 4.8. These two OP amps (in Fig. 4.6 and Fig. 4.8) have the similar dc voltage gain, as shown in the following

$$A_V(0)_{N-input} = g_{m1-N} \cdot g_{m6-P} \cdot R_1 \cdot R_2 \qquad (4-3)$$

$$A_V(0)_{P-input} = g_{m1-P} \cdot g_{m6-N} \cdot R_1 \cdot R_2 \qquad (4-4)$$

where R_1 is the value of r_{o2} parallel with r_{o4} and R_2 is the value of r_{o6} parallel with r_{o7}. From equations (4 - 3) and (4 - 4), the dc voltage gain of OP amp with P-TFTs input stage is almost similar to that of OP amp with N-TFTs input stage, when $(W/L)_1$ and $(W/L)_6$ are designed with the same device dimensions.

There are some advantages in the OP amp with P-TFTs input stage compared with the OP amp with N-TFTs input stage. The OP amp with P-TFTs input stage has larger unity-gain frequency since $\omega_u \sim |p_2| = g_{m6}/C_L$ and g_{m6-N} is larger than g_{m6-P}.

Furthermore, this OP amp with P-TFTs input stage also has better slew rate than the OP amp with N-TFTs input stage due to the larger unity-gain frequency in the OP amp with P-TFTs input stage. The OP amp with P-TFTs input stage also has more steady circuit performances, because the critical part (differential pair) of the OP amp is composed of the P-TFTs which have less device characteristic variation. The simulated frequency response and comparison on circuit performances are shown in Fig. 4.9 and Table 4.3, respectively. From this simulation results, we can find that the circuit performances in this proposed output buffer also can be maintained nearly the same as the performances in the output buffer with N-TFTs input stage

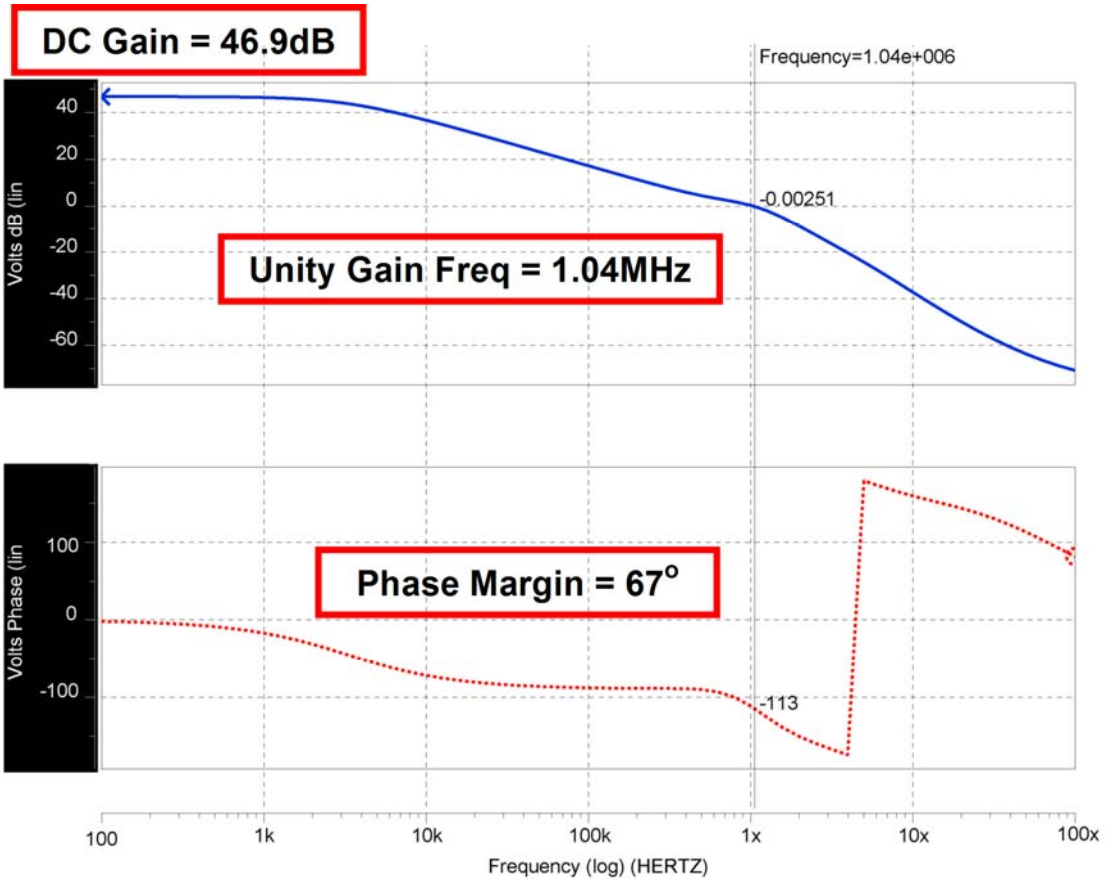


Fig. 4.9 The simulated frequency response of the class-A analog output buffer with P-TFTs input stage in open-loop condition.

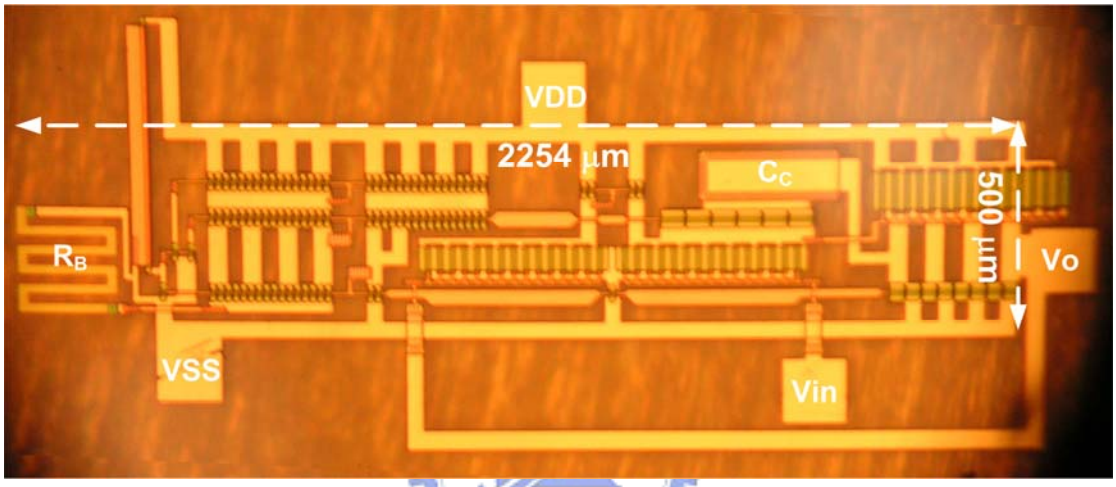
Table 4.3
The summary and comparison of the simulated circuit performances of the output buffer in Fig. 4.6 and Fig. 4.8.

Open-Loop Characteristics		
Output Buffer Type	***N-TFTs input stage OP amp***	***P-TFTs input stage OP amp***
Differential Gain	52.8 dB	46.9 dB
Phase Margin	82.5 °	67 °
Unity Gain Bandwidth	1.01 MHz	1.04 MHz
CMRR	57.81 dB	59.3 dB
PSRR + (–)	58.7 (62.2) dB	76.3 (52.3) dB
Close-Loop Characteristics		
Output Swing	1.8 ~ 9.2 V	0.91 ~ 9.1 V
Slew Rate	1.510 V/μs	1.885 V/μs
Average Power Dissipation	1.386 mW	1.734 mW
Power Supply	V_{DD} = 10 V, V_{SS} = 0 V	V_{DD} = 10 V, V_{SS} = 0 V

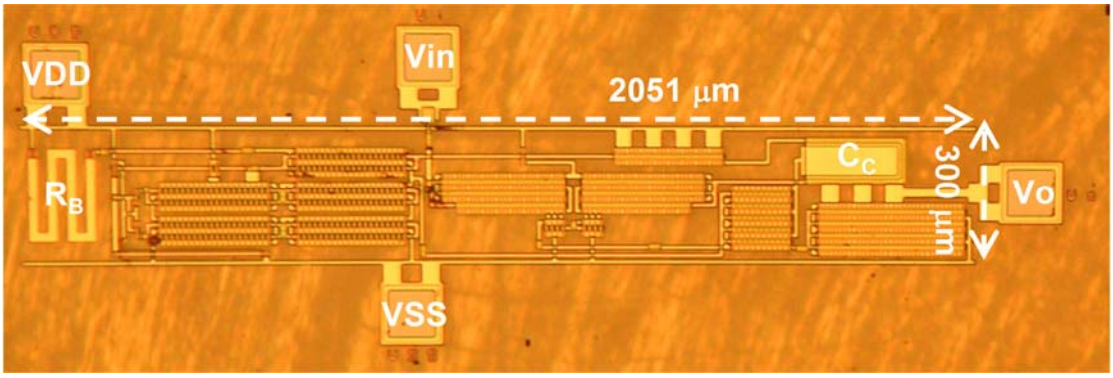
Besides, the P-TFTs have less flicker noise (1/f noise) than that of N-TFTs, since holes are less likely to be trapped. For this reason, the proposed output buffer with P-TFTs input stage has better flicker noise (1/f noise) performance than that of the output buffer with N-TFTs input stage. Moreover, the proposed output buffer with P-TFTs input stage also has other advantages, such as larger slew rate, lower input offset voltage, and better immunity to noise, as comparing to the source follower output buffer. The proposed output buffer with P-TFTs input stage can be operated at 50-kHz operation frequency with an output voltage swing of 1-to-9 V. The power supply of this circuit is V_{DD} of 10 V and V_{SS} of 0 V.

4.4 EXPERIMENTAL RESULTS

The class-A output buffers with N-TFTs input stage and P-TFTs input stage have been design and fabricated in a 8μm LTPS technology. The photographs of these buffers on glass substrate with the corresponding pin names are shown in Fig. 4.10 (a) and Fig. 4.10 (b), respectively.



(a)



(b)

Fig. 4.10 The photographs of the class-A output buffers with (a) N-TFTs input stage and (b) P-TFTs input stage.

The setup illustrations for slew rate, output swing, and unity-gain bandwidth measurement are shown in Fig. 4.11 and Fig. 4.12, respectively. Tektronix TDS 3054 is an oscilloscope using to detect and display the signal waveforms. HP 4156B is a semiconductor parameter which can provide a V_{DD} of 10 V and V_{SS} of 0 V. Agilent 81110A and HP 8116A are function generators which can provide input signals, like square waveform or sine waveform. These instruments are used to measure the fabricated output buffer circuit.

Fig. 4.13 shows the proposed analog output buffer under the PCB (printed circuit board) with wire bonding and the measurement setup illustration with the wire bonding glass substrate samples. The glass samples under the PCB with wire bonding has more flexible measurement method for other application and demonstration.

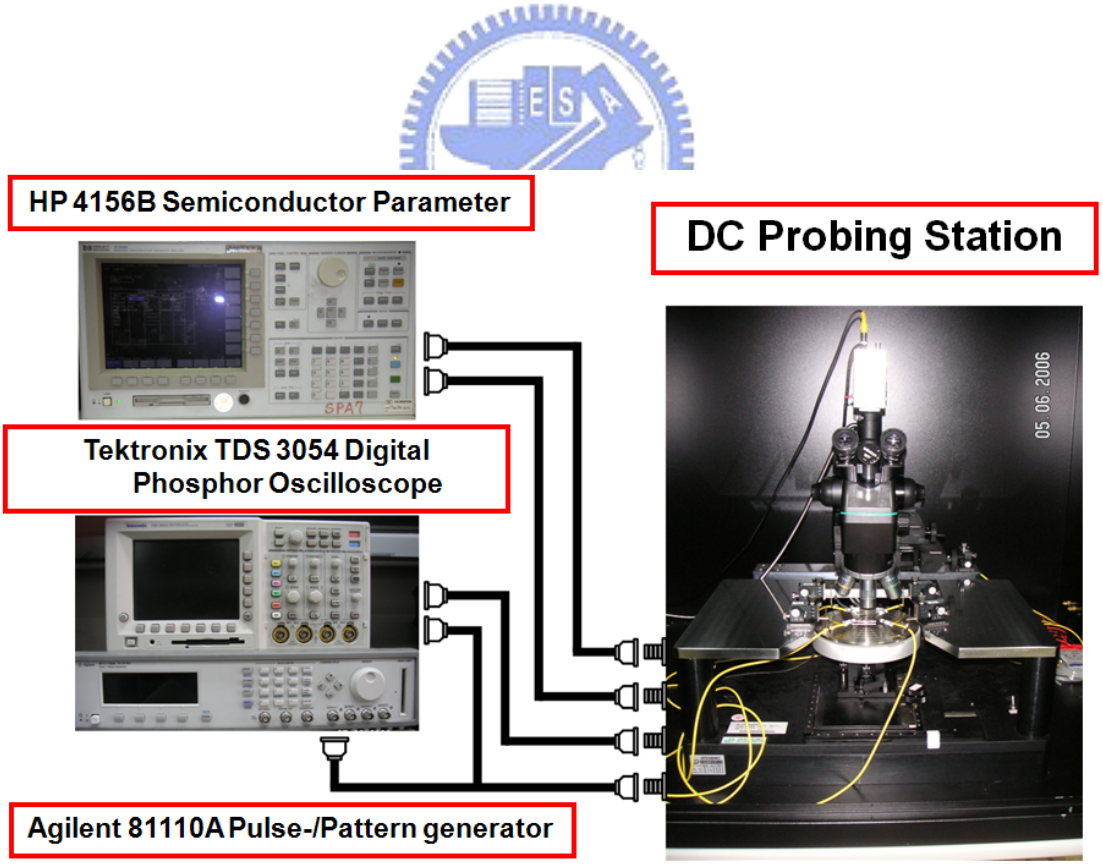


Fig. 4.11 The setup illustration for slew rate and output swing measurement with DC probing station.

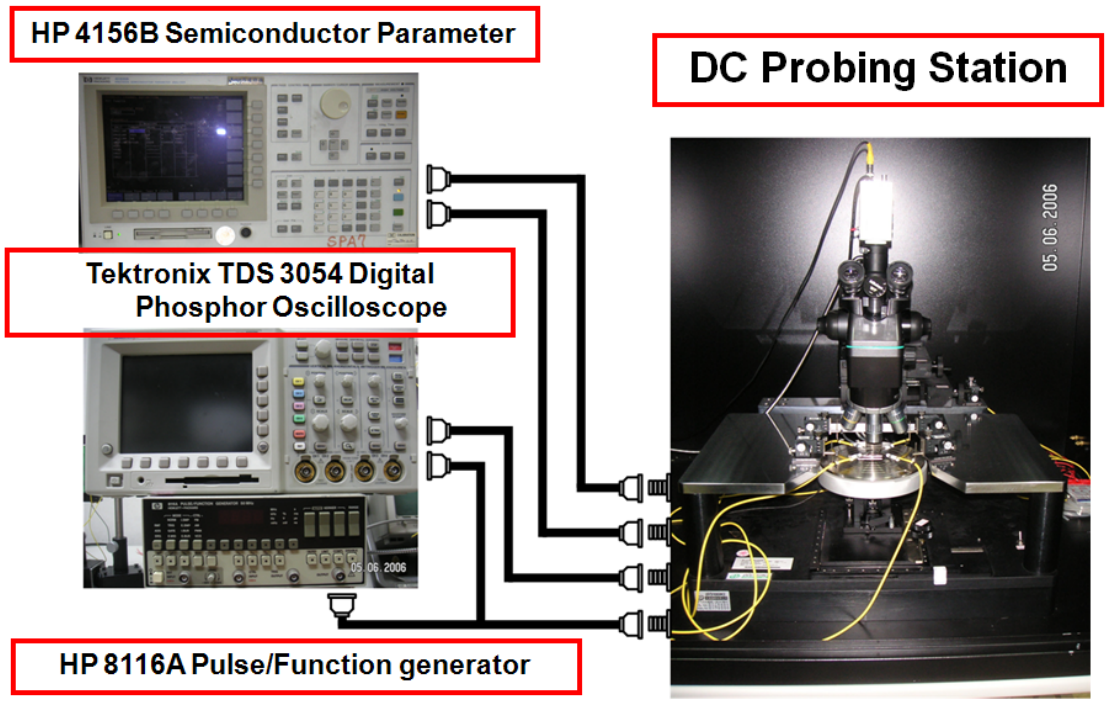


Fig. 4.12 The setup illustration for unity-gain bandwidth measurement with DC probing station.

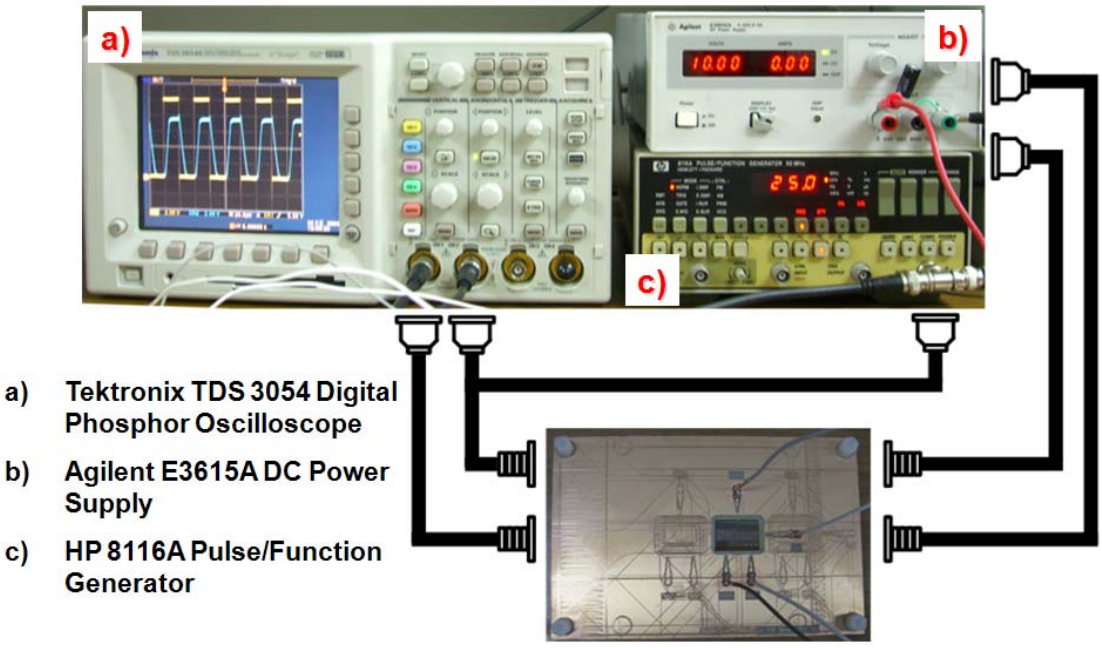


Fig. 4.13 The proposed analog output buffer under the PCB with wire bonding and the measurement setup illustration with the wire bonding glass substrate samples.

The measured output waveforms of class-A output buffers with N-TFTs input stage and P-TFTs input stage are compared in Fig. 4.14 and Fig. 4.15. Based on Fig. 4.14, we can find that the slew rate (output swing) of these two output buffers are 1.843 V/ms (0.2-to-6.8 V) and 1.961 V/ms (0.8-to-9.6 V), respectively. Moreover, from Fig. 4.15, the unity-gain bandwidth of these two output buffers are 55.6 kHz and 107.2 kHz, respectively.

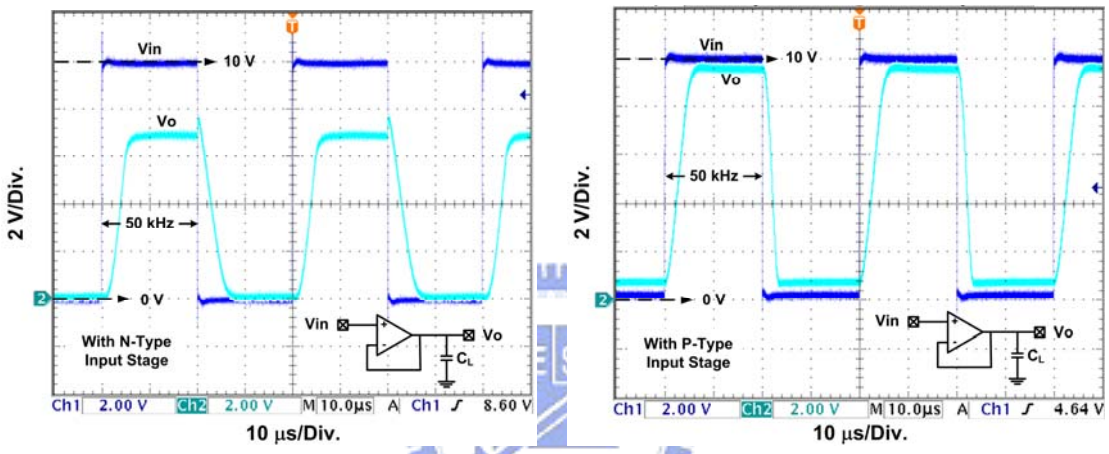


Fig. 4.14 The measured output waveforms of the class-A output buffers with (a) N-TFTs input stage and (b) P-TFTs input stage about slew rate and output swing.

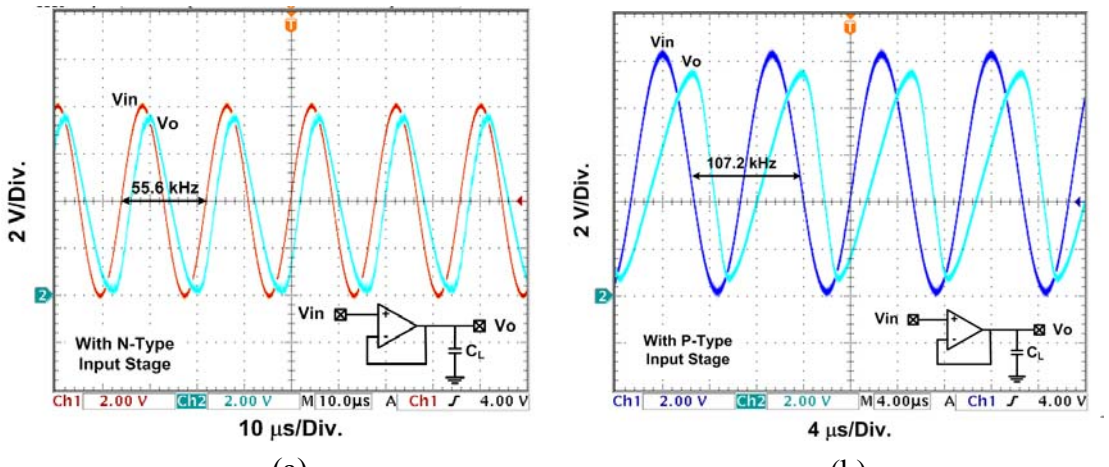


Fig. 4.15 The measured output waveforms of the class-A output buffers with (a) N-TFTs input stage and (b) P-TFTs input stage about unity-gain bandwidth.

The measured results of slew rate and output swing among 13 class-A output buffers with N-TFTs input stage are shown in Fig. 4.16. The output buffer with N-TFTs input stage really has poor manufacturing yield and performance stability due to the wider device variation. Based on the measured results in Fig. 4.14 and Fig. 4.15, obviously, we can find that the proposed output buffer with P-TFTs input stage has higher manufacturing yield and performance stability than those of the output buffer with N-TFTs input stage. The experimental results also have proven that replacing the critical part of the analog circuit by P-TFTs is a valid technique for suppressing device characteristic variation on glass substrate.

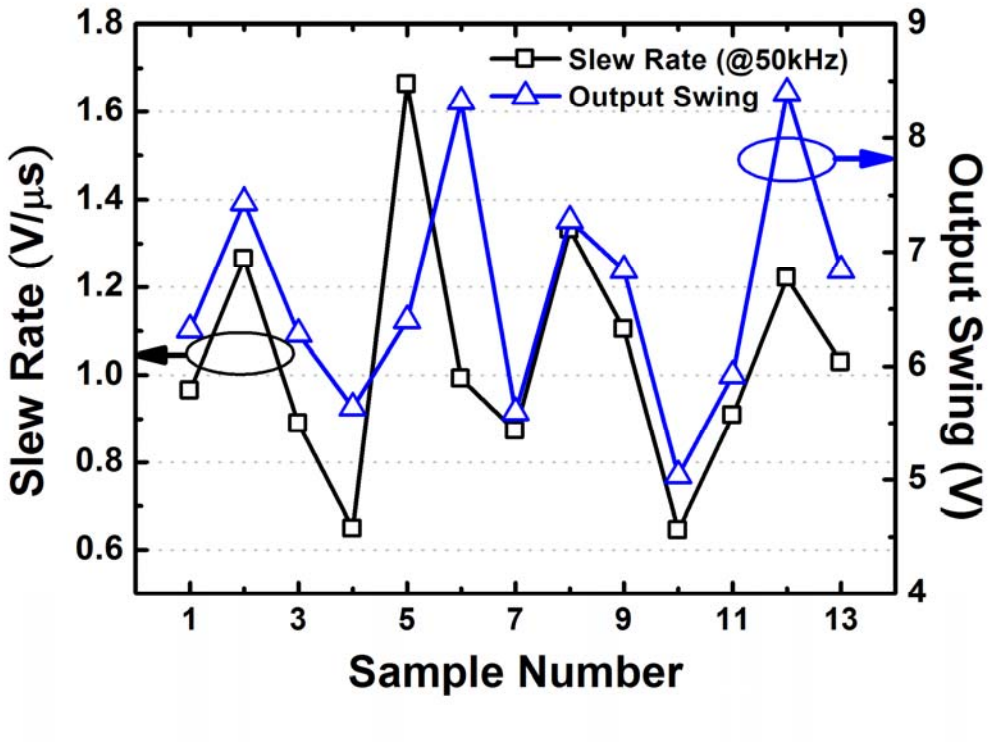
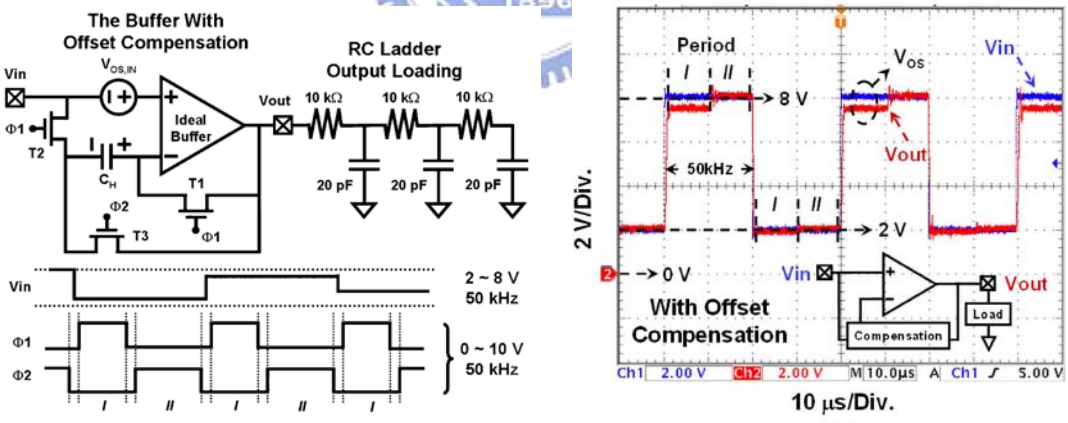


Fig. 4.16 The slew rate and output swing of the class-A output buffer with N-TFTs input stage, which are measured from 13 samples on glass substrate.

4.5 DISCUSSION

The accuracy of the data driver is determined by DAC circuit combined with analog output buffer. Even though the DAC has high accuracy, the data driver also has not enough accuracy with a low accuracy analog output buffer. For this reason, the input offset voltage of the analog output buffer will become a serious issue in data drivers. Fig. 4.17 shows a valid input offset compensation method and the measurement results of this analog output buffer with the offset compensation technique [22]. During the period I, the offset voltage is stored in C_H. In the period II, the detected offset voltage in C_H is added into the inverting input node. From Fig. 4.17 (b), we can find that the offset voltage of this analog output buffer can be compensated under the second period by using this offset compensation technique.



(a) (b)

Fig. 4.17 (a) Circuit and signal-timing diagram of the analog output buffer with the offset compensation technique. (b) The measurement result of this analog output buffer with the offset compensation technique under 50-kHz square wave with a swing of 2-to-8 V.

4.6 SUMMARY

In this chapter, A class-A output buffer with device variation suppressing technique in LTPS technology has been proposed and verified in 8-μm LTPS technology. The output buffer with P-TFTs input stage can be operated at 50-kHz operation frequency with at least 1-to-9 V output swing under V_{DD} of 10 V and V_{SS} of 0 V. The slew rate of this proposed output buffer is 1.961 V/μs. The device characteristic variation has been successfully suppressed by replacing the critical part of analog circuits by the P-TFTs. The proposed output buffer with P-TFTs input stage can be used in the on-panel data drivers to provide a uniform brightness and high resolution display. Furthermore, this proposed analog output buffer is also suitable for ambient light sensor system to boosting the output signal. Fig. 4.18 shows the proposed analog output buffers are used for pixel array in TFT-LCD panel.

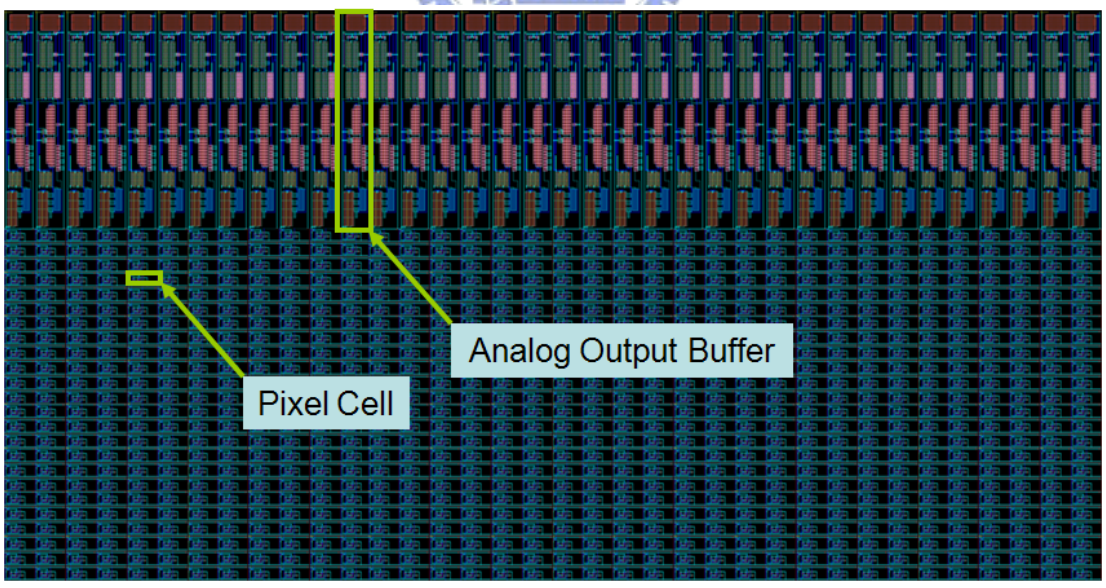


Fig. 4.18 The proposed class-A output buffer with P-TFTs input stage using for pixel array in TFT-LCD panel.

Chapter 5

Conclusion and Future Works

5.1 CONCLUSION

A novel 6-bit folded R-string DAC with gamma correction for on-panel data driver has been proposed in chapter 3. This proposed DAC has been successfully verified in 8-μm and 3-μm LTPS technology. By using the folded R-string and segmented digital decoders, the area of the R-string DAC can be effectively reduced to about one sixth and the complexity of circuit can be simplified. Furthermore, this architecture is also more suitable for gamma correction design and many kinds of LTPS process. Although, there is only a discussion for normally white TN-type liquid crystal in this thesis. This proposed architecture is also suitable for many kinds of gamma value and normally white (or black) TFT-LCD panel by modifying the R-string value and the decoder architecture.

In chapter 4, a class-A output buffer with device variation suppressing technique in LTPS technology has been proposed and verified in 8-μm LTPS technology. The output buffer with P-TFTs input stage can be operated at 50-kHz operation frequency with at least 1-to-9 V output swing under V_{DD} of 10 V and V_{SS} of 0 V. The slew rate of this proposed output buffer is 1.961 V/μs. The device characteristic variation has been successfully suppressed by replacing the critical part of analog circuits by the P-TFTs. The proposed output buffer with P-TFTs input stage can be used in the on-panel data drivers to provide a uniform brightness and high resolution display.

5.2 FUTRUE WORKS

Although the proposed 6-bit folded R-string DAC in this thesis are successfully designed and verified in LTPS technology. The accuracy of the data driver is determined by DAC circuit combined with analog output buffer. Even though the DAC has high accuracy, the data driver also has not enough accuracy with a low accuracy analog output buffer. This is because that the analog output buffer has large input offset voltage. For this reason, the input offset voltage of the analog output buffer will become a serious issue in data drivers. Fig. 5.1 shows a valid input offset compensation method [20]. In this circuit, the pre-charge buffers first execute rapid charging or discharging of the data-line with respect to the analog signal voltage of the R-DAC. After that, the R-DAC output, which is a signal voltage precisely determined by the reference string resistance, is connected directly to the data-line. By using this method, the offset of the pre-charge buffers can be neglected in this operation mode of the proposed DAC. Furthermore, since the pre-charge buffers carry most of the power load required to charge the data-line, static current through the reference string resistance can be kept to a minimum.

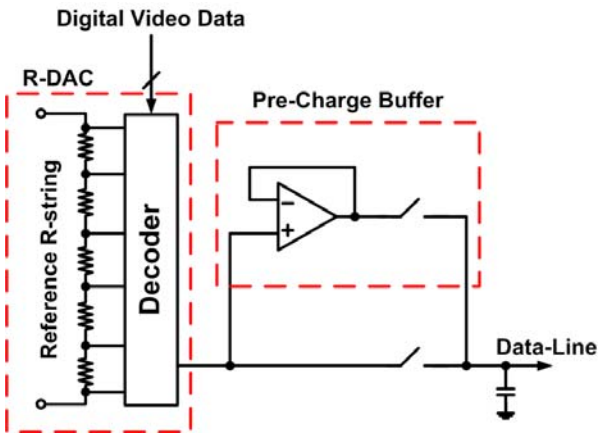


Fig. 5.1 The architecture of the DAC circuit combined with analog output buffer with input offset compensation method in TFT-LCD panel.

In addition, the power dissipation must be minimized while displays are used toward portable applications. The analog output buffer is a critical design to achieve the low power dissipation on TFT-LCD panels. In chapter 4, we propose a class-A output buffer with device variation suppressing technique in LTPS technology. But, the class-A output buffer has a drawback which is less power efficiency. This is because this kind of output buffer always has a DC current path. If we can replace the output stage of the OP amp by class-B or class-AB output stage, the power consumption of analog output buffer will be reduced effectively [29]. For example, Fig. 5.2 shows a class-B analog output buffer with device variation suppressing technique.

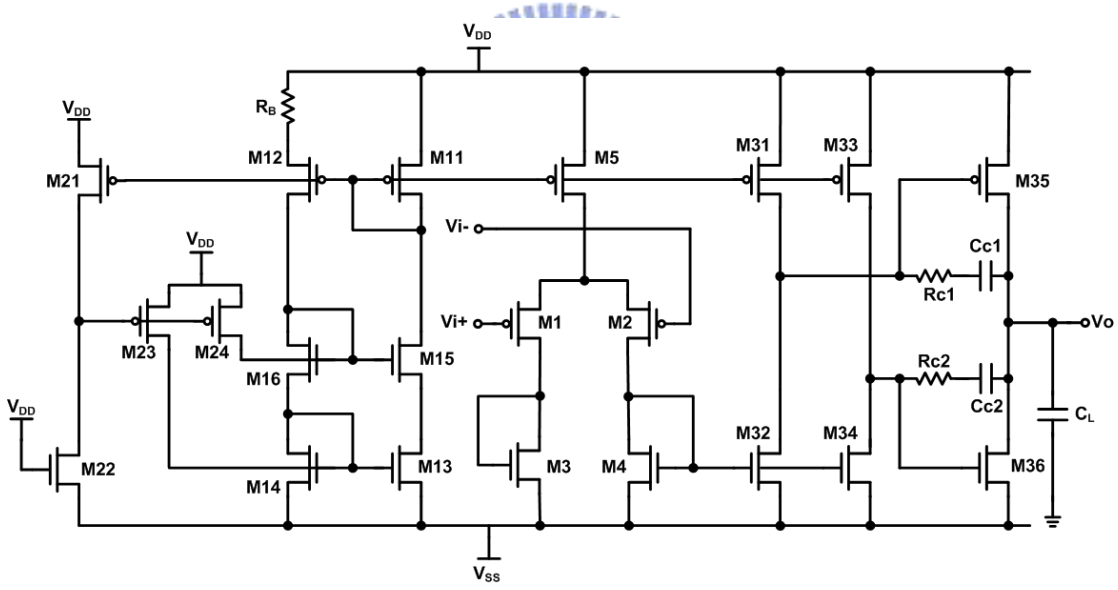


Fig. 5.2 A class-B analog output buffer with device variation suppressing technique.

REFERENCES

[1] S. Uchikoga, "Low-temperature polycrystalline silicon thin-film transistor technologies for system-on-glass displays," in *MRS Bulletin*, pp. 881−886, Nov. 2002.

[2] K. Yoneda, R. Yokoyama, and T. Yamada, "Future application potential of low temperature p-Si TFT LCD displays," *SID*, *Dig*. *Tech*. *Papers*, *2001*, vol. 50, No. 1, pp. 1242−1245.

[3] Y. Nakajima, Y. Teranishi, Y. Kida, and Y. Maki, "Ultra-low-power LTPS TFT-LCD technology using a multi-bit pixel memory circuit," *SID*, *Dig*. *Tech*. *Papers*, *2006*, vol. 22, No. 4, pp. 1185−1188.

[4] Y. Nakajima, Y. Kida, M. Murase, Y. Toyoshima, and Y. Maki, "Latest development of "System-on-Glass" display with low temperature poly-Si TFT," *SID*, *Dig*. *Tech*. *Papers*, *2004*, vol. 21, No. 3, pp. 864−867.

[5] B. Lee, Y. Hirayama. Y. Kubota, S. Imai, A. Imaya, M. Katayama, K. Kato, A. Ishikawa, T. Ikeda, Y. Kurokawa, T. Ozaki, K. Mutaguch and S. Yamazaki, "A CPU on a glass substrate using CG-silicon TFTs," *ISSCC*, 2003, vol. 9, No. 4, Feb. 2003.

[6] T. Nishibe and H. Nakamura, "Value-added circuit and function integration for SOG (System-on-Glass) based on LTPS technology," *SID*, *Dig*. *Tech*. *Papers*, *2006*, vol. 16, No. 4, pp. 1091−1094.

[7] E. Lueder, *Liquid Crystal Displays Addressing Schemes and Electro-Optical Effects*, John Wiley and Sons, Inc., Sep. 2004.

[8] T. Tsukada, *TFT/LCD Liquid-Crystal Displays Addressed by Thin-Film Transistors*, Gordon and Breach Publishers, 1996.

[9] D. McCartney, *LCD Electronics Theory of Operation Handout*, Fall 2005.

[10] Y.-H. Tai, *Design and Operation of TFT-LCD Panels*, Wu-Nan Book, Inc., Apr. 2006.

[11] P. R. Gray, P. J. Hurst, Stephen H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, Inc., 2001.

[12] D. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, Inc., 1997.

[13] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, New York: Oxford University Press, 2002.

[14] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Companies, Inc., 2001.

[15] J.-Y. Hu and W.-T. Sun, "Method for reducing spikes in a digital-to-analog converter," U.S. Patent 6819277, Nov. 16, 2004.

[16] M. Pelgrom, "A 50 MHz 10-bit CMOS digital-to-analog converter with 75 Omega buffer," *ISSCC*, 1990, vol. 12, No. 2, pp. 200−201, 295, Feb. 1990.

[17] J.-T. Wu, *Analog Integrated Circuits (II) Handout*, Spring 2006.

[18] Y. Uraoka, T. Hatayama, T. Fuyuki, T. Kawamura, and Y. Tsuchihashi, "Reliability of low temperature poly-silicon TFTs under inverter operation," *IEEE Trans. on Electron Devices*, vol. 48, No. 10, pp. 2370–2374, Oct. 2001.

[19] Y. M. Ha, "P-type technology for large size low temperature poly-Si TFT-LCDs," *SID, Dig. Tech. Papers, 2000*, pp.1116–1119.

[20] Y. Nonaka, H. Haga, H. Tsuchi, Y. Kitagishi, T. Matsuzaki, M. Sugimoto, H. Hayama, and H. Asada, "A low-power SOG LCD with integrated DACs and a DC-DC converter for mobile applications," *SID, Dig. Tech. Papers, 2004*, pp. 1448–1451.

[21] S. H. Yeh, W. T. Sun, J. S. Yu, C. C. Chen, J. Lee, and C. S. Yang, "A 2.2-inch QVGA system-on-glass LCD using p-type low temperature poly-silicon thin film transistors," *SID, Dig. Tech. Papers, 2005*, pp. 352–355.

[22] M. D. Ker, C. K. Deng, and J. L. Huang, "On-panel output buffer with offset compensation technique for data driver in LTPS technology," *IEEE J. Display*

Tech., vol. 2, No. 2, pp. 153–159, June 2006.

[23] W. Y. Guo, A. Shih, C. Y. Meng, and Y. M. Tsai, "Reliability of low temperature poly-Si thin film transistor," *SID, Dig. Tech. Papers, 2003*, pp. 224–227.

[24] Y. H. Tai, "Device variation and its influences on the LTPS TFT circuits," *International TFT Conference 2005*.

[25] S. C. Huang, G. F. Peng, J. L. Chern, and Y. H. Tai, "Statistical investigation on the variation behavior of low-temperature poly-Si TFTs for circuit simulation," *SID, Dig. Tech. Papers, 2006*, pp. 329–332.

[26] C. C. Pai and Y. H. Tai, "A novel analogue buffer using poly-Si TFTs for active matrix displays," in *IDMC Tech. Dig., 2005*, pp. 483–486.

[27] S. I. Hsieh, H. T. Chen, Y. C. Chen, C. L. Chen, and Y. C. King, "Threshold voltage uniformity enhancement for low-temperature polysilicon thin-film transistors using tilt alignment technique," *Electrochemical and Solid-State Lett.*, pp. H57–H60, 2006.

[28] W. Y. Guo, C. Y. Meng, A. Shih, and Y. M. Tsai, "Reliability of low temperature poly-Si thin film transistor," in *IDMC Tech. Dig., 2003*.

[29] C.-W. Lu and C.-L. Lee, "A low power high speed Class-B buffer amplifier for flat panel display application," in *DELTA Tech. Dig.*, 2002, pp. 172−176.

簡歷

姓　　名：李宇軒

學　　歷：

私立國光高級中學　　(87年9月~90年6月)

國立交通大學電機與控制工程學系　　(90年9月~94年6月)

國立交通大學電子研究所碩士班　　(94年6月~96年6月)

研究所修習課程：

類比積體電路 I、II	吳介琮教授
數位積體電路	周世傑教授
積體電路之靜電放電防護設計特論	柯明道教授
計算機結構	黃俊達教授
顯示電子電路	戴亞翔教授
TFTLCD 面板設計實務	戴亞翔教授
平面顯示器驅動原理及電路設計	劉昌和副理
TFT-LCD 驅動電路設計	宋國明教授
液晶顯示器驅動原理	馬志遠經理

永久地址：高雄市左營區後昌路 611 巷 48 號

Email： leefish.ee94g@nctu.edu.tw

leefish.ece90@nctu.edu.tw

m9411615@alab.ee.nctu.edu.tw

PUBLICATION LIST

[1] Y.-H. Li, M.-D. Ker, C.-Y. Huang, and C.-Y. Hsu, “On-panel analog output buffer for data driver with consideration of device characteristic variation in LTPS technology,” in *ASIA Display Tech. Dig.*, 2007, vol.1, pp. 210−215.

[2] M.-D. Ker, Y.-H. Li, and C.-Y. Hsu, “Novel digital-to-analog converter with gamma correction for on-panel data driver in LTPS technology,” patent pending, 2007.