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具有正負電壓極性之抑制癲癇發作 雙向電流刺激器設計

Design of Mono-Polar Biphasic Stimulus Driver to Suppress Epileptic Seizure in 0.18µm 1.8V/3.3V CMOS Process

研究生: 顧珊綺 (Shan-Chi Ku)

指導教授: 柯明道教授 (Prof. Ming-Dou Ker)

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近年,結合醫學與微電子學,電流刺激器已被視為嶄新的醫療技術,功能性電刺激 (Functional electrical stimulation) 與治療性電刺激 (Therapeutic electrical stimulation)已被證實可以藉由傳送電訊號給神經系統來恢復一個人的某些身體功能,可以應用於心臟、四肢肌肉、視網膜、癲癇、電子耳..等。

具有負載適應性的刺激器,在輸出刺激電流時,隨著不同電極組織的等效阻抗,在輸出端可能有接近七伏特的高壓,為了承受輸出端的高壓,過去的刺激器電路大多使用高壓製程來實作,而本刺激器電路為了與智慧型仿生系統中的其他電路做單晶片整合,因此必須使用低壓製程來實作。本刺激器透過電壓限制的技

巧,使其能以低壓製程 1.8V/3.3V 元件來承受高工作電壓(±7.2V),而電晶體不會面臨電性過壓的可靠度問題。

從生醫電子安全的考量,需要減少雙向電流的電荷誤差,以避免電荷累積在電極上而造成神經細胞的傷害。由於不同的組織、位置、植入時間,老鼠的大腦組織的等效阻抗變化範圍大,從幾十 kΩ 到幾百 kΩ。對不同大小的老鼠腦組織之等效阻抗,電流刺激器皆可提供週期性電流脈波輸出,抑制癲癇的發作。雙向電流刺激方式依每個刺激位置電極數可分為兩種:兩根電極(雙極性)刺激以及一根電極(單極性)刺激。雙極性刺激為輸出高低電位之兩根電極做刺激,其高低電位會互換,使電流周期性地正負反向;單極性刺激為一根電極對共地電極做刺激,當輸出正刺激電流時電極電壓為正電壓,反向電流時電極電壓為負電壓。從電路的角度,對多通道刺激器而言,只需要一半數目的 PAD,連接電極的輸出端,因此可以減少晶片的面積。單極性刺激相較於雙極性刺激可以有較大的刺激範圍。然而,單極性刺激器需要正負高工作電壓,在低壓製程下增加電路設計的挑戰性。

所設計的單極性雙向電流刺激器,因晶片外部只提供 VDD=1.8V 供應電壓, 所以晶片內部需要藉由 DC-DC 轉換器產生刺激器所需的高工作電壓 VCC 和 VSS。本刺激器可以由三位元來選擇輸出刺激器電流大小為 10,20,30,40, 50μA。在刺激電流 30μA 下,本刺激器可適用的電極阻抗從 50kΩ 到 200kΩ,此 電路在 TSMC 0.18μm 1.8V/3.3V CMOS 製程下實現。

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Student: Shan-Chi Ku Advisor: Prof. Ming-Dou Ker

Department of Electronics Engineering & Institute of Electronics National Chiao-Tung University



Nowadays, the stimulator that transmits artificial electrical signals into nervous system to restore some physical functions of a human has been investigated and verified. Functional electrical stimulation (FES) and therapeutic electrical stimulation (TES) systems have been developed for restoring function in different applications such as cardiac pacing, extremity muscle exercising, vision restoration and suppression of epileptic seizure.

When the stimulator with high-voltage-tolerant consideration delivers stimulus current, the output voltage of stimulator may be larger than system supply voltage due to variation of electrode-tissue equivalent impedance. In order to sustain the high operating voltage at the output of stimulator, conventional stimulator is fabricated in high-voltage process. The proposed stimulator will be integrated with other circuits

such as bio-signal processor and microcontroller for systems-on-chip (SOC). Besides, a stimulator with adaptive loading consideration in low-voltage CMOS process is also needed.

In this work, a high-voltage-tolerant stimulator in a 0.18µm 1.8V/3.3V CMOS process is proposed. Using stacked transistors and voltage limiting technique prevent from reliability issues such as electrical overstress and gate-oxide breakdown. The stimulus driver is designed to deliver charge balanced biphasic pulses and reduces the mismatch between the anodic and cathodic pulses to avoid charge accumulation hurting the never cells. The biphasic stimulation methodology about electrode configuration is classified into two types: two leads per site (bipolar stimulation) and one lead per site (monopolar stimulation). For multi-channel application, the number of interconnect leads between the stimulator and tissue by monopolar type is a half of the number by bipolar type, reducing chip area of contact pads. The monopolar configuration is preferred over a bipolar counterpart if the stimulus current is intended to spread over a wider area.

The regulator circuit of the SoC project only provides VDD (1.8V) to the high-voltage-tolerant stimulator. Therefore, the proposed monopolar biphasic stimulator consists of the stimulus driver, positive high voltage generator, and negative high voltage generator. In addition, the output stimulus current of stimulator could be $10 \sim 50~\mu A$. The loading of stimulator can be adaptive within the electrode-tissue impedance from $50k\Omega$ to $200k\Omega$ in series with $12nF\sim 200nF$ capacitor in stimulus current of $30~\mu A$ in the TSMC $0.18\mu m$ 1.8V/3.3V CMOS process.