國 立 交 通 大 學

電子研究所

博 士 論 文

具製程電壓溫度補償之非晶體震盪器電路設計與實現

DESIGN AND IMPLEMENTATION OF CRYSTAL-LESS CLOCK GENERATOR WITH PROCESS VOLTAGE TEMPERATURE COMPENSATION

研 究 生： 陸亭州(Ting-Chou Lu)

指導教授： 柯明道(Ming-Dou Ker)

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中 華 民 國 一 0 六 年 六 月

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中 華 民 國 一 0 六 年　六　月

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摘要

隨著半導體製程進步，低操作電壓電路之應用逐漸隨半導體進步而日趨盛行，而其中最無法降低電壓部分為晶體振盪器。其有穩地性極佳但必須操作在高操作電壓之工作環境之特性。因此，無晶體振盪器之可行性日趨重要，但低操作電壓伴隨著電路操作頻率增快、處理資料量增加，引發劇烈系統晶片溫度變化，降低電路穩定性、造成資料錯誤等缺點。為了避免上述問題產生以及搭配低電壓電路設計，系統晶片整合時需規劃於電路中一溫度製程補償電路，作為監測並管理晶片溫度於安全範圍內。因此低成本、高精準度之無晶體頻率產生器已成為近年積體電路相當熱門之研究議題。

傳統類比式無晶體振盪器利用疊接方式做操作電壓之補償，並利用BJT作為穩定溫度之能帶隙參考電壓電路。然而此些方式並無法利用在低電壓之溫度補償架構上主要為BJT之可驅動電壓遠大於低電壓之操作電壓。此種溫度補償電路為具有高解析且高精準度之溫度補償電路。但由於電路功率消耗大、晶片面積大、轉換率低、製成與電壓限彈性度低等缺點。使得傳統式溫度補償電路於低電壓應用時，有許多限制與成本過高的問題。

為改善上述類比式溫度感測器缺點，本篇提出低電壓操作電路，利用基極操作電壓，次臨界區MOSFET操作元件，以及-gm增益放大技術來使得操作於低電壓趨為可行。實現具有功率消耗低、晶片面積小、設計複雜度低與系統相容度高之溫度補償電路，改善了傳統式溫度補償電路之缺點。但是電路特性與應用規格之不同，目前尚未有人達到低電壓頻率飄移精準之無晶體頻率產生器。

本篇論文主要提出共兩顆不同的具溫度電壓頻率補償之無晶體震盪器，一為具八個相位輸出，本電路實現於TSMC 18um混合訊號製程，供應電壓為1.8伏特並以環型震盪器為基底，採用兩點校正的方式，並找出所在之製程及溫度飄移後，使用簡易類比方式進行線性度修正增加量測精準度，提供具溫度製程補償之準確輸出。並在於面積極小的情況，達到相位間誤差小於5.5%以及duty Cycle 誤差小於4.3%，經修正後溫度係數為小於70ppm/℃，八相位頻率為192MHz之輸出頻率。

另一顆為超低壓具溫度補償之無晶體頻率產生器，本電路實現於TSMC 65nm混合訊號製程，供應電壓為0.5伏特，並提供一不具頻率電壓溫度影響且其輸出頻率為2.4GHz 之時脈，前端以環型振盪器及LC壓控震盪器以及數位電路構成製程選擇電路，校正頻率產生器因製程變異引起的偏移誤差。經選擇製程後由查看設計好的比較表後再經溫度補償。以低電壓的能帶隙電壓產生電路以及低電壓之溫度控制器產生一部隨溫度以及製程影響之電路；功率消耗為2.5mW/sample，操作溫度0°C~ 100°C，經查表修正後頻率誤差為33.47 ppm/℃。

本研究將以類比式無晶體頻率產生器之方法為主，保留原有之優點並朝高精準度補償為設計目標，以達到頻率飄移為50 ppm/℃ 之規格。此外傳統文獻中為了提高精準度於量測時採用兩點校正(two point calibration)之測試方法，增加了許多測試成本，此問題亦為本研究探討要點之一。

此外。為了維持論文的完整性，附錄A並收錄了利用了TCAD軟體模擬討論背電極對非晶體氧化銦鎵鋅(amorphous IGZO)之空乏層的影響，因為電子空乏效應，在高的功函數的背金屬下，電子都被金屬移走，而此行為導致了臨界電壓的增加，而利用了TCAD軟體的模擬，可發現增加通道長度以及減少厚度可以有效地增進此效應。而附錄B收錄了作者於博士班期間發表的另一篇有關玻璃基板的參考電壓電路。

DESIGN AND IMPLEMENTATION OF CRYSTAL-LESS CLOCK GENERATOR WITH PROCESS VOLTAGE TEMPERATURE COMPENSATION

Student: Ting-Chou Lu **Advisor: Dr. Ming-Dou Ker**

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Abstract

Process and temperature variations have become a serious concern for ultra-low voltage (ULV) technology. The clock generator is the essential component for the ULV very-large-scale integration (VLSI). MOSFETs is operated in the sub-threshold region are widely applied for ULV technology. However, MOSFETs at subthreshold region have relatively high variations with process and temperature. In this paper, process and temperature variations on the clock generators has been studied.

A multi-phase crystal-less clock generator (MPCLCG) with a process-voltage-temperature (PVT) calibration circuit is proposed in Chapter 3. It operates at 192 MHz with 8 phases outputs, and is implemented as a 0.18 μm CMOS process for digital power management systems. A temperature-calibrated circuit is proposed to align operational frequency under process and supply voltage variations. It occupies an area of 65μm ×75μm and consumes 1.1 mW with the power supply of 1.8 V. Temperature coefficient (TC) is 69.5 ppm/°C from 0 to 100°C, and 2-point calibration is applied to calibrate PVT variation. The measured period jitter is a 4.58-ps RMS jitter and a 34.55-

ps peak-to-peak jitter (P2P jitter) at 192 MHz within 12.67k-hits. At 192 MHz, it shows a 1-MHz-offset phase noise of −102dBc/Hz. Phase to phase errors and duty cycle errors are less than 5.5% and 4.3%, respectively.

Being operated with 0.5V supply voltage in a standard 65nm CMOS process, a new CMOS temperature compensated crystal-less clock generator. The bias current provided by the bandgap reference circuit and low-dropout operate amplifier are nearly independent of temperature due to the existence of mutual compensation of mobility and threshold voltage variation. The new proposed temperature compensated crystal-less clock generator functions well by the analog linear compensation mechanism. Chapter 4 presents an ultra-low voltage 2.4GHz CMOS voltage controlled oscillator with temperature and process compensation. A new all-digital auto compensated mechanism to reduce process and temperature variation without any laser trimming is proposed. With the compensated circuit, the VCO frequency-drift is 16.6 times the improvements of the uncompensated one as temperature changes. Furthermore, it also provides low jitter performance. We also discuss the time to digital converter system for time measurement unit in chapter 5.

The Appendix A shows the electron distribution in an amorphous indium–gallium–zinc-oxide (a-IGZO) thin-film transistor (TFT) with a floating metal–semiconductor (MS) back interface is analyzed using a technology computer-aided design (TCAD) model. The channel geometry (i.e., length and thickness) effect is carefully investigated. At a high work function (i.e., 5 eV) of the capping metal, the capping metal (electron depletion effect) mostly removes electrons inside a-IGZO. The depletion of the IGZO film leads to an increase in threshold voltage in a-IGZO TFT. TCAD simulation reveals that increasing channel length and decreasing IGZO thickness significantly enhance such an electron depletion effect. Finally, the electron depletion effect is applied to a-IGZO TFT with a high-conductivity IGZO film to greatly suppress the leakage current by over 5 orders.

The Appendix B shows a voltage reference circuits on poly-Silicon TFT. Because this paper is based on author’s master thesis, detailed contents could refer the author’s master thesis.

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Even the darkest night will end and the sun will rise. Victor Hugo, Les Misérables

謹以此篇論文獻給我摯愛的家人

陸亭州 於 2017/06/28

Contents

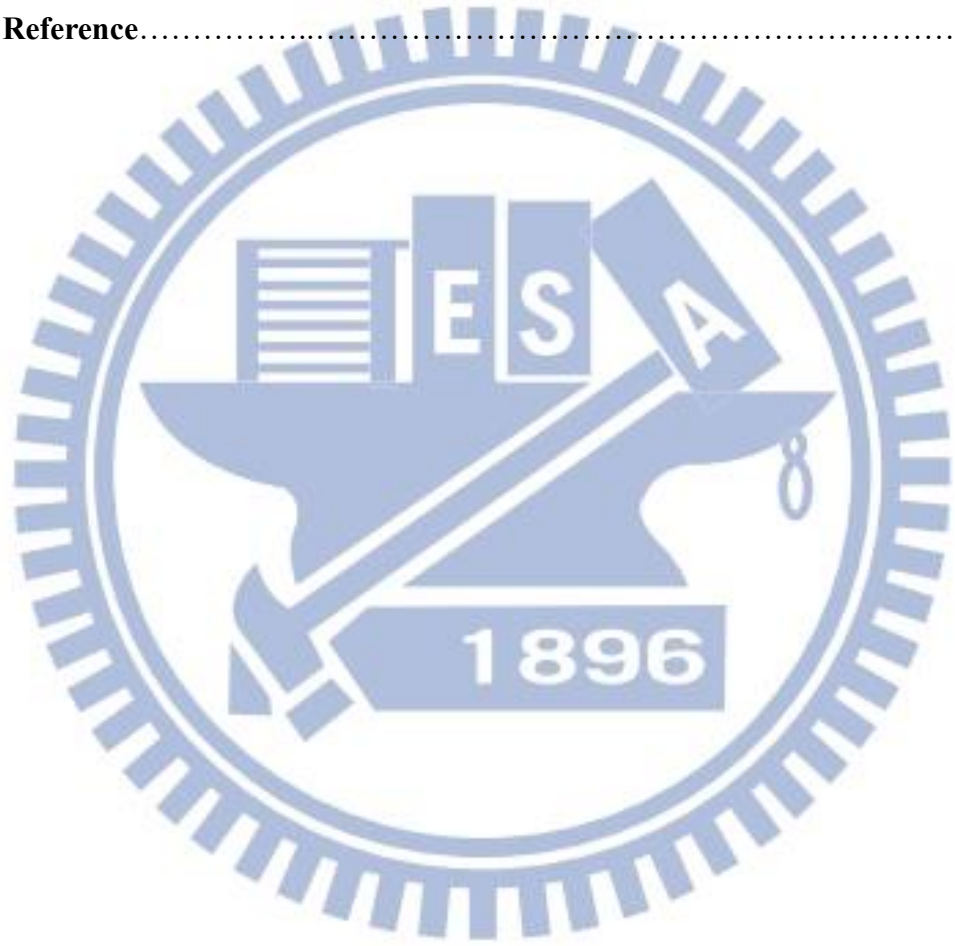
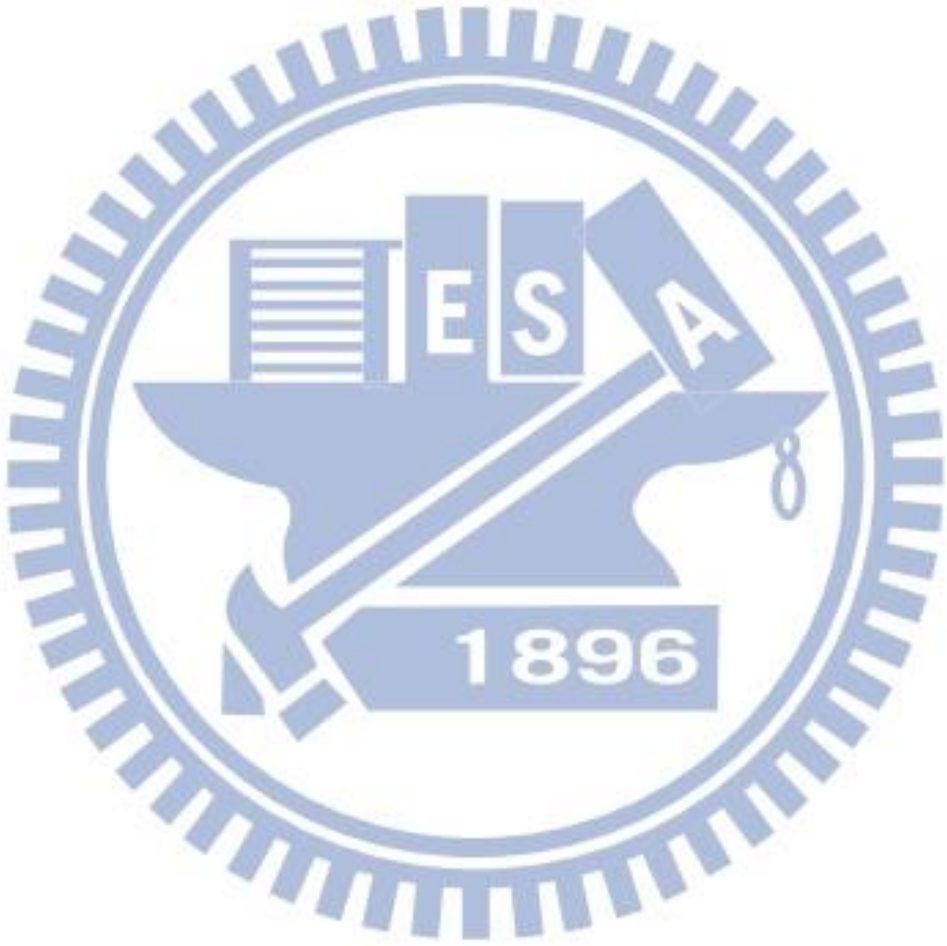


Figure Captions

Table Captions



Chapter 1. Introduction

This chapter deals with the background and the organization of this dissertation are discussed. First, the motivation of this thesis has been mentioned. Secondly, we discuss the delay variation of process, voltage, and temperature on VLSI system. And then the compensation methods for different clock references are introduced. Finally, the organization of this dissertation is well described.

1.1. Motivation

With the explosive growth of portable devices and biotechnology, wireless has become one of the most important design criteria in digital, analogy, and radio frequency (RF) circuits [1]. The clock generator is an essential component for such applications. However, power consumption and frequency drifts are the key factors to be overcome in the clock generator. The crystal oscillators (XOs) had been widely applied for most condition

XOs provide precise reference clock to PLLs or DLLs for high-speed applications. However, the crystal (XTAL) is an off-chip component with high power consumption [4]. Nowadays, crystal-less clock generators have been attracted by portable devices manufactories because their low cost, small size, and on-chip characteristics.

Figure 1.1 shows the comparison of XOs and CLCGs. We can find that temperature variations and phase noise are Process, voltage and temperature (PVT) variations are the critical factors of frequency drifts for clock generators. Typically, PVT compensations include material and electronic compensations [5], [6]. Material

compensation applies a substance with a positive temperature coefficient of frequency (TCF) in the resonator such as SiO_2 to neutralize the effect of negative TCF of the silicon resonator [7], [8]. Electronic compensations include off-chip and on-chip calibrations. Both mostly above methods combine proportional to absolute temperature (PTAT) circuit and the complementary to absolute temperature (CTAT) circuit to compensate temperature variations. Off-chip calibrations compensate the variation by off-chip circuits or external control signals [9], [10]. On-chip compensation, also known as auto calibrations, integrate sensors and compensated circuits and could all be accomplished in the chip [11], [12]. Since the additional testing procedure and off-chip circuitry are reduced, low cost will then become another advantage in on-chip compensation. Nowadays, on-chip compensation has been widely implemented with increasing precision [13], [14].

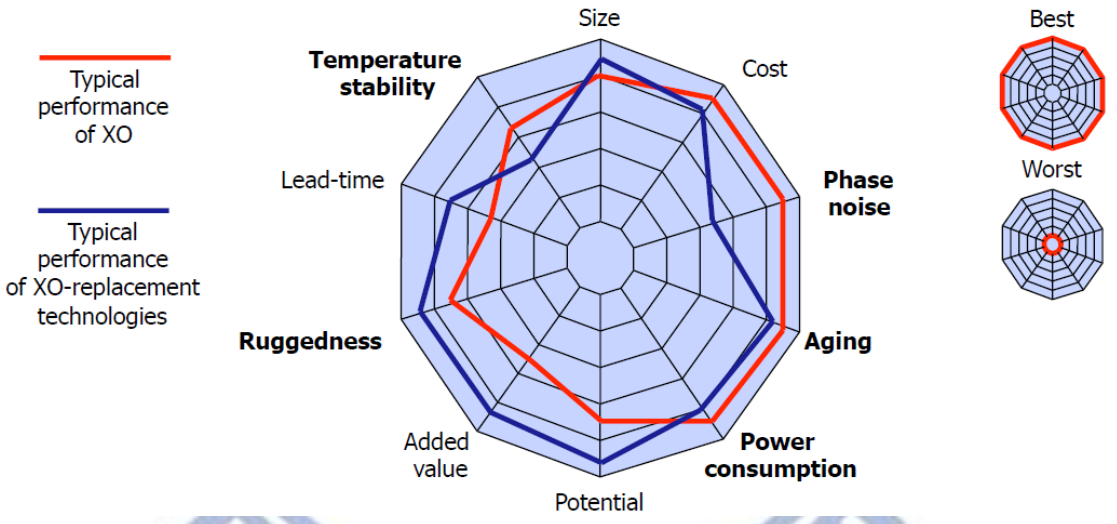


Figure 1.1 Comparison between XO and CLCGs [14].

1.2. **Analysis of PVT Variations of VLSI system**

Time domain (s)	*Mechanism*	*Delay impact approx. (3 sigma)* (%)
10^{12}	Lithography node	20
10^{9}	Electromigration	5
10^{8}	Hot-electron effect	5
10^{6}	Negative bias temperature instability	15
10^{4}	Chip electrical mean variation	15
10^{-1}	Across-chip L_{poly} variation	15
10^{-4}	Self heating/temperature	12
10^{-8}	SOI history effect	10
10^{-10}	Supply voltage	17
10^{-10}	Line-to-line coupling	10
10^{-11}	Residual source/drain charge	5

Table 1.1 Order of magnitude variability time domains and estimated delay impact [15].

Variability in delays of CMOS clock circuits arises from the very large-scale integrated (VLSI) circuit technologies beyond the ability to control specific performance-dependent parameters [15]

The variability is one of the most urgent problems to overcome. Delay variabilities can be temporal and spatial in nature [16] .The term spatial variation refers to lateral and vertical differences from intended polygon dimensions and films thickness. Temporally, the variability can occur across nanoseconds (such as residual source/drain charge and line-to-line couple) to years (such as electro-migration and lithography node) [17]; these are shown in Table 1 [18].

Spatial variation modes exist between devices, between circuits, between chips and across wafers, lots, and the lifetime of any particular fabrication system. There are lots of methods to describe device variability; one useful approach is shown in Table 1.2. Variations are separated into rows according to spatial and temporal variation. Temporal, irreversible device variation contributors are associated with age and device wear-out.

For instance, atomistic dopant variation, line-edge roughness and film thickness variation are belonging to spatial and device-to-device variation. These above-mentioned variations are also part of intrinsic device variability. The intrinsic variations are caused by atom-level differences between devices that occur even though the devices may have identical layout geometry and environment. Even though there is no systematic process variation between MOSFETs, there is still a fair wide Gaussian distribution of threshold voltage [19].

Mostly temporal variations such as environmental operating temperature, activity factor (how often and how long the device is on), are belonging to extrinsic variation. Comparing with intrinsic variations, it is typically not associated with fundamental atomistic problems, but rather with the operating dynamics of a modern fabricator. The reversible terms can be recovered by changing the environmental condition or compensated with circuitries. Irreversible terms couldn't be recovered after occurring, but can be prevented by serval process modified way.

Furthermore, a VLSI circuit composes of numerous devices spatially distributed over a relatively small area of silicon. There circuits are typically connected to one or more power supplies via a network of wire referred to as the on-chip power grid. Temperature and power-supply variations has emerged as important sources of design components. Local temperature variations within the die that cause It is common to have power-supply variations create a 10%variation in delivered power to different parts of design, and that same 10% variation can in turn cause a similar amount of delay variation.

Proximity	*Spatial*	*Temporal*	
		Reversible	*Irreversible*
Variation of chip mean	Parameter means (L_G, V_T, t_{ox})	Environmental operating temperature Activity factor	Hot-electron effect NBTI shift
Within-chip variation	Pattern-density/ layout-induced transconductance	On-die hot spots	Hot-spot-enhanced NBTI
Device-to-device variation	Atomistic dopant variation Line-edge roughness Parameter std. dev.	SOI body history Self heating	$\sigma_{VT\text{-}NBTI}$ (NBTI-induced V_T distribution)

Temporal—dynamic, time-dependent delay variation
Pattern density—variation caused by variation in density of polygons in given area
Hot spots—regions of excessive local heating caused by high power dissipation density
Hot-spot-induced NBTI—Threshold variation caused by excessive local heating
Self heating—Individual device heating caused by extended periods of high device current

Table 1.2 Categorization of device variations [15].

1.3.Analysis and Design of PVT Compensation for Clock System

According to section 1.1, process (including most spatial terms and σVT-NBTI), voltage (including activity factor), and temperature (including environmental operating temperature, on-die hot spots, and so on) variation are the important factors of delays. For the clocking system, the delay of devices directly affects output frequency. Therefore, PVT variations can be detected by sensing and cataloging above variations, and compensated by circuit design and process modification.

The amount of PVT variations for the clock systems depend on the oscillator catalog. For instance, crystal oscillator (XO) are relatively high precise and resistant as PVT variations occurs. However, there are still necessary to improve PVT variation for much more highly precise applications. The temperature coefficient (TC) of XOs with PVT compensations can be lower than 5 ppm. However, the crystal (XTAL) is an off-chip component with high power consumption. Therefore, the crystal less clock generator (CLCG) are widely applied in the digital or RF circuits.

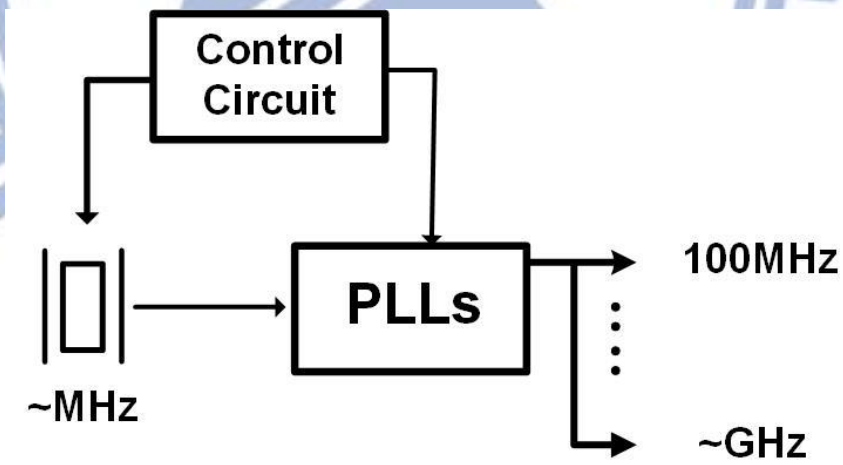


Figure 1.2 Block Diagram of XO systems.

Currently, crystal oscillators (XOs), micro electro mechanical systems (MEMS) oscillators and complementary metal-oxide-semiconductor (CMOS)-based oscillators are three main ways used to generate the reference clock signal. XOs provide highly precise and nearly temperature independent reference clock. However, the crystal

(XTAL) is an off-chip component with high power consumption. MEMS oscillators provide higher Q and better signal characteristic than CMOS-based oscillators, whereas need additional micro electro mechanical process to be integrated with traditional CMOS process [20].

MEMS oscillators provide higher Q and better signal characteristic than CMOS based oscillators, whereas need additional micro electro mechanical process to be integrated with traditional CMOS process. TC of MEMS oscillators are around 10 ppm where is between XOs and CMOS-based oscillators.

Furthermore, there are three kinds of CMOS based oscillators. The inductance-capacitor (LC) oscillators operate at high frequency [21]. The structure has high Q and low phase noise. It mostly targets at RF frequency synthesis. Relaxation oscillators repeatedly alternate between two states with a period that depend on the charging of a capacitor [22], [23]. Relaxation oscillators are also a stable LC based oscillator are with low phase noise [24]-[25]. All digital oscillator design can be integrated with digital signal processing (DSP) for portable and medical applications [26]-[28] Ring oscillators, Delay locked-loop (DLL), and phase locked-loop (PLL) are belonged to this catalog. Above these oscillators are with different circuit characteristics and PVT variations.

There are many PVT compensated methods for different oscillators and situations. The PVT compensated methods can be roughly divided into two parts, which are analog and digital. For example, figure 1.3 shows a traditional analog temperature compensated crystal oscillator (TCXO) structure [29]. It applies compensating circuits, such as thermistor or varactor diodes, to compensate the variations. Besides, the basic digital compensation circuits of TCXO. It applies a temperature sensor to detect the variation of temperature. Its results compare with coefficient table and compensate by logic and math function.

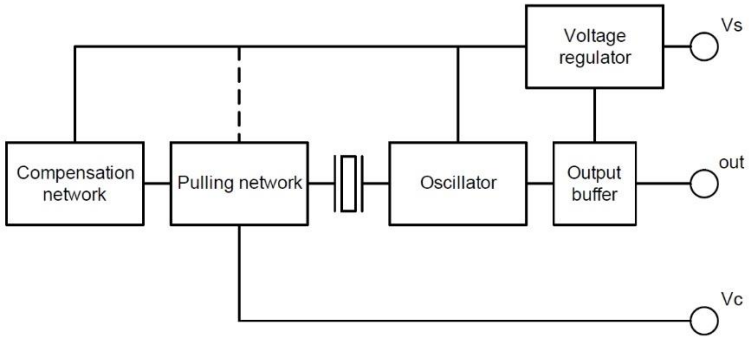


Figure 1.3 Block Diagram of Temperature [29].

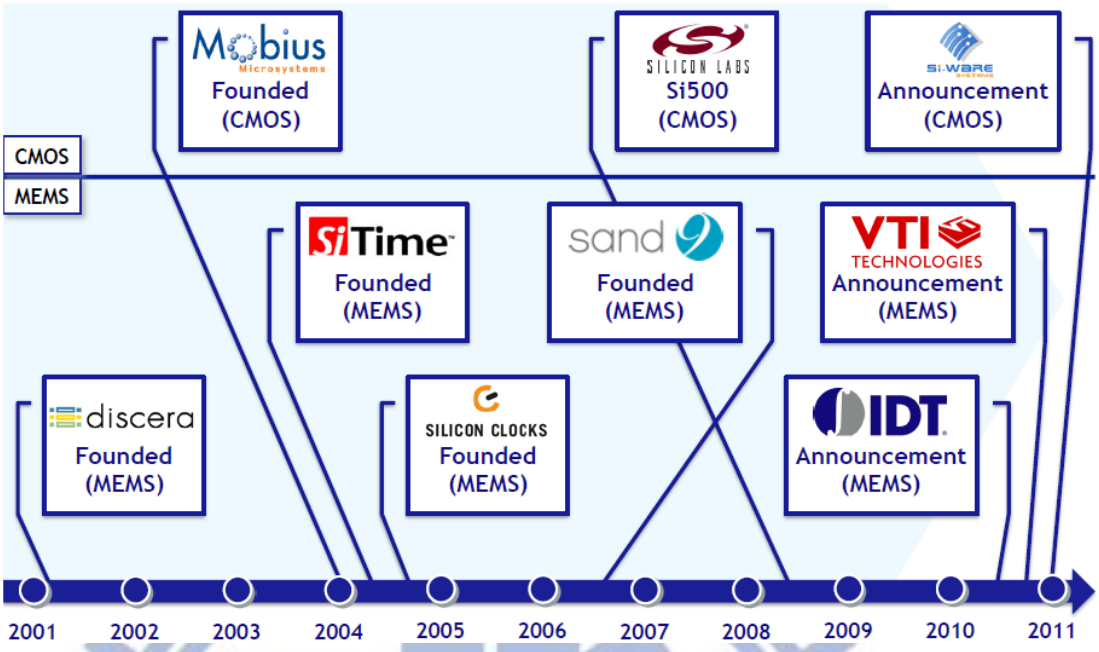


Figure 1.4 Main IC Supplies of CLCGs [28].

1.4. Thesis Organization

This dissertation is composed of seven chapters. This dissertation (chapter 2 ~ chapter 5) focuses on the clock generator with PVT compensation issues and the design of CLCG with auto-calibration under different situation.

This chapter provided an introduction on the challenges of the PVT variation of CMOS device and the relationship between devices and clock circuits. The catalogs of clock generators are described and the correspond PVT compensated method are also discussed in Chapter1

In Chapter 2, we discuss the operating principle of clock generators and accompanied noise. The basic noise of clock has been analyzed and their solutions. We will also discuss and analyze the characteristic of the conventional CLCGs and PVT compensated circuits. Lastly, the analysis and design issues of PVT compensated circuits for clocking circuits are presented.

In Chapter 3, One multi-phase crystal-less clock generator (MPCLCG) with a process-voltage-temperature (PVT) calibration circuit is proposed. It operates at 192 MHz with 8 phases outputs, and is implemented as a 0.18 μm CMOS process for digital

power management systems. A temperature-calibrated circuit is proposed to align operational frequency under process and supply voltage variations. It occupies an area of 65μm ×75μm and consumes 1.1 mW with the power supply of 1.8 V. Temperature coefficient (TC) is 69.5 ppm/°C from 0 to 100°C, and 2-point calibration is applied to calibrate PVT variation.

In Chapter 4, process and temperature variations on the clock generators has been studied. This paper presents an ultra-low voltage 2.4GHz CMOS voltage controlled oscillator with temperature and process compensation. A new all-digital auto compensated mechanism to reduce process and temperature variation without any laser trimming is proposed. With the compensated circuit, the VCO frequency-drift is 16.6 times the improvements of the uncompensated one as temperature changes. Furthermore, it also provides low jitter performance.

Chapter 5 summarizes the main results of this dissertation. Some suggestions for the future works are also addressed in this chapter.

Appendix A shows the electron distribution in an amorphous indium–gallium–zinc-oxide (a-IGZO) thin-film transistor (TFT) with a floating metal–semiconductor (MS) back interface is analyzed using a technology computer-aided design (TCAD) model. The channel geometry (i.e., length and thickness) effect is carefully investigated.

Appendix B shows a voltage reference circuits on poly-Silicon TFT. Because this paper is based on author's master thesis, detailed contents could refer the author's master thesis.

Chapter 2. Basics of CLCGs and Their Corresponding PVT Compensated Circuit

The chapter introduces the fundamentals of CLCGs and their PVT compensated circuits. We will discuss and analyze the characteristic of the conventional CLCGs and PVT compensated circuits. Lastly, the analysis and design issues of PVT compensated circuits for clocking circuits are presented. The analysis results specify the research directions of the thesis.

2.1. Operation Principle of Crystal-less Clock Generators and the Accompanied Noise

2.1.1. Operational Principle of Crystal-less Clock Generators

Oscillators are fundamentally nonlinear, and oscillator's nonlinearity is the reason for their stable amplitude. However, linear models are still often used to describe oscillatory behavior. That is acceptable as oscillation start-up condition because oscillation at stat-up is a small signal. Fig. 2.1 shows the linear model of oscillator.

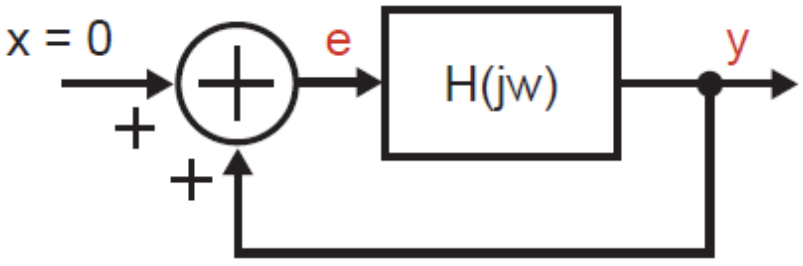


Figure 2.1 The block diagram of linear model for oscillator.

Where A(jω) is amplified gain and b(jω) is feedback network. Therefore, the closed loop gains G(jω) can be explained as

$$G(j\omega) = \frac{A(j\omega)}{1-A(j\omega)\beta(j\omega)} \quad (2.1)$$

From the Barkhausen's stability criterion, the self-sustaining oscillation at frequency ω_o if match the following conditions. The loop gain is equal to unity where $|A(j\omega)\beta(j\omega)| = 1$ and the phase shift around the loop is equal to $\angle A(j\omega)\beta(j\omega) = 2n\pi, where\ \ n \in 0, 1, 2, ...$ The linear model can yield a start-up condition and provide a rough estimate frequency of oscillation. However, the periodically stable frequency could be far different from the small signal linear prediction. That is because that the output doubles as the input doubles in a linear system. In an oscillator, it leads to an amplitude that is arbitrary [30].

2.1.2. Noise Analysis of Crystal-less Clock Generator

In the following section, we shortly discuss the noise from the crystal-less clock generators and analyze what kinds of noise we should handle. Fig. 2.2 shows the illustration of noise which occurs within time domain and frequency, respectively. Noticed that noise of amplitude variations suppressed by feedback in oscillator [31]. Jitter is the noise of the desired signal in time domain and phase noise is the same noise in frequency domain. The relationship between jitter at time-domain view and phase noise at frequency- domain view can be simply described. They are actually two sides of one; therefore, we discuss the jitter in theory and the main measured way of jitter are phase noise.

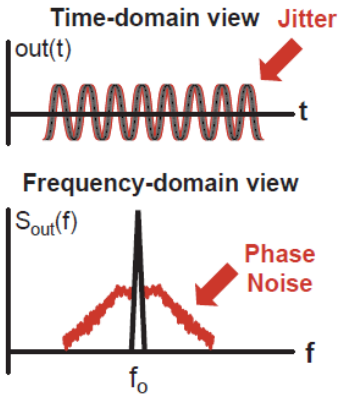


Figure 2.2 The block diagram of linear model for oscillator.

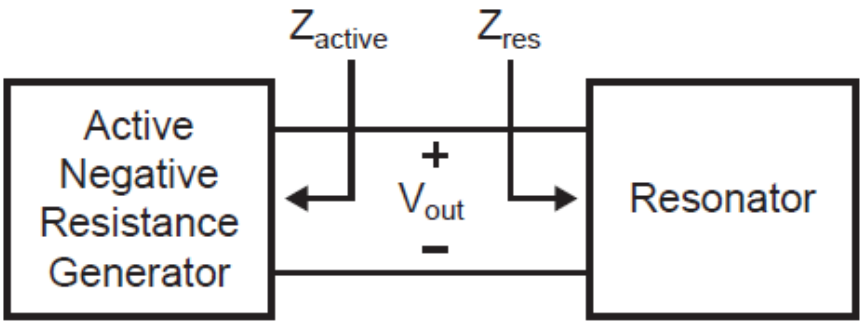


Figure 2.3 (a) The schematic diagram of CLCG. []

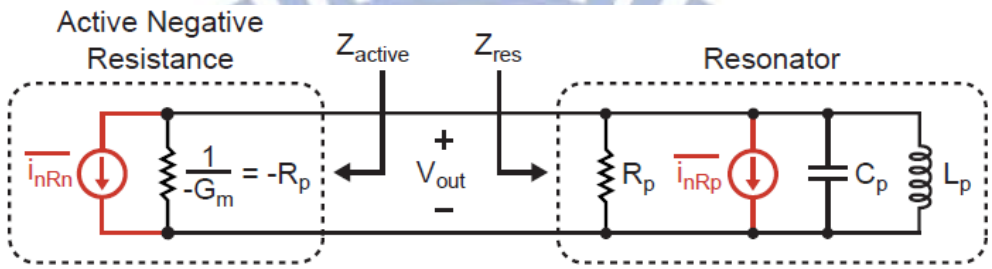


Fig. 2.3 (b)The noise and impedance schematic diagram of CLCG.

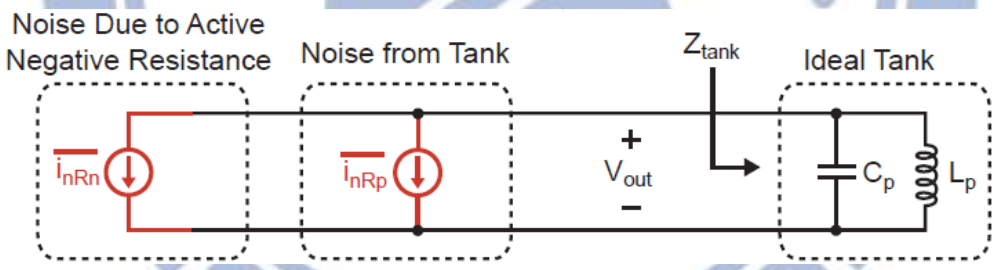


Fig. 2.3 (c)The noise and impedance schematic diagram of CLCG.

Fig. 2.3(a) shows the block diagram of a clock generator that includes an active negative resistance generator and a resonator. Fig. 2.3 (b) shows the impedance of active negative resistance and resonator. Where Z_{active} represents the active negative resistance and Z_{res} is the impendence of resonator. Then we split the noise source and ideal impedance in Fig. 2.3(c). Assume noise from active negative resistance element and tank are uncorrelated. Then, the expression represents total noise density that impacts both amplitude and phase of oscillator output are as below.

$$\frac{\overline{v_{out}^2}}{\Delta f} = \left(\frac{\overline{i_{nRp}^2}}{\Delta f} + \frac{\overline{i_{nRn}^2}}{\Delta f}\right)|Z_{tank}(\Delta f)|^2$$

$$= \frac{\overline{v_{out}^2}}{\Delta f}\left(1 + \frac{\overline{i_{nRn}^2}}{\Delta f} / \frac{\overline{i_{nRp}^2}}{\Delta f}\right)|Z_{tank}(\Delta f)|^2 \quad (2.2)$$

Where is $\frac{\overline{i_{nRn}^2}}{\Delta f}$ and $\frac{\overline{i_{nRp}^2}}{\Delta f}$ are the density of white noise current for the resistance and resonator, separately. $\frac{\overline{i_{nRp}^2}}{\Delta f} = 4\text{kT}\frac{1}{R_p}$ for single-sided spectrum. The tank impedance at a frequency Δf away from the resonance frequency ca be approximated by $|Z_{tank}(\Delta f)|^2 \approx \left(\frac{R_p}{2Q}\frac{f_o}{\Delta f}\right)^2$ as Q is tank quality factor. $\left(1 + \frac{\overline{i_{nRn}^2}}{\Delta f} / \frac{\overline{i_{nRp}^2}}{\Delta f}\right) = F(\Delta f)$. F($\Delta$f) is called as noise factor and it is taken as a constant in this derivation process. Besides, the single side band noise to carrier ratio is been defined as the following equation.

$$L(\Delta f) = 10\log\left(\frac{Spectral\ density\ of\ noise}{Power\ of\ carrier}\right) \quad (2.3)$$

Where spectral density of noise can be presented as $S_{noise}(\Delta f) = \frac{1}{R_p}\frac{\overline{v_{out}^2}}{\Delta f}$. Therefore, eq. () can be rewritten as.

$$L(\Delta f) = 10\log\left(\frac{S_{noise}(\Delta f)}{P_{sig}}\right) = 10\log\left(\frac{2kTF(\Delta f)}{P_{sig}}\left(\frac{1}{2Q}\frac{f_o}{\Delta f}\right)^2\right) \quad (2.4)$$

The above equation is the renowned Lesson's equation. Notice that only half of the noise is attributed to phase noise. This is due to a non-rigorous argument that the noise partitions to FM and AM noise and therefore only half of the noise contributes to the phase noise. The right hand side shows that the phase noise drops like $1/f^2$, an experimentally observed fact in a region of the spectrum. It's also clear that the Q factor is the key factor in determining the phase noise level.

However, the Lesson's equation is linear and time invariant. The more detailed insights into cyclostationary behavior, 1/f noise upconversion and impact of noise current modulation can be provided by Ali Hahimiri's thesis [32]. Besides, the related phase noise analysis can also refer Emad Hegazi and Jocob Rael's book [33].

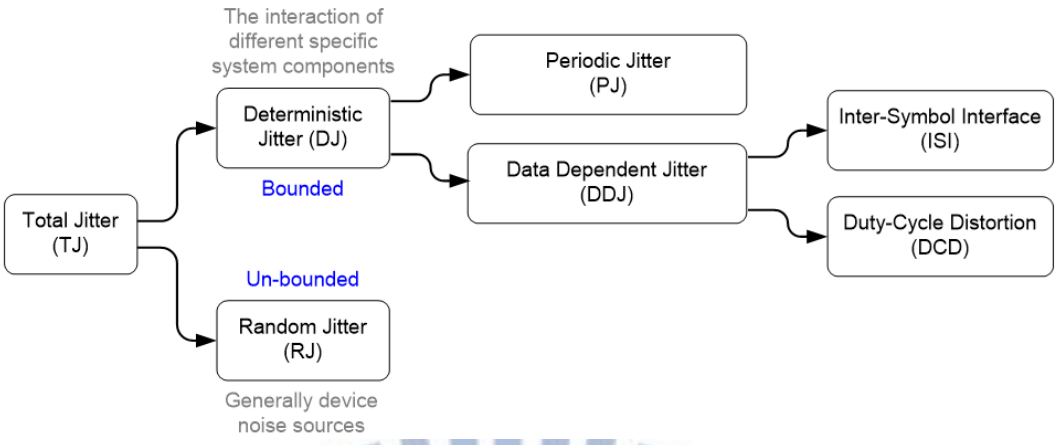
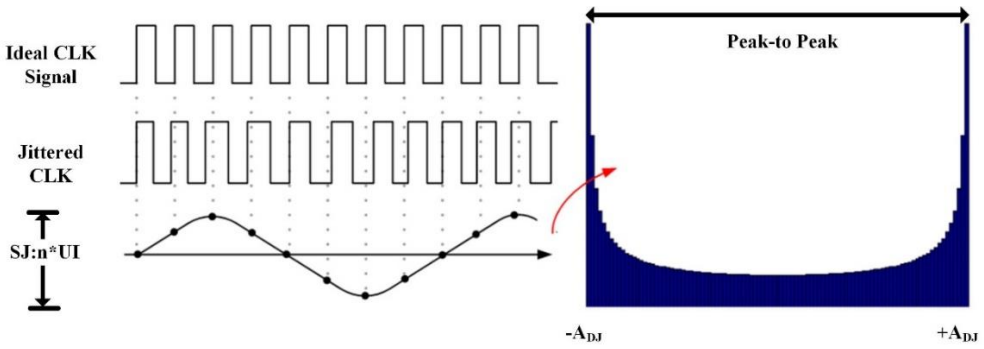


Figure 2.4 The noise and impedance schematic diagram of CLCG.

The phase noise is measured by the spectrum analyzer, and the measurement are executed in the following chapter. Because the jitter noise and phase noise are two sides of one where mentioned above this section, the next paragraph we discuss the category of jitter noise and related measured method. We can be easy to distinguish which noise should be considered by analyzing the category of jitter noise.

RJ is unbounded and there is a finite probability that random effects could cause a logic transition to appear anywhere, though, of course, the probability of an extremely large amount of RJ on a given transition is increasingly small. RJ usually belongs to Gaussian distribution or normal distribution. RJ is uncorrelated to the data. Besides, RJ is random in nature and does not occur with any predictable regularity.

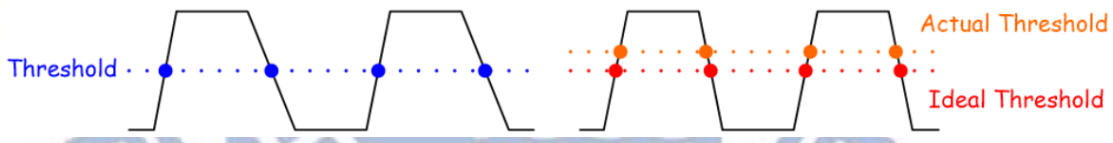
Fig. 2.4 shows the catalog of timing jitter noise. There are two major types of timing jitter, which are deterministic jitter (DJ) and random jitter (RJ). Deterministic jitter is defined as jitter that is bonded, with a well-defined minimum and maximum extent. There are a variety a deterministic data sources, mainly including periodic jitter (PJ) and data dependent jitter (DDJ). DDJ breaks down into the inter-symbol Interface (ISI) and duty-cycle distortion (DCD).



(a) (b)

Figure 2.5 (a)Time domain of DJ and (b) related jitter histogram.

Fig. 2.4 (a) shows the jitter due to a purely periodic jitter aggressor that is a single sinsoid periodic jitter which is caused by clocks or other periodic sources. Fig. 2.4(b) is the jitter histogram of the DJ. PJ is ultimately an example of periodic phase modulation and may be the most useful category. When a PJ peak is identified it can usually be associated with a noisy circuit element operating at that same frequency. The classic example is power supply feed-through, but PJ can also be caused by crosstalk from neighboring data lines or any other type of Electromagnetic Interference (EMI).



(a) (b)

Fig. 2.5(c) The noise and impedance schematic diagram of CLCG.

DDJ is correlated with the sequence of bits in the data stream. It most causes by the signal attenuation in the channel or non-linearity of circuitry. The typical example is inter-symbol Interface (ISI) and duty-cycle distortion (DCD). DDJ is a measure of asymmetry in the duty cycle of the transmitter. It can be classified by two main reasons. In Fig. 2.5(a), One is the mismatch between rising edge and falling edge caused by the charging rate or discharging rate which also means different slew rate (SR). Another is the drift of decision through which shown in Fig. 2.5(b). DCD most occurs in comparators or analog-to-digital converters (ADC).

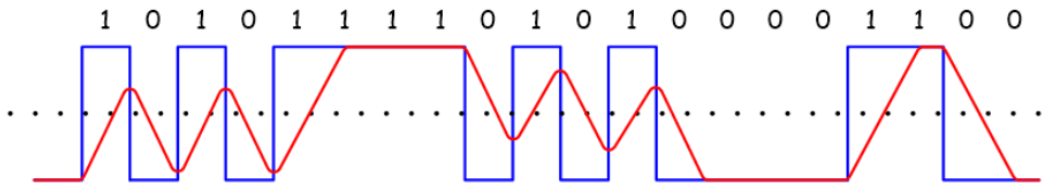


Figure 2.6The noise and impedance schematic diagram of CLCG.

ISI is caused by a combination of the design of the trace and circuit geometry, the media composing both the conductor and dielectric of the circuit, and the waveform of the transmitted signal. The effects include skin effect, dielectric loss, reflect, cross talk, dispersion and limitation of system bandwidth and so on. Fig. 2.6 represents the variation of edge response in time domain.

DDJ usually adjust the quality of system transmission, especially in receiving end. The clock data recovery circuit (CDR) process data retimed in the receiving data. For the CLCG, RJ and PJ are what should be concentrated on, and the related measurement will be revealed at the following chapter. In chapter 1, we mention the PVT variations are great influence on CLCG, and we will also discuss the relationship between jitter (phase noise) and PVT variations.

2.2. Overview of CLCG with PVT Compensation

2.2.1. CMOS-based Oscillators and Related PVT Compensation

CMOS-based oscillators are more and more attended due to the dimension and power consumption issues; although XOs and MEMS oscillators has much better stability than CMOS-based oscillators. In this section, three kinds of CMOS-based oscillators with their PVT compensation, which are mentioned in Section 1.3. would be discussed. Traditional CMOS-based oscillators have gradually been replaced by all digital for applications such as the internal control and the high-speed interfac. The low voltage, power and small area features of all digital CMOS-based oscillators bring enormous benefits. Relaxation oscillators repeatedly alternate between two states with

a period that depend on the charging of a capacitor. Inductance-capacitor (LC) oscillators operate at high frequency. The structure has high Q and low phase noise. It mostly targets at RF frequency synthesis.

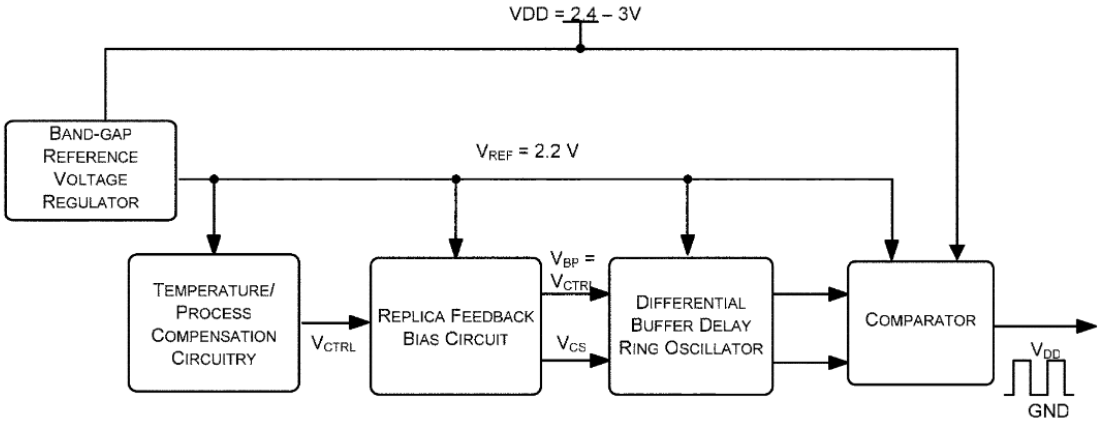


Fig. 2.7 The noise and impedance schematic diagram of CLCG [34].

Fig. 2.7 shows the block diagram of a previous traditional CMOS-based oscillator, which is based on a ring oscillator [34]. It contains a bandgap reference (BGR) voltage regulator, a temperature/process compensation circuitry, a differential buffer delay ring oscillator and a comparator. A bandgap referenced voltage regulator generates a supply and temperature independent reference voltage. It is primarily divided into two sub-circuits: A bandgap reference with a stacked CMOS topology [35] and a feedback transconductance amplifier that raises the output of the bandgap circuit from 1.25 V to 2.2 V. This serves as a stable temperature independent supply voltage for the oscillator and the supporting circuits. The system uses a voltage controlled differential ring oscillator to generate a reference frequency.

In the frequency compensation circuit, a threshold voltage sensing circuit generates a process-dependent reference voltage from V_{REF}, which is supplied to the temperature compensating circuit. The output of the compensation circuit is a control voltage, V_{CTRL}, which stabilizes the frequency of oscillation by varying a reference current, I_{REF}. The output of the oscillator is converted to a full swing rail-to-rail clock signal by a process independent voltage comparator [36] to make it compatible with standard digital logic and increase noise immunity. The comparator also ensures that the clock duty cycle stays at 50%.

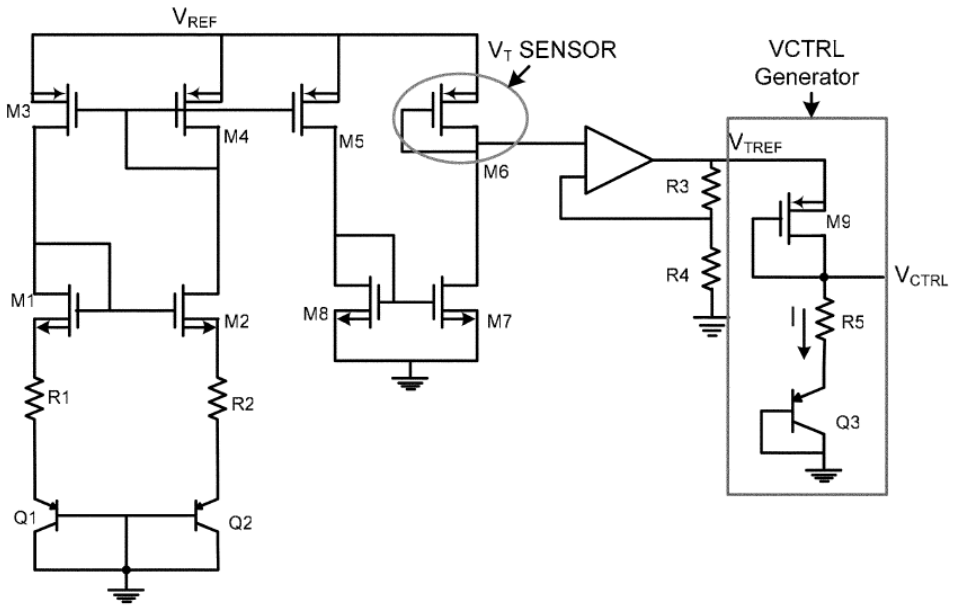


Fig. 2.8 Schematic of the basic temperature and process compensating bias generator [34].

Fig. 2.8 shows the schematic of the completely compensated circuits. The part of the circuit to the left is a self-biased reference circuit that provides a temperature independent current source, limited only by the matching of the resistors. The op-amp buffer stage boosts this reference level to (2.2 V under typical conditions) but is sensitive to the threshold voltage drift of M6.

The control voltage generator, VCTRL Generator, is implemented using a diode connected PNP transistor Q3 that provides a negative temperature coefficient. The temperature slope of can be adjusted through the ratio of M9. The temperature shift caused by the R3–R4 feedback in the amplifier is been ignored, since the effects cancel out to the first order. Therefore, the control voltage is been given by

$$V_{CTRL} = V_{TREF} - |V_{T9}| - \sqrt{\frac{2I}{\mu_p C_{ox}(W/L)_9}} \tag{2.5}$$

The temperature variation after compensation is down to$\pm$0.84%. The frequency stability is improved by more than 4.5 with the introduction of the compensation scheme. The average process variation within a single run at room temperature is $\pm$1.1% with compensation whereas it is almost $\pm$8% without it, a 7 X improvement.

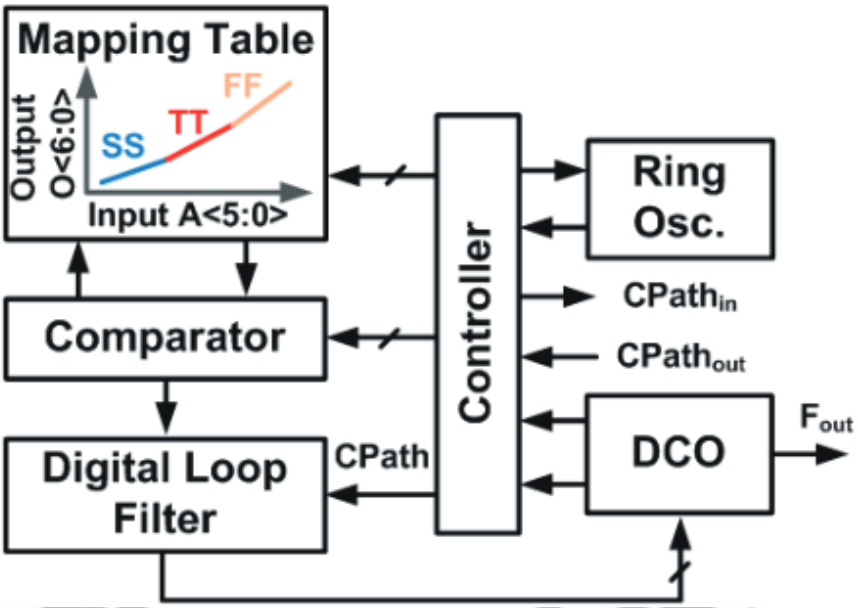


Fig. 2.9 Block diagram of all digital CLCG [26].

The all-digital CLCG uses frequency difference between the ring oscillator and the digital controlled oscillator (DCO) to create a mapping table under process and temperature variations [26]. The digital loop filter (DLF) adopts a successive-approximation register (SAR) algorithm for fast locking time. Fig. 2.9 shows the block diagram of the all-digital CLCG. It consists of a comparator, controller, a ring oscillator, a mapping table, a 9-bit digital loop filter (DLF), and a 9-bit digital controlled oscillator (DCO). The mapping table is based on process and temperature variations. In the mapping table detection (MTD), the frequency difference between the ring oscillator and the digital controlled oscillator (DCO).

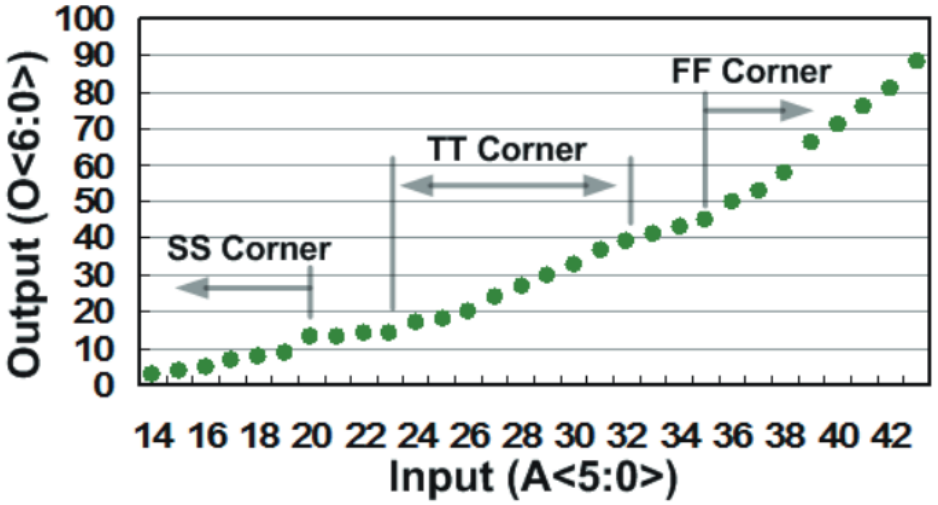


Fig. 2.10 Simulated results of mapping table [26].

The locking acquisition mechanism can be theoretically considered as a sequence of four operations:

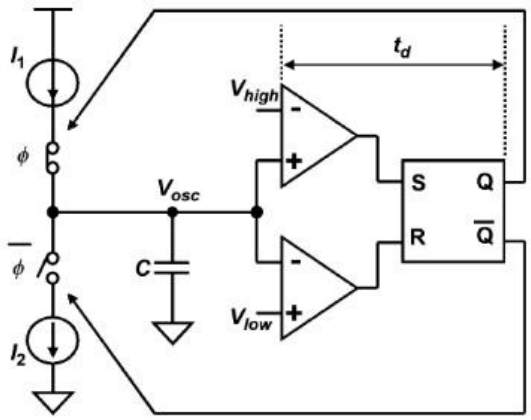
1. Initialization: After Start goes high, outputs of the registers must be set or reset. The frequency difference between the ring oscillator and DCO frequency is decided.

2. Mapping table detection: When the initialization is completed, the frequency difference between the ring oscillator and DCO frequency can find a mapping value in the mapping table. The simulated results of mapping table is shown in Fig. 2.10. Thus, the process and temperature of this chip can be defined.

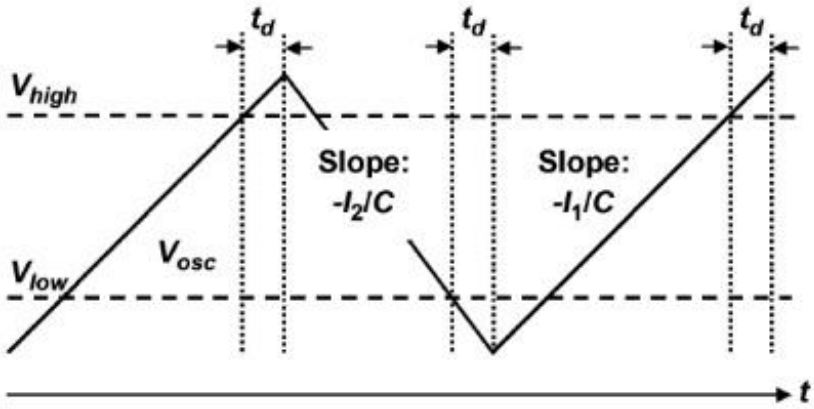
3. After completing mapping table detection, the DLF get the mapping value from the table and then the DLF uses the mapping value to achieve the target frequency of DCO. Therefore, the DCO output follows the DLF algorithm, which clock period is eight times as much as DCO output period.

4. Fine tuning track: Suppose the process and temperature variations affect the DCO operational frequency. At the fine-tuning stage, the CLCG can tune output frequency to reduce the process and temperature effects. The mechanism maintains that the function of the DSP system can work under the operational frequency of the CLCG. The CLCG was implemented in a one-poly nine-metal (1P9M) 65 nm CMOS process with power consumption smaller than 5 μW measured at 0.3 V. The locked frequency is 12 MHz, as well as the frequency draft is less than ±4.3% under the temperature from 0 to 100°C.

2.2.2. Relaxation Oscillators and Related PVT Compensation



(a)



(b)

Fig. 2.11 (a) Conventtional RC oscillator (b) Waveform

Fig. 2.11 illustrates a commonly known conventional relaxation oscillator [23].

Oscillation is performed by iteration of charging and discharging the capacitor as follows:

1) The voltage V_{osc} rises while charging C by I_1.

2) If $V_{OSC} > V_{high}$, a comparator sets RS-FF and changes the state of oscillator into discharging phase.

3) V_{OSC} falls while discharging C by I_2.

4) If $V_{OSC} < V_{low}$, another comparator resets RS-FF and the state returns to charging phase. The issues of this oscillator are as follows:

First, variation of comparator's delay t_d results in frequency variation with voltage and temperature. Second, aging of current sources (I_1, I_2) will degrade the accuracy of the slope of and varies frequency. Third, flicker noise of current sources (I_1, I_2) will degrade low offset-frequency phase noise or accumulated jitter.

A simple solution to obtain a stable and accurate oscillation is to shorten t_d to be neglected; however, this approach needs huge power to comparators so that it does not match with our motivation for low power dissipation. Therefore, the authors propose a feedback concept called voltage averaging feedback (VAF) to achieve both accuracy and low power dissipation by maintaining whole oscillation waveform

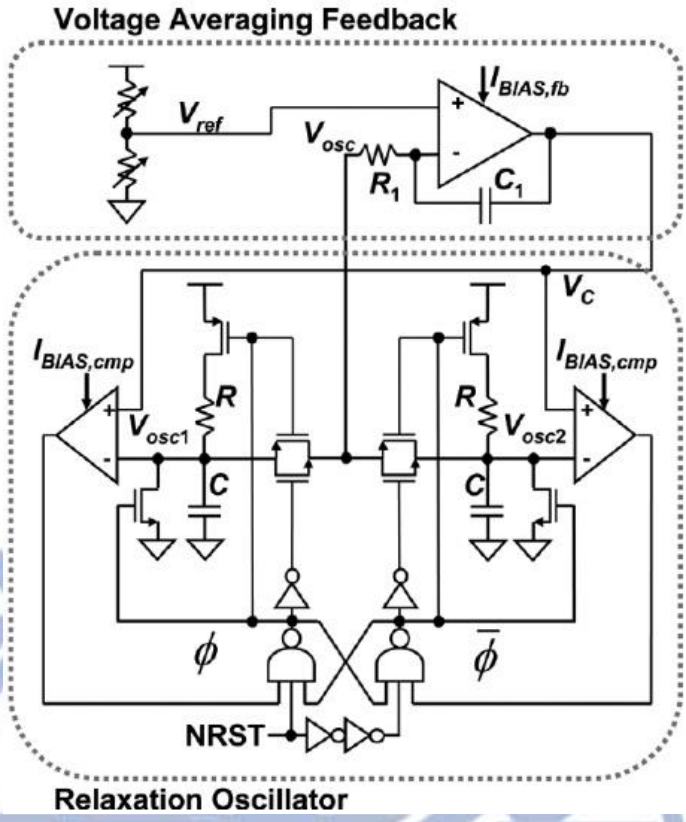


Fig.2.12 Voltage averaging feedback concept [23]

Fig. 2.12 shows the concept that comprises a complementary relaxation oscillator and an active filter for VAF, where the same complementary design is chosen for comparators and a feedback amplifier for rail-to-rail input and lass to obtain enough phase margin. The relaxation oscillator part is considered as a voltage-controlled oscillator with a control signal V_C. Oscillation waveforms V_{OSC1} and V_{OSC2} are summed up to and transferred to the active filter part.

By the measurement varying temperature at V_{DD} = 1.8 V and bias for comparator $I_{BIAS,cmp}$ =1μA, the oscillation without VAF resulted in a large variation of ±2.67% because of comparators' delay. On the other hand, the oscillation with VAF achieved ± 0.75%. Because temperature characteristic is mainly dominated by *R*, not comparators. Frequency variation reduced from 0.75% to 0.19% by blending diffused and polysilicon resistors with different sensitivities to temperature.

2.2.3. *LC Oscillators and Related PVT Compensation*

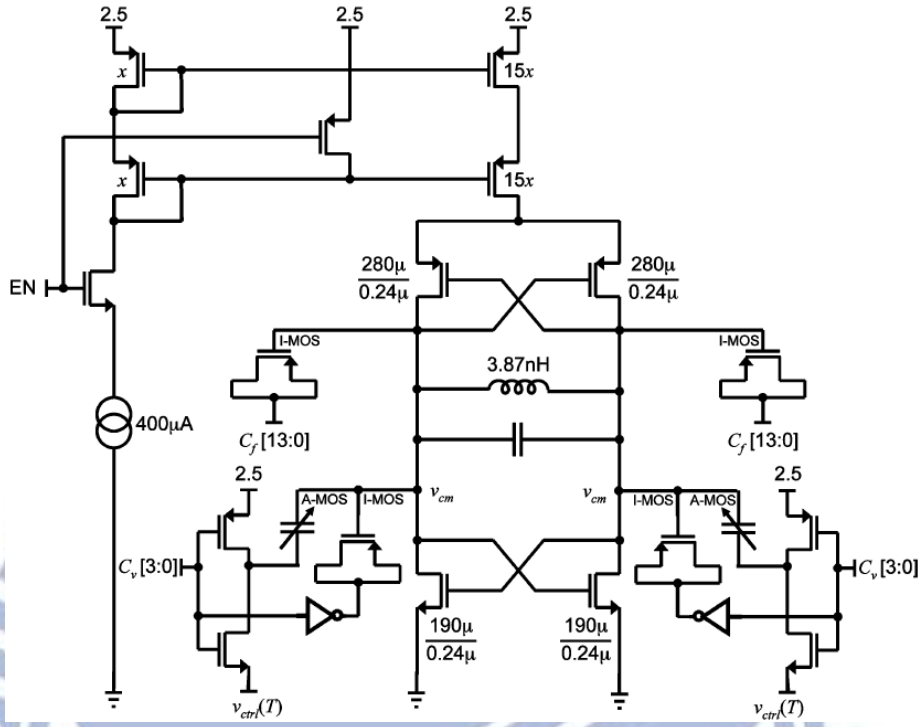


Fig. 2.13 800 MHz LC oscillator with PVT compensation [37].

The LC oscillator is shown in Fig. 2.13, where the topology is cross-coupled and complementary [37]. The target center frequency is 800 MHz, thus enabling division by 32 to generate 25 MHz, which is a typical reference frequency for Ethernet and similar protocols.

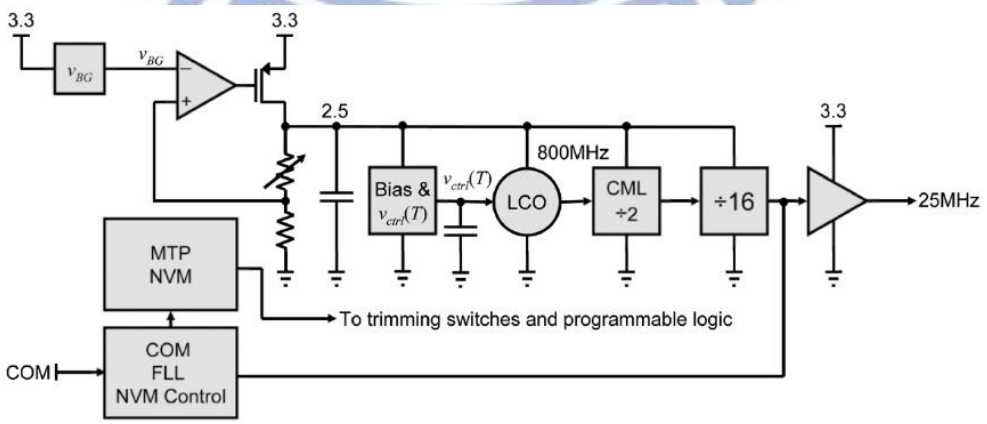


Fig. 2.14 Chip architecture of the whole circuitry.

The chip architecture is shown in Fig. 14. A bandgap-referenced and load-compensated low drop-out (LDO) regulator steps 3.3 V to the 2.5-V core voltage.

Trimming coefficients for the LDO, bias currents and the fixed and variable capacitors are stored in an 88-b multi-time programmable (MTP) NVM. Custom logic was synthesized to support the NVM interface, a simple serial communication interface, and a digital frequency-locked loop (FLL) for automatic nominal frequency calibration.

The FLL implementation has been demonstrated in [38]. The FLL determines the trimming coefficient for the I-MOS capacitor array that centers the LCO frequency by counting deep races between the LCO and a precision off-chip oven-controlled crystal oscillator (OCXO) such that the frequency discrepancy can be resolved. Once the FLL converges (typically within 100 ms), the coefficient is stored in NVM, loaded upon power-on reset thereafter, and the reference signal is never again required. The TC for 3.3V±10% and -10 to 80℃ is ±152 ppm.

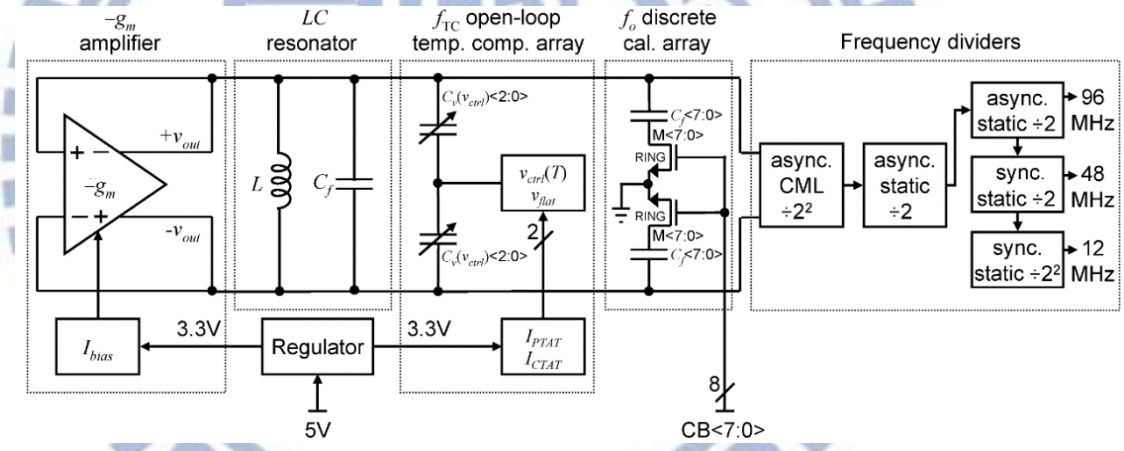


Fig. 2.15 The USB 2.0 compliant RF-TCHO clock generator architecture [23]

The prior art shown in Fig. 2.15 is a monolithic and self-referenced RF temperature compensated LC VCO [23], as each functional block is shown in simplified form as a module. A temperature and supply-independent current reference, I_{bias}, biases the –gm amplifier and maintains constant harmonic content in the LC network, thus minimizing bias-induced frequency drift. Temperature compensation is achieved open-loop with a reactive compensation method using a programmable array of accumulation-mode MOS (A-MOS) varactors that are biased by either a temperature-dependent voltage $V_{ctrl}(T)$, or by a temperature-independent voltage V_{flat}, both of which are derived from temperature-dependent current sources, I_{PTAT} and I_{CTAT}, along with resistors. The

uncompensated f_{TC} is expected to be negative due to the coil loss R_L. Consequently, V_{ctrl} (T) must increase over temperature to reduce the net tank capacitance and maintain the self-oscillation frequency. To account for process variation, programmable discrete frequency calibration was implemented as a switched-capacitor array with poly–insulator–poly (PiP) capacitors and nMOS switches.

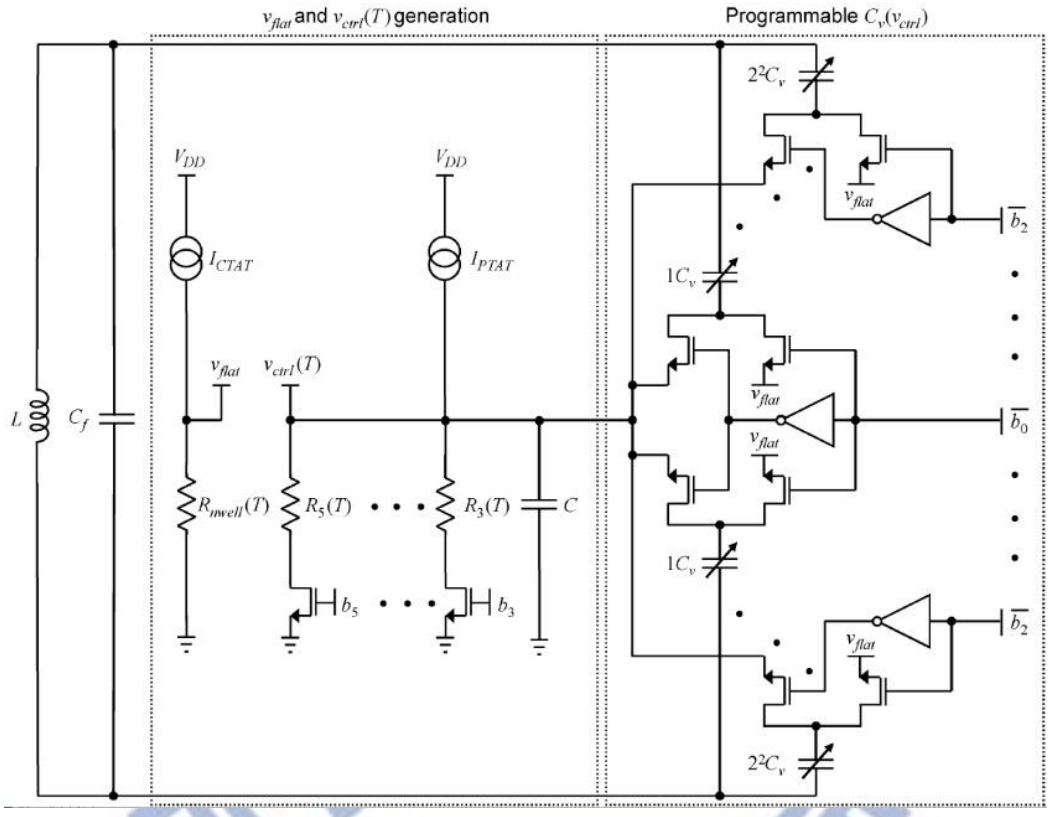


Fig. 2.16 Programmable binary-weighted array for discrete and monotonic self-oscillation frequency calibrations.

The open-loop reactive temperature compensation circuitry is shown in Fig. 2.16. The PTAT current I_{PTAT} is driven into one of three selectable resistor banks, all of the same magnitude, but of differing TCs depending on the type of resistors in the bank. The programmable resistor bank includes n-well, n-diffusion and poly-Si resistors, which exhibit positive TCs with decreasing magnitude, respectively. The PTAT voltage V_{ctrl}(T) is filtered across a large PiP capacitor C and sets the backgate voltage on a programmable array of A-MOS varactors. Three binary-weighted programmable varactor states exist. When a bit is set, the back-gate of the corresponding varactor is connected to V_{ctrl}(T) and when it is cleared, the backgate is connected to the

temperature-independent voltage V_{flat}, which is derived by sinking I_{CTAT} into an n-well resistor with a high positive TC. The array allows the oscillation frequency to remain constant, but the ratio of the temperature-dependent to temperature-independent capacitance to be programmed, thus modifying f_{TC}. Six bits program the open-loop TC circuitry, three of which control the resistor bank and three of which select the size of the A-MOS varactor. These bits are determined post-fabrication via a one-time full temperature characterization effort, stored in NVM for all devices, and loaded thereafter upon power-on rest. TC trimming for each device is not required. Results reported subsequently utilized the state where the net resistor included 80% n-diffusion and 20% unsalicided poly-Si resistors. The TC is +8.1ppm/°C.

2.2.4. Micro Electro Mechanical Systems and their PVT Compensation

Since the crystal is off- chip component with high power consumption, crystal-less clock generators have become widely applied for RF or VLSI circuits. Micro electro mechanical systems (MEMS) oscillators and CMOS-based oscillators that are mentioned at 2.2.1 are widely applied ways used to generate the reference clock signal.

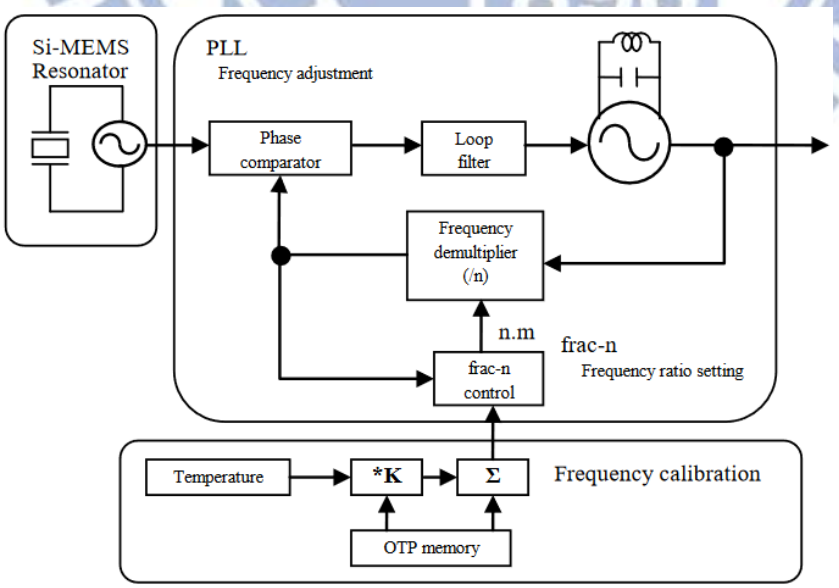


Fig. 2.17 The structure of MEM oscillator with temperature compensation [39].

A MEMS oscillator uses a silicon resonator as the oscillating source and requires a PLL circuit to correct the frequency for manufacturing tolerances and temperature coefficient. The basic structure of these oscillators is given in Figure 2.17. Like other CMOS oscillators, MEMS oscillators have a complex structure consisting of a resonator, a fractional-n PLL, and temperature compensation and manufacturing calibration. MEMS oscillators provide higher Q and better signal characteristic than CMOS-based oscillators, whereas need additional micro electro mechanical process to be integrated with traditional CMOS process [39]. Figure 2.18 shows the comparison of MEMS oscillator and XO. We can obviously find out that MEMS has a high jitter and high power consumption. No matter improving the jitter performance or reducing the power consumption, the performance of XOs are better than MEMS oscillators [40].

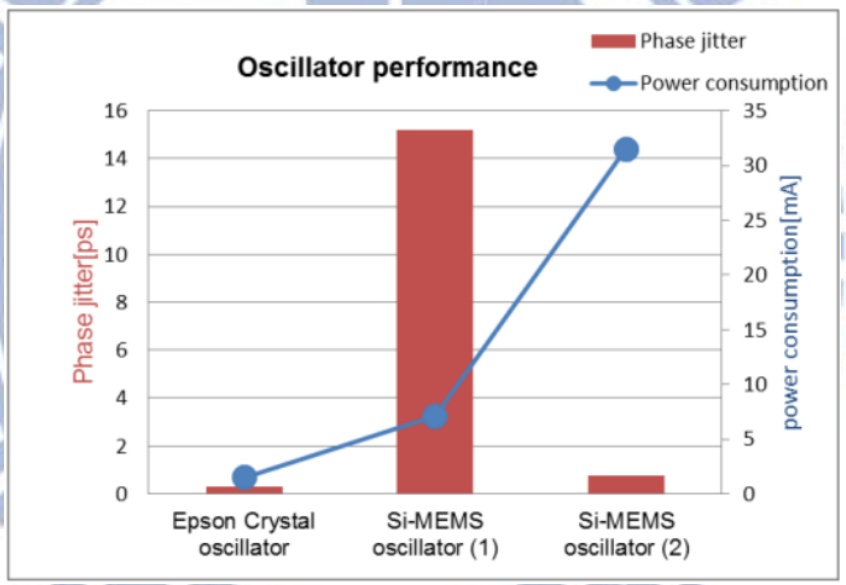


Fig. 2.18 Comparison between crystal and MEMS oscillator [40].

Figure 2.19 shows a novel conventional temperature compensated MEMS oscillators [41]. It consists of a main oscillator, a resistance temperature detector (RTD), a low-pass loop filter H(s), and a heater amplifier for the micro-oven. Two identical resonators are located next to each other on the same die. One is the oscillator and the other one serves as the micro-oven (with voltage applied across its body). The RTD circuit extracts the resonator temperature information – structural resistance, compare it with a reference resistor (R_{REF}) and then generates a resistance error signal to the low-pass loop filter H(s). The main objective of loop filter is to provide a high gain so as to

suppress the resistance error and minimize the micro-oven temperature drift. The micro-oven adjacent to the main resonator is controlled by this feedback loop automatically and hence achieves an active temperature compensation. Without compensation, the overall frequency drift is about 2000 ppm. After applying proposed temperature compensation scheme, the frequency drift is greatly reduced to ±5.5 ppm.

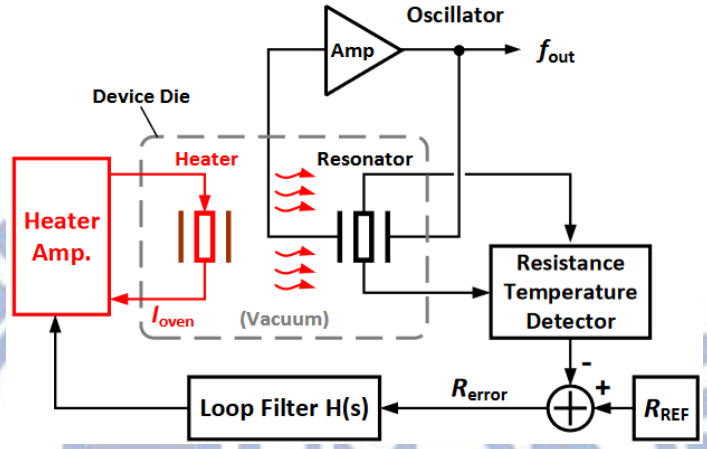


Fig. 2.19 Comparison between crystal and MEMS oscillator [41].

Although MEMS oscillators provide higher Q, better TC (about 10ppm through 70 degree), and better signal characteristic than CMOS-based oscillators, MEMS oscillators need additional micro electro mechanical process to be integrated with traditional CMOS process.

Chapter 3. An 8 phases 192 MHz Crystal-less Clock Generator with PVT Calibration

This Chapter is briefly depicted an 8 phases 192 MHz crystal-less clock generator with PVT calibration in a 0.18 mm CMOS process. The proposed design architecture offers benefits. First, the PVT calibrated CLCG architecture can compensate the process, voltage, and temperature variations. Whether the clock system is positive or negative TC, the calibrated mechanism can make sure that the clock system can be compensated under various situations. Second, a voltage controlled oscillator and a phase error corrector can stabilize the 8 phases' outputs under diversified situation. Third, this design applies a level shift instead of tap buffers to amplify the output swing; therefore, it can guaranteed full swing outputs. Final, the dimension of our proposed design are so small that can be widely applied in VLSI circuitry.

3.1. Architecture of CLCG with PVT compensation Circuit

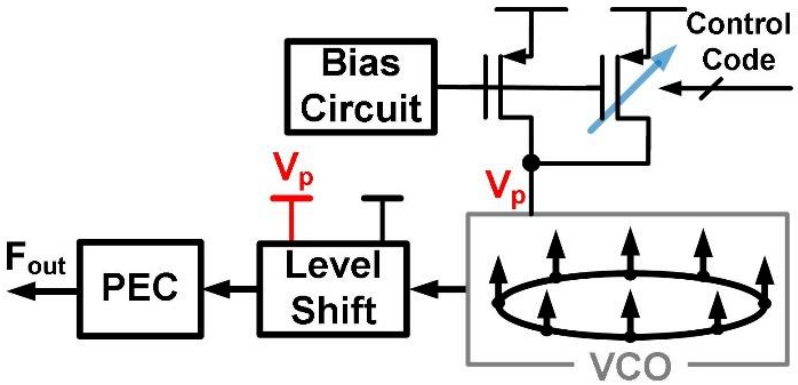


Figure 3.1 Block diagram of the proposed CLCG.

Fig. 3.1 shows the structure of the proposed multi-phase PVT calibrated CLCG. It includes a ring oscillator, a phase error corrector (PEC), a level shifter and a bias circuit.

The bias circuit consists of current source and a PVT calibrated circuit. The PVT calibrated circuit effectively improve the resistance of PVT variation. The PEC circuit reduces phase error, which mainly occurs at the mismatch of each phase. The level shifter amplifies the output swing to ensure full swing outputs.

3.1.1. Crystal-less Clock Generator and Phase Error Corrector Circuit

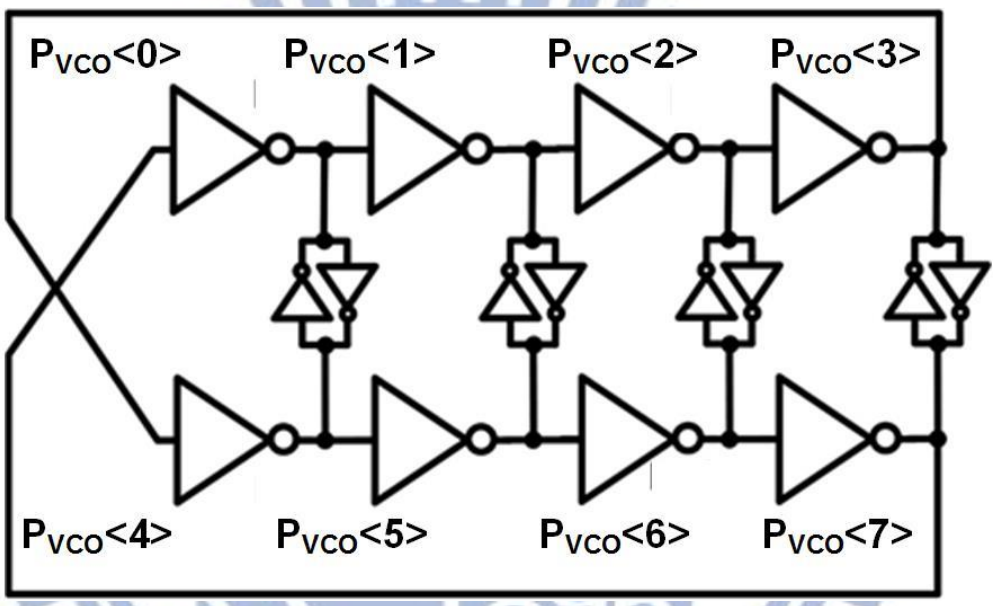


Figure 3.2 Schematic of the 8 phases differential ring oscillator.

The schematic of the applied voltage controlled oscillator (VCO) is illustrated in Fig. 3.2. This structure applies The VCO adopts 4 stages differential cell with 8 phases outputs. The delay cells are differential cell, and detailed schematic is shown as below. The latches are weak inverters, which can keep P<0> and P<4> truly inverted and reduce the mismatch from the multi-phase delay. The advantage of differential ring cell is it can provide even phase outputs symmetrically. Comparing to traditional ring oscillators, the differential ring oscillators can realize even outputs. The docking inverter pairs, which connect Pvco <1> and Pvco <5>, can effectively balance the phase-to-phase error.

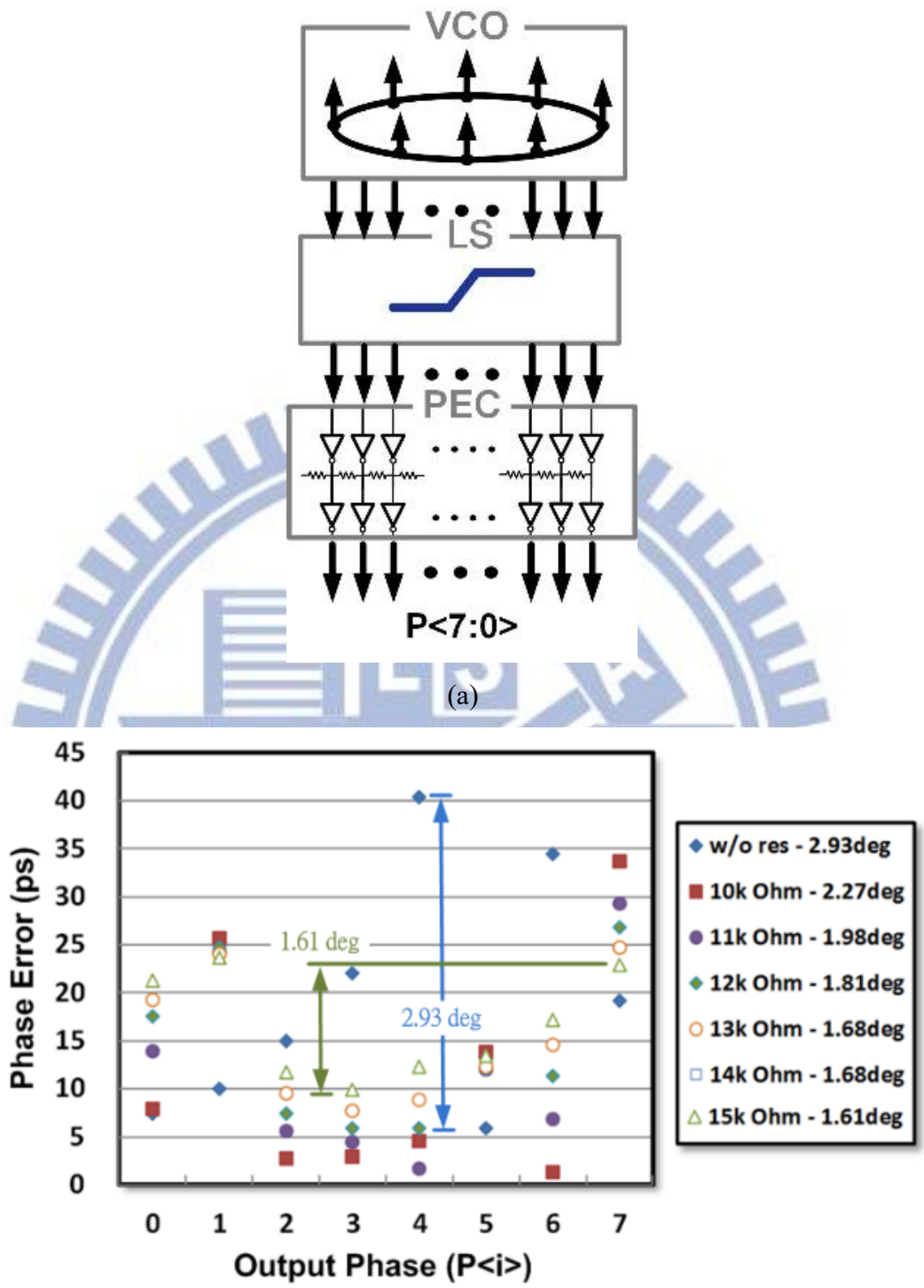


Figure 3.3 (a) Block diagram of the VCO, LS, and PEC, and (b) simulated result between output phase and phase error.

Fig. 3.3 illustrates the circuit of VCO with a phase error correct (PEC) circuit. The

phase error mainly occurs at the mismatch of each phase. The circuit routing of the ring oscillator and process variation are the major reasons. The PEC circuit applies resistors between each phase to balance the mismatch. Fig. 3.3(b) shows the relationship between output phase and phase error. The phase error without PEC circuit is 40.5 ps (2.93˚) at P<4>. The PEC circuit adopts 15k Ohm to achieve the minimum phase error, which is 1.61 ˚. Thus, the PEC can reduce the 45% phase error [42].

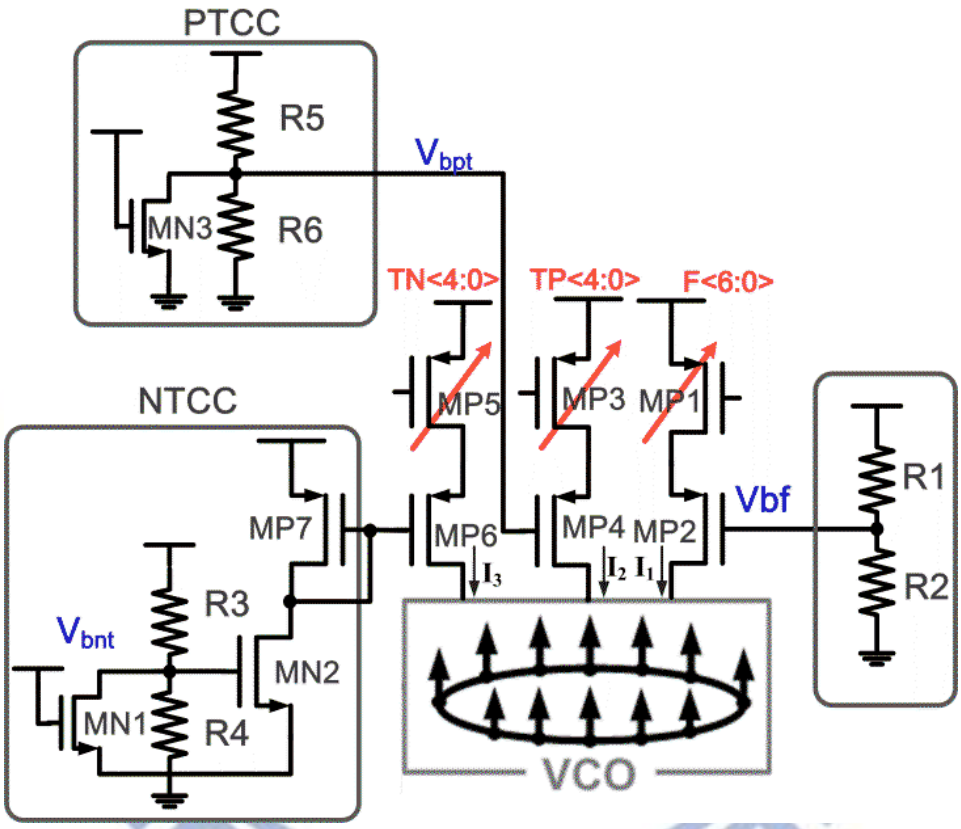


Figure 3.4 Block diagram of the PVT calibrated circuit.

3.1.2. PVT Calibrated Circuit

The modified PVT calibrated CLCG architecture is demonstrated in Fig. 3.4. The calibrated circuits calibrate the variation by digital controlling bias circuit. There are three PVT calibrated mechanisms for CLCG. The digital code, F<6:0>, can calibrate the process and frequency variations. The digital code, TP<4:0>, can calibrate the positive temperature variation and the digital code, TN<4:0>, modifies the negative

temperature variation. The frequency calibration consists of MP1, MP2, R1, and R2. F<6:0> can control the current I_1, which can modify the VCO frequency. R1, R2, and MP2 are the bias circuit. The bias voltage V_{bf} is as follow.

$$V_{bf} = V_{DD} - (V_{SD(MP1)} + V_{SG(MP2)}) = \frac{R_2}{R_1+R_2} V_{DD} \quad (1)$$

where V_{SD}(MP1) and V_{SG}(MP2) are the source-to-drain voltage of MP1 and the source-to-gate voltage of MP2, respectively. The voltage division of resistance has to keep MP2 operate at the saturation region.

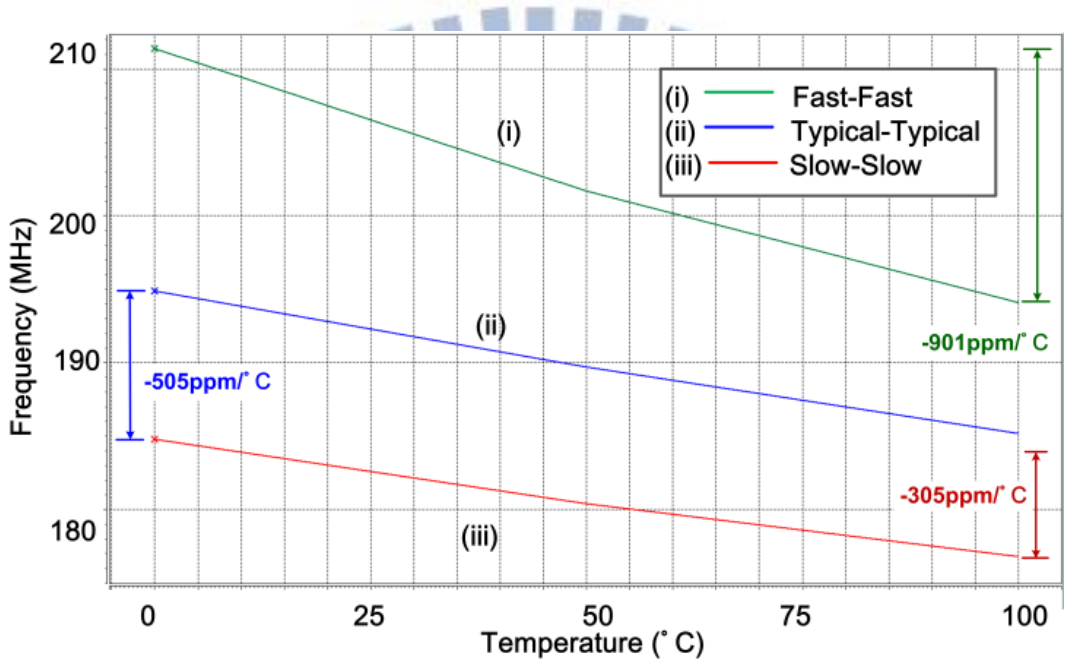


Figure 3.5 Simulated frequency versus temperature for the proposed DCO without temperature calibration.

Simulated frequency versus temperature for the CLCG without temperature calibrations is shown in Fig. 5. Temperature coefficients (TC) are -350, -505, and -901 ppm/˚C of slow-slow (SS), typical-typical (TT) and fast-fast (FF) corners, respectively. The TC of CLCG are all negative temperature coefficients. The negative temperature coefficient calibration (NTCC) circuit calibrates negative TC. MP5, MP6, MP7, MN2, MN3, R5, and R6 consist of the NTCC. TN<4:0> can control the current I_3, which can modify the VCO frequency. MP6 and MP7 can transfer the calibrated current to I3.

The simulated results of the temperature calibration part are shown in Fig. 3.6. The temperature calibration circuit consists one transistor Ma and two bias resistors Rbias1

and Rbias2. The MOSFET drain current ID is expressed as

$$I_D \propto \mu(T)(V_{DD} - V_{TH}(T))^{\alpha} \quad (2)$$

The threshold voltage V_{TH}(T) and mobility μ(T) have temperature dependence [43], [44] as follows.

$$V_{TH}(T) = V_{TH}(T_0) - k(T - T_0) \quad (3)$$

$$\mu(T) = \mu(T_0)(\frac{T}{T_0})^{-m} \quad (4)$$

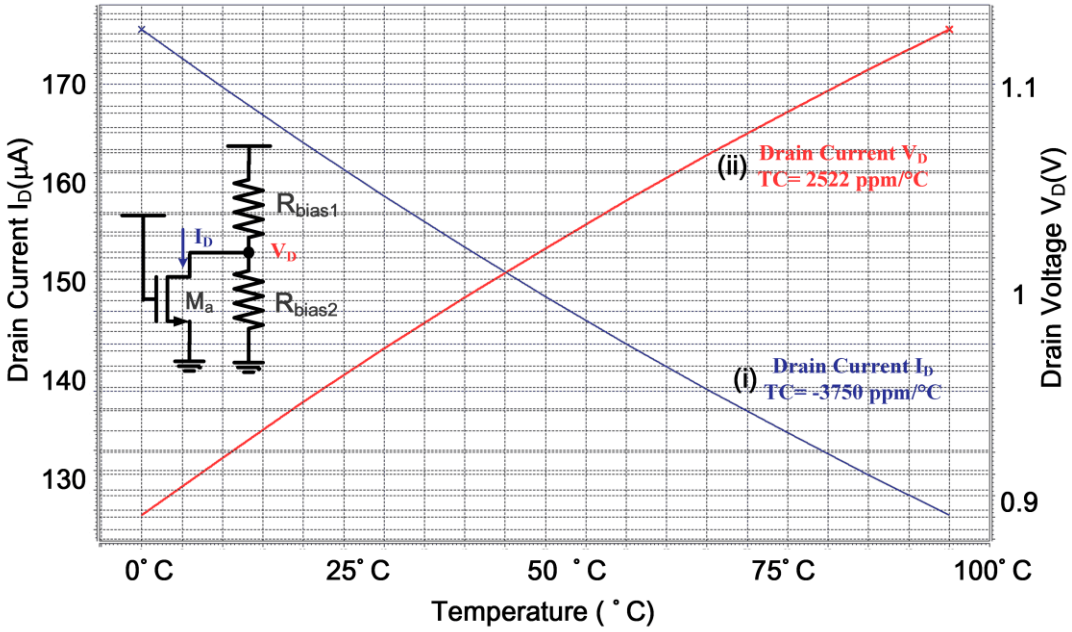


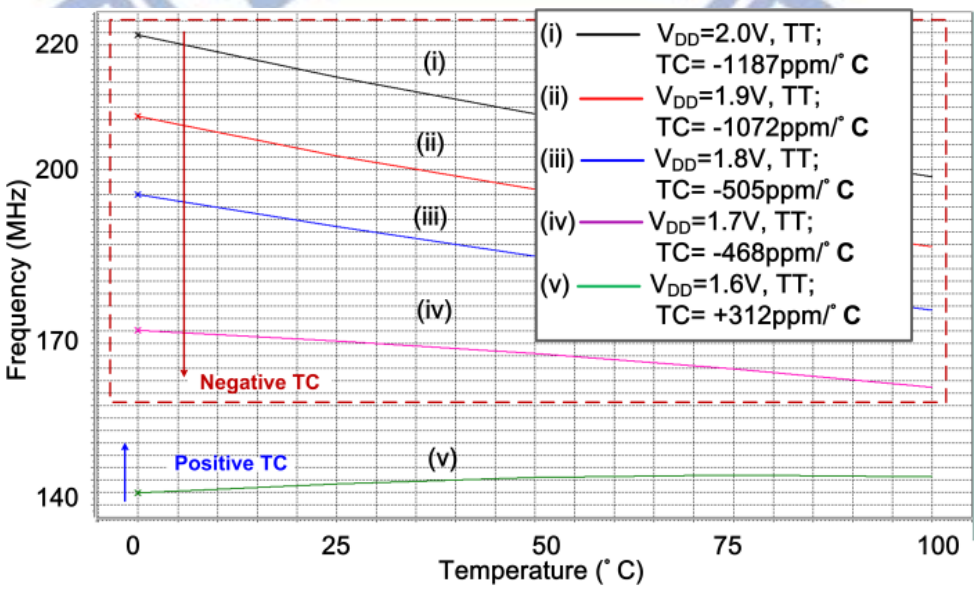
Figure 3.6 Simulated drain current I_D and drain voltage V_D versus temperature for the temperature calibration part.

where T is the present temperature and T_0 is the room temperature (T_0=300K). α typical assumes 2. k is the threshold voltage temperature coefficient whose typical value is 2.5mV/K. m is mobility temperature exponent whose typical value is about 1.5~2. Both μ and V_{TH} are negative temperature coefficient. The effect of drain current by μ is much higher than that by V_{TH} as V_{DD} and V_{TH}(T) are relatively large, such as V_{DD}=1.8V and V_{TH} =0.7V [45]. Fig. 7 shows the same trend of drain current versus temperature where drain current is negative TC = -3750 ppm/°C. On the contrary, the effect of drain current by V_{TH} is higher than that by μ as V_{DD} and V_{TH}(T) are relatively small, such as V_{DD}< 1V and V_{TH} =0.7V

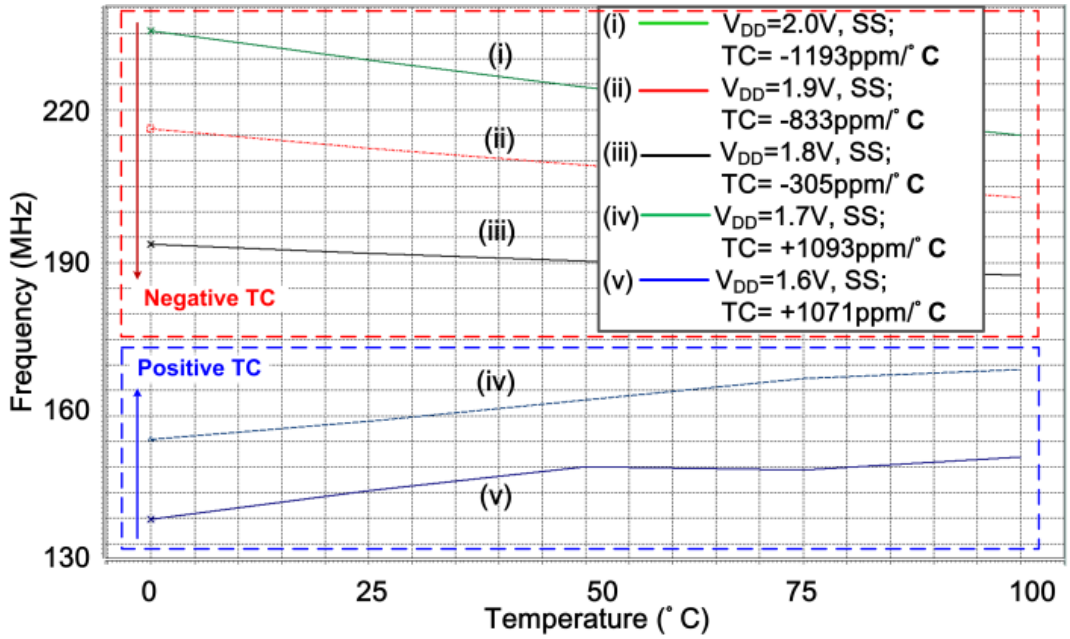
The NTCC circuit consists of the temperature calibration part and a pair of current mirror. The temperature part includes R5, R6, and MN2 . It produces the positive TC bias voltage V_{bnt}. V_{bnt} controls the drain current of MN2, $I_{D(MN2)}$. As V_{bnt} increases with temperature, $I_{D(MN2)}$ increases with temperature. With MP6 and MP7, I_3 is approximately proportional to absolute temperature (PTAT). Therefore, the output frequency can be pulled up with temperature by bias current I_3. The PTAT current modifies a negative temperature coefficient via digital code, TN<4:0>.

Fig. 3.7(a) is the simulation results of the frequency accuracy of CLCG under TT corner with supply voltage variation. TC are 312, -468, -505, -1072, and -1187 ppm/˚C of V_{DD} =1.6 V, 1.7 V, 1.8 V, 1.9 V, and 2.0 V. However, TC turns to the positive temperature coefficient as reducing the supply voltage of 1.6 V. As the MOS device has a large current, the CLCG can obtain a negative temperature coefficient easily.

When process corner and supply voltage variations (SS corner and low supply voltage), the CLCG becomes a positive temperature coefficient. For example, Fig. 3.7(b) shows the simulation results of the frequency accuracy of CLCG under SS corner. The TCs with V_{DD}=1.6 V and V_{DD}=1.7 V become positive temperature coefficients. It leads that the negative temperature calibrated circuit can't be applied under low voltage supplies. The main reason is that the additional bias circuit reduces the head room of the VCO. Applying long channel length devices of the oscillator keeps TC staying in a negative temperature coefficient. Besides, introducing the positive temperature calibrated circuit (PTCC) is the low cost and low power consumption way.



(a)



(b)

Figure 3.7 Simulated frequency versus temperature for the proposed VCO under(a)typical-typical and (b)slow-slow corner with supply voltage variation.

MP3, MP4, MN1, R3, and R4 consist of the positive temperature calibration, which is the same as Fig.6. TP<4:0> can control the current I_2, which can modify the frequency. As V_{bpt} increases with temperature, $I_2=I_{D(mp4)}$ decreases. Therefore, I_2 is complementary to absolute temperature (CTAT). The CTAT current modifies the positive temperature variation by digital code, TP<4:0>.

3.1.3. Level Shifter

Buffers are widely applied to amplify the digital signals. As the operating voltage increases to a high voltage, the output signal couldn't be properly amplified to full swing or even turn off to zero. The schematic of level shifter is shown in Fig. 3.8. The level shifter amplifies the output swing to ensure full swing outputs. The output signal of VCO provides low voltage supply (V_{DDL}) input signal (P_{VCO}<i>) to level shifter. The function of two NMOS devices with gate connection to $P_{VCO}<i>$ and $\overline{P_{VCO}<i>}$ is speed up the transition and avoid glitch during the transition. For example, as

Pvco<i>=0 and bar Pvco<i>=1, Gate of MP1=0 and MP1 is tuned on. MN3 also is tuned on to provide additional current. Fig. 3.9 shows the simulation with and without the two NMOS devices. It apparently finds that there are glitches which slow down the transition. The input signal which is low voltage level ensures that the CLCG could produce high voltage level output signal P_{LS}<i> under a low voltage supply. Furthermore, the power consumption of level shifter is lower than traditional buffers [46].

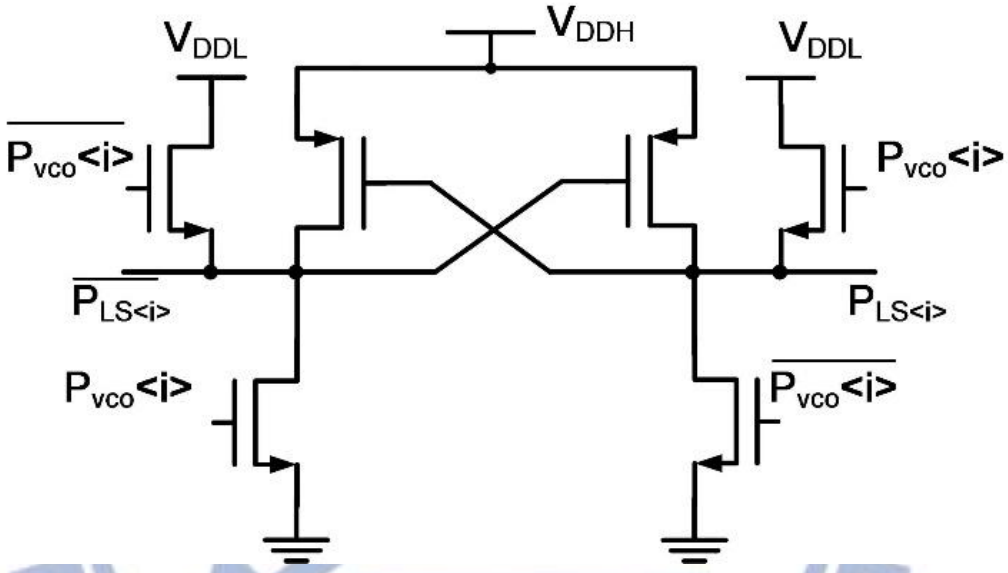
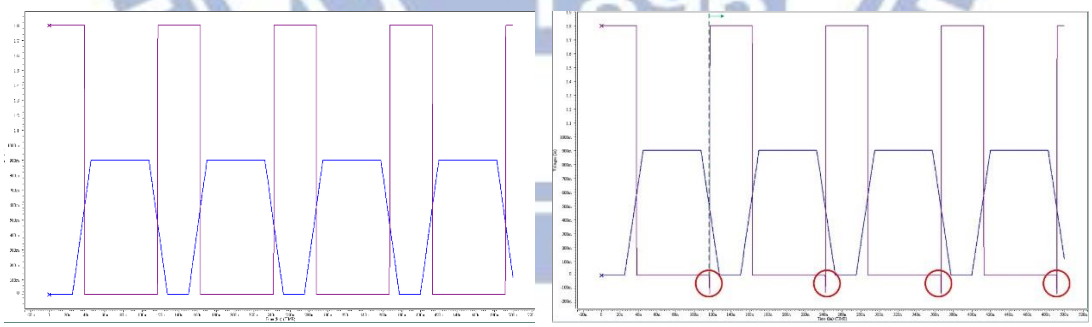


Figure 3.8 Schematic of a level shifter.



(a) (b)

Figure 3.9 Simulation result of level shifter (a) without (b) with two NMOS devices.

3.2.**Stability of Temperature Compensation Circuit**

Fig. 8 shows the simulation result after temperature calibration. Temperature coefficients (TC) are 83, 62.5, and 46.9 ppm/˚C of SS, TT and FF corners, respectively. TC at VDD = 1.6V is 119 ppm/˚C of TT corner. The compensated curve of negative TC is concave, and the compensated curve of positive TC is convex on the contrary.

The frequency resolution of F<6:0> is $\frac{\text{Tuning Range}}{2^N} = \frac{128\text{MHz}}{2^7} = 1MHz$. Where N is digital code counts. Besides, the frequency resolution of TP<4:0> is $\frac{\text{Tuning Range}}{2^N} = \frac{16\text{MHz}}{2^5} = 500\ kHz$. Tuning step of TP<4:0> is 32.5 ppm/°C. The frequency resolution of TN<4:0> and TP<4:0> are 500 kHz.

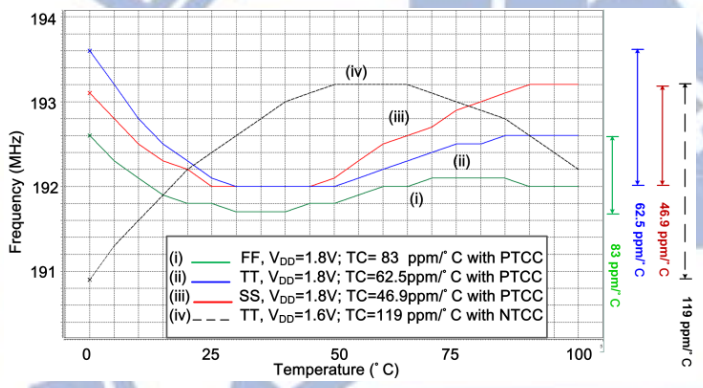


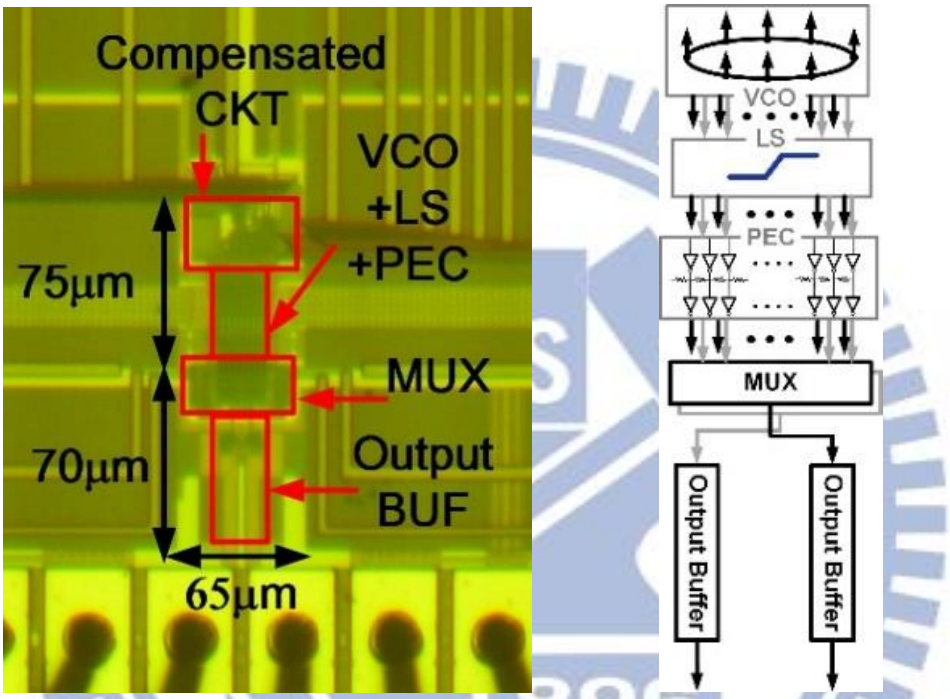
Figure 3.10 Simulation results of frequency versus temperature for the proposed CLCG after calibration.

3.3.**Experiment Results**

In this chapter, we deal with the testing flowchart, including the environment setup and PVT compensation step. Beginning with the measured environment setup and experiment results of the proposed PVT compensation circuit, we present the measured results of the calibration mode and measurement mode. We also analyze and summarize the measured duty cycle error and phase-to-phase error on the proposed circuit.

3.3.1. Concept

Compensation flow shows in Section 3.3.4 and related results show in Fig. 3.15. Temperature coefficient (TC) is 69.5 ppm/°C from 0 to 100°C, and 2-point calibration is applied to calibrate PVT variation. Phase to phase errors and duty cycle errors are less than 5.5% and 4.3%, respectively.



(a) (b)

Figure 3.11 (a) Die photograph of the proposed circuit, and (b) block of output stage.

The proposed clock generator has been fabricated in a 0.18 μm GP (general-purpose) CMOS process without specialized analog process options. Die photograph is shown in Fig. 3.11(a). The core dimension, which includes multiplexer (MUX) and output buffers, is 65 μm x 145 μm. The MUX and output buffers are used to measure the information of each phase output signal. Therefore, the CLCG core area is 65 μm x 75 μm.

In Fig. 3.11(b), the block of output stage for measuring phase to phase errors and duty cycle errors is illustrated. The output stage includes MUX and output buffers. The MUX is applied to select phases and phase to phase errors can be measured by selecting

two adjacent phases. The MUX is also capable to produce additional jitter each output phase. The output buffer includes tap buffers and resistances. The total power consumption is 1.1 mW at 1.8 V.

3.3.2. *Environment Setup*

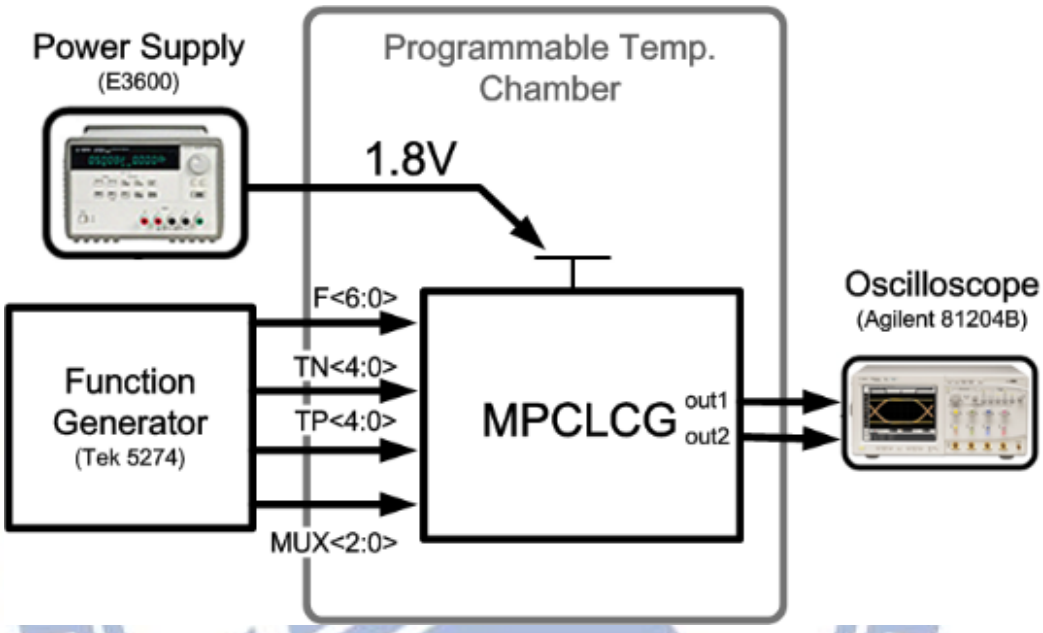


Figure 3.12 Measurement setup.

Fig. 3.12 shows the measurement environment. Temperature measurements were performed in a programmable thermal chamber. Frequency drift was measured with a real-time oscilloscope (Agilent 81204B).

3.3.3. *Jitter and Phase Noise Performance*

Fig. 3.13 represents the operating frequencies of CLCG at 20˚C and the jitter histogram at 1.8 V. The CLCG output demonstrates a 4.58-ps RMS jitter and a 34.55-ps peak-to-peak jitter (P2P jitter) at 192MHz within 12.67k hits. The RMS and P2P period jitters are less than 0.088% and 0.665%, respectively. Fig. 3.14 shows the output spectrum of the VCO with a supply voltage of 1.8 V, and the phase noise of output

signal. As shown in Fig. 14, the phase noise is -102.03 dBc/Hz @ 1 MHz offset and -124.24 dBc/Hz @ 10 MHz.

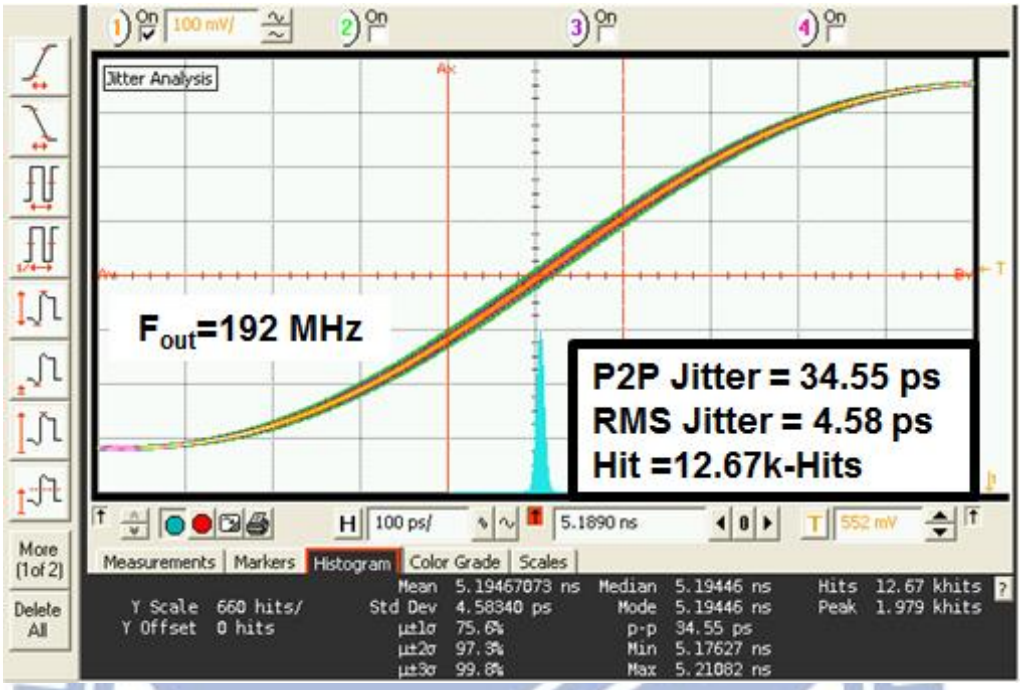


Figure 3.13 Jitter performance where RMS=4.58ps and P2P=34.55ps of 192 MHz output at 1.8V.

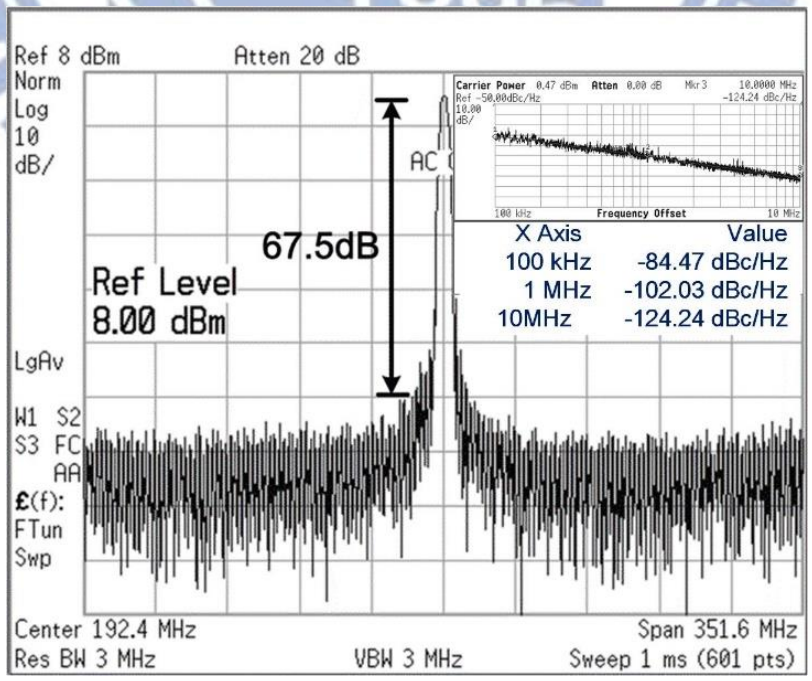


Figure 3.14 Measured output spectrum and phase noise of 192MHz output of the VCO with a supply voltage of 1.8 V.

3.3.4. Measurement of Temperature Compensation

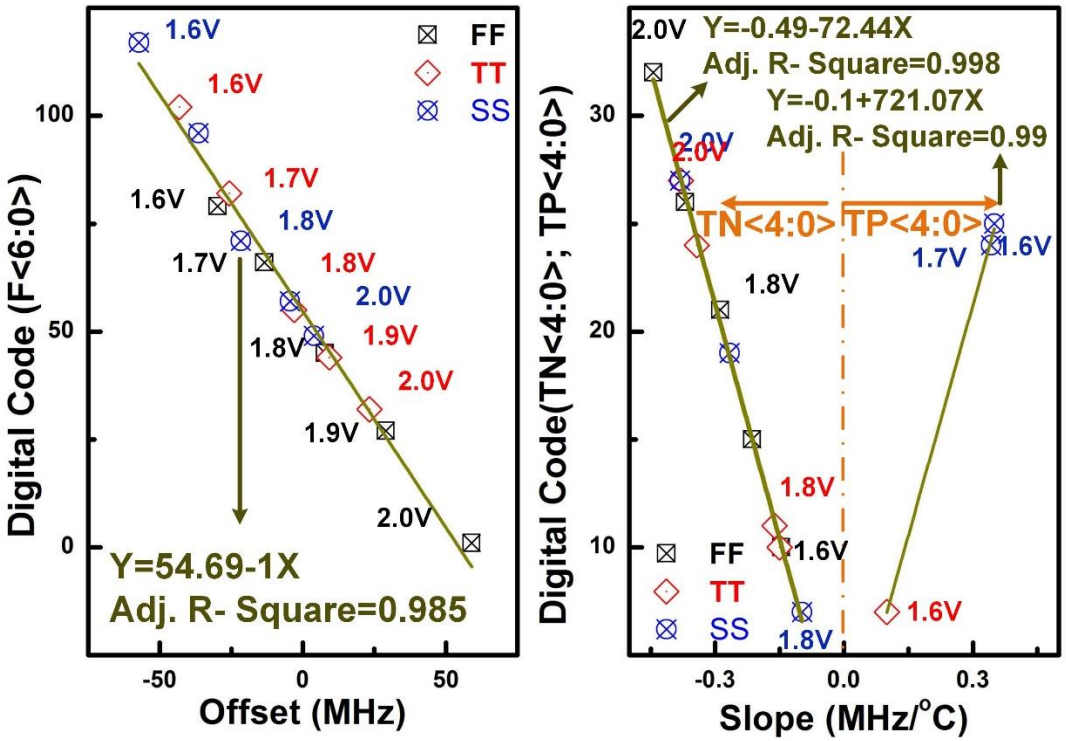
The PVT calibration setup can be considered theoretically as the following operations: First of all, we determine the offset and slope by temperature measurement. After setting all the digital code, F<6:0>, TP<4:0> and TN<4:0> to zero, we put the device under test (DUT) into a programmable temperature chamber and measure the frequency at 20°C and 80°C respectively. Therefore, the offset (ΔF) which denotes the difference between measured frequency and targeted frequency could be found. And the temperature offset, ΔT, is equal to 60°C, that is 80°C - 20°C. $slope = \frac{\Delta F80°C - \Delta F20°C}{\Delta T}$.

Secondly, we select the temperature calibration circuit by the trend of the temperature dependence. The measured frequency to temperature curve is used to spot the temperature calibration circuit. If the slope is negative, the negative calibration circuit is applied. Otherwise, the positive calibration circuit is adopted for a positive TC.

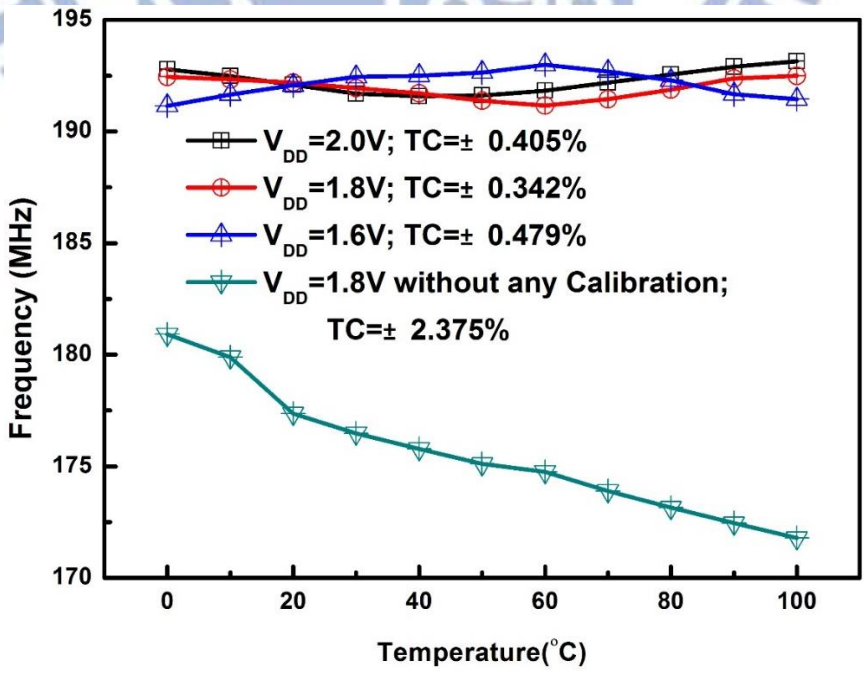
Finally, the calibrated circuits calibrate the frequency variation automatically. From Fig. 3.10, one optimal compensated point is obtained under one temperature and voltage setting. These simulated optimal compensated points are then plotted in Fig. 3.15. The vertical axis refers to digital code in both Fig 3.15(a) and (b) while the horizontal axis denotes an offset and a slope respectively in Fig 3.15(a) and Fig 3.15(b). We plotted fitting lines by linear regression analysis. Then we could get any desired digital code by substituting measured offset and slope into fitting lines in Fig 3.15(a) and (b). The calibration step process one time and one set code for mass industry realistic case. The method can dramatically reduce measured cost; however, the chip to chip could not be avoid actually.

Measured results after calibration are shown in Fig. 3.15(c). After calibration mechanism, PVT calibration which calibrates the initial frequency to 192 MHz at 20°C has been applied. The total temperature coefficient is measured in the external 1.8-V unregulated power supply under a temperature range from 0 to 100°C. TC without any calibration is ±2.375% or 475 ppm/°C and turns out to be ±0.342% or 69.5 ppm/°C

after calibration. Fig. 3.15(c) also shows the measured results under various supply voltage. The blue line, representing V_{DD}=1.6V, is the only one with positive temperature calibration and the unique concave curve, which conforms to theoretical simulation.



(a) (b)



(c)

Figure 3.15 (a) Relationship between digital code and (a)offset, (b)slope, and (c) Measurement result after temperature calibration with VDD variation.

3.3.5. *Duty cycle Error and Phase to Phase Error*

In Fig. 3.16, the duty cycle and phase to phase errors under the two test chips are shown. The maximum duty cycle error is 3.6%, which occurs at P<3>. The phase to phase duty cycle error (DCi–DCi-1) is a crucial point for pulse width modulation (PWM) applied in power converter [47]. The maximum phase to phase duty cycle error is 4.3% occurring at stage 3 which is between P<2> and P<3>.

Fig. 3.17 represents the output phase and phase error of two chips respectively. Output phase increases 45° per phase. The phase error is the error between ideal phase and measured error. The maximum phase error is 5.5% occurring at P<6>. The total phase error is between -4.3 to +5.5%. The phase error can be reduced efficiently by adjusting the VDD of output buffers.

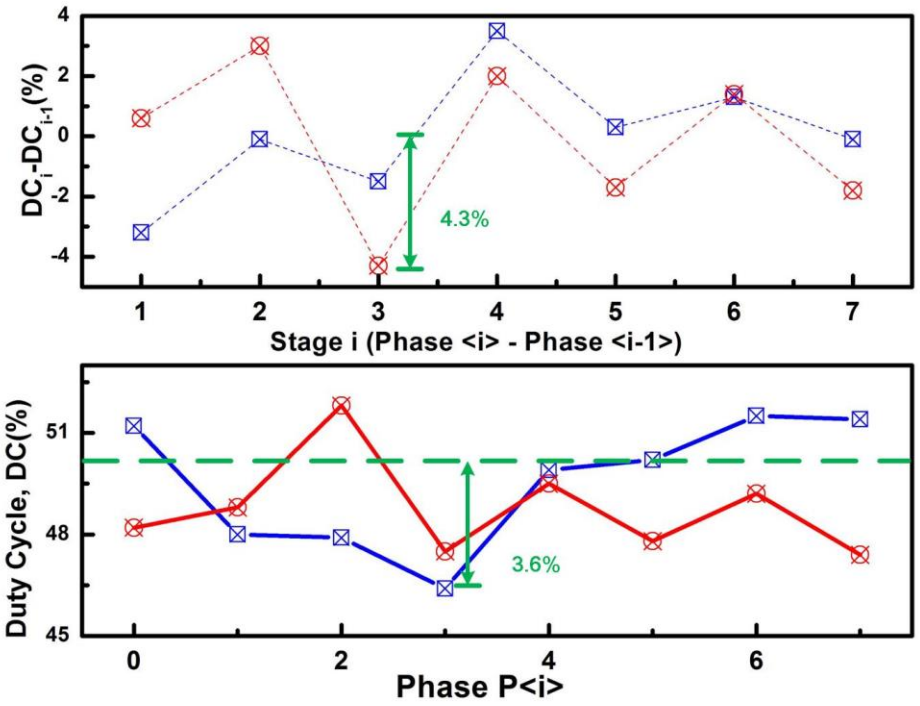


Figure 3.16 Measurement result of duty cycle error and phase to phase duty cycle error.

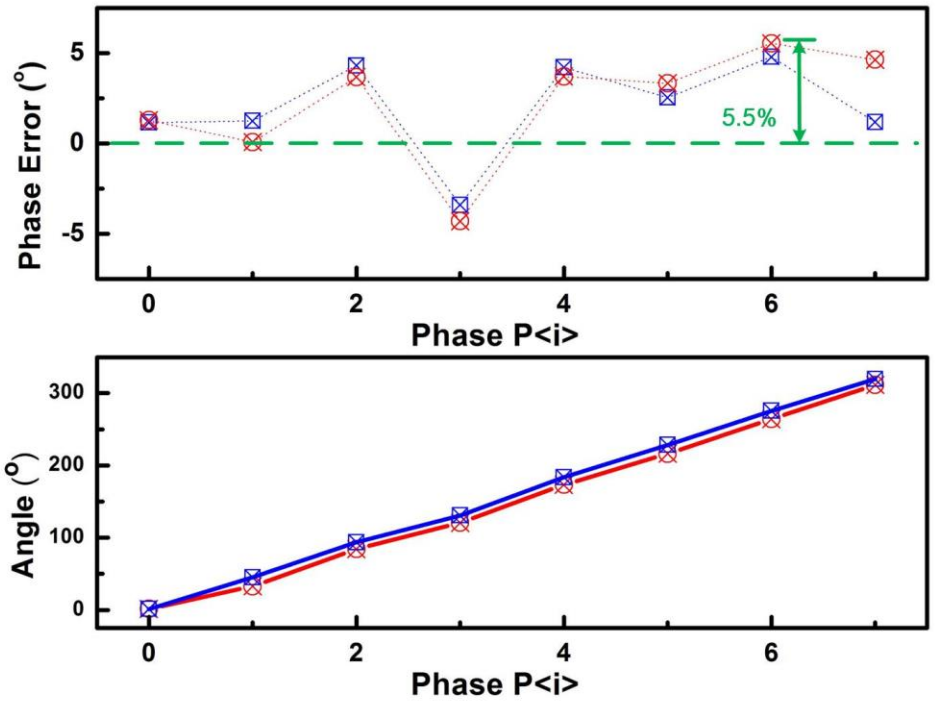


Figure 3.17 Measurement result of output phase and phase to phase error.

3.4.Comparison and FOM

Fig. 3.18 shows the figure of merits (FoM) versus temperature coefficients. The FOM is defined as a ratio of the power consumption to the oscillation frequency (nW/kHz) [10]. The calculated FOM is 5.73 nW/kHz for the proposed circuit, and is better than other works expect for [6], [7], and [10]. However, the area of the proposed circuit is smaller than others. Besides, the frequency of proposed circuit is much higher than other works.

Comparing with traditional PVT calibration mechanism such as blending TC of polysilicon resistor and diffusion resistor or bandgap reference circuit [10], [11], the proposed PVT calibration circuit has nearly equivalent TC as above works. The oscillators of relaxation or thermal diffusivity based have lower TC than others structures. However, above designs have large die dimensions or high power consumption. Therefore, these designs are widely applied at precisely micro-electromechanical systems.

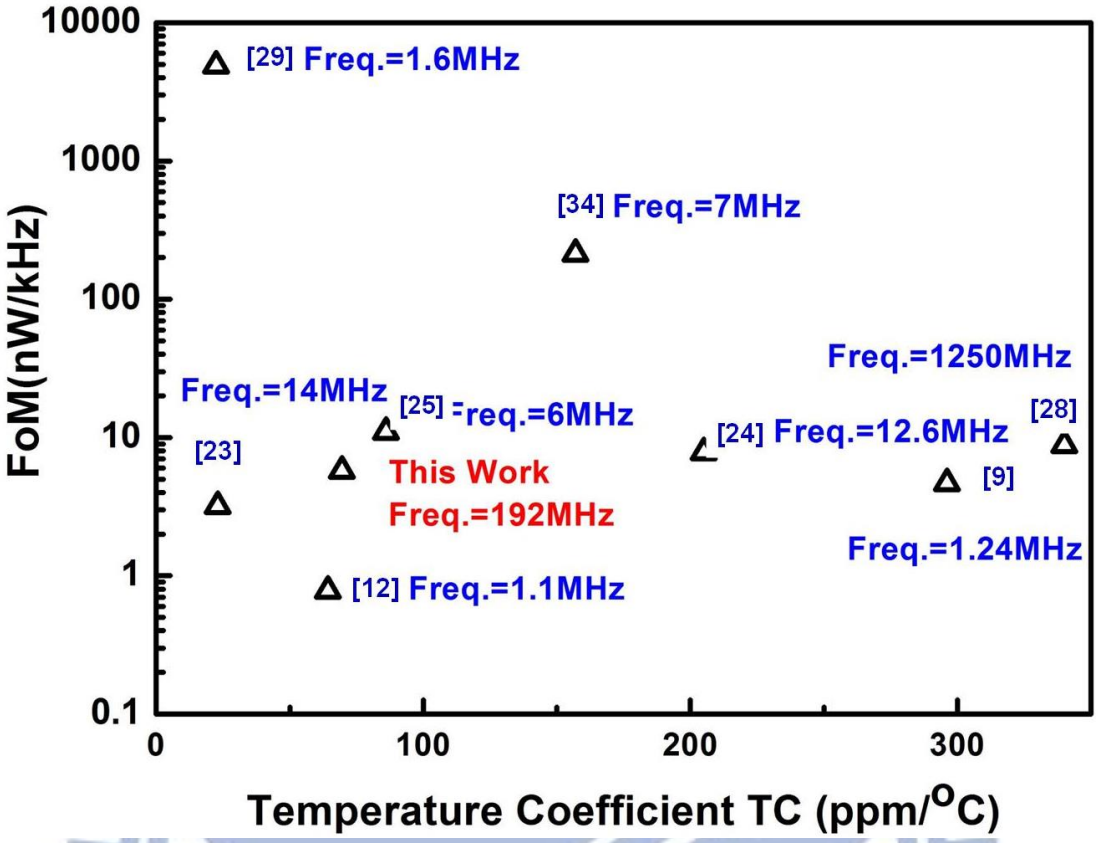


Figure 3.18 FOM versus Temperature coefficients.

Table 3.1 Performance Comparisons of Clock generators

	[9]	[23]	[24]	[25]	[12]	[34]	[28]	[29]	This work
Architecture	Rex.	Rex.	Rex.	RC.	Rex.	Ring	Ring.	Ther. Diff.	Ring
Technology(nm)	130	180	65	65	180	250	130	700	180
Multi-Phase	1	1	1	1	1	1	1	1	8
Supply voltage (V)	1.2	1.8	1.2	1.8	1.8	2.4	3.3	5	1.8
Frequency (MHz)	1.24	14	12.6	6	1.1	7.03	1250	1.6	192
Power (mW)	0.0058	0.045	0.0984	0.066	0.00086	1.5	11	7.8	1.1
TC(ppm/˚C)	296	23@ - 40~125 ˚C	205@ 0~80 ˚C	86@ 0~100 ˚C	64.3@ -20 ~80 ˚C	101@ -40 ~125 ˚C	340@ -40 ~125 ˚C	22.4@ -55 ~125 ˚C	69.5@ 0~100 ˚C
DC variation (%)	±1.8@ 1.01~0.99V	±0.16@ 1.7~1.9V	±0.07@ 1.1~1.5V	N.A	<3@ 1.2~2.4V	0.31@ 2.4~2.75 V	N.A.	N.A.	±3.6
Jitter (ps) (RMS) (P-P)	3448p (0.278%)	40p(PP) (0.056%)	N.A.	N.A.	N.A.	N.A.	N.A.	312ps (0.0195%)	4.58p (0.088%) 34.55p (0.665%)
PN (dBc/Hz) @1MHz	N.A	-115	-120	-97.6	-74.2	N.A.	-88	N.A.	-102
Area (mm^2)	0.016	0.04	0.01	0.03	0.075	1.6	0.014	6.75	0.0049
FOM (nW/kHz)	4.68	3.2	7.81	11	0.78	213.4	8.8	4875	5.73

Table I summarizes and compares the current temperature calibrated clock generators and the proposed circuit. Compared to other ring oscillator, our proposed 8 phases CLCG exhibits the lowest temperature sensitivity, smaller size and lower jitter performance. Besides, the performance of the duty cycle error and phase error are quiet excellent performance as well.

3.5.**Conclusion**

The proposed 8 phases crystal-less clock generator circuit was fabricated in a 0.18 μm CMOS technology. It consumes 1.1 mW with a power supply of 1.8 V, and occupies core dimension of 65μm ×75μm excluding output buffer and MUX. The measured period jitters are 4.58-ps RMS jitter and a 34.55-ps P2P jitter at 192 MHz within 12.67k hits. At 192 MHz, the phase noise of CLCG is −102 dBc/Hz at 1-MHz-offset.

Operational frequencies vary ±0.34% at V_{DD}=1.8 V and ±0.479% with 10% supply voltage variation between 0° an output buffer and MUX. The measured period jitters are a 4.58-ps RMS jitter and a 34.55-ps P2P jitter at 192 MHz within 12.67k hits. At 192 MHz, the phase noise of CLCG is −102 dBc/Hz at 1-MHz-offset. Operational frequencies vary ±0.34% at V_{DD}=1.8 V and ±0.479% with 10% supply voltage variation between 0° and 100°C. The maximum duty cycle error is 4.3%, and the phase to phase errors are less than ±5.5°. This work not only realizes a CLCG operating with 8 phases outputs, but also fulfills sufficiently high frequency stability and accuracy under the process and temperature variations.

Chapter 4. The Ultra-Low Voltage CMOS Voltage Controlled Oscillator with Voltage, Process and Temperature Compensation

This chapter is briefly depicted a 2.4 GHz voltage CMOS controlled voltage oscillator with voltage, process, and temperature compensation under ultra-low supply voltage. In this chapter, process and temperature variations on the clock generators have been studied. A new all-digital auto compensated mechanism to reduce process and temperature variation without any laser trimming is proposed. With the compensated circuit, the VCO frequency-drift is 16.6 times the improvements of the uncompensated one as temperature changes. Furthermore, it also provides low jitter performance.

The industrial, scientific, and medical (ISM) band of 2.4 GHz is reserved internationally for the use of RF energy for industrial, scientific and medical purposes [48], [49]. Wireless body-area networks (WBAN) which are rapidly growing applications, and are used for communication among sensor nodes operating in, on or, around the human body [50], [51]. The human body communication (HBC) is a wireless communication method used to connect devices through the human body as a transmission media. HBC has high speed and low power characteristics and is suitable for contact-based services [52], [53]. Hence, the clock generator operating at 2.4GHz is the critical and essential component for healthcare purpose.

The auto-calibrated process and temperature compensated circuit includes a process detector to detect process variation and all digital compensation circuit. Besides, a temperature voltage controlled compensated circuit is applied to calibrate the variation from temperature. The proposed circuit was fabricated in a 65 nm CMOS technology. It makes the operation of CLCG with very low supply voltages, down to 0.5 V, as well as achieves sufficient high frequency stability and accuracy against the variations from process and temperature.

4.1.Concept of VCO with PVT Compensation

Figure 4.1 shows the structure of the proposed ultra-low-voltage (ULV) CLCG. It includes the LC oscillator, auto-calibrated process and temperature circuit, and digital controlled varactors and temperature compensation circuit.

The LC oscillator provides a stable output frequency. The auto-calibrated process, voltage and temperature circuit includes two major part. One includes a process sensor and a process selector, which can detect fabricated process and decide the compensated code DF<5:0> and DT<5:0>. DF<5:0> directly modulate the digital controlled varators. The other is the compensated CKT that provide correspond voltage depending on DT<5:0> for digital controlled varactors. The output signals Fout are amplified by tap buffers and passed the open drain circuit and bias tee circuit.

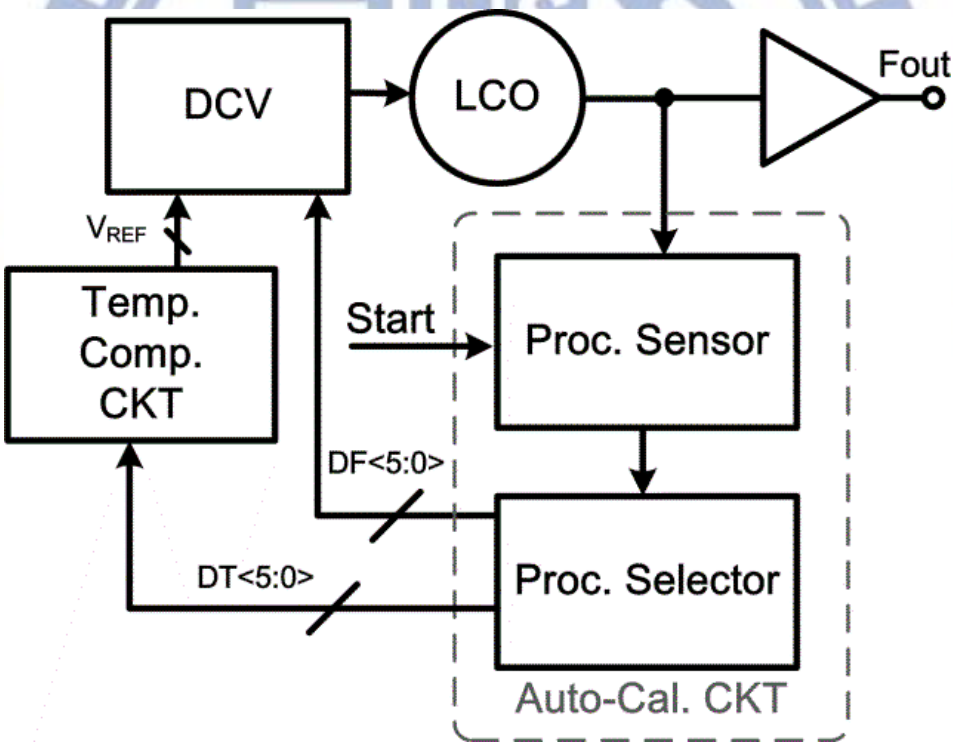
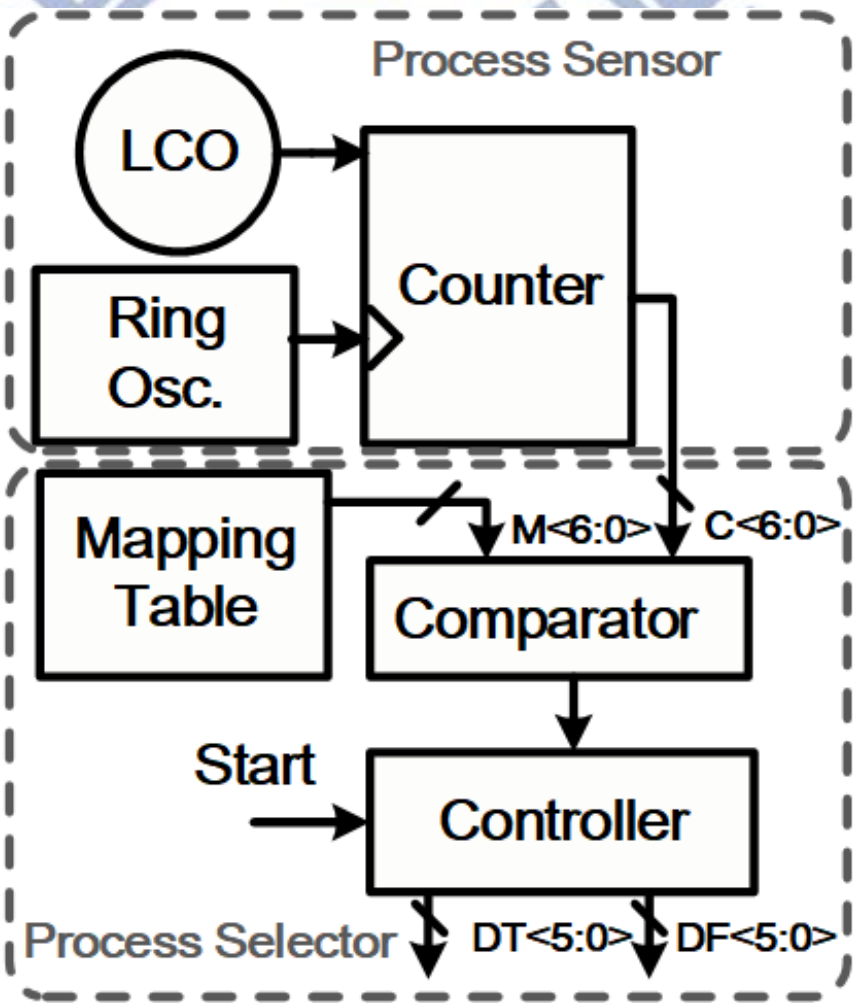


Figure 4.1 Block diagram of the proposed CLCG.

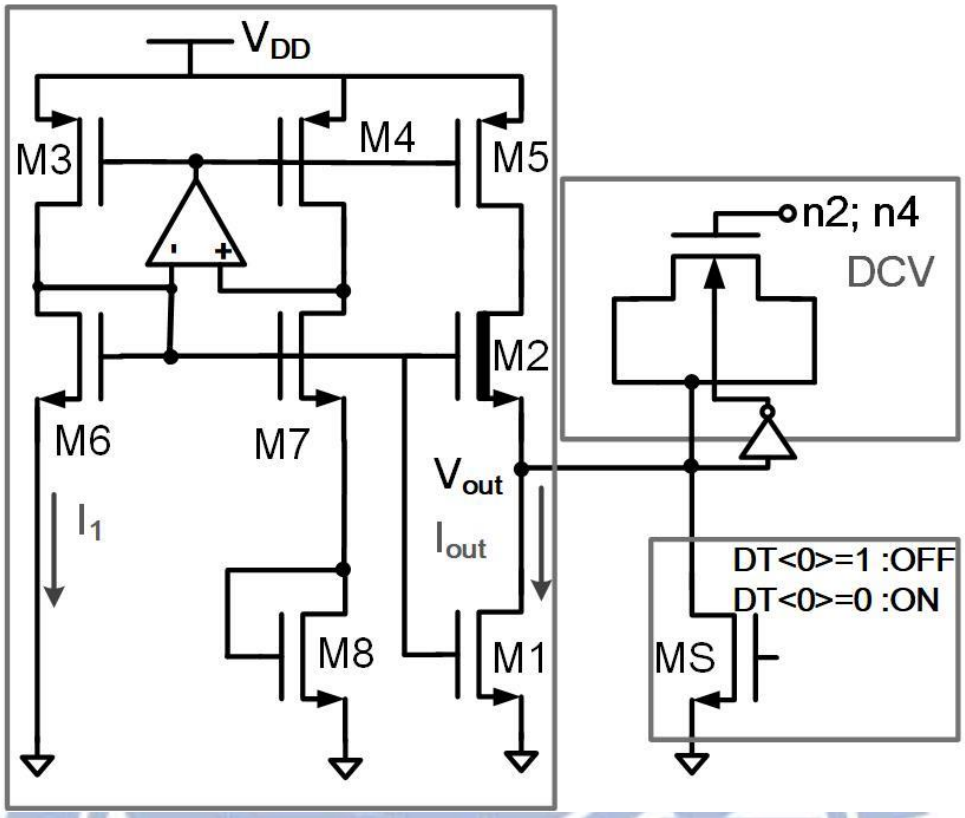
4.2.Architecture and Circuit Implementation

4.2.1. Auto-Calibrated Process and Temperature Circuit and Its Operating Principle

Figure 3 shows the block diagram of an auto-calibrated process and temperature compensated circuit. It consists of a process detector and a digital process and temperature compensated circuit. The ring oscillator, a LC VCO, and a counter consist of the process sensor.



(a)



(b)

Figure 4.2 The block diagram of auto-calibrated compensated circuit.

The signals of a LC VCO and a ring oscillator are taken as the input and clock of counter, respectively. The output digital codes of the counter (C<6:0>) are dependent on the process variation. The mapping table is based on the process and temperature variations in the mapping table detection (MTD) [26]. Three process corners which are slow-slow (SS), typical-typical (TT), and fast-fast (FF) with 5% VDD variation are considered. The output digital signal of mapping table (M<6:0>) is the calibration parameter that depends on the process variation and used to adjust the target frequency DCO.

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parameter that depends on the process variation and used to adjust the target frequency DCO.

Figure 4.3(a) shows the simulated frequency versus temperature for the proposed LC VCO without any calibration. Temperature coefficient (TC) are 705, 550, and 534 ppm/°C of the slow-slow (SS), typical-typical (TT), and fast-fast (FF) corners, respectively. The LC VCO frequency differences of corners are too slight (about 50MHz) to be distinguished. Then, a low speed ring oscillator operated at 60MHz with TT corner is introduced to sense the process variation.

Figure 4.3(b) shows the simulated frequency versus temperature for the ring oscillator with different corners. TC of ring oscillators are 25500, 16000, and 10200 ppm/°C of the SS, TT, and FF corners, respectively. The highly process, voltage, and temperature (PVT) dependent characteristic of a ring oscillator can be used to detect the PVT variations efficiently.

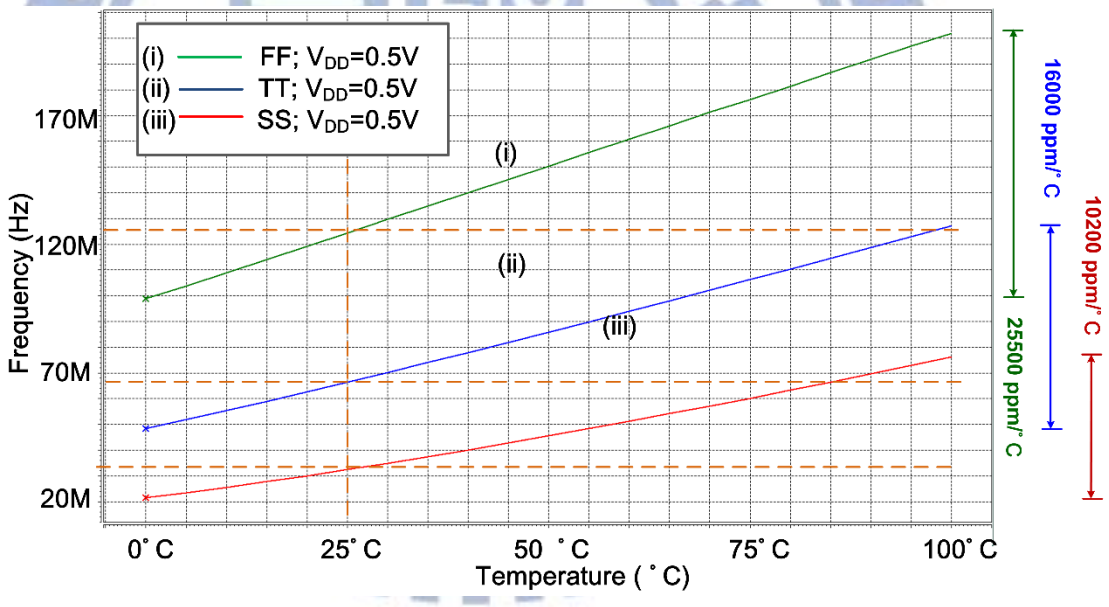


Figure 4.3(a). Simulated result of frequency versus temperature for the LC VCO without any calibration.

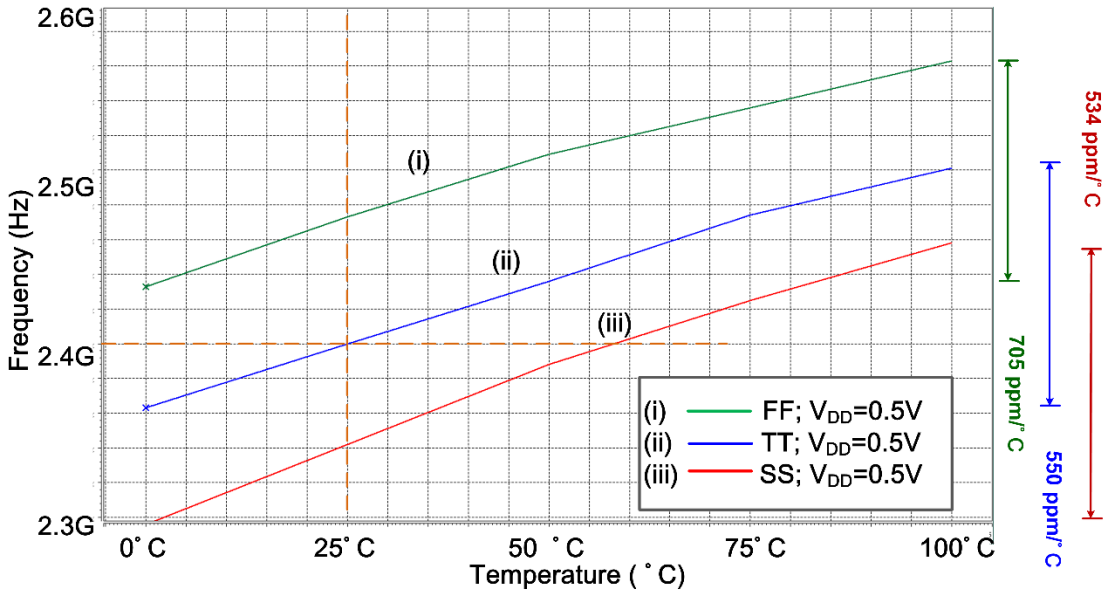


Figure 4.3(b) Simulated result of frequency versus temperature for the ring oscillator without any calibration.

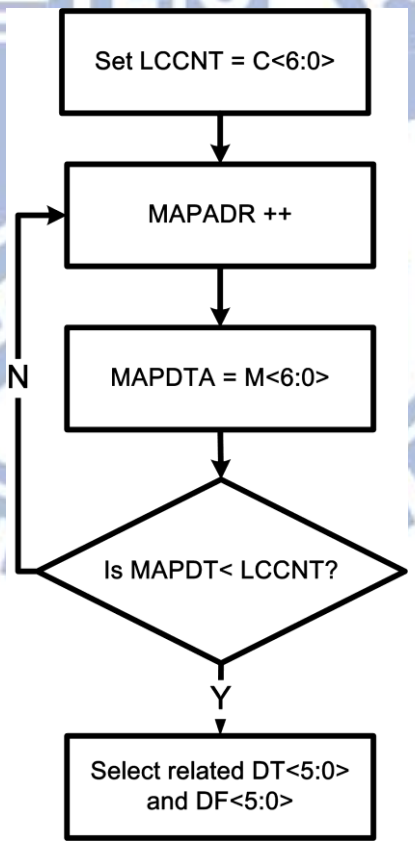


Figure 4.4 (a). Flow charts of mapping table selection for the proposed mechanism of auto calibrated process and temperature circuit

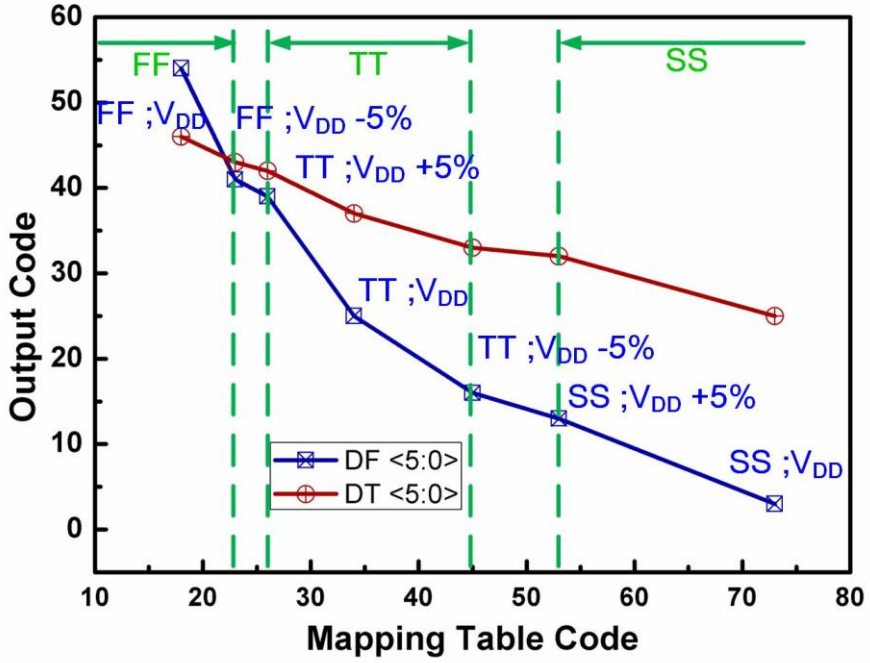


Figure 4.4 (b). Relationship between mapping table code and output code.

Figure 4.4(a) shows the flow charts of mapping table selection. The mapping table selected mechanism can be theoretically considered as the sequence of four operations:

1. Initialization: The calibration must be operated at initial temperature (30°C) to avoid temperature variations. As Start goes high, outputs of the registers must be set or reset. The counter outputs C<6:0> are decided by the frequency of the ring oscillator and LC oscillator, and then the counter output C<6:0> saves to the register LCCNT.

2. Mapping table selection: When the initialization is completed, the mapping table value M<6:0> according to its mapping address MAPADR saves to the register MAPDATA. If MAPDATA > LCCNT, the corresponding M<6:0> can be found. Otherwise, it increases the MAPADR value and compares the MAPDATA and LCCNT again until finds out the applicable M<6:0>.

3. After completing mapping table detection, the controller gets the matching M<6:0>. The mapping table value M<6:0> and its corresponding process code DF<5:0>and temperature code DT<5:0> are shown in Fig. 5(b) Thus, the corresponding DF<5:0> and DT <5:0> of this chip can be defined. Then, the controller uses the mapping value to achieve the target frequency by switching varactors for temperature and process compensation.

4. One-point calibration: At the fine tuning stage, single point calibration is applied to modify the output frequency at room temperature. The mechanism maintains that the function of the calibration system can work under the operational frequency of the CLCG. The calibration only process one time as one-point calibration and could not sense environment variations with time. The dynamic power variation or sudden variation could not be detected by this mechanism. All compensations are based on mapping table after calibration

The frequency resolution of DF<5:0> is$\frac{\text{Tuning Range}}{\text{N}} = \frac{192\text{MHz}}{64} = 3\text{MHz}$. The frequency tuning step is 12.5 ppm/°C where is sufficient for this condition. The frequency resolution of DT<5:0> is also 3MHz. The resolution depends on the frequency of a LC VCO and a ring oscillator. The resolution increases with high speed of a LC VCO and low speed of a ring oscillator. The mapping table selection is cover by SS, TT, FF corners. However, if the ring oscillator speed is higher than above situations and the LC-VCO speed is kept at relative low speed, such as slow-fast (SF) corner. The counter output code might be out of range. Therefore, the design should be increased the compensated range to overcome this situation.

4.2.2. Process LC Oscillator

The LC voltage-controlled oscillator (LC VCO) is shown in Fig. 2. By utilizing the capacitive feedback and the forward-body- bias (FBB) technique [54], the LC VCO can be operated with reduced supply voltage and power consumption while maintaining remarkable circuit performance in terms of phase noise, tuning range, and output swing. As $C_{11}=C_{12}=C_1$, $C_{21}=C_{22}=C_2$, $L_{11}=L_{12}=L_1$and $L_{21}=L_{22}=L_2$, the oscillation frequency and transconductance can be approximated by

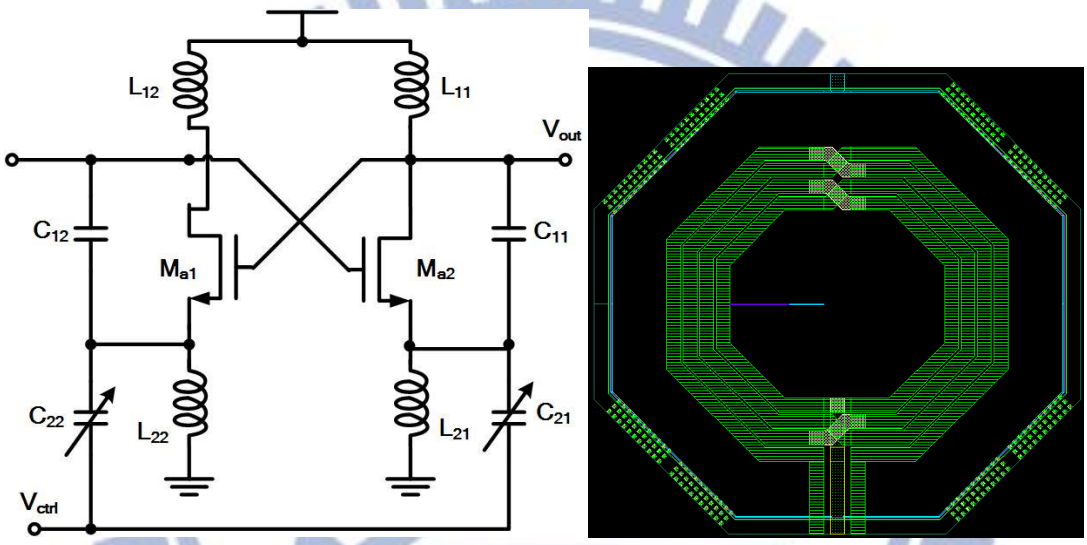
$$\omega_0 \approx \sqrt{\frac{1}{L_2C_2} + \frac{C_1+C_2}{L_1C_1C_2}} \quad (1)$$

As $L_1=L_2=L_P$, the equation (1) can be simplified as

$$\omega_0 \approx \sqrt{\frac{1}{L_p}\left(\frac{1}{C_1} + \frac{2}{C_2}\right)} \quad (2)$$

From (2), it is clear that the variation of C_2 has more influence on ω than C_1. Therefore, the capacitor C_2 is applied as tuning varactors to a reasonable tuning range of the LC VCO under ultra-low-voltage operations. Besides, increasing the capacitance of C_1 can get wider tuning range. Then, C_1 are implanted with metal-insulator-metal (MIM) capacitors, which have high capacitance and better stability.

The process in this proposed paper is TSMC 65nm GP (general purpose) 1p9m RF CMOS process. Metal3 to Metal 9 are Cu metal layers. The metal layer of inductors is "metal 9" and its layout view is shown as following.



(a) (b)

Figure 4.5 Schematic of the voltage-controlled LC oscillator.

4.2.3. Digital Controlled Varactors

Figure 6(a) illustrates the circuit of the DCV (Digital controlled varactors). Fig. 6(b) shows the capacitor value of DCV versus its controlled voltage with different devices. DCV should produce a smaller capacitor value to maintain a higher operating frequency of DCO. The complementary signal of F<0> is applied to NMOS source/drain of DCV to produce two quantized levels of capacitor values. Besides, the source/drain- to-bulk junctions are forward biased at 0.5 V. Accordingly, DCV has two different timing resolutions and provides the same output loading for DCO. In Fig. 6(b), (i) and (iv) produced by Low Vth (LVT) MOSFET has wider tuning range of the

capacitor than (ii) and (iv) produced by Low Vth (LVT) MOSFET. Therefore, DCV can be realized for a wide tuning range and high-speed frequency by selecting LVT MOSFETs in the proposed circuit.

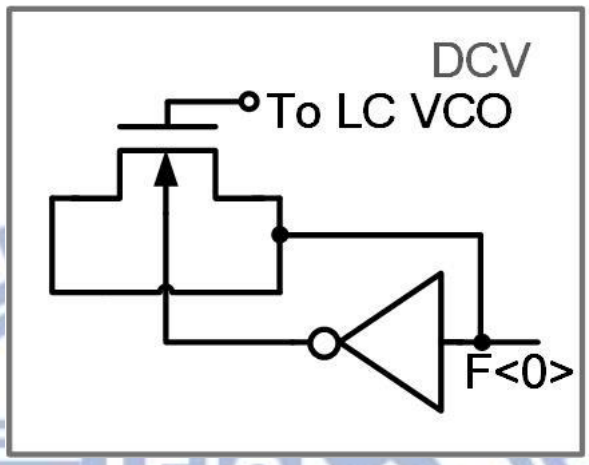


Fig. 4.6(a). Schematic of digital controlled varactors for frequency calibration

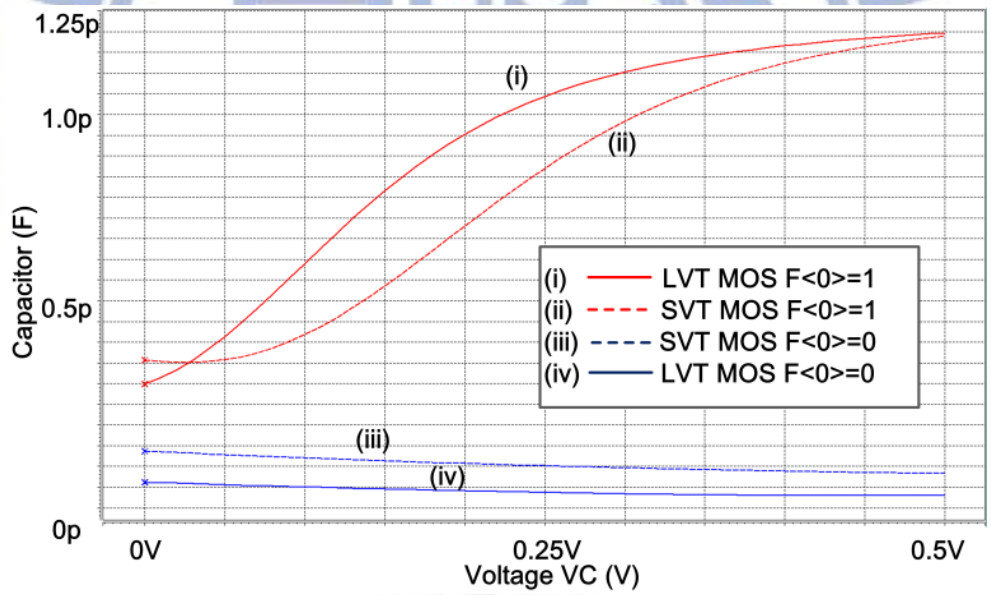


Fig. 6(b). Capacitor value of DCV versus its controlled voltage.

The parasitic diode could cause phase noise degradation compare to MIM capacitor in ref [12]. However, the MOS capacitor has wide range and high speed characteristic. The forward biasing current of the D-B and S-B diodes are around 300 fA. The simulated device W/L is 10μm/10μm.The following figure shows the forward biasing current of the D-B and S-B diodes.

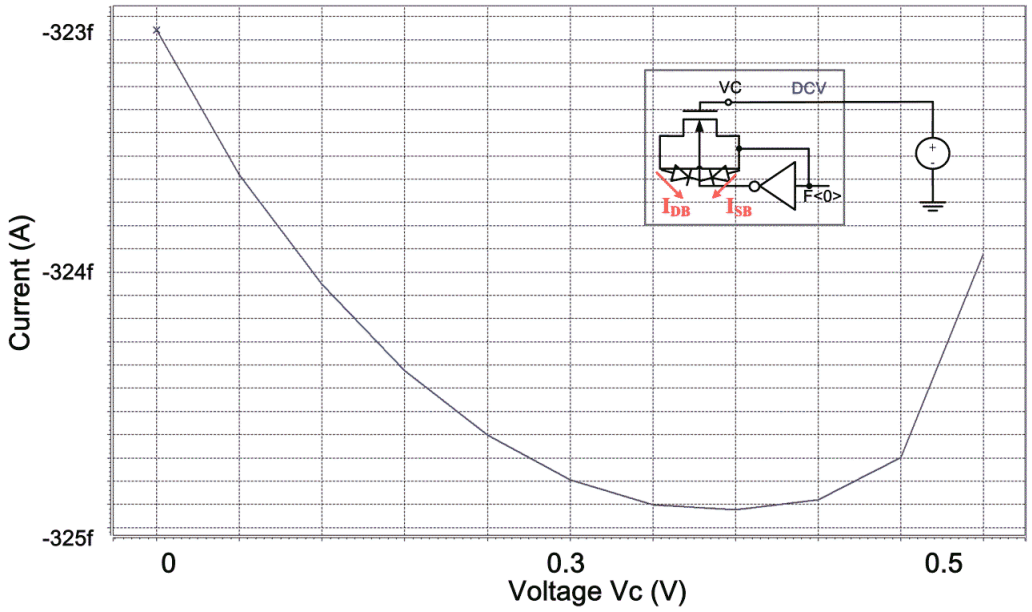


Figure 4.6(c) The forward biasing current of the D-B and S-B diodes versus tuning voltage.

4.2.4. *Temperature Compensated Voltage Reference Consisting Subthreshold MOSFETs*

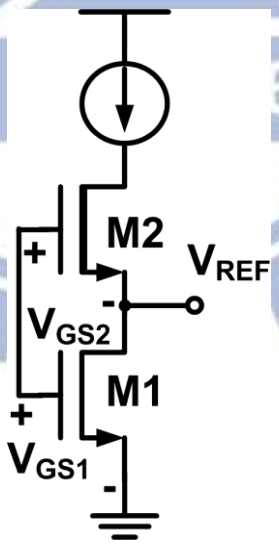


Figure 4.7. Scheme of principle of a proposed voltage reference.

The voltage reference in this work can be simply expressed as a current source and two diode connected transistors, which act as active load shown in Fig. 4.7. Low voltage reference mostly adopt two structure for compensation positive TC, BJT and

subthreshold region MOS [55], [56]. Similar structures had been used in prior art [57]. One current source and one diode connected transistor operated in saturated region or subthreshold region. The NMOS provides a temperature compensation reference voltage (V_{REF}). The reference voltage V_{REF} in this work can be modified as following.

$$V_{REF} = V_{GS1} - V_{GS2} \tag{1}$$

Where transistor M1 is operated in subthreshold region, and M2 is the native NMOS. Native NMOS is not implanted in P-well but directly in P-substrate. The characteristic of native NMOS is intermediate between enhancement and depletion modes and the threshold voltage is nearly zero [58].

The function of the subthreshold drain current of a MOSFET is an exponential function of the gate-source voltage and the drain-source voltage, and I-V characteristics of nMOS operated in subthreshold region is given by

$$I_D = \mu S V_T^2 \exp(\frac{V_{GS} - V_{th}}{\eta V_T})[1 - \exp(-\frac{V_{DS}}{V_T})] \tag{2}$$

Where μ is the electron mobility, S = COX(W/L)(η-1) (COX is the gate oxide capacitance per unit area, (W/L) is the transistor aspect ratio, and η is the subthreshold slope factor). V_T = kBT/q is the thermal voltage (kB is the Boltzmann constant, q is the elementary charge and T is the absolute temperature), V_{th} is the MOSFET threshold voltage, V_{GS} and V_{DS} are the gate-to-source and the drain-to-source voltages, respectively. As $V_{DS} \geqq 4V_T \approx 0.1V$, the current I_D is almost independent of V_{DS}, and V_{GS} can be approximated by

$$V_{GS} = V_{th} + \eta V_T \ln(\frac{I_D}{\mu S V_T^2}) \tag{3}$$

Where V_T is proportioned to absolute temperature (PTAT) and V_{th} decreases with absolute temperature linearly is shown as [13]

$$V_{th}(T) = V_{th}(T_0) + \alpha(T - T_0) \tag{4}$$

Where T_0 is the reference temperature, where is 300˚K and α is a negative value.

The current operated in saturation region is shown as following

$$I_D = \frac{1}{2} S_2 \mu_2 (V_{GS2} - V_{th2})^2 \tag{5}$$

Where V_{th2} is threshold voltage of native NMOS transistor, and its value is approach to zero. Therefore, the output voltage can be rewritten as

$$V_{REF} = V_{GS1} - V_{GS2} = V_{th1} + \eta V_T \ln(\frac{I_D}{\mu_1 S_1 V_T^2}) - V_{th2} - \sqrt{\frac{2I_D}{S_2 \mu_2}} \tag{6}$$

The temperature coefficient of output voltage can be formulated as

$$\frac{dV_{REF}}{dT} = (\alpha_1 - \alpha_2) + \frac{k}{q}\eta \ln(\frac{I_D(T)}{\mu_1 S_1 V_T^2}) + \frac{kT}{q}\eta \frac{\partial}{\partial T}\ln(\frac{I_D(T)}{\mu_1 S_1 V_T^2}) - \frac{1}{2}(\frac{2I_D}{S_2\mu_2})^{-\frac{1}{2}} \frac{\partial}{\partial T}(\frac{2I_D(T)}{S_2\mu_2}) \tag{7}$$

A zero TC can be achieved to have the temperature compensation of output voltage. The following equation has to be satisfied

$$\frac{dV_{REF}}{dT} = 0 \tag{8}$$

Therefore, finding out the dependence between bias current and temperature is essential to clarify the temperature compensated mechanism.

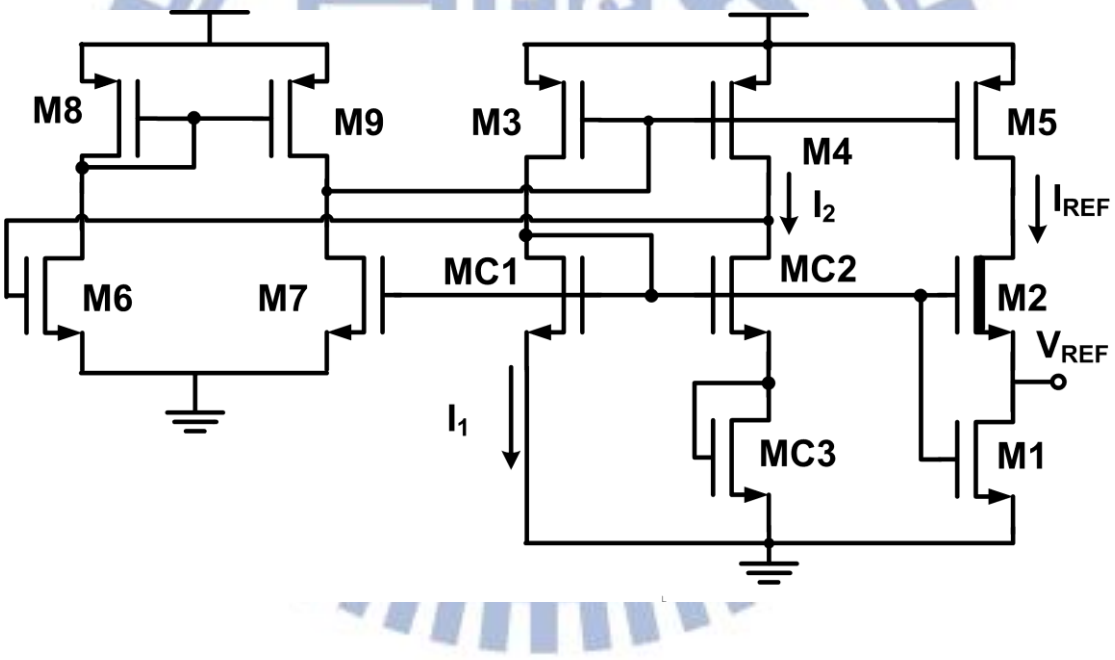


Figure 4.8 Scheme of proposed temperature compensated voltage reference

The architecture of the proposed voltage reference is illustrated in Fig. 4.8. The self-biased current source has no resistors and all MOSFETs work in the subthreshold region. It generates the current to be injected in the active load transistors due to the low power characteristics, such as high mobility and uniform amorphous structure. It is to provide a stable current, which compensates temperature effects on V_{REF}, and voltage variations can be reduced the supply by OP Amp and bypass capacitors. The

current I_D in (8) can be obtained by taking into account a linear combination of NMOS voltages in the sub-threshold region. Among the possible solutions for the current reference we chose a self-biased configuration where only three subthreshold operated NMOSs perform such combination. By using the virtual short characteristic of OP Amp, the DC equation of current source can be explained as

$$V_{GSc1} = V_{GSc2} + V_{GSc3} \tag{9}$$

Substitute VGS with (3), (9) can be rewritten as follows

$$V_{thc1} + \eta V_T \ln(\frac{I_{D1}}{\mu_{c1} S_{c1} V_T^2}) = V_{thc2} + \eta V_T \ln(\frac{I_{D2}}{\mu_{c2} S_{c2} V_T^2}) + V_{th} + \eta V_T \ln(\frac{I_{D2}}{\mu_{c3} S_{c3} V_T^2}) \tag{10}$$

Let $V_{th}=V_{thc2}+V_{thc3}-V_{thc1}$ and assume the electron mobilities μ are almost the same ($\mu_{c1}=\mu_{c2}=\mu_{c3}$). The current ratio can be decided by PMOS aspect ratio ($I_2/I_1 = (W_4/L_4)/(W_3/L_3)=A$). We can express the current I_1 as

$$I_1 = A\mu V_T^2 \exp(-\frac{\Delta V_{th}}{BV_T}) \tag{11}$$

Where $A=(S_2S_3/a_2S_1)$, and $B=(\eta 2+\eta 3-\eta 1)$. The generated current I_1 is mirrored to the active load by the current mirror consisted of M3, M4, and M5. Assume the ratio of mirror

($I_{REF}/I_1=(W5/L5)/(W3/L3)$)is β, therefore, (6) can be rewritten as

$$V_{REF} = V_{GS1} - V_{GS2} = V_{th1} - V_{th2} + \eta V_T \ln(\frac{A\beta}{\mu S_1 V_T^2}) - \frac{\Delta V_{th}}{BV_T} - \sqrt{\frac{2AV_T^2}{S_2} \exp(-\frac{\Delta V_{th}}{BV_T})} \tag{12}$$

The Taylor series of nature logarithm (ln) can be express as

$$\ln x = \sum_{n=1}^{\infty} \frac{(-1)^{n+1}}{n} (x-1)^n = (x-1) - \frac{1}{2}(x-1)^2 + \frac{1}{3}(x-1)^3 ..... \tag{13}$$

As the order of current is less than 10^{-8} (about 10nA), the square root term of (12) is about 10^{-4}. It affects the Taylor series is lower than 10th terms; therefore, the square root term in (12) can be neglected under Nano-Amp scale. Reference voltage can be approach as

$$V_{REF} = V_{GS1} - V_{GS2} = V_{th1} - V_{th2} - \frac{\Delta V_{th}}{BV_T} + \eta V_T \ln(\frac{A\beta}{\mu S_1 V_T^2}) \tag{14}$$

We can find that the temperature dependence of voltage reference is Vth and VT. The temperature compensation can be design by setting δVREF/δT=0, and find out the fitting ratio of (W1/L1) and (W2/L2). The gate of M1 and M2 are also connected to the gate of MC1 and MC2, its purpose is to keep M1 and M2 always on by the diode-connected transistor MC3.

A differential operational amplifier with active-loaded MOS pair is designed to be used in the reference core. It employs a differential input pair, consisting of transistors M1 and M2 used low threshold voltage devices and operated in weak inversion, so sufficient headroom remains available for ultra-low supply voltage. The amplifier is self-biased from the supply and consumes 110nA of current, providing a DC gain of 20dB. It provides higher PSRR and its characteristic of virtual short for circuit design.

4.3. Experiment Results

4.3.1. Concept

In this chapter, we deal with the testing environment, including the instruments and component circuits on the test broad. Beginning with the measured environment setup and experiment results of the proposed CLCG, we present the characteristics and performance of the measured results. We also analyze and summarize the supply noise effects on the proposed CLCG.

4.3.2. Environment Setup

The proposed frequency generator has been fabricated in a 65nm GP (general-purpose) CMOS process without specialized analogy process options. Figure 4.9 shows the measurement setup with bias tee for output signal. F_{ct}<5:0> is a 6-bit manual frequency controlled code for one-point calibration. Temperature measurements were performed in a programmable thermal chamber.

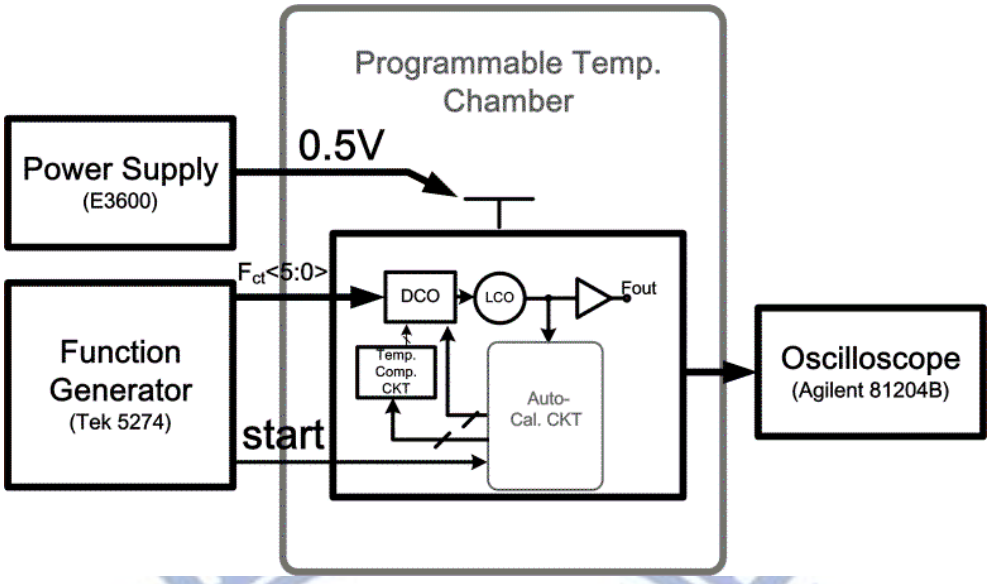


Figure 4.9 Measurement setup.

The output buffer includes tap buffers and an open drain circuit. The output stage of CLCGs usually dominate the output power. The schematic of output stage and equivalent impedance of measured environment is shown in Fig. 4.10. The buffers provide stable output signals, and the combination of the open drain device and the bias tee device has a characteristic of low loss. The buffers are designed for ensuring stable output signals in every simulation under different situations, and the stable measured output power reflect an achievement of the design purpose of the buffers and open drain circuit.

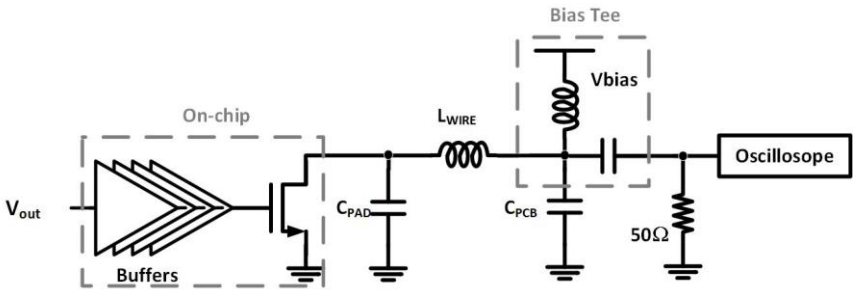
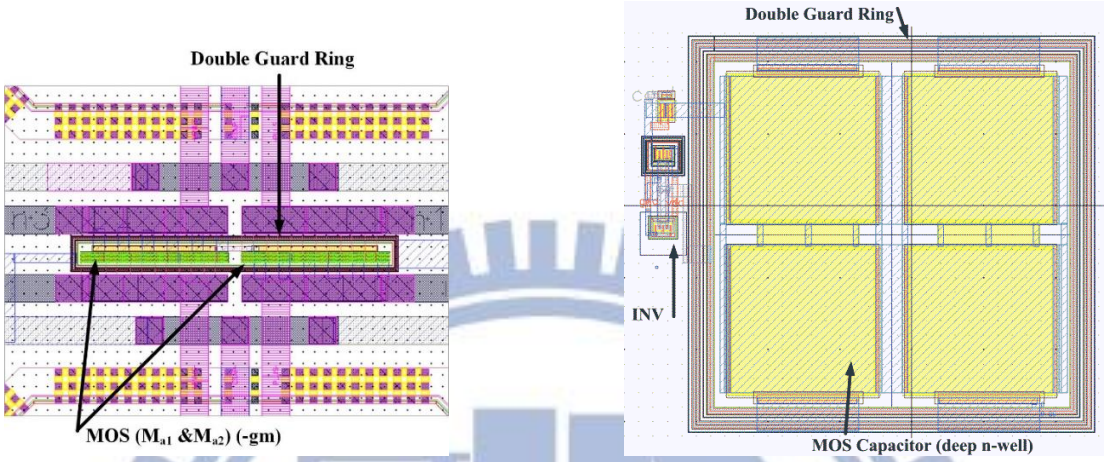


Figure 4.10 The output stage and equivalent impedance of measurement environment

The MOSFETs of high frequency devices such as varactors and the –gm part (M_{a1} and M_{a2} in Fig. 2) of LCO are applied deep n-well devices. Deep n-well structure is

used to block substrate noise. The devices are also applied double guard rings to isolate each body. Therefore, the LVT devices have isolated body but not sharing the same substrate with other NMOS devices by deep n-well and guard ring structure. The layout view of one varactor and the –gm part are shown in Fig. 4.11.



(a) (b)

Figure 4.11 Layout view of (a) MOS Capacitor and (b) –gm.

4.3.3. Measurement of VCO performance

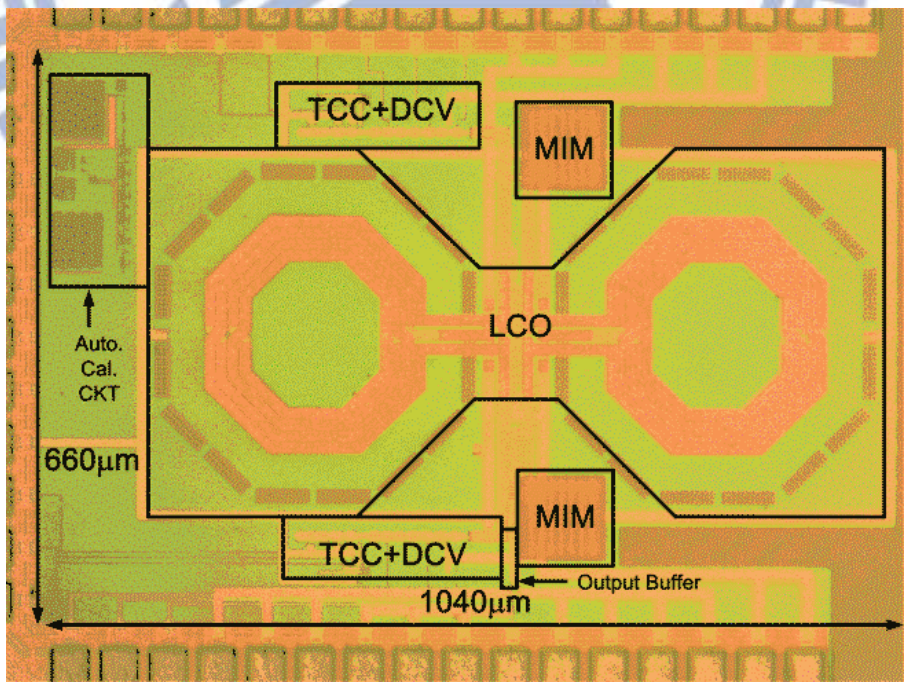


Figure 4.12 Die photograph of the proposed circuit fabricated in a 65-nm

CMOS process.

The die photograph is shown in Fig. 4.12. The core dimension included inductors is 660μm x 1040μm. Figure 4.13 represents the operating frequencies at 25°C and the jitter histogram at 0.5 V, which demonstrates a 1.45-ps RMS jitter and a 10.47-ps peak-to-peak jitter (P2P jitter) at 2.4 GHz within 12.95k hits. The RMS and P2P period jitters are less than 0.35% and 2.53%, respectively. The voltage amplitude is 0.78V where bias tee voltage is 1.2V at V_{DD}=0.5V. The total power consumption is 2.5mW at V_{DD}=0.5V.

Figure 4.14 shows the measured results of the output spectrum and phase noise of 2.4 GHz output of the VCO with V_{DD}=0.5V. As shows in Fig. 14, the phase noise is -101.52 dBc/Hz @100kHz offset and -123.29 dBc/Hz @ 1MHz as T=20°C.

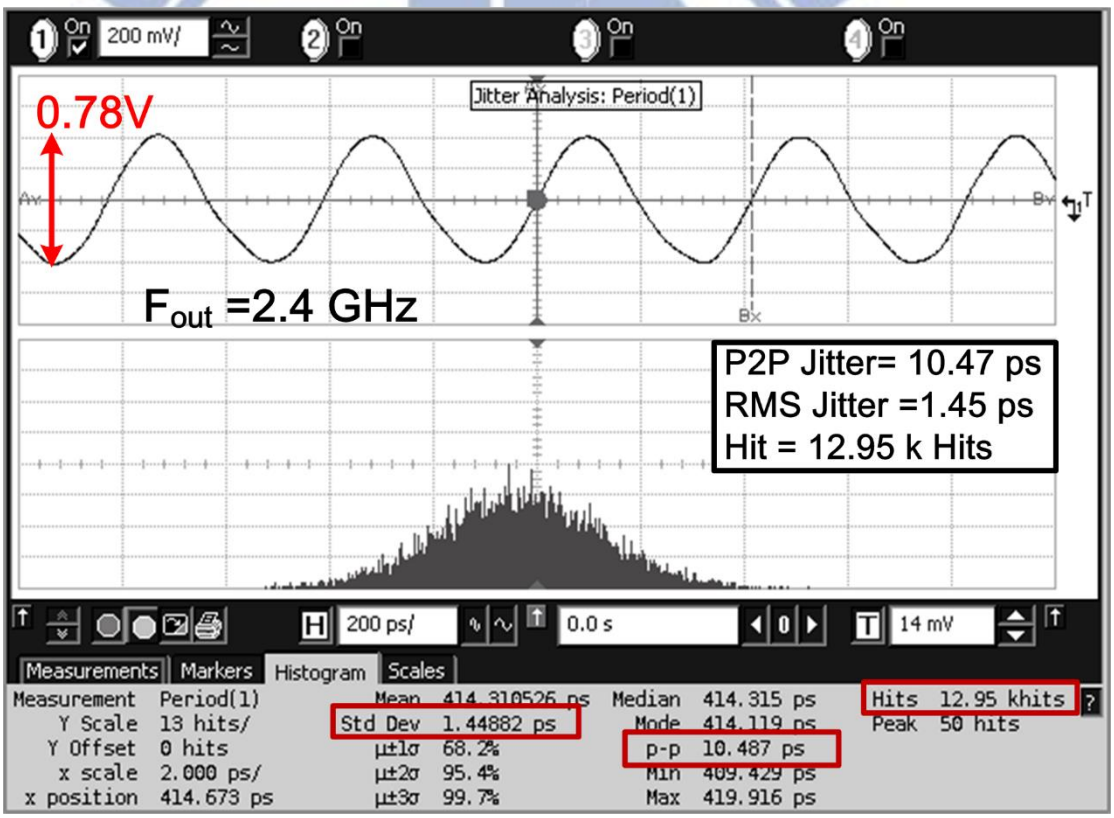


Figure 4.13 Jitter performances where RMS=1.45ps and P2P=10.47ps of 2.4GHz output at V_{DD}=0.5V.

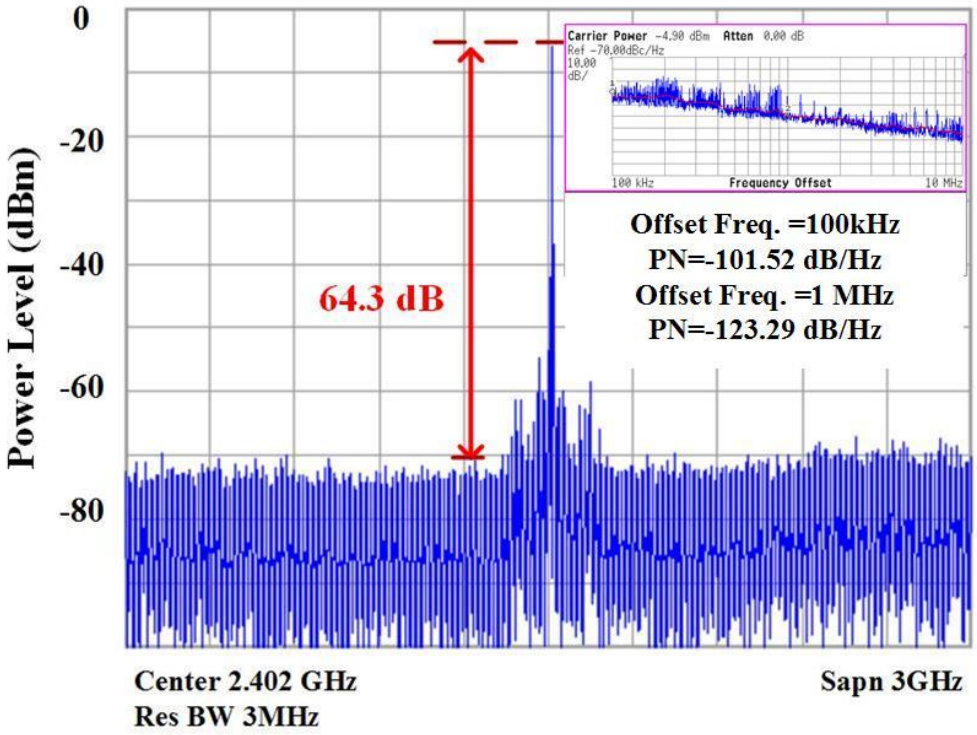
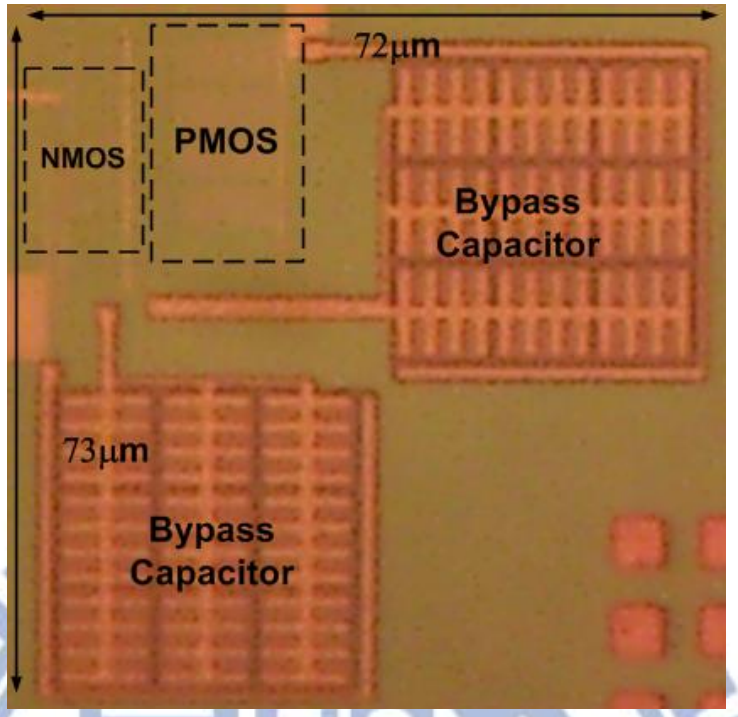


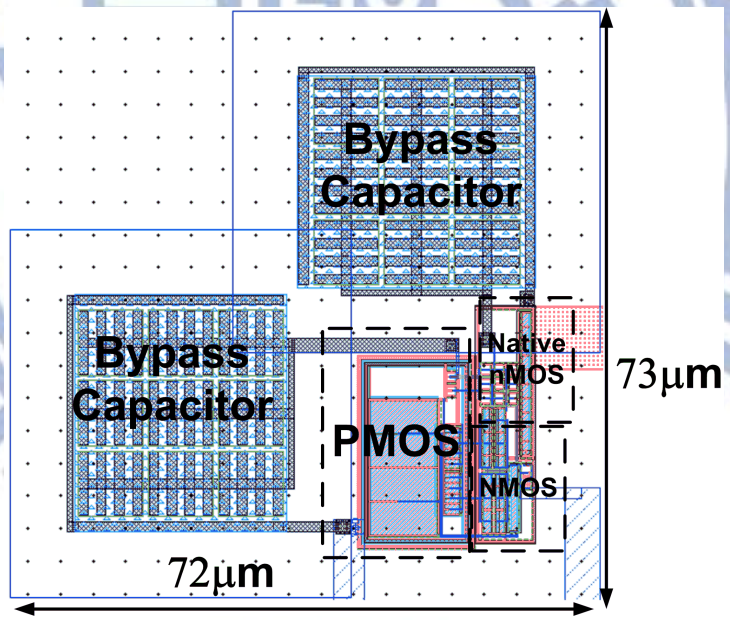
Figure 4.14. Measured output spectrum and phase noise of 2.4 GHz output of the VCO with a supply voltage of 0.5V.

4.3.4. Measurement of Voltage Reference Circuit

New proposed voltage reference circuit has been fabricated in TSMC 65nm General Purpose (GP) CMOS technology. The chip photo and layout of the fabricated voltage reference circuit are shown in Fig. 4.15 (a) and (b) separately. Chip size of the fabricated bandgap reference circuit is 0.0053mm^2 (72 × 73 μm^2). The threshold voltage of Low V_T (LVT) NMOS and PMOS are 0.246V and -0.257V separately.



(a)



(b)

Figure 4.15. (a)Die photo and (b) layout of the proposed CMOS voltage reference circuit.

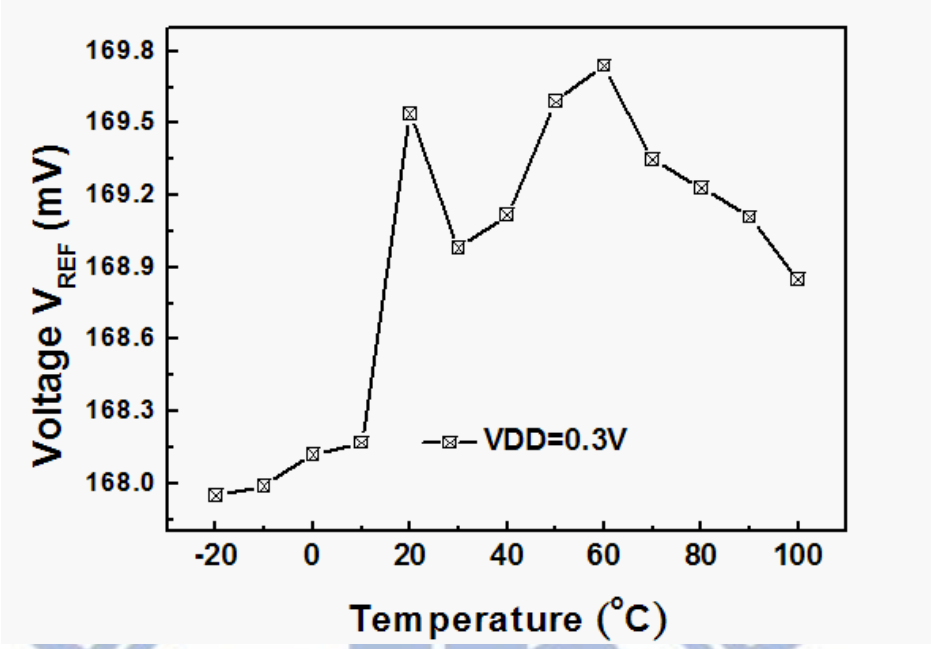


Figure 4.16 Measured output voltage as a function of temperature. Supply voltage sets to 0.3 V. Temperature coefficients 105 ppm/˚C were observed.

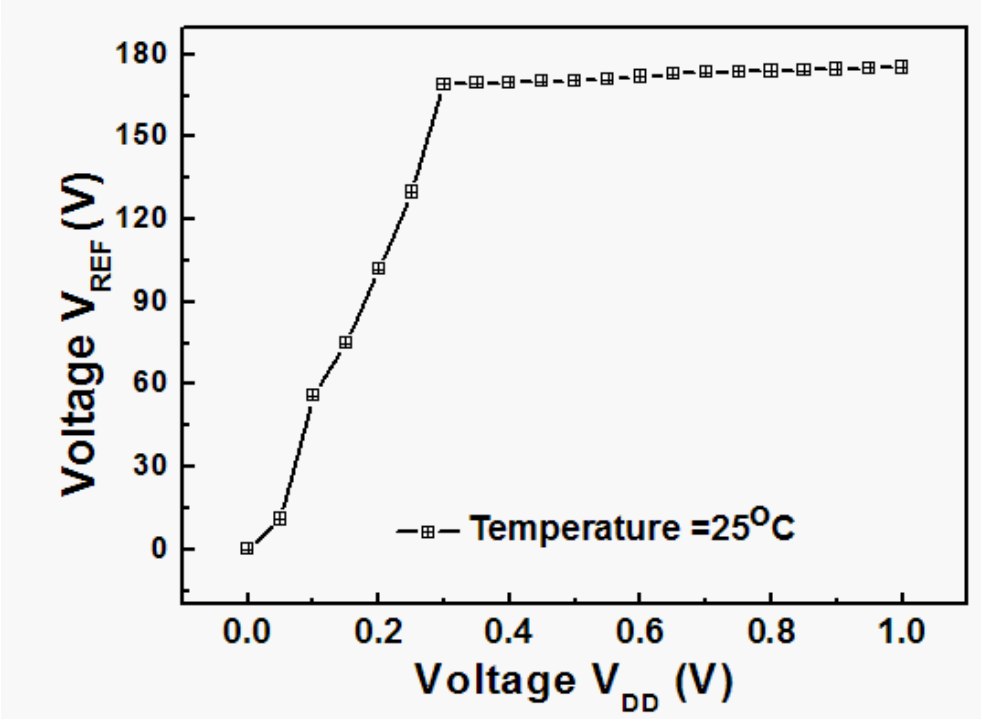


Figure 4.17 Measured output voltage VREF at room temperature (T=25˚C) as a function of power supply. Line regulation was 4.8% for supply voltages 0.3-1.0V.

The power supply voltage V_{DD} is set to 0.3 V as just for signal reference circuit test, and the total operating current is 193 nA. V_{DD} of integrated version has been redesigned to 0.5V. The measured results of the output voltage V_{REF} are shown in Fig. 4.16, and the measured temperature coefficient of the fabricated bandgap reference circuit is around 105 ppm/°C (without laser trimming after fabrication) from -20 to 100 ˚C, whereas the output voltage (V_{REF}) is kept at 168 mV.

The linear regulation shown in Fig. 4.17 is 4.8% from V_{DD} 0.3V to 1V. The linear regulation is higher than proper value because the transistors which are LVT MOSFETs are operated in saturation region instead of subthreshold region as supply voltage is higher than 0.65V. Besides, the dimensions of transistors are designed reasonable for 65nm GP CMOS process instead of large channel length which is used for reducing process variation and improving PSRR performance. The total power consumption of full circuit at V_{DD} =0.3V is about 70nW.

4.3.5. Measurement under PVT Variation

Frequency drift over temperature and power supply voltage was measured with the real-time oscilloscope (Agilent 81204B). Measured results with temperature compensation are shown in Fig. 4.18(a). After auto-calibration mechanism, one-point calibration which calibrates the initial frequency to 2.4 GHz at 30°C has been applied. The total measured temperature coefficient is 33.4 to 58.5 ppm/°C in the external 0.5-V unregulated power supply and over a temperature range of 0 to 100°C. The temperature variation of 5 chips is less than 0.5%. The worst case (Chip 3) is slightly overcompensated. The bits of digital temperature code DT<5:0> is insufficient to set a response with a less positive coefficient, though to add that functionality into future revisions is necessary.

The TC without auto-calibration is 556 ppm/°C. The result is similar to the simulation of TT corner. Therefore, frequency-drift of the VCO with the compensated circuit is 16.6 times of the original one without compensation. Fig. 4.18(b) shows the measured results of TC with supply voltage variation. TC of VDD +5%,-5%, +10%, -10% is 41.6 ppm/˚C, 47.9 ppm/˚C, 187 ppm/˚C, and 175 ppm/˚C separately. We can see that the temperature compensation of +/-10% is not enough to compensate the

frequency. Because the mapping table only has with 5% variation in order to keep 1-to-1 mapping. On the contrary, TC of VDD +5% is close to the VDD =0.5V. It means that the compensation mechanism is work at the condition of VDD +5%.

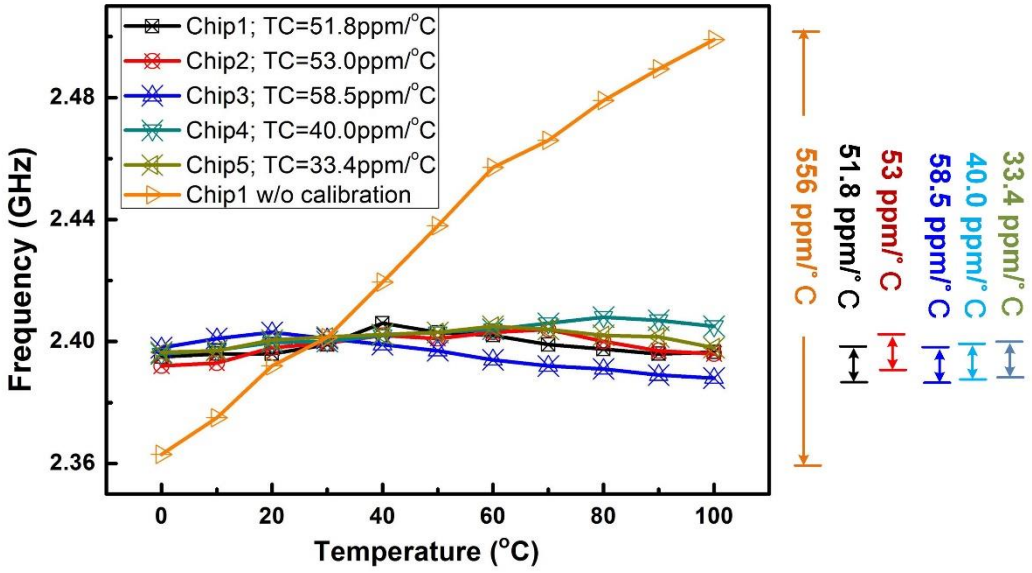


Figure 4.18 (b) Measured results of frequency versus temperature of the tested dies after temperature and process calibration

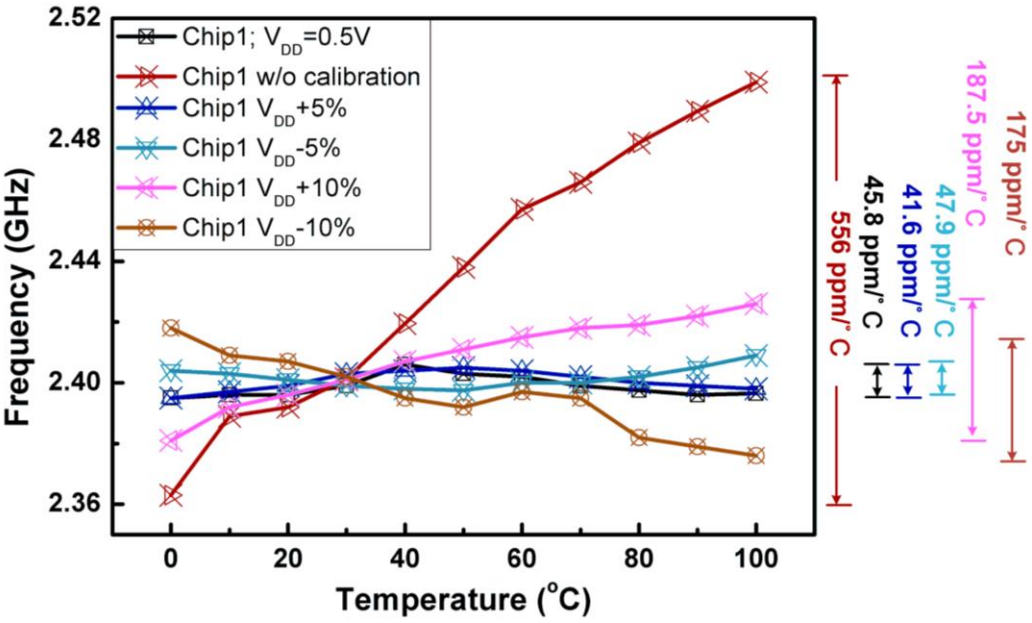


Figure 4.18 (b). Measured results of frequency versus temperature with the supply voltage variation

Simulated and measured results of the relationship between phase noise and temperature are shown in Fig. 4.19. Phase noise becomes worse as temperature increases. The gm of LC-VCO MOSFETs is getting worse at high temperature, and the Q value of an inductor in low temperature is higher than high temperature [24]. The two main reasons lead to high phase noise at high temperature.

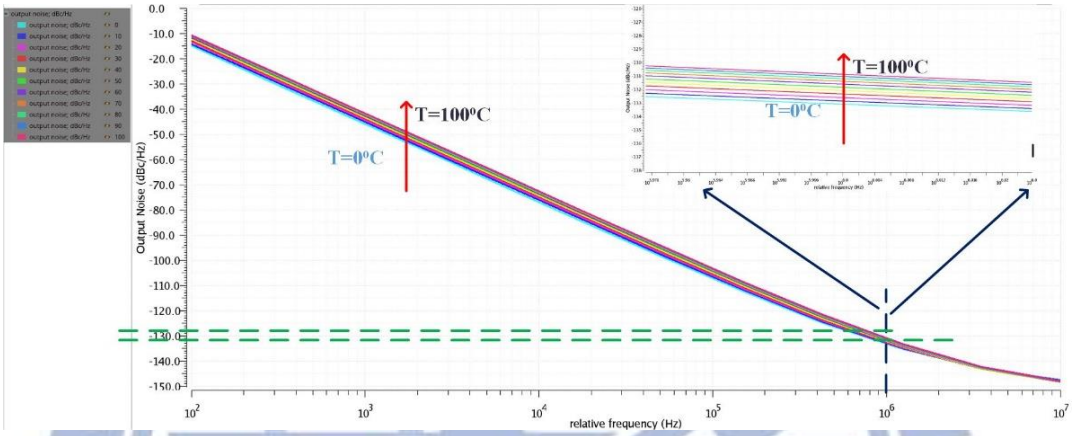


Figure 4.19 (a) simulated results of phase noise with temperature variation.

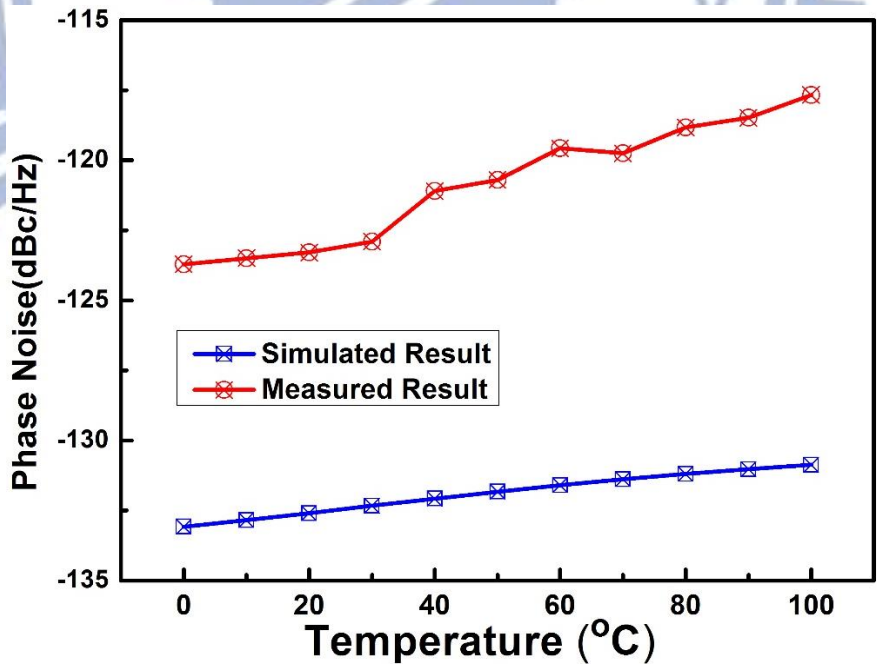
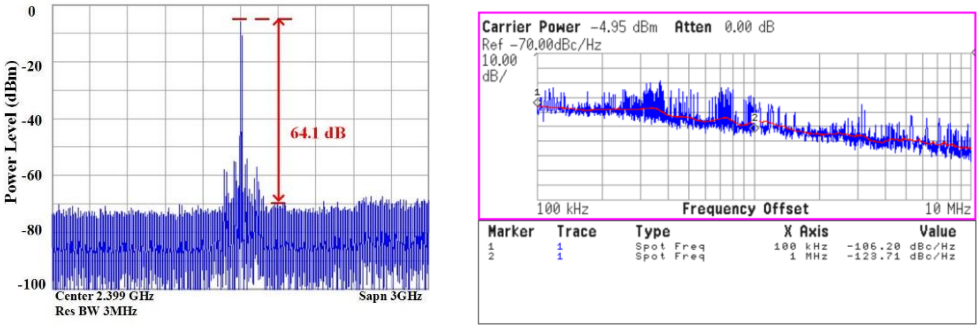
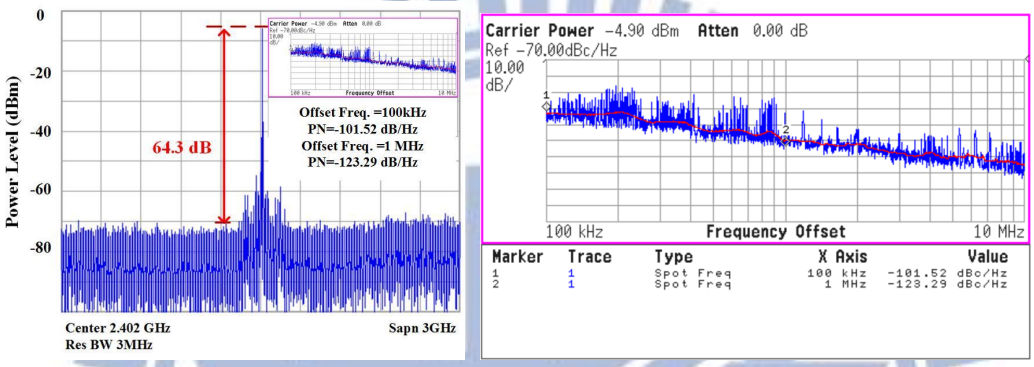


Figure 4.19 Measured and simulated results of the relationship between phase noise and temperature.

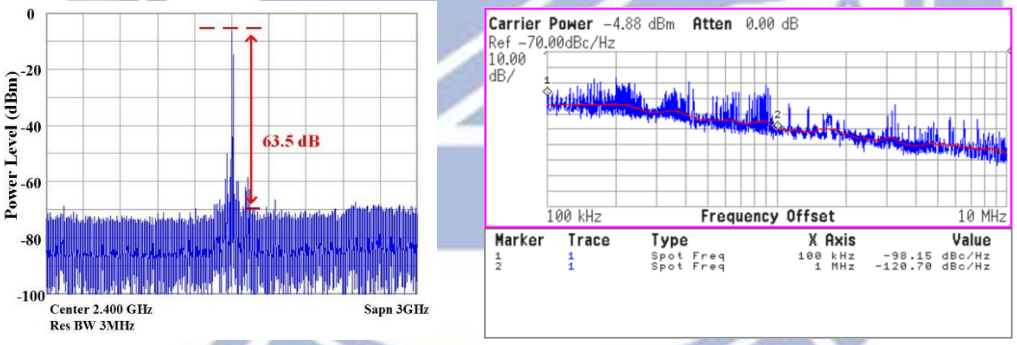
4.4.6 Output power spectrum and phase noise



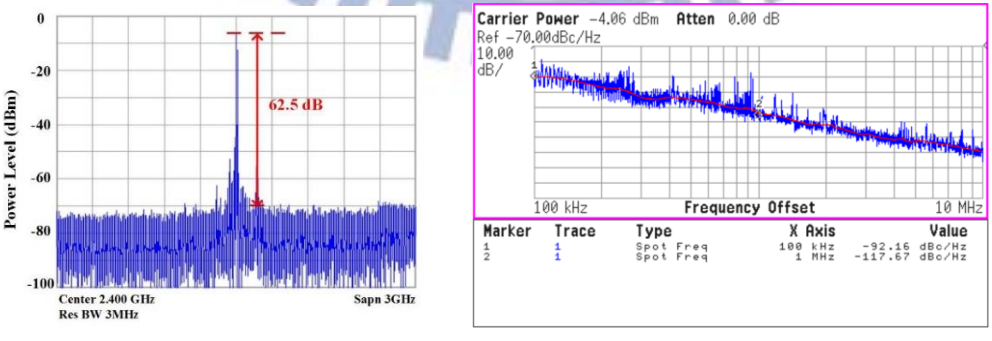
(a)



(b)



(c)



(d)

Figure 4.20 Measured Results of output power at (a)T=0℃, (b) T=20℃, (c) T=50℃, and (d) T=100℃.

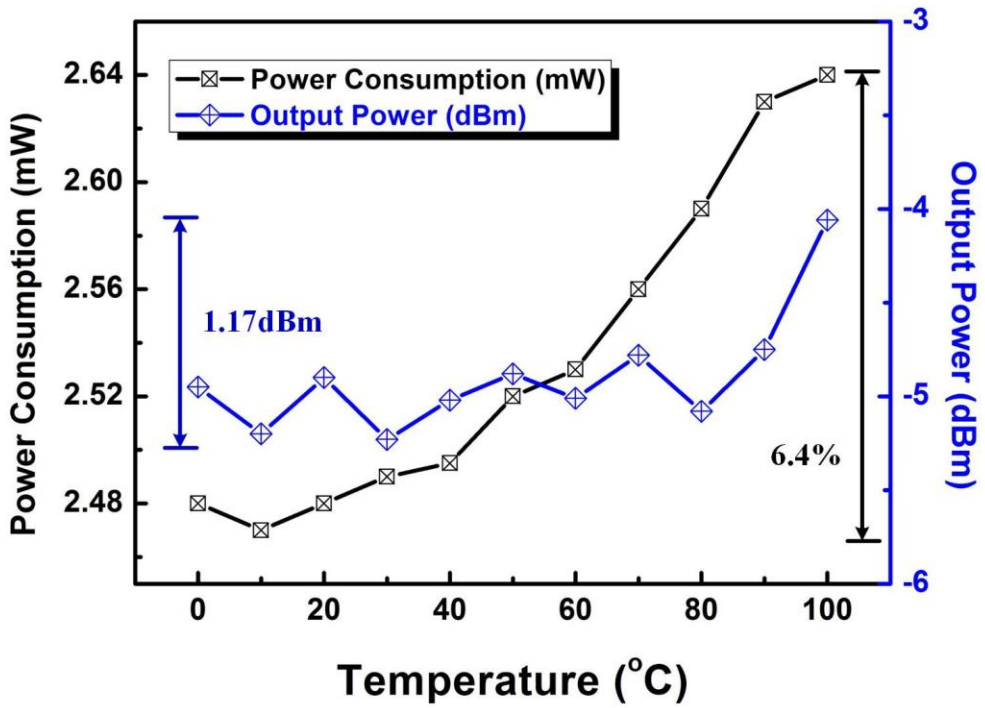


Figure 4.21 Measured results of power consumption and output power

Figure 4.20 shows the measured results of the output spectrum and phase noise of 2.4 GHz output of the VCO with VDD=0.5V. As shows in Fig. 4.20, the phase noise is -101.52 dBc/Hz @100kHz offset and -123.29 dBc/Hz @ 1MHz as T=20°C. The measured results show that temperature variations barely influence all of the output power. Measurement of power consumption and output power are summarized in Fig. 4.21. Output power change from -4.06 dBm to -5.23 dBm over a temperature range of 0 to 100°C. Measured results show that temperature variations barely influence all of the output power.

There are two main reasons to support the measured results. First, all the measured results are calibrated to a fixed frequency=2.4GHz by our calibrated mechanism. As output frequency does not vary with temperature, the variation of output power vary inconspicuously. Besides, the phase noise at high temperature, such as T=100°C, does not worsen sharply. It implies that the output signals still keep stable and sufficient output power.

Second, the output stage of CLCGs usually dominate the output power. The schematic of output stage and equivalent impedance of measured environment is shown

in Fig. 21. The buffers provide stable output signals, and the combination of the open drain device and the bias tee device has a characteristic of low loss. The buffers are designed for ensuring stable output signals in every simulation under different situations, and the stable measured output power reflect an achievement of the design purpose of the buffers and open drain circuit.

The power consumptions are 2.5 and 2.64 mW at T=20 and 100℃ respectively (excluding the output buffers and open drain circuit). We can infer that the power consumption increases as temperature raises from Fig. 4. 21. Considering the fact that LC VCO dominates power consumption, the total power consumption would be increased while LC VCO frequency increases resulting from increasing temperature. Moreover, the minor correlation of frequency and temperature calibrated by the compensated circuit is applied to mitigate the situation such that the power consumption is not supposed to be increased theoretically. However, our inference from Fig. 4.21 is disaccord with the effect introduced by the compensated circuits. The explanation to this contradiction relies on the absence of compensated circuits in other circuits, such as digital parts. This absence undoubtedly enlarges the power consumption since increasing currents of MOSFETs lead to increasing power consumption as temperature increases.

4.4.FOM and Comparison

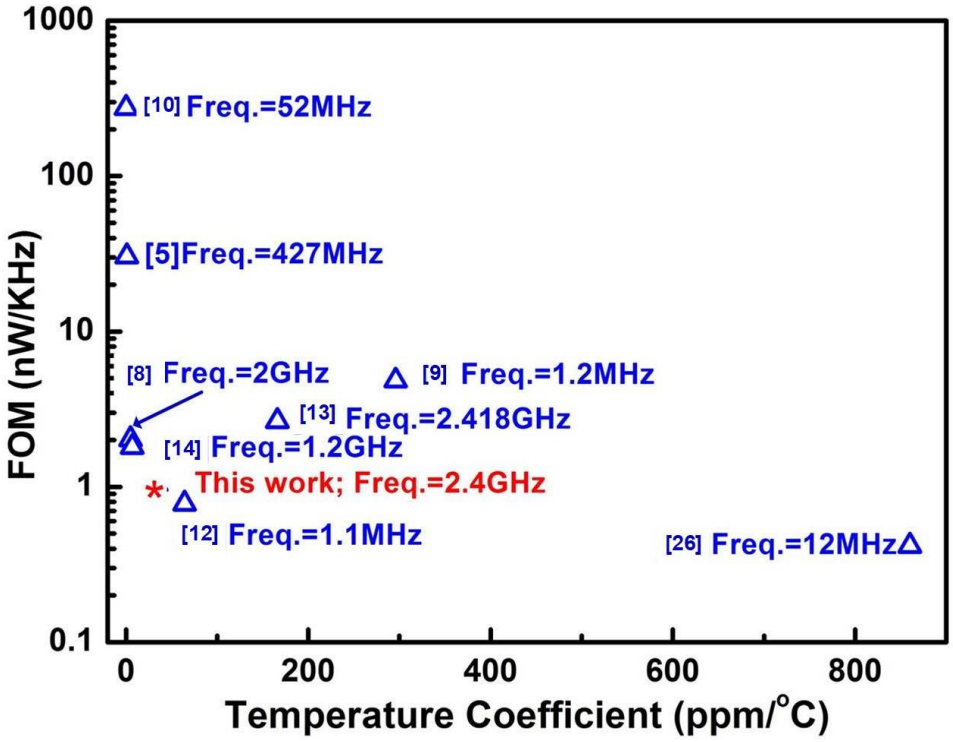


Figure 4.22. FoM versus Temperature Coefficients

Figure 4.22 shows the figure of merits (FoM) versus temperature coefficients. The FOM is defined as the ratio of the power consumption to the oscillation frequency (nW/kHz) [12], which is shown as below.

$$\boldsymbol{FOM = \frac{Power\ Consumption}{Operating\ \ Frequency}\ (nW/KHz)} \qquad ()$$

Calculated FOM is 1.04 nW/kHz for the proposed circuit. The crystal-less clock generators in Table 1 are classified into two categories by their operating frequency. One aims to replace XOs and is operated around MHz, such as [11] and [21]. The other is a substitute for XOs and multipliers and is operated around GHz, such as [7] and [12]. The low operating frequency have better FOM because the existence of large noise provided by frequency multipliers is not included in FOM. Although, the FOM of our proposed work are slightly higher than [11] and [21], the TC of our work is actually better than [11] and [21]. In other word, our proposed work is considerably competitive if the above papers are operated at around GHz.

The proposed technique could not only be operated at ultra-low voltage, 0.5 v, and high frequency around GHz, but also automatically calibrate its temperature and

process. As the related works only focus on a part of scenarios, either on supply voltage, power consumption, or frequency accuracy, the main contribution of the proposed method is the very first design investigating the whole situations.

4.5.**Conclusion**

Table II summarizes the results of this work and compares with previous temperature compensated clock generators. Comparing to other on-chip works, such as ADPLL, DLL and RC oscillator, the proposed ULV CLCG exhibits the lowest temperature sensitivity and comparable low jitter performance. The oscillators of MEMS and FBAR have lower TC and better phase noise than others structures. However, the MEMS oscillator needs additional MEMS mask process, and FBAR resonator has to fabricate with BiCMOS process. In addition, above MEMS or FBAR

Table 4.1 Performance comparisons of clock generators

Parameter	TCASII'14[12]	ASSCC'12[26]	TCASII'14[9]	JSSC'13[10]	JSSC'12[5]	IUS'06[8]	ISSCC'14[13]	JSSC'16[14]	This Work
Temp. Comp. Method	On Chip	On Chip	Material	Off Chip	Material+ Off Chip	Material	On Chip	On Chip	On chip
Technology (nm)	180	65	130	350	180*	Bi-CMOS	40	65	65
Supply Voltage (V)	1.8	0.3	1.8	2.5	2.5	2.7	1.1	1.2	0.5
Frequency (MHz)	1.1	12	1.2	52	427	2000	2418	1200~2000	2400
Power(mW)	0.00086	0.005	0.0058	14.25	13	4.05	6.4	3.6	2.5
TC(ppm/°C)	64.3	<860	296	0.02	0.805	5	166	6.9	33.4
Jitter (ps) (RMS)	N/A	0.294ns 287ps	33n	3.2	N/A	N/A	3.29 N/A	0.44	1.45 10.47
Phase Noise (dBc/Hz)	-74.2 @1MHz	-105.69 @1MHz	N/A	-142 @1MHz	-145 @1MHz	-138 @1MHz	-94.3 @1MHz	-122.53 @1Mhz	-123.29 @1MHz
Area (mm^2)	0.075	0.0048	0.016	5.049	0.7	5.6	0.02	0.032	0.665
FOM (nW/KHz)	0.78	0.416	4.83	274	30.44	2.025	2.647	1.8	1.04

designs are high power consumption with large die dimension.

The proposed ultra-low-voltage crystal-less clock generator with auto calibrated process and temperature compensated circuit has been successfully verified in a 65 nm CMOS technology. LC VCO provides low jitter and high phase noise performance, and TCC with an auto-calibration technique can detect and compensate the variations from the process and temperature. As demonstrated in this work, the proposed design that makes the operation of CLCG with very low supply voltages, down to 0.5 V, as well as achieve sufficient high frequency stability and accuracy against the variations from process and temperature for the HBC application.

Chapter 5. Conclusion and Future Works

This chapter summarizes the specific new results of this dissertation. Future works for CLCG with PVT compensaiton topics are also addressed in this chapter.

5.1. Specific New Results of This Dissertation

Chapter 1 clarify of PVT variation of clock system and introduce the necessary of PVT compensation.

Chapter 2 discuss of CLCG with PVT compensated circuits and related compensated methods.

This dissertation mainly proposes two structures of CLCG with their PVT compensation circuits for different applications.

Firstly, one multi-phase crystal-less clock generator (MPCLCG) with a PVT calibration circuit is proposed in Chapter 3. It operates at 192 MHz with 8 phases outputs, and is implemented as a 0.18 μm CMOS process for digital power management systems. A temperature calibrated circuit is proposed to align operational frequency under process and supply voltage variations

The other is ultra-low-voltage crystal-less clock generator with an auto-calibrated process and temperature circuit, which is proposed in Chapter 4. The auto-calibrated process and temperature compensated circuit includes a process detector to detect process variation and all digital compensation circuit.

Beside, appendix A and appendix B also provide temperature related discussed in their own fields. Appendix A discuss the electron distribution in an amorphous indium-gallium-zinc-oxide (a-IGZO) thin film transistor (TFT) with a floating metal-semiconductor (MS) back interface by using the technology computer-aid design (TCAD) model. Appendix B propose the temperature coefficient (TC) of LTPS TFT devices and the relationship between the activation energy and the TC.

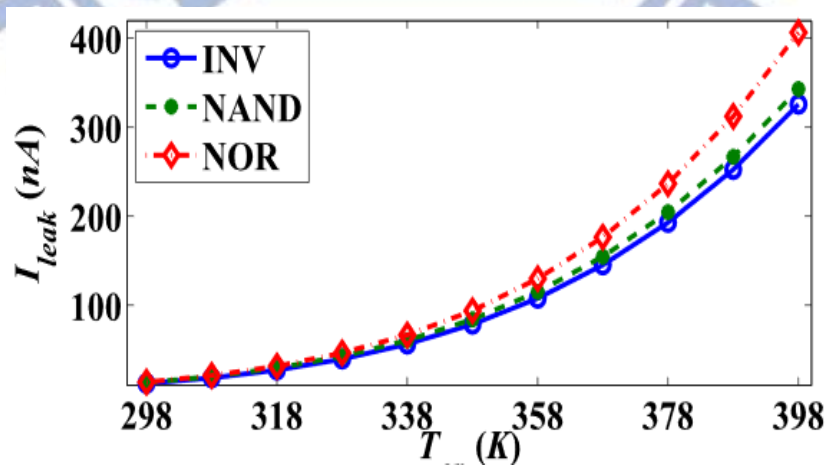
This dissertation find out various kinds issues about temperature variations. And we provide reliable solutions to overcome these variations

Appendix A investigates electron depletion effect in a-IGZO TFT with a floating capping metal by TCAD simulation and leakage reduction. This paper verifies that capping metals with various work functions on the IGZO back interface significantly affects electron distribution.

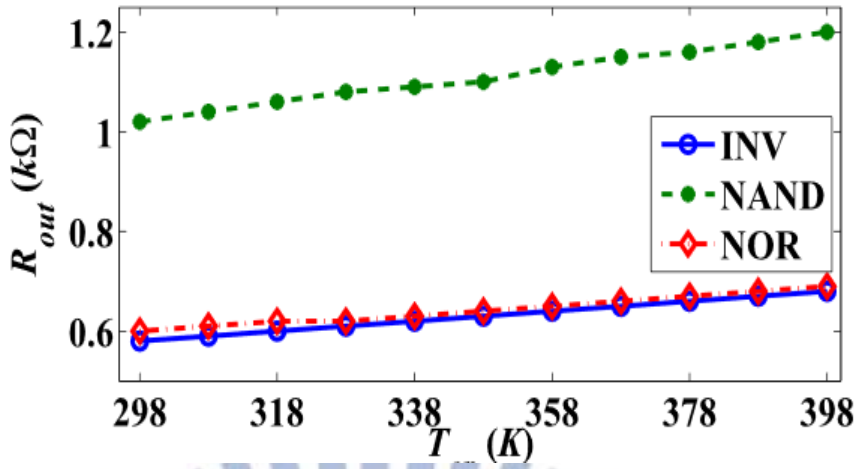
5.2.**Future Works**

Continued scaling of bulk CMOS technology is facing formidable challenges. FinFET of the 16 or 22-nm technology still suffer from PVT variations. FinFET circuits need to be carefully optimized with temperature taken into consideration. Fig. 5.1 shows the relationship between temperature and leakage current, R_{out}, and C_{out} of logic gates of FinFET [84]. Leakage current becomes worse as temperature increases. Beside, R_{out} and C_{out} also strongly influence by the temperature variations.

Therefore, we find that FinFET circuits need to be carefully optimized with temperature taken into consideration, since the ratio between the leakage currents of a circuit can vary drastically depending on the operating temperature assumed. CLCG with PVT compensation circuits could be further discuss of the FinFET devices.



(a)



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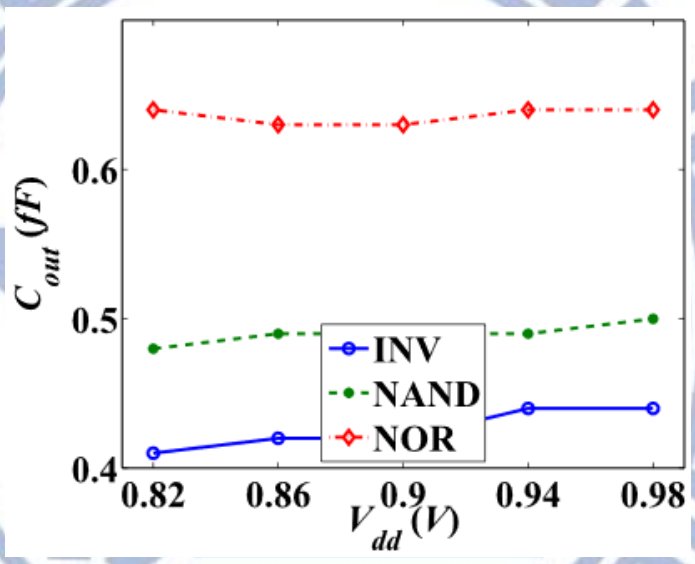


(c)

Figure 5.1 Effect of process/voltage variations on (a) I_{leak}, (b) R_{out}, and (c) Cout (T_{op}=298 K) [84].

Since the proposed CLCGs with PVT compensated circuits are not actually real time auto calibrated circuit, these circuits only provide one time auto-calibrated mechanism. I will continue invest and figure out the technique in the future.

Appendix A. Investing Electron Depletion Effect in Amorphous IGZO TFT with a floating capping metal by TCAD

The electron distribution in an amorphous indium-gallium-zinc-oxide (a-IGZO) thin film transistor (TFT) with a floating metal-semiconductor (MS) back interface is analyzed by using the technology computer-aid design (TCAD) model. The channel geometry (i.e. length and thickness) effect is carefully investigated. With a high work function (i.e. 5 eV) in the capping metal, the capping metal (electron depletion effect) mostly removes electrons inside a-IGZO. The depleted IGZO film leads to an increase of threshold voltage in a-IGZO TFT. TCAD simulation reveals that increasing channel length and decreasing IGZO thickness significantly enhance such an electron depletion effect. Finally, the electron depletion effect is applied on a-IGZO TFT with high conductivity IGZO film to greatly suppress the leakage current over 5 orders.

A.1 Introduction

Recently, amorphous In-Ga-Zn-O (a-IGZO) thin-film transistors (TFTs) have attracted considerable interest for applications to the active-matrix (AM) backplane of LCD and OLED displays because of their excellent characteristics, such as high mobility and uniform amorphous structure [59], [60]. Electron transport in a-IGZO is known to follow percolation transport [61], [62]. Potential barriers generated due to the random distribution of Ga^{3+} and Zn^{2+} ions in the network structure strongly limit the carrier transport. Increasing carrier concentration can reduce the potential barrier and hence improve the carrier mobility [63], [64]. High electron concentration in channel region, however, leads to either leakage between source and drain electrodes or a negatively shift threshold voltage [65]. For achieving a better control of the leakage current, electron concentration should be kept low in channel region [66]. Even with

identical IGZO film property, capping different materials onto back interface of a-IGZO may also affect the carrier concentration in channel region [67], [68]. In our previous work, we investigated the threshold voltage shift in a-IGZO TFT by capping a floating metal onto the back interface of a-IGZO [69]. Electron depletion or electron injection was proposed to explain the threshold voltage shift when the capping metal has high work function (e.g. 5 eV) or low work function (2.9 eV), respectively.

Here, with Silvaco TCAD simulation, we further investigate the geometry effect of the electron depletion phenomenon. Two-dimensional electron distribution reveals that capping floating metal with high work function (e.g. 5 eV) reduces channel electron concentration from 2×10^{18} cm^{-3} to 5×10^{13} cm^{-3}. Reducing film thickness and increasing channel length enhances the electron depletion effect. Finally, we applied the electron depletion effect to do leakage control experiment. For a-IGZO TFT with a UV-treated conductive channel, capping a floating gold onto the central region of back interface reduces the off-state current from 3×10^{-4} A to 5×10^{-9} A.

A.2 Simulation Setting and Experimental

The insets of Fig. A.1(a) and Fig. A.1(b) show the schematic diagram of a standard bottom gate a-IGZO TFT (STD device) and a floating-metal-capped (FMC) IGZO TFT. In this paper, source and drain electrodes are 10-nm-thick aluminum. Gate insulator is a 100-nm-thick silicon nitride. Channel length is ranged from 200 μm to 0.2 μm. IGZO thickness is changed from 100 nm to 5 nm. For FMC IGZO TFT, a floating metal with a work function ranged from 5.5 eV to 4 eV is capped onto the central region of back interface between the source and the drain electrodes. The length of the floating metal is fixed as half of the channel length. To discuss electron distribution under thermal equilibrium, drain to source voltage (VDS) and gate to source voltage (VGS) are both 0 V. The permittivity, electron affinity, and energy gap at 300K of IGZO are 4 F/m, 3.8 eV, and 3 eV, respectively. The electron and hole mobility are 10 $cm^2/V \cdot s$ and 10^{-5} $cm^2/V \cdot s$. Conduction band density and valence band density at 300K are 5×10^{18} cm^{-3} and 5×10^{18} cm^{-3}, respectively. Different gate bias is applied only in Fig. A.3(a) and Fig. A.4(c) when we discuss the restoring of electron concentration.

Heavily doped p-type Si (100) was used as a substrate and as a gate electrode. A

100-nm-thick silicon nitride was deposited by low pressure chemical vapor deposition at 780˚C to serve as the gate dielectric. Then, a 35-nm-thick a-IGZO layer (3 inch circular target, In:Ga:Zn=1:1:1 atom %) was deposited through a shadow mask at room temperature by using a radio-frequency sputtering system with a power of 100 W, a working pressure of 5 mtorr, and an Ar flow rate of 20 sccm. The width of IGZO layer is used to define the channel width (W) as 1000 μm. Then, 100-nm-thick Ti pads were evaporated through shadow mask to form source and drain electrodes and to define the channel length (L) as 400 μm. UV treatment was done in nitrogen environment while the wavelength and the power density of the Xe excimer lamp were 172 nm and 50 mW/cm^2, respectively. Finally, gold pad (width as 1000 μm and length as 200 μm) was evaporated through a shadow mask to cap the central region of the back interface. All electrical characteristics were measured by Agilent 4156 I-V analyzer. The threshold voltage and the mobility were extracted from the slope and the x-axis intercept of the $\sqrt{I_D}-V_G$ curves in saturation region (V_D = 20 V).

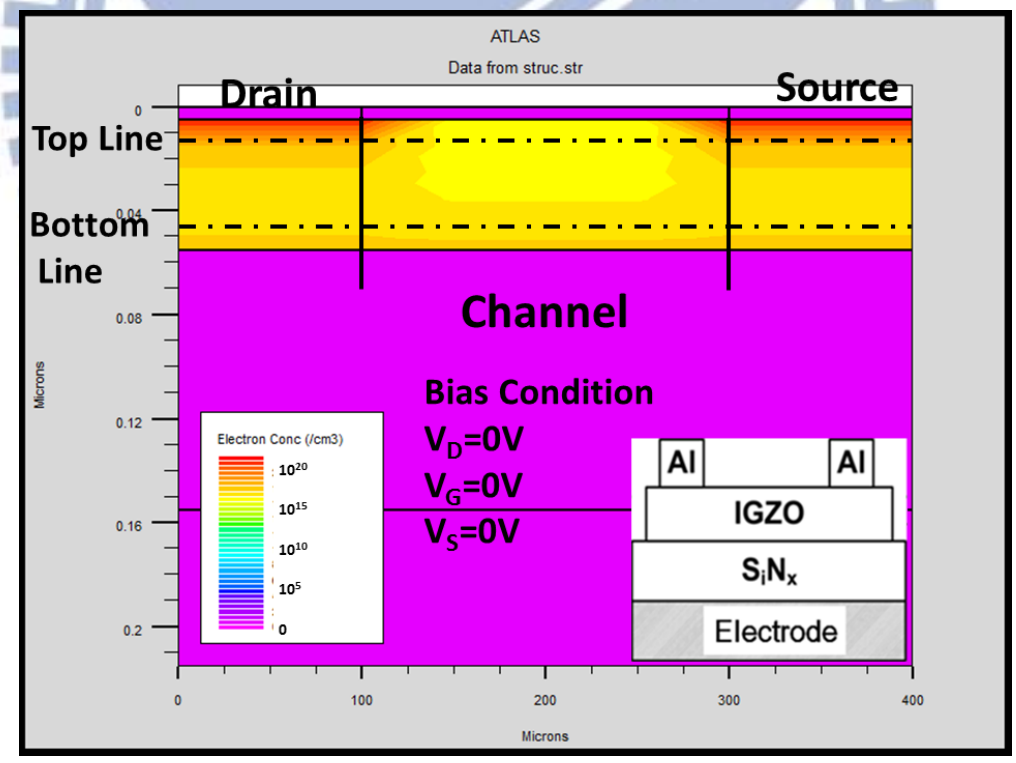


Figure A.1 The 2-D electron concentration for (a) a standard (STD) a-IGZO TFT and (b) a floating-metal-capped (FMC) IGZO TFT. The work function of the floating metal in (b) is 5 eV.

A.3 Simulation Results

Firstly, we compare the 2-dimentional electron distribution in a standard IGZO TFT and a floating-metal-capped (FMC) IGZO TFT as shown in Fig. A.1(a) and Fig. A.1(b), respectively. In Figs. A.1(a) and A.1(b), channel length is 200 μm and IGZO thickness is 50 nm. Work function of the floating metal is 5 eV. We can clearly observe that the electron concentration under floating metal in Fig. A.1(b) is much smaller than that in the central channel region of STD device in Fig. A.1(a). We further compare the electron concentration close to back interface and front channel by plotting the 1-dimentional electron distribution along the Top Line and Bottom Line, respectively. Top Line, as indicated in Fig. A.1(a) and Fig. A.1(b), locates in upper IGZO film with a distance to back interface as 10% IGZO thickness. Bottom Line, on the other hand, locates in lower IGZO film with a distance to front interface as 10% IGZO thickness.

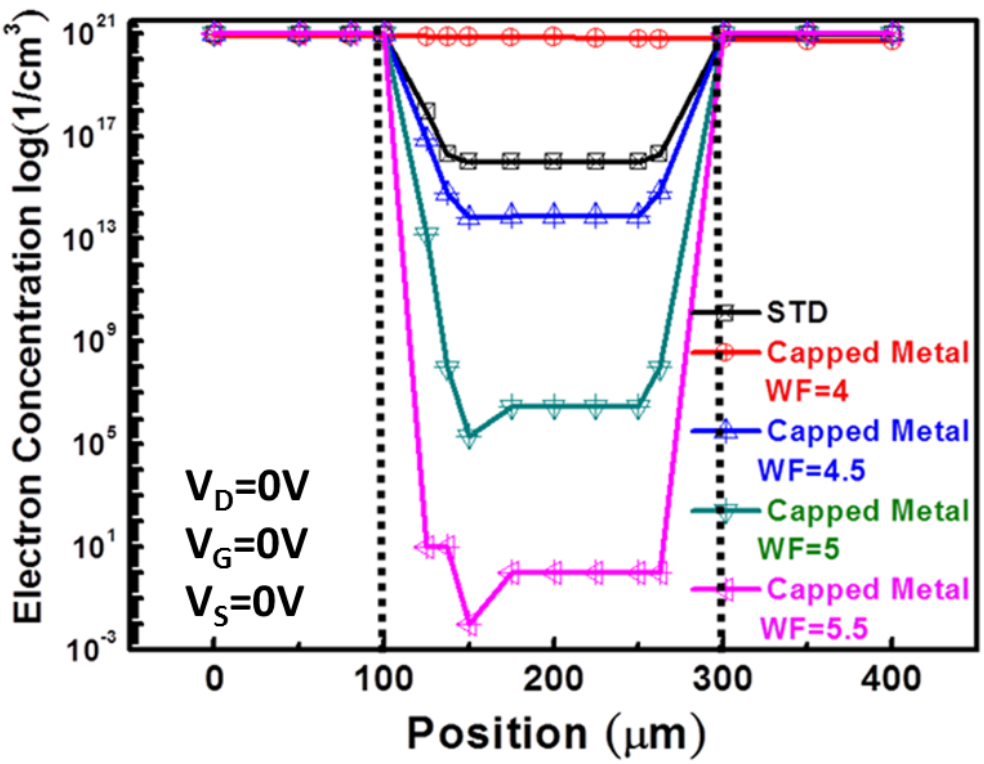


Figure A.2(a)

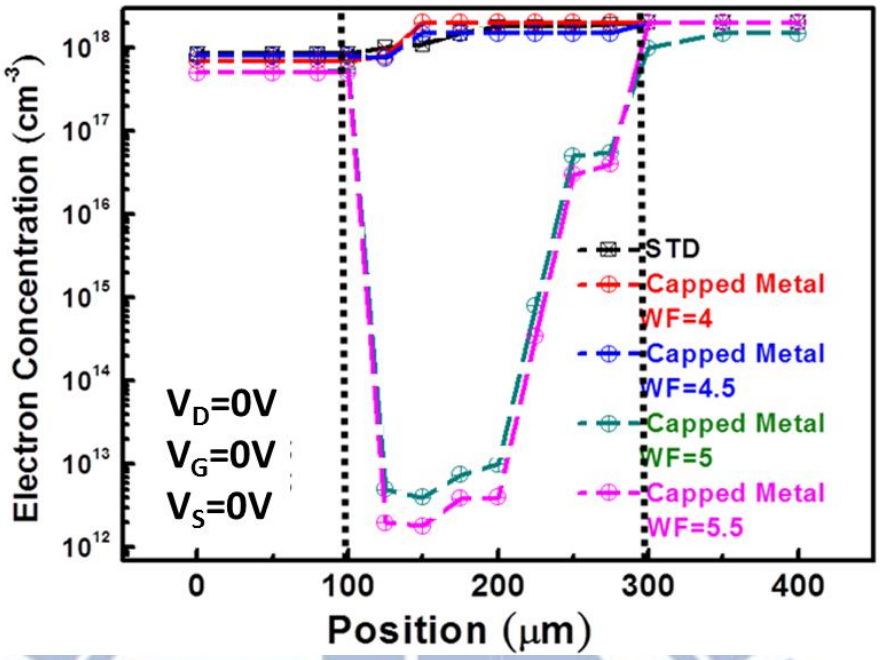


Fig. A.2(b)

Figure A.1 The electron concentration along (a) Top Line and (b) Bottom Line in STD and FMC IGZO TFTs with different work functions of the floating metal.

Figure2 (a) shows the electron concentration along Top Lines when the floating capping metal exhibits different work functions. The ratio of channel length to capping metal length is kept as 2:1. The work function of capping metal varies from 4 eV to 5.5 eV. As the work function of capping metal increases, the electron concentration in the channel decreases. The IGZO body is almost depleted as the work function of capping metal is 5.5 eV. This verifies that electrons in IGZO are removed by the capping metal when work function of capping metal is higher than that of IGZO. When the work function of capping metal is 4, electron concentration is higher than that of STD device, revealing an injection of electrons from capping metal to IGZO film.

The electron concentrations along Bottom Lines when the floating capping metal exhibits different work functions are shown in Fig. 2(b). When the work function of capping metal is 5 eV or 5.5 eV, electron concentration at Bottom Line is significantly reduced, indicating that the electron depletion effect also affects the electron concentration in front channel region. A more positive threshold voltage is required to induce sufficient electrons in front channel to turn on the transistor. For such electron-depleted devices, the influences of gate bias on electron concentration at Bottom Line

are investigated.

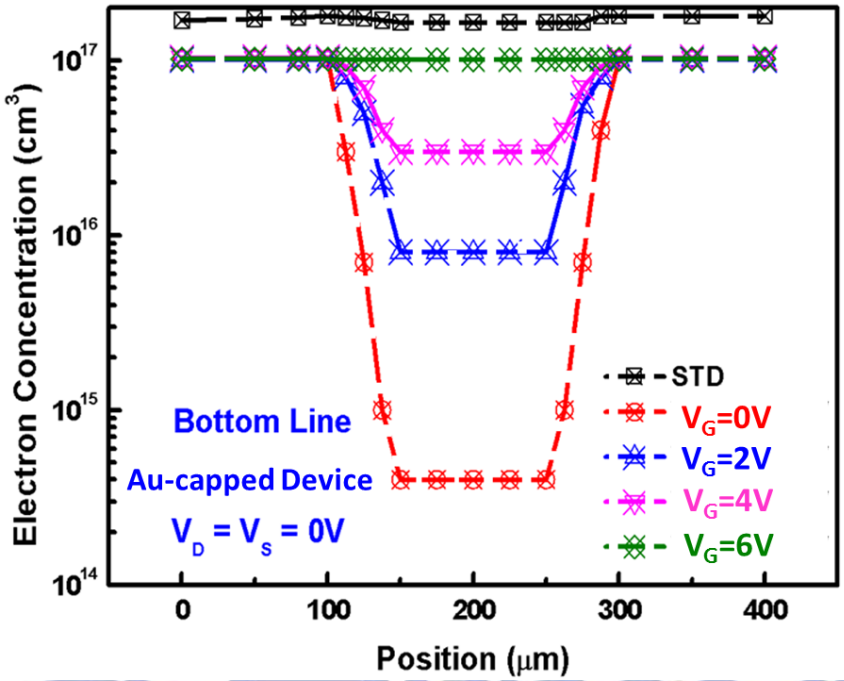


Fig. A.3 (a)

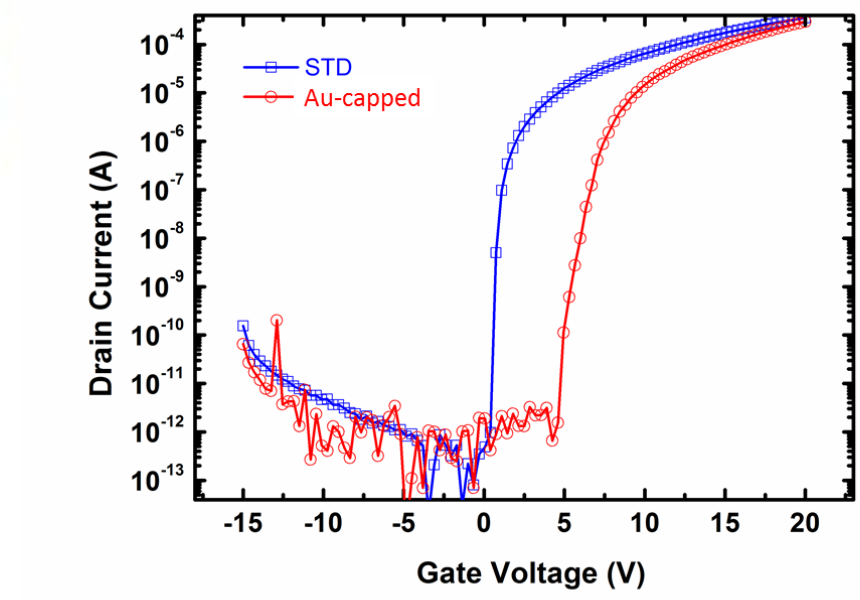


Figure A.3 (b)

Figure A.2 (a)The electron concentration of STD and FMC a-IGZO TFT with different gate bias. Drain and source are grounded (VD=VS=0). (b) The experimental transfer characteristic of STD and Au-capped a-IGZO TFTs.

As shown in Fig. 3(a), for Au-capped device (i.e. the work function is 5 eV),

electron concentration at central position increases from 3×10^{14} cm^{-3} to 1×10^{17} cm^{-3} when gate bias is added from 0 V to 6 V. For STD device, front-channel electron concentration is 1.4×10^{17} cm^{-3}.

Results in Fig. A.3(a) suggest that, by applying a suitable gate bias, the electron concentration at Bottom Line of FMC IGZO TFT can be almost identical to that of STD IGZO TFT. The applied gate bias, which restores the electron concentration of FMC IGZO TFT, is about 6 volts. Experimentally, as shown in reference [64] and reproduced in Fig. A.3(b), a 6-V threshold voltage shift is also observed when capping floating gold metal onto the back interface of a-IGZO TFT. It is noted that the device geometry in experimental results (Fig. A.3(b)) and in simulated results (Fig. A.3(a)) are the same. Here we define that the applied gate bias to restore the Bottom-Line electron concentration is named as VG, restore.

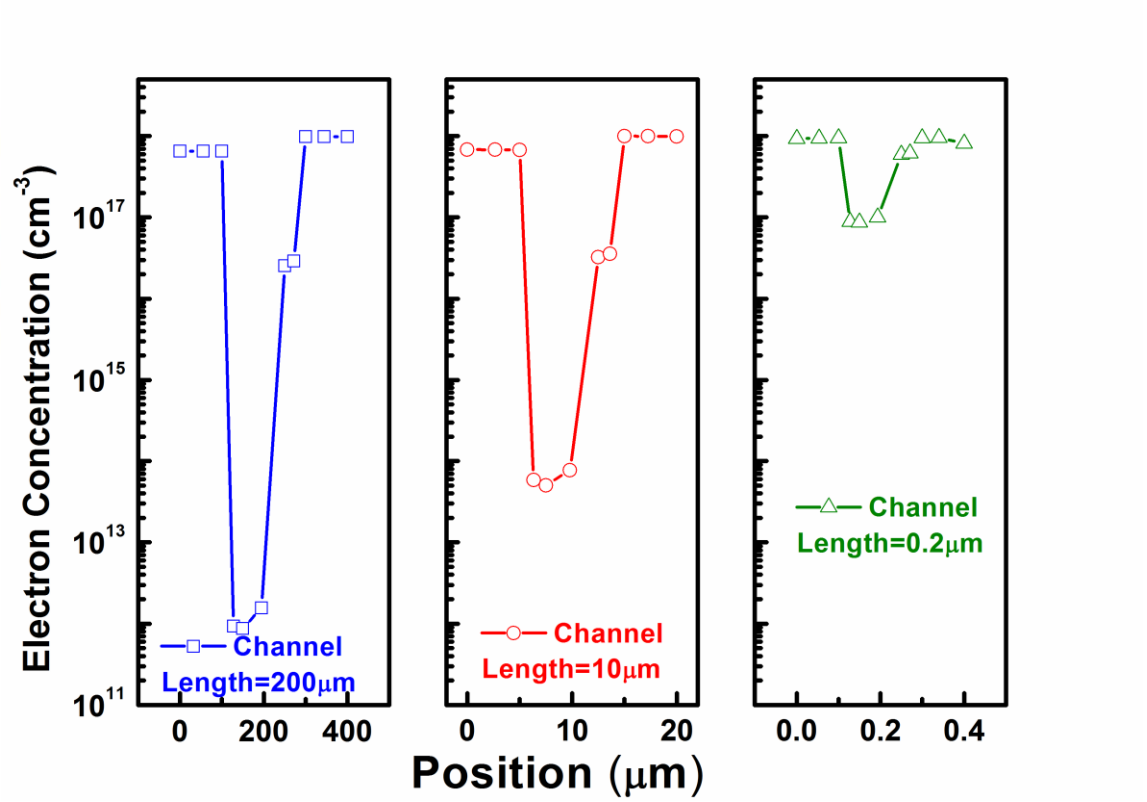


Figure A.4 (a)

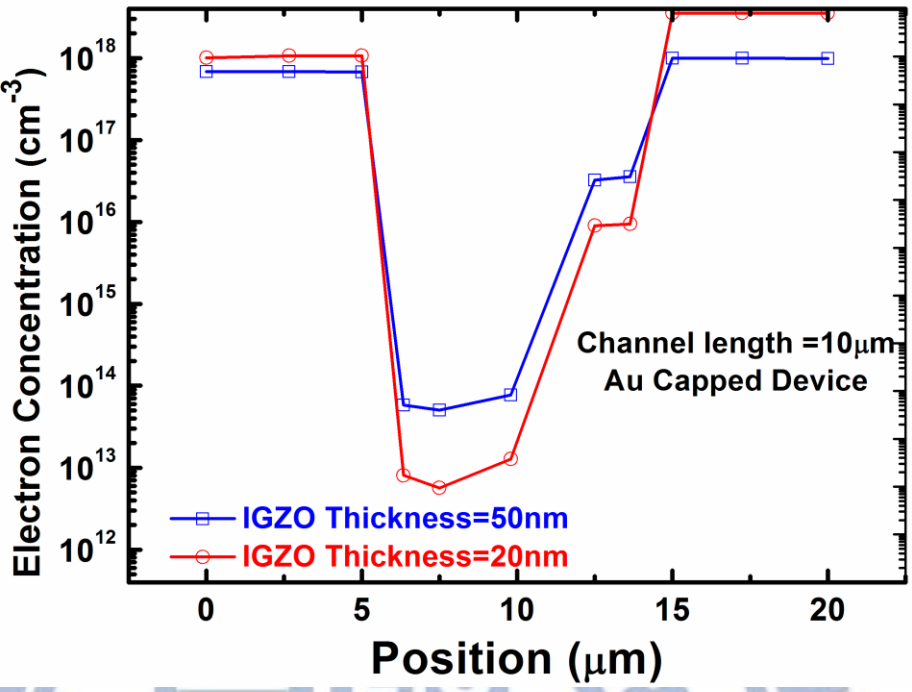


Figure A.4 (b)

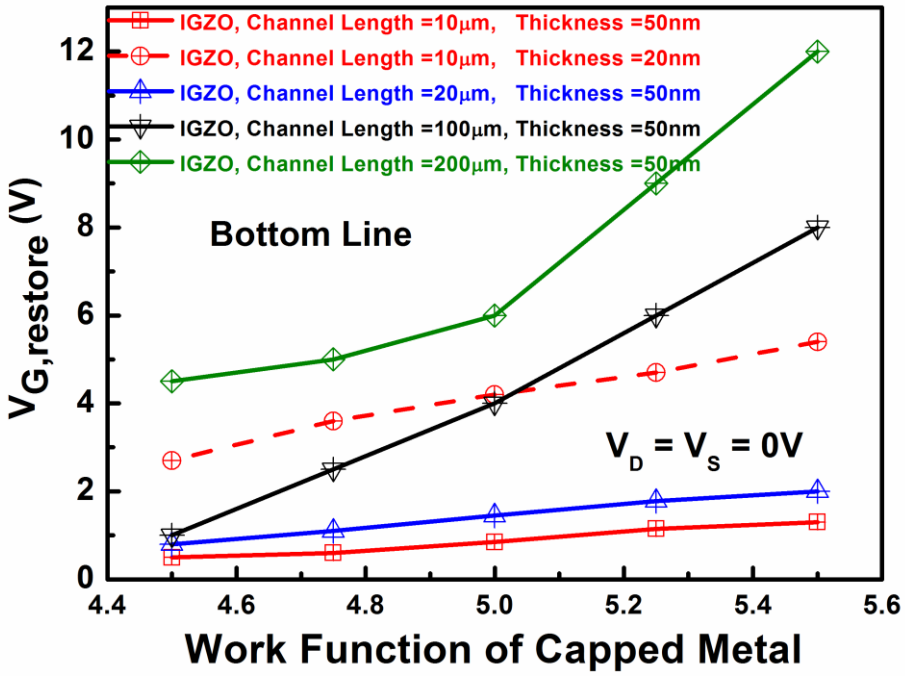


Fig. A.4 (c)

Figure A.3 Bottom-Line electron concentrations of Au-capped IGZO TFT with (a) different channel length and (b) different IGZO thickness. (c) $V_{G,restore}$ plotted as the work function of the floating capping metal with different channel length and

IGZO thickness

We then further compare the Bottom-Line electron concentrations of Au-capped IGZO TFT with different channel length and different IGZO thickness in Figs. A.4(a) and A.4(b), respectively. When channel length reduces from 200 μm, 10 μm, to 0.2 μm in Fig. A.4(a), electron depletion effect in front channel region becomes less and less obvious. With a fixed channel length as 10 μm, in Fig. A.4(b), electron depletion effect becomes more significant when IGZO thickness decreases from 50 nm to 20 nm. The geometry effect can be observed more clearly when comparing $V_{G,restore}$ of devices with different channel geometries and with different capping metals. In Fig. A.4(c), $V_{G,restore}$ is plotted as the work function of the floating capping metal. For all these cases with different channel length and different IGZO thickness, $V_{G,restore}$ becomes more positive when the work function of the capping metal is increased. Reducing channel length and increasing IGZO47 thickness lead to a reduction in $V_{G,restore}$. Specifically speaking, for channel length as 10 μm and IGZO thickness as 50 nm, $V_{G,restore}$ is smaller than 1.3 V, indicating that capping metal has only little influence on device performance. Reducing IGZO thickness to 20 nm and keeping channel length as 10 μm, however, produce a large $V_{G,restore}$ (2.5 V to 4.5 V) due to the electron depletion effect.

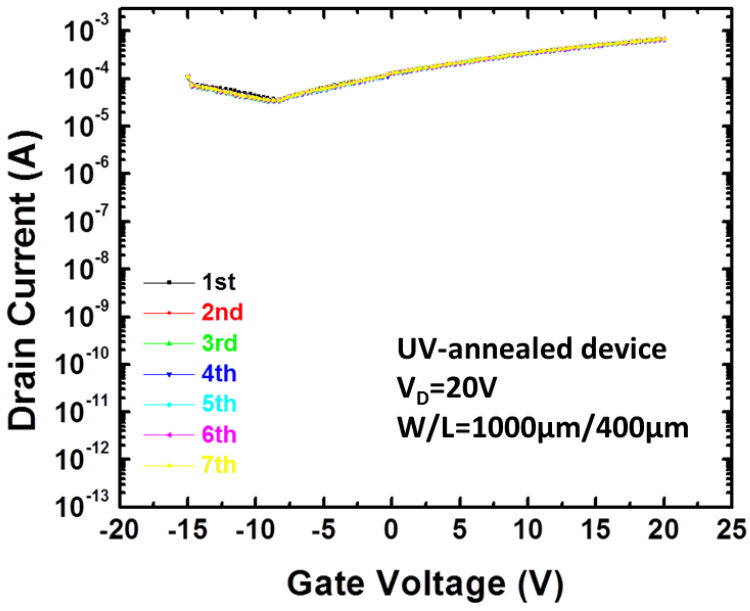


Fig. A.5 (a)

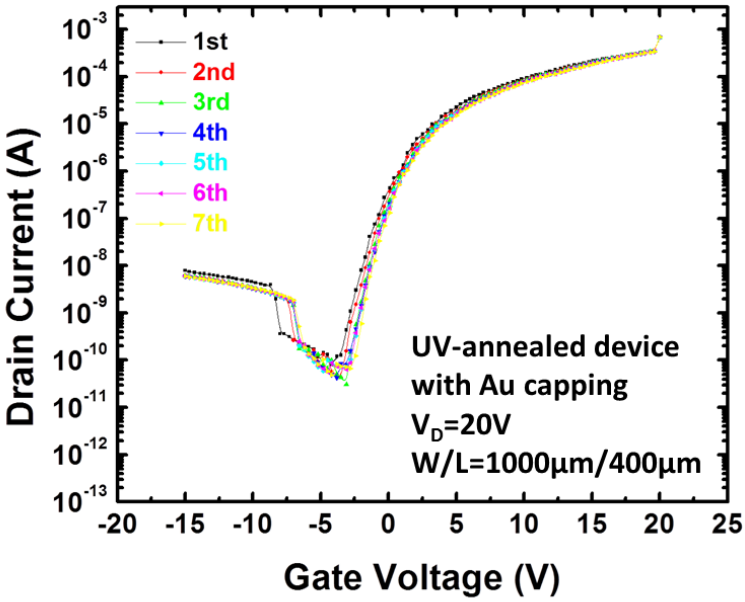


Fig. A.5 (b)

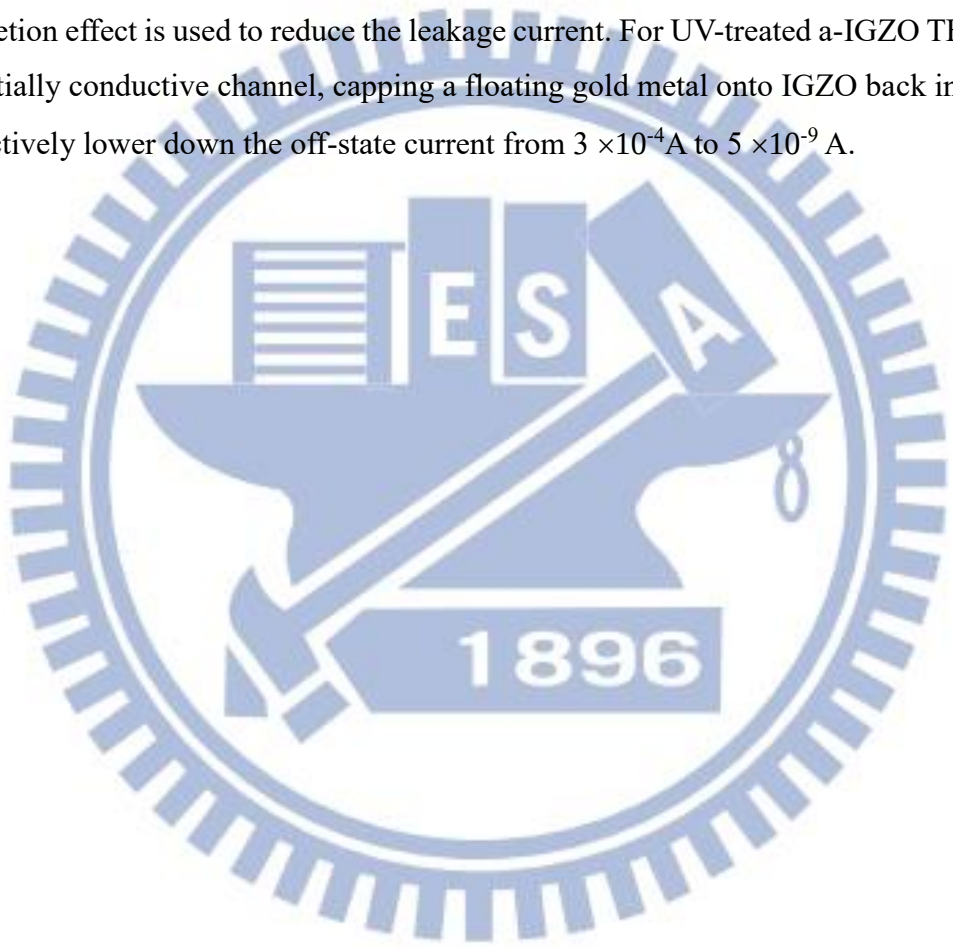
Figure A.4. Experimental transfer characteristics of (a) UV-annealed a-IGZO TFT and (b) UV-annealed a-IGZO TFT after Au capping. Continuous 7-times measurements were shown.

Finally, experimentally, we demonstrate a leakage reduction effect by utilizing the electron depletion due to gold capping. The transfer characteristics of the initial a-IGZO TFT after UV annealing are shown in Fig. A.5(a). High concentration of oxygen deficiency is produced by UV exposure. Hence, the carrier concentration in IGZO film is enlarged to generate a large leakage current (3×10^{-4}A) between source and drain electrodes. After capping gold metal onto the central region of the back interface, transfer characteristics of Au-capped IGZO TFT are shown in Fig. A.5(b). Good transistor performance can be obtained and the leakage current is reduced to be 5×10^{-9} A. The extracted mobility, threshold voltage, subthreshold swing, and on/off current ratio are 15 cm^2/Vs, 1.4 V, 0.72 V/dec, and 5×10^6, respectively.

A.4 Conclusion

In this study, the 2-dimensional electron distribution of n-channel a-IGZO TFT

with a floating metal-semiconductor (MS) back contact is demonstrated by using Silvaco TCAD simulator. The simulated results verify that capping metals with various work functions onto IGZO back interface leads to a significant influence on electron distribution. Particularly, when capping a floating metal with high work function, electrons inside IGZO film are obviously depleted. The electron depletion effect can also affect the electron concentration in front channel region and hence lead to a shift of threshold voltage. Increasing channel length and reducing IGZO film thickness effectively enhance the electron depletion effect. Finally, experimentally, the electron depletion effect is used to reduce the leakage current. For UV-treated a-IGZO TFT with a initially conductive channel, capping a floating gold metal onto IGZO back interface effectively lower down the off-state current from 3×10^{-4}A to 5×10^{-9} A.



Appendix B. TC of Poly-Silicon TFT and its Application on Voltage Reference circuit

The temperature coefficient (TC) of n-type polycrystalline silicon thin-film transistors (poly-Si TFTs) is investigated in this work. The relationship between TC and the activation energy is observed and explained. From the experimental results, it is also found that TC is not sensitive to the deviation of the laser crystallization energy. On the contrary, channel width can effectively modulate the TC of TFTs. By using the diode-connected poly-Si TFTs with different channel widths, the first voltage reference circuit with temperature compensation for precise analog circuit design on glass substrate is proposed and realized. From the experimental results in a LTPS process, the output voltage of voltage reference circuit with temperature compensation exhibits a very low TC of 195 ppm/°C, between 25°C and 125°C. The proposed voltage reference circuit with temperature compensation can be applied to design precise analog circuits for System-on-Panel (SoP) or System-on-Glass (SoG) applications, which enables the analog circuits to be integrated in the active matrix LCD (AMLCD) panels.

B.1 Introduction

Polycrystalline silicon thin-film transistors (Poly-Si TFTs) with the increased carrier mobility have been widely used in active-matrix liquid-crystal displays (AMLCDs), which integrated the corresponding peripheral driving circuitry on panel [1], [2]. The CPU, memory, timing controller, digital-to-analog converter (DAC), and driving buffer had been implemented on glass substrate with the low-temperature polycrystalline silicon (LTPS) TFT process. LTPS AMLCDs integrated with driver and control circuits on glass substrate have been practically applied in portable systems, such as mobile phone, digital camera, and notebook, etc. [3], [4]. However, even with the advanced crystallization technologies such as the excimer laser annealing (ELA) or the sequential laser solidification (SLS) process, it is still observed that the carrier

transport in poly-Si TFTs is dominated by the thermionic emission effect [5], [6]. The energy barriers at grain boundaries confine the carrier movement, reduce the field-effect mobility, and make the device characteristics to be strongly dependent on temperature. As a result, to reduce the impact of temperature variation on the performance of analog circuits in the LTPS process is a very important design challenge.

The voltage reference circuit with temperature compensation is the key design in analog circuits to provide a stable voltage reference with low sensitivity to temperature and supply voltage [7]-[10]. The voltage reference circuit with temperature compensation has been widely used in analog and digital circuits, such as DRAM, flash memory, analog-to-digital converter (ADC), and so on. Though the Voltage reference circuit with temperature compensation is important to provide a stable output voltage, the LTPS Voltage reference circuit with temperature compensation on glass substrate was never reported in the past. The conventional CMOS voltage reference circuit with temperature compensation incorporated with BJTs or p-n junction diodes is a great challenge for LTPS process, since the characteristics of the poly-Si BJTs or the poly-Si p-n junction diodes are still unknown or lack of investigation. On the contrary, the characteristics of LTPS TFT devices are strongly dependent on temperature even if the devices are operated in saturation region [5], [6]. Therefore, the LTPS voltage reference circuit with temperature compensation can be realized by using only LTPS TFT devices on glass substrate.

In this paper, the temperature coefficient (TC) of LTPS TFT devices is first analyzed. The relationship between the activation energy and the TC is investigated. Then, the influences from the laser energy density of the ELA process on the TC of TFT devices are discussed. Followed by the investigation on the channel width effect to the TC, a combination of a narrow-width device and a wide-width device is proposed to generate a positive TC by an appropriate circuit arrangement. The positive TC can be used to compensate the negative TC of TFT devices to achieve the design of a stable output voltage with low sensitivity to the temperature. Finally, this concept has been demonstrated with the first on-glass voltage reference circuit with temperature compensation in LTPS process. Without additional laser trimming after fabrication, the new proposed bandgap voltage reference circuit has been verified on the glass substrate with the output voltage of 6.87 V at room temperature. The temperature coefficient of voltage reference circuit with temperature compensation output voltage is 195 ppm/°C

under VDD power supply of 10 V when the temperature varies from 25 °C to 125 °C.

B.2 Traditional Voltage Reference Circuit

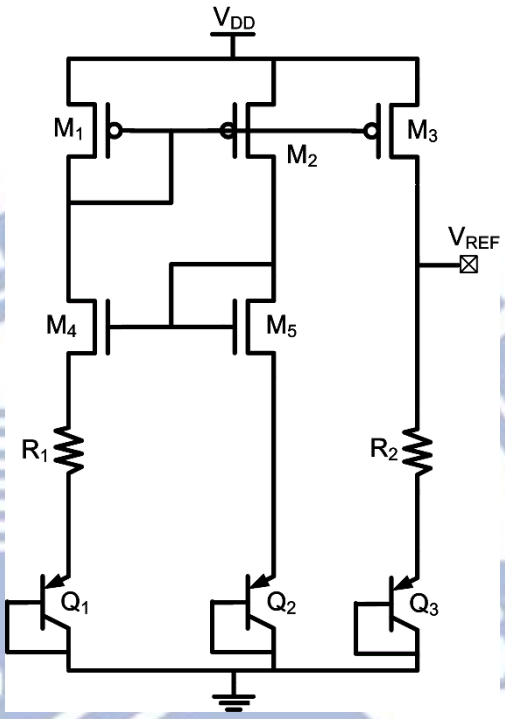


Fig. B.1 The traditional voltage reference circuit with temperature compensation in CMOS technology.

A traditional implementation of voltage reference circuit with temperature compensation in CMOS technology is shown in Fig. B.1 [11]. In this circuit, the output voltage (V_{REF}) is the sum of a base-emitter voltage (V_{EB}) of BJT Q3 and the voltage drop across the upper resistor R2. The BJTs (Q1, Q2, and Q3) are typically implemented by the diode-connected vertical parasitic PNP bipolar junction transistors in CMOS process with the current proportional to exp(V_{EB}/V_T), where V_T ($=kT/q$) is the thermal voltage. Under constant current bias, V_{EB} is strongly dependent on V_T as well as temperature. The current mirror is designed to bias Q_1, Q_2, and Q_3 with identical current. Then, the voltage drop on the resistor R_1 can be expressed by

$$V_{R1} = V_T \ln(\frac{A_1}{A_2}), \tag{B.1}$$

where A_1 and A_2 are the emitter areas of Q_1 and Q_2. It is noted that V_{R1} exhibits a positive temperature coefficient when A_1 is larger than A_2. Besides, since the current flows through R_1 is equal to the current flows through R_2, the voltage drop on the resistor R_2 can be expressed by

$$V_{R2} = \frac{R_2}{R_1} V_T \ln(\frac{A_1}{A_2}). \tag{B.2}$$

Hence, the output voltage of the traditional voltage reference circuit with temperature compensation can be written as

$$V_{REF} = V_{EB3} + \frac{R_2}{R_1} V_T \ln(\frac{A_1}{A_2}). \tag{B.3}$$

The second item in Eq. (3) is proportional to the absolute temperature (PTAT), which is used to compensate the negative temperature coefficient of V_{EB3}. In general, the PTAT voltage comes from the thermal voltage V_T with a temperature coefficient about + 0.085 mV/°C in CMOS technology, which is quite smaller than that of V_{EB}. After multiplying the PTAT voltage with an appropriate factor (R_2/R_1) and summing with V_{EB}, the voltage reference circuit with temperature compensation would result in very low sensitivity to temperature. Consequently, if a proper ratio of resistors is kept, the output voltage (V_{REF}) with very low sensitivity to temperature can be obtained.

From the analysis on traditional voltage reference circuit with temperature compensation, it is known that the realization of voltage reference circuit with temperature compensation in CMOS process strongly depends on the temperature coefficient of BJTs (Q_1, Q_2, and Q_3). In other words, the exponential term exp(V_{EB}/V_T) in the I-V relationship of BJTs makes it possible to obtain a PTAT voltage from the voltage difference of a large-area BJT and a small-area BJT. The voltage across MOSFETs was not sensitive to temperature, so MOSFETs were seldom used in voltage reference circuit with temperature compensation directly. A pure MOSFET voltage reference circuit with temperature compensation was realized only when the MOSFETs are biased in subthreshold region [9]. Unlike MOSFETs, the characteristics of LTPS TFTs are strongly dependent on temperature even when the devices are operated in above threshold region [5], [6]. Therefore, it is expected that the voltage reference circuit with temperature compensation can be realized by using only LTPS TFT devices on glass substrate.

B.3 TFT Fabrication

For device analysis, the typical top-gate, coplanar self-aligned n-type poly-Si TFTs with 1.25-μm-length LDD structure in a 3-μm LTPS process were used in this study. First, the buffer layer was deposited on the glass substrate. Then, the undoped 50-nm-thick a-Si layer was deposited and crystallized by XeCl excimer laser with a laser energy density varied from 340 mJ/ cm^2 to 420 mJ/ cm^2. The recrystallized poly-Si films were patterned into the active islands. Afterward, the 60-nm-thick oxide layer was deposited as the gate insulator. Then, the 200-nm-thick Molybdenum was deposited and patterned as the gate electrode. The n^- doping was performed self-aligned to the gate electrode. The n^+ source/drain region was defined by an additional mask. The dopants were activated by thermal process. After the deposition of nitride passivation and the formation of contact holes, the 550-nm-thick Titanium/Aluminum/Titanium tri-layer metal was deposited and patterned as the metal pads. The channel lengths of TFT devices are all kept as 6 μm while the channel widths are designed from 30 μm to 6 μm in the on-glass voltage reference circuit with temperature compensation.

B.4 Measured Results and Temperature Model

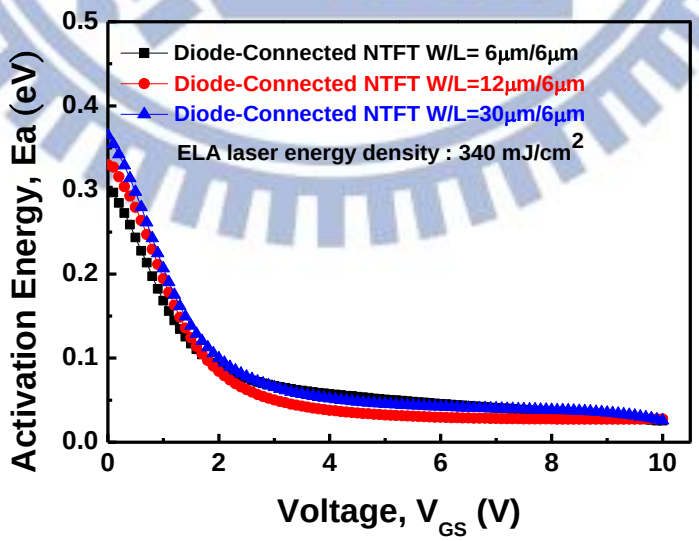
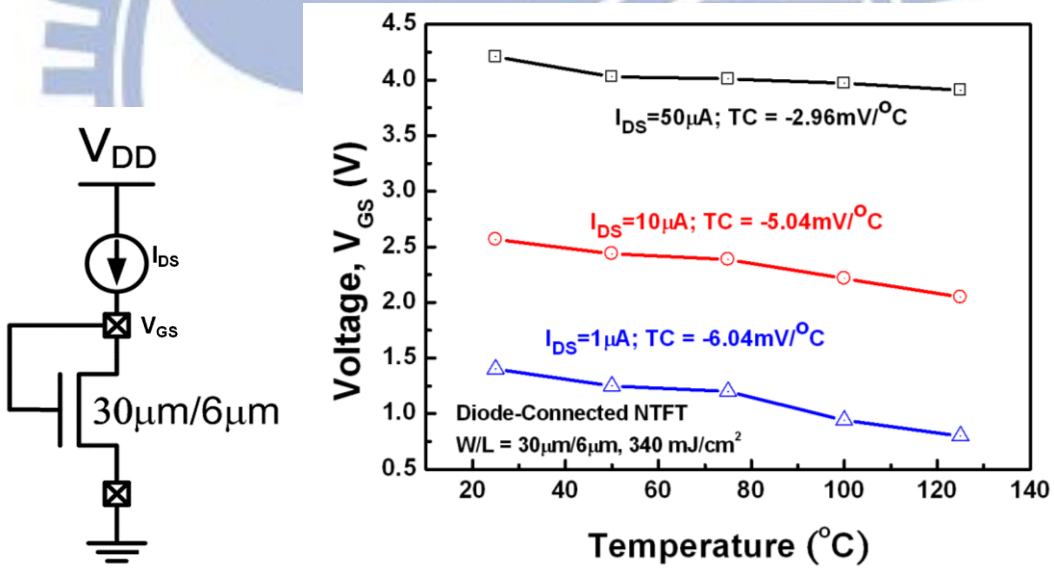


Fig. 2 The activation energy as a function of V_{GS} for diode-connected NTFTs with W/L as 6μm/6μm, 12μm/6μm, and 30μm/6μm.

Since the temperature response of the LTPS devices is mostly influenced by the thermionic emission effect with an activation energy associated with the grain boundary barrier height, the relationship between the activation energy and the temperature coefficient is first investigated in this paper. As shown in Fig. B.2, the activation energy (E_a) extracted from the Arrhenius plot of the drain current is depicted as a function of the gate bias (V_{GS}). The drain bias (V_{DS}) is equal to V_{GS} for the diode-connected TFT devices. Devices with three different channel widths are measured in Fig. 2. Devices are fabricated in the same run with identical crystallization laser energy density. It is found that, similar to the three-terminal LTPS devices, E_a of the diode-connected devices is strongly dependent on V_{GS}. Under small gate bias, E_a is high. When V_{GS} is increased, E_a decreases drastically. It is well known that, for the 3-terminal LTPS TFTs, the measured activation energy represents the grain boundary energy barrier of the poly-Si film which is sensitive to the poly-Si thin film properties [5], [6]. Channel width has no influence on the thin film properties, so devices with different channel widths exhibit similar E_a characteristics as those measured in Fig. B.2.



(a) (b)

Fig. 3 (a) The setup to measure V_{GS} under the bias of I_{DS}. (b) The relationship between V_{GS} and temperature under three different current levels (1 μA, 10 μA, and 50 μA).

Then, to extract the temperature coefficient, the setup to measure V_{GS} of the fabricated devices under the bias of three different current levels (1 μA, 10 μA, and 50 μA) is shown in Fig. B.3(a). The measured V_{GS} of the fabricated device with channel

width of 30 μm is plotted as a function of temperature in Fig. B.3(b). As shown in Fig. B.3(b), V_{GS} is decreased while the temperature increases. Almost linear relationship between V_{GS} and temperature can be observed in Fig. B.3(b), the slope represents the temperature coefficient (TC). For the diode-connected NTFT with channel width of 30 μm under different current levels, the TC is negative. Additionally, the magnitude of TC decreases when the bias current is increased. When the bias current increases from 1 μA, 10 μA, to 50 μA, the TC varies from -6.04 mV/°C, -5.04 mV/°C, to -2.96 mV/°C. It is noted that for one identical diode-connected device, the increase of bias current gives rise to the increase of operation voltage. As a result, the larger bias current makes the devices operated under larger V_{GS} with smaller E_a and smaller magnitude of TC. This result clearly demonstrates the relationship between the activation energy and the TC. Furthermore, the aforementioned discussion can be expressed by the following derivation.

For LTPS TFTs, the drain current I_{DS} of devices operated in saturation region can be expressed as [12], [13]

$$I_{DS} = \frac{W}{2L}\mu_0 C_{ox}(V_{GS} - V_{TH})^2 \exp(-\frac{V_B}{V_T}), \tag{B.4}$$

where μ_0 is the carrier mobility within the grain, L denotes the effective channel length, W is the effective channel width, C_{ox} is the gate oxide capacitance per unit area, V_{TH} is the threshold voltage of TFT device, which V_{GS} is the gate-to-source voltage of TFT device. V_B is the potential barrier at grain boundaries which is associated with the crystallization quality of the poly-Si film. When the activation energy is extracted from the Arrhenius plot of the drain current, E_a is equal to qV_B. Under small V_{GS}, V_B is large. When the V_{GS} increases, V_B decreases rapidly. When the device in circuit is operated under small V_{GS}, the drain current I_{DS} of device is dominated by the exponential term and can be simplified by

$$I_{DS} = W\alpha \exp(-\frac{V_B}{V_T}), \tag{B.5}$$

where α is only weakly dependent on V_{GS} but it is insensitive to temperature. Then, the equation of V_B can be derived as

$$V_B = V_T \ln(\frac{W\alpha}{I_{DS}}) = \frac{kT}{q}\ln(\frac{W\alpha}{I_{DS}}). \tag{B.6}$$

When there is a variation of temperature ΔT, the corresponding variation on V_B is

$$\Delta V_B = \frac{k\Delta T}{q} \ln(\frac{W\alpha}{I_{DS}}). \quad \text{(B.7)}$$

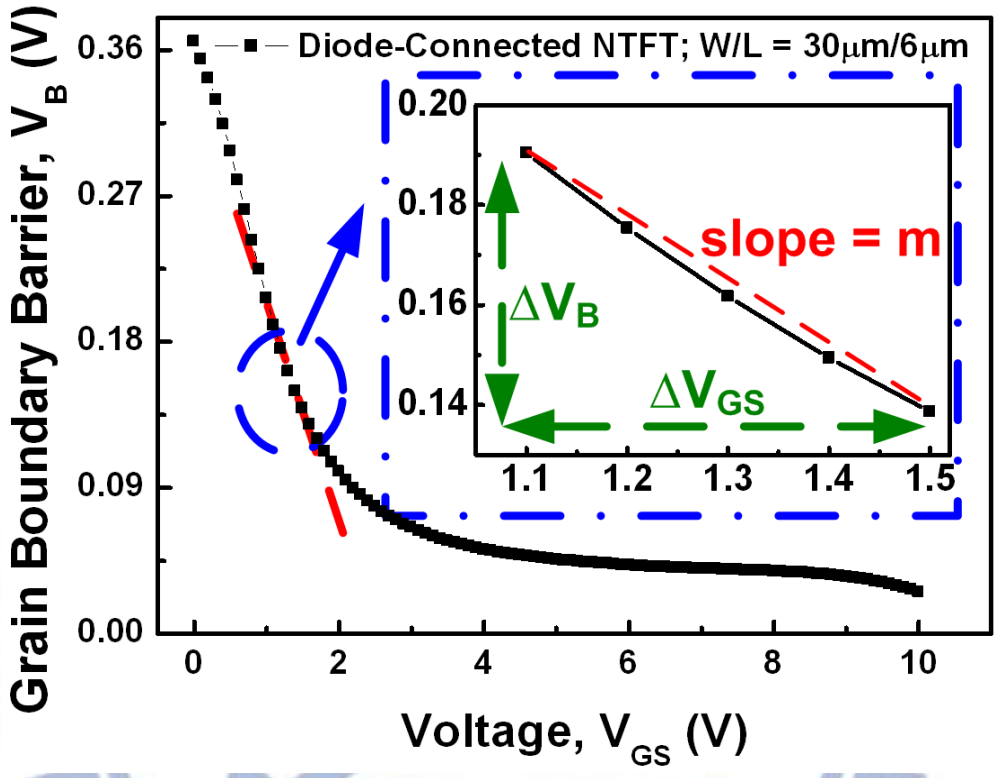


Fig. B.4 The activation energy as a function of V_{GS} for diode-connected NTFTs with poly-Si film crystallized by laser energy density as 340, 400, and 420 mJ/cm^2. (b) The relationship between V_{GS} and temperature under identical I_{DS} as 10 μA. Devices W/L are 6μm/6μm.

Fig. B.4 shows the measured dependence between potential barrier of grain boundary V_B and gate-to-source voltage V_{GS} of diode-connected NTFT with device dimension W/L of 30μm/6μm, whereas the laser energy density is kept at 340 mJ/cm^2. As shown in Fig. B.4, the variation of V_B is related to the variation of V_{GS}. Assume that the variation of V_{GS} (ΔV_{GS}) is very small, and a negative linear approximation can be given between ΔV_B and ΔV_{GS} as

$$\Delta V_{GS} = -\frac{1}{m}\Delta V_B = -\frac{k\Delta T}{mq}\ln(\frac{W\alpha}{I_{DS}}), \tag{B.8}$$

where m is the absolute slope of the linear approximation between ΔV_B and ΔV_{GS} in Fig. 4. Finally, the temperature coefficient (TC) can be found as

$$TC = \frac{\Delta V_{GS}}{\Delta T} = -\frac{k}{mq}\ln(\frac{W\alpha}{I_{DS}}) = -\frac{\Delta V_B}{m\Delta T}. \tag{B.9}$$

Even though the increase of V_B accompanies with the increase of m, the variation of V_B can be more significant than that of m under a proper design.

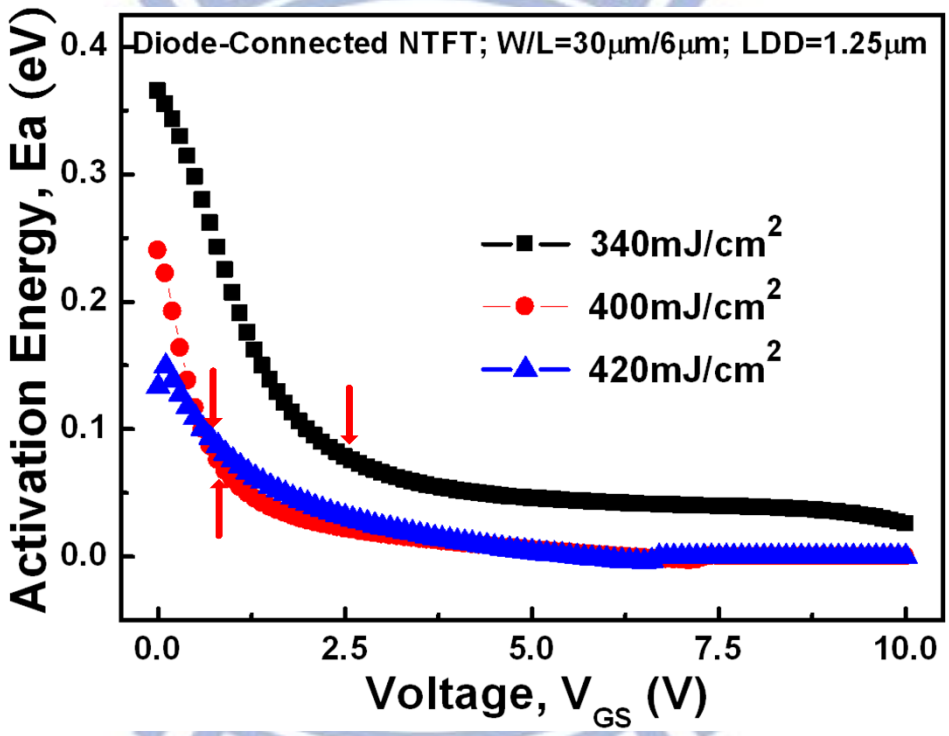


Fig. B.5(a)

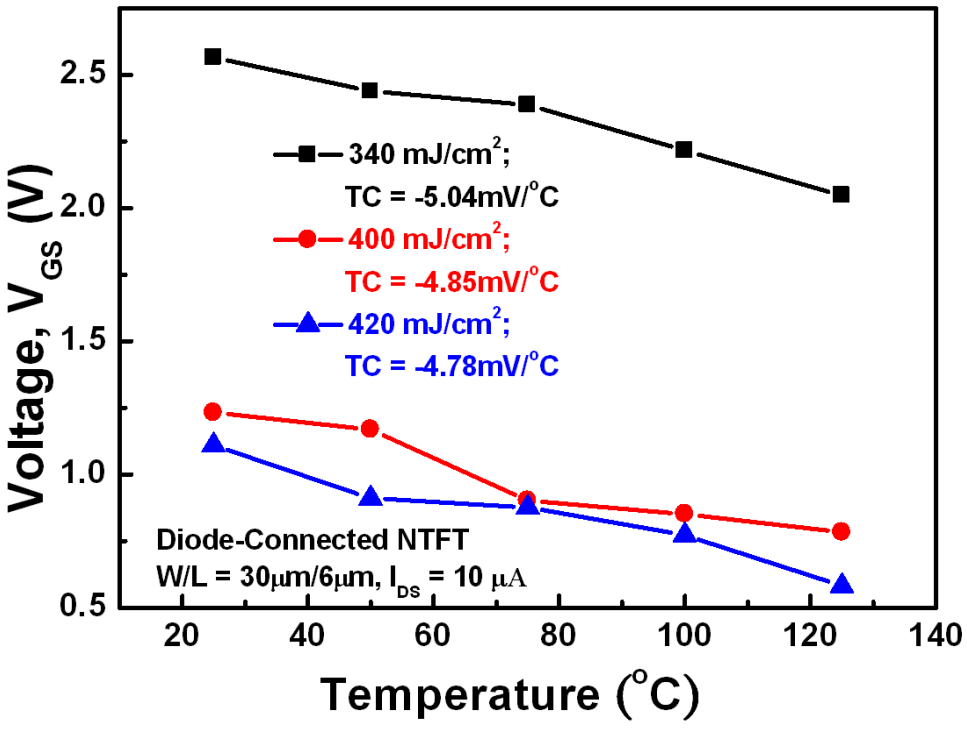


Fig. 5 (a) The activation energy as a function of V_{GS} for diode-connected NTFTs with poly-Si film crystallized by laser energy density as 340, 400, and 420 mJ/cm^2. (b) The relationship between V_{GS} and temperature under identical I_{DS} as 10 μA. Devices W/L are 6μm/6μm.

The activation energy, as well as the grain boundary barrier, should be related to the grain structure and the grain boundary property. It is therefore presumed that the laser energy density of the ELA process influences the grain structure and affects the TC of the devices. Fig. B.5(a) shows the activation energy of the diode-connected devices with the poly-Si film crystallized under different laser energies (340, 400, and 420 mJ/cm^2). The channel width of the TFT device studied in Fig. B.5(a) is 30 μm. The activation energy is found to be reduced with increasing laser energy density. As a result, the TC of the devices with higher laser energy density is also smaller than those with lower laser energy density as shown in Fig. B.5(b). However, the influence of laser energy density on the TC is not significant. When the laser energy density changes ±10%, the TC changes only about ±2.75%. The reason can be explained by identifying the biasing points of three devices in Fig. B.5(a). The operation voltages of three devices under the bias of 10-μA I_{DS} are indicated by the arrow symbols in Fig. B.5(a). It is found that the activation energies of the three biasing points are similar. This makes

the TC insensitive to the deviation of the laser energy density in the ELA process. Similar results can be also observed for the devices with small channel width of 6 μm in Fig. B.6(a) and Fig. B.6(b), where the laser energies for poly-Si film crystallized are also 340, 400, and 420 mJ/cm^2.

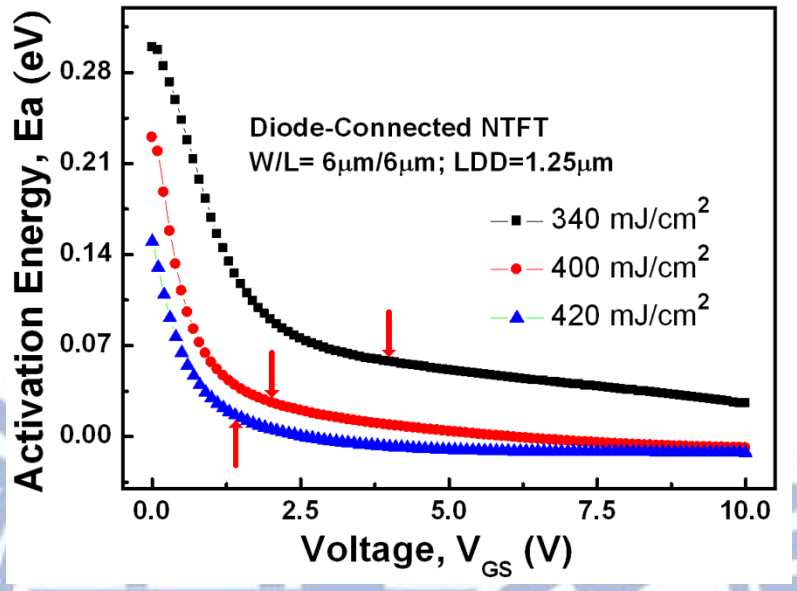


Fig. B.6(a)

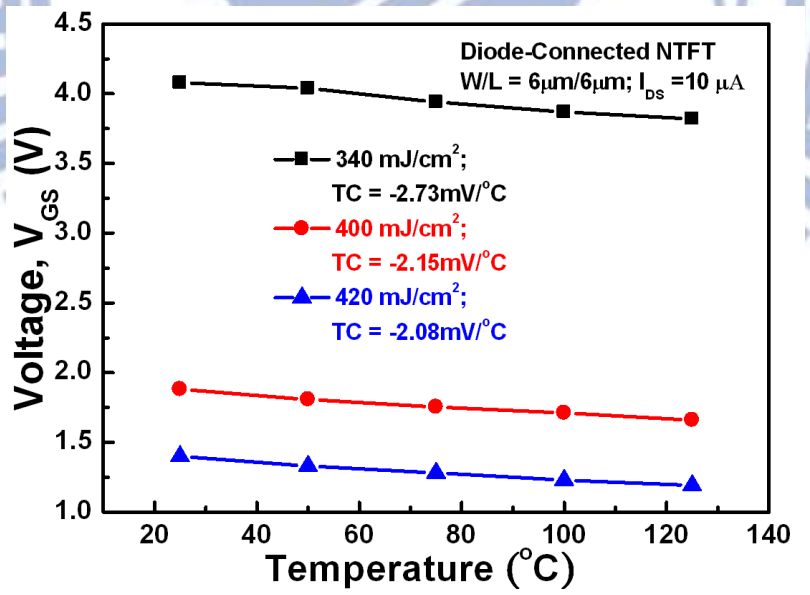


Fig. 6(a)

Fig. 6(b) The activation energy as a function of V_{GS} for diode-connected NTFTs with poly-Si film crystallized by laser energy density as 340, 400, and 420 mJ/cm^2. (b) The relationship between V_{GS} and temperature under identical I_{DS} as 10 μA. Devices W/L are 6μm/6μm.

The influence of the channel width on the TC, however, is found to be significant. When the diode-connected devices are biased under a constant current of 10 μA, V_{GS} of TFT devices with channel widths of 6 μm and 30 μm are plotted as a function of temperature in Fig. B.7, whereas the laser energy density is kept at 400 mJ/cm^2. Obviously, the wide-channel-width device exhibits more negative TC than the narrow-channel-width device. From Fig. B.2, it has been observed that the channel width has only little influence on the device activation energy. However, when all the devices are biased by identical current source, the wide-channel-width devices are operated under small V_{GS} and the narrow-channel-width devices are operated under large V_{GS}. When V_{GS} is reduced, the activation energy is drastically enlarged as shown in Fig. B.2. As a result, the absolute value of the TC is significantly enlarged by increasing the channel width. Such a phenomenon can be also explained by Eq. (9).

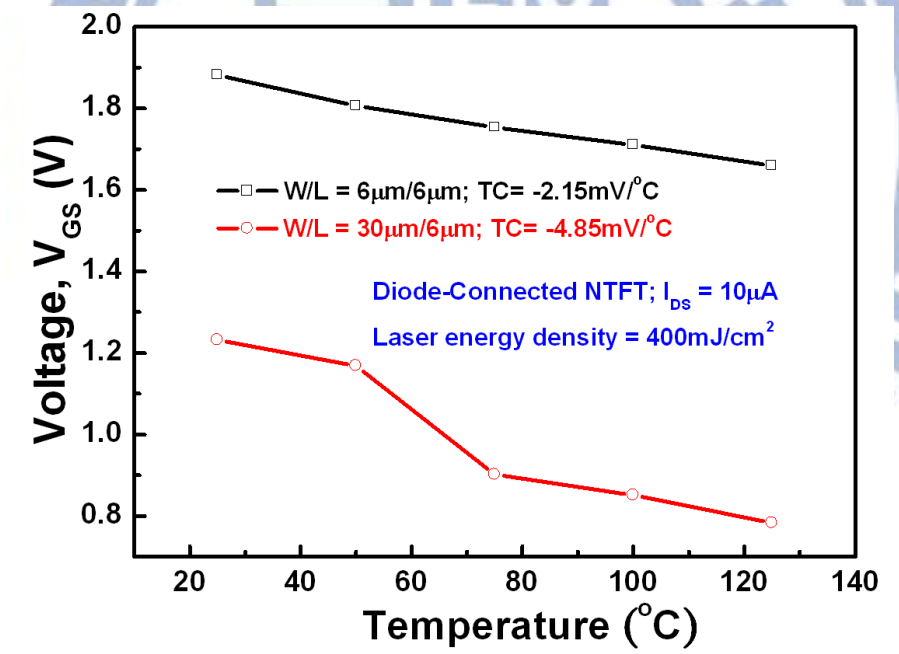


Fig. B.7 The relationship between V_{GS} and temperature of devices with different channel widths under identical I_{DS} of 10 μA.

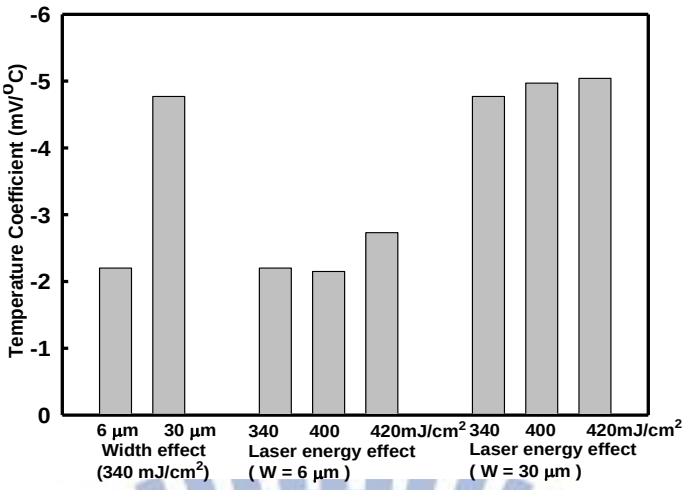


Fig. B.8 The TC of the diode-connected NTFT devices biased under a 10-μA current source to investigate the influences of channel width and crystallization laser energy on the TC of the diode-connected NTFT devices.

Finally, the TC of the diode-connected NTFT devices biased under a 10-μA current are plotted in Fig. 8. The influences of channel width and crystallization laser energy on the TC of the diode-connected NTFT devices are compared. It can be concluded that the influence of ELA laser energy density or the poly-Si thin film property on the TC is relatively small. This makes the voltage reference circuit with temperature compensation not sensitive to the deviation of the laser annealing process in the LTPS technology. On the contrary, changing the device channel width can effectively change the TC of the diode-connected device. This enables the designer to modulate the TC of the diode-connected devices easily.

B.5 Application on Voltage Reference Circuit

The difference of TCs between the wide-channel-width device and the narrow-channel-width device is very useful if a positive TC can be extracted from the V_{GS} of the wide-channel-width device to the V_{GS} of the narrow-channel-width device. This positive TC can be used to compensate the negative TC in the V_{GS} of TFT devices.

A. Implementation

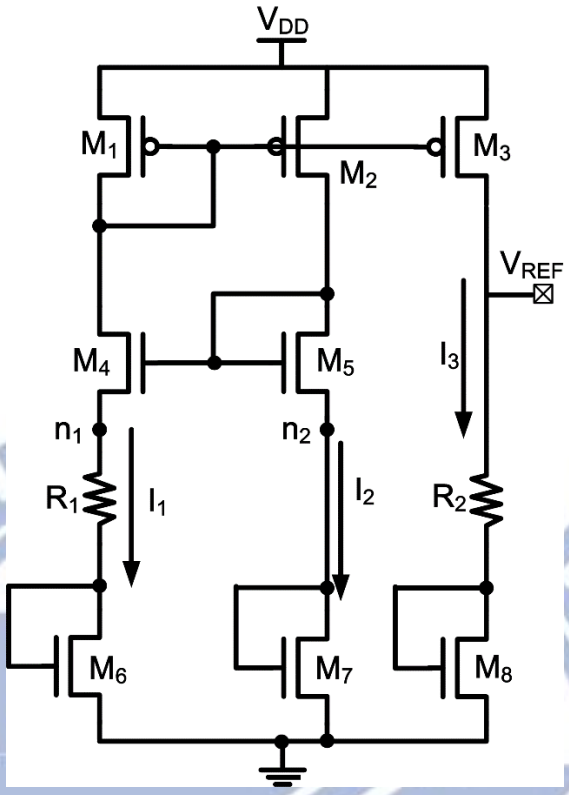


Fig. B.9 The implementation of the new proposed voltage reference circuit with temperature compensation in a 3-μm LTPS process.

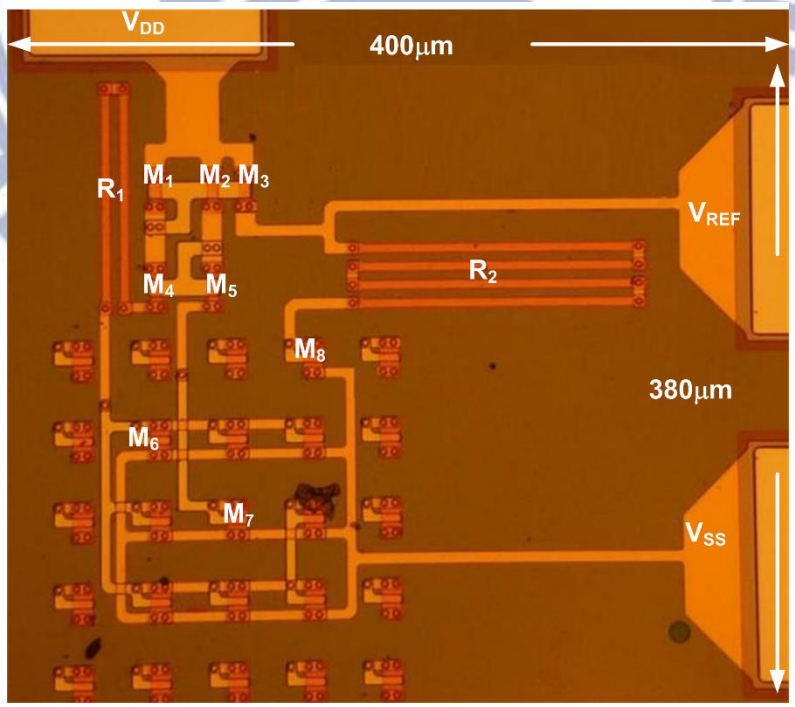


Fig. 10 The on-glass circuit photo of the new proposed voltage reference circuit with temperature compensation fabricated in a 3-μm LTPS process.

The new proposed voltage reference circuit with temperature compensation designed and fabricated by a 3-μm LTPS technology is shown in Fig. B.9. In this circuit, the TFTs M_1, M_2, M_3, M_4, and M_5 are biased in saturation region. The diode-connected NTFT devices M_6, M_7, and M_8, which replace the diode-connected BJTs in traditional CMOS voltage reference circuit with temperature compensation (Fig. B.1) [11], are also biased in saturation region. The nodes n_1 and n_2 are designed to have equal potential by the current mirror circuit.

The channel width of M_6 (W_6) is larger than the channel width of M_7 (W_7), so the TC of M_6 is more negative than the TC of M_7. The voltage drop on the resistor R_1 (V_{R1}) therefore exhibits a positive TC. If the dependence of m on V_{GS} is neglected, the variation of V_{R1} (ΔV_{R1}) as a function of ΔT can be expressed as

$$\Delta V_{R1} = \frac{k\Delta T}{mq}\ln(\frac{W_6}{W_7}) = \frac{k\Delta T}{mq}\ln N. \tag{B.10}$$

Obviously, ΔV_{R1} is proportional to the absolute temperature (PTAT). Hence, a PTAT loop is formed by M_6, M_7, and R_1. The PTAT current variation ΔI_1 can be written as

$$\Delta I_1 = \frac{k\Delta T}{mqR_1}\ln N, \tag{B.11}$$

where N ($=W_6/W_7$) is the channel width ratio of M_6 and M_7. The current mirror, which is composed of M_1, M_2, and M_3, imposes equal currents in these three branches I_1, I_2, and I_3 of the circuit. The output voltage (V_{REF}) is the sum of a gate-source voltage of TFT M_8 (V_{GS8}) and the voltage drop across the upper resistor (V_{R2}). Therefore, the output voltage variation (ΔV_{REF}) of the new proposed voltage reference circuit with temperature compensation can be expressed as

$$\Delta V_{REF} = \Delta I_3 R_2 + \Delta V_{GS8} = \frac{R_2}{R_1}\frac{k\Delta T}{mq}\ln N + \Delta V_{GS8}, \tag{B.12}$$

where R_1 and R_2 are the resistances shown in Fig. 9. The first item in Eq. (B.12) with positive TC is proportional to the absolute temperature (PTAT), which is used to compensate the negative temperature coefficient of ΔV_{GS8}. After multiplying the PTAT voltage with an appropriate factor (proper ratio of resistors) and summing with ΔV_{GS8}, the output voltage of voltage reference circuit with temperature compensation would

result in very low sensitivity to temperature.

The proposed voltage reference circuit with temperature compensation has been fabricated in a 3-μm LTPS technology. Figure 10 shows the chip photo of the new proposed voltage reference circuit with temperature compensation fabricated on glass substrate. The chip size of the proposed voltage reference circuit with temperature compensation is 400 × 380 μm^2. The resistance R_1 and R_2 implemented by the poly resistance are also included into the layout.

B. Measurement Results

The threshold voltage of TFT devices in a 3-μm LTPS technology is $V_{thn} \approx V_{thp} \approx$ 1.25 V at 25 °C. The total gate area of M_6 is 480 μm^2 and that of M_7 is 80 μm^2 in this fabrication. The resistors in this chip, formed by poly resistors, have minimum process variation to improve the accuracy of resistance ratio. The power supply voltage V_{DD} is set to 10 V, and the total operating current is 8.97 μA. The measured results of the output voltage V_{REF} from 25 to 125℃ are shown in Fig. B.11, where the R2 is drawn with different values in the test chips. As R_2 is equal to 500 kΩ, the measured temperature coefficient of the fabricated voltage reference circuit with temperature compensation on glass substrate is around 195 ppm/°C without laser trimming after fabrication, whereas the output voltage (V_{REF}) is kept at 6.87 V.

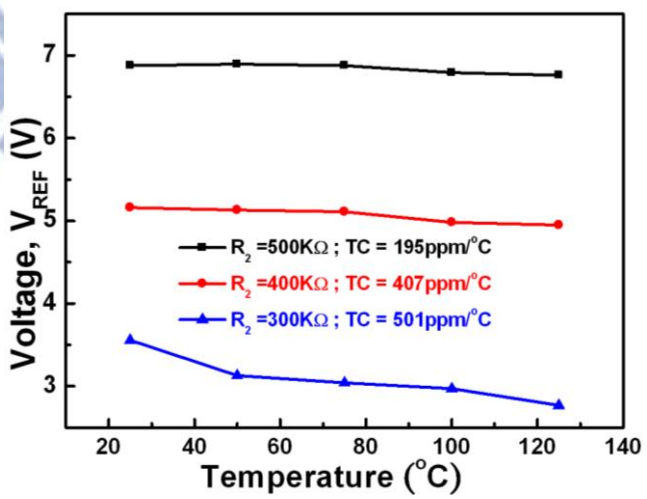


Fig. B.11 The measured output voltage V_{REF} of the fabricated voltage reference circuit with temperature compensation under different resistance of R_2 without laser trimming after fabrication.

B.6 Conclusion

The temperature coefficient of TFT devices in LTPS technology is strongly dependent on the activation energy of the devices. With a suitable control, higher activation energy gives rise to higher absolute value of the temperature coefficient. The influence of the laser energy density in ELA process on the temperature coefficient of the devices is not significant. On the other hand, the bias current level and the channel width have a strong impact on the device temperature coefficient. As a result, the temperature coefficient of devices can be controlled by regulating the channel width of the devices. With an appropriate circuit design, a positive temperature coefficient can be generated by using the voltage drop between devices those have different temperature coefficients (different channel widths). Then, the positive temperature coefficient can be used to compensate the negative temperature coefficient from the devices. The first voltage reference circuit with temperature compensation has been successfully verified in a 3-μm LTPS process. The measured reference output voltage is 6.87 V with a temperature coefficient of 195 ppm/°C. The proposed voltage reference circuit with temperature compensation consumes an operating current of only 8.97 μA under the supply voltage of 10 V on glass substrate. This new voltage reference circuit with temperature compensation can be used to realize precise analog circuits in LTPS process for System-on-Glass (SoG) applications.

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