國立交通大學

電機資訊國際學位學程

博士論文

高壓積體電路 BCD 製程之陣列式功率電晶體元件設計及可靠性分析

Device Design and Reliability Analysis of Large-Array Power Field-Effect-Transistors in BCD Process

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摘要

現今矽(Si)半導體是功率半導體工業主要來源之一，其製造技術經過數十年的發展，能以低成本提供大量的成熟、可靠和穩健的技術。功率半導體元件的進步在很大程度上是基於低壓應用製程開發的技術和工藝，然後進行縮放和優化，以使元件能夠承受更高的電壓和電流，並滿足更高額定功率的要求。然而，研究和製造的主要目標是整合和完善現有半導體元件的特徵和特性。目前，已有超過 20 種功率場效應電晶體(FET)，其中最常見的兩種是接面場效電晶體(JFET)和金屬氧化物半導體場效應電晶體（MOSFET）。而 JFET 和 MOSFET 的工作原理和電氣特性非常相似，且具有輸入阻抗高、製作簡單、操作簡單、雜訊小、開關速度快等各種優點，使得這些功率元件可廣泛應用於不同的應用中。然而，尺寸縮小化以及高性能的應用趨勢與元件可靠性相互矛盾。目前，功率元件開發趨勢主要專注於提高額定功率、提高可操作區域、增強穩健性、更好的可控性、更好的自我保護能力、以及在正常和故障條件下的可靠行為等議題。

第 2 章描述如何使用在 0.15μm BCD 工藝中可選擇的摻雜層來研究安全工作區(SOA)和 ESD 自我保護能力的改進。相較於原始元件(稱為 NCH)，加入此摻雜層的改良結構(稱為 NCH_ZDI)具有顯著的改進，且不影響擊穿電壓、閾值電壓和導通電阻等基本參數。此外，大型陣列元件(LAD)結構的多指狀佈局與體電位的佈局考量對電性安全工作區(E-SOA)，觸發電壓(Vt1)和二次擊穿電流(It2)的影響亦在第 2 章中描述。

第 3 章針對第 2 章中介紹的改良結構進行非箝位感應開關(UIS)測試，並分析其對能量承受度的改善。與原始元件相比，修改後的元件在較高的雪崩單脈衝(EAS)能

量和最大雪崩電流(IAV)性能皆有顯著的改善。另外，在針對閘極電荷的分析中亦可證實在體電位區使用額外的植入後，其品質因數保持不受影響。

功率器件的相關能量負荷能力是影響元件設計及其可靠性的最主要問題之一。第4章檢查了電感和功率電晶體之間用於非箝位感應開關測試的能量轉換模型。根據實驗結果，在通道導通期間存儲在電感中的能量可以消散在通道關閉後的功率電晶體。故我們提出了一個新的理論模型來描述功率電晶體在UIS測試中的電學和熱學行為，並在第4章中用實驗結果進行了分析。提出的UIS能量模型與測量的數據呈現出良好的一致性。

現今已經有許多接面型場效電晶體可在CMOS和Bipolar-CMOS-DMOS(BCD)技術中實現，然而許多需要silicon-on-insulator (SOI)晶片或額外摻雜步驟的開發工藝都是專有的。本論文在第5章中提出一個基於現有標準CMOS和BCD工藝中之摻雜層所實現的新型JFET結構，是一個在具有p型ESD摻雜層的標準CMOS工藝中的水平式n型5V JFET元件，此JFET元件能夠通過佈局調整其夾止電壓 (V_P) 和零電壓汲極電流（I_{DS0}），而測量結果證實此JFET元件可以在同一晶片中容納不同的夾止電壓。此外，本論文還提出了一種30V垂直式n型JFET結構，為在0.25μmBCD工藝中實現具有低夾止電壓之JFET元件，其可以通過不同的p型摻雜層代替原始結構中的PFD層來調節夾止電壓，因此本JFET器件可以用作ON/OFF開關，用於控制負載的電源；當其尺寸通過合適的縮放，也可以用作ESD保護元件或自我保護元件。由於JFET中沒有二次崩潰電壓，故其安全工作區比較大，因此不需要過壓保護。

第六章總結了本論文的主要研究成果，並討論了基於提出的JFET結構的未來工作。通過這些功率半導體元件技術相關的新穎成果，本論文為半導體行業提供了先進的學術研究成果和實用設計及可靠性解決方案。本論文的相關工作已獲得專利，並在IEEE期刊上發表。

Device Design and Reliability Analysis of Large-Array Power Field-Effect-Transistors in BCD Process

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Abstract

At present, the power semiconductor industry is majorly served by silicon (Si) semiconductor material as Si device fabrication technology has evolved over the years to provide mature, reliable and robust technologies in huge volumes at remarkably low costs. The progress of power devices has been largely dependent on technologies and processes developed initially for lower power applications and then scaled and optimized to enable the components to withstand higher voltages and currents to meet the requirements of higher power ratings. However, the main objectives of research and manufacturing are to integrate and ameliorate the features and characteristics of the existing Si devices. There are more than 20 different kinds of power field-effect-transistor (FETs), but the two most likely became familiar are the junction field-effect-transistor (JFET), and the metal-oxide-semiconductor field-effect-transistor (MOSFET). JFETs and MOSFETs are quite similar in their operating principles and in their electrical characteristics. Wide variety of advantages such as simple fabrication, easy operations, high input impedance, less noisy, fast switching speed etc. makes these power FETs to be used popularly in different power applications. However, shrinking of the device size along with applications demanding higher performance contradicts with the device reliabilities

requirement of these devices. The major power FET device development trends have always focused on increasing the power ratings while at the same time research effort needs to be focused towards improving the overall device performance in terms of operating areas, increased robustness, better controllability with self-protection ability, and reliable behavior under normal and fault conditions.

Chapter 2 investigates the improvement of the safe-operating-area (SOA) and ESD self-protection ability by using an optional implantation layer for 5-V n-channel large array power MOSFET in a 0.15-μm BCD process. A remarkable improvement is noticed in modified structure (named as NCH_ZDI) with an optional implantation layer within the existing process in compare to the original device (named as NCH) without compromising the basic parameters like the breakdown voltage, threshold voltage, and ON-resistance. The impact of inserting body pick-ups into multi-finger layout of large array device (LAD) structure to the electrical SOA (E-SOA), trigger voltage (Vt1), and secondary breakdown current (It2) is also present in chapter 2.

In addition to the SOA and ESD self-protection ability of the modified structure presented in Chapter 2, one of the most needed dynamic parameters for large array structures, the unclamped inductive switching (UIS) test is performed to analyze the improvement in the energy handling capability of the modified device in compare to the original device in chapter 3. Significant improvement in the maximum avalanche current (I_{AV}) and enhanced performances of the energy in avalanche single pulse (EAS) is noticed in compare to the original device. In addition, gate charge is also compared and significant conclusion is drawn that figure-of-merit remain unaffected after using additional implantation at the body area.

The energy handling capability of the power devices is one of the most dominating issues for the designers that affect the device design and its reliability. The fundamental model of the energy transformation between the inductor and the power transistor for the

unclamped inductive switching test is inspected in chapter 4. Based on the experimental results, the energy stored in the inductor at the period of the channel turn-ON can be dissipated by the power transistor after the channel is turned OFF. A new theoretical model to well describe the electrical and thermal behaviors of the power transistor during the UIS test has been proposed and analyzed with the experimental silicon results in chapter 4. The proposed UIS energy model shows good agreement with measured silicon data.

Nowadays, there have been several attempts to implement junction field-effect-transistors in CMOS and bipolar-CMOS-DMOS (BCD) technologies. However, many of these developments either required silicon-on-insulator (SOI) wafers or extra implantation steps and the processes thus developed were all proprietary. In chapter 5, new low-voltage (LV) and high-voltage (HV) JFET structures are proposed in the standard 0.25-μm CMOS/BCD processes within existing mask layers. An optional P-type ESD implantation is used to realize 5-V JFET structure. The proposed LV JFET is useful for 5 V applications while HV JFET structure can tuned its breakdown voltage for 20 V to 40 V applications with small variation in PFD layer which is used to isolate NBL and HVNW. The proposed LV and HV JFETs enable to adjust its pinch-off voltage (V_P) and zero-bias drain current (I_{DS0}) via layout medications. Measurement results from proposed structures have verified that different pinch-off voltages can be accommodated in the same chip. The proposed JFET devices are suitable to use a robust over current protection and can be used as an ON/OFF switch for controlling electrical power to a load, also as ESD protection device or self-protected device when its size is suitable scaled.

Chapter 6 summarizes the main results of this dissertation, whether the future works based on proposed JFET structures are discussed as well. With these novel results in power FETs technologies, this dissertation provides both advanced academia research achievements and practical design and reliability solutions to semiconductor industries. The related works in this dissertation have been patented and published in IEEE journals.


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Publication List

(A) Referred Journal Papers:

1. **K. Nidhi**, M.-D. Ker, T. Lin, and J.-H. Lee, "Improving safe-operating-area of a 5-V n-channel large array MOSFET in a 0.15-μm BCD Process," *IEEE Transactions on Electron Devices*, vol. 65, no. 7, pp. 2948–2956, May 2018, doi: 10.1109/TED.2018.2838545.
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