國立交通大學

電子研究所

博 士 論 文

低寄生電容與高安全度之

靜電放電防護設計與應用

Low-Capacitance and High-Reliable ESD

Protection Designs in CMOS Technology

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摘要

隨著近年來通訊技術與積體電路製程的持續演進，無線與有線通訊裝置已經成為生活中不可或缺的重要設備。所有電子產品必須符合可靠度的規範，以便讓使用者用得安心，並提供該產品足夠的耐用年限。靜電放電(Electrostatic Discharge, ESD)是積體電路可靠度中最重要的一環，大多數電子產品的故障與損壞均與遭受靜電放電轟擊有關，因此所有電子產品的輸入輸出端口都需加入靜電放電防護電路，至少需通過 HBM 2 kV 與 CDM 500 V 的產品安全規範。然而於輸入輸出端口施加靜電放電防護電路，其寄生效應對電路效能將產生不可避免的負面影響，靜電放電防護元件的寄生效應會嚴重影響射頻電路與高速輸入輸出介面電路的頻寬，為了使射頻電路與高速輸入輸出介面電路能安全操作在應用頻段，靜電放電防護元件的寄生效應需被最小化。除此之外，為了維持良好的靜電放電耐受度，主動式電源箝制靜電放電防護電路在全晶片靜電放電防護上扮演重要的腳色。不幸的是，傳統具有 *RC* 網路的電源箝制靜電放電防護電路在熱插拔應用中經常發生誤觸發問題，因此如何開發有效的靜電放電防護設計而不影響正常電路功能，是目前積體電路設計上的重要課題之一。

傳統上，矽控整流器(Silicon-Controlled Rectifier, SCR)因其良好的靜電放電耐受能力與低寄生電容而被廣泛作為靜電放電防護元件使用，但其具有高觸發電壓(V_{t1})，可能在矽控整流器導通前，內部電路先被靜電放電毀損，因此難以廣泛應用於高速積體電路之中。第二章中提出了一個具有低觸發電壓的新型矽控整流器，藉由在其佈局中加入 P+/N+對接結構，以縮短矽控整流器中的電流路徑，進而有效達到減少觸發電壓與導通電阻，使此種矽控整流器能有效應用於保護高速輸入輸出介面電路。

隨著積體電路技術的發展，射頻與高速輸入輸出介面電路操作在更高頻段的需求

日漸增加，如何提高靜電放電防護元件的保護能力並同時避免元件寄生效應影響高頻高速電路的操作，具有相當的困難度與挑戰。因此，第三章提出具有堆疊二極體內嵌系控整流器的分散式靜電放電防護電路用於保護寬頻射頻電路，此設計不僅能達到良好的寬頻阻抗匹配，也能藉由將靜電放電元件藏於焊墊(pad)之下，有效減少面積與得到較高的靜電放電耐受能力。根據晶片量測結果，新型分散式靜電放電防護電路，在 0.1 GHz 至 10 GHz 的頻段內的反射與插入損耗皆能符合需求，且能承受靜電槍 5 千伏特電壓的轟擊。

本論文第四章為電源箝制靜電放電防護電路的安全操作研究。為了克服傳統具有 *RC* 網路的電源箝制靜電放電防護電路的誤觸發問題，本論文提出一新型具有能同時偵測靜電放電突波之電壓爬升時間與電壓準位之電源箝制靜電放電防護電路來達到抑制錯誤啟動事件。此電路被實作於 0.18 微米 1.8 伏特之 CMOS 製程之中，實驗結果顯示新型電源箝制靜電放電防護電路具有良好的靜電放電耐受度(HBM 5.2 kV)與免疫錯誤啟動事件(免疫爬升時間為 10 ns 雜訊)，而且藉由使用小尺寸回授 NMOS 串聯於二極體串尾端，可以有效降低電源箝制靜電放電防護電路之待機漏電(270 nA)。

目前發展的系統單晶片積體電路為了符合產品需求，其系統具有多種電壓準位和不同功能之積體電路，IC 產品在經過靜電放電轟擊測試後，毀損點往往出現在不同電壓準位的介面電路，傳統上會在不同電壓區塊間各別加入獨立的靜電放電防護電路。然而此方式不僅增加電路佈局的複雜度，且當靜電放電轟擊發生在不同電壓區塊之間，過長的放電路徑將降低防護元件的保護效果。第五章即針對此問題提出一新型二極體觸發矽控整流器。此設計不僅能作為自身電源區塊的靜電放電防護元件(可承受 HBM 6 kV)，也能針對不同電源區塊間的接面電路進行防護(可承受 HBM 5.8 kV)。相對於傳統設計架構，新型靜電放電防護元件能大幅減少佈局面積。

本論文第六章為電源箝制靜電放電防護電路的安全操作研究。為了克服傳統電源箝制靜電放電防護電路的誤觸發與高漏電問題，本論文提出一新型具有能同時偵測靜電放電突波之電壓爬升時間與電壓準位之電源箝制靜電放電防護電路來達到抑制錯誤啟動事件。並且藉由使用多晶矽二極體可以有效降低電源箝制靜電放電防護電路之待機漏電(低於 1 μA)。

最後，第七章總結了本篇論文的主要結果，並且提出一些關於未來可以持續進行研究的討論。本論文所提出的新型元件設計與測試結構皆搭配實體晶片進行驗證，所有研究成果皆已發表於國際期刊或國際知名學術會議。

Low-Capacitance and High-Reliable ESD Protection Designs in CMOS Technology

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Abstract

With the continuous evolution of communication technology and integrated circuit (IC), wireless and wireline communication devices had become essential in daily life. All microelectronic products must meet the reliability specifications to be safely used and provide moderate life time. Electrostatic discharge (ESD) protection ability has become one of the important concerns on the reliability of IC products. Most of the failures and damages found in ICs were demonstrated to be related to ESD events. On-chip ESD protection circuits must be added for all I/O pads in IC products to sustain the HBM 2 kV and CDM 500 V for the reliability specifications. However, applying ESD protection devices at the I/O pads inevitably introduce some negative impacts to the high-speed circuit performance due to their parasitic effects. The parasitic capacitance caused by ESD protection devices will strongly degrade the bandwidth in normal high-frequency operation. Thus, the parasitic effects of the ESD protection devices should be minimized. Besides, to sustain good ESD robustness, the active power-rail ESD clamp circuit plays an important role in whole-chip ESD protection design. Unfortunately, the traditional *RC*-based power-rail ESD clamp with NMOS of large size often suffered a mis-triggering issue in hot plug-in condition. The power-rail ESD clamp circuit should be designed to sustain good ESD robustness without influencing the circuit performance.

In Chapter 2, a new SCR-based ESD protection device is used to meliorate the ESD protection effectiveness and parasitic capacitance for high-speed I/O applications. By using a P+ and N+ junction contact with silicide to shorten the path of the SCR, the trigger voltage and turn-on resistance can be reduced to get good ESD robustness.

In Chapter 3, a new distributed ESD protection structure with the stacked diodes with embedded SCR (SDSCR) is proposed to improve the bandwidth and input resistance of ESD protection circuit for broadband RF applications. The ESD protection devices of the proposed circuit are put under the I/O pad to reduce layout area and can discharge the ESD current immediately. From the experimental results, the proposed distributed ESD protection circuit with the SDSCRs can effectively sustain the HMM stress of 5 kV without influencing RF performance.

In Chapter 4, a new power-rail ESD clamp circuit with both timing and voltage-level detection is proposed against false trigger events. The experimental results in a 0.18-μm 1.8-V CMOS process have successfully verified that the proposed power-rail ESD clamp circuit can sustain good ESD robustness (HBM 5.2 kV) without suffering the false trigger issue (high immunity for transient waveform with 10 ns rise time). The standby leakage current along the proposed power-rail ESD clamp circuit under the normal circuit operating condition has been also effectively reduced (270 nA) by adding a feedback NMOS in series into the diode string.

In Chapter 5, a new diode-triggered quad-silicon-controlled rectifier (DTQSCR) is proposed and realized in a 0.18-μm 1.8-V/3.3-V CMOS process to effectively protect the interface circuit between separated power domains. Comparing to the traditional ESD protection design with GGNMOS, and the FOM (ESD level / layout area) of the proposed design is significantly improved ~36% to protect the interface circuits across separated power domains.

In Chapter 6, a simple structure for power-rail ESD clamp circuit with both timing and

voltage-level detection is proposed against false trigger events. A *RC* stage is used for dv/dt detection and a diode string is used to detect the over-stress voltage level during ESD events. The experimental results in a 0.18-μm 1.8-V CMOS process have successfully verified that the proposed power-rail ESD clamp circuit can sustain good ESD robustness (HBM 4.8 kV) without suffering the false trigger issue (high immunity for transient waveform with 10 ns rise time). By using fully isolated polysilicon diodes, the standby leakage current of the proposed power-rail ESD clamp can be effectively reduced (below 1 μA).

Chapter 7 summarizes the results of this dissertation, where the future works based on the new proposed designs and test structures are discussed as well. The related works in this dissertation have been published in several international journals or conferences.