國 立 交 通 大 學

電子研究所

碩 士 論 文

應用於 USB Type-C 介面之

過壓偵測電路與湧浪防護設計

Design of Over-Voltage Detection Circuit and Surge Protection for the CC Pin in USB Type-C Interface against Electrical Overstress Events

研 究 生: 柯兆陽 (Chao-Yang Ke)

指導教授: 柯明道教授 (Prof. Ming-Dou Ker)

中 華 民 國 一〇九 年 二 月

應用於 USB Type-C 介面之
過壓偵測電路與湧浪防護設計

Design of Over-Voltage Detection Circuit and Surge Protection for the CC Pin in USB Type-C Interface against Electrical Overstress Events

研 究 生： 柯兆陽　　Student： Chao-Yang Ke

指導教授： 柯明道　　Advisor： Ming-Dou Ker

國 立 交 通 大 學

電子研究所

碩 士 論 文

A Thesis
Submitted to
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master of Science
in
Electronics Engineering

February 2020
Hsinchu, Taiwan, Republic of China

中 華 民 國 一〇九 年 二 月

應用於 USB Type-C 介面之
過壓偵測電路與湧浪防護設計

學生: 柯 兆 陽　　　　　　　指導教授: 柯 明 道 教授

國立交通大學

電子研究所

摘要

USB Type-C 近幾年成為電子產品當中熱門的傳輸介面，未來將有望統一使用於所有電子產品中，主要由於其支援高速資料傳輸、快速充電以及正反插拔等功能，而上述的功能均須由組態通道腳位(CC 腳位)進行協定，因此 CC 腳位的角色至關重要。為了支援快速充電，V_{BUS} 腳位必須抬升至最高 20 伏特的電壓，然而由於 USB Type-C 接頭上的腳位數量眾多且間距相近，CC 腳位因為在插拔時有機會誤觸到鄰近的 V_{BUS} 腳位，造成 V_{BUS} 腳位較高的工作電壓施加在 CC 腳位上，使得 CC 腳位發生過壓的問題，造成內部電路的損壞。另外，為了支援快速充電、高功率傳輸等功能，在連接至內部電源管理 IC 的腳位(V_{BUS} 腳位與 CC 腳位)也會有湧浪事件(surge events)發生，此問題同樣也會對內部電路造成損壞。因

此，針對上述兩項議題，本研究提出了兩種過壓防護電路，能夠用於偵測 CC 腳位的電壓等級，當電壓高於一個定值，此過壓防護電路會被觸發進而關閉 HVNMOS 切換開關(pass transistor)，保護內部電路受到過壓損壞，同時又能夠避免 HVNMOS 切換開關受到熱載子退化效應(hot carrier degradation)的影響。

本論文主要分為四個部分，首先，第一部分會先簡介 USB Type-C 傳輸介面以及相關的規格，並介紹 CC 腳位的功能。接著會切入此研究主要面對的議題，一個是 CC 腳位因為在插拔時誤觸到 V_{BUS} 腳位造成的過壓事件，另一個是湧浪事件。第二部分則是針對前人已經提出的過壓防護電路做簡單的介紹。

第三部分探討此兩種過電壓的事件分別對於 HVNMOS 切換開關所造成的熱載子退化性應。研究結果可以發現，HVNMOS 切換開關在導通狀態(ON-state)下，經過了 10000 次的轟擊之後電性參數有明顯的偏移，因此證明 HVNMOS 雖然能夠用於保護內部電路免於過壓損壞，但是同時必須搭配過壓防護電路，才能讓 HVNMOS 本身有夠好穩健性(robustness)去抵抗熱載子退化效應。

第四部分則是提出了新型的過壓防護電路設計，其中分為兩種類型，一種是能夠偵測 CC 腳位因為在插拔時誤觸到 V_{BUS} 腳位造成的過壓事件，另一種是能夠偵測湧浪事件。而兩種電路都能夠透過齊納二極體(Zener diode)來調整電路本身的觸發電壓。由量測結果顯示，此兩種過壓防護電路均能夠在過電壓事件來臨時，關閉 HVNMOS 切換開關，同時，CC 腳位內部電路的壓降也能夠下降至 5 伏特左右，使內部電路免於過壓損壞。

此研究不論是在元件層級(device-level)或是電路層級(circuit-level)方面，都經過 0.15 微米(0.15 μm) BCD 製程下線驗證，因此本研究所提出的過壓防護電路解決方案能夠完全整合於 USB Type-C IC 產品當中，進而增加 USB Type-C 產品的可靠度。

Design of Over-Voltage Detection Circuit and Surge Protection for the CC Pin in USB Type-C Interface against Electrical Overstress Events

Student: Chao-Yang Ke **Advisor: Prof. Ming-Dou Ker**

Institute of Electronics

National Chiao-Tung University

Abstract

USB Type-C has drawn much attention due to the advantages of high power delivery, fast charging, and high-speed data transmission. Therefore, it will most probably become the unified input/output interface of electronic devices in the future. The CC (configuration channel) pin in USB Type-C plays an important role to achieve those functions mentioned above by system protocol. In order to achieve fast charging, the V_{BUS} pin is needed to be raised up to a maximum level of 20 V. However, owing to the shrinking space between the pins of the connector, the CC pin next to the V_{BUS} pin takes higher risks of EOS events when shorting to V_{BUS} pin during plugging or

unplugging operations. Besides, high power delivery makes the USB Type-C interface system be in the risk of surge damage, especially for the power management integrated circuit (PMIC) which contains V_{BUS} pins and CC pins. Hence, a new proposed over-voltage protection (OVP) circuit is used to detect the voltage of the CC pin. When the voltage onto the CC pin is raised to a specific value, the OVP circuit is triggered to turn OFF the HVNMOS pass transistor. Thus, the internal circuit of the CC pin can be prevented from being damaged by EOS or surge events, and the robustness against hot carrier degradation can be improved significantly.

This thesis can be divided into four parts, the first part is the introduction of the USB Type-C interface and the CC pin. The EOS and surge events in the USB Type-C interface being focused in this thesis are pointed out as well. The second part introduces some prior arts of over-voltage protection circuits in the USB Type-C interface.

The third part is to investigate the hot carrier degradation (HCD) on the HVNMOS with both events respectively. The measurement results confirm that the EOS and surge events do cause HCD after many times zapping on the drain side when the HVNMOS is in ON-state. Therefore, the HVNMOS used as a pass transistor at the CC pin is requested to keep in OFF-state during EOS and surge events.

The fourth part is the verification of the new proposed OVP circuits with two types. The main function of the proposed OVP circuits is to turn OFF the gate when EOS or surge events happening on the CC pin and limit the unexpected high voltage entering into the internal circuit of the CC pin. The proposed OVP circuits are successfully verified in a 0.15-μm BCD technology. As a result, the OVP circuit can be fully on-chip integrated into the USB Type-C IC products to enhance the reliability against EOS and surge events.