

國立交通大學

電子研究所

碩 士 論 文

高壓製程靜電放電防護元件之

湧浪耐受特性改善

The logo of National Tsing Hua University is a circular seal. It features a central design with a book and a torch, surrounded by the university's name in Chinese and English. The year '1896' is inscribed at the bottom of the seal.

**Improvement of ESD Protection Devices in High-Voltage BCD Technology against Surge Test**

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中華民國 一〇九 年 二 月

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# 高壓製程靜電放電防護元件之 湧浪耐受特性改善

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高壓製程積體電路在車用電子、驅動面板、消費性電子產品及電源管理等方面，近年來均獲得極大的重視與廣泛應用。在高壓製程技術中，為了使高壓電晶體能承受高操作電壓，製程上的複雜度與確保高壓元件可靠度的困難性也隨之增加。靜電放電(ESD)及湧浪(Surge)防護能力是目前高壓電子產品可靠度的重要指標之一。

隨著數位歐盟(Digital Europe)、國家電工委員會(IEC)、中國通訊標準化協會(CCSA)等國際組織要求消費性電子產品之充電接頭統一為 USB Type-C，且 USB Type-C 具有正反插拔、高速資料傳輸，以及高功率快速充電等特點，USB Type-C 近幾年成為電子產品中相當熱門的傳輸介面。目前業界對於 USB Type-C  $V_{BUS}$  腳位( $V_{BUS}$  pin)之常用規格為 28-V 湧浪耐受能力，由於 USB Type-C 為外部連接

埠，在插拔過程中容易受到湧浪轟擊，進而使內部電路受損，因此第二章將針對 USB Type-C 之高壓  $V_{BUS}$  腳位的輸入輸出介面進行湧浪耐受能力的探討，並且提出湧浪防護之設計考量。另外，針對晶圓廠提供之高壓積體電路靜電放電防護元件—PNP 雙載子接面電晶體(PNP BJT)，進行湧浪耐受特性量測與分析。

本論文第三章提出使用堆疊架構之低壓電晶體作為高壓積體電路中的靜電放電及湧浪防護元件，避開複雜的高壓製程所導致之可靠度問題，並藉由調整堆疊個數用於  $V_{BUS}$  腳位之操作電壓，將此低壓堆疊元件與 PNP 雙載子接面電晶體之靜電放電及湧浪防護特性相互比較。接著第四章提出一應用於高壓  $V_{BUS}$  輸入輸出介面之湧浪防護元件，藉由調整其 PNP 雙載子接面電晶體之佈局方式，以提升此高壓輸入輸出介面之整體湧浪耐受度，此新型 PNP 雙載子接面電晶體已於 0.15 微米高壓 BCD (Bipolar-CMOS-DMOS) 製程中獲得實驗驗證。

為了符合業界產品需求，目前發展的系統單晶片積體電路具有多種電壓準位和不同功能之積體電路，而針對不同電壓準位設計靜電放電及湧浪防護元件，藉由調整 PNP 雙載子接面電晶體之元件結構，僅微幅增加其佈局面積，即可提供不同操作電壓介面之防護元件，並且應用於電視面板之全晶片靜電放電防護設計。

最後，將本篇論文的主要結果總結於第六章，並且提出一些關於未來可以持續進行研究的討論。本論文提出之學術研究貢獻，除了對高壓製程靜電放電防護元件之湧浪耐受特性調查與改善外，更實際應用於積體電路產品之全晶片靜電放電設計。

# **Improvement of ESD Protection Devices in High-Voltage BCD Technology against Surge Test**

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Recently, the demands of high-voltage integrated circuits (ICs) are increasing rapidly with the popularization of automotive electronics, driver circuits for display panels, consumer integrated circuits (ICs), and power management applications. In the high-voltage (HV) technology, the complexity of the process and the reliability of HV devices have become more challenging compared with the low-voltage (LV) devices. With the thriving applications in silicon ICs, the demands of HV ICs are increasing rapidly, on-chip electrostatic discharge (ESD) and surge protection capabilities are the important reliability issues for HV electronic products.

Since Digital Europe, International Electrotechnical Commission (IEC), and other international organizations have been requiring USB Type-C as the unified charging

connectors of consumer electronic products. However, USB Type-C has drawn much attention due to the advantages of high power delivery, fast charging, and high-speed data transmission. Therefore, it will become the unified input/output interface of all electronic devices in the future. Since USB Type-C is an exposed external system port, surge events easily occurred at the  $V_{BUS}$  interfaces on USB Type-C during plugging and unplugging. From the industry specification, the  $V_{BUS}$  HV pins have to pass 28-V surge immunity. Chapter 2 is to investigate surge immunity of the  $V_{BUS}$  pins on USB type-C HV interfaces and design considerations of the on-chip surge protection device.

Because the maximum target voltage of  $V_{BUS}$  interfaces is 20-V, the on-chip protection devices must have non-snapback characteristics to prevent latch-up danger. Chapter 3 is to compare the ESD and surge performance between the HV PNP BJT and LV devices with stacked configuration. To meet the specification of USB type-C  $V_{BUS}$  interfaces regulated to 28-V surge level, the on-chip protection device should be added under/near the pad on  $V_{BUS}$  HV interfaces. Chapter 4 is to propose the new test structures of HV PNP BJT, and surge immunity of the proposed on-chip HV PNP BJT protection devices can be optimized by adjusting the layout diagram of the devices. The proposed on-chip surge protection devices have been successfully verified in a 0.15- $\mu\text{m}$  BCD technology.

Since different functions with multiple operating voltages are integrated into a silicon chip for TV panel applications, Chapter 5 is to introduce the ESD and surge protection device for several signal voltages by adjusting the device structures of the proposed PNP BJT, where the concept of whole-chip ESD protection design for TV panel applications is mentioned as well. In the end, Chapter 6 is to summarize the main results of this thesis, where the future work based on the trend of analog applications in the industry is discussed as well.