國立交通大學

電子研究所

碩　士　論　文

實現於互補式金氧半製程下的蕭特基二極體
及其在跨域元件充電模式的靜電防護能力

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in 0.18-μm CMOS Process
for Cross-Domain CDM ESD Protection

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摘要

靜電放電(Electrostatic Discharge, ESD)是現今積體電路中最具挑戰性的可靠度議題之一，由於積體電路朝向系統單晶片(System on Chip, SoC)發展，為了達到不同的需求像是電源管理或是抗雜訊，一顆晶片上出現不同供電域已經成為了必然。除此之外，為了提升運算速度，電晶體的閘極氧化層也越來越薄，使得元件充電模式(Charged-Device Model, CDM)靜電放電更為嚴重。因此，跨域的元件充電模式靜電放電防護便是此次的研究方向。

典型的全晶片靜電防護架構以二極體作為放電路徑的一部分，面對元件充電模式靜電放電，本論文試圖利用蕭特基二極體(Schottky Diode)較低的啟動電壓來改善其放電行為，然而在 0.18 微米 CMOS 製程中，以二矽化鈦($TiSi_2$)與矽所形成的蕭特基接面大幅降低電流密度，使得靜電耐受度下降。

接著在跨域電路 VSS 間放置不同靜電放電二極體，結果同樣顯示以蕭特基接面為放電路徑者會降低靜電耐受度。對遭受元件充電模式靜電放電測試損害之元件做故障分析(Failure Analysis)，定位出故障點皆位於介面電路之中。

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Abstract

Electrostatic discharge (ESD) is one of the most challenging reliability issues for integrated circuits (ICs). With the development of ICs toward system-on-chip (SoC) applications, it has been necessary for multiple power domains to be integrated into a single chip for the purpose of power management or noise isolation. In addition, the transistors have been fabricated with thinner gate oxide to achieve higher operating speed, making charged-device model (CDM) ESD events more critical. Thus, cross-domain CDM ESD protection design became the research direction of this thesis.

A typical whole-chip ESD protection circuit takes diodes as part of the discharge path. This paper attempts to utilize the low cut-in voltage of Schottky diodes to improve the discharge behavior under CDM ESD events. However, the Schottky junction formed by $TiSi_2$ and silicon greatly reduces the current density, and decreases ESD robustness in 0.18-μm CMOS process.

Furthermore, different diodes are placed between the VSS of cross-domain circuits, and the results show a lower CDM ESD level for Schottky junctions. Failure analysis (FA) is applied to detect the failure points after the CDM ESD test, which is then summarized to be located at the interface circuits.