國立交通大學

電子研究所

博士論文

應用於可植入式生醫晶片之靜電放電防護電路與閂鎖防護設計

On-chip ESD Protection and Latch-up Prevention in Silicon Chips for Implantable Biomedical Applications

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摘　　要

隨著半導體產業的發展，製程正以驚人的速度微縮，也因為電晶體的閘極氧化層變得更薄，靜電放電對於電路的衝擊已然成為影響產品可靠度的主要因素之一。然而，對於植入式生醫元件來說，電路若是因為損壞而產生錯誤的操作，往往都有可能危害到病人的生命安全。因此，植入式生醫元件勢必要做到全晶片的靜電放電防護設計，以避免電路遭受靜電放電轟擊後產生致命性的錯誤操作。

與一般的電路相比，植入式生醫元件中的電路通常都有較高的供應電壓，同時也擁有包含正、負電壓的輸入輸出端，所以必須使用額外設計的靜電放電防護元件來做保護。正因為如此，有許多能夠承受高電壓的電壓箝位電路 (power-rail ESD clamp circuit) 已經被提出，並且做了驗證。不過，應用於負電壓下的電壓箝位電路卻從來沒有被提起過。由於元件結構中有許多寄生路徑存在，在設計防護電路時必須仔細的考量，才不會造成電路的錯誤操作。因此，第二章中提出了一種可以應用於負電壓下的電壓箝位電路，不僅可以提供操作於-6 V 電壓下的電路做使用，也可以經過觸發電路來讓靜電放電主要元件迅速導通，以達成良好的靜電放電耐受度。同時，本章也提出了一種雙向的元件，可以安裝在±3V 應用的輸入輸出端，來釋放靜電放電電流，以保護內部電路不受靜電轟擊的影響。所提出的雙向元件已結合刺激器的輸出端來做驗證，並且確實可以達到該有的

保護效果。因此，將本章所提出的兩種元件安裝於電路中，再加上先前技術所提出的電壓箝位電路，便可以達到完整的全晶片靜電放電防護效果。

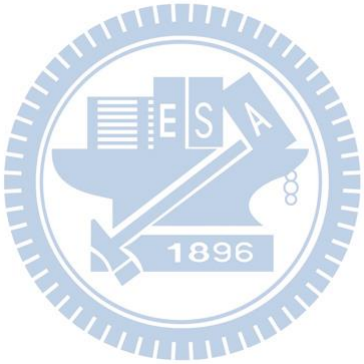
然而，為了讓電晶體與 P-substrate 做隔離，第二章所提出的電路使用了 deep n-well 來做隔離，並且將其連接至 0 V 的電位。正因為如此，在製程的微縮下，所有的元件將會離彼此之間的距離越來越近。在這樣的情況下，閂鎖效應 (latch-up) 便有可能會藉由寄生的 p-n-p-n 結構產生，並且對電路造成影響。因此，第三章便以 pMOS 到接地 DNW 的測試結構來研究閂鎖效應的免疫能力。在測試結構中，一種以蕭特基二極體 (Schottky barrier Diode, SBD) 嵌入的設計被提出。利用蕭特基二極體的特性，可以使結構中的保持電壓有效地提升，讓閂鎖效應不再輕易發生，進一步增加電路的閂鎖效應的免疫能力。

雖然造成閂鎖效應的結構會對電路造成預期外的影響，但是這樣的結構也被當作非常良好的靜電放電防護元件。由於其能夠在更小的佈局面積下提供良好的靜電放電防護能力，矽控整流器 (Silicon-Controlled Rectifier, SCR) 也經常被應用為防護元件，但由於那過低的持有電壓，使得其無法在積體電路中做廣泛的應用。有鑑於第三章的應用，嵌入式蕭特基二極體成功地提升了 SCR 的持有電壓，並且不會影響電路的正常操作，或是改變佈局的方法。所以，第四章提出了一種嵌入式蕭特基二極體矽控整流器，不僅能夠使 SCR 的保持電壓提升，也能夠達到不錯的靜電放電保護能力。如此一來，便可以讓 SCR 元件在應用的層面上更加地廣泛。

由於 SCR 元件的優秀防護能力，使得其在先進製程上也有一定的發展性。對於佈局規則嚴格以及昂貴的鰭式場效電晶體 (Fin Field-Effect Transistor, FinFET) 製程來說，若能減少靜電放電防護元件的佈局面積，勢必可以降低晶片的開發成本。因此，第五章提出了一種翻轉式的 SCR 元件，利用改變電流的流向，來增加同樣面積下的靜電放電能力。透過實驗的結果證明，所提出的元件不僅能更快地導通來排放電流，也確實能夠提供更好的靜電放電防護能力。

總結上述所言，本論文所提出之電壓箝位電路以及雙向防護元件能應用於植入式生醫電路，並且可以確實操作在負電壓之應用下，同時也利用蕭特基接面解決了負電壓應用下可能遭受的閂鎖問題。由蕭特基二極體嵌入所衍生出的 SCR 架構也同樣擁有足夠

高的持有電壓，並且適合做為高電壓應用下的植入式生醫電路靜電放電防護元件。因此，本論文所提出之靜電放電防護元件能夠裝載在植入式生醫電路的 GND 到 VSSH 還有 I/O 到 GND 之間，使得全晶片之靜電放電防護可以真正的實現。



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Abstract

With the development of the semiconductor industry, the manufacturing process is shrinking at an astonishing speed. Due to the gate-oxide of the transistor becoming thinner, the electrostatic discharge (ESD) protection has been known as one of the important issues in the various reliability specifications. However, in the implanted biomedical devices, any erroneous operation caused by the damaged of internal circuit is possible to endanger the life of patient. Considering the requirement of high reliability for the implanted biomedical devices, the ESD protection circuits should be installed between any power pin to avoid the damage caused by ESD stresses.

In the implanted biomedical devices, the voltage bias is usually higher than that of the normal operation. Furthermore, the negative voltage has also been widely applied in the circuit of implanted biomedical devices. In order to protect the negative-voltage pins of the implanted silicon chip from the ESD damage, the ESD protection circuit should be carefully designed to avoid any wrong current path under normal circuit operation with the negative voltage. In Chapter 2, a new power-rail ESD clamp circuit for the application with an operating voltage of

-6 V has been proposed. With the proposed ESD detection circuit, the turn-on speed of the main ESD clamp device can be greatly enhanced. In addition, a bi-directional device has also been proposed in this chapter, which can be installed between the I/O port and GND of ±3 V application to protect the internal circuit from the ESD stresses. Thus, after combining the power-rail ESD clamp circuits and the bi-directional devices, the whole chip ESD protection design for implanted biomedical devices can be realized.

In Chapter 3, a test structure has been fabricated to investigate the latch-up issue in the negative voltage application. In order to supply the negative voltage source for circuit operations in the silicon chip with the grounded common p-type substrate, the isolation rings configured with n-well (NW) and deep n-well (DNW) layers must be used to isolate the circuits of nMOS devices operating with negative voltage from the common P-substrate. Such NW/DNW isolation rings in the circuit layouts are often connected to GND (0V) for the circuit operations with a negative voltage source. However, a parasitic p-n-p-n path from I/O pMOS to this grounded NW/DNW isolation ring may be formed, which may put the circuits at high risk of the latch-up issue. In this chapter, a novel method to improve latch-up immunity against such parasitic p-n-p-n path in the circuits with grounded NW/DNW isolation ring is proposed. By using the Schottky junction, the holding voltage (V_h) of the parasitic p-n-p-n path can be significantly increased, and the latch-up immunity can be effectively improved.

The silicon-controlled rectifier (SCR) has been reported to protect CMOS integrated circuits (IC's), due to the high ESD robustness within a small silicon area. However, the holding voltage (V_h) of the SCR device was too low to endure the latch-up issue. Thus, the V_h value of the SCR device must be improved to become greater than the circuit operating voltage for safe applications. In Chapter 4, the Schottky-embedded modified lateral silicon-controlled rectifier (SMLSCR) with high holding voltage for ESD protection was proposed. By using the Schottky barrier junction, the V_h value of the SCR device can be improved by the reverse-bias Schottky barrier diode (SBD) that is embedded into the SCR device structure. Among those experimental

results, the SMLSCR device can demonstrates a good ESD protection capability.

The FinFET architecture has been widely used in the digital circuit application, due to the good short channel effect control and driving current boost. However, the low-level thermal dispassion and smaller effective silicon volume would cause significant impact during the circuits under ESD event. Thus, the ESD protection device should be installed into the high-speed digital circuit to enhance the ESD robustness. To avoid affecting the circuit performance, the parasitic capacitance of the ESD device must be as low as possible. In Chapter 5, a Fin-diode-triggered rotated SCR with a dual ESD current path has been proposed. The proposed devices have better current-handling capability, sufficiently low parasitic, compact layout area, and low leakage current.

In summary, the proposed power-rail ESD clamp circuit and the bi-directional device can be applied to the implantable biomedical circuits, where can operate under negative voltage applications. Simultaneously, the latch-up issue that may be encountered under negative voltage applications can also be solved by the Schottky junction. The Schottky-embedded SCR architecture also has a sufficiently high holding voltage and is suitable for the implantable biomedical circuit ESD protection device under high voltage application. Therefore, after equipped the proposed ESD protection devices at GND-to-VSSH and I/O-to-GND of implanted biomedical circuit, the whole-chip ESD protection design can be truly realized.