國 立 交 通 大 學

電子研究所

碩 士 論 文

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且相容二倍工作電壓之靜電放電箝制電路

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Power-Rail ESD Clamp Circuits Against False Trigger

During Fast Power-ON Events

研 究 生: 黃瀚生 (Han-Sheng Huang)

指導教授: 柯明道教授 (Prof. Ming-Dou Ker)

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摘要

隨著互補式金氧半（CMOS）製程技術不斷演進，核心運算晶片閘極氧化層厚度與工作電壓（1xVDD）持續下降以提供更快的操作速度與降低功耗，然而在系統電路板上，周遭晶片可能還維持在較高的工作電壓（2xVDD 或是更高）。為兼容較早期的介面規格，過去已有 2xVDD 共容輸出緩衝器與邏輯閘被開發協助混合電壓共容輸入/輸出介面並只用 1xVDD 元件。

針對前述 2xVDD 共容相關電路的靜電放電防護，考量在快速上電情況中，因為 2xVDD 電壓上電速度過快，導致傳統使用時間偵測機制之 2xVDD 共容靜電放電箝制電路出現無法保持關閉的誤觸發問題。所以本論文提出改用電壓偵測

機制之 2xVDD 電壓共容靜電放電箝制電路，使用基板觸發(Substrate-Trigger)技術的堆疊式電晶體(Stacked-NMOS)做為主要靜電防護元件，利用二極體連接方式的電晶體(Diode-Connected-PMOS)組成二極體串，設定可調整的最低啟動電壓(Minimum Starting Voltage, $V_{STARTING}$)以區分快速上電事件情況與靜電放電突波情況。傳統與新提出之 2xVDD 共容並只用 1xVDD 元件的靜電放電箝制電路已於 1.8 伏/3.3 伏 0.18 微米互補式金氧半製程下成功驗證。實驗結果證明新提出之設計能夠防止快速上電誤觸發事件並且具有優異的靜電放電防護能力達 HBM Level 5.25kV。

然而考量供應電壓上電順序，2xVDD 較 1xVDD 先上電，前述新提出之 2xVDD 共容靜電放電箝制電路會有暫態過壓問題發生。故本論文修改所提出之設計，加入二極體串電壓分壓器將 2xVDD 分出一半的電壓取代 1xVDD 電源線，在晶片工作與上電情況下偏壓所有靜電放電箝制電路內的 1xVDD 元件，確保電路各元件安全地偏壓而沒有過壓問題。二極體串電壓分壓器使用多晶矽二極體組成，已於相同 1.8 伏/3.3 伏 0.18 微米互補式金氧半製程下驗證，可以降低待機漏電，減少製造成本並提高佈局整合度。實驗結果證明修改之設計能夠有效減緩暫態過壓問題，同時提供足夠高的二次崩潰電流(It2)達約 4A 並可以防止快速上電誤觸發事件。

Design of 2xVDD-Tolerant Power-Rail ESD Clamp Circuits Against False Trigger During Fast Power-ON Events

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Abstract

As CMOS technology is continuously scaled down to nanoscale, the gate oxide of core devices becomes thinner with a lower operating voltage level (1xVDD) to gain a lower power consumption at higher operating speed. However, for compatible to some earlier circuit specifications with higher operating voltage levels (2xVDD, or even more), some 2xVDD-tolerant output buffers and 2xVDD-tolerant logic gates with only 1xVDD devices had been developed to support mixed-voltage I/O interfaces.

For ESD protection of 2xVDD-tolerant circuits aforementioned, under fast power-on condition, 2xVDD rises too fast for traditional RC-based 2xVDD-tolerant power-rail ESD clamp circuit to keep in off-state results in false-trigger issue. Therefore, a

new 2xVDD-tolerant power-rail ESD clamp circuit adopting voltage detection mechanism is proposed and stacked-NMOS (STNMOS) using substrate-trigger technique is combined as main ESD-clamping device. The voltage detection mechanism with diode string composed of diode-connected PMOS is used to set an adjustable minimum starting voltage ($V_{STARTING}$) to distinguish fast power-on condition and ESD pulse condition. The traditional and proposed design with only 1xVDD devices have been successfully verified in a 0.18-μm 1.8/3.3-V CMOS process. The experimental results have confirmed that the proposed ESD clamp circuit can sustain a good HBM ESD level of 5.25kV and high immunity against false-trigger issue under fast power-on condition.

However, in consideration of power-on sequence, that 2xVDD rises before 1xVDD rises makes the proposed 2xVDD-tolerant power-rail ESD clamp circuit suffer transient over-voltage issue. Therefore, in this thesis, without using 1xVDD power line, the proposed design is modified by adding a diode string as a voltage divider. 2xVDD is divided in half by the extra diode string, and all the 1xVDD devices used can be biased safely without over-voltage issue under circuit operating and power-on condition. The voltage divider is composed of polysilicon diodes fabricated and verified in the same 0.18-μm 1.8/3.3-V CMOS process for lower standby leakage current, less fabrication cost and higher layout compatibility. The experimental results have confirmed that the modified design can effectively relieve the transient over-voltage issue while high secondary breakdown current (It2) of ～4A and high immunity to false-trigger issue are still achieved.