國立陽明交通大學

電子研究所

碩 士 論 文

Institute of Electronics

National Yang Ming Chiao Tung University

Master Thesis

應用於帕金森氏症治療之電流—電壓雙模式可植入式單端雙相刺激器設計

Design of Dual-Mode Monopolar Biphasic Implantable Stimulator for Parkinson Disease Application

研 究 生：蕭榆潔 (Hsiao, Yu-Jie)

指導教授：柯明道 (Ker, Ming-Dou)

中 華 民 國 一一〇 年 二 月

February 2021

應用於帕金森氏症治療之電流—電壓雙模式可植入式單端雙相刺激器設計

Design of Dual-Mode Monopolar Biphasic Implantable Stimulator for Parkinson Disease Application

研 究 生：蕭榆潔　　Student: Yu-Jie Hsiao

指導教授：柯明道教授　　Advisor: Prof. Ming-Dou Ker

國 立 陽 明 交 通 大 學

電子研究所

碩 士 論 文

A Thesis
Submitted to
Institute of Electronics
College of Electrical and Computer Engineering
National Yang Ming Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master of Science
in
Electronics Engineering

February 2021
Hsinchu, Taiwan, Republic of China

中 華 民 國 一一〇 年 二 月

應用於帕金森氏症治療之電流—電壓雙模式可植入式單端雙相刺激器設計

學生：蕭 榆 潔　　指導教授：柯 明 道 教授

國立陽明交通大學

電子研究所

摘要

全球至今已有數億人受神經系統疾病所苦，常見包括癲癇、偏頭痛、慢性疼痛、失智症以及帕金森氏症等疾病。其中帕金森氏症為僅次於阿茲海默症，第二常見的神經退化性疾病，影響全球約一千多萬人。由於其病因尚不清楚且無法以藥物根治，近年來，在生物醫學與電子工程研究的合作下，神經調控手術可配合藥物對其進行更有效的治療。

隨著積體電路與醫學技術的進步，智慧型仿生晶片的發展已在臨床上證實有顯著療效，並應用於不同疾病治療。已廣泛用於帕金森氏症治療的腦深層刺激手術是利用植入電極，將電刺激器安裝於腦視丘下核、蒼白球等處，藉由脈衝微電流來調節腦部不正常的放電現象，來改善帕金森症狀。

本篇論文支援研究團隊的帕金森氏症計劃，考慮植入式系統單晶片(SoC)整合與不同規格需求，分別提出兩種在 0.18μm 1.8V/ 3.3V 低壓製程與 0.18μm 1.8V/ 5V/ 6V~70V 高壓製程實現的多通道定電流—定電壓雙模式單端雙相位刺激器。低壓製程的電刺激器已整合在 SoC 並於動物實驗完成功能及安全性的驗證，可達到±0.2mA~±3.6mA/ ±0.2V~±3.6V 的輸出電流/ 電壓。

而高壓製程的電刺激器由於規格可達到±0.2mA~±10mA/ ±0.2V~±10V 的輸出電流/ 電壓，可運用耐高壓的電晶體以減少低壓製程中為防元件過壓而堆疊的電晶體數量。另外在高輸出電流值的情況下，非預期中的峰值可能對組織造成傷害，此電刺激器也提出了一降低峰值的改善電路，並在晶片量測獲得驗證。

Design of Dual-Mode Monopolar Biphasic Implantable Stimulator for Parkinson Disease Application

Student: Yu-Jie Hsiao Advisor: Prof. Ming-Dou Ker

Institute of Electronics

National Yang Ming Chiao Tung University

Abstract

To date, there are already hundreds of millions of people around the world who have suffered from neurological diseases, including epilepsy, migraine, chronic pain, dementia, and Parkinson’s disease. Among them, Parkinson's disease is second only to Alzheimer's disease and the second most common neurodegenerative disease, affecting more than 10 million people worldwide. Since the cause of the disease hasn’t been found out and cannot be cured with medical treatment, in recent years, with the cooperation of biomedical and electronic engineering research, neuromodulation surgery can be operated along with medicine to treat the patients in a much more effective way.

With the advancement of integrated circuits and medical technology, the development of smart biomimetic ICs has been clinically proven to have significant

effects and is applied to the treatment of different diseases. Deep brain stimulation surgery, which has been widely used in the treatment of Parkinson's disease, uses implanted electrodes to install electrical stimulators in the subthalamic nucleus (STN), globus pallidus (GPi), etc. Then, electric pulses of current are released to regulate abnormal brain discharge and improve Parkinson's symptoms.

This thesis supports Parkinson's disease project in the research team. Considering the integration of implantable system-on-chip (SoC) and the requirements of different specifications, two multi-channel constant current-voltage (dual-mode) monopolar biphasic stimulators realized in 0.18μm 1.8V/ 3.3V LV CMOS process and 0.18μm 1.8V/ 5V/ 6V~70V HV CMOS process are proposed. The stimulator in LV process has been integrated into the SoC and has been verified for function and safety tests in animal experiments. It can achieve an output current/ voltage range of ±0.2mA~±3.6mA/ ±0.2V~±3.6V.

Because the stimulator in HV process has to reach an output current/ voltage range of ±0.2mA~±10mA/ ±0.2V~±10V, HV transistors can be used to reduce the stacking of components in the LV process to prevent voltage overstress. In addition, in the case of large amplitude during current output mode, unexpected peaks may cause damage to the tissues. Thus, this stimulator also proposes an improved circuit to reduce the peaks, which has been verified by measurement.

Acknowledgment

首先要感謝柯明道教授的教導，無論是研究上、生涯上的建議都讓我受益良多。每次咪挺都能獲得新的研究方向、業界知識，或是心靈上的醍醐灌頂，謝謝老師花這麼多時間在我們身上，尤其在高壓晶片 tape out 出去前發現錯誤真的是拯救了我。還要謝謝在 PD 計劃貢獻心力的教授跟同學們，像是常常給予我刺激器建議的吳重雨校長，以及其暐學長、亦桓學長等一起在實驗室跟體外機晶片奮鬥的夥伴們，很榮幸能一起參與到動物實驗。

再來是實驗室的學長姐們，謝謝道容學姊、昱凱學長、大宇學長、明均學姊、兆陽學長，親切地帶領我們，還有曉平學姊跟佳琪學姊幫助我好多 Charge pump 跟刺激器的問題。一起研究跟修課的好同學彥彰、瀚生、承昀、致鋼、同是 307 的孟融大師、家昀、筱柔，有你們的研究生活真的是一點都不孤單，一起吃飯、唱歌、討論功課、聊聊心事都是我覺得好幸福的事。活潑的學弟妹子齊、昱均、浥庭、雨鑫、易軒也總是為實驗室帶來笑聲。

謝謝 TSRI 提供我下線的機會，還有 TSRI 的工程師及行政人員有效率又有耐心的幫助，讓我能順利完成自己畫的晶片。

最後想謝謝家人朋友們對我貼心的照顧，陪我走過這兩年多艱難又迷茫的時光，謝謝哥哥跟筱頡無論多忙都會接我的電話，跟你們聊天心情都好好。謝謝建和在我寫論文的時候安撫我暴躁的脾氣，每天逗我開心。

好多感謝說不完，真的覺得自己好幸運，我好愛你們~

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation

In addition to traditional ways of treating diseases with medicine, neuromodulation has become another therapeutic option in recent years. Progress in neuromodulation has brought benefits to hundreds of thousands of patients who have suffered neurological disorders. The International Neuromodulation Society (INS) defines neuromodulation as a technology that acts directly upon nerves, working by either stimulating nerves actively to generate a biological response or by applying targeted pharmaceutical agents in tiny doses.

The application of neuromodulation covers a wide range of disorders related to nervous system control, such as Parkinson's disease (PD), Epilepsy, Dystonia, which are listed in Fig. 1.1 [1].

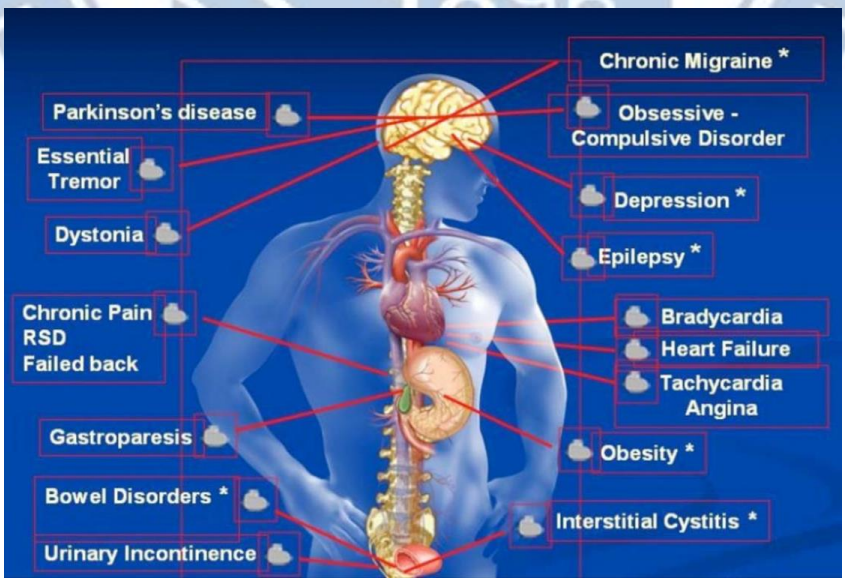


Fig. 1.1 Applications of neuromodulatory devices to the treatment of various medical disorders. [1]

Nowadays, functional electrical stimulation (FES) provides an effective treatment by delivering electric pulses to peripheral sensory and motor nerves to restore the loss of function [2]. For example, there are chronic electrical stimulation applied in spinal cord injured (SCI) patients [3], cochlear implant for hearing loss [4], and deep brain stimulation (DBS) for Parkinson disease. In this thesis, 2 stimulators in LV and HV process are designed for treating Parkinson disease, which has already affected thousands of people in the world so far.

1.2 Overview of Parkinson's Disease and Treatment

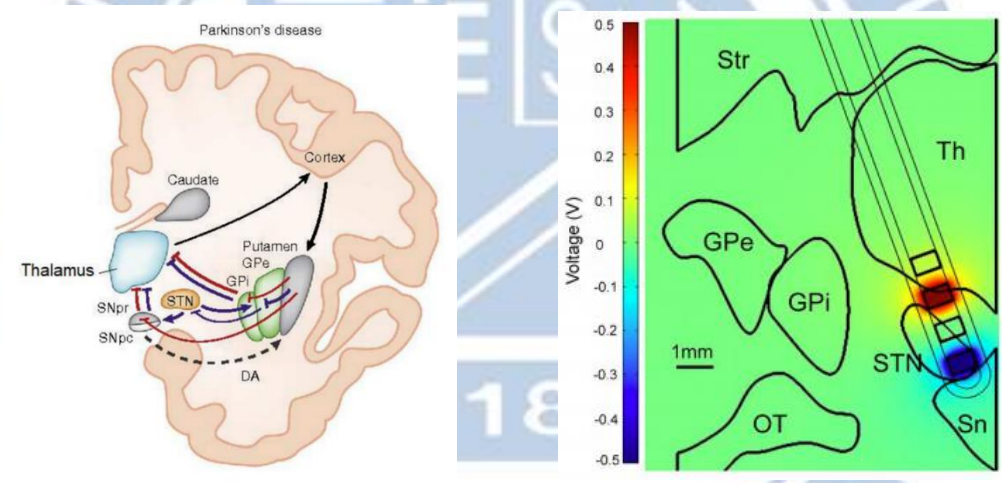
Parkinson's disease (PD) is a neurodegenerative disease that mainly affects the motor nervous system, causing difficulty in movement and even tremor. The cause of PD is still unknown and there is no cure for this disease so far; hence, treatment aims to improve the symptoms in order to ease patients' discomfort.

Since it is believed that the motor symptoms of PD are caused by dopamine deficit owing to the death of cells in the substantia nigra, levodopa (L-DOPA) followed by dopamine agonists are in the first place serving as medication treatment. However, they become less effective as the patient's condition gets worse, along with other side effects.

Another therapy is deep brain stimulation (DBS), which implants a neurostimulator into the brain through neurosurgery, and the implanted cylindrical electrodes deliver electric impulses to the specific region of the brain [5]. It does not cause damage to brain tissues; instead, it can keep motor symptoms under control by generating electric current pulses to modulate those abnormal activities in the brain. Studies have proved that the combination of levodopa and DBS can be administered individually, and demonstrate an improvement in gait parameters [6]. As a result, DBS has become one of the most effective treatments for PD.

Fig. 1.2 shows signal paths related to dopamine that are important in DBS

implementation. Usually, DBS surgery implants the electrode model into the Sub-thalamic nucleus (STN), Globus Pallidus (GPi), or Thalamus in the brain. When stimulation starts, stimulus phases of 130~185 Hz will be sent to the electrode model to help the symptoms of PD by stimulating nerve cells. Several pieces of research have proved that most of the symptoms of PD can be relieved by stimulation of STN or GPi [7], [8]. In general, stimulation of GPi can control drug-induced dyskinesia, movement-related symptoms such as slow movement and stiffness can be improved by stimulation of STN, and stimulation by Thalamus can treat tremor. Above all, the implanted electrodes can be taken out of the brain at any time without harming nerve cells.



(a) (b)

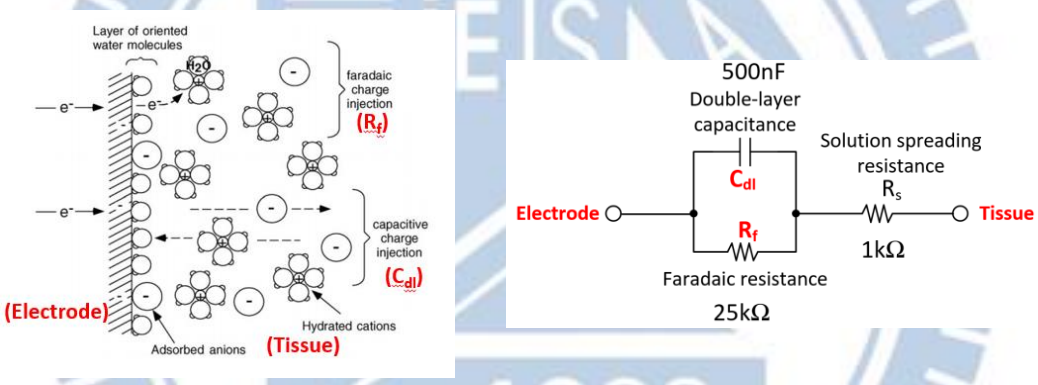
Fig. 1.2 (a) Schematic representation of a classical model in Parkinson's disease. [9] (b) Electrode in STN. [10]

1.3 Introduction of Electrode-Tissue Model

During neurostimulation, electrodes are implanted into the human body and form an interface with body tissue. This interface and equivalent circuit model of it are depicted in 0 [11]. The main components in the simplified circuit model shown in 0 (b) include a double-layer capacitance (C_{dl}), which is formed by ions that are attracted by the electrode, solution spreading resistance (R_s), which is determined by tissue fluid,

and faradic resistance (R_f), which is a changing value determined by oxidation or reduction reaction happened between the electrode and the tissue.

The resistance and capacitance in this equivalent circuit model can be obtained by the curve fitting method. In PD application, the values have been extracted that C_{dl} equals 500nF, R_f equals 25kΩ, and R_s equals 1kΩ. However, as discussed in the article [12], the values of them may be changed and have nonlinear characteristics during stimulation by many factors, such as stimulation frequency, current density passing through, and pulse duration. Above all, this linear equivalent circuit model still gives convenience in doing simulation and measurement.

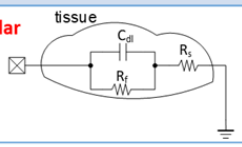
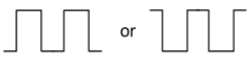
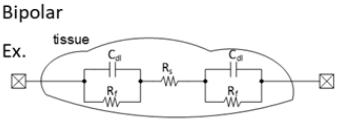
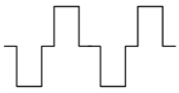


(a) (b)

Fig. 1.3 (a) Electrode-tissue interface (b) Equivalent electrode-tissue circuit model. [11]

1.4 Introduction of Stimulation Patterns

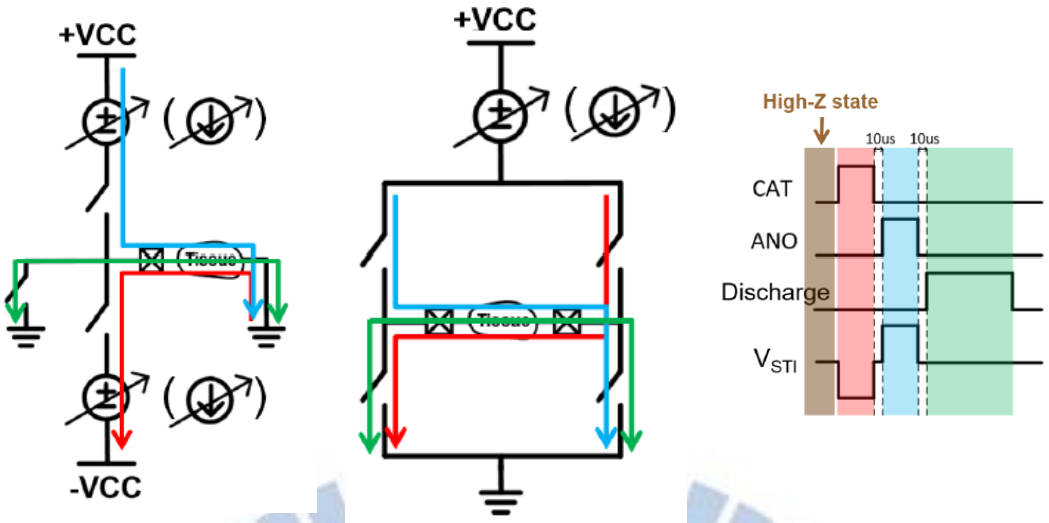
Table 1.1 Patterns of stimulation.

Stimulation Configuration	Stimulation Pulse
Monopolar Ex. 	Monophasic Ex. 
Bipolar Ex. 	Biphasic Ex. 

During neuro-stimulation, a stimulator serves as a constant current source or a constant voltage source according to whether current-mode or voltage-mode stimulation is chosen, as known as constant current stimulator (CCS) or constant voltage stimulator (CVS), respectively. Both current-mode and voltage-mode stimulation are applied in clinical treatment and have 2 types of stimulation configuration (monopolar and bipolar) and 2 types of stimulation pulse (monophasic and biphasic) as illustrated in Table 1.1. In this work, two CCS/ CVS dual-mode monopolar biphasic stimulators are purposed.

A study has investigated the influence of monopolar and bipolar implementation in clinical models [13]. Though bipolar stimulation is more flexible in producing selective activation with more sensitivity, monopolar stimulation has a broader activation region under the same inject current. The simple structure and operation of the two configurations are shown in 0 [14]. Instead of using the opposite way of the current path between two selected channels to produce a negative current in bipolar stimulator, monopolar stimulator needs both positive and negative power supplies, which is also a difficulty when designing this work.

Turning to stimulation pulse, although monophasic pulses can stimulate tissue by either cathode pulse or anode pulse, several applications of FES use biphasic stimulation due to its charge-balanced characteristic to maintain biocompatibility by protecting tissue or electrode from damage [15], [16]. The first phase of a biphasic pulse makes the main impact, and the following phase is a balancing wave, which can reduce the unwanted chemical effect caused by electrical stimulation. That is, the capacitor C_{dl} of the electrode model will have charge remained due to plenty of variation during circuit realizing. Thus, besides biphasic pulses implementation, other charge-balancing methods have been used. For instance, passive and active discharge circuits are applied in this work.



(a) (b) (c)

Fig. 1.4 (a) Operation of monopolar stimulator (b) Operation of bipolar stimulator (c) States of a stimulator. [14]

1.5 Introduction of Implantable Closed-Loop SoC

Stimulators used in DBS surgery are classified into open-loop and closed-loop (also known as adaptive) paradigms. Among them, open-loop DBS is more common for commercial use. Nonetheless, several pieces of research have presented that open-loop DBS leads to higher power consumption than closed-loop DBS [17], [18].

Similar to the concept of the SoC structure presented in [22], 0 shows the block diagram of implanted closed-loop SoC. Besides, stimulators in this thesis will be applied in SoC with this structure and then verified in measurement and animal experiments. This whole DBS system consists of one implanted closed-loop SoC that is implanted in the patient's brain, and one external SoC for doctors to control functions through a graphical user interface (GUI) on a laptop. For PD, the β-band (12-30Hz) of local field potential (LFP) is an efficient bio-marker, and it can be detected by neural-signal acquisition analog front-end (AFE) to determine whether to do stimulation by giving command from bio-signal processor. After receiving message of stimulating, a dual-mode stimulator, which is demonstrated in this thesis, will generate electric pulses

to the human body by electrodes. At last, AFE will sense the artifact again to form a closed-loop DBS system. All powers are supplied by the power management unit (PMU). In addition, wireless power and bilateral data telemetry are preferred to extend the lifetime of this device and provide doctors with information in need.

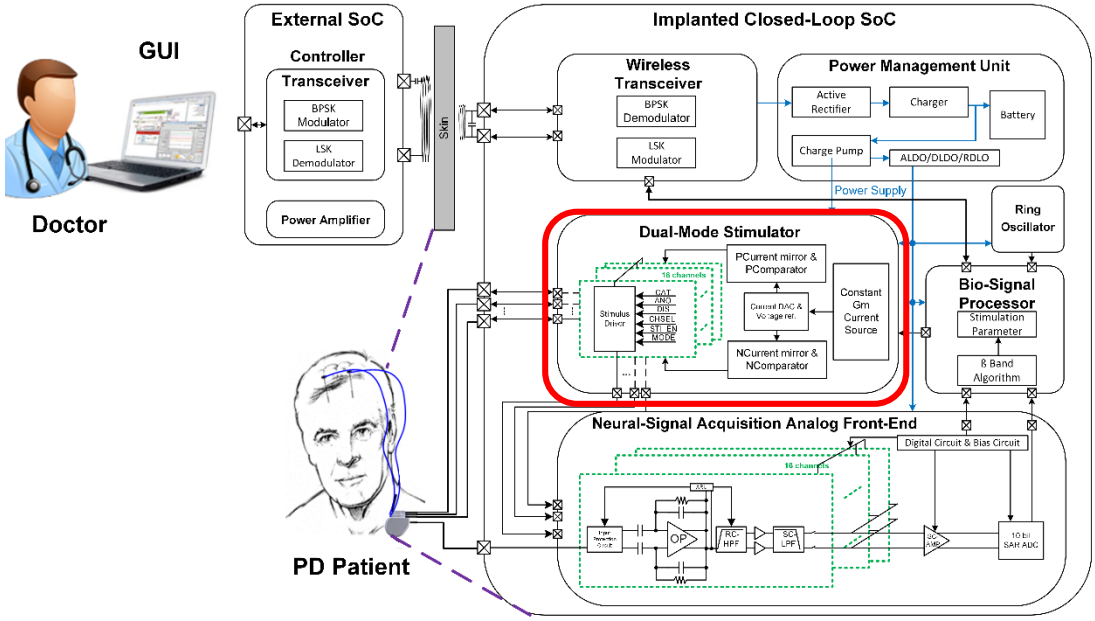


Fig. 1.5 The block diagram of implanted closed-loop DBS SoC with wireless telemetry.

1.6 Thesis Organization

This thesis is organized in four chapters. The first chapter describes motivation of this research and organization of this thesis, following by background knowledge of Parkinson's Disease with its treatment and basic concept of implantable SoC device.

Design of 16-channel dual-mode monopolar stimulator realized in TSMC 0.18μm 1.8V/ 3.3V process is presented in chapter 2, including the prior arts, details of design consideration, simulation results, measurement results, and results in vivo animal experiment test.

Chapter 3 proposes design of 8-channel dual-mode monopolar stimulator with peak-reduced function realized in TSMC 0.18μm HVGen2 process. In this chapter, design considerations and constraints of this HV process will first be demonstrated, and then design, simulation results, and measurement results of this work will be shown.

At last, chapter 4 summarizes the results of works in this thesis, and delivers ideas for future work.

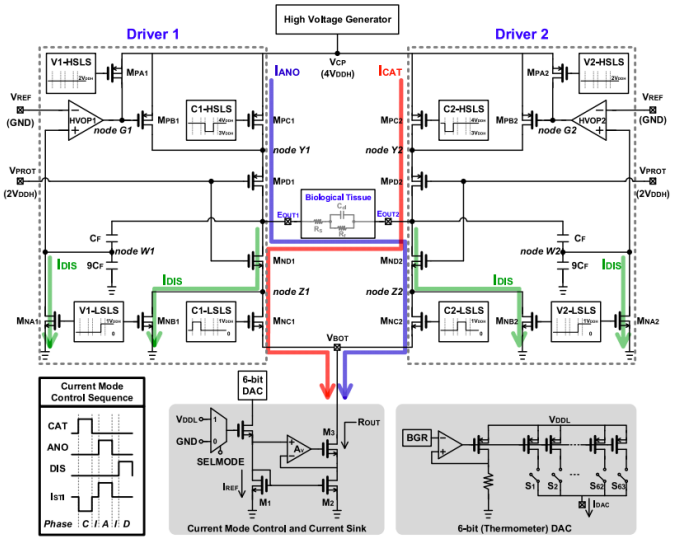
Chapter 2

Design of LV Monopolar Biphasic Dual-Mode Stimulator

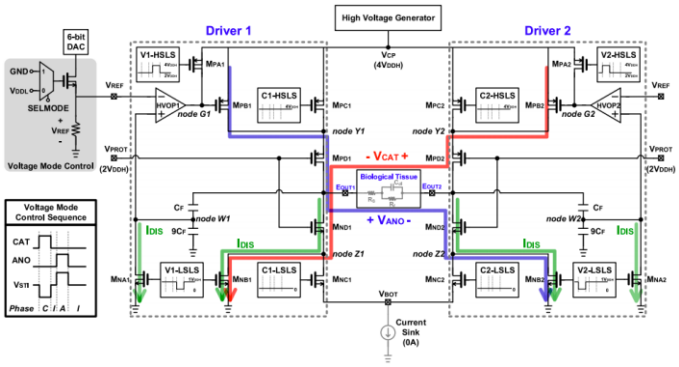
2.1 Prior Art of Dual-Mode Stimulator

2.1.1 Bipolar Dual-Mode Stimulator

Prior work of bipolar configuration with a dual-mode driver structure is purposed in [19]. This stimulator is able to deliver both constant current stimulation and constant voltage stimulation. During the current-mode stimulation, which is shown in Fig. 2.1 (a), the current sink draws a current from V_{CP} through switches on I_{CAT} or I_{ANO} route to stimulate the tissue. In contrast, during the voltage-mode stimulation, which is shown in Fig. 2.1 (b), voltage reference V_{REF} that is generated by voltage source is compared with feedbacks from the stimulus output and then controls the transistors on route V_{CAT} or V_{ANO} to turn on in cathodic stimulation or anodic stimulation, respectively.



(a)



(b)

Fig. 2.1 (a) Current-mode (b) Voltage-mode operation of bipolar dual-mode stimulator. [19]

2.1.2 Monopolar Dual-Mode Stimulator

Since monopolar stimulator shows more efficacy than bipolar stimulator, a dual-mode stimulator in monopolar configuration is purposed in [20]. Similar to the circuit in chapter 2.1.1, this circuit has both current-mode stimulation and voltage-mode stimulation realized in one circuit. As shown in Fig. 2.2, switches S1 and S3 are controlled to turn on current-mode stimulation and send the current from current source to the output. As for voltage-mode stimulation, switches S2, S4, S5 and S6 are turned on in order to form a closed-loop calibration for the voltage output.

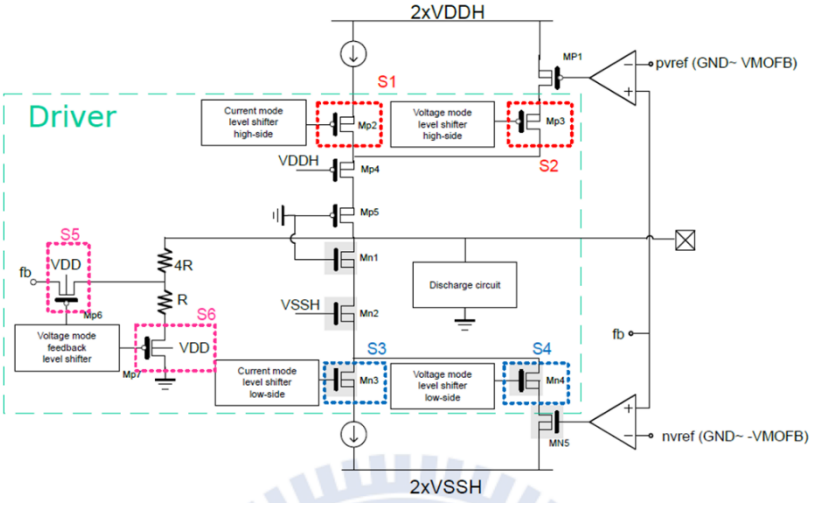


Fig. 2.2 The stimulus driver of a monopolar dual-mode stimulator. [20]

Table 2.2 Specifications of LV Dual-Mode Stimulator.

Process	TSMC 0.18μm LV 1.8/3.3V CMOS process
Stimulator Type	Monopolar Biphasic Constant Current/ Voltage Stimulator
Device	1.8V/ 3.3V LV MOS
Supply Voltage	1.8 V/ ±3V/ ±6V
Stimulation Current Amplitude (@1kΩ)	0.2mA ~ 3.6mA (0.2mA per step)
Stimulation Voltage Amplitude (@1kΩ)	0.2V ~ 3.6V (0.2V per step)
Channel Numbers	8 channels x 2 leads
Pulse Width	20 ~ 450 μs
Stimulation Period	4 ~ 500 ms (2~250Hz)
Output Load	Electrode model
Mismatch Current	Minimum
Mismatch Voltage	Minimum
Stand-by Power	Minimum
Residual DC Current	Minimum

2.2 Specifications of LV Dual-Mode Stimulator

Table 2.3 shows specifications of the LV dual-mode stimulator. The stimulator is a monopolar biphasic dual-mode stimulator, which is able to deliver either constant current or constant voltage to the output. It has 16 channels in total, 8 channels on each lead. It is fabricated in TSMC 0.18-μm LV 1.8/3.3V CMOS process, which provides transistors with voltage tolerance 1.8V+10%=1.98V and 3.3V+10%=3.63V, due to requirement for cooperating with other circuit blocks in the whole SoC.

Since biphasic monopolar structure is selected in this work, both positive and negative voltage are required. All of the voltages are supplied by power supplies when

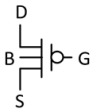
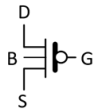
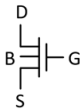
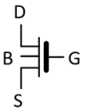
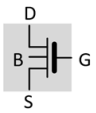
the stimulator is under measurement independently, and SoC is supposed to provide them by power management units when implanted.

The output load 1kΩ is estimated by resistance of human body. Due to the voltage tolerance of 3.63V in transistors, output stimulus current should be carefully scaled down when output load is over 1kΩ.

2.3 Design of LV Dual-Mode Stimulator Circuit

2.3.1 Brief Introduction and Constraints of 0.18μm 1.8V/ 3.3V LV CMOS process

Table 2.2 Symbols of different MOSFETs in 0.18μm1.8V/ 3.3V LV CMOS process.

	PMOS		NMOS		
Device Type	1.8V	3.3V	1.8V	3.3V	3.3V_DNW*
Symbol					
Voltage Tolerance for V_{DS} and V_{GS}	1.8V +10%	3.3V +10%	1.8V +10%	3.3V +10%	3.3V +10%

*DNW: Deep N-Well (biased to highest voltage of the device)

The process adopted for this work is TSMC 0.18μm 1.8V/ 3.3V LV CMOS process. Table 2.2 shows the symbols used in this work to indicate different types of MOSFETs. To summarize, there are two thicknesses of gate oxide which give voltage tolerance of 1.8V+10% and 3.3V+10%. That is, voltage between any two terminals in 1.8V/ 3.3V MOSFETs should be under 1.98V/ 3.63V for reliability concern. Owing to consideration of being integrated into SoC, the p-substrate is grounded. However, negative voltages exist in this work; therefore, to prevent forward leakage, PMOS is avoided to be used under negative voltage situations even when the bulk of it is biased

to ground. As for NMOS, deep N-well layer is provided to separate the p-substrate and p-well in NMOS.

2.3.2 Architecture

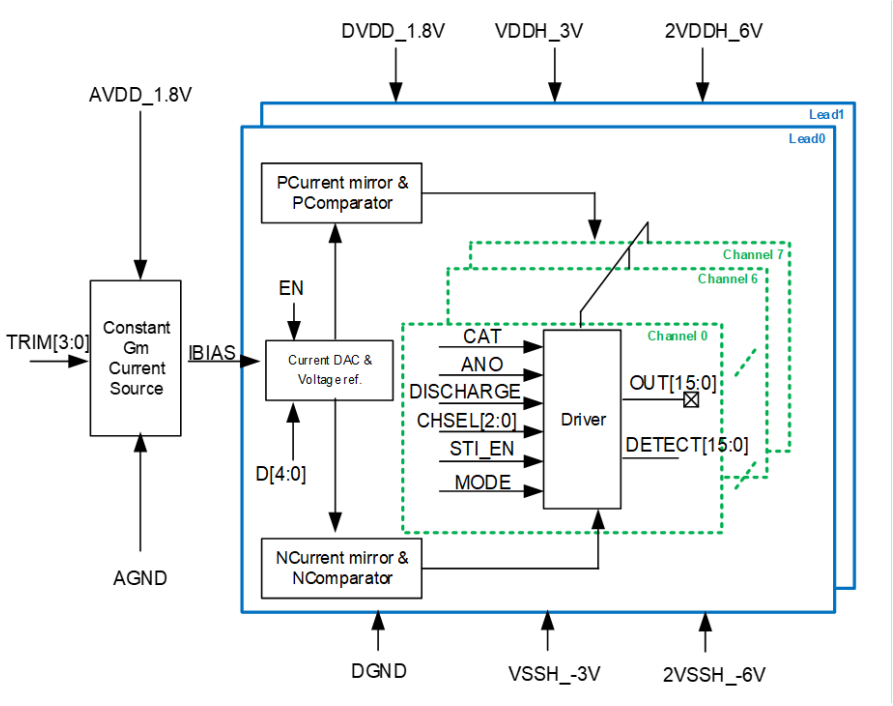
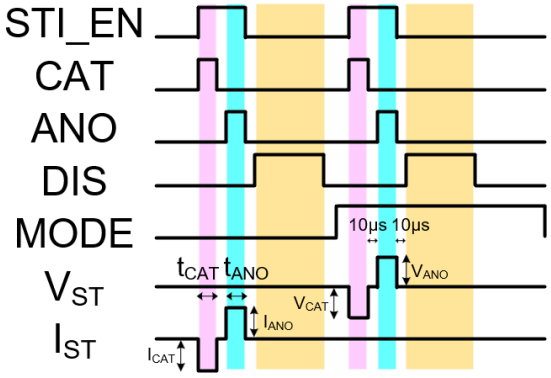


Fig. 2.3 Block diagram of LV dual-mode stimulator.

Fig. 2.3 shows an overview of this work. There are 8 channels per lead, 16 channels in total. In order to produce the reference current and reference voltage for current mode and voltage mode, a constant gm circuit is needed to create a stable bias voltage IBIAS. TRIM[3:0] are control signals designed for adjusting current accuracy due to process variation. After receiving IBIAS, a digital to analog converter (DAC) and voltage reference circuits generate the required amount of reference current and voltage by given amplitude control signals I[4:0]. Then, the reference current is multiplied by 100 times to the stimulus driver by the current mirror. Moreover, the reference voltage is sent to the comparator to compare with the feedback output voltage.

STI_EN is logic high when the stimulation is on, and the channel selected by 3-bit pin CHSEL[2:0] will deliver biphasic pulses. The STI_EN signal also controls whether the detect mode is on for the AFEA circuit to sense signals received from the output. The type of stimulation is decided by cathodic (CAT), anodic (ANO), discharge (DISCHARGE), and current or voltage mode (MODE) signals. Fig. 2.4 shows how the control signals work and the expected output waveform.



Amplitude I[4:0]	Stimulus Current I_{ST}	Stimulus Voltage V_{ST}
00001	0.2 mA	0.2 V
00010	0.4 mA	0.4 V
00011	0.6 mA	0.6 V
...	... (0.2 mA/ per step)	... (0.2 V/ per step)
10010	3.6 mA	3.6 V

Fig. 2.4 Control signals and output waveform of LV dual-mode stimulator.

2.3.3 Constant-Gm Reference Circuit

Because this work requires accurate output current and voltage for stimulation, it is necessary to design a constant-gm circuit to provide a stable current source for the following DAC and supply other parts of this stimulator with bias voltages that are required. The circuit is shown in Fig. 2.5, and it is designed by means of that presented in [21]. To begin, all MOSFETs should operate in strong inversion and satisfy square law, and the sizes of Mp1 and Mp3, which is a pair of the current mirror, are equal to generate the same current value I_{ref} so that

$$I_{ref} = I_{DS.Mp1} = I_{DS.Mp3} = I_{DS.Mn2} = I_{DS.Mn4} \tag{2.1}$$

After that, the size of Mn4 is designed to be 4 times larger than Mn2 in order to get half overdrive voltage than that of Mn2; that is,

$$(\frac{W}{L})_{Mn4} = 4(\frac{W}{L})_{Mn2} \tag{2.2}$$

If square law is satisfied, then

$$V_{OV.Mn4} = \frac{V_{OV.Mn2}}{2} \tag{2.3}$$

R1 to R5 are designed for trimming to deal with non-negligible process variation of resistors. For readability consideration, R is defined as total resistance after trimming is done. Since the voltage across R is

$$V_{OV.Mn2} - V_{OV.Mn4} = \frac{V_{OV.Mn2}}{2} \tag{2.4}$$

Equation (2.3) becomes

$$V_{OV.Mn4} = \frac{2I_{DS.Mn4}}{gm_{Mn4}} = \frac{V_{OV.Mn2}}{2} = I_{DS.Mn4} \cdot R \tag{2.5}$$

After rearranged, equation (2.5) leads to a conclusion that

$$gm_{Mn4} = \frac{2}{R} = constant \tag{2.6}$$

In other words, the current flowing out through Mn4 has the characteristics of gm equaling to a constant under any CMOS process, corner, temperature, and supply voltage variation. Also, the current has a fixed gm; therefore, it can ensure a relatively stable bandwidth when designing the amplifier, such as comparators in this work. The reference current value set in this work is 2μA, which is $\frac{1}{100}$ of the minimum amplitude for stimulation, 0.2mA. A start-up circuit is designed to avoid the zero-current condition.

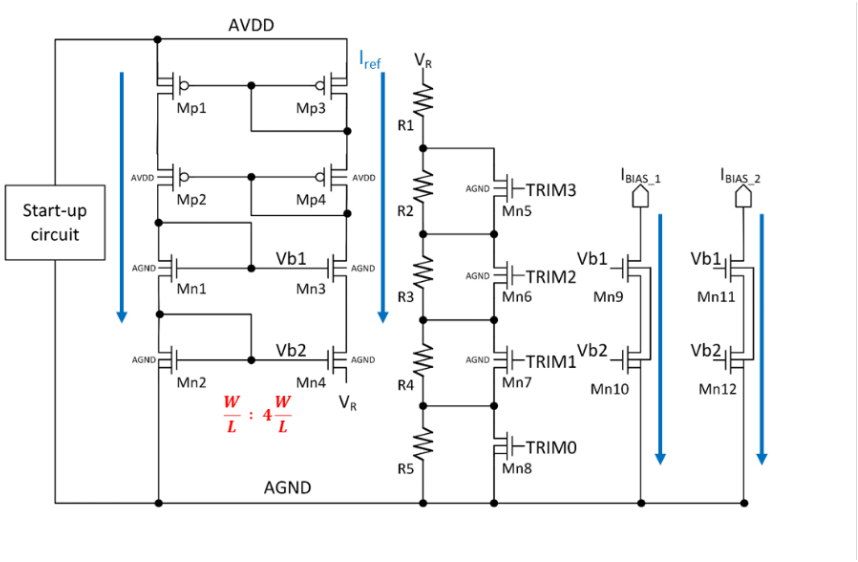


Fig. 2.5 Circuit of constant-gm reference.

2.3.4 DAC for Current and Voltage Reference

A binary-weighted current-switching DAC [23] is designed for generating output reference current which is decided by amplitude control signal D[4:0]. It is a cascode structure that gives high accuracy; nevertheless, the headroom voltage is limited. The reference current will be

$$I_{DAC} = IBIAS \cdot (D0 + 2 \cdot D1 + 2^2 \cdot D2 + 2^3 \cdot D3 + 2^3 \cdot D4) \qquad (2.7)$$

Furthermore, using only one DAC, which is illustrated in Fig. 2.6, for both cathode and anode mode aims to achieve a smaller mismatch rate. The bias voltages B1 and B2 are given by constant gm circuit, and so does the current source IBIAS. An enable control signal $\overline{EN}$ is designed in order to turn off the DAC when no stimulation is needed so that tissues are protected from the unexpected current. In addition, due to the need for high accuracy and matching, cascode structure is chosen, and dummy MOS and guard ring protection are implemented during layout.

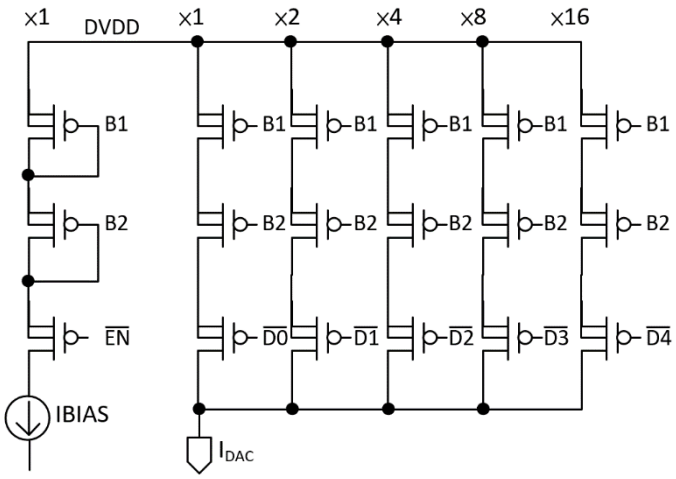


Fig. 2.6 The circuit of DAC for current and voltage reference.

2.3.5 Current Mirror for Current Mode and Voltage Reference for Voltage Mode

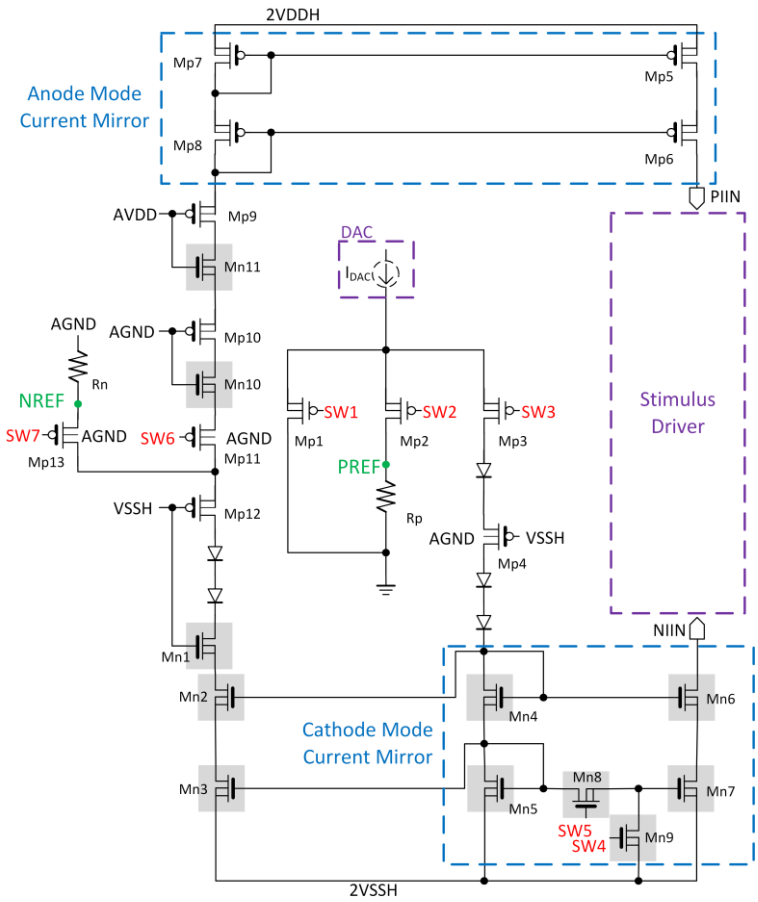


Fig. 2.7 The circuit of current mirror for current mode and voltage reference for voltage mode.

I_{DAC}, reference current sent by DAC, is delivered to the circuit illustrated in Fig. 2.7. Through operations of control switches SW1~SW7, current sources for current

mode stimulation and voltage references for voltage mode stimulation are able to be generated, respectively. The operating status of the switches is shown in Table 2.3.

Transistors used have at most 3.3+10%=3.63V constraint in the drain to source voltage; as a result, diodes and pairs of PMOS and NMOS such as Mp9 and Mn11 biased in different voltage range are applied to prevent overstress problem. During current mode stimulation, I_{DAC} is multiplied by 100 times through anode mode or cathode mode current mirror to generate current source PIIN or NIIN. Since the accuracy of output current should be as high as possible, a method of 2-dimension common centroid is applied on all the transistors of current mirrors for matching properties, and cascoded current mirrors are used in the layout. To avoid unwanted current from leaking into the driver, SW4 and SW5 are designed to turn off the cathode mode current mirror when it is not in cathode-current mode.

On the other hand, during voltage mode stimulation, reference current runs through either resistor Rp or Rn, so that voltage reference PREF or NREF for feedback comparators can be produced. Due to the fact that resistors are sensitive to process variation, matching factors should be carefully considered while layout for accuracy. For instance, dummy resistors are added.

Table 2.3 Status of switches in the circuit of current mirror and voltage reference.

Switches That are Turned Onc	**Current Mode**	**Voltage Mode**	**High-Z Mode**
Cathode Stimulation	SW3, SW5	SW3, SW4, SW7	SW1, SW4
Anode Stimulation	SW3, SW4, SW6	SW2	
Switches that are not mentioned are off.			

2.3.6 Stimulus Driver

The structure of the stimulus driver in this work is illustrated in Fig. 2.8. Current sources PIIN and NIIN are generated by current mirrors described in section 2.3.5, and also are the reference voltage pref and nref. The main job of this driver is to output the required stimulation current or voltage to the tissue.

There are 4 statuses which are anode mode, cathode mode, high-Z mode, and detect mode switching in total. Furthermore, switches are controlled by level shifters in different power domains according to the selected status, and their states and the following output voltage are listed in Table 2.4 and Table 2.5. Especially, the state of detect mode has further operation that is designed in passive discharge circuit and is demonstrated in section 3.3.8.

Transistors Mp2, Mp3, Mn1 and Mn2 are stacked for gate-oxide overstress concern given that these devices have only 3.3V+10% tolerance, thus their V_{GS} are biased by proper voltage. SW1 – SW4 control Mp1, Mp4, Mn3 and Mn4 to deliver output current and output voltage; therefore, they are designed as power MOSFETs to obtain better driving ability.

For voltage stimulation, the resistors on output are added to sense the output voltage, send part of it to Pcomparator or Ncomparator, and compare it with reference voltage pref or nref in order to complete a feedback loop during voltage mode. Thus, switch SW5 is turned on only in voltage mode; otherwise, SW5 is turned off to block current leakage. In this case, the ratio of feedback resistors is set to 4 to prevent overstress in Mp7 and Mp8. Moreover, SWP and SWN are set to turn off Mp5 to block unwanted output from Pcomparator or Ncomparator.

High-Z mode is designed for avoiding leakage current when the present channel is not assigned for stimulation, then every switch is turned off to obtain high impedance.

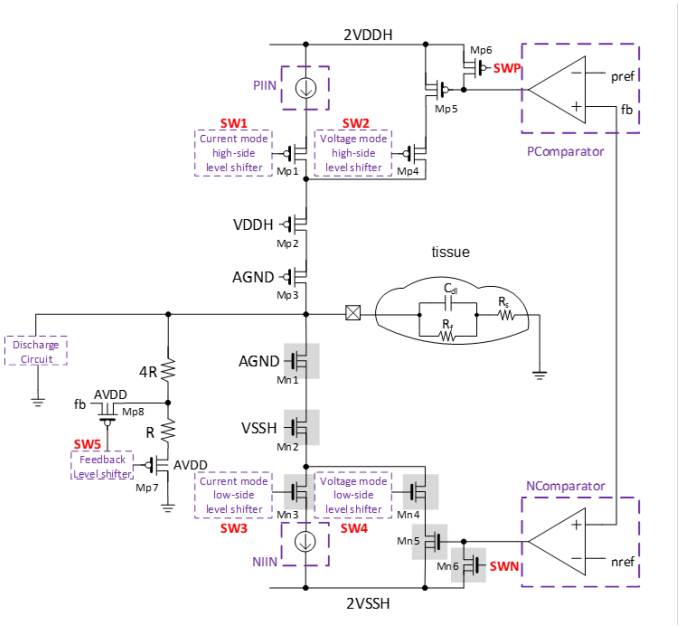


Fig. 2.8 The circuit of stimulus driver.

Table 2.4 Status of switches in the circuit of stimulus driver.

Switches That are Turned On	**Current Mode**	**Voltage Mode**	**High-Z Mode**	**Detect Mode**
Cathode Stimulation	SW3, SWP	SW4, SW5, SWP	SWP, SWN	SWP, SWN (extra switches illustrated in passive discharge circuit)
Anode Stimulation	SW1, SWN	SW2, SW5, SWN		
Switches that are not mentioned are off.				

Table 2.5 Voltages of control signals of switches.

Voltage of switches	**SW1**	**SW2**	**SW3**	**SW4**	**SW5**	**SWP**	**SWN**
On	VDDH	VDDH	VSSH	VSSH	VSSH	VDDH	VSSH
Off	2VDDH	2VDDH	2VSSH	2VSSH	AVDD	2VDDH	2VSSH

2.3.7 Comparators

The circuits of P-comparator and N-comparator are illustrated in Fig. 2.9 and Fig. 2.10, respectively. They compare the feedback voltage divided by ratio of feedback

resistors with reference voltage pref or nref generated by the circuit in chapter 2.3.5 and deliver output swings of VDDH to 2VDDH or VSSH to 2VSSH to control the current flowing into the stimulus driver. Since the current flowing in this operational amplifier (OPA) is not necessary to be an accurate value, the bias voltages can be generated by the constant-gm circuit which is already in this work instead of creating its own circuit for bias voltages.

For P-comparator, the reason that the source voltage of Mn5 and Mn6 is connected to VSSH rather than ground is to avoid them from getting into the triode region when the input is about ground level, and so is the reason for biasing AVDD at the source of Mp1 and Mp2 in N-comparator. Mn1, Mn2, Mn3, and Mn4 in P-comparator are stacked with their gates biased to VDDH or ground in order to prevent all transistors from gate-oxide overstress problem, and diodes added in N-comparator are also designed for this consideration.

The capacitors loaded on outputs aims to enhance the stability such as the phase margin of these two OPAs. At last, the bodies of Mp5 and Mp6 in N-comparator are grounded as a result that PMOS is not allowed to have a negative bulk voltage as it has been mentioned in chapter 2.3.1. If so, grounded p-substrate and negative n-well in PMOS will form a p-n junction forward-leakage route.

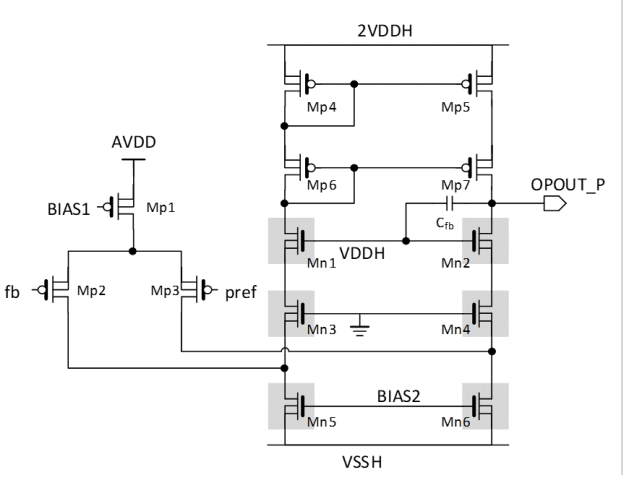


Fig. 2.9 The circuit of P-comparator for voltage feedback.

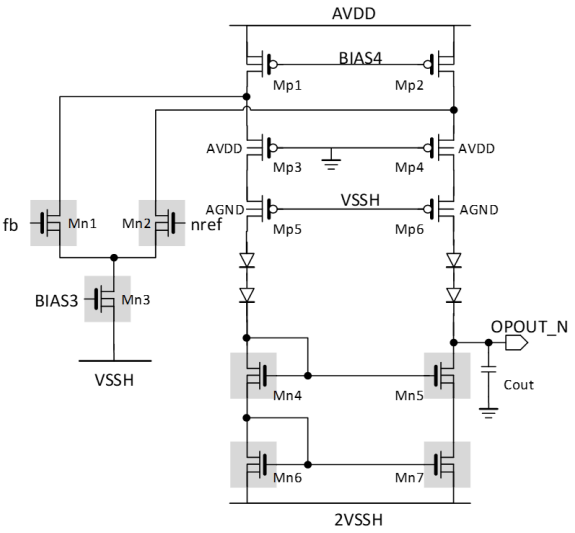


Fig. 2.10 The circuit of N-comparator for voltage feedback.

2.3.8 Passive and Active Discharge Circuit

If the charge cannot be balanced after cathode and anode stimulation, the residual charge left on the capacitor of the tissue model (C_{dl}) may cause safety issues because of leakage current. In actual situations, due to process variations, no matter how careful the design is, the current and duration of cathode and anode stimulation are not possible to be perfectly matched. In brief, passive discharge circuit discharges left charge directly to the ground; in contrast, active discharge circuit senses voltage on output pad with a close loop and feedback with an amount of charge in opposite voltage polarity to speed up the discharge process.

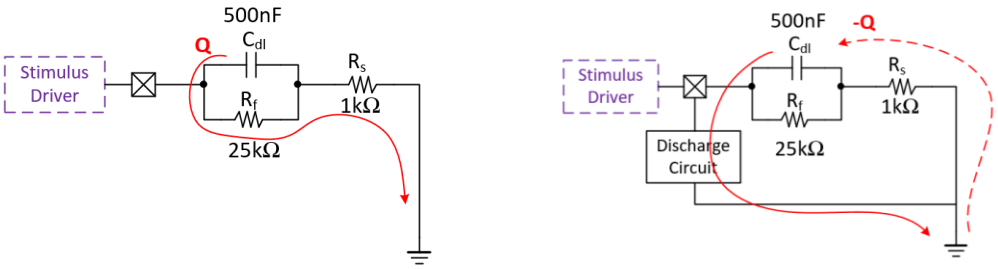
Discharge current paths with and without a discharge circuit are shown in Fig. 2.11. When there is no discharge circuit added, the discharge time constant is

$$\tau_{w/o\ discharge} = C_{dl} \times \left(R_f + R_s\right) = 13ms \tag{2.8}$$

If a discharge circuit is attached, C_{dl} can be directly discharged to the ground and the path will not pass the large resistance R_f. Thus, the new discharge time constant will become

$$\tau_{w/i\ discharge} = C_{dl} \times R_s = 0.5ms \tag{2.9}$$

It implies that a discharge circuit is important and can shorten the discharge time, protecting tissue from damage.



(a) (b)

Fig. 2.11 Discharge current path of circuit (a) without discharge circuit (b) with discharge circuit.

The structure of the passive discharge circuit is shown in Fig. 2.12, which is of the concept of that presented in [20]. It contains one PMOS and one NMOS only and does discharge by passing the remaining charge to the ground. Furthermore, the connection of bodies is designed so that parasitic diodes can work for avoiding current leakage.

All operations of different modes are illustrated in Table 2.6. Mp and Mn serve as a bidirectional switch that connects tissue with the ground. The gate voltages of Mp and Mn are set to 0V so as to turn off this circuit for no leakage current whether in anode-mode stimulation or cathode-mode stimulation. Moreover, during discharge mode, the voltage of output is around zero level. The channel that is currently selected to stimulate turns Mp and Mn on and directly leads the output pad to the ground for discharging. For other channels that are not selected for stimulation, Mn is still turned off since the voltage between the output pad and gate voltage will not be over the threshold voltage. Last, the signal sensed from the output pad should be delivered to the analog front-end amplifier (AFEA) circuit on the SoC; thus, Mn is turned off to block the output pad from the ground to avoid current leakage. Besides, the artifact received from the output

pad is around 0V, so it can be sent to AFEA through Mp, which has the gate voltage of -3V, to complete the function of closed-loop SoC.

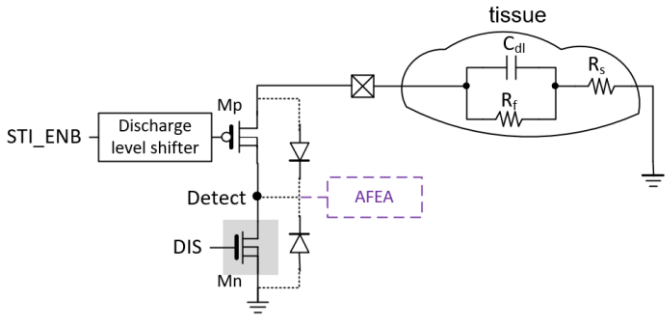
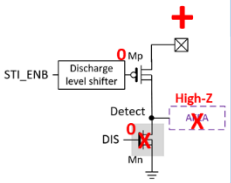
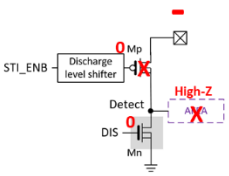
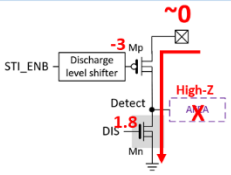
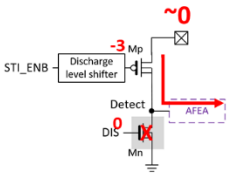
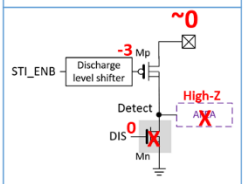


Fig. 2.12 Passive discharge circuit.

Table 2.6 Operation of the passive discharge circuit in different modes.

	Stimulation/ High-Z Mode		Discharge Mode	Detect Mode (STI_EN = 0)
	Positive Output	Negative Output		
Selected Channel				
Others (Unselected) Channels				

The structure of the active discharge circuit, which is also presented in the thesis [20], is depicted in Fig. 2.13. In comparison with passive discharge, the active discharge circuit can discharge the residual charge of the capacitor by actively compensating the voltage of the opposite polarity. Therefore, the process of active discharge can be faster than that of passive discharge. The disadvantage of it is to consume more power because of the comparator and the push-pull circuit in it. When there is a positive residual charge on C_{dl}, Mn1, Mn2, Mp1, Mp2, and Mp3 are turned on that voltage on the output pad can be compared with the ground by the comparator. Then, when the gate-source

voltage of Mp3 reaches the threshold voltage, Mp3 draws a current from the output pad to VSSH (-3V) to balance the positive charge. On the contrary, if a negative residual charge is left on C_{dl}, Mn5 draws a current from VDDH (+3V) to the output pad to balance it. The sizes of Mn5 and Mp3, which form a push-pull circuit, are designed for a bigger size to speed up the discharging process. If the discharge mode is off, Mn3, Mn4, and Mn5 are turned on and the comparator is turned off for stability. It is noteworthy there is a passive discharge path marked in this figure, the control circuit is designed to also do passive discharge by this circuit in chapter 3 and the measurement results are shown in chapter 3.5.3.

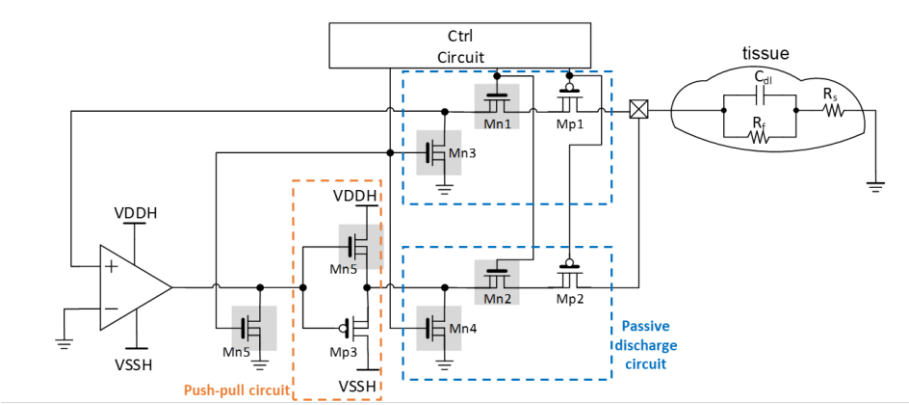


Fig. 2.13 Active discharge circuit.

2.4 Simulation Results

The output load used in both simulation and measurement is shown in Fig. 2.14, which is the electrode-tissue model mentioned in chapter 1.3. The value of C_{dl}, R_f, and R_s are extracted to discrete components based on real situation. Following simulation and measurement results are all measured based on this output load, while stimulus current output results are obtained by V_s divided by R_s (1kΩ).

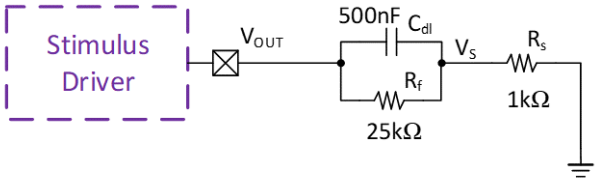


Fig. 2.14 Output load of the stimulator.

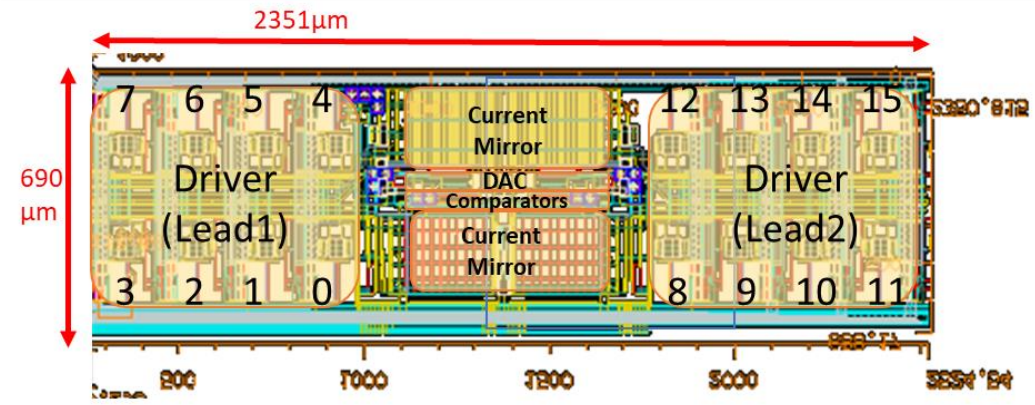


Fig. 2.15 Layout photo of LV Dual-Mode Stimulator.

The photo of layout is shown in Fig. 2.15, and the total area is 2351µm *690µm. Stimulus drivers are placed symmetrically, and current mirrors are drawn as the way to draw power transistors due to the large size.

As depicted in Fig. 2.16, the stimulator is able to deliver biphasic pulses to the selected channel dependent on the 3-bit signal CHSEL[2:0]. In addition, when the driver is in high-Z state, the output pad of it may be coupled by output voltage from other channel to -3.6V~3.6V. To verify whether this high-Z state has worked, Fig. 2.17 shows the setup that an ideal voltage source is applied at the output pad to generate a biphasic pulse ranging from -3.6V to 3.6V. Waveforms of voltages between any 2 terminals of 3.3V devices are all proved to not exceed the tolerance limit (3.3V+10%).

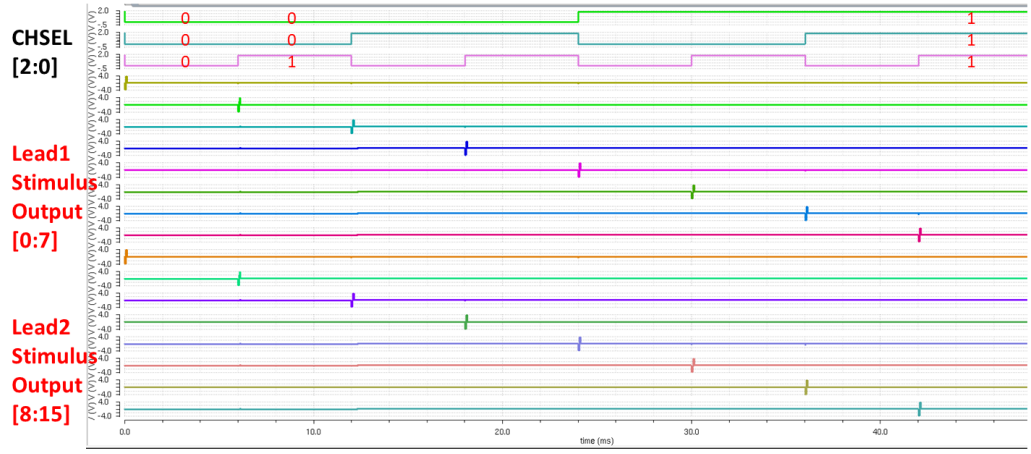


Fig. 2.16 Simulation results of stimulus output while tuning CHSEL[2:0].

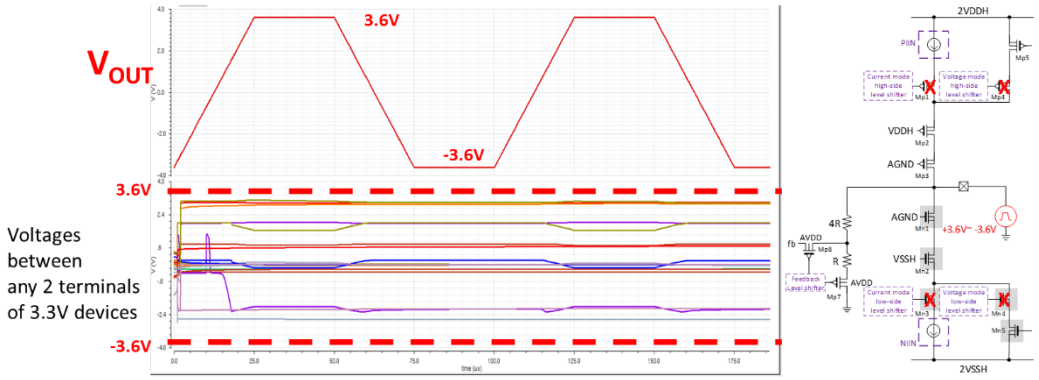
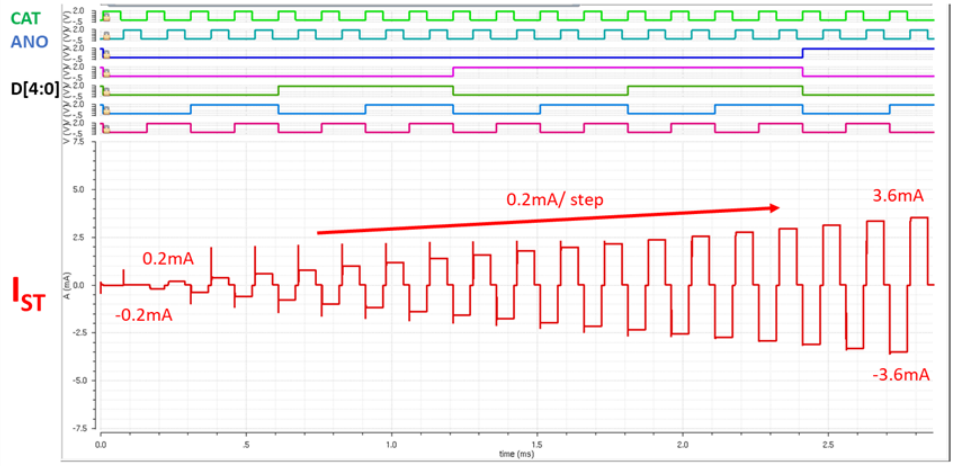


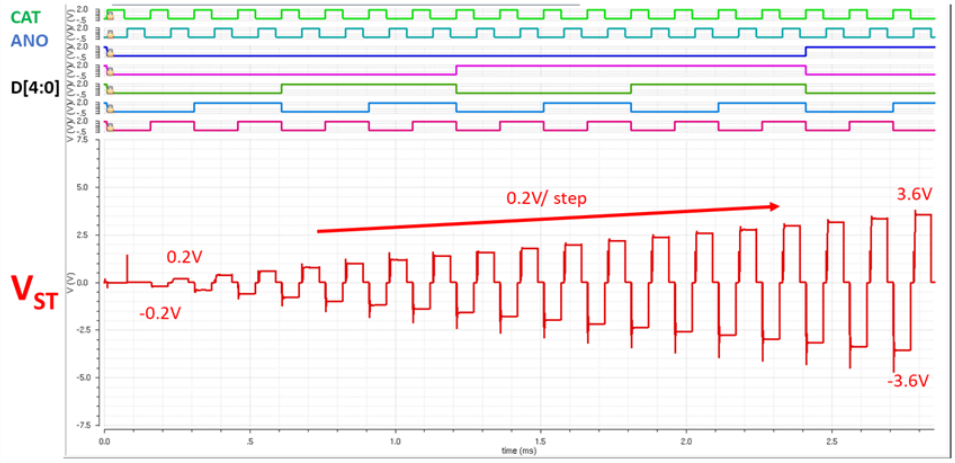
Fig. 2.17 Overstress test under high-Z mode.

2.4.1 Current and Voltage Mode

The specification of current/ voltage amplitude is from 0.2mA/ V to 3.6mA/ V and -0.2mA/ V to -3.6mA/ V with 0.2mA/ V per step by tunable signal D[4:0]. Fig. 2.18 shows stimulus output current and voltage in full scale of this work, and Fig. 2.19 and Fig. 2.20 show influence of process variation in constant-gm circuit and current mirrors, which are usually sensitive for accuracy, under Monte Carlo simulation. 50 times of Monte Carlo simulation are run using the largest amplitude in current mode or voltage mode, it can be observed that the results are stable under process variation.

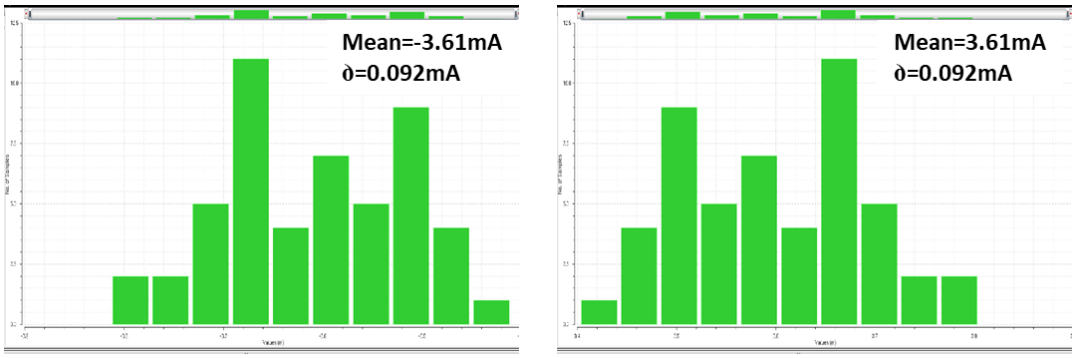


(a)



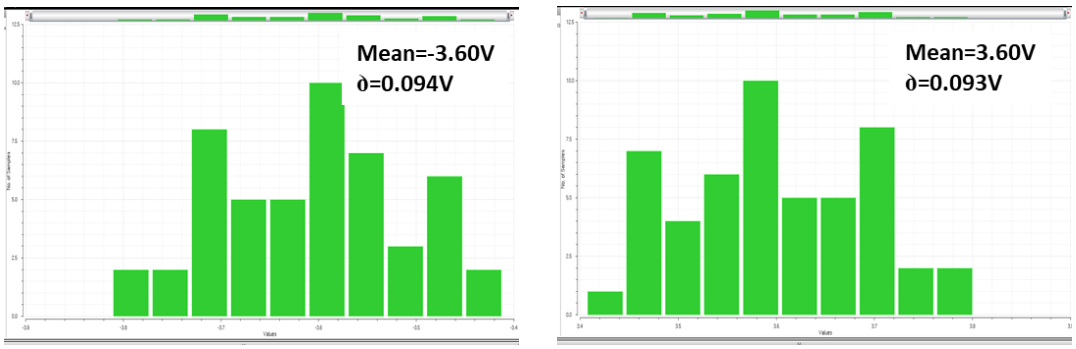
(b)

Fig. 2.18 Post-layout simulation result of (a) current-mode (b) voltage-mode output for tunable amplitude test of LV dual-mode stimulator.



(a) (b)

Fig. 2.19 Charts of running 50 times Monte Carlo simulation in largest current amplitude (3.6mA) during (a) cathode mode (b) anode mode.



(a) (b)

Fig. 2.20 Charts of running 50 times Monte Carlo simulation in largest voltage amplitude (3.6V) during (a) cathode mode (b) anode mode.

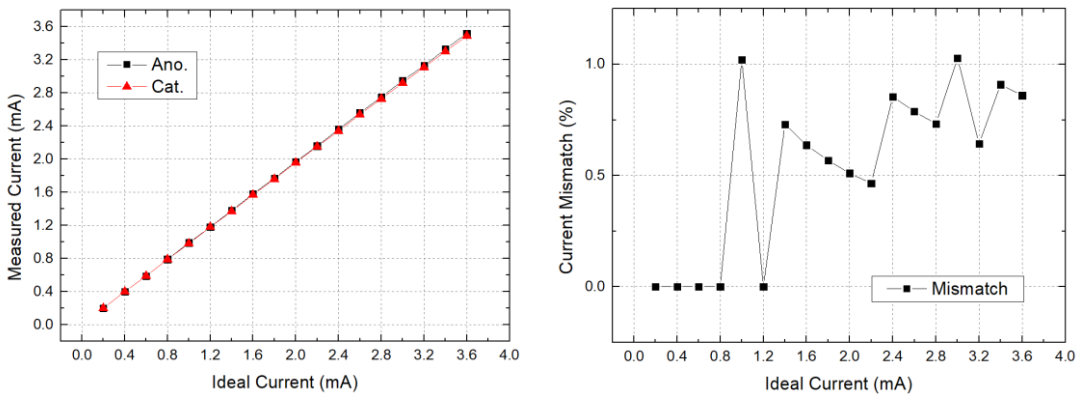
All the stimulus output values and mismatches are sorted into Fig. 2.21. The current mismatch and voltage mismatch are defined by equation 2.10 and equation 2.11.

$$Current\ \ Mismatch\ \ (\%) = \frac{|I_{ANO}|-|I_{CAT}|}{|I_{CAT}|} \times 100\ \ (\%) \tag{2.10}$$

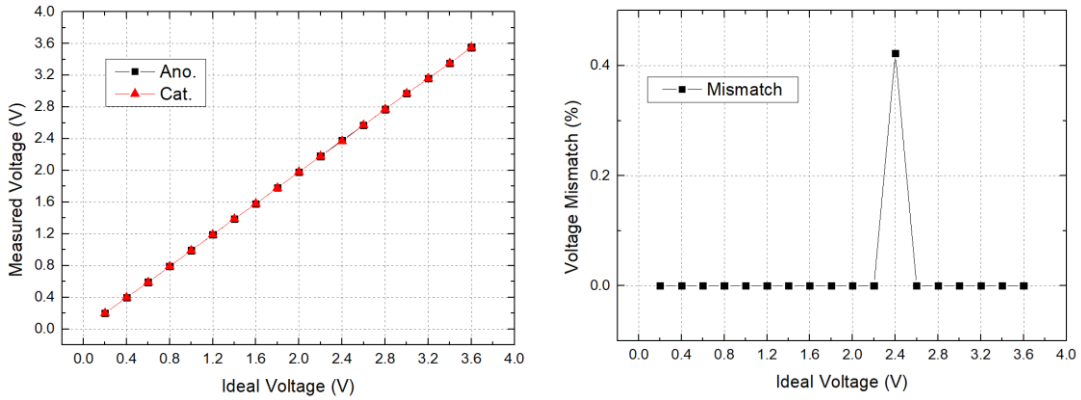
$$Voltage\ \ Mismatch\ \ (\%) = \frac{|V_{ANO}|-|V_{CAT}|}{|V_{CAT}|} \times 100\ \ (\%) \tag{2.11}$$

The current mismatch in this work is under 1.02%, and the voltage mismatch in this work is under 0.42%.

Furthermore, the overstress issue also needs to be tested during stimulation process. As it is shown in Fig. 2.22, voltages between any 2 terminals in both current-mode stimulation and voltage-mode stimulation are in the tolerance range of ±3.6V.

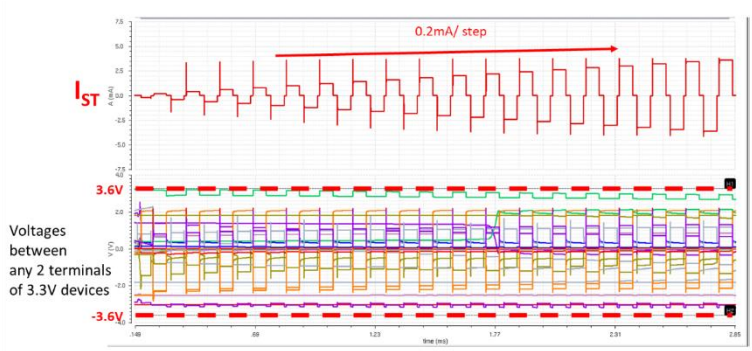


(a)

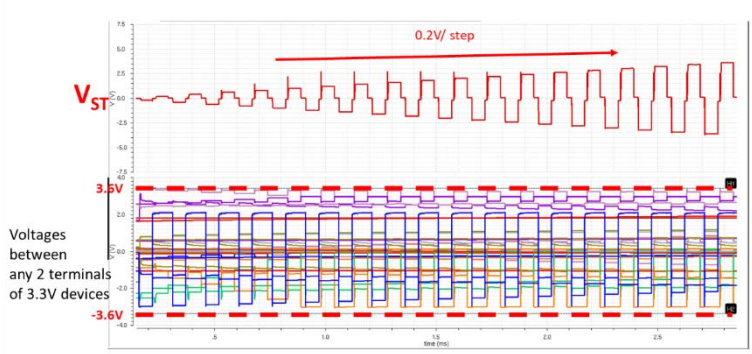


(b)

Fig. 2.21 Post-layout results of (a) current (b) voltage mismatches of LV dual-mode stimulator.



(a)



(b)

Fig. 2.22 Overstress test under (a) current-mode (b) voltage-mode stimulation.

2.4.2 Detect Mode

The simulation setup for testing detect mode is shown in Fig. 2.23. A voltage source sending 0.2V peak-to-peak signal is added to output pad, and part of the circuit

of AFEA is connected to the detect point. Above all, it is necessary to be sure that signal sensed from output pad can well pass through Mp to detect point. Secondly, Mn should be turned off during detect mode to make sure there is no leakage to ground. As shown in the waveform, the signal of sine wave can be completely sent to detect point, and current passing Mn during detect mode is almost zero.

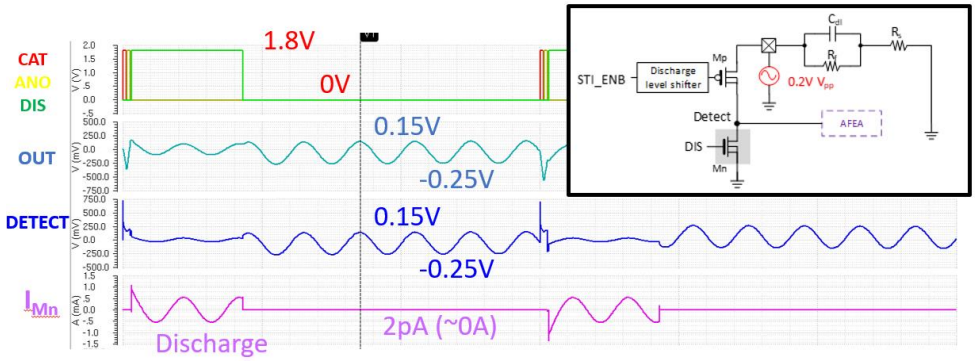
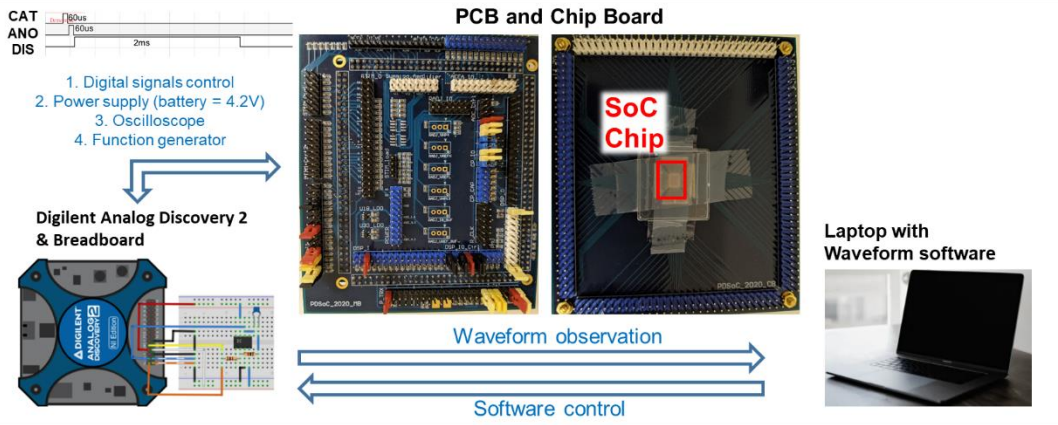


Fig. 2.23 Post-layout simulation result of detect mode.

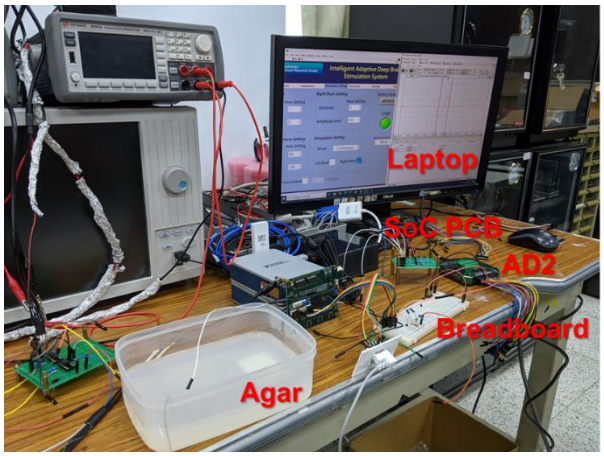
2.5 Measurement Results

The measurement setup of this work is depicted in Fig. 2.24 (a). Because this stimulator has been integrated on SoC, after checking the functions and output waveforms when all power supplies are given on chip by only sending a battery voltage of 4.2V matches the ones when power supplies are all supplied independently by Keysight B2902A precision source, measurement process can be simplified by controlling all the powers on SoC and only one power supply of 4.2V is needed. In addition, Digilent Analog Discovery 2 (AD2) is a measurement instrument with pocket size and can serve as power supply within ±5V, function generator, oscilloscope within ±25V and digital (logical) pattern generator of 0V and 3.3V; thus, waveform observation of this work can also rely on it due to the specification within ±3.6V stimulus output. For medical experiment and use, it is preferred for its portable characteristic and it only needs a breadboard to do calibration. Fig. 2.24 (b) shows the

practical measurement environment of this work. The agar is prepared for simulating animal experiment to see how the stimulation works on a real tissue.



(a)



(b)

Fig. 2.24 (a) The measurement setup of the LV dual-mode stimulator. (b) The practical measurement environment of the LV dual-mode stimulator.

Fig. 2.25 verifies that the frequency and duration time are accurate and are controllable.

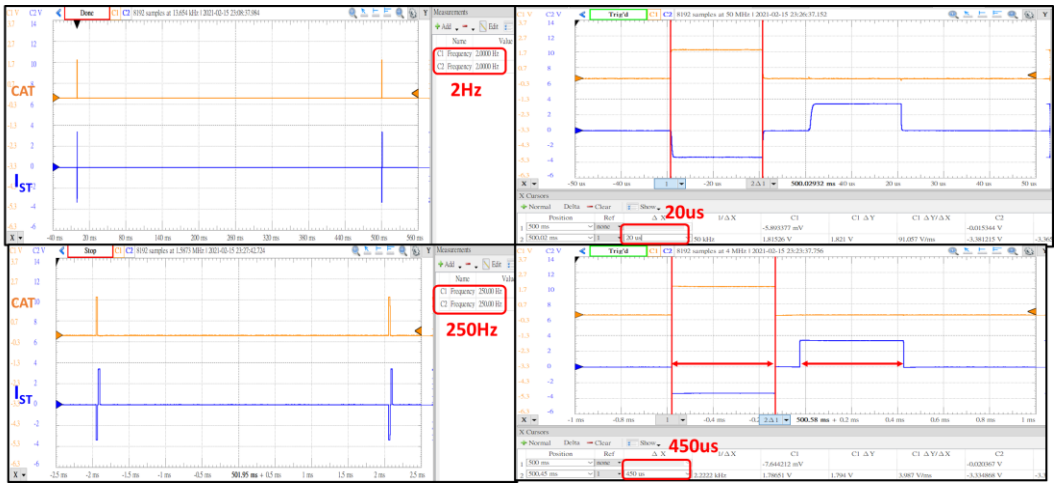


Fig. 2.25 The frequency and stimulation duration test of LV dual-mode stimulator.

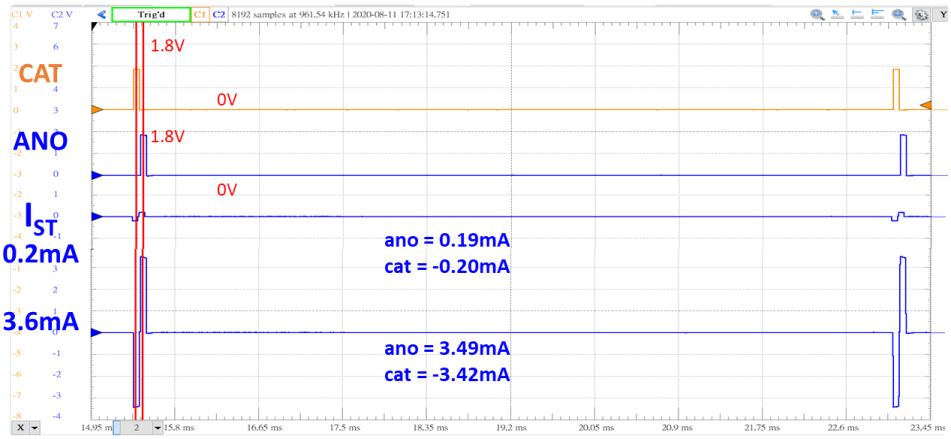
2.5.1 Current Mode and Voltage Mode

The stimulus output waveforms are shown in Fig. 2.26, and the results are measured with electrode-tissue model connected at output load. The current outputs are measured by the cross voltage on R_s (1kΩ), which can also be transferred to mA directly since 1V/ 1kΩ = 1mA. The CAT and ANO signals are set to 60μs and DIS signal is set to 2ms with 10μs delay between each signals, and the stimulation period is set to 6ms (about 166.67Hz).

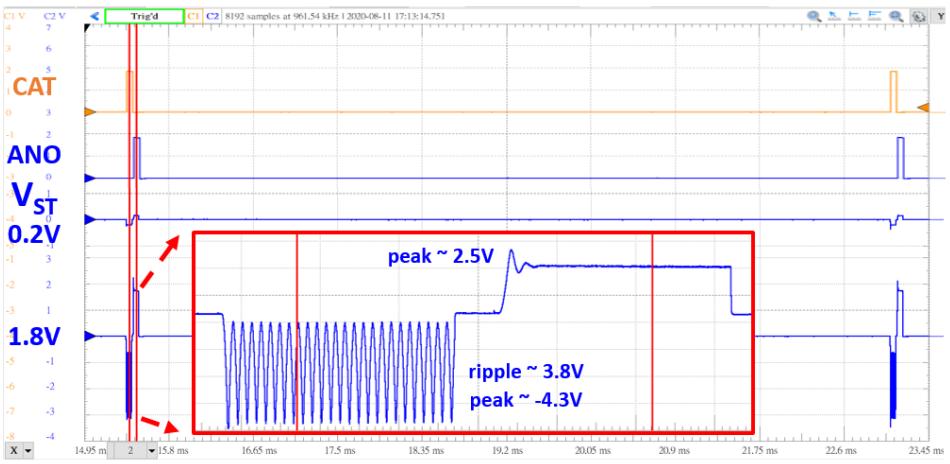
During current-mode stimulation, it can be seen from Fig. 2.26 (a) that this stimulator can give corresponding stimulation according to the CAT and ANO signals, and the output waveforms are symmetrical and clean. As for the voltage mode stimulation, the amplitude is chosen to stimulate only to 1.8V maximum because it is found that the output of the voltage stimulation has oscillation issue. If a higher voltage amplitude is selected, it will cause voltage overstress problems in the circuit (3.3V+10% tolerance). In Fig. 2.26 (b), it can be seen that the anode-mode stimulation can quickly become a stable output waveform. However, the peak voltage reaches about 2.5V (139% of desired voltage amplitude), while the stimulus output of the cathode-mode stimulation hardly converges, and its peak voltage reaches as high as 4.3V (239%

of desired voltage amplitude). The oscillation value in cathode-mode stimulation is about 3.8V. Although the problem of oscillation exists, the average voltage is still in line with the preset voltage amplitude. This problem will be sorted in chapter 3.5.4 with the measurement results of the HV dual-mode stimulator for further discussion.

All current output and voltage output are organized in Fig. 2.27, and the mismatches are calculated using equation (2.10) and equation (2.11). The mismatch of the current-mode stimulation is below 3.48%, and the mismatch of the voltage-mode stimulation is below 8.22% except for the ones in smaller voltage amplitude (0.2~0.4V) which is about 12.50%~21.05%. It is inferred that the circuit is not stable enough due to the oscillation of the voltage mode, and the output value of the small amplitude get a large mismatch value by slight difference. Detailed analysis and discussion of mismatch will be in the discharge mode section below.

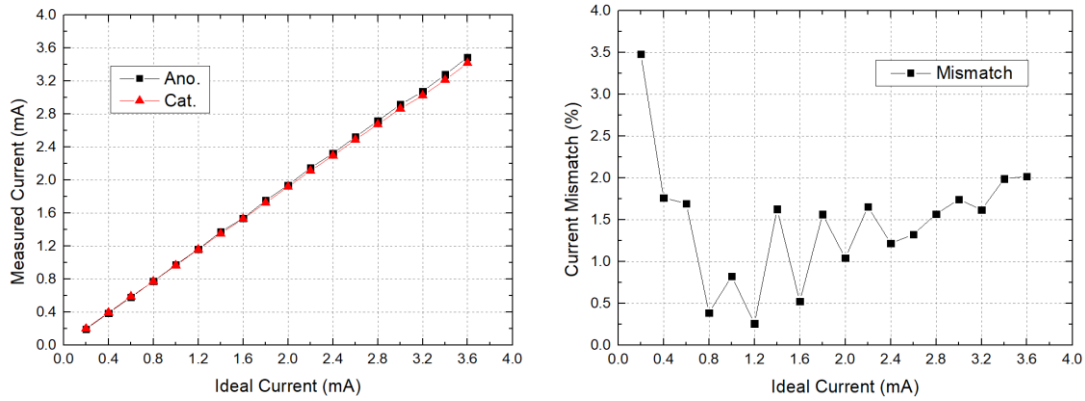


(a)

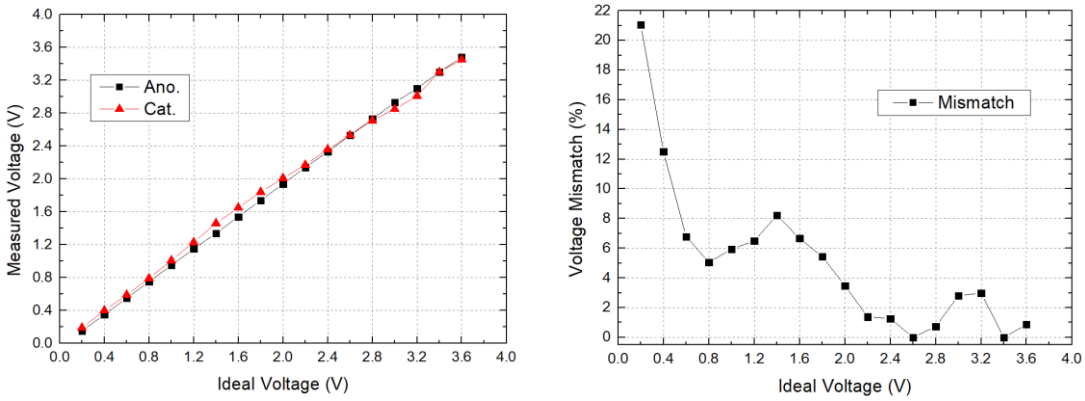


(b)

Fig. 2.26 The measurement results of (a) current-mode (b) voltage-mode stimulus output of LV dual-mode stimulator.



(a)



(b)

Fig. 2.27 The measurement results of (a) current (b) voltage mismatches of LV dual-mode stimulator.

2.5.2 High-Z Mode and Detect-Mode Circuit

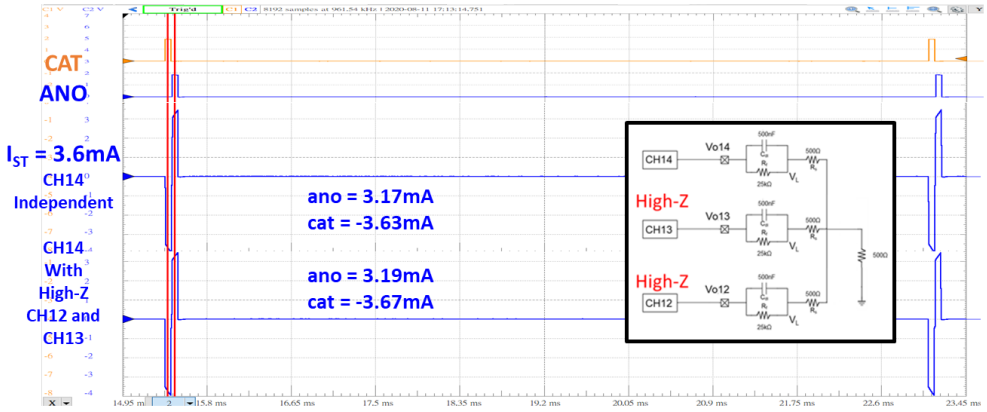


Fig. 2.28 The measurement results and setup of the high-Z mode test of LV dual-mode stimulator.

The measurement results and setup of high-Z mode are depicted in Fig. 2.28. Three channels, which in this measurement are chosen to be CH12~ CH14, are connected with each other through a 500Ω resistor and all connected to the ground with the same 500Ω resistor. This value for setup is obtained in the same way that extracts the electrode-tissue model. In this case, CH14 is selected to stimulate and the other channels should all in the high-Z mode. To verify the high-Z mode function, CH14 should not be affected by any unexpected current from the output pad. As shown in the waveform, the two stimulus output of CH14 stimulating independently and it stimulating with sharing output pad with other 2 channels are almost the same; therefore, it can be proved that high-Z mode works in the driver.

The measurement results and setup of the detect-mode circuit are illustrated in Fig. 2.29. Since the detect connection point connects to the AFEA circuit inside SoC, we can check the function of the detect-mode circuit when stimulation is on. AFEA is turned into the high-Z state when the STI_EN signal is on, which means that it is stimulating, and there will be no leakage current passing to the ground or AFEA circuit whether it is cathode-mode stimulation or anode-mode stimulation. As shown in the

waveform, the stimulus output in the 0.2mA amplitude connected with the AFEA circuit almost equals to the one not connected. Also, the waveforms in 3.6mA amplitude are consistent whether connected with the AFEA circuit or not. Therefore, the detect-mode circuit does not cause adverse effects on this work.

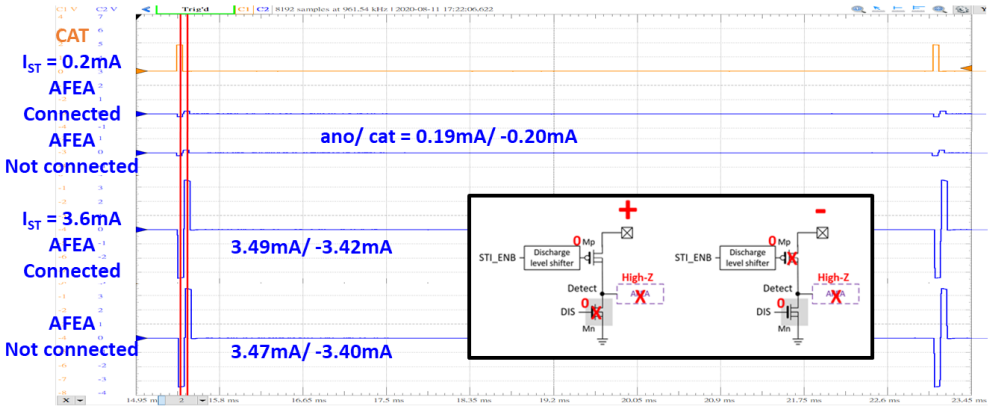


Fig. 2.29 The measurement results and setup of the detect-mode test of LV dual-mode stimulator.

2.5.3 Discharge Circuit

There are two focuses when it comes to safety issues on the double-layer capacitor C_{dl} of the electrode-tissue model. First, in safety rule ISO 14708-1, it has been mentioned that the direct current density at the surface of any conductive surface or electrode should be ≤ 0.75 μA/mm^2. In PD application, we use Medtronic model 3389, which is in the shape of a cylindrical electrode, and the area of each electrode is 1.27mm (diameter)×1.5mm (length)≈5.98mm^2. Therefore, the allowed residual current is 5.98 mm2×0.75μA/mm^2=4.49μA.

The other rule is that the residual charge on C_{dl} has a safety margin in different kinds of electrode metal materials, as listed in Table 2.7 [24]. The Medtronic model 3389 is made of platinum (Pt), which means the maximum residual charge should be 0.0598cm^2×(0.05~0.15)mC/cm^{-2}=2.99~8.97μC, and the potential limit is -0.6~0.8V.

Table 2.7 Charge-injection limit of electrodes of different materials. [24]

Material	Mechanism	Maximum Q_{inj} (mC cm^{-2})	Potential Limits V versus Ag|AgCl	Comments	References
Pt and PtIr alloys	Faradaic/capacitive	0.05–0.15	−0.6–0.8		71
Activated iridium oxide	Faradaic	1–5	−0.6–0.8	Positive bias required for high Q_{inj}. Damaged by extreme negative potentials (<−0.6 V)	72, 73
Thermal iridium oxide	Faradaic	~1	−0.6–0.8 V	Positive bias required for high Q_{inj}	74
Sputtered iridium oxide	Faradaic	1–5	−0.6–0.8 V	Benefits from positive bias. Damaged by extreme negative potentials (<−0.6 V)	75; S.F. Cogan, J. Ehrlich, T.D. Plante, A. Smirnov, D.B. Shire, M. Gingerich, J.F. Rizzo, unpublished
Tantalum/Ta_2O_5	Capacitive	~0.5		Requires large positive bias	76, 77
Titanium nitride	Capacitive	~1	−0.9 to 0.9	Oxidized at positive potentials	78
PEDOT	Faradaic	15	−0.9 to 0.6	Benefits from positive bias	79

The rule of allowed residual current can be verified with the worst case of mismatch charge, which is

$$\frac{(I_{ST}\times mismatch)_{max}\times duration}{period} \tag{2.12}$$

In this stimulator, the max residual current is

$$\frac{(3.418mA\times 2.02\%)\times 60\mu s}{6ms} = 690nA \leq 4.49\mu A \tag{2.13}$$

which passes the residual current limit.

However, when it comes to the residual charge, which is measured by V_{Cdl} and shown in Fig. 2.30, it is obvious that both discharge circuits can release much more amount of current than no discharge circuit added, and passive discharge circuit and active discharge circuit are about the same effect due to small mismatch in this stimulator.

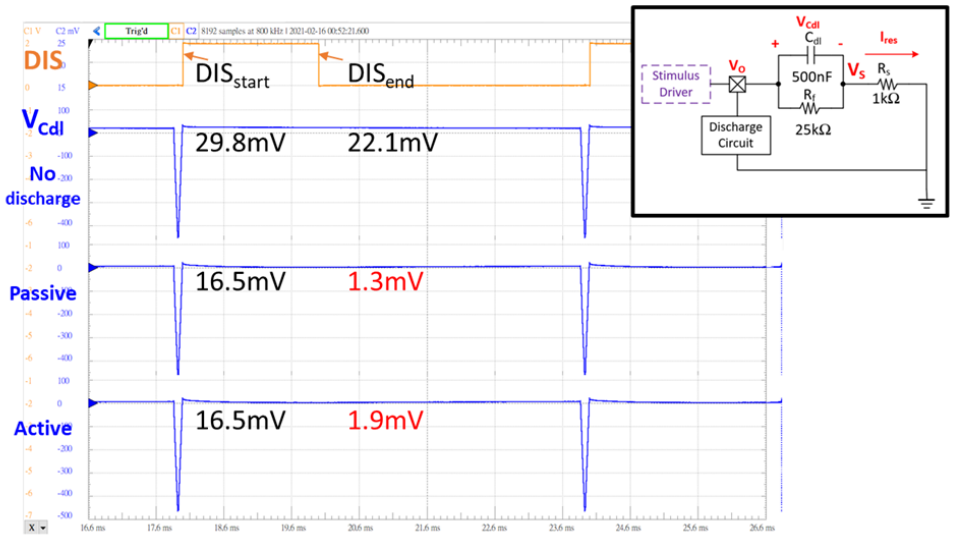
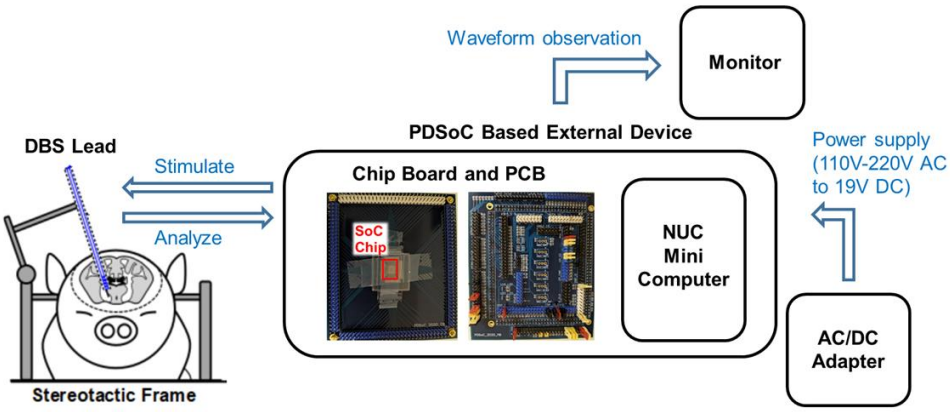


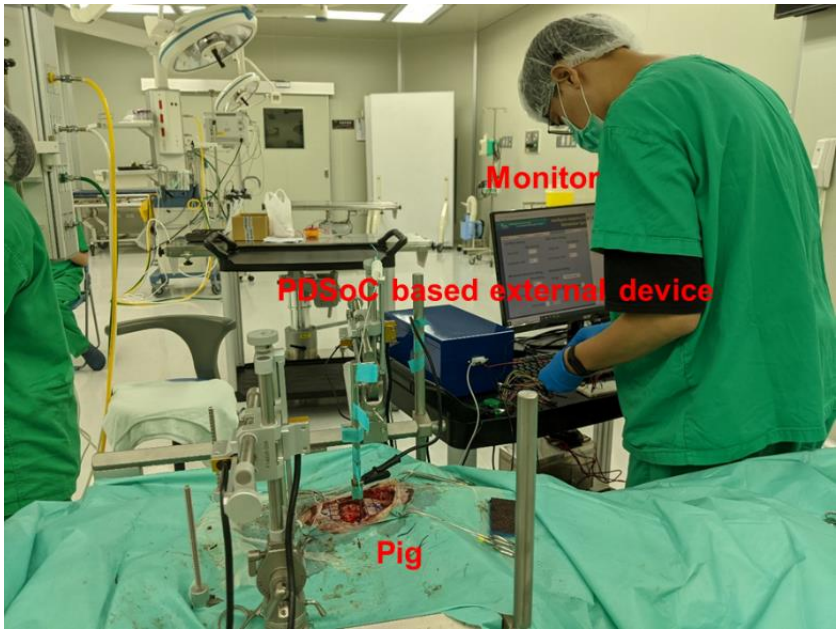
Fig. 2.30 The measurement results and schematic view of residual potential on C_{dl} of LV dual-mode stimulator.

2.5.4 Animal Experiment Results

The LV dual-mode stimulator has been integrated on the SoC and functions of current mode stimulation have been verified in animal experiment on Lee-Sung pigs. Fig. 2.31 are a block diagram of the experiment set up and a photo of the practical experiment environment.



(a)



(b)

Fig. 2.31 (a) The measurement setup of the animal experiment. (b) The practical measurement environment of the animal experiment.

As shown in Fig. 2.32, since the resistance of the pig brain is about 1~2k ohms, the stimulation current is set to 2.8mA to prevent damage to the components. To begin, the PDSoC-based external device uses a 1k ohm resistor to confirm the output current, and then the stimulus pulses are sent by electrode which is in advance input into the brain. After 30 minutes of continuous stimulation, the waveform is basically the same but the voltage at the output terminal increased, which is presumably caused by the change of the resistance of the pig brain and the faradic resistance on electrode. After the experiment, the pig brain was sliced and sent for safety test, which was at last passed.

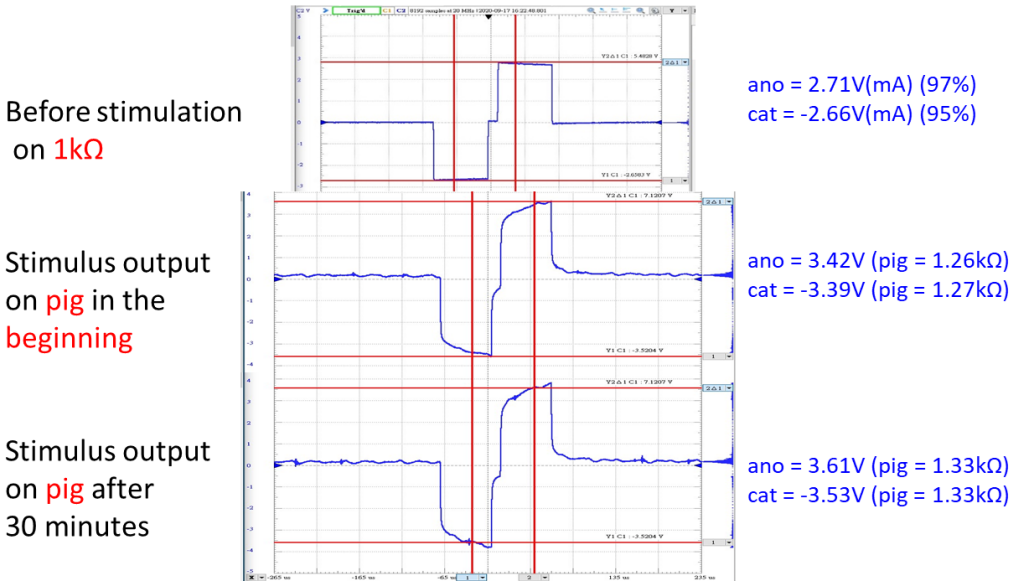


Fig. 2.32 The measurement results of current-mode output with stimulus current set to 2.8mA.

2.6 Summary

A LV monopolar biphasic dual-mode stimulator is fabricated in TSMC 0.18-μm LV 1.8/3.3V CMOS process is purposed and verified in measurement in this chapter. The comparison of the specification and results in pre-layout simulation, post-layout simulation, and measurement is listed in Table 2.8. The amplitudes drop from the ideal value in the specification as they go higher in post-layout simulation and measurement; therefore, the layout should be improved in DAC and current mirror to make the current and voltage reference more accurate. In addition, the current mismatch gets higher in measurement because of fabrication, and the voltage mismatch is much higher due to the unexpected oscillation. The current mismatch can be solved by charge balancing by discharge circuits; however, the oscillation problem in voltage-mode stimulation is still under investigation and will be discussed in chapter 3. The standby power cannot be calculated since this stimulator is already integrated on SoC.

The results comparison of this work with other presented stimulators are listed in Table 2.9.

Table 2.8 Comparison of results of LV dual-mode stimulator.

	Specification	Pre-sim	Post-sim	Measurement
Current mode/ CAT (@1kΩ) (mA)	-0.2 -1 -2 -3 -3.6	-0.20 -1.01 -2.01 -3.02 -3.62	-0.20 -0.98 -1.96 -2.92 -3.49	-0.20 -0.97 -1.92 -2.87 -3.42
Current mode/ ANO (@1kΩ) (mA)	0.2 1 2 3 3.6	0.20 1.01 2.01 3.02 3.62	0.20 0.99 1.97 2.95 3.52	0.19 0.98 1.94 2.92 3.49
Voltage mode/ CAT (@1kΩ) (V)	-0.2 -1 -2 -3 -3.6	-0.20 -1.00 -2.01 -3.01 -3.61	-0.20 -0.99 -1.98 -2.97 -3.55	-0.19 -1.01 -2.01 -2.85 -3.45
Voltage mode / ANO (@1kΩ) (V)	0.2 1 2 3 3.6	0.2 1.01 2.01 3.01 3.61	0.20 0.99 1.98 2.97 3.55	0.15 0.95 1.94 2.93 3.48
Step	0.2mA/ 0.2V			
Mismatch current (%)	minimum	<0.01%	<1.02%	<3.48%
Mismatch voltage (%)	minimum	<0.01%	<0.42%	unknown (oscillation)
Standby power	minimum	252.38uW	265.35uW	unknown (on SoC, not independent)

Table 2.9 Performance comparison of LV dual-mode stimulator with other works.

	[28] 2018 SSC-L	[29] 2013 TBioCAS	[31] 2018 JESCAS	This work Chapter 2
Technology	0.18µm HV	0.35µm HV	0.18µm LV	0.18µm LV
Stimulator Type	Monopolar CCS/CVS	Monopolar /Bipolar CCS	Bipolar CCS	Monopolar CCS/CVS
Number of Channels	1	2	N/A	16
Result Type	Measurement			
Stimulation Amplitude	0~10.2mA/ ±6V	0.032~1mA	0.2~3mA	±3.6mA/ ±3.6V
Resolution	32 steps (5-bit)	32 steps (5-bit)	7 steps (4-bit)	18 steps (5-bit)
Mismatch Current	N/A	0.3%	1.7%	3.48%
Mismatch Voltage	N/A	N/A	N/A	N/A
Supply Voltage	±9V	0~15V	3.3V	±6/±3/1.8 V

Chapter 3

Design of HV Monopolar Biphasic Dual-Mode Stimulator with Low Peak Transient Current

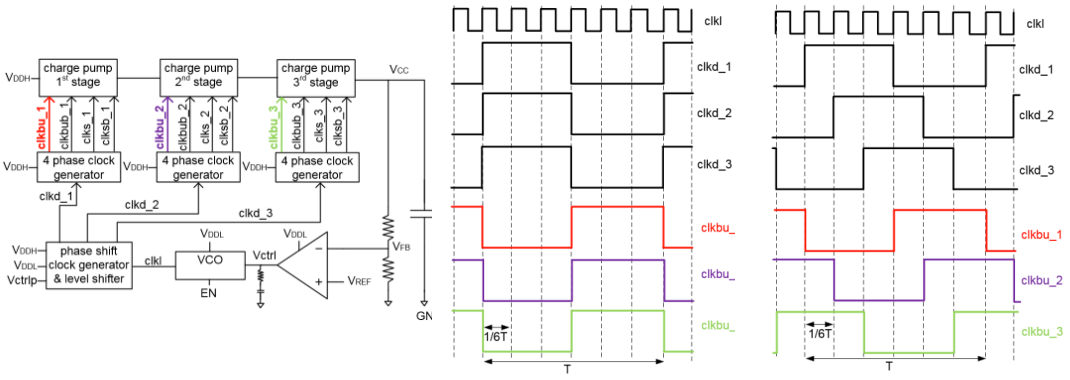
3.1 Motivation and Prior Art of HV Dual-Mode Stimulator

According to research [25], correct stimulation parameters (frequency, pulse width, amplitude, etc.) for DBS is crucial and still under investigation. The efficacy of DBS treatment can be optimized by increasing amplitude followed by changing the electric contacts or increasing pulse width. In this case, a combination of short pulse width and high amplitude (5~10V or mA) is an option. In this work, a 10V/ 10mA amplitude of stimulus output is expected to be achieved, and the amplitude also covers the specification in chapter 2.

The stimulator in chapter 2 is fabricated in LV process which has transistors with at most 3.63V tolerance voltage. A thesis [26] has presented a method to accomplish the HV driver by stacking LV transistors; however, it needs many transistors, complicated structure, and will take up a large area. In contrast, in this work, 16~29V HV transistors in 0.18-μm HVGen2 CMOS process are used and are able to reduce the area consumption to reach this specification.

Most structures and circuits are similar to the ones in chapter 2; however, through the simulation of chapter 2, it is found that the current output of this circuit has a problem that peak current exists. For high voltage specification such as 10mA, this peak voltage may cause damage to the tissue. Therefore, referring to the concept of peak reduction in a thesis [27], it uses phase shifting to avoid high current input from flowing into the circuit immediately, as illustrated in Fig. 3.1. In this work, since the frequency of signals is not high, the required delay time needs to reach the level of microsecond.

If a common delay circuit is used, a large capacitor will be needed, which will cause an unworthy area loss. Therefore, a delay circuit for this stimulator is purposed so that peak reduction for this work can be achieved.



(a) (b) (c)

Fig. 3.1 (a) charge pump with clock shifting for peak reducing (b) clock signal before peak reducing (c) clock signal after peak reducing. [27]

Table 3.1 Specifications of HV Dual-Mode Stimulator.

Process	TSMC 0.18μm HVGen2 CMOS process
Stimulator Type	Monopolar Biphasic Constant Current/ Voltage Stimulator
Device	1.8V/ 5V LV MOS 16V/ 29V HV PMOS (Vgs=0~ 5.5V) 16V/ 24V/ 29V HV NMOS (Vgs=0~ 5.5V)
Supply Voltage	1.8V/ ±5V/ ±10V/ ±15V
Stimulation Current Amplitude (@1kΩ)	0.2mA ~ 10mA (0.2mA per step)
Stimulation Voltage Amplitude (@1kΩ)	0.2V ~10V (0.2V per step)
Channel Numbers	8
Pulse Width	20 ~ 450 us
Stimulation Period	4 ~ 500ms (2 ~ 250Hz)
Output Load	Electrode model
Discharge Circuit	Passive discharge for channel 2, 3, 6, 7 Active discharge for channel 0, 1, 4, 5
Mismatch Current	Minimum
Mismatch Voltage	Minimum
Stand-by Power	Minimum
Residual DC Current	Minimum

3.2 Specifications of HV Dual-Mode Stimulator

Table 3.1 shows specifications of the HV dual-mode stimulator. The stimulator is also a monopolar biphasic dual-mode stimulator; however, it is fabricated in TSMC 0.18-μm HVGen2 CMOS process. It has 8 channels in total, which four of them are with passive discharge circuit and the other four of them are with active discharge circuit that can also do passive discharge function.

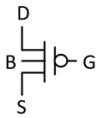
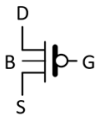
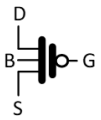
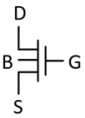
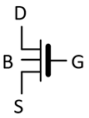
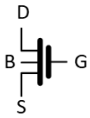
Since the current/ voltage specification are scaled up to ±10mA/ ±10V, the power supplies that are over 10V must be needed. This stimulator is still in the testing stage; hence, all the voltages will be supplied by precision instruments, and should be supplied by power management units and charge pumps if it is integrated into a SoC in the future. Notably, 50 steps of high-resolution amplitude are designed for wider use.

Given that there are many high voltages in this specification, advantages in this CMOS process can be properly taken. In this work, 1.8V and 5V LV MOSFETs are used, and so are the HV MOSFETs listed in the table. The detailed introduction of this process is delivered in next section.

3.3 Design of HV Dual-Mode Stimulator Circuit

3.3.1 Brief Introduction and Constraints of 0.18μm HVGen2 CMOS process

Table 3.2 Symbols of different MOSFETs in 0.18μm HV CMOS process.

	PMOS			NMOS		
Device Type	1.8V	5V	HV (16~29V)	1.8V	5V	HV (16~29V)
Symbol						
Voltage Tolerance for V_{DS} and V_{GS}	1.8V +10%	5V +10%	Spec. +10% V_{GS}= 5.5V	1.8V +10%	5V +10%	Spec. +10% V_{GS}= 5.5V

The process used for this work is TSMC 0.18μm HVGen2 CMOS process. Table 3.2 are the symbols used for readability in the following schematic views of different types of MOSFETs. Among them, HV MOSFETs with different voltage tolerances are used and may cause confusion; as a result, they share the same symbol and will be marked a specific name later in the schematic views. In comparison with the LV CMOS process in chapter 2, LV devices in this process have two thicknesses of gate oxide which give voltage tolerance of 1.8V+10% and 5V+10%.

Particularly in this process, in order to obtain better connectivity between HV and LV areas, all LV devices should be put in an isolation ring as it is illustrated in Table 3.3. Since there is a rule if V_{inside} < -5V, then V_{HVNW} should be

$$V_{HVNW} - V_{inside} \leq 5V, \tag{3.1}$$

if

$$V_{inside} < -5V, \tag{3.2}$$

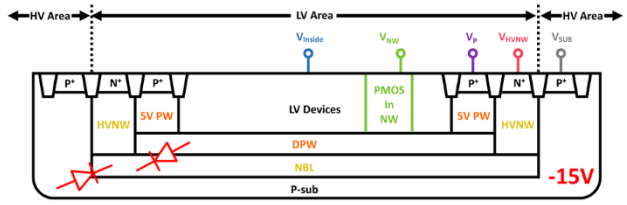
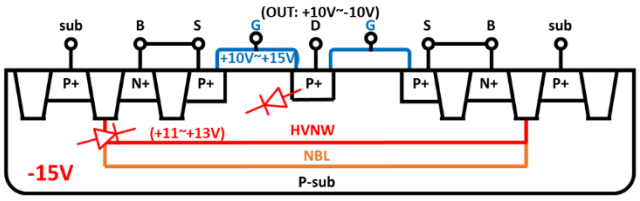
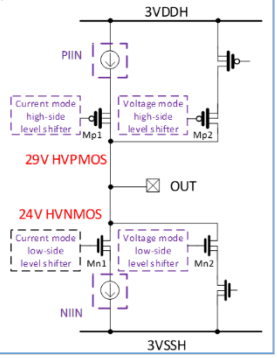
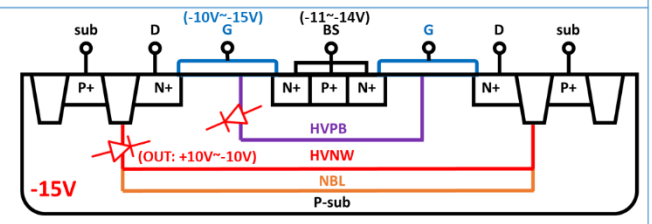
then

$$V_{HVNW} < 0V. \tag{3.3}$$

This implies that the p-substrate of the whole chip cannot be ground level as usual to avoid the p-n junction forward-leakage problem; therefore, it is biased in the minimum voltage -15V.

As for HV MOSFETs, which are also shown in Table 3.3, although they seem to have high tolerances, the gate-source voltage of them is limited to 5.5V. The NBL layer is a buried n-well that separates the p-well inside the transistor from the p-substrate. Suitable types of HV MOSFETs should be carefully chosen and all voltages should be properly biased owing to these constraints.

Table 3.3 Cross-Section Views and Design Considerations in 0.18μm HV CMOS process.

	Cross-Section View	Design Considerations
Isolation Ring for LV Devices		V_{HVNW}-V_{inside}≤ 5V. 5V PW connects to minimum voltage in LV area, while P-sub connects to minimum voltage in whole system.
29V HV PMOS (In Driver)		V_{GS}< 5.5V, V_{DS}< 31.9V for PMOS, V_{GS}< 5.5V, V_{DS} < 26.4V for NMOS. Simplified Stimulus Driver Circuit: 
24V HV NMOS (In Driver)		

3.3.2 Architecture

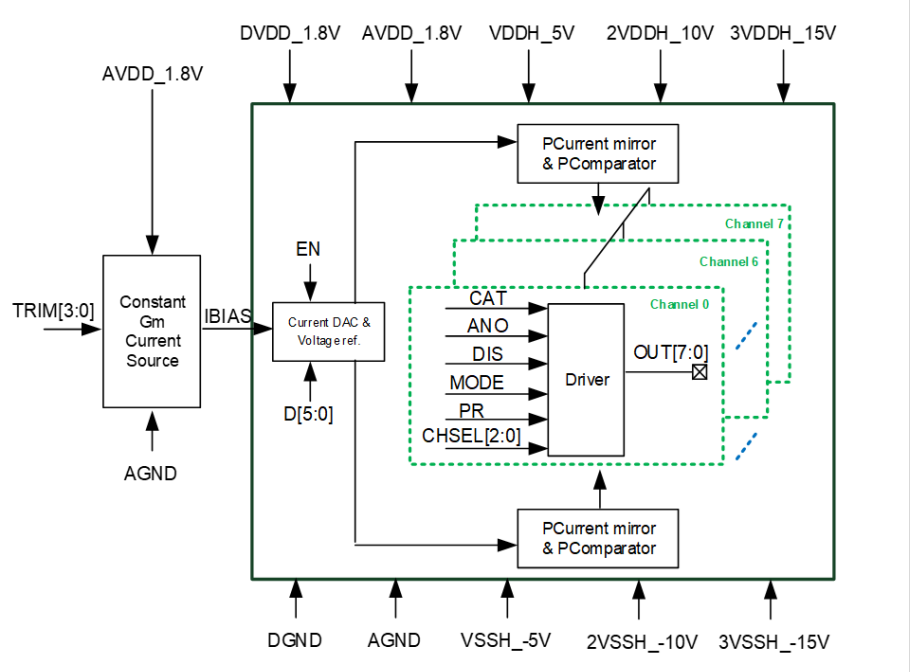


Fig. 3.2 Block diagram of HV dual-mode stimulator.

The block diagram of this HV dual-mode stimulator is shown in Fig. 3.2. The general circuit architecture is similar to that of chapter 2; still, there are several differences in this work. To begin, the power supplies are changed into VDDH (5V), 2VDDH (10V), 3VDDH (15V), VSSH (-5V), 2VSSH (-10V), and 3VSSH(-15V) due to the modified specification. Next, transistors in the driver and current mirror circuit are redesigned on the basis of this HV CMOS process, and the details are discussed in chapter 3.3.3 and chapter 3.3.5. Then, switches are added in comparators and active discharge circuit to reduce power consumption when it is not stimulating. Last, a peak-reduced circuit is purposed to eliminate the peak current in the current mirror circuits and it is discussed in chapter 3.3.4.

3.3.3 HV Current Mirror for Current Mode and Voltage Reference for Voltage Mode

As shown in Fig. 3.3, the current sent by the DAC passes through the switch controlled by the control signals to form the current source in the current mode and the reference voltage required in the voltage mode. The thesis [20] mentioned that if switch control is used between DAC and current mirror, the peak value of current output can be reduced. Therefore, SW4 and SW5 are designed to separate the DAC and the current mirror. In this circuit, Mp4 is chosen to be 16V HV PMOS, Mn1~Mn4 are 16V HV NMOS, and Mp9 is 29V HV PMOS to avoid the overstress issue. Specifically, due to the gate to source voltage has a limit of 5.5V, voltages of their gates should be carefully designed to not violate this rule.

Operation of these switches are listed in Table 3.4. Because SW4 and SW5 are turned off in high-Z mode, if the switch of voltage mode is on, it is better to bypass the current of DAC through SW1 to ground to prevent comparator from unexpected working. As for high-Z mode when the switch of current mode is on, SW3 can be turned on instead of SW1 to keep DAC from generating current that causes leakage.

Furthermore, current mirrors with peak-reduced circuit and without peak-reduced circuit are illustrated in cathode mode current mirror and anode mode current mirror, respectively. Actually, they both exists in these two current mirrors and can be decided which one to use by the control signal PR, and it is shown in figure this way to explain more clearly. The detailed information about how peak-reduce circuit works is in the next section.

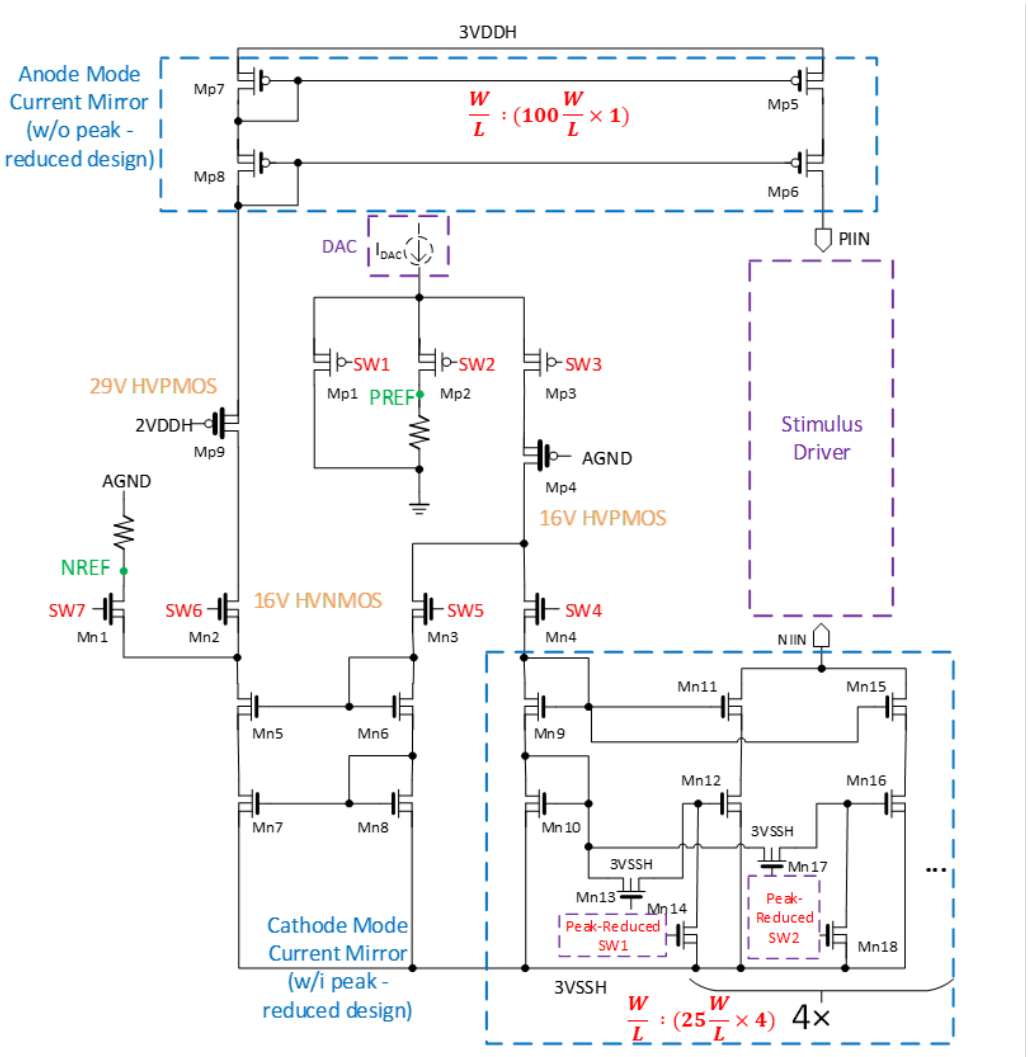


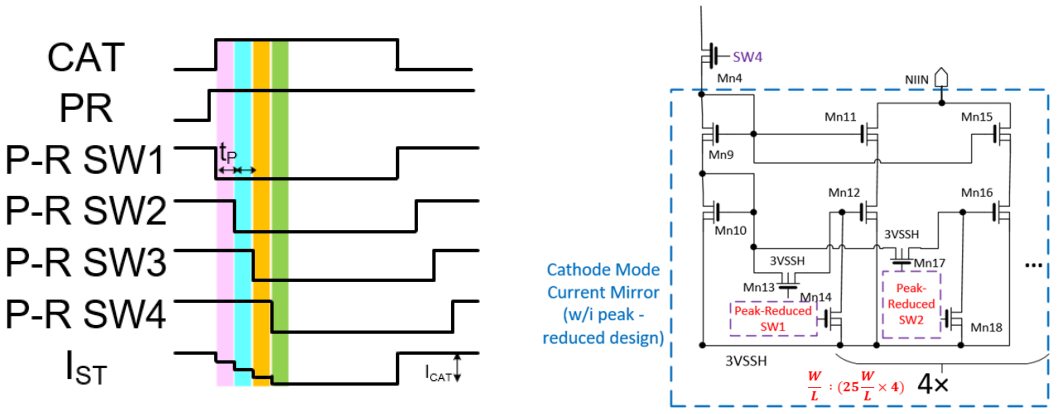
Fig. 3.3 The circuit of current mirror for current mode and voltage reference for voltage mode in HV dual-mode stimulator.

Table 3.4 Status of switches in the circuit of current mirror and voltage reference in HV dual-mode stimulator.

Switches That are Turned On	Current Mode	Voltage Mode	High-Z Mode
Cathode Stimulation	SW3, SW4	SW3, SW5, SW7	SW3 (current) SW1 (voltage)
Anode Stimulation	SW3, SW5, SW6	SW2	
Switches that are not mentioned are off.			

3.3.4 Purposed Peak-Reduced circuit

In Fig. 3.3, the peak-reduced circuit is shown by comparing the cathode mode current mirror with it with the anode mode current mirror without it. The anode mode current mirror uses a more common practice to directly use a current mirror with a size of 1:100 to generate stimulation current. The instantaneous reference current passing through will cause the gate voltage of the current mirror to change suddenly, causing the large transistor with a size of 100 times (Mp6) to produce a peak current, which may have an adverse effect on the tissue. Therefore, it is redesigned into The peak-reduced circuit in the cathode mode current mirror illustrated in Fig. 3.4 (b). In this case, it divides the transistor with a size of 100 times into 4 transistors with a size of 25 times without increasing the layout area, and then design the switches with the time difference as shown in Fig. 3.4 (a) to make 4 transistors mirror the current and enter it to the driver according to the time difference. In this design, there are both circuits of original and peak-reduced designs in both current mirrors, and a control signal PR is used to select which one to use to compare the effects of them.



(a) (b)

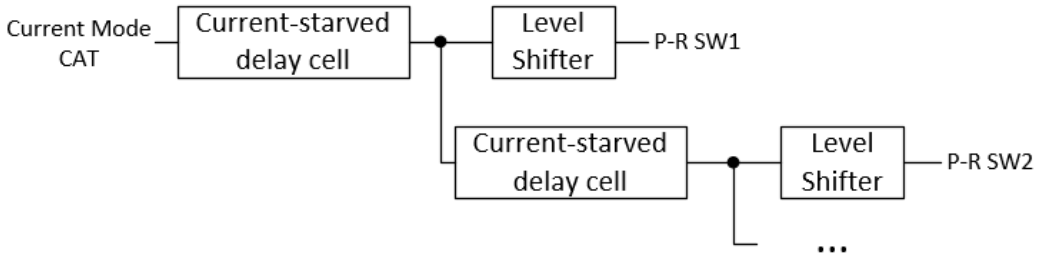
Fig. 3.4 (a) Time chart of peak-reduced switches (b) Cathode mode current mirror with peak-reduced design.

The traditional delay cell is to connect two inverters and load a capacitor; Thus, the delay time of it is controlled by the size of the inverter and the capacitor. If it is needed to delay to a longer period (μs level), a large capacitor must be used, which will consume a large area. Therefore, referring to the concept of the paper [28], a current-starved delay cell is used in this circuit, as shown in Fig. 3.5. This circuit can determine the length of the delay by controlling the amount of current flowing into the inverter and capacitor C1, while Mp1 and Mp2 operate as current sources, and Mn1 and Mp2 work as current sinks, That is, the inverters in the middle starve for current. The propagation delay can be analytically defined as

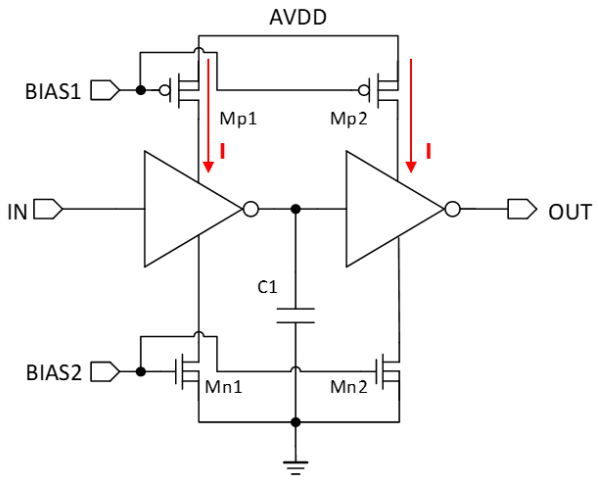
$$Propagation\ \ Delay = t_p = \frac{C_1 \cdot AVDD}{K_p \cdot I} \tag{3.4}$$

where K_p is the technology parameter.

Spice is used to simulate this design for the required time according to this equation. BIAS1 and BIAS2 can be got from the inherent constant gm in this work for the required values, and level shifters are at last connected to form the switch control circuit.



(a)



(b)

Fig. 3.5 (a) Circuit of peak-reduced switches (b) Circuit of current-starved delay cell.

3.3.5 HV Stimulus Driver

The operation of this stimulus driver is similar to that in chapter 2.3.6. Due to the use of HV components, the main transistors serving as driver switches can be realized with only 4 HV MOSFETs Mp1, Mp2, Mn1, and Mn2. The 29 HV PMOS and 24 HV NMOS are decided owing to their cross voltage, which is about 24V drain to source voltage. The output voltage of level shifters SW1 and SW2 are designed to be 2VDDH (on) or 3VDDH (off), while the output voltage of level shifters SW3 and SW4 are 2VSSH (on) or 3VSSH (off).

Another modification is that the switch between resistors and ground has been removed considering the leakage current of it does not cause many effects on the whole circuit. The ratio of the resistor divider is 7 to keep Mp5 from facing the high voltage

directly, and the value of resistors is about 4MΩ in total. Thus, the leakage current passing through the resistors to the ground is a maximum of 10V/ 4MΩ = 2.5μA, which is about 0.025% of output current.

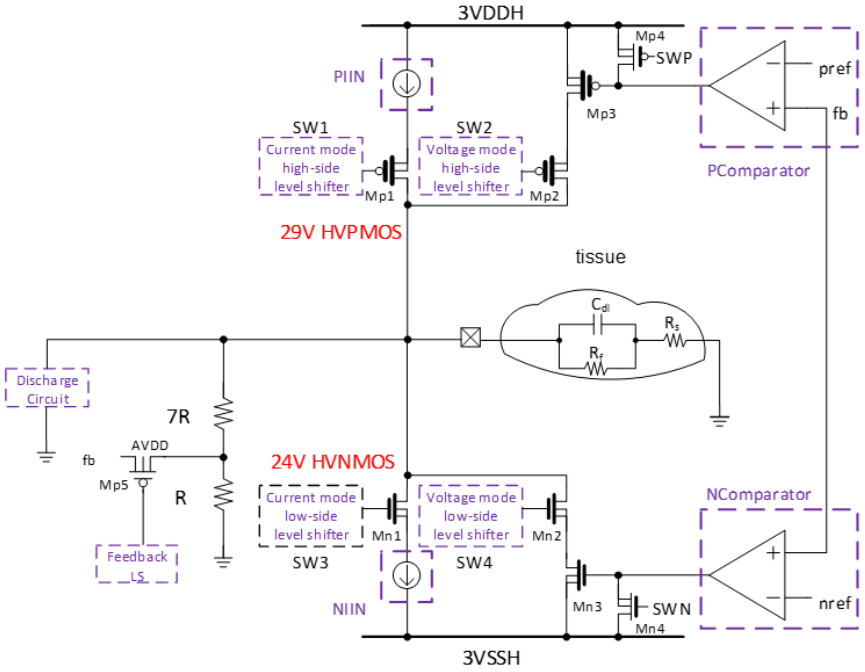


Fig. 3.6 The circuit schematic of the stimulus driver in HV dual-mode stimulator.

3.4 Simulation Results

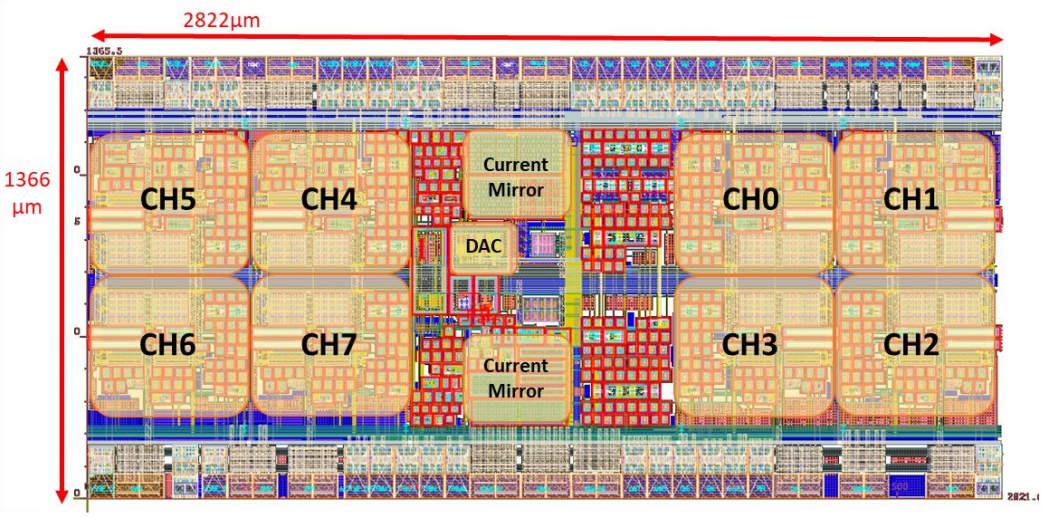


Fig. 3.7 Layout photo of HV Dual-Mode Stimulator.

The photo of the layout is shown in Fig. 3.7, and the total area is 2822μm *1366μm, and the placement is similar to that of the stimulator in chapter 2. Since there are many voltage ranges in this work, isolation rings biased in different voltage ranges are used to avoid overstress problems; therefore, the area of this chip is larger than that is realized in LV CMOS process. Fig. 3.8 shows the operation of changing channels by the 3-bit signal CHSEL[2:0] in this work.

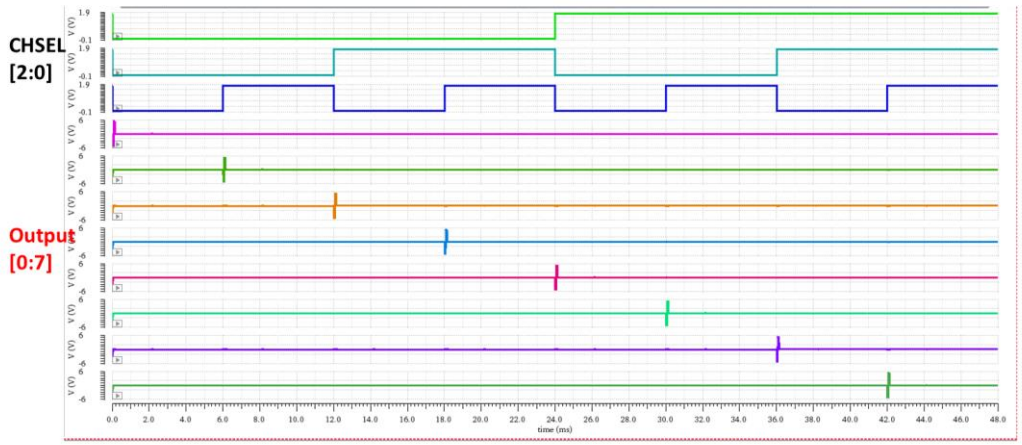
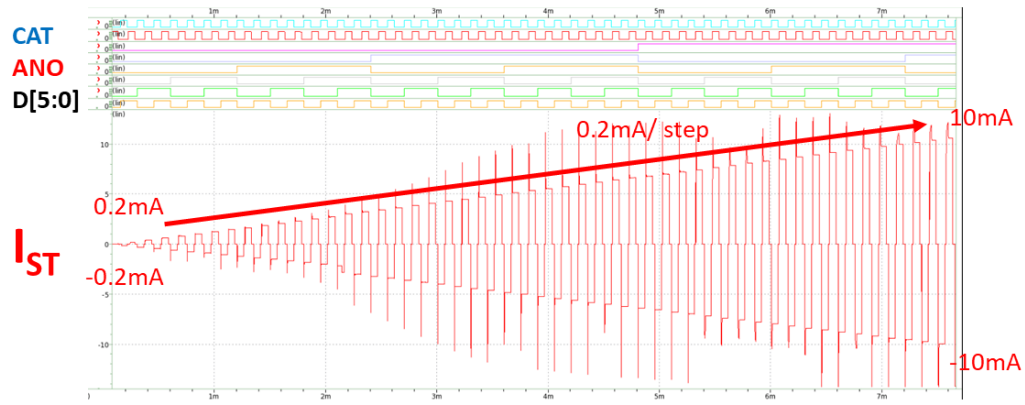
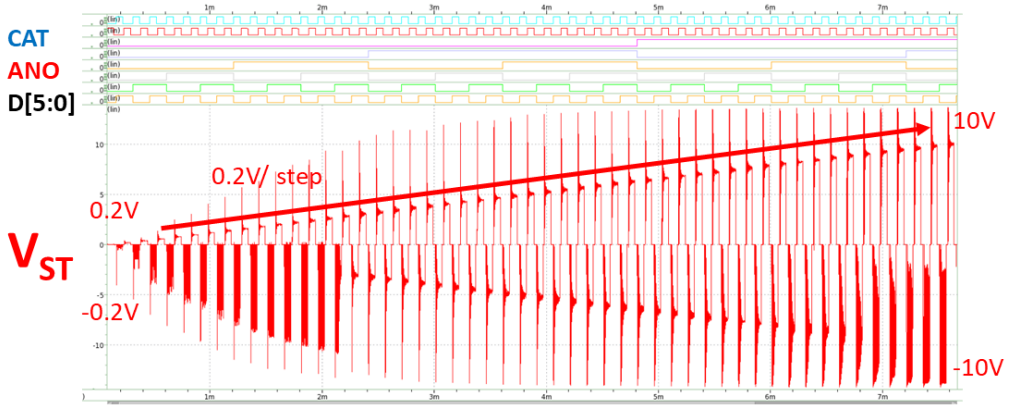


Fig. 3.8 Simulation results of stimulus output while tuning CHSEL[2:0] in HV dual-mode stimulator.

3.4.1 Current Mode and Voltage Mode



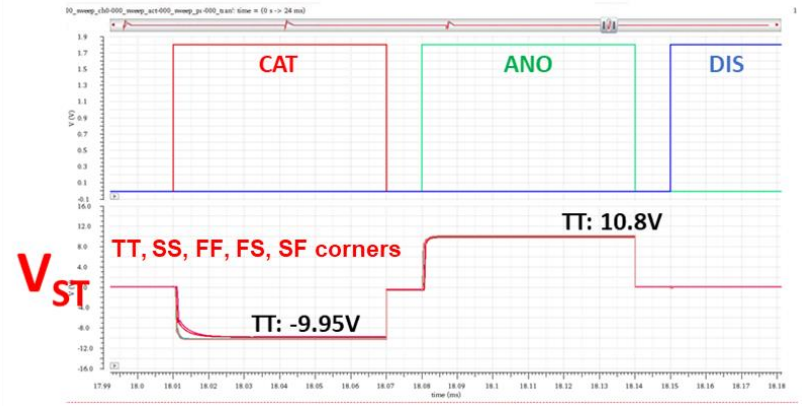
(a)



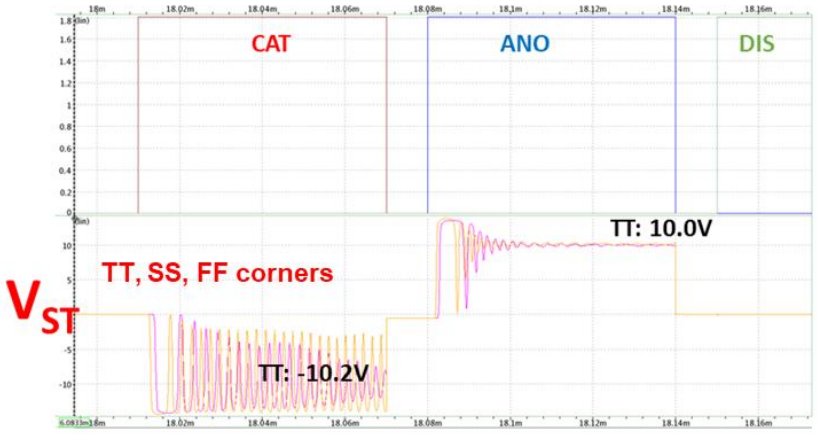
(b)

Fig. 3.9 Post-layout simulation result of (a) current-mode (b) voltage-mode output for tunable amplitude test in HV dual-mode stimulator.

The specification of current/ voltage amplitude is from 0.2mA/ V to 10mA/ V and -0.2mA/ V to -10mA/ V with 0.2mA/ V per step by tunable signal D[5:0]. Fig. 3.9 shows the stimulus output current and voltage on the full scale of this work. It is noteworthy that there is an oscillation in some of the stimulation in voltage mode; therefore, pre-layout simulation in 5 corners and post-layout simulation results are taken a deeper observation in Fig. 3.10 for further analysis. The output curves of TT, SS, FF, SF, and FS corner in the pre-layout simulation are almost overlapped with no oscillation at all; however, output curves in post-layout simulation include obvious oscillation in cathode mode stimulation and oscillation at the beginning of anode mode stimulation. As the output voltage slowly stabilizes, the average value of the output voltage still matches the expected value. It means that the phase margin of comparators may be affected by parasitic capacitors and parasitic resistors.



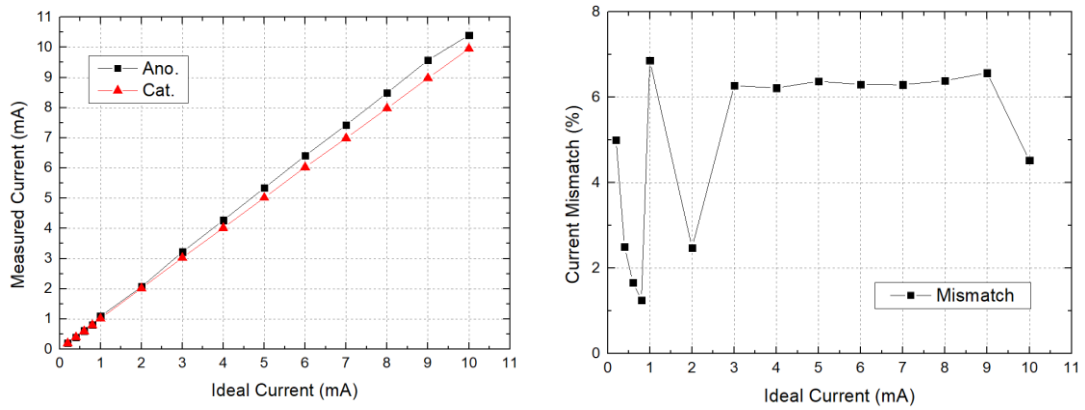
(a)



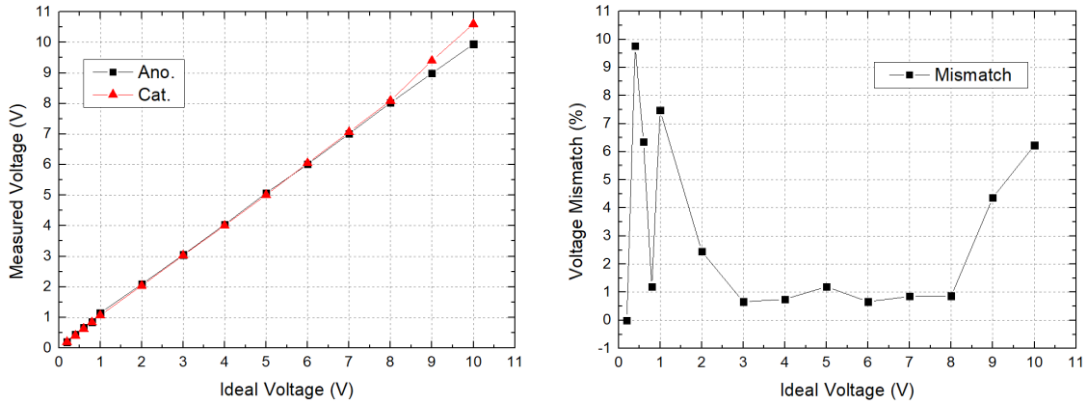
(b)

Fig. 3.10 (a) Pre-layout simulation (b) Post-layout simulation results of voltage-mode output at highest amplitude in every corner in HV dual-mode stimulator.

All the stimulus output values and mismatches in current mode and voltage mode are organized into Fig. 3.11. The current mismatch in the HV dual-mode stimulator is under 6.87%, and the voltage mismatch in this work is under 9.76%. In addition, mismatch usually gets larger in the higher amplitude in both modes. Since the resolution of this work is much higher than the one in chapter 2, which is 50 steps comparing with 18 steps, a slight mismatch in low amplitude can be magnified 50 times to become a much larger value.



(a)



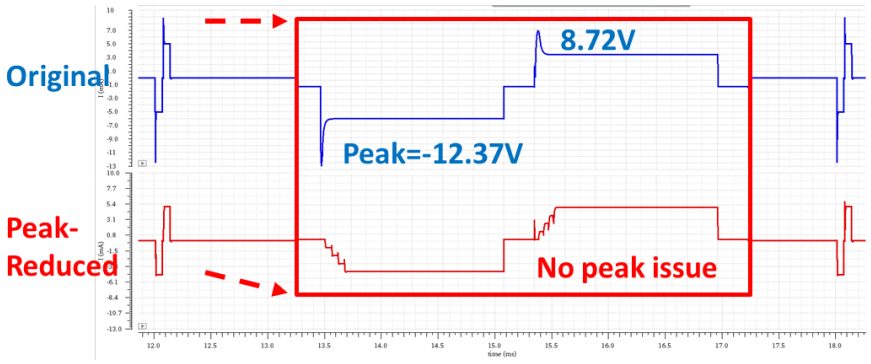
(b)

Fig. 3.11 Post-layout results of (a) current (b) voltage mismatches of HV dual-mode stimulator.

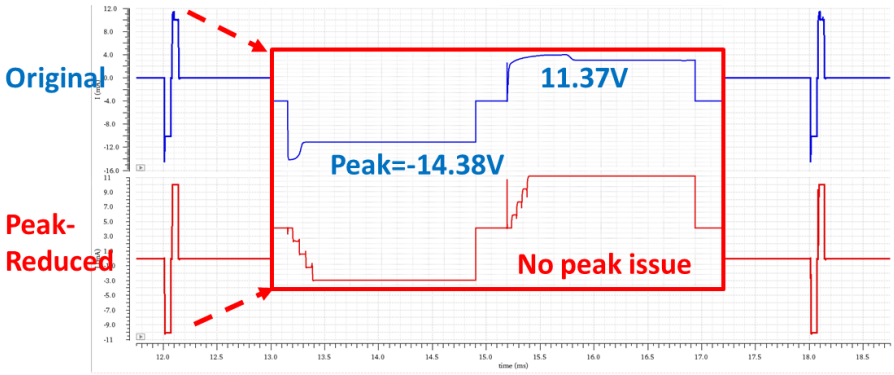
3.4.2 Peak-Reduced Circuit

The peak-reduced circuit is designed for eliminating the peak current caused by a large ratio of the current mirror, Fig. 3.12 shows the comparison of original and peak-reduced output waveform in 5mA and 10mA (largest amplitude) current-mode stimulation. It can be observed that due to the delay time in the peak-reduced switch, 4 current mirrors are turned on one after another. The delay time is designed to let the output stabilize at the time that the original circuit reaches the stable state, and can be a little longer for better observation. If this function is verified after measurement, the delay time can be designed tunable using tuning resistors in the constant-gm circuit or

designing its own control voltage. Ideally, the delay time is designed to be consistent in cathode-mode and anode-mode stimulation; however, there will still be some mismatch between them. The mismatch will be small due to the short period of peak-reduced process and can be fixed by discharging after stimulation. Mainly, the peak issue is solved in both amplitudes in post-layout simulation.



(a)



(b)

Fig. 3.12 Post-layout results of comparison of original and peak-reduced output waveform during (a) 5mA (b) 10mA current mode stimulation.

3.5 Measurement Results

The die microphotograph of the HV dual-mode stimulator chip fabricated in a 0.18μm HVGen2 CMOS process is shown in Fig. 3.13. All the capacitors are implemented with the metal-insulator-metal (MIM) capacitors.

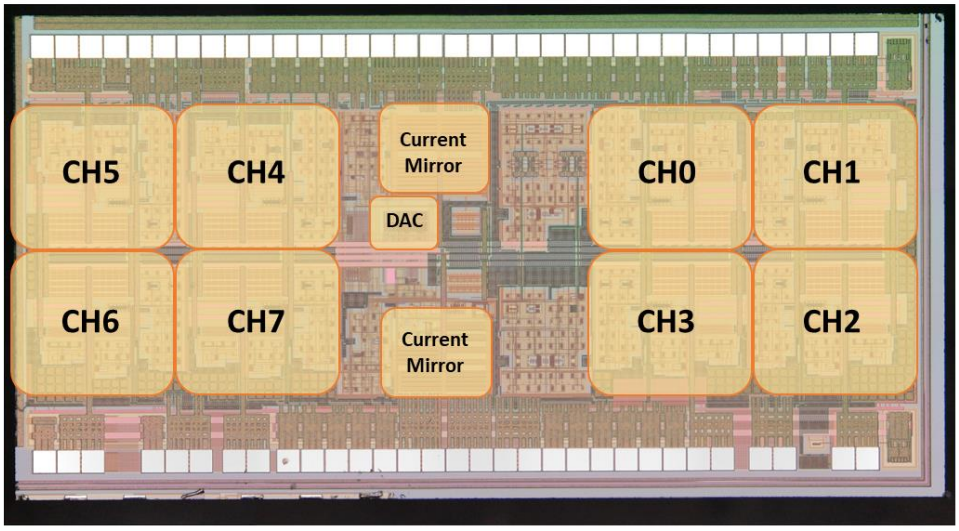
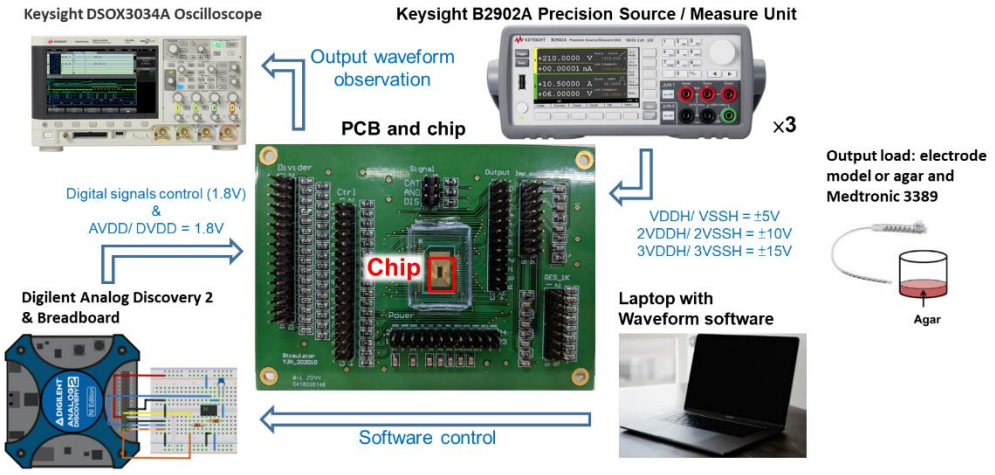
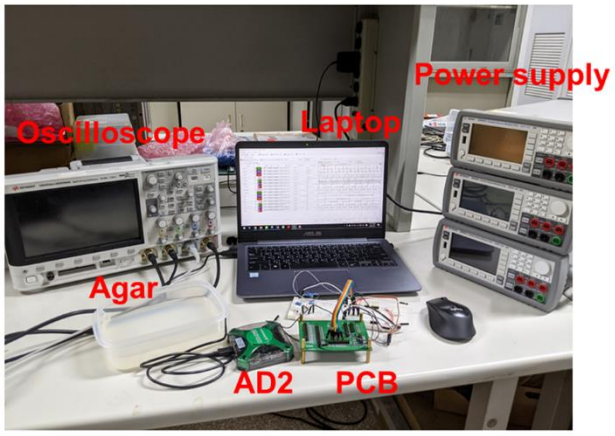


Fig. 3.13 The microphotograph of the fabricated HV dual-mode stimulator chip.

The chip is bonded on PCB for measurement, and the whole measurement setup and practical environment are shown in Fig. 3.14. Since Digilent Analog Discovery 2 (AD2) has a limit voltage of ±5V as the USB input, power supplies and waveform observation in this stimulator are not able to rely on it. Given that this stimulator has not been integrated into SoC, these power supplies will be sent by charge pumps in the future. Under this condition, 3 Keysight B2902A precision source are needed to generate power supplies of VDDH (5V), 2VDDH (10V), 3VDDH (15V), VSSH (-5V), 2VSSH (-10V), and 3VSSH (-15V). The oscilloscope, Keysight DSOX3034A, is used to observe the waveforms of all functions and output of the stimulator. Moreover, the AD2 along with Waveform software on the laptop is used to give control signals.



(a)



(b)

Fig. 3.14 (a) The measurement setup of the HV dual-mode stimulator. (b) The practical measurement environment of the HV dual-mode stimulator.

The commonly implemented frequency is 2~250Hz with stimulation duration of 60μs, so we choose the period of 6ms (166.67Hz) as it is used in chapter 2 for better observation and calculation. The result shown in Fig. 3.15 verifies the frequency and duration time are accurate and can be adjusted by control signals given. Fig. 3.16 shows that channel can be switched to one another by tuning CHSEL[2:0].

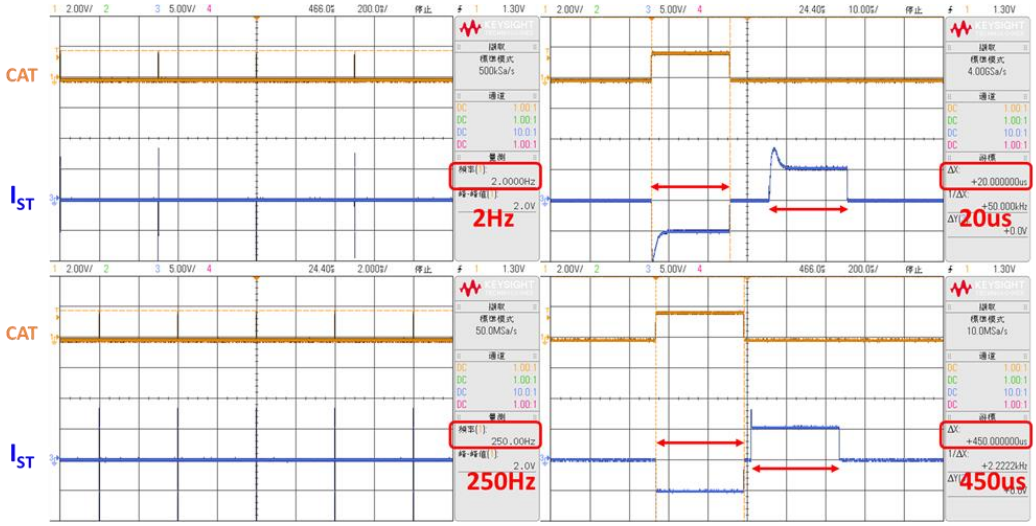


Fig. 3.15 The frequency and stimulation duration test of HV dual-mode stimulator.

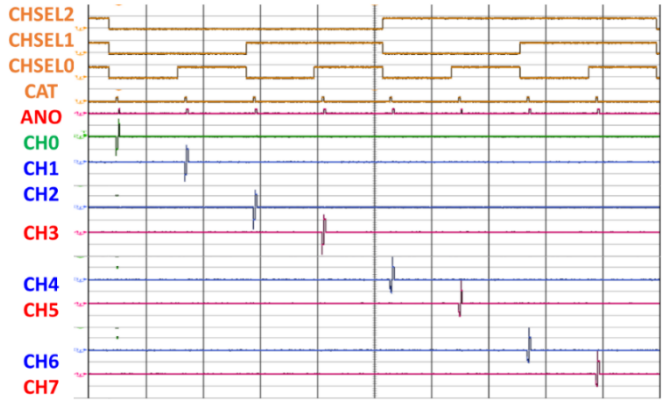


Fig. 3.16 Measurement results of stimulus output while tuning CHSEL[2:0] in HV dual-mode stimulator.

The measurement setup for the high-Z mode test is the same as the one in chapter 2.5.2. In Fig. 3.17, CH0 is selected to do stimulation, and the stimulus output of it is consistent whether it is connected to other channels. Besides, we use level shifters to produce switches that can control mode changes in stimulus driver, outputs of switches PI, PV, NI, and NV shown in Fig. 3.18 is probed from one of the channels (CH0). As it can be found that the output of these switches can be successfully shifted to 2VDDH (10V), 3VDDH (15V), 2VSSH (-10V), and 3VSSH (-15V) as is needed. The little voltage drop in NI and NV may be caused by measurement tools since this output pad

is not designed with a protective circuit due to its high voltage; however, this voltage drop does not block the driver from turning on and off.

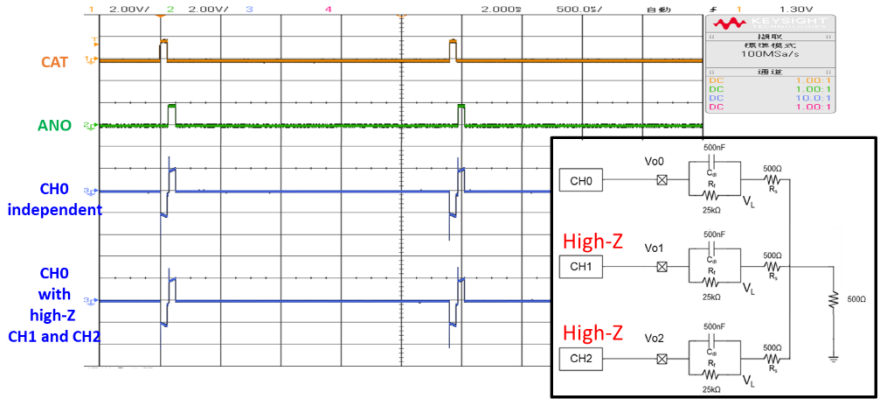


Fig. 3.17 The measurement results and setup of high-Z mode test of HV dual-mode stimulator.

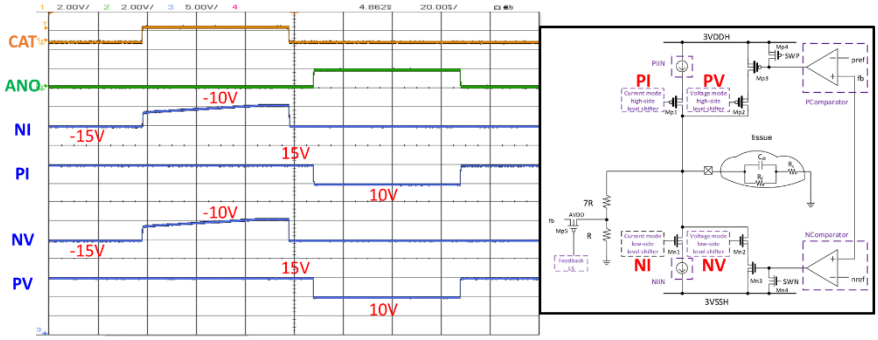
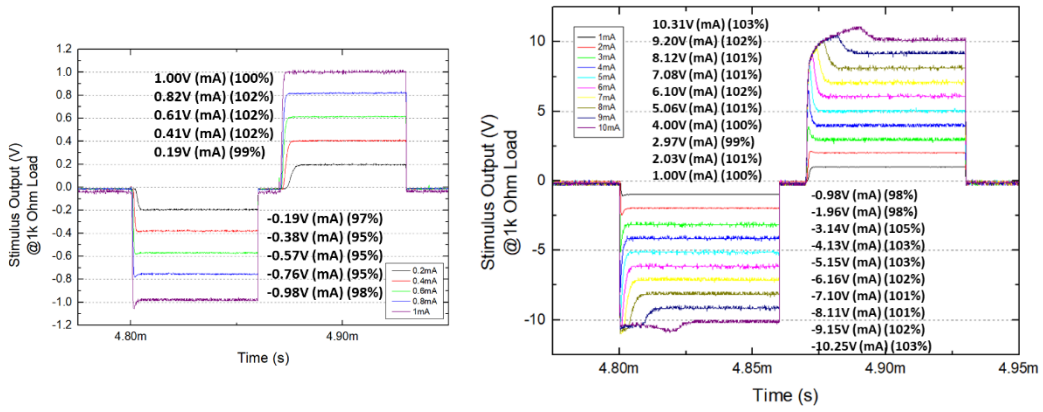


Fig. 3.18 Output waveforms of switches that control MOSFETs in stimulus driver of HV dual-mode stimulator.

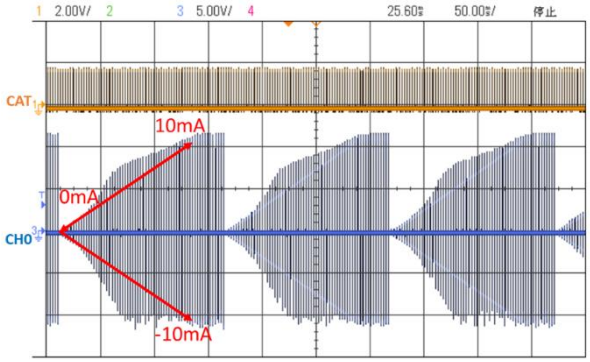
3.5.1 Current Mode

The current-mode stimulus output waveforms are shown in Fig. 3.19. They are sorted into small amplitudes (0.2mA~1.0mA) and large amplitudes (1mA~10mA) as a result of the wide range of scale that it will be messy to show 50 steps of the output waveform. It is noteworthy that the peak current starts to arise when the amplitude is larger than 2mA.

Data of 2 different chips are organized in Fig. 3.20. They have only a slight difference in output current value due to process variation, and the maximum mismatch is about 7.11% in small amplitudes.

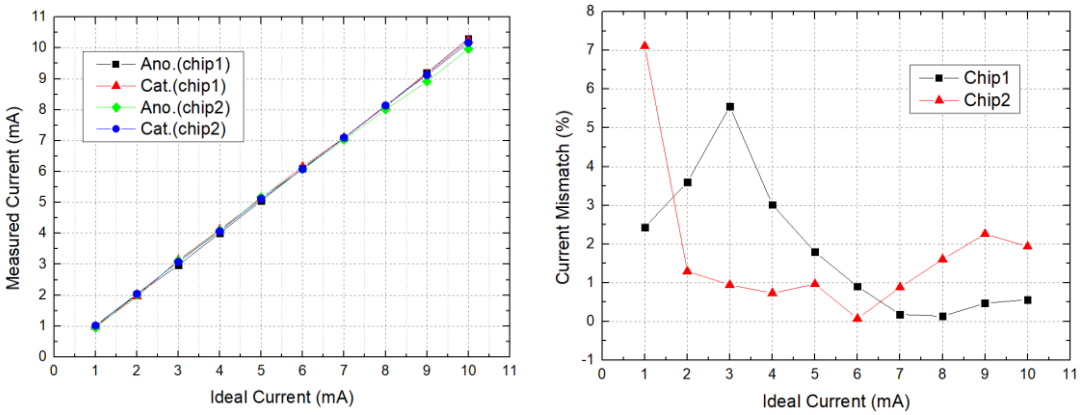


(a) (b)



(c)

Fig. 3.19 Measurement results of current-mode stimulus output in (a) small amplitudes (0.2mA~1.0mA) (b) large amplitudes (1mA~10mA) (c) full scale.



(a) (b)

Fig. 3.20 The measurement results and mismatches of 2 different chips of HV dual-mode stimulator.

3.5.2 Peak-Reduced Circuit

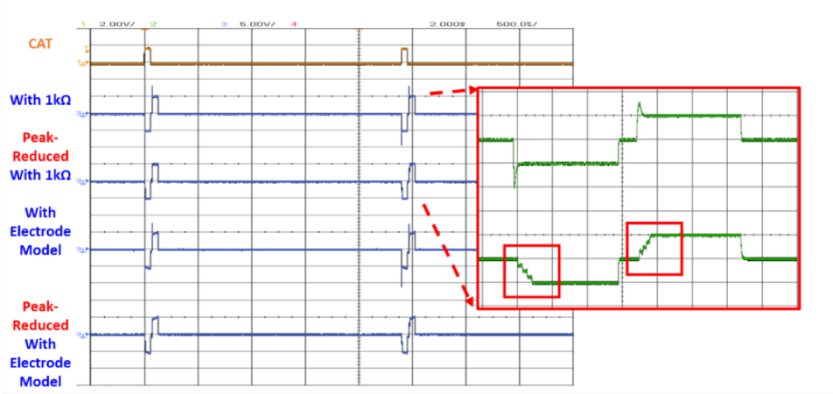


Fig. 3.21 The measurement results of the comparison of stimulus output with and without the peak-reduced circuit of HV dual-mode stimulator.

Fig. 3.21 shows the comparison of stimulus output with and without the peak-reduced circuit when the output load is only the R_s or the whole electrode model. The ones with the electrode model show characteristics of charging and discharging on C_{dl}. As expected, they all show peak current when they are without the peak-reduced circuit and are fixed after PR is turned on. The phenomenon of the 4 steps of current mirrors turning on is also clearly measured as shown in Fig. 3.22. Furthermore, this delay time can be tuned if this technique is used in the future. However, the output during 10mA

shows an unexpected peak current different from the post-layout simulation. This implies that there may be another path for peak current.

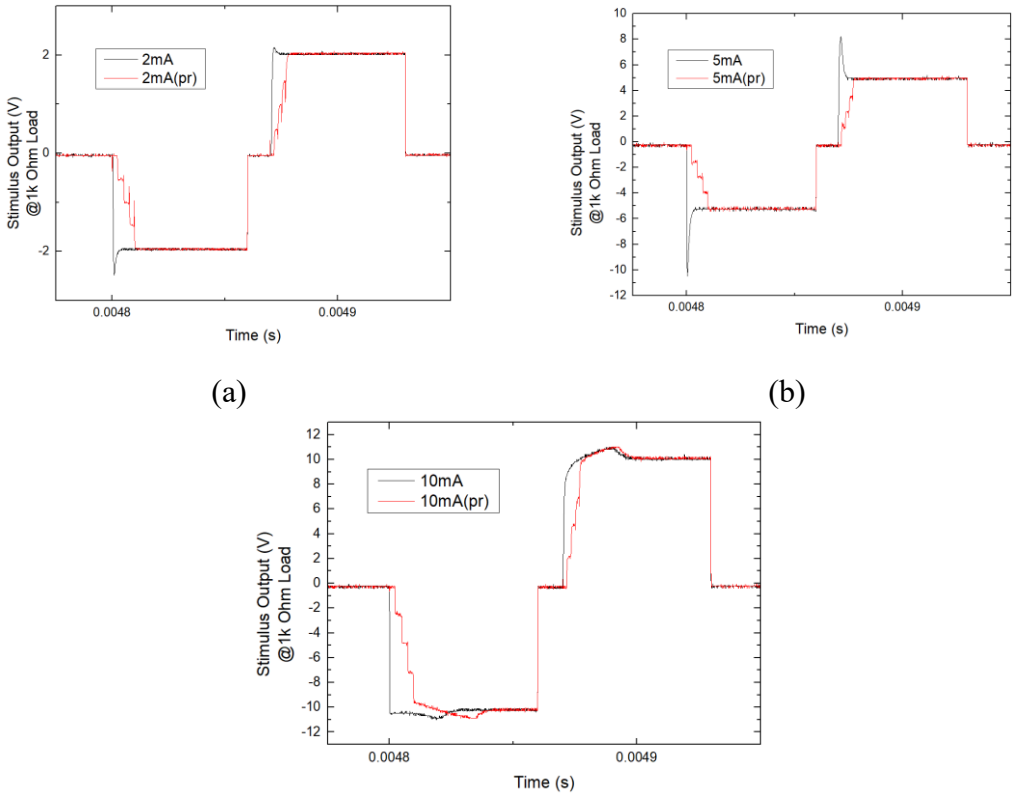


Fig. 3.22 The measurement results of the comparison of stimulus output with and without the peak-reduced circuit when the amplitude is selected to be (a) 2mA (b) 5mA (c) 10mA of HV dual-mode stimulator.

3.5.3 Discharge Circuit

Three types of discharging paths are designed for measurement in this work, which are passive discharge circuit, passive discharge path in the active discharge circuit described in Fig. 2.13, and the active discharge circuit.

The max residual current in this stimulator is

$$\frac{(I_{ST}\times mismatch)_{max}\times duration}{period} = \frac{3.14mA\times 5.55\%\times 60\mu s}{6ms} = 1.74uA \leq 4.49\mu A \qquad (3.5)$$

which has passed the limit of 4.49μA.

Fig. 3.23 shows that the three discharge paths all reduce the residual charge on C_{dl} effectively, and the active discharge circuit can leave the capacitor with the least residual charge and discharge at the highest speed to protect the tissue. In general, they all pass the limit of residual charge 2.99~8.97μC, which equals to a residual voltage of 5.98~17.94V due to Q=CV, and the potential limit -0.6~0.8V.

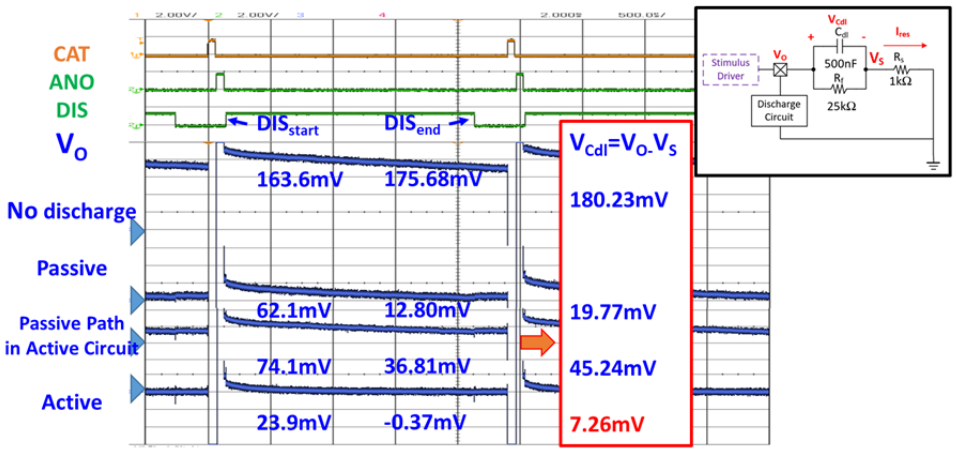
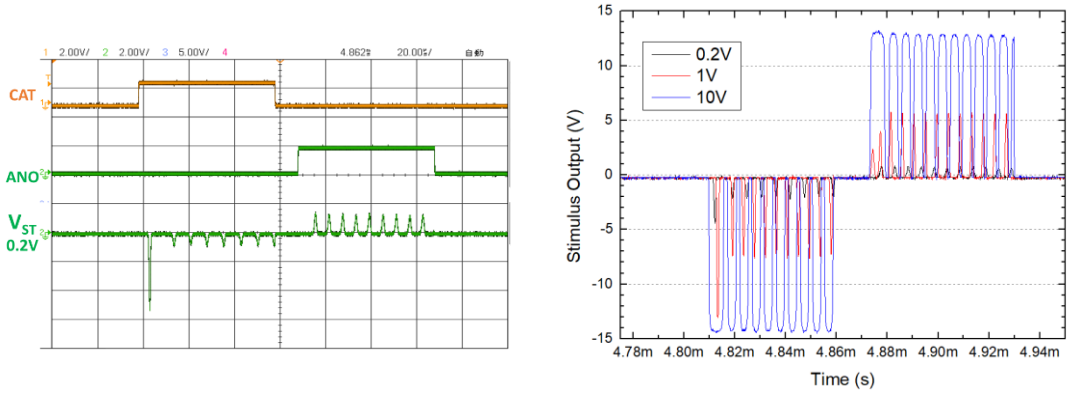


Fig. 3.23 The measurement results and schematic view of residual potential on C_{dl} of HV dual-mode stimulator.

3.5.4 Voltage Mode and Discussion

Fig. 3.24 shows the stimulus output of the voltage-mode stimulation in 0.2V amplitude and the full scale. In comparison with the simulation results in Fig. 3.10, the oscillating problem is much more serious in measurement results, and they never reach the steady-state even in the smallest amplitude.

Since there is the same problem in the voltage-mode stimulation in the LV dual-mode stimulator in chapter 2.5.1, it can be discussed together. Fig. 3.25 shows the feedback loop of voltage-mode stimulation in a driver. The possible reasons for the first guess for the oscillation problem may be the phase margin of the comparators, SW2 and SW4 for Mp4 and Mn4, frequency pulses from other circuits on the SoC, parasitic capacitance and resistance, or other unfound reasons.



(a) (b)

Fig. 3.24 The measurement results of the voltage-mode stimulus output of HV dual-mode stimulator.

To begin, the most possible reason is the phase margin of the comparators. Nonetheless, Fig. 3.26 has shown the Bode plot of one of the comparators and all results of phase margin in every comparator designed in this thesis. Since a system is usually steady when the phase margin of an operational amplifier is over 45 degrees, the post-layout simulation results have shown that all the phase margin of comparators match this condition. Secondly, the SW2 and SW4 have been proved to work well in Fig. 3.18. Next, since no other circuits are attached in the HV dual-mode stimulator, the possible reason that it is affected by other circuits on the SoC can be excluded.

Last, because the pre-layout simulation results in both works show no oscillation at all, the parasitic capacitance and resistance may be a reason for it. Moreover, since they should have been applied in post-layout simulation, a deeper look should be taken into the post-layout simulation results in both works. In Fig. 2.18, the post-layout simulation results of LV dual-mode stimulator in chapter 2 have shown that it takes a little more time to get into steady-state in cathode-mode stimulation, and thus the measurement results shown in Fig. 2.26 gives more oscillation in cathode-mode stimulation. As for the HV dual-mode stimulator in chapter 3, though there is an oscillation in the post-layout simulation results in Fig. 3.10, the output waveform still

converges in anode-mode stimulation. However, all stimulus outputs in the measurement results do not converge at all.

To conclude, the comparison of pre-layout and post-layout simulation results verifies that the parasitic capacitance and resistance make this feedback loop unstable. In addition, stimulus outputs in post-layout simulation should be clean and enter the steady-state soon to ensure no oscillation in measurement. However, since the phase margins of comparators are theoretically enough for stability the main reason for oscillation is still under investigation.

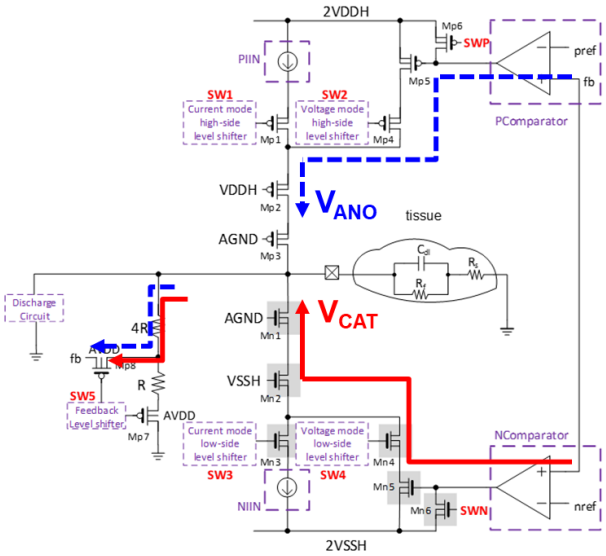


Fig. 3.25 The feedback loop of voltage-mode stimulation in LV dual-mode stimulator.

Phase Margin	Pcomparator	Ncomparator
LV (˚) (Chapter 2)	86.33	67.91
HV (˚) (Chapter 3)	67.32	57.70

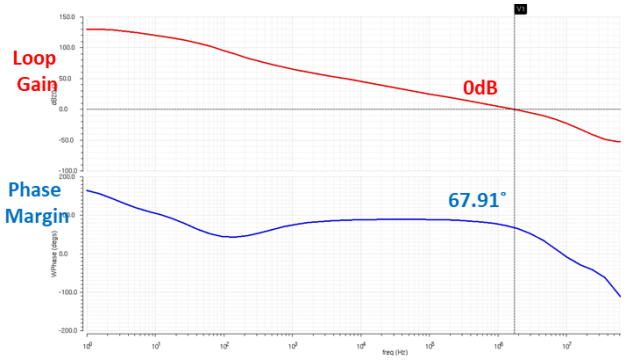
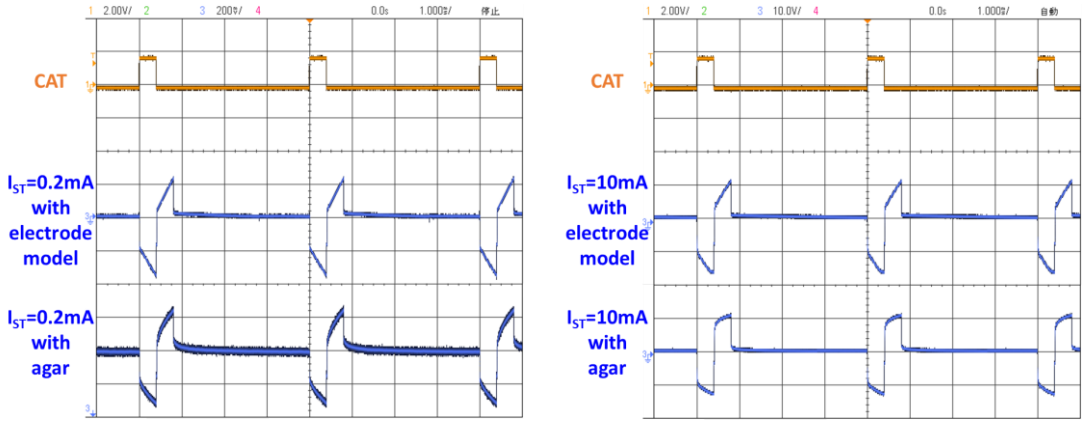


Fig. 3.26 Post-layout simulation results of phase margin of all comparators in this thesis and the Bode plot of Ncomparator in LV dual-mode stimulator.

3.5.5 Stimulation in Agar

Electrical stimulation experiment in agar can mimic the real measurement environment under the actual animal experiment. The output load used for measurement in previous sections are equivalent electrode model extracted from the electrode, Medtronic 3389 DBS lead, in agar; therefore, the measurement results of stimulation with electrode model load and agar load are compared in Fig. 3.27. The stimulus outputs in agar show slight changes of slopes in both cathode mode and anode mode because the faradic resistance in electrode is actually a changing value. Overall, the stimulus output results are close between using electrode model and agar as output load. Thus, it can be proved that electrode model used in previous measurements can be applied as impedence for stimulation.



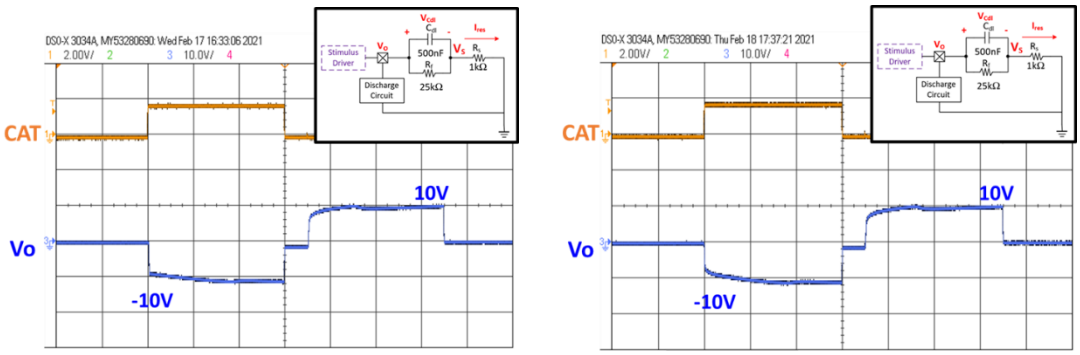
(a) (b)

Fig. 3.27 The measurement results of the current-mode stimulus output of HV dual-mode stimulator with (a) electrode model (b) agar.

3.5.6 Reliability Test

Since the SoC is designed to be implantable, surgical removal is risky to the patient. Therefore, the durability and reliability of the stimulator must be sufficient to withstand continuous use. For PD use, each time of stimulation usually does not exceed half an

hour. In this case, an experiment of continuously stimulating for 24 hours is conducted. As shown in Fig. 3.28, the stimulus output when the stimulation starts is similar to the stimulus output after over 24 hours. Therefore, the reliability of this stimulator is verified for long-time stimulation.



(a) (b)

Fig. 3.28 The measurement results of the current-mode stimulus output (a) at the beginning of stimulation (b) after continuous stimulation lasting for over 24 hours.

3.6 Summary

A HV monopolar biphasic dual-mode stimulator is fabricated in TSMC 0.18-μm HVGen2 CMOS process is purposed and verified in measurement in this chapter. The comparison of the specification and results in pre-layout simulation, post-layout simulation, and measurement are listed in Table 3.5. The current-mode stimulus outputs in measurement results can achieve ±10mA with a slight error. The current mismatch is less than 6% in current mode; however, the oscillation problem appears seriously in the voltage mode, causing difficulties measuring the values and calculating the voltage mismatch rate. The standby power is small than that in chapter 2 during simulation is perhaps because of the switches designed to turn off unused circuits that may have leaking current. Nevertheless, the increased standby power in measurement results may

result from the leakage current on PCB. The results comparison of this work with other presented stimulators are listed in Table 3.6.

Table 3.5 Comparison of results of HV dual-mode stimulator.

	Specification	Pre-sim	Post-sim	Measurement
Current mode/ CAT (@1kΩ) (mA)	-0.2 -1 -5 -8 -10	-0.20 -1.00 -5.02 -8.03 -10.03	-0.20 -1.02 -5.02 -7.98 -9.95	-0.21 -1.02 -5.12 -8.14 -10.17
Current mode/ ANO (@1kΩ) (mA)	0.2 1 5 8 10	0.20 1.00 5.02 8.03 10.04	0.22 1.09 5.34 8.49 10.40	0.20 0.95 5.17 8.00 9.97
Voltage mode/ CAT (@1kΩ) (V)	-0.2 -1 -5 -8 -10	-0.20 -1.00 -5.02 -8.03 -10.04	-0.20 -1.07 -5.01 -8.09 -10.60	oscillating
Voltage mode / ANO (@1kΩ) (V)	0.2 1 5 8 10	0.20 1.00 5.02 8.02 10.02	0.20 1.15 5.07 8.02 9.94	oscillating
Step	0.2mA/ 0.2V			
Mismatch current (%)	minimum	<0.1%	<5%	<6%
Mismatch voltage (%)	minimum	<0.25%	<6.5%	unknown (oscillation)
Standby power	minimum	24.92μW	14.27μW	267.89μW

Table 3.6 Performance comparison of HV dual-mode stimulator with other works.

	[28] 2018 SSC-L	[29] 2013 TBioCAS	[30] 2015 ISCAS	[18] 2020 TBioCAS	This work Chapter 3
Technology	0.18μm HV	0.35μm HV	0.18μm HV	0.25μm HV	0.18μm HV
Stimulator Type	Monopolar CCS/CVS	Monopolar /Bipolar CCS	Bipolar CCS	Bipolar CCS/CVS	Monopolar CCS/CVS
Number of Channels	1	2	8	4	8
Result Type	Measurement				
Stimulation Amplitude	0~10.2mA/ ±6V	0.032~1mA	0.5~8mA	0~5mA/ 0~10V	±10mA/ ±10V
Resolution	32 steps (5-bit)	32 steps (5-bit)	17 steps (5-bit)	50/ 20 steps (6-bit)	50 steps (6-bit)
Mismatch Current	N/A	0.3%	0.03%	N/A	6%
Mismatch Voltage	N/A	N/A	N/A	N/A	6.5% (post-sim)
Supply Voltage	±9V	0~15V	1.8/20V	2.5/5V	1.8V/±5V/ ±10V/±15V

Chapter 4

Conclusions and Future Work

4.1 Conclusions

Two stimulators for Parkinson's disease application are purposed in this thesis. The LV dual-mode stimulator fabricated in TSMC 0.18-μm LV 1.8/3.3V CMOS process in chapter 2 can deliver biphasic ±3.6mA/ V current and voltage amplitude with 0.2mA/ V per step, and the safety after discharge is tested. It has already been integrated into SoC and verified with the whole SoC chip, such as detect mode with AFEA circuit and power supplied by PMU and charge pump circuit.

To achieve a more effective DBS, a stimulator fabricated in TSMC 0.18-μm HVGen2 CMOS process in chapter 3 is purposed, which can deliver ±10mA/ V current and voltage amplitude with 0.2mA/ V per step. Due to the specification of high amplitude, a peak current problem appears and can be eliminated by the purposed peak-reduced circuit. Besides, 3 paths of discharge circuit are compared that they are all effective in releasing charge on the electrode-tissue model.

All the functions in both stimulators are verified without reliability issues except that the voltage-mode stimulation contains an oscillation issue to be solved.

4.2 Future Work

4.2.1 Accuracy of Current and Voltage Amplitude

Table 4.1 Comparison of accuracy of current amplitude.

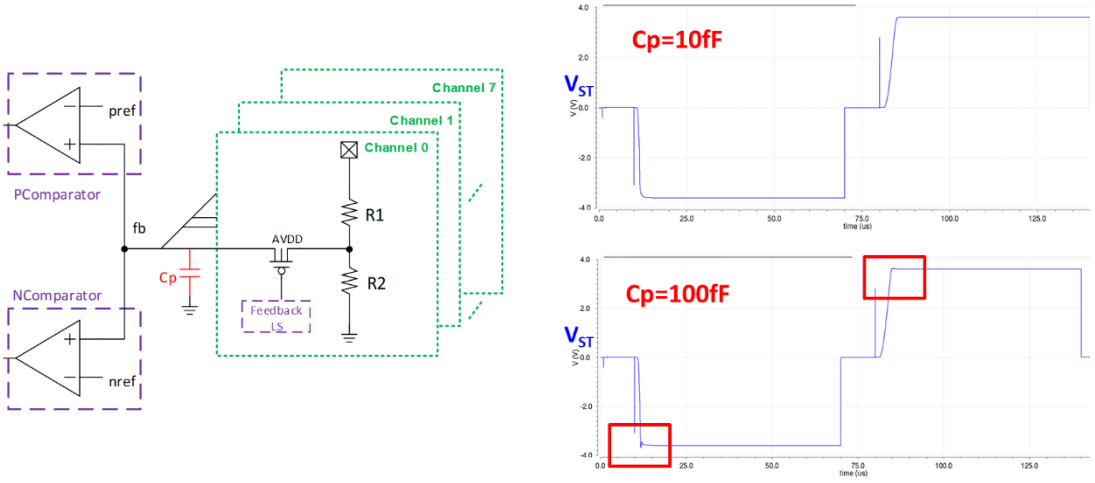
		Specification	Pre-sim	Post-sim	Measurement	Error in high amp.
Chapter 2 LV Current-mode output	CAT (@1k) (mA)	-0.2 -1 -2 -3 -3.6	-0.20 -1.01 -2.01 -3.02 -3.62	-0.20 -0.98 -1.96 -2.92 -3.49	-0.20 -0.97 -1.92 -2.87 -3.42	5.00%
	ANO (@1k) (mA)	0.2 1 2 3 3.6	0.20 1.01 2.01 3.02 3.62	0.20 0.99 1.97 2.95 3.52	0.19 0.98 1.94 2.92 3.49	3.06%
Chapter 3 HV Current-mode output	CAT (@1k) (mA)	-0.2 -1 -5 -8 -10	-0.20 -1.00 -5.02 -8.03 -10.03	-0.20 -1.02 -5.02 -7.98 -9.95	-0.21 -1.02 -5.12 -8.14 -10.17	1.70%
	ANO (@1k) (mA)	0.2 1 5 8 10	0.20 1.00 5.02 8.03 10.04	0.22 1.09 5.34 8.49 10.40	0.20 0.95 5.17 8.00 9.97	0.30%

Even though the resolution is higher and the amplitude range is wider in the stimulator of chapter 3 than that in chapter 2, the one in chapter 3 shows less distortion at high amplitude. As compared in Table 4.1, the output of the stimulator in chapter 2 decreases as the amplitude increases in post-layout simulation. The reason may come from the layout in DAC. In chapter 3, The layout technique of dummy MOSFETs is used to improve the matching properties of the current mirrors in DAC. Thus, the same technique should be applied in the stimulator of chapter 2.

4.2.2 Oscillation in Voltage-Mode Stimulation

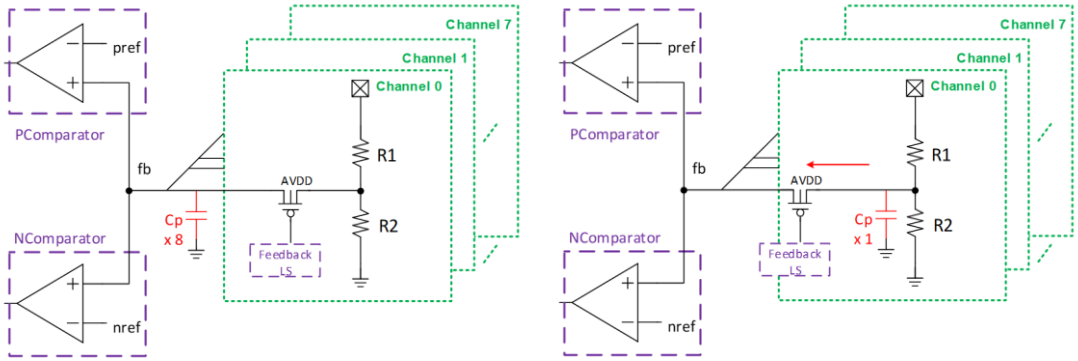
As discussed in chapter 3.5.4, oscillation problems exist in both stimulators in chapter 2 and chapter 3. Some possible reasons such as phase margin of comparators themselves and influenced by other circuits on SoC are excluded; therefore, parasitic resistance and capacitance are considered the most likely cause. Fig. 4.1 (a) shows the

pre-layout simulation setup of voltage-mode stimulation under different parasitic capacitances to simulate the actual wire capacitance. Fig. 4.1 (b) shows that a slight oscillation appears under large capacitance. Fig. 4.2 illustrates the modification of the layout. In the original version, the switches are right next to the resistor dividers at every channel; thus, every feedback loop contains long metal wires to the switches of every channel and makes 8 times the parasitic capacitance. Moving the switches close to the comparators reduces the total parasitic capacitance of every single feedback loop.



(a) (b)

Fig. 4.1 (a) Parasitic capacitance simulation setup. (b) Stimulus output under small and large parasitic capacitance.

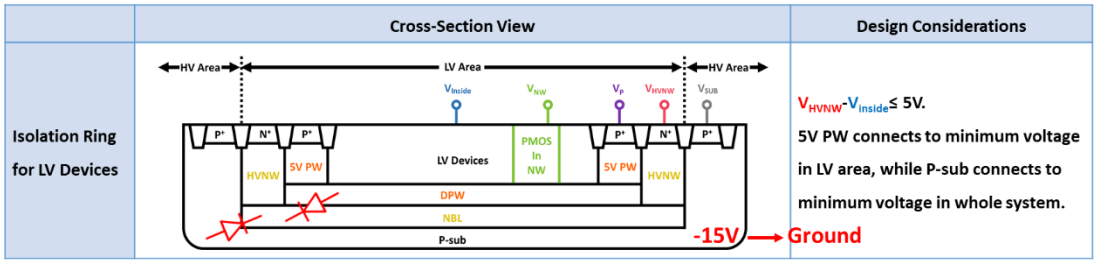


(a) (b)

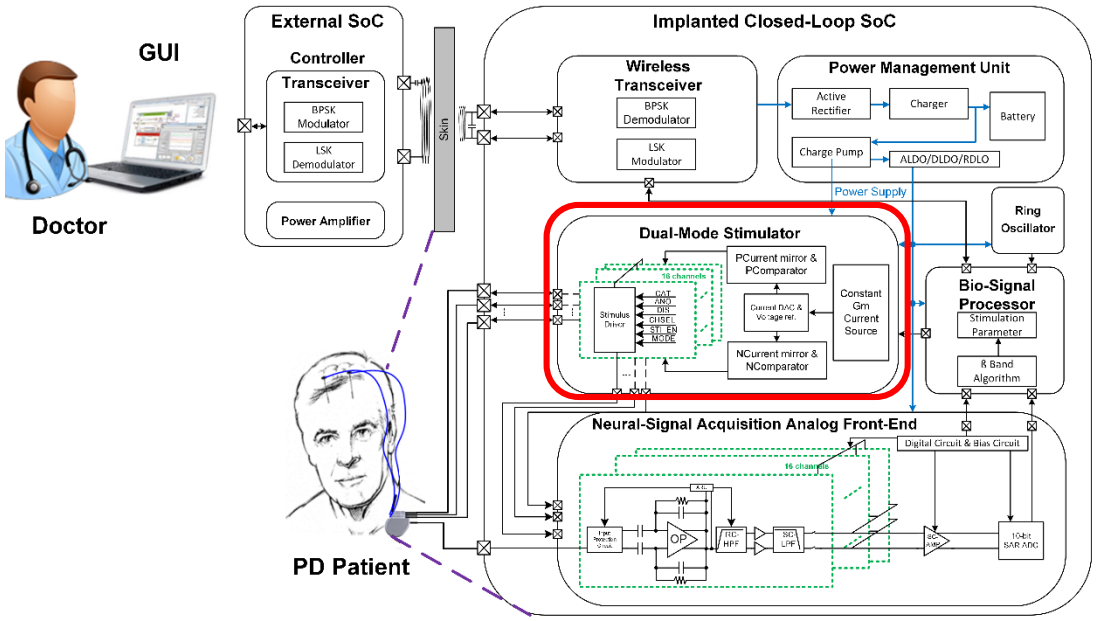
Fig. 4.2 (a) Parasitic capacitance when the switch is on the right side. (b) Modified layout of parasitic capacitance when the switch is moved to the left side.

4.2.3 SoC Integration of HV Dual-Mode Stimulator

Fig. 4.3 demonstrated the constraints of isolation ring in 0.18μm HVGen2 CMOS process and the block diagram of implantable SoC. Since the isolation ring has a rule that $V_{HVNW} - V_{inside} \leq 5V$, if p-substrate is grounded, LV devices cannot be used in voltages lower than -5V; otherwise, the voltage of HVNW will be lower than ground and cause p-n junction forward leakage. However, biasing -15V for p-substrate may cause problems during the power-on process and leakage on the PCB board. Besides, the grounded p-substrate is more common in circuit design and better for SoC integration. As a result, the LV devices should be replaced by HV devices in future work, with Vgs=5.5V constraints considered. Above all, this HV dual-mode stimulator can be integrated on SoC and used for DBS treatment in the future.



(a)



(b)

Fig. 4.3 (a) Constraints of isolation ring (b) SoC integration.

References

[1] C. O. Oluigbo and A. R. Rezai, "Addressing neurological disorders with neuromodulation," *IEEE Transactions on Biomedical Engineering*, vol. 58, no. 7, pp. 1907–1917, July 2011.

[2] G. Alon, "Functional electrical stimulation (FES): clinical successes and failures to date," *Journal of Novel Physiotherapy and Rehabilitation*, vol. 2, pp. 080–086, 2018.

[3] B. D. Popovic, J. Watt, R. B. Stein, J. Raso and T. Overton, "Functional electrical stimulation in the rehabilitation of the spinal cord injured child," in *Proc. IEEE Engineering in Medicine and Biology Society*, 1991, pp. 938-939.

[4] P. C. Loizou, "Introduction to cochlear implants," *IEEE Eng. Med. Biol. Mag.*, vol. 18, no. 1, pp. 32–42, 1999.

[5] E. B. Montgomery, Jr., *Deep Brain Stimulation Programming: Mechanisms, Principles, and Practice*, 2nd ed. Oxford, U.K.: Oxford Univ. Press, 2016.

[6] Islam, A., Alcock, L., Nazarpour, K. *et al.*, "Effect of Parkinson's disease and two therapeutic interventions on muscle activity during walking: a systematic review." *npj Parkinson's Disease*, vol. 6, no. 22, 2020.

[7] E. B. Montgomery Jr., "Deep brain stimulation reduces symptoms of Parkinson disease," *Cleveland Clin. J. Med.*, vol. 66, pp. 9–11, Jan. 1999

[8] P. Ashby, G. Paradiso, J. A. SaintCyr, R. Chen, A. E. Lang, and A. M. Lozano, "Potentials recorded at the scalp by stimulation near the human subthalamic nucleus," *Clin. Neurophys.*, vol. 112, no. 3, pp. 431–437, Mar. 2001

[9] F. Alonso, "Models and simulations of the electric field in deep brain stimulation : comparison of lead designs, operating modes and tissue conductivity," PhD dissertation, Linköping University Electronic Press, Linköping, 2018.

[10] S. Miocinovic, M. Parent, C. R. Butson, P. J. Hahn, G. S. Russo, J. L. Vitek, and C. C. McIntyre, "Computational analysis of subthalamic nucleus and lenticular fasciculus activation during therapeutic deep brain stimulation," *J. Neurophysiol.*, vol. 96, pp. 1569–1580, 2006.

[11] D. R. Merrill, M. Bikson, and J. G. R. Jefferys, "Electrical stimulation of excitable tissue: Design of efficacious and safe protocols," *J. Neurosci. Methods*, vol. 141, pp. 171–198, 2005.

[12] X. F. Wei and W. M. Grill, "Impedance characteristics of deep brain stimulation electrodes in vitro and in vivo," *J. Neural Eng.*, vol. 6, no. 4, Aug. 2009.

[13] J. Gomez-Tames, T. Kutsuna, M. Tamura, Y. Muragaki, and A. Hirata, "Intraoperative direct subcortical stimulation: Comparison of monopolar and bipolar stimulation," *Phys. Med. Biol.*, vol. 63, no. 22, p. 225013, Nov. 2018.

[14] C.-C. Hsieh, "Design of multi-channel monopolar biphasic voltage stimulator for implantable biomedical applications," Master's thesis, Dept. of Elect. Eng., NCTU, Taiwan, 2018.

[15] L. S. Robblee and T. L. Rose, "Electrochemical guidelines for selection of protocols and electrode materials for neural stimulation," in *Neural Prostheses—Fundamental Studies*, Prentice Hall, Englewood Cliffs, NJ, pp. 25–66, 1990.

[16] R. V. Shannon, "A model of safe levels for electrical stimulation," *IEEE Trans. Biomed. Eng.*, vol. 39, no.4, pp. 424–426, Apr. 1992.

[17] J. G. Habets, M. Heijmans, M. L. Kuijf, M. L. Janssen, Y. Temel, and P. L. Kubben, "An update on adaptive deep brain stimulation in parkinson's disease," *Movement Disorders*, vol. 33, no. 12, pp. 1834–1843, 2018.

[18] J. E. Fleming, E. Dunn, and M. M. Lowery, "Simulation of closed-loop deep brain stimulation control schemes for suppression of pathological beta oscillations in Parkinson's disease," *Front. Neurosci*., vol. 14, p. 166, Mar. 2020.

[19] T.-Y. Yen and M.-D. Ker, "Design of dual-mode stimulus chip with built-in high voltage generator for biomedical applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 14, no. 5, pp. 961-970, Oct. 2020.

[20] T.-J. Hung, "Design of monopolar biphasic 8-channel current and voltage stimulator for Parkinson's disease," Master's thesis, Dept. of Elect. Eng., NCTU, Taiwan, 2019.

[21] P. G. A. Jespers and B. Murmann, "Practical circuit examples I," in *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*, Cambridge: Cambridge University Press, 2017, pp. 114–164.

[22] C.-Y. Wu *et al.*, "Design considerations and clinical applications of closed loop neural disorder control SoCs," in *Proc. IEEE Conference on Design Automation*, 2017, pp. 295–298.

[23] B. Razavi, "The current-steering DAC [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 10, no. 1, pp. 11–15, 2018.

[24] S. F. Cogan, "Neural stimulation and recording electrodes," *Annual review of biomedical engineering*, vol. 10, pp. 275–309, May 2008.

[25] R. Ramasubbu, S. Lang, and Z. H. T. Kiss, "Dosing of electrical parameters in deep brain stimulation (DBS) for intractable depression: a review of clinical studies," *Frontiers in Psychiatry*, vol. 9, p. 302, July 2018.

[26] T.-Y. Yang, “Design of 16-channel biphasic stimulus driver to suppress epileptic seizure in the low voltage process,” Master’s thesis, Dept. of Elect. Eng., NCTU, Taiwan, 2015.

[27] W.-H. Cheng, “Design of high-voltage generator with low supply peak current for biomedical applications,” Master’s thesis, Dept. of Elect. Eng., NCTU, Taiwan, 2015.

[28] G. S. Jovanovic and M. K. Stojcev, “Current starved delay element with symmetric load,” *International Journal of Electronics*, vol. 93, no. 3, pp. 167–175, 2006.

[29] M. Haas, P. Vogelmann, and M. Ortmanns, “A neuromodulator frontend with reconfigurable class-b current and voltage controlled stimulator,” *IEEE Solid-State Circuits Lett.*, vol. 1, no. 3, pp. 54–57, Mar. 2018.

[30] H. Chun, Y. Yang, and T. Lehmann, “Safety ensuring retinal prosthesis with precise charge balance and low power consumption,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 1, pp. 108–118, May 2013.

[31] M. Kilic and A. Schmid, “An implantable high-voltage cortical stimulator for post-stroke rehabilitation enhancement with high-current driving capacity,” *IEEE International Symposium on Circuits and Systems*, pp. 758–761, 2015.

[32] Z. Luo and M.-D. Ker, "A high-voltage-tolerant and power-efficient stimulator with adaptive power supply realized in low-voltage CMOS process for implantable biomedical applications," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 8, no. 2, pp. 178-186, 2018.

Vita

姓　　名：蕭榆潔

學　　歷：

高雄市立高雄女子高級中學　　(100 年 9 月~103 年 6 月)

國立交通大學電子工程學系　　(103 年 9 月~107 年 6 月)

國立交通大學電子研究所　　(107 年 9 月~110 年 1 月)

研究所修習課程:

積體電路之靜電防護設計特論	柯明道 教授
醫學工程概論	鄭裕庭 教授
電源管理晶片設計與實作	陳柏宏 教授
類比積體電路	吳介琮 教授
數位積體電路(英文班)	黃威　 教授
計算機結構	劉志尉 教授
前瞻類比積體電路	洪浩喬 教授
功率積體電路	陳柏宏 教授

Email：miyajessie.ee07g@nctu.edu.tw