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堆疊式場效電晶體防護結構在跨域元件充電模式之靜電放電防護設計與驗證

Design of Stacking-MOS Protection Structure for Interface Circuits against Cross-Domain CDM ESD Stresses

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摘要

對於先進 CMOS 技術中的積體電路 (IC)，靜電放電(Electrostatic Discharge, ESD)仍然是現今積體電路中最具挑戰性的可靠度議題之一。出於電路性能、面積成本和功率消耗的考量，積體電路技術遵循摩爾定律而持續微縮，以達到更高的電晶體密度與更強大的性能。隨著電子消費性展品的多樣化，積體電路朝向系統單晶片（SoC）應用的發展，將複雜的電路與功能區塊整合於單一晶片以符合實際應用需求。伴隨積體電路設計的複雜化，為了實現電源管理和電源雜訊隔離等需求，勢必會將多個電源域整合於單一晶片之中，以供應不同電路區塊之獨立電源。此外，先進積體電路技術採用短通道電晶體提升電路操作及運算的速度，同時為了避免可靠度、短通道效應和功率消耗等問題，應用電壓也必須隨之降低，

而必須實現更薄的電晶體柵極氧化層以達到高性能。然而，這並不利於靜電放電防護電路的設計，並導致積體電路內部的元件充電模式(Charged-Device Model, CDM)靜電放電更為嚴重，特別是在跨域靜電放電應力之下，擁有各自獨立電源區塊之間的介面電路容易因快速暫態過壓而損壞。這使得跨域介面電路之元件充電模式靜電放電防護設計成為至關重要的問題，因此，本論文針對急需被解決的介面電路進行架構上的設計與改良，作為本次研究的核心價值。

本論文首先探討跨域電路的靜電放電潛在威脅，接著概觀現今已發表的跨域靜電放電防護設計，分析不同的設計技巧與應用層面，以進一步了解設計之策略。已發表的各種本地箝位電路設計有助於解決介面電路所面臨的瞬態過壓問題，然而，需要配置額外的面積施作防護電路，且經常伴隨著應用層面的限制與性能的下降。因此，本論文提出了截然不同的一種新型保護電路設計方法，使用具有堆疊的頭/尾場效電晶體結構以抵抗跨域元件充電模式下的靜電放電應力，於 0.18-μm 1.8-V CMOS 製程技術中進行了實驗設計、電路模擬與晶片實現，並獲得成功的驗證。此外，還詳細研究不同連接方式的堆疊場效電晶體結構之間在訊號傳輸或靜電轟擊下的差異性。跨域測試電路的實驗結果包含應用非常快速傳輸線脈衝(VF-TLP)之跨域靜電測試、跨域元件充電模式和跨域人體模式，都顯示堆疊場效電晶體防護結構具有更好的 ESD 穩健性。著重於 CDM 穩健性考量所有介面電路設計，接收端堆疊設計搭配栓鎖連接(Rx-Latch)具有最好的保護效果，而傳輸端堆疊設計均有一致且顯著的保護效果。若將其餘跨域靜電測試結果納入考量，傳輸端堆疊設計搭配栓鎖連接(Tx-Latch)會是傳輸端最佳的改良方式，歸因於整體良好的保護效果及面積效益。CDM 和 VF-TLP 的實驗結果顯示在 VDD2 與 VSS1 之間的放電路徑並未良好地被設計，由於電源軌 ESD 箝位電路中主要放電的元件具有淺溝渠隔離結構，導致啟動速度過慢，而無法應對快速放電事件。最後，測試晶片於 CDM 測試後進行失效分析，驗證了典型的 CDM 失效機制，每組測試電路都顯示接收端電晶體的閘極氧化層損壞，符合原先設計的預期。由此證實，預測的 CDM 電路模擬方法具有定性分析介面電路瞬態過壓的重要價值。

Design of Stacking-MOS Protection Structure for Interface Circuits against Cross-Domain CDM ESD Stresses

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Abstract

Electrostatic discharge (ESD) is a challenging reliability issue for integrated circuits (ICs) in advanced CMOS technology. For the consideration of circuit performance, area cost, and power consumption, integrated circuit technology follows Moore's law and continues to shrink for achieving higher transistor density and more powerful performance. With the development of ICs toward system-on-chip (SoC) applications, it has been often to integrate multiple power domains into a single chip for power management or noise isolation considerations. Besides, the fabricated transistors with thinner gate oxide for high-speed operation cause the ICs more sensitive

to charged-device model (CDM) ESD events, especially under cross-domain stresses. The interface circuit between independent power domains is easily damaged by fast transient overvoltage. This makes the cross-domain CDM ESD protection more and more important. For circuit integration and CDM protection, this work focus on the design and improvement of the interface circuit which needs to be solved urgently.

First of all, the internal ESD threats under cross-domain stresses were discussed. An overview of the prior arts, which have been published for cross-domain ESD protection design, was organized to analyze different design techniques and application fields to further understand design strategies. Various local clamp circuit designs have been published to solve the transient overvoltage issue of interface circuits. However, additional areas need to be configured for protection circuits, resulting in application restrictions and performance degradation. Hence, a new protection design with stacking footer/header MOS structure against cross-domain CDM ESD stresses was proposed in this work and verified in TSMC 0.18-μm 1.8-V CMOS technology. Also, the differences in signal transmission or ESD robustness between different interconnection with the stacking-MOS structure are studied in detail. The experimental results of the cross-domain test circuit include the cross-domain ESD test using a very fast transmission line pulse (VF-TLP), the cross-domain charge device model (CDM), and the cross-domain human body model (HBM), show that the stacking-MOS structures have better ESD robustness. Focusing on the CDM robustness, the stacking-MOS design of the receiver with latch connection (Rx-Latch) has the best protection capability, while the stacking-MOS designs of the transmitter with various connections have a consistent and significant protection capability. If else cross-domain ESD test results are taken into consideration, the stacking-MOS design of the transmitter with a latch connection (Tx-Latch) will be the best choice for transmitters, due to the good ESD robustness and area efficiency among them. Moreover, the experimental results of

CDM and VF-TLP show that the discharge path between VDD2 and VSS1 was not well designed. Because the main device in the power-rail ESD clamp circuit 2 has shallow trench isolation (STI) structure, which limits the turn-on speed and unable to respond to fast discharge events. In the end, the CDM test chip was implemented failure analysis after CDM tests to verify the typical failure mechanism. As a result, each test circuit shows the gate-oxide damage of the receiver MOS transistor, which reveals that the predictive CDM circuit simulation method has a significant value of qualitatively analyzing the transient overvoltage of interface circuits.

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Chapter 1
Introduction

This chapter is divided into six sections. The motivation of this thesis is illustrated in 1.1. The introduction of ESD and classic test models are illustrated in 1.2. The CDM ESD threats for CMOS ICs are briefly discussed in 1.3. The internal ESD threats under cross-domain ESD stresses are discussed in 1.4. The prior arts of cross-domain ESD protection design are introduced in 1.5. Finally, the organization of this thesis is illustrated in 1.6.

1.1 Motivation

Electrostatic discharge (ESD) is one of the most important issues on the reliability of IC products. While the CMOS technologies scaled-down, the CDM ESD issue has become more critical because of the thinner gate oxide in larger chip size. With the continuous development of integrated circuits (ICs) in the direction of System-on-Chip (SoC) applications, multiple independent power domains in an IC are requested by different circuit blocks, such as mixed-voltage, mixed-signal, and power management applications [1]–[6]. The supply voltage of core circuits was often reduced to save power consumption, while others may still require the separated power domains for circuit performance and noise isolation, especially for analog/RF circuits with higher noise sensitivity and SNR requirements.

Unfortunately, the interface circuits between the separated power domains are very sensitive to ESD events. Some efforts had been developed to avoid ESD damages at the

cross-domain interface circuits [1]–[16]. During ESD stress across separated power domains, the whole-chip ESD protection can be established with the assistance of power-rail ESD clamp circuits and bi-directional diodes to conduct ESD currents away from the interface circuits between different domains. However, closer to the actual situation, the bi-directional diodes were connected barely between the separated VSS power lines. Apart from this, some additional local ESD clamps were placed nearby the interface circuits to further reduce overstress voltages during ESD stresses [1]–[16]. Although some solutions were ever made, the cross-domain ESD stress is still a challenging issue in recent years.

With concerns of CDM ESD protection, the cross-domain interface is the most vulnerable situation. The CDM charges are mostly accumulated in the common p-substrate when the IC is initially floating, which would be discharged through the VDD/VSS metal lines from the internal circuit blocks during CDM ESD events to cause gate-oxide damages at the interface circuits between the separated power domains. To further prevent this kind of CDM damage, a new protection design with stacking footer/header MOS structure against cross-domain CDM ESD stresses was proposed and verified in this thesis.

1.2 Introduction of ESD and Classic Test Models

Electrostatic is a phenomenon of losing or obtaining electrons on the surface of the material through friction or induction, making the space charge static. When electrostatic transfers between two objects with different potentials, the electrostatic discharge (ESD) will happen and may be accompanied by arcs or sparks. Specifically, ESD is an instantaneous charge flow between two objects, such as little sparks that appears when touching metal conductors in a dry environment or lightning and thunder in nature are all kinds of ESD events.

As ESD problems are introduced in the production and manufacturing process, IC will inevitably suffer various ESD damages, which can be analyzed and appropriately classified. During the process of fabrication, package, test, and human processing, lots of environmental factors will result in different types of ESD on wafers. Therefore, the purpose of the ESD model is to establish a test method to solve ESD problems and provide technical support. Currently, the human body model (HBM), machine model (MM), and charging device model (CDM) are the main ESD test models used in industry, supporting the simulation of ESD events generated from various environments.

1.2.1 Human Body Model (HBM)

HBM is one of the typical ESD test models. As the name implies, HBM simulates the accumulation of electrostatic in the human body due to friction or induction. While the charged body touches an equivalently grounded IC or electronic component, a discharge event will be generated by charge displacement, thereby destroying the circuit or component. The simplified equivalent circuit is shown in Fig. 1.1. The C_{HBM} (100pF) and R_{HBM} (1.5kΩ) represent the equivalent capacitance and resistance of the human body, respectively. First, the switch is closed through node A, and the capacitor C_{HBM} will switch to HV supply through the charging resistor (R_{Charge}) to the specified ESD level. The C_{HBM} and R_{Charge} dominate the time constant of charge and discharge procedure. After the C_{HBM} accumulates the corresponding charge, the switch is closed to node B, and the charge on the C_{HBM} will be transferred to the device under test (DUT) through the R_{HBM} to form a discharge path and release ESD energy to the DUT.

A typical transient HBM current waveform is shown in Fig. 1.2 The HV supply is set to 2kV, and the relative charge is generated on the C_{HBM}, and then instantly switched to R_{HBM} and DUT to form a discharge loop. Assuming that the turn-on resistance (R_{on}) of DUT is quite small, the current waveform can be approximated as RC charging and

discharging process. The peak current (I_{peak}) is about 1.33A, the rise time (t_r) is about 10ns, and the pulse duration time (t_d) of the HBM current tail is about hundreds of ns. One can refer to the ESDA/JEDEC joint standard JS-001 for relevant information [17].

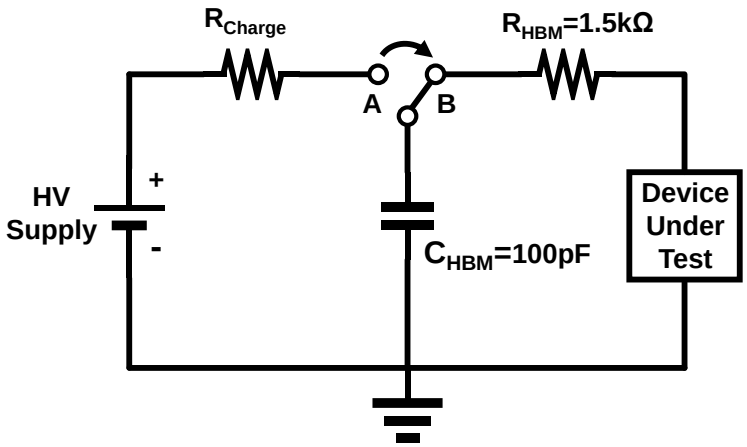


Fig. 1.1. The simplified equivalent circuit of the human body model (HBM)

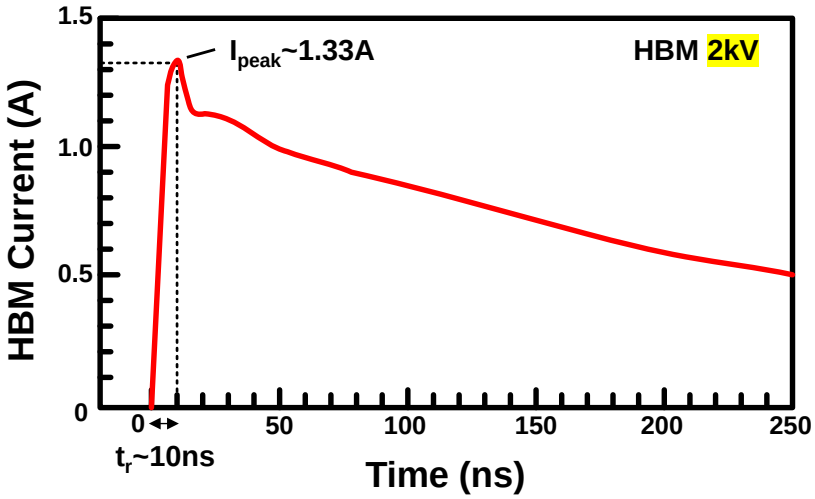


Fig. 1.2. A typical transient ESD current waveform of HBM 2kV

1.2.2 Machine Model (MM)

Usually, mass production relies on lots of metal machines, which are accompanied by much lower equivalent resistance than the human body. Hence, the MM, originally developed in Japan, was created in response to the worst case of HBM ESD events. The simplified equivalent circuit is shown in Fig. 1.3, to emulate the discharging of charged machines (metal tools, mechanical arms), the C_{MM} (200pF) represents the equivalent capacitance of conductive objects, and the RMM (0Ω) represents the equivalent

resistance for low resistance discharge paths. However, many results show that MM is redundant for the human body model (HBM) since similar failure mechanisms are observed by each other, and the ESD robustness of the two models usually tracks each other. As a result, the test model has been quickly eliminated throughout the industry.

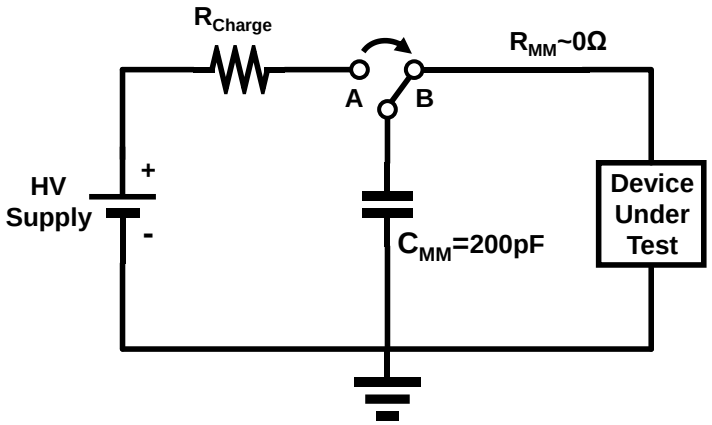


Fig. 1.3. The simplified equivalent circuit of the machine model (MM)

1.2.3 Charge Device Model (CDM)

Unlike HBM or MM, CDM simulates a device charged by triboelectric effect or electrostatic induction. The CDM charge is initially stored inside the IC, when the IC's pins are touched or grounded instantly, the charge is transferred from the IC's internal circuit to an external conductive object. The simplified equivalent circuit is shown in Fig. 1.4, where DUT is placed with C_{CDM} on the charging path. Note that, DUT can be expressed as the composition of equivalent resistance (R_{DUT}), and parasitic inductor caused by metal routing and wire bonding (L_{DUT}), respectively. Initially, the switch is closed to A to charing the DUT by HV supply. After a while, the switch is closed to B, and the discharge path is established, indicating the internal charge flows out, and through the core circuit to the external ground. Notably, since the C_{CDM} depends on the circuit design, wafer thickness, die size, layout style, package form, and various situations, the current flows through IC becomes unpredictable. For the reasons, CDM events are much more complicated than HBM and MM. Thus, most ESD protection

circuits/devices are used to provide a direct discharge path from the I/O pad to the VDD/VSS rail in HBM and MM events.

A typical transient CDM current waveform is shown in Fig. 1.5. The HV supply is set to 500V, and the relative charge is generated on the CCDM, and then instantly switched to the ground to form a discharge loop with R_{DUT} and L_{DUT}. Assuming that the RDUT is quite small, the current loop can be approximated as the RLC series resonance, which leads the waveform to oscillate significantly. The peak current (I_{peak}) is about 6A, and the rise time (t_r) is about 200ps for the small capacitor module. One can refer to the ESDA/JEDEC joint standard JS-002 for relevant information [18].

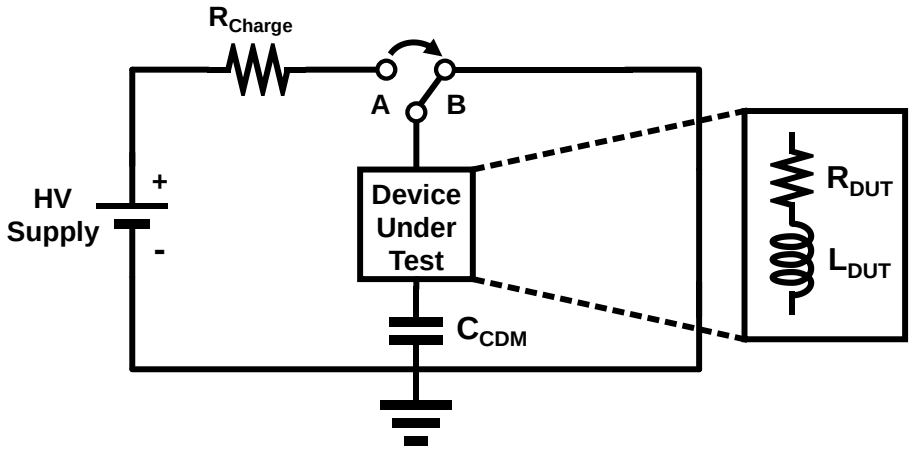


Fig. 1.4. The simplified equivalent circuit of charged device model (CDM)

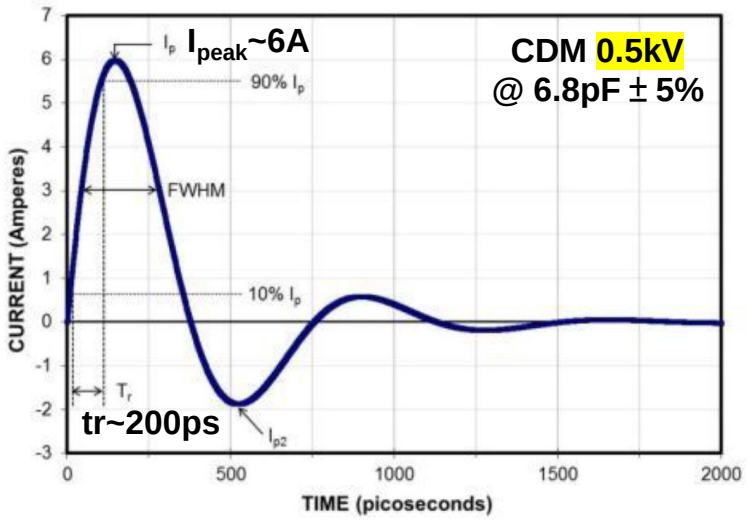


Fig. 1.5. A typical transient ESD current waveform of CDM 500V

1.3 CDM ESD Threats for CMOS Integrated Circuits

As the manufacturing process continues to evolve, to achieve better chip processing performance and complex calculations, while taking into account requirements such as speed, area, and power consumption, the size of the transistor and the operating voltage must be reduced along with the evolution. However, in the device structure of the advanced process technology, the gate-oxide thickness is getting thinner and thinner to improve the driving ability. At the same time, the physical mechanism of the CDM ESD event is due to the steps of the wafer manufacturing process such as diffusion, lithography, etching, deposition, and grinding, etc. These procedures generate some positive or negative CDM charges stored in the common p-substrate of the wafer bottom, which is a large enough area to store a large amount of charge. After wafer-out and enters the packaging and testing level, the I/O pins are easy to be touched, and the potential difference will generate a huge displacement current releases the charge stored inside the chip to an external grounded object.

The displacement current is dominated by the parasitic capacitance of the die and the potential difference, that is, the amount of stored charge. The large capacitance region, which is the gate-oxide of metal-oxide-semiconductor (MOS) transistor, inside the chip would be dangerous and vulnerable. Therefore, the typical CDM ESD failure is often accompanied by the gate-oxide breakdown, as shown in Fig. 1.6.

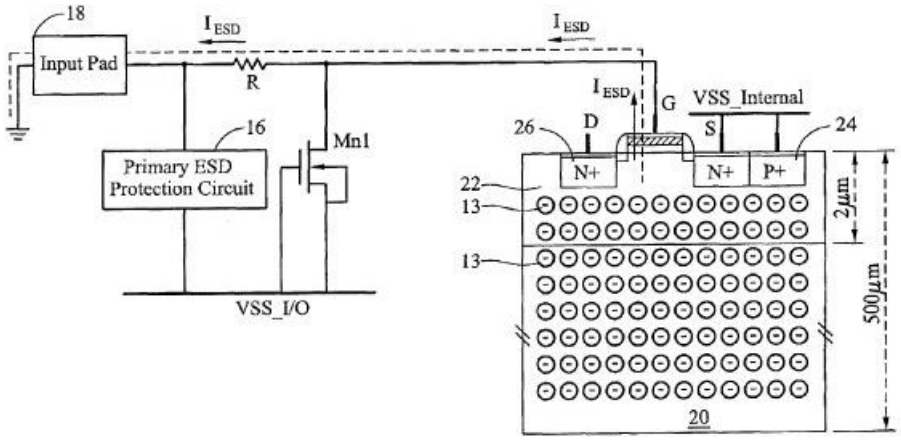


Fig. 1.6. A typical CDM ESD failure causes a gate-oxide breakdown [19].

The reference current waveform of CDM ESD is shown in Fig. 1.7. For detailed values, please refer to the international JEDEC standard of CDM test (JS-002) [18]. In content, different capacitor modules are used to calibrate the CDM tester, and list key factors and specific ranges of the discharge waveform for different test condition, as shown in Table 1.1. Under CDM stress, with peak currents reaching 5A or more for large packages, and rise times below 450ns or less, this can be significant. As known, CDM ESD will release a lot of energy in a fast transient. Therefore, in various ESD events, CDM has the most significant destructions, and more effective protection designs are urgent to need, especially for advanced technologies commonly used in the industry.

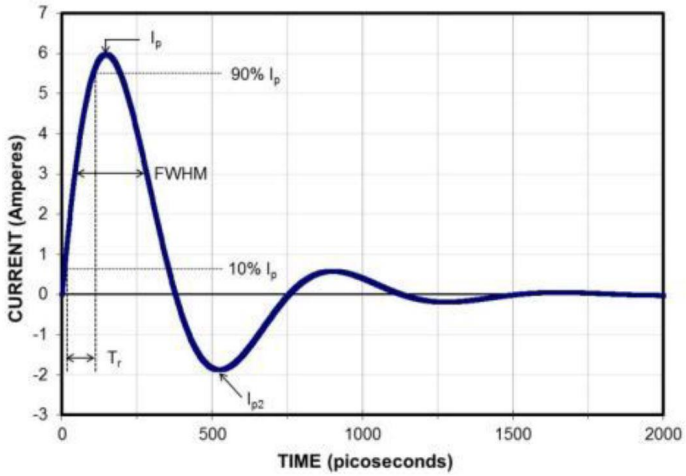


Fig. 1.7. The reference CDM characteristic current waveform and parameters [18].

Table 1.1

CDM Waveform Characteristics for a 1 GHz Bandwidth Oscilloscope [18]

1 GHz BW Oscilloscope		Test Condition									
		TC 125		TC 250		TC 500		TC 750		TC 1000	
Verification Module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak Current (A)	Ip	1.0-1.6	1.9-3.2	2.1-3.1	4.2-6.3	4.4-5.9	9.1-12.3	6.6-8.9	13.7-18.5	8.8-11.9	18.3-24.7
Rise time (ps)	Tr	<350	<450	<350	<450	<350	<450	<350	<450	<350	<450
Full width at half maximum (ps)	FWHM	325-725	500-1000	325-725	500-1000	325-725	500-1000	325-725	500-1000	325-725	500-1000
Undershoot (A, max. 2nd peak)	Ip_2	<70% Ip	<50% Ip	<70% Ip	<50% Ip	<70% Ip	<50% Ip	<70% Ip	<50% Ip	<70% Ip	<50% Ip

To integrate more functional blocks with complex power domains into a single SoC IC, the chip size would be inevitably increased, and the packaging styles of the chip were also developing towards a thinner form, to facilitate the realization of stacking technologies such as 2.5D and 3D ICs. This type of IC usually has a larger die parasitic capacitance (C_{die}), which leads to a larger CDM current peak value. Even if sufficient ESD protection circuits are embedded into the I/O ring around the IC, the internal core circuit cannot be well protected because of CDM. The physical mechanism of CDM discharge is to transfer the charge from the internal circuit to the external I/O pad. This process often causes the gate-oxide breakdown along the path, as shown in Fig. 1.8.

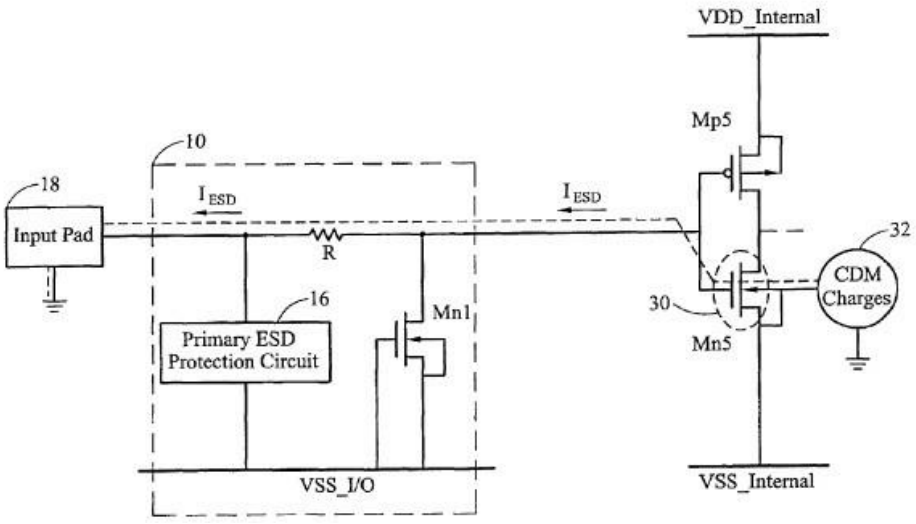


Fig. 1.8. The gate-oxide damage since the CDM charge transfer from common p-substrate to external grounded pad through internal circuits. [19]

At present, many works of literature have pointed out the common four cases of damage that CDM can easily cause in the chip. Here are listed in sequence, the gate-oxide damaged of the I/O devices, the gates of the internal devices are directly connected to power or ground bus, a longer signal path without parasitic diode, cross-power domain interface. The most critical case is the damage of the cross-power domain interface circuit because most of the fatal CDM charge is prone to accumulate on the power/ground metal bus. Until the discharge current path crosses separated power domains, it is easy to damage the gate-oxide at the interface. To prevent this kind of CDM from damaging the complex power domain, a series of protection designs would be introduced in Chapter 2. By the way, the improvement of the interface circuit is also crucial to enhance the overall CDM robustness.

1.4 Internal ESD Threats Under Cross-Domain ESD Stresses

Fig. 1.9 illustrates an ESD protection scheme of an IC product with multiple separated power domains. Generally, whole-chip ESD protection consists of an I/O ESD protection circuit for each domain, power-rail ESD clamp circuits between VDD and VSS rails, and bi-directional diodes between VSS rails of different domains.

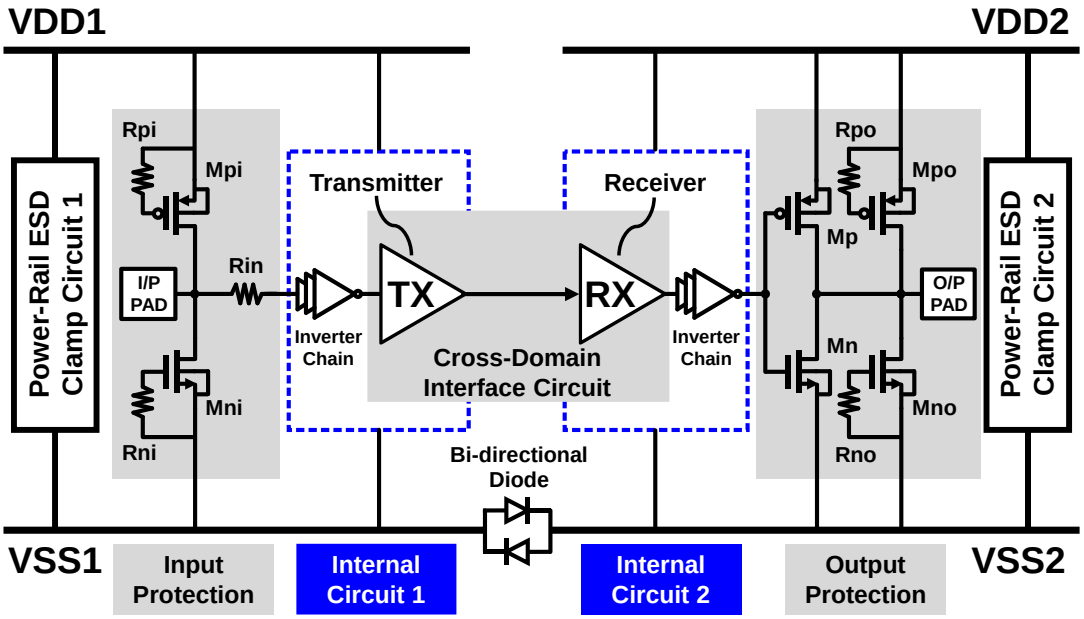


Fig. 1.9. An ESD protection scheme of an IC product with multiple power domains

The input ESD protection is used against pad-to-VDD and pad-to-VSS ESD stresses at the input pad, it consists of gate-grounded NMOS (Mni), gate-VDD PMOS (Mpi), and Rin. The output protection is used for pad-to-VDD and pad-to-VSS ESD protection at the output pad, the driving strength of the output buffer is determined according to the external load, signal operation frequency, and distortion tolerance. Also, by connecting different finger numbers of Mp and Mn to get the appropriate driving current and achieve signal specifications, the other fingers are connected as Mno and Mpo. The power-rail ESD clamp circuit, which consists of an RC-based ESD transient detection circuit and a substrate-triggered field-oxide device (STFOD) [20], is the main ESD device. Both internal circuits 1 and 2 are set as digital circuit blocks between

separate power domains. To ensure the driving capability, the inverter chains, as a tapered buffer, were inserted between I/O ESD protection and the interface circuit. A pair of inverters are set as the transmitter (TX) and the receiver (RX) to represent the interface circuit that transfers signals from the circuit in VDD1/VSS1 domain to VDD2/VSS2 domain.

1.4.1 Cross-Domain ESD Threats

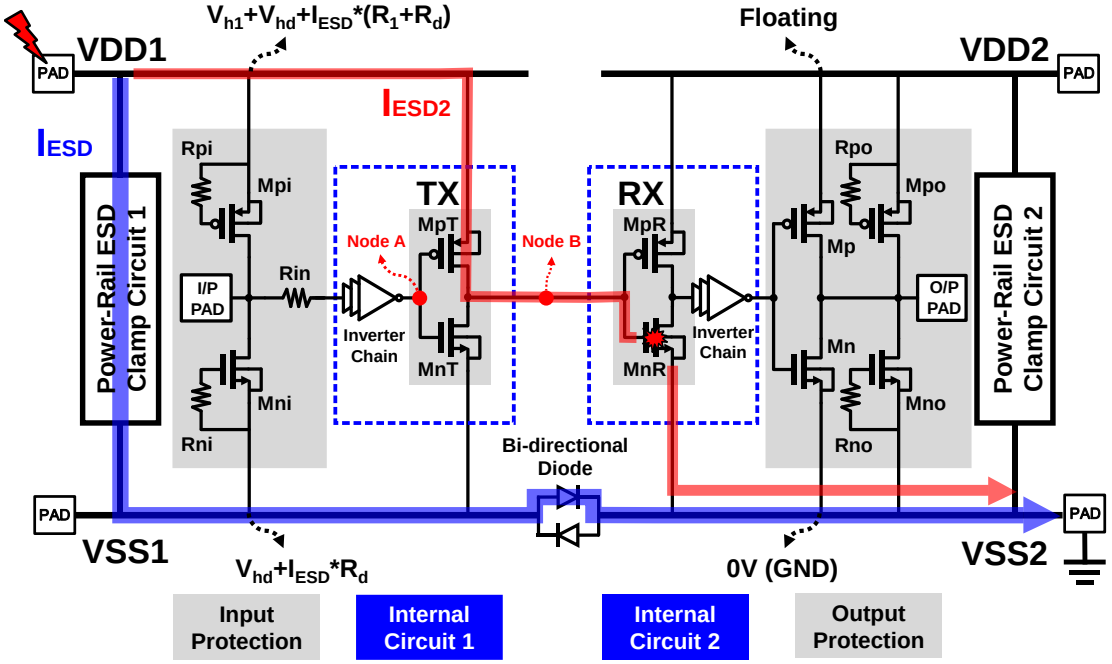
However, the interface circuits are often damaged under cross-domain ESD stresses even with full-chip ESD protection [1]–[16]. In fact, in a fast transient ESD event, the ESD current may find another unexpected path across the domain-crossing circuits before the power-rail ESD clamp bypass the ESD current to the VSS bus. To simplify the voltage drop model, the parasitic resistances of power and ground bus have not been included for explaining, but running the actual circuit simulation must consider these parasitic effects. The cross-domain ESD threats can be divided into four stressing modes to explain separately in the following.

A. VDD1-to-VSS2 Stress (Mode-1)

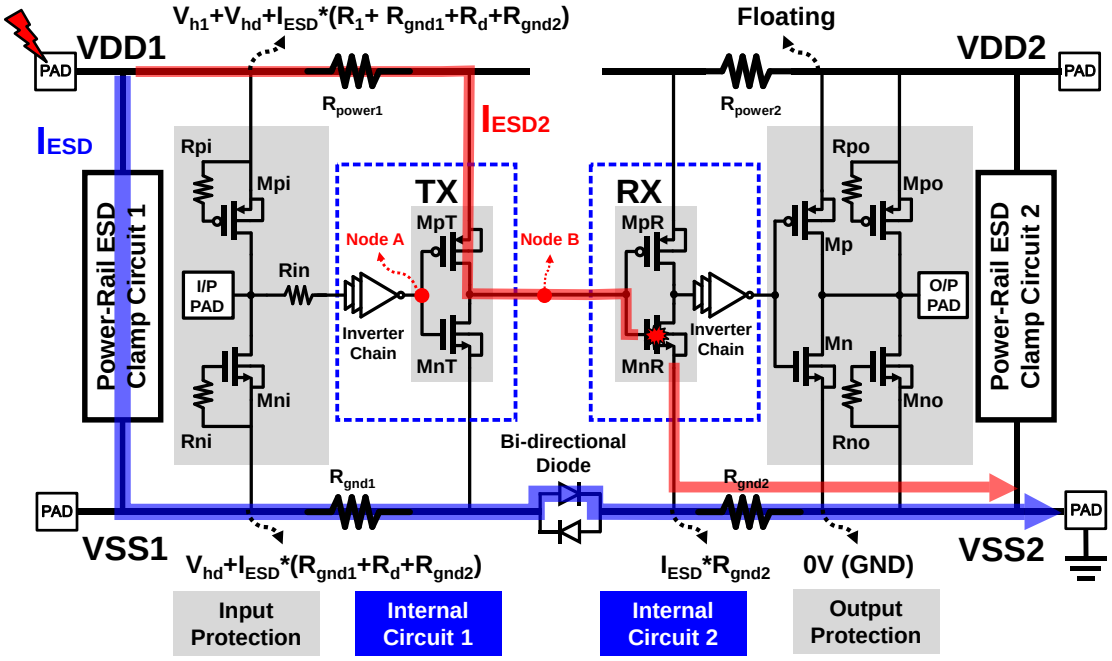
As shown in Fig. 1.10 (a), when the ESD zaps across different power domains, for example, positive ESD stress was applied on VDD1 and grounded VSS2, and the ESD current could be discharged from VDD1 to VSS1 by power-rail ESD clamp circuit 1 in VDD1/VSS1 domain, and then from VSS1 to VSS2 through the bi-directional diode to the VSS2. The V_{h1}/V_{hd} and R_1/R_d are the holding voltage and the turn-on resistance of power-rail ESD clamp circuit 1/bi-directional diode, respectively.

In tradition, the purpose of the power-rail ESD clamp circuit in each domain is to dissipate the ESD current to the VSS rail during a cross-domain ESD event. But, the long current dissipation path I_{ESD1} may induce a large voltage drop between separate power domains. Since the voltage of node A is initially floating, the voltage of node B can be raised to near VDD1 by unexpected path I_{ESD2} through the on-state transmitter's PMOS transistor (M_{pT}) to charge parasitic capacitance in the receiver side, the largest voltage drop will be across the gate-oxide of the receiver's NMOS transistor (M_{nR}). Eventually, the gate-oxide of M_{nR} was destroyed and form a DC leakage path.

For more correct explanations, in this mode, the layout-dependent parasitic effects have been added to the voltage drop model (see Fig. 1.10 (b)) to explain the instantaneous overvoltage generated during cross-domain ESD events. The parasitic resistances of power and ground buses, which are labeled as R_{power} and R_{gnd}, are essential in long discharge paths and normally depend on the complexity of the circuit layout. The actual resistances must be extracted from the physical layout and substituted into circuit models for simulation or analysis in circuit-level design.



(a)



(b)

Fig. 1.10. A positive ESD stress was applied on VDD1 and grounded VSS2 (a) without parasitic resistances and (b) with parasitic resistances.

B. VDD1-to-VDD2 Stress (Mode-2)

Under the VDD1-to-VDD2 stress, it will generate a longer dissipation path than the Mode-1 and induce a larger voltage difference across the interface circuit. As shown in Fig. 1.11, when positive ESD stress was applied on VDD1 and grounded VDD2, a long ESD current dissipation path I_{ESD1} is formed. The ESD current from VSS2 to VDD2 is discharged by power-rail ESD clamp circuit 2. Note that, the V_{h2} and R_2 are holding voltage and equivalent turn-on resistance of the body diodes, respectively. The node voltage of the main ESD dissipation path has been marked in the figure. Since node A is initially floating, node B will be pulled up to a potential near VDD1, and the parasitic capacitance on the receiver side will be charged through the turned-on M_{pT}. Such a discharge mechanism will also generate a large voltage difference between the M_{nR} and M_{pR} at the receiver module and ultimately destroy the gate-oxide, depending on the oxide thickness and breakdown voltage of the RX-NMOS and RX-PMOS. Significantly, Mode-2 stress condition causes more serious and complex failure mechanisms.

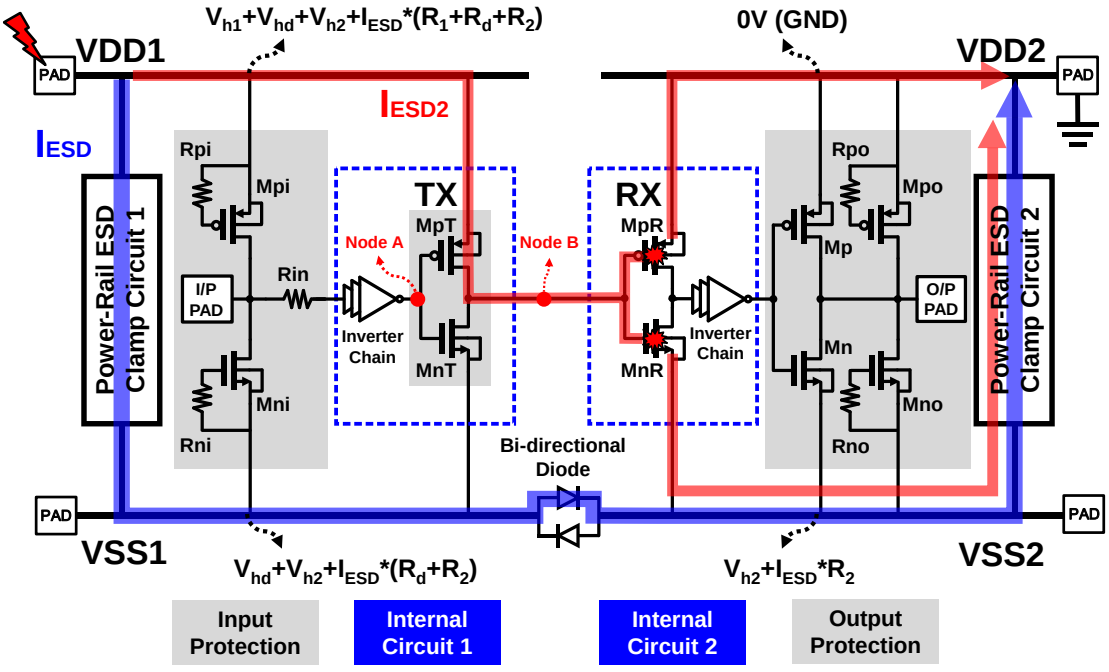


Fig. 1.11. A positive ESD stress was applied on VDD1 and grounded VDD2.

C. VDD2-to-VSS1 Stress (Mode-3)

On the other hand, the VDD2-to-VSS1 stress (see Fig. 1.12), which is the opposite direction of Mode-1, is often not discussed in the existing literature. Because the initial-off RX-PMOS (M_{pR}) exhibits high impedance characteristics during discharge and suppresses unexpected ESD paths flowing to the interface circuits to cause internal damages. Thus, because of the high impedance, ESD energy can be guided to the main dissipation path I_{ESD}. However, the excessive energy of injection will instantaneously pull up the potential of node A, and form a large potential difference across the gate-oxide of M_{pR} since node B is initially floating. For the core device, although the breakdown voltage of PMOS is generally higher than that of NMOS. If the main discharge path is not designed well, the layout is complicated, or the main ESD devices are not uniformly activated, resulting in higher parasitic impedances, which are easy to cause gate-oxide damage of M_{pR}. It may even be worse than Mode-1 or Mode-2.

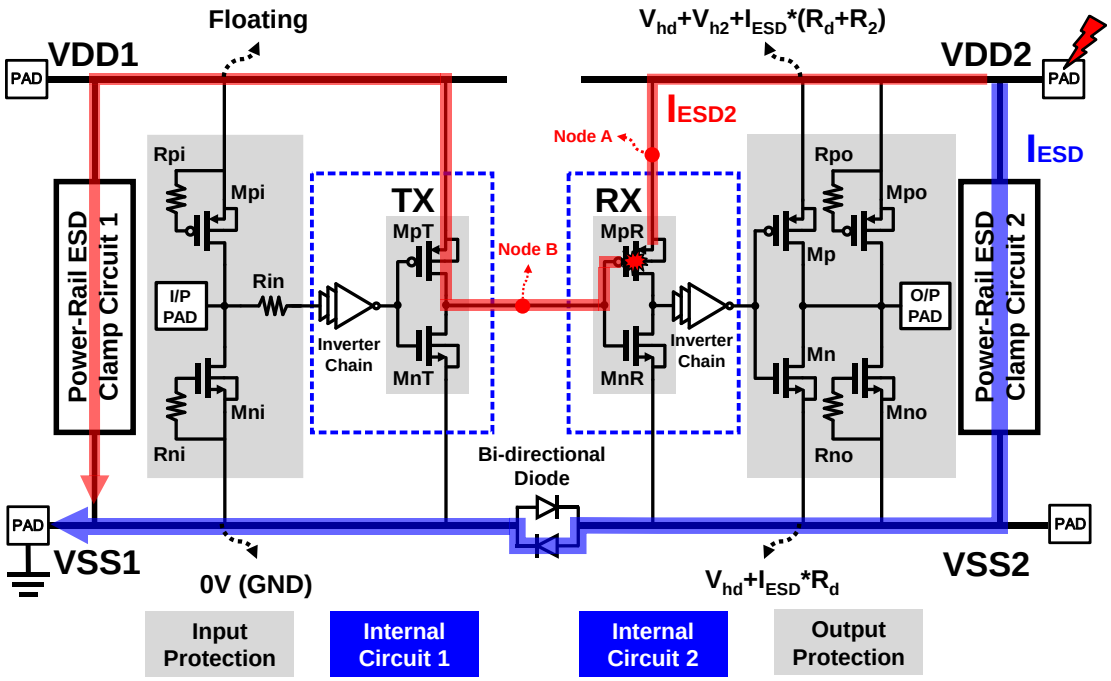


Fig. 1.12. A positive ESD stress was applied on VDD2 and grounded VSS1.

D. VDD2-to-VDD1 Stress (Mode-4)

Similarly, the VDD2-to-VDD1 stress (see Fig. 1.13), which is similar to the aforementioned Mode-3, but accompanied by a longer discharge path and a larger voltage drop. Hence, the RX-PMOS M_{pR} is absolutely a victim device, which is easily damaged, causing unexpected discharge path I_{ESD2}.

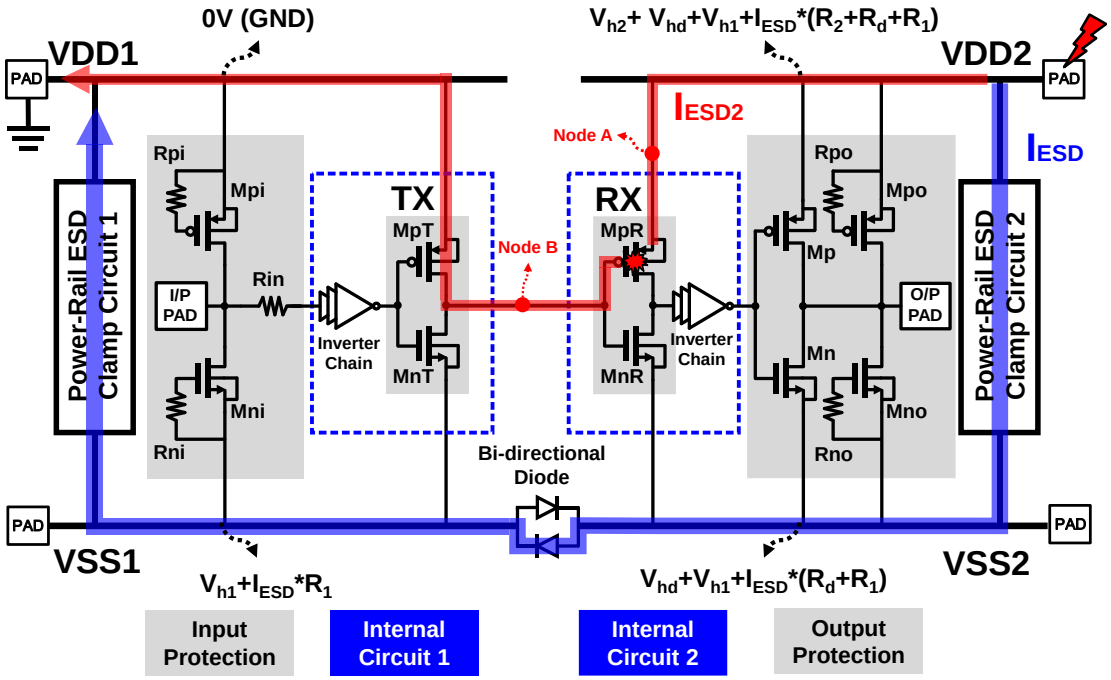


Fig. 1.13. A positive ESD stress was applied on VDD2 and grounded VDD1.

1.4.2 Cross-Domain CDM ESD Threats

CDM events can be applied to the same explanation since the charges are stored in the common p-substrate and connected to the VSS rail. However, the surrounding ESD protection circuit is unable to turn on efficiently because of extremely short rise time and duration time. Significantly, under CDM stress with peak currents reaching 5A or more for large packages, the core transistors of the interface circuit will suffer from voltage overstress and become more critical in advanced process technology. Generally, common cross-domain CDM events can be simply divided into the following two modes.

A. CDM stress performed on VDD1 (Mode-1)

An example is shown in Fig. 1.14, which illustrates a CDM stress performed on VDD1, where RX-NMOS (M_{nR}) is damaged by CDM charge, which is stored in common p-substrate, and then flows through the M_{P1} body diode to the grounded VDD1. In detail, it is assumed that the positive or negative CDM charge (Q_{CDM}) is stored in the common p-substrate inside the IC by inductive charging, where the p-sub is connected to all p-wells of NMOS and VSS buses. While the grounded pogo pin is probed on the VDD1 pad, the instantaneous charge transfer generates a huge displacement current forming a cross-domain CDM issue. Because the VDD2/VSS2 domain circuit is farther away from the VDD1 pin, the interface circuit will suffer more serious damage. Furthermore, the turn-on speed of the ESD protection circuit is critical in such a fast discharge phenomenon. If the turn-on speed is too slow, the gate-oxide of RX-NMOS (M_{nR}) will be broken by the fatal CDM charge, causing damage to the interface circuit.

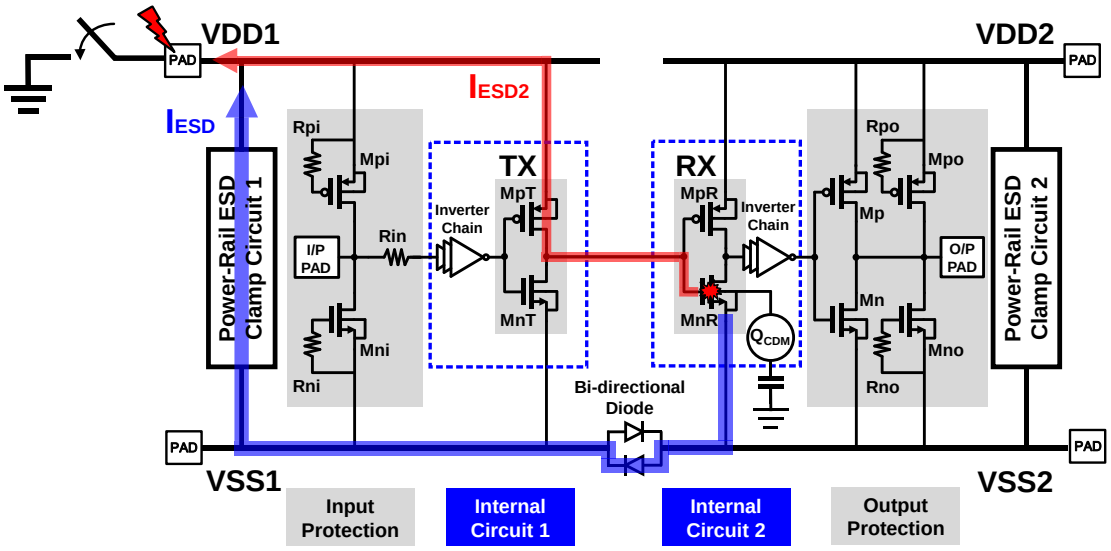


Fig. 1.14. A CDM stress is performed on VDD1 forming a cross-domain CDM ESD event.

B. CDM stress performed on VDD2 (Mode-2)

Similarly, as shown in Fig. 1.15, when the grounded pogo pin is probed on the VDD2 pad, the positive or negative CDM charge stored in VDD1/VSS1 and p-substrate, instantly transfers to form the main discharge path I_{ESD}. However, part of the CDM charge may flow to the gate terminal of M_{pR} through the channel surface or the body diode of M_{nT}, and form a large voltage difference, which will cause the gate-oxide damage of M_{pR}. This kind of phenomenon is strongly dependant on the device size of the TX-NMOS and the parasitic impedance on the main discharge path.

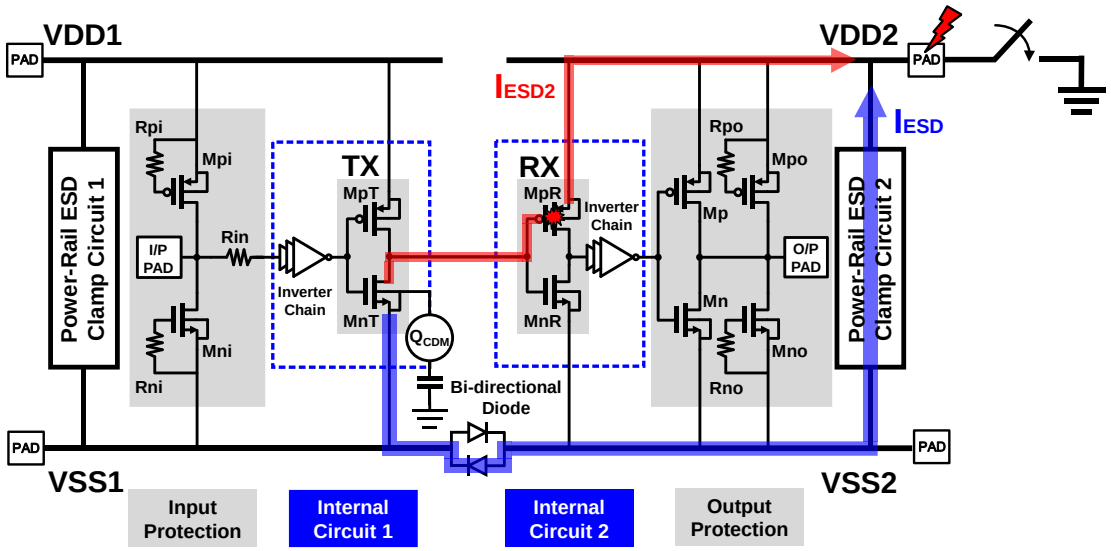


Fig. 1.15. A CDM stress is performed on VDD2 forming a cross-domain CDM ESD event.

1.4.3 Summary

Concerning the CDM protection, the cross-domain interface is the most vulnerable situation as compared with the input gate oxide damaged of I/O devices, the transistor gate directly connected to power or ground rail, and the long signal path without discharge path formed by parasitic junction diode. .Even if there are many failure analysis (FA) procedures, such ESD failures across the domain-crossing circuits are usually difficult to examine and modify [6]. Thus, many EDA tools are currently developing related simulation algorithms to assist IC designers in simulating and analyzing the failure point of cross-domain circuits around the whole chip, and then insert necessary local protection to the corresponding location. However, this kind of simulation methodology still requires lots of experimental databases to achieve higher accuracy. Therefore, improving the ESD robustness of the cross-domain interface circuit is the most straightforward solution.

1.5 Prior Arts of Cross-Domain ESD Protection Design

1.5.1 Gate-Grounded NMOS and Gate-VDD PMOS Design

To prevent this kind of cross-domain CDM damage, a typical second ESD protection design is shown in Fig. 1.16 [1]. The protection design network consists of a series resistor, a pair of gate-ground NMOS (M_{nESD}), and gate-VDD PMOS (M_{pESD}). In general, the M_{nESD} and M_{pESD} are added between the signal line and the VSS/VDD rail, respectively. Both transistors are turned off during normal operation since |vgs| is not high enough to invert the conduction channel. When the ESD event occurs, the collector-base junction of the parasitic NPN/PNP BJT becomes reverse biased to the critical electric field and then induces punch-through breakdown or even avalanche breakdown. As the current flows from the base to the ground through the parasitic resistor, a potential difference will be established across the base-emitter junction, turning on the parasitic NPN BJT and creating the ESD dissipation current path.

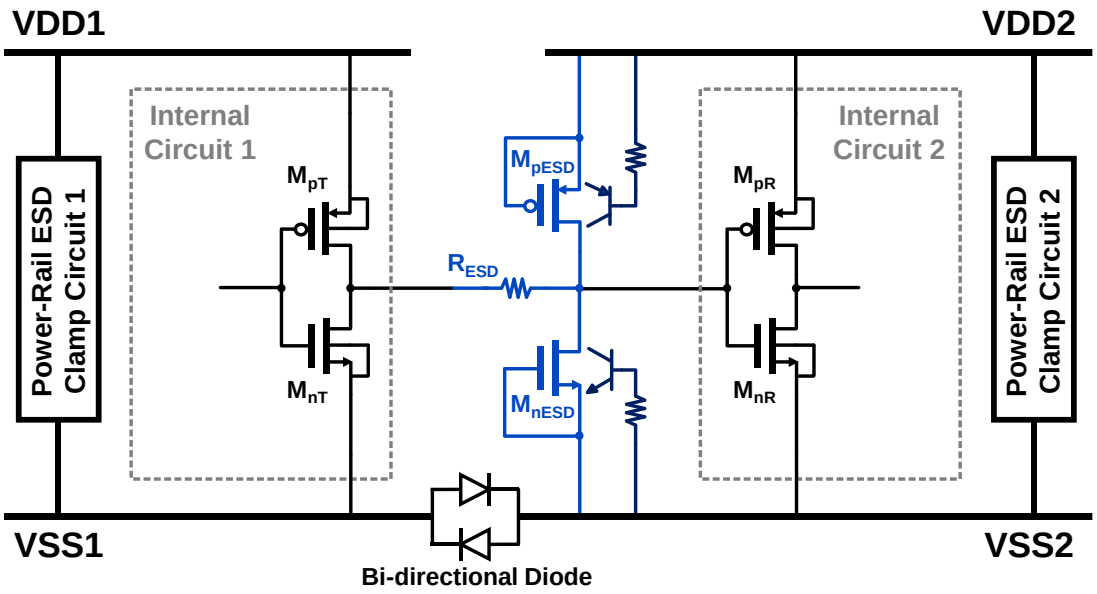


Fig. 1.16. The cross-domain circuit with the 2nd ESD protection circuit consists of the design of GGNMOS and GDPMOS.

1.5.2 Dual Diode Design

Another typical second ESD protection design is shown in Fig. 1.17. The protection design network consists of a series resistor, a pair of diodes. In general, the D_n and D_p are added between the signal line and the VSS/VDD rail, respectively. Both diodes are turned off during normal operation since the voltage drop (V_d) across diodes is not high enough to over than cut-in voltage. When the ESD event occurs, the dual diodes become forward biased or reversed breakdown under various stress conditions. For example, a cross-domain ESD event appears between VDD1 and VSS2 (VDD1-to-VSS2), the ESD current will initially dissipate through the power-rail ESD clamp circuit to the VSS1, and then through the bi-directional diodes to VSS2. As the voltage across the D_p and power-rail ESD clamp circuit 2 is high enough to forward, or even breakdown the reversed D_n, the ESD dissipation current path will be established thereby clamping the cross-domain voltage and protecting the receiver MOS (M_{nR} and M_{pR}). Generally, the 2nd ESD protection transistors or diodes should be placed as close to the gates of the receiver module as possible to minimize the voltage drop during cross-domain CDM ESD events.

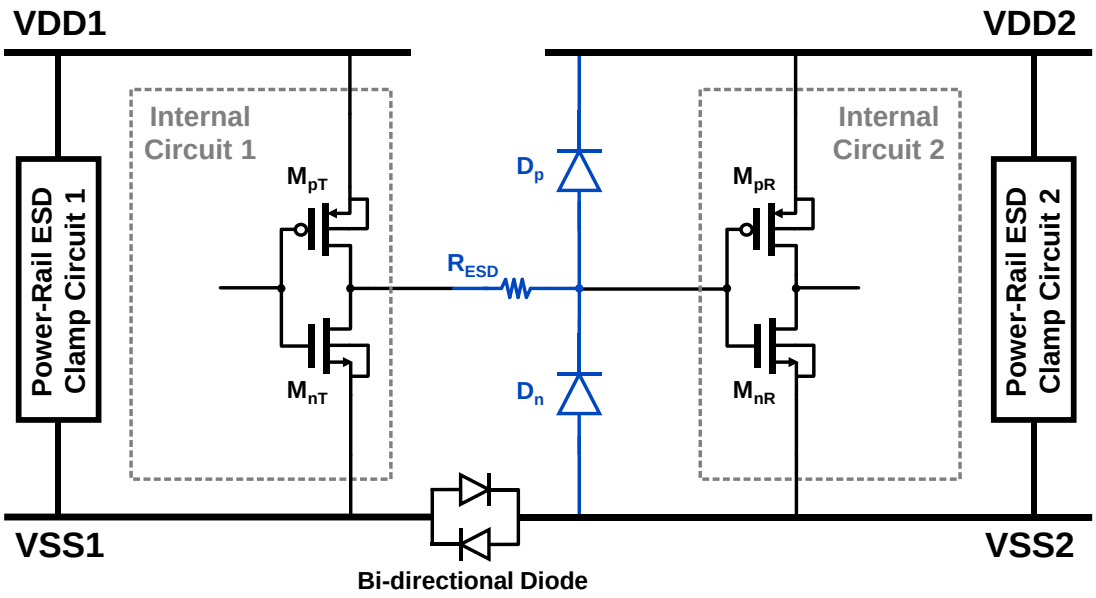


Fig. 1.17. The cross-domain circuit with the 2nd ESD protection circuit consists of the design of a dual diode.

1.5.3 Ground-Current-Trigger (GCT) Technique

A cross-domain circuit with the 2nd ESD protection circuit using the ground-current-trigger (GCT) technique [4], as shown in Fig. 1.18, the gate and the source of an additional NMOS (M_{GCT}) is inserted across the bi-directional diodes, while the drain is connected to the signal line as a local clamp circuit. Under the normal circuit operation, the M_{GCT} is normally turned-off since no potential difference is generated between the VSS1 and the VSS2. While a cross-domain ESD event appears between VDD1 and VSS2 (VDD1-to-VSS2), the ESD current will initially dissipate through the power-rail ESD clamp circuit to the VSS1, and then through the bi-directional diodes. As the voltage drop across the forward diode rises above to higher than the threshold voltage of M_{GCT}, the ground-current trigger effect leads M_{GCT} turned on and operated as a local ESD clamp to protect the thin gate-oxide of the NMOS transistor (M_{nR}) inside the receiver module. Of course, the GCT technique can also be used between the signal line and VDD2 to protect the gate-oxide of the PMOS transistor (M_{pR}) inside the receiver module.

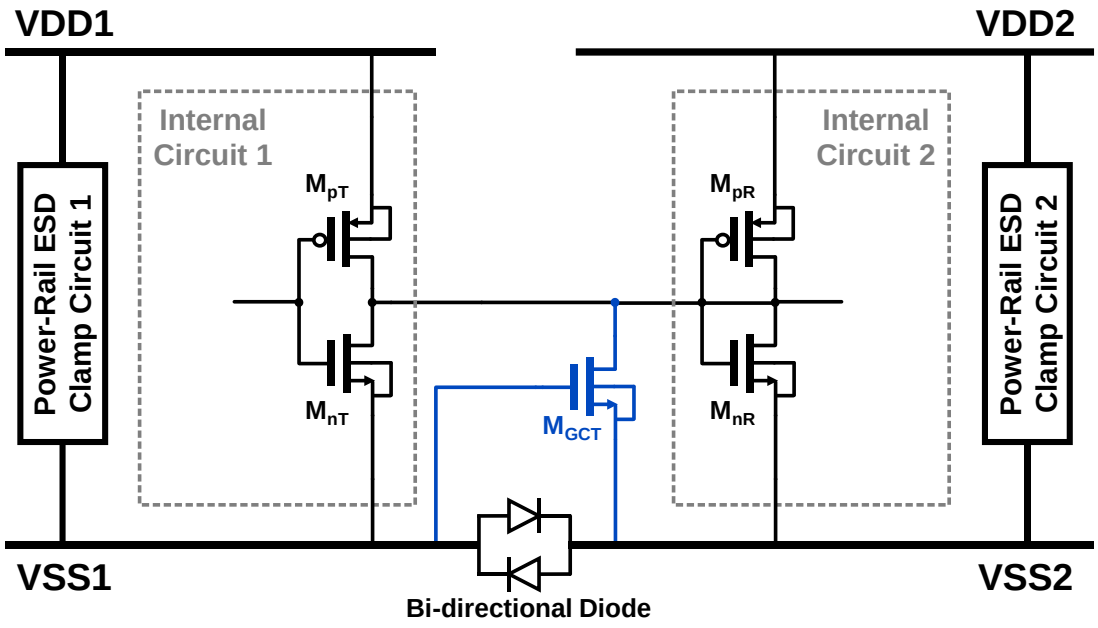


Fig. 1.18. The cross-domain circuit with the 2nd ESD protection circuit using the ground-current-trigger (GCT) technique [4].

1.5.4 Gate-Controlled (GC) Technique

A cross-domain circuit with the 2nd ESD protection circuit using the gate-controlled (GC) technique [6], as shown in Fig. 1.19, to further clamp overstress voltages across the gate-oxides of the receiver module. Under normal circuit operation, the gate-controlled NMOS (M_{GCN}) and gate-controlled PMOS (M_{GCP}) are turned off since both gates are connected to the VSS2 and the VDD2 respectively, to avoid leakage path and abnormal function. When a cross-domain ESD event appears between VDD1 and VSS2 (VDD1-to-VSS2), the M_{GCP} will be turned on during positive stress since V_{gs} is high enough and VDD2 is floating, while the parasitic body diode of the M_{GCP} will provide sufficient clamping strength under negative stress as well. When a cross-domain ESD event appears between VDD1 and VDD2 (VDD1-to-VDD2), the ESD current is initially discharged by the power-rail ESD clamp circuits and the bi-directional diodes. The M_{GCN} will be turned on under both positive and negative stress due to high enough V_{gs} of the M_{GCN}, and then provide sufficient clamping strength. This design can more comprehensively protect the interface circuit under various test combinations.

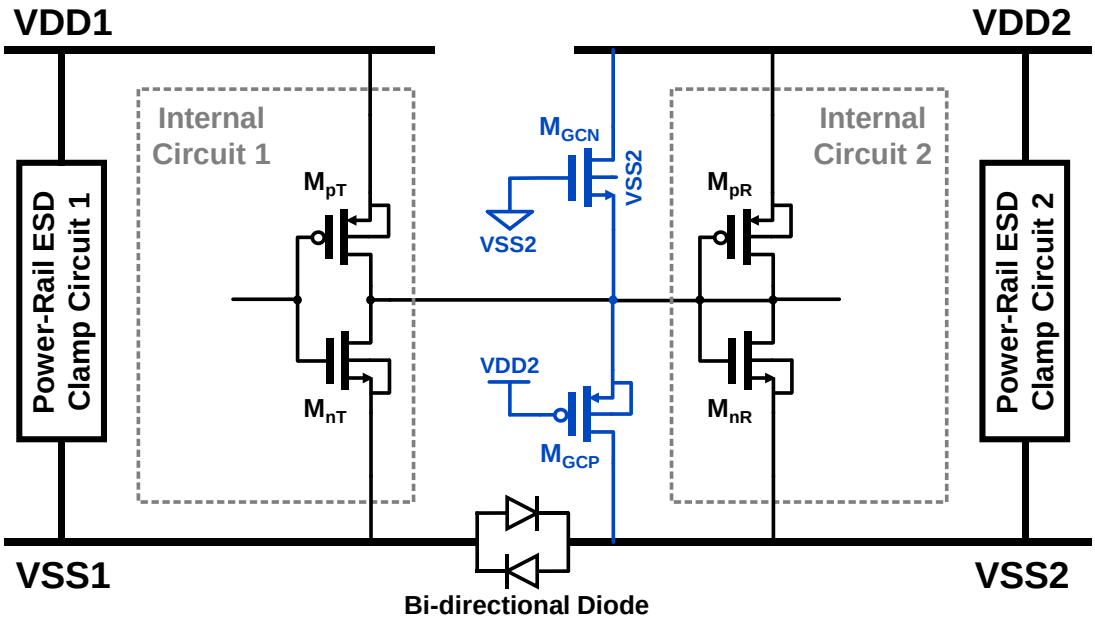


Fig. 1.19. The cross-domain circuit with the 2nd ESD protection circuit using the gate-controlled (GC) technique [6].

1.5.4 Summary

Unfortunately, the introduced prior arts of cross-domain ESD protection design have some shortcomings. The implementation of the R_{ESD}, M_{nESD}, M_{pESD}, D_n, D_p, M_{GCT}, M_{GCN}, and M_{GCP} will occupy additional areas and contribute propagation delay time to the signal transmission. Thus, the design impacts between area, speed, and ESD performance must be a trade-off depending on specifications.

Furthermore, high voltage to low voltage (HV-to-LV) interfaces and power-down mode applications are not available for traditional designs, such as the GGNMOS and GDPMOS design, or the dual diode design, because of the mis-triggering of the parasitic diodes or physical diodes under normal circuit operation.

Hence, in this thesis, a couple of new design solutions to overcome possible application issues mentioned above have been proposed and verified, while ensuring the improvement of ESD performance, in exchange for less area and speed budgets.

1.6 Thesis Organization

This thesis is divided into 4 chapters. Chapter 1 starts with motivation, and then introduces the basic concepts of ESD and typical ESD test models. The cross-domain ESD threats of typical HBM or CDM are discussed in detail. At the end of Chapter 1, some prior arts of cross-domain ESD protection design were introduced. The individual advantages and shortcomings of prior arts in terms of performance, area, integration, application, and power impact, will be discussed and compared with the new proposed designs as a summarized specification list in Chapter 2. Finally, the range of circuit specifications in terms of speed or area will be defined and set as a design target.

Chapter 2 focuses on the introduction and detailed description of new proposed designs for cross-domain interface circuits. The design and planning of cross-domain test circuits will also be introduced and assisted by simulation tools. A series of simulation results can be obtained by simulation methods such as the functional and CDM-like simulation, which will be done to predict the circuit behavior under normal operation or ESD events. The functional simulation is used to ensure that the chip has basic functions for verifying the failure behavior, and the CDM-like simulation is used to qualitatively predict cross-domain voltage during CDM ESD events.

A series of experimental results are organized in Chapter 3. First of all, the introduction of field-induced CDM ESD tester and relevant knowledge will be mentioned. Second, the floor plan and layout principles of the CDM test chip will be discussed in detail as well. Moreover, for defining the principles of failure criterion easily, the electrical and functional verifications before the ESD test are introduced. Later, followed by a series of experimental results, the ESD robustness of the different designs for interface circuits was investigated by traced the VF-TLP I-V characteristics, CDM, and HBM robustness. Apart from this, the comparison of the ESD performance between cross-domain test circuits with all designs is presented. Finally, the correlation

and difference between the results of various ESD tests are discussed. Particularly, the most concerning issue is the CDM. Thus, the failure analysis (FA) procedures were further implemented to verify the various newly proposed designs, and support to confirm the failure location and failure mechanism. Conclusions for the measurement results of this thesis are illustrated in Chapter 4. Discussions about future work are arranged in this chapter as well.

Chapter 2

Interface Circuit Designs for Cross-Domain CDM Protection

Before interface circuit design, the specifications (Table 2.1) of the cross-domain circuit must be properly defined. Since prior arts have some shortcomings, including low area efficiency and poor circuit integration, etc. Therefore, the experimental design tends to improve circuit integration, while improving cross-domain ESD performance, and minimize signal degradation by optimizing transistor size and driving capability.

Table 2.1

Specification Table of Proposed Cross-Domain Test Circuits

Specification of Proposed Designs	
Process Technology	TSMC 0.18μm 1.8V / 3.3V CMOS process
Power Supply [V]	VDD1 = VDD2 = +1.8, VSS1 = VSS2 = 0
Input / Output Signal Swing [V]	V_{IN} = V_{OUT} = 0 ~ +1.8 (Full Swing)
Duty-Cycle [%]	50 ± 5
Maximum Input Clock Frequency (f_{max}) [MHz] (Pure Interface Circuit)	100
DC leakage [nA]	I_{DD1} < 3, I_{DD2} < 300
Power Consumption (P_{VDD1}) [μW]	Static Power (P_S) < 0.0054 Dynamic Power (P_D) @ **f=1MHz** < 1.8
Power Consumption (P_{VDD2}) [μW]	Static Power (P_S) < 0.54 Dynamic Power (P_D) @ **f=1MHz** < 180
Pure Interface Circuit Area [$μm^2$]	88.4 (Horizontal Track = 20)
Internal Circuit Area [$μm^2$]	176.8 (Horizontal Track = 40)

2.1 Proposed Designs of Cross-Domain CDM Protection Circuit

According to the aforementioned prior art designs for cross-domain CDM protection, different kinds of local clamp circuits have been applied to protect interface circuits [1]–[16] and designed for special applications such as HV-to-LV level shifter, PLL interface, or power-down mode circuit. Usually, additional protection devices or circuits are inserted into the signal path to protect interface circuits. However, based on area and performance impacts, the structure of the cross-domain interface circuit (including transmitter and receiver module) should be modified, optimized, and designed for the same drive function, but simultaneously enhance the effective impedance to achieve higher cross-domain CDM ESD robustness. The test chip is completely planned and designed for physical verification and comparison.

2.1.1 Cross-Domain Circuit Architecture and Test-Keys Overview

A. Cross-Domain Circuit Architecture

Based on the consideration of performance and power consumption, low voltage (LV) devices are widely used in core circuits, due to the thinner gate oxide and larger oxide capacitance (C_{ox}), but easily breakdown by any ESD energy, especially CDM ESD. Therefore, the I/O and core devices of the two domains choose 1.8V-LV devices as a worst-case to verify the cross-domain ESD tolerance, making the results referential and closing to practical applications. Also, the experimental results without the impact of thickness difference can effectively compare each proposed design. Thus, the VDD1 and VDD2 will be supplied to 1.8V under normal power-on conditions.

To build a multi-domain IC, a cross-domain circuit (see Fig. 2.1) is implemented under the TSMC 0.18-μm 1.8-V CMOS process. This circuit includes power-rail ESD clamp circuits, I/O ESD protection circuits for each domain, bi-directional diodes between the separated VSS, and two inverters as the interface circuit. Both the

transmitter and receiver modules use the inverter cell, provided by the 0.18-μm standard cell library, with a specific driving capability. Choosing a larger size inverter on the Tx side can promote unexpected discharge paths across the interface circuit and the smallest size inverter on the Rx side as a worst-case, and the gate potential rises more rapidly since its minimal parasitic capacitance.

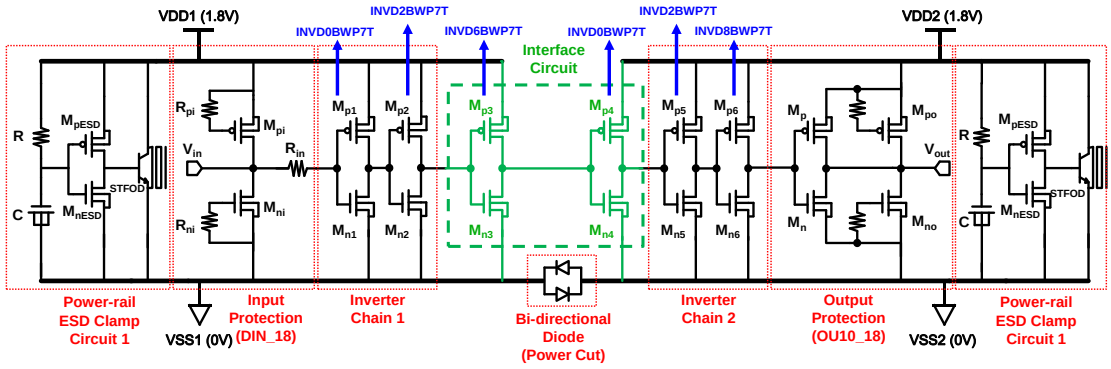


Fig. 2.1. A cross-domain circuit is implemented under the TSMC 0.18-μm 1.8-V CMOS process to build a multi-domain IC.

Taken from the DIN_18, OU10_18, Power Cut, and Power-rail ESD Clamp Circuit of the I/O Cell Library to establish the whole circuit ESD protection system. The parameters of the ESD protection circuits are shown in Table 2.2. The DIN_18 is used for pad-to-VDD and pad-to-VSS ESD protection at the input pad, it consists of a pair of the gate-grounded NMOS (GGNMOS) and the gate-VDD PMOS (GDPMOS). The OU10_18 is used for pad-to-VDD and pad-to-VSS ESD protection at the output pad, it has the same device dimension and multiple finger numbers of each NMOS and PMOS as the DIN_18. The driving strength of the output buffer can be determined according to the external load, signal operation frequency, and distortion tolerance by connecting different gate finger numbers of NMOS and PMOS to get the appropriate driving current and achieve the signal specifications, the other fingers are connected to implement the GGNMOS and the GDPMOS.

The Power Cut uses a bi-directional anti-parallel diode to connect the separate VDD or VSS rail, blocking noise and dissipating ESD current as main functions. Under normal operation, the ground bounce effect causes serious noise disturbance in the VDD/VSS rail, and the reversed diode with cut-in voltage isolates coupling noise and prevents affecting the operation of the sensitive circuits. By modulating the number of diode strings, the noise threshold and voltage differences between multi-domain could be configurable. Under cross-domain ESD stress, the ESD dissipation path could be established by the forward diodes pair to achieve the whole-chip ESD protection. In this experiment, the ESD dissipation path between the VSS rails was established, the VDD rail was separated to generate internal damages, and a single back-to-back (B2B) diode pair was selected as the general case of the digital circuit. The power-rail ESD clamp circuit consists of an RC-based ESD transient detection circuit and a substrate-triggered field-oxide device (STFOD) with a perimeter equivalent to 188 μm as the main ESD device [20], is individually installed in each power domain.

Taken from inverter chains and interface circuits of standard cell library are set as digital circuit blocks between separate power domains. The parameters of the transistors used in the internal circuit are listed in Table 2.3. To ensure the driving ability when doing the measurement, insert inverter chains in which the sizes of the transistor are gradually increased with stages between I/O ESD protection and interface circuits. A pair of inverters are set as the transmitter and the receiver to represent the interface circuit that transfers signals from the circuit in the VDD1/VSS1 domain to the VDD2/VSS2 domain.

Table 2.2

The Parameters of ESD Protection Circuits

ESD Protection Circuit	Device (Unit)	Parameter
Input Protection (DIN_18)	Resistor (kΩ)	Rin = 0.2 R_{pi} = R_{ni} = 1
	MOS W/L (μm/μm)	M_{pi} = 360 / 0.25 M_{ni} = 360 / 0.5
Output Protection (OU10_18)	Resistor (Ω)	M_p = 150 / 0.25 M_n = 75 / 0.5 M_{po} = 210 / 0.25 M_{po} = 285 / 0.5
	MOS W/L (μm/μm)	
Bi-directional Diode (Power Cut)	Cell W*L (μm*μm)	7.74*19
	Total Perimeter (μm)	53.48
RC-Based Power-rail ESD Clamp Circuit (ESDH)	Resistor (kΩ)	R_{ESD} ~ 95
	Capacitor (pF)	C_{ESD} ~ 2
	MOS W/L (μm/μm)	M_{pESD} = 60 / 0.25 M_{nESD} = 24 / 0.25

Table 2.3

The Parameters of Transistors Used in The Internal Circuit

Internal Circuit	Standard Cell	MOS W/L (μm/μm)
Inverter Chain-1	INVD0BWP7T	M_{p1} = 0.685/0.18
		M_{n1} = 0.5/0.18
	INVD2BWP7T	M_{p2} = 2.74/0.18
		M_{n2} = 2/0.18
Inverter Chain-2	INVD6BWP7T	M_{p3} = 8.22/0.18
		M_{n3} = 6/0.18
	INVD0BWP7T	M_{p4} = 0.685/0.18
		M_{n4} = 0.5/0.18
Interface Circuit	INVD2BWP7T	M_{p5} = 2.74/0.18
		M_{n5} = 2/0.18
	INVD8BWP7T	M_{p6} = 10.96/0.18
		M_{n6} = 8/0.18

B. Test-Keys Overview

Each cross-domain interface circuit (including receiver module (RX) and transmitter module (TX)) of the test chip is partially taken from the TSMC 0.18-μm 1.8-V Standard Cell Library, and refer to the layout style of the combined logic cell to design and improve. The purpose is to integrate the new designs in a cell library for the logic synthesis tool or auto-placement & route (APR) tool. Moreover, the EDA simulation algorithms, which provide necessary assistance in the circuit-level design, can analyze the victim location, especially the cross-domain region, to greatly reduce the time-to-market and cost of failure analysis.

First of all, this experiment will adopt the new proposed designs as test-keys that embed in the RX or TX to build the test circuits, which are connected to the interface circuit with the same pre-stage and post-stage and are configured with the same whole-circuit ESD protection circuit. The key factors of test-keys include circuit architecture and interconnection. All test-keys have the same inverting function and classify their characteristics for a brief description (see Table 2.4). To eliminate the influence of size variation, the transistor size is fixed in each test circuit except Rx-LD design. For timing considerations, cell optimization and performance improvement are straightforward solutions.

Table 2.4

The List of All Test-Keys with Prefix Codes and Brief Descriptions

Code	Modified	Description
Baseline	-	Inverter (reference design)
Rx-LD	Rx	Inverter (large dimension transistors embedded in Rx-module)
Rx-CC	Rx	Stack-MOS inverter with cross-coupled of the gate connection
Rx-STC	Rx	Stack-MOS inverter with standard tie high/low circuits
Rx-Latch	Rx	Stack-MOS inverter with a latch structure
Tx-CC	Tx	Stack-MOS inverter with cross-coupled of the gate connection
Tx-STC	Tx	Stack-MOS inverter with standard tie high/low circuits
Tx-Latch	Tx	Stack-MOS inverter with a latch structure

2.1.2 Baseline (Reference Design) and Dimension Variation (Study on CDM)

A cross-domain circuit without any modification, set as the baseline (reference design), as shown in Fig. 2.2, both transmitter and receiver use an inverter for signal transmission. The inverter is taken from the INVD cell of the TSMC 0.18-μm 1.8-V Standard Cell Library. A series of simulation results will be detail described in Chapter 3.2 and Chapter 3.3 as a comparison standard. The parameters of the transistors in the internal circuit are listed in Table 2.5.

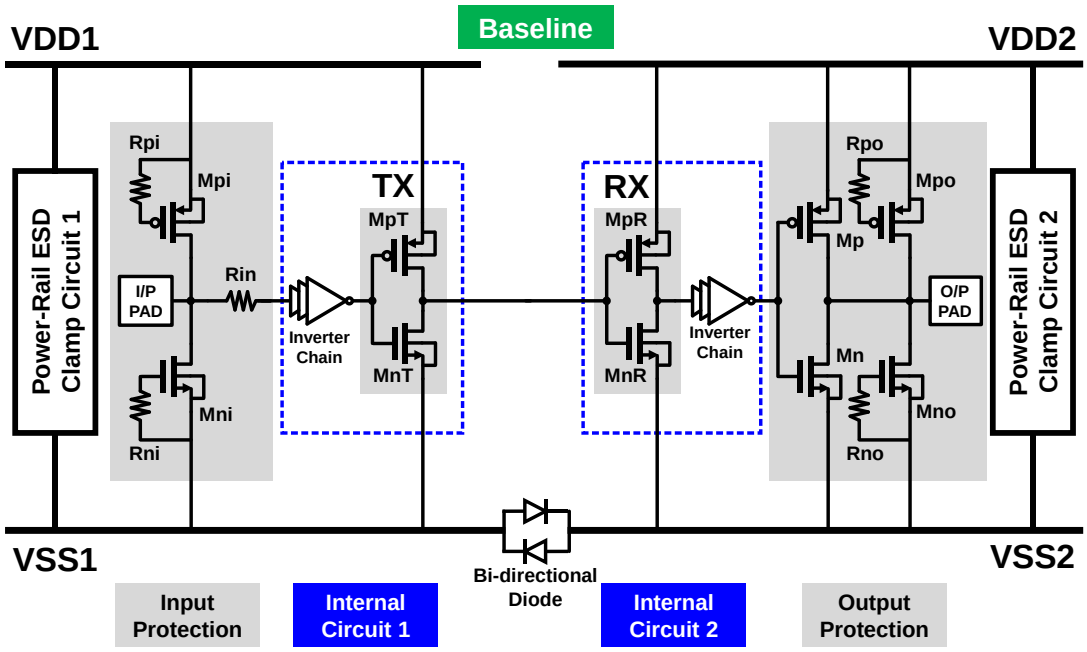


Fig. 2.2. A cross-domain circuit without any modification, set as the Baseline design.

A cross-domain circuit with dimension variation, set as Rx-LD design (see Fig. 2.3), same TX as Baseline but different RX. To investigate whether the transistor size and number of the finger have impacts on cross-domain ESD robustness or not, the largest INVD cell was taken as the RX inverter. In general, the larger size transistor with larger gate and junction areas can dissipate more ESD heats (such as HBM or MM). However, for CDM ESD events, the CDM charges prefer to transfer from the large oxide capacitance (C_{ox}), and cause serious gate-oxide damage. The parameters of the transistors in the internal circuit are listed in Table 2.5.

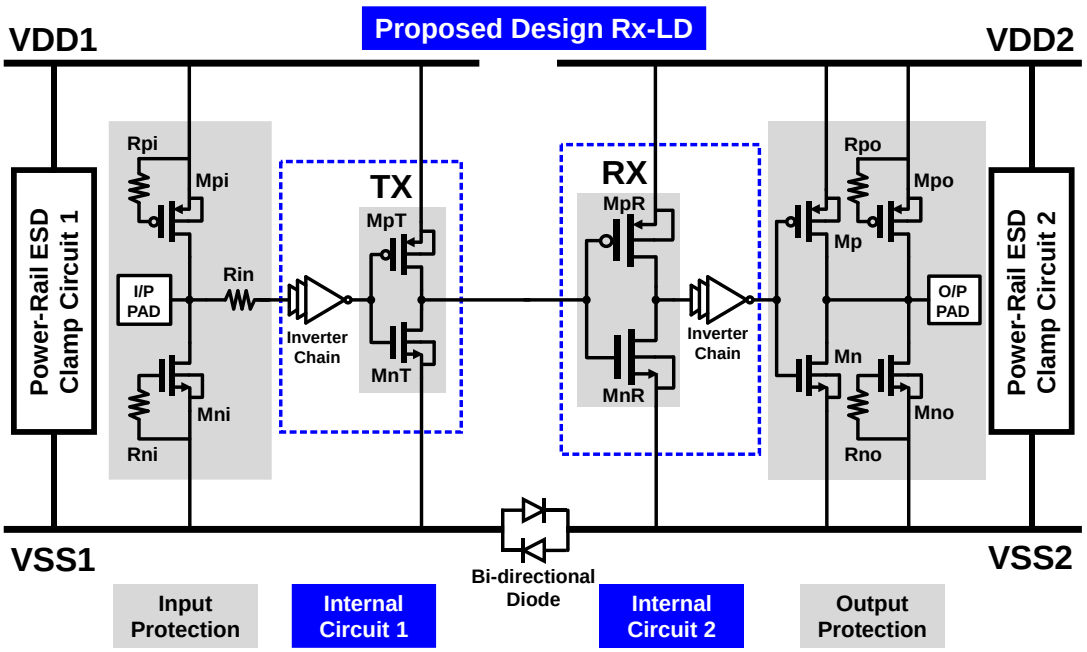


Fig. 2.3. A cross-domain circuit with dimension variation, set as Rx-LD design.

Table 2.5

The Design Parameters of Selected Devices Used in The Baseline and Rx-LD Designs

Subcircuit	Device Parameter	Baseline	Rx-LD
Transmitter (TX)	MOS W/L (μm/μm)	M_{nT}=6/0.18 M_{pT}=8.22/0.18	M_{nT}=6/0.18 M_{pT}=8.22/0.18
Receiver (RX)	MOS W/L (μm/μm)	M_{nR}=0.5/0.18 M_{pR}=0.685/0.18	M_{nR}=12/0.18 M_{pR}=16.44/0.18

2.1.3 Stacking-MOS Design and Modification of Receiver Module

Based on area cost and circuit performance considerations, the structure of the cross-domain interface circuit should be modified and optimized, and achieve higher cross-domain CDM ESD robustness. The new proposed Rx-CC (Cross-Coupled), Rx-STC (Standard Tie-Circuit), and Rx-Latch (Latch structure) design circuits with Rx modification as shown in Fig. 2.4 ~ Fig. 2.7. By modifying the interconnection of the receiver module with stacking MOS structure to have the same function as the reference

design under normal operation, thus enhancing the equivalent impedance of the interface circuit under ESD event and suppressing the generation of unexpected discharge paths. Fig. 2.4 illustrates a schematic diagram from the previous work [7], a receiver module consists of stacking header PMOS (M_{pR2}) and footer NMOS (M_{nR2}) directly cross-couple connected to VSS2 and VDD2, respectively. Both are coupled with an inverter constituted of a PMOS transistor M_{pR1} and an NMOS transistor M_{nR1}. The gates of M_{pR1} and M_{nR1} are tied together which are connected to the signal line, while the drains of the M_{pR1} and the M_{nR1} are tied together for providing an output signal to the next stage circuit, the inverter chain.

The gate to the source overlapped junction must be protected first because of the lowest breakdown voltage [21]. When a cross-domain ESD event occurs as mentioned above, the large potential difference will cross between the gate of M_{nR1} and the source of M_{nR2}. The internal node V_n forms a floating node, and the total parasitic capacitance on the V_n forms a voltage divider. By modulating the sizes of M_{nR1} and M_{nR2}, the voltage coupled to the V_n node can be dynamically adjusted, which could alleviate the overvoltage of M_{nR1}. The PMOS side also adopts the same symmetrical structure as NMOS. Under the corresponding cross-domain ESD stress condition, a voltage divider is formed at the floating node V_p to relieve the transient overvoltage of M_{pR1}.

In the digital circuit, a combinational logic in the form of stacking transistors needs sizing to achieve the same driving capability. However, during high-speed signal transmission, a transient potential difference between the source and body of M_{nR1} and M_{pR1} causes the body effect and degrades the switching speed. Therefore, the timing specification and the area cost are required to tradeoff. As for the main reasons for CDM damage mentioned earlier, the direct connection of the gate to VDD/VSS will have poor CDM robustness. Thus, this test-key is helpful to analyze the failure mechanism and discover the root cause.

The effective breakdown voltage of M_{pR1} and M_{nR1} can be enhanced by increasing the number of header PMOS transistors and footer NMOS transistors [8], respectively. Moreover, the size of the parasitic capacitance will determine the ratio of the voltage divider, and the value of the equivalent breakdown voltage could be well designed by spice simulation and layout extraction.

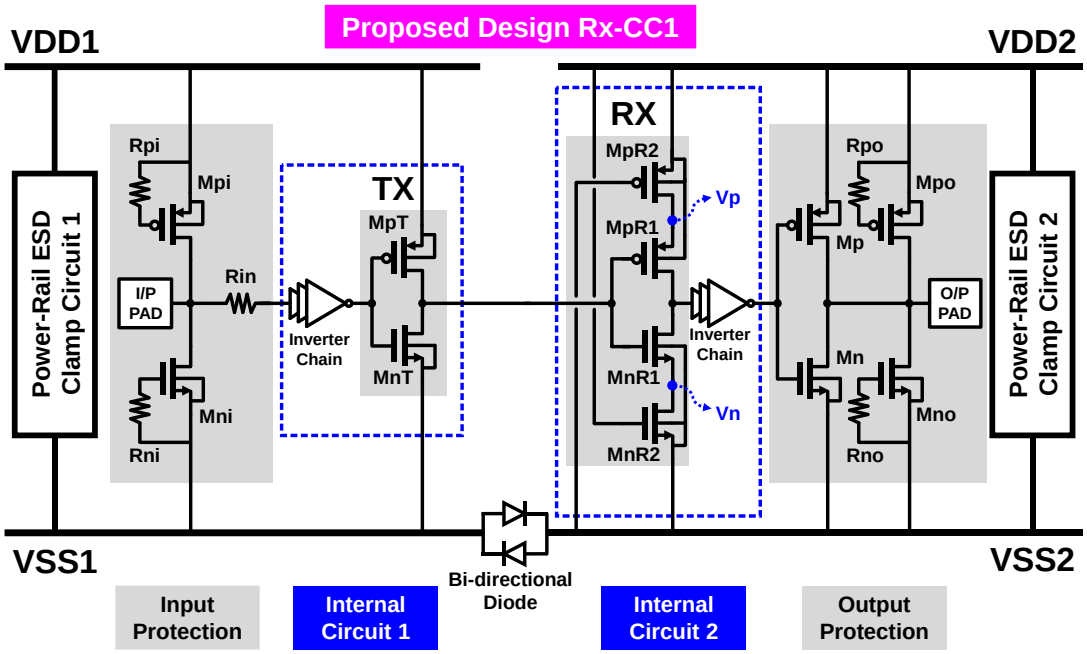


Fig. 2.4. The proposed design Rx-CC1, with a receiver module, consists of stacking header PMOS (M_{pR2}) and footer NMOS (M_{nR2}) directly cross-couple connected to VSS2 and VDD2, respectively.

Turning now to Fig. 2.5, which illustrates a similar schematic diagram of a receiver module consists of stacking footer PMOS (M_{pR1}) and header NMOS (M_{nR1}) directly cross-couple connected to VSS2 and VDD2, respectively. Both are coupled with an inverter constituted of a PMOS transistor M_{pR2} and an NMOS transistor M_{nR2}. The gates of M_{pR2} and M_{nR2} are tied together which are connected to the signal line, while the drains of the M_{pR1} and the M_{nR1} are tied together for providing an output signal to the next stage circuit, the inverter chain.

The Rx-CC2 is similar to the Rx-CC1 design, except for the interconnections of the stacking-MOS structure. This design improves the logical driving strength and signals transmission speed for M_{nR2} and M_{pR2} transistors, which are mainly used for signal transmission, and eliminate the body effect under normal operation. But, it suffers from charge sharing due to internal junction capacitance at floating node V_n/V_p. Hence, the overall performance will not be significantly improved. During cross-domain ESD stress, this configuration will form a voltage divider at node V_p/V_n to increase the equivalent breakdown voltage of M_{pR1} and M_{nR1}. However, M_{nR2} and M_{pR2} still suffer gate-oxide overstress issues, result in the ESD performance could not be guaranteed and evaluated.

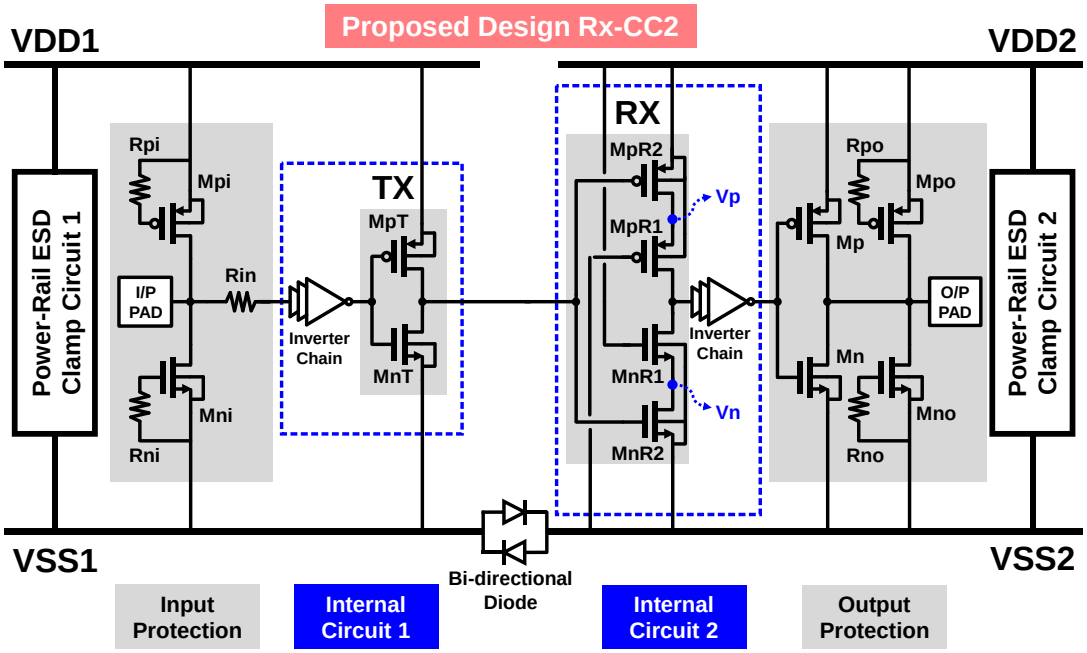


Fig. 2.5. The proposed design Rx-CC2, with a receiver module, consists of stacking footer PMOS (M_{pR1}) and header NMOS (M_{nR1}) directly cross-couple connected to VSS2 and VDD2, respectively.

The most common failure mechanism in CDM ESD events is the gate-oxide breakdown. Since the metal bus is prone to accumulate CDM charges, tie circuits have become one of the solutions [22] but occupied more area. Fig. Rx-STC. illustrates a

receiver module consists of stacking header PMOS (M_{pT2}) and footer NMOS (M_{nT2}) with standard tie-low/high circuits.

The unused pin in the digital circuit should be locked in a stable state instead of floating, to keep the logic output out of an intermediate state. The standard tie high/low circuits taken from the standard cell library, are used to avoid direct gate connection to the VDD/VSS bus, thereby protecting the cell from gate-oxide damage. In this case, the M_{nH}/M_{pL} transistor acts as a diode-connected start-up circuit, and M_{pH}/M_{nL} pull logic high/low as output to bias the M_{nR2}/M_{pR2} in fully-on-state, respectively. However, the M_{nR1}/M_{pR1} still has a body effect that degrades the operating performance. Concerning the cross-domain ESD issue, this configuration has the opportunity to comprehensively improve the ESD level. The tie circuits close the gate terminals of M_{nR2} and M_{pR2}, creating high impedances to form voltage dividers on the floating nodes V_p and V_n.

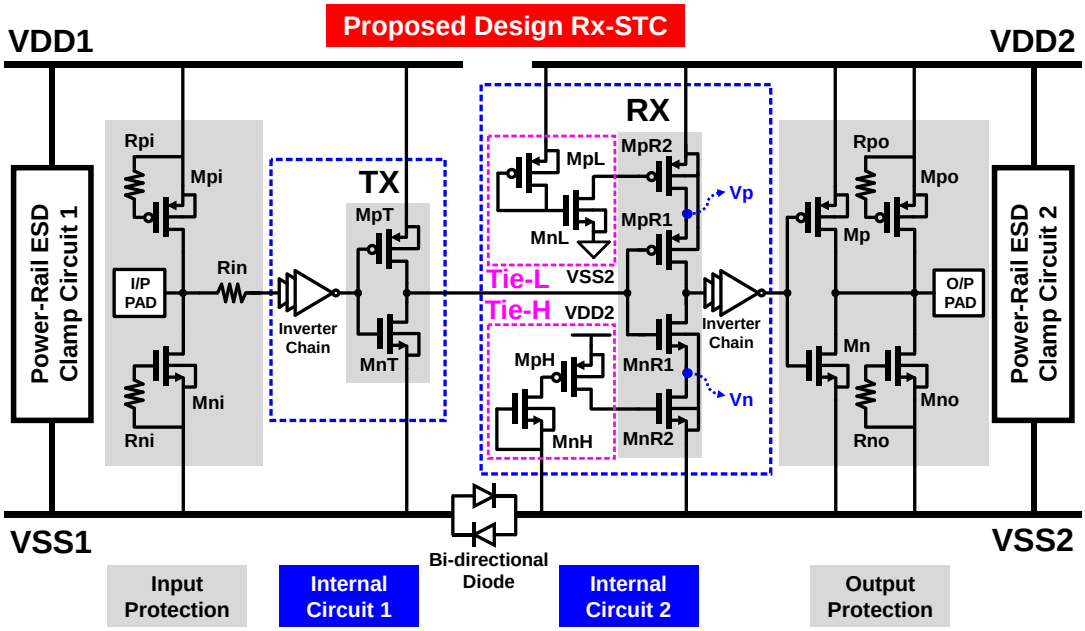


Fig. 2.6. The proposed design Rx-STC, with a receiver module, consists of stacking header PMOS (M_{pT2}), footer NMOS (M_{nT2}), and the standard tie-low/high circuits.

Fig. 2.7. illustrates a receiver module consists of stacking structures connected to inter-stage node V_n and V_p, which form a symmetrical latch structure. The latch structure could eliminate the requirement for additional tie circuits.

However, the latch structure needs to be carefully designed and used. During the normal power-on transition, M_{pR2} is first turned on to pull up V_p to logic high (H or 1), then M_{nR2} is turned on to pull V_n to logic low (L or 0), and the zero-current state is tripped to form closed-loop positive feedback. This preset process requires sufficient regeneration time to take MnR2 and MpR2 in a fully-on state. Note that, high-speed signals are rapidly switching during interface circuit communication, and noise interference, which may couple to V_n, V_p nodes, may occur, and then cause M_{nR2} and M_{pR2} to escape from the original logic state. If a high level of logic output is lower than VDD/2, the malfunction will happen in the post-stages, and the frequency at this time is defined as the maximum frequency (f_{max}), which could be evaluated as a performance limit in terms of speed. In this experiment, the size of transistors in the latch structure has been well designed to ensure stable output for high-speed signals.

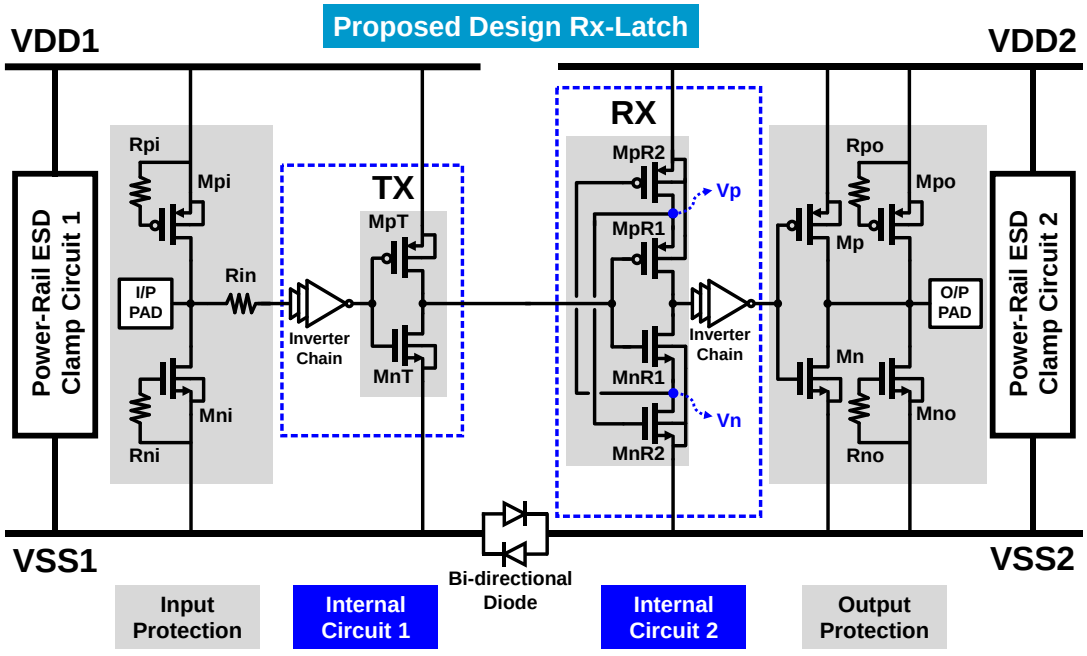


Fig. 2.7. The proposed design Rx-Latch, with a receiver module, consists of stacking structures connected to inter-stage node V_n and V_p, which form a symmetrical latch structure.

In summary, for the Rx-CC1, Rx-STC, and Rx-Latch designs, a voltage divider with the floating nodes V_p and V_n was formed to couple the instantaneous rising voltage during cross-domain ESD stress, thus increase the equivalent breakdown voltage of the receiver module. Furthermore, the gate connection of the stacking MOS via tie circuits prevents the CDM charges on the metal wire from breaking down the gate-oxide of the interface circuit and ensures a better CDM ESD robustness under different conditions. For the designs of Rx modification, the parameters of the transistors in the internal circuit are listed in Table 2.6.

Table 2.6

The Design Parameters of Selected Devices Used in The Baseline and Rx Modifications.

Subcircuit	**Device Parameter**	**Baseline**	**Rx-CC1, Rx-CC2, Rx-STC, and Rx-Latch**
Transmitter (TX)	**MOS W/L (μm/μm)**	**M_{nT}=6/0.18** **M_{pT}=8.22/0.18**	**M_{nT}=6/0.18** **M_{pT}=8.22/0.18**
Receiver (RX)	**MOS W/L (μm/μm)**	**M_{nR}=0.5/0.18** **M_{pR}=0.685/0.18**	**M_{nH}=M_{nL}=1/0.18** **M_{pH}=M_{pL}=1.37/0.18** **M_{nR1}=M_{nR2}=0.5/0.18** **M_{pR1}=M_{pR2}=0.685/0.18**

2.1.4 Stacking-MOS Design and Modification of Transmitter Module

Likewise, the new proposed Tx-CC (Cross-Coupled), Tx-STC (Standard Tie-Circuit), and Tx-Latch (Latch structure) design circuits as shown in Fig. 2.8. ~ Fig. 2.11. By modifying the interconnection of the transmitter module with stacking MOS structure to have the same function as the reference design under normal operation, thus enhancing the equivalent impedance of the interface circuit under ESD event and suppressing the generation of unexpected discharge paths.

Fig. 2.8. illustrates a schematic diagram similar to Rx-CC1, a transmitter module consists of stacking header PMOS M_{pT2} and footer NMOS M_{nT2} directly cross-couple connected to VSS2 and VDD2, respectively. Fig. 2.9. illustrates a schematic diagram similar to Rx-CC2, a transmitter module consists of stacking footer PMOS M_{pT1} and header NMOS M_{nT1} directly connected to VSS2 and VDD2, respectively. Fig. 2.10. illustrates a schematic diagram similar to Rx-STC, a transmitter module consists of stacking header PMOS M_{pT2} and footer NMOS M_{nT2} with standard tie-low/high circuits. Fig. 2.11. illustrates a schematic diagram similar to Rx-Latch, a transmitter module consists of stacking MOS structures connected to inter-stage node V_n and V_p, which form a symmetrical latch structure. The latch structure could eliminate the requirement for additional tie circuits.

In conclusion, for the Tx-CC1, Tx-CC2, Tx-STC, and Tx-Latch designs, a voltage divider with the floating nodes V_p and V_n was formed to couple the instantaneous rising voltage during cross-domain ESD stress, thus increase the equivalent breakdown voltage of the transmitter module. Furthermore, the gate connection of the stacking MOS via tie circuits prevents the CDM charges on the metal wire from breaking down the gate-oxide of the interface circuit and ensures a better CDM ESD robustness under different conditions. For the designs of Tx modification, the parameters of the transistors in the internal circuit are listed in Table 2.7.

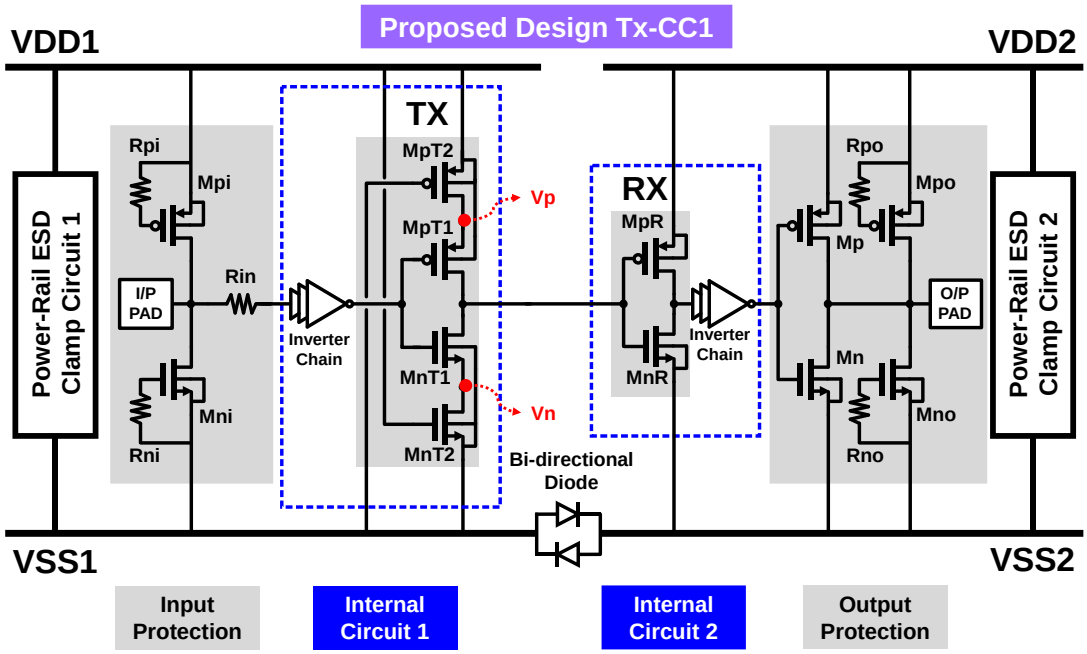


Fig. 2.8. The proposed design Tx-CC1, with a transmitter module, consists of stacking header PMOS (M_{pR2}) and footer NMOS (M_{nR2}) directly cross-couple connected to VSS2 and VDD2, respectively.

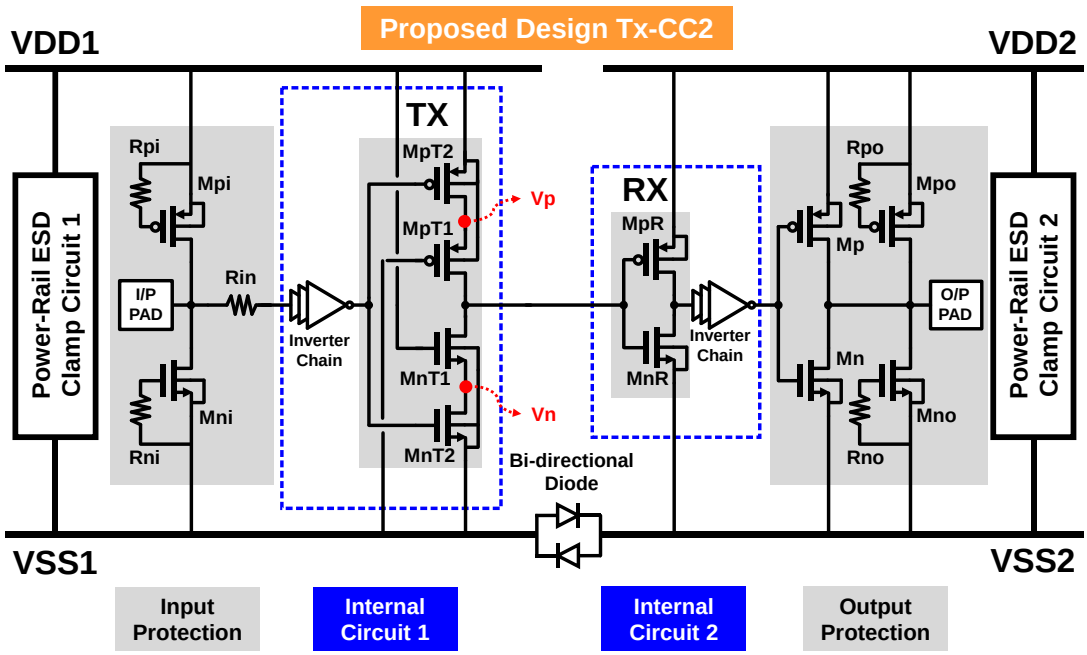


Fig. 2.9. The proposed design Tx-CC2, with a transmitter module, consists of stacking footer PMOS (M_{pR1}) and header NMOS (M_{nR1}) directly cross-couple connected to VSS2 and VDD2, respectively.

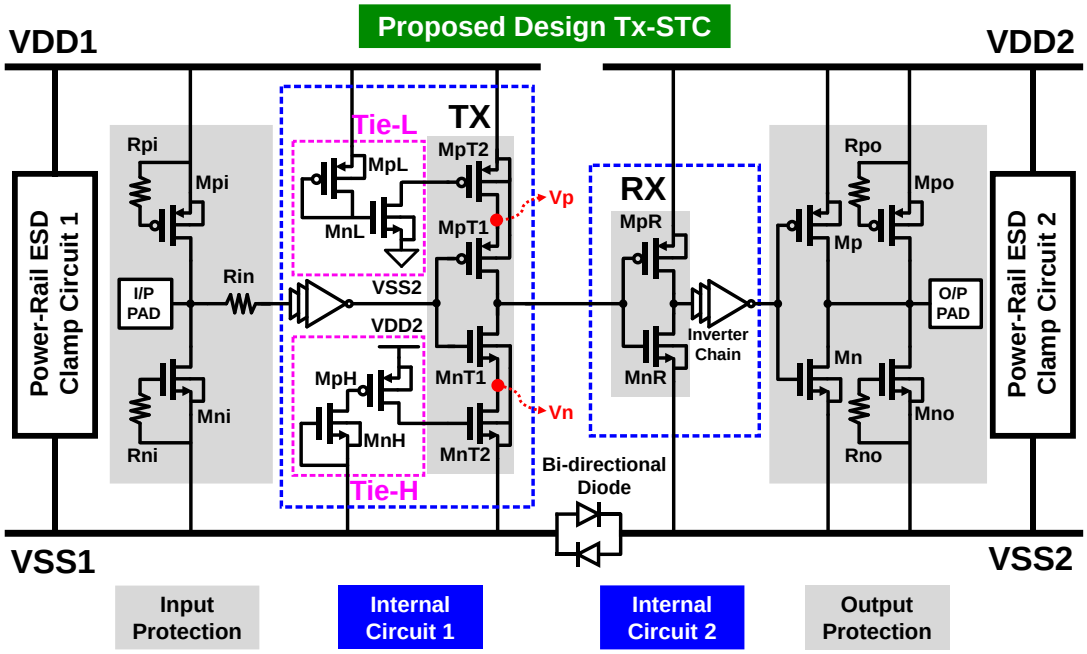


Fig. 2.10. The proposed design Tx-STC, with a transmitter module, consists of stacking header PMOS (M_{pT2}), footer NMOS (M_{nT2}), and the standard tie-low/high circuits.

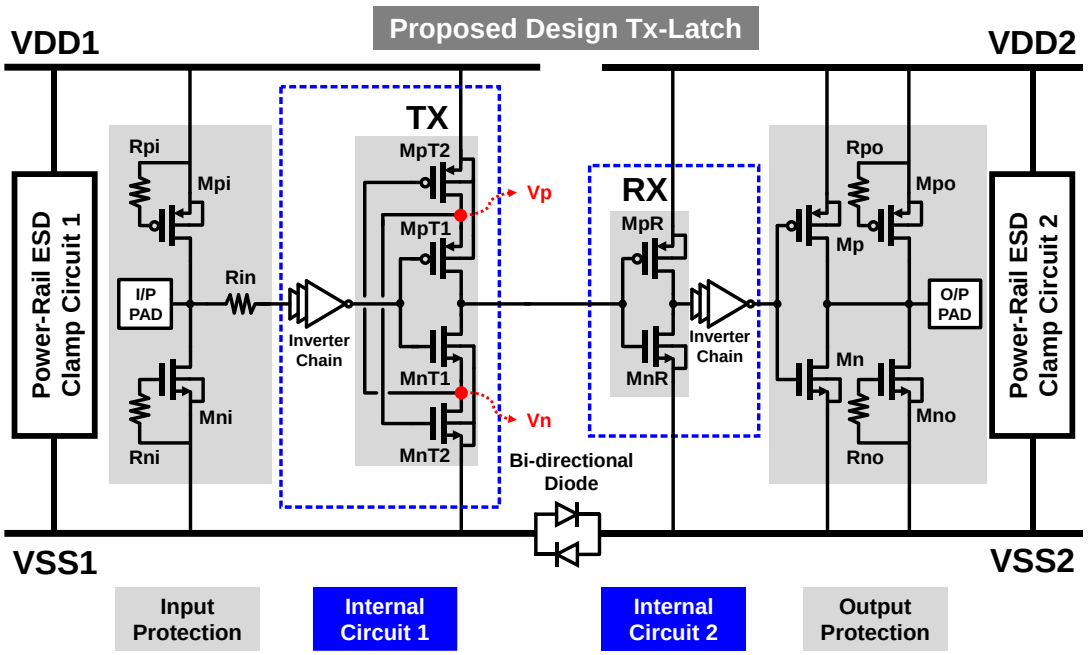


Fig. 2.11. The proposed design Tx-Latch, with a transmitter module, consists of stacking structures connected to inter-stage node V_n and V_p, which form a symmetrical latch structure.

Table 2.7

The Design Parameters of Selected Devices Used In The Baseline and Tx Modifications.

Subcircuit	Device Parameter	Baseline	Tx-CC1, Tx-CC2, Tx- STC, and Tx-Latch
Transmitter (TX)	**MOS W/L (µm/µm)**	**M_{nT}=6/0.18** **M_{pT}=8.22/0.18**	**M_{nH}=M_{nL}=1/0.18** **M_{pH}=M_{pL}=1.37/0.18** **M_{nT1}= M_{nT1}=6/0.18** **M_{pT1}=M_{pT2}=8.22/0.18**
Receiver (RX)	**MOS W/L (µm/µm)**	**M_{nR}=0.5/0.18** **M_{pR}=0.685/0.18**	**M_{nR} =0.5/0.18** **M_{pR} =0.685/0.18**

2.2 Simulation Results

For ensuring each test circuit can be implemented correctly and maintain the same function under normal power-on, the functional simulation will be adopted. Besides, in the circuit-level design, the qualitative analysis of the circuit behavior is necessary. There are various simulation methods for any ESD events. In this thesis, a CDM-like simulation method, for initially observing the cross-domain voltage of the test circuit, helps to check the transient overvoltage across gate-oxides and compare each design. Note that, the method introduced here is a pre-layout simulation, which does not include parasitic resistances and capacitances. If accuracy is required, the extraction RC parameter can be added to the simulation.

Unfortunately, in the ESD dissipation path, the STFOD and bi-directional diode were not be provided spice models and relevant simulation parameters by process design kit (PDK). Therefore, using the lateral NPN BJT and P^+/N-well junction diode instead of ESD devices to perform all simulations, results in inaccurate results, but provide quite enough information and trends in the circuit-level design.

2.2.1 Functional Simulation Under Normal Power-ON Condition

Under the normal power-on condition, both VDD1 and VDD2 are powered to 1.8V, with separated VSS1 and VSS2 which are biased to 0V. The simulation set-up is shown in Fig. 2.12. The Interface circuit is divided into VDD1/VSS1 and VDD2/VSS2 domains and each domain has an independent VDD/VSS pin, so there are 6 ports in total, namely VDD1, VDD2, VSS1, VSS2, V_{IN}, and V_{OUT}. During the functional simulation, VDD1 and VDD2 will be forced the same ramp voltage V_{DC} (rise time tr=1ms for simulating the power-on situation), V_{IN} will be applied a periodic square wave of 1MHz as a clock signal with the amplitude of full-swing 1.8V. Since the internal cross-domain interface circuit is a non-inverting buffer formed by two inverter stages, the additional inverter-

chains, as a tapper buffer, will be inserted in pre-stage and post-stage to keep the signal integrity. Overall, with the odd number of inverters, the V_{OUT} should out of phase to V_{IN}. Also, the function simulation has performed PVT variation analysis, considering T = 25℃ and 125℃ as temperature variations, and the tt, ff, and ss corner as process variations.

Due to the absence of the HSPICE-model, the STFOD is replaced with a vertical NPN BJT. The NPN BJT with device dimensions W*L=5μ*5μ was adopted 28 unit cells in parallel, so the total perimeter and emitter junction area are approximately the same as STFOD. Similarly, because the ESD diode is essentially a P+/N-well junction diode, the ESD bi-directional diodes are replaced with an anti-parallel P+/Nwell diode, with device dimension W/L=18μ/6μ. The simulated results of the proposed design test circuits are shown in Fig. 2.13.

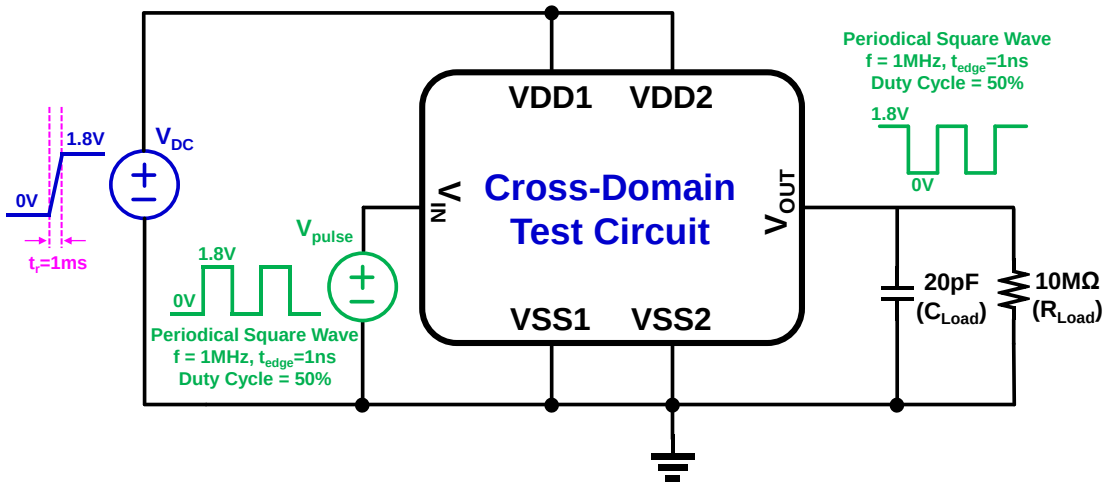
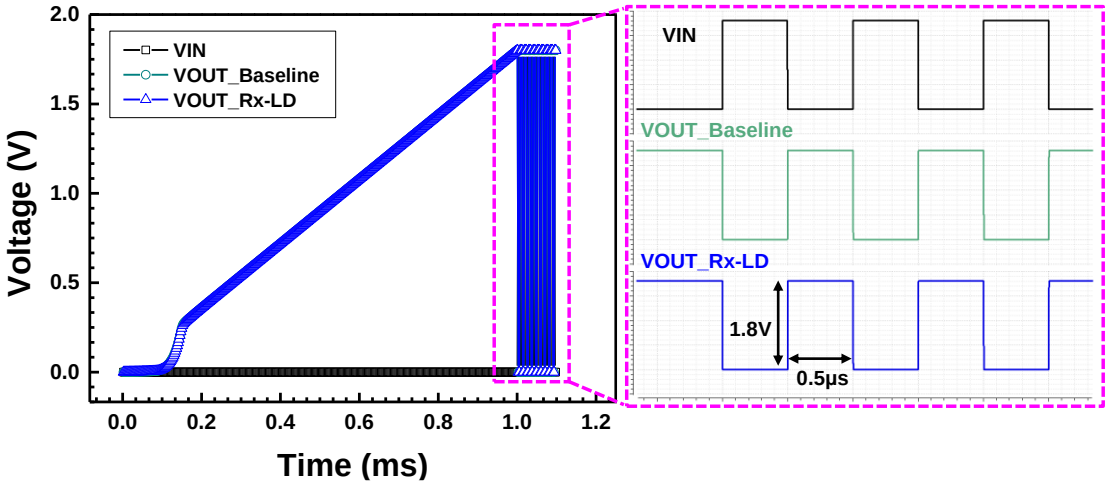
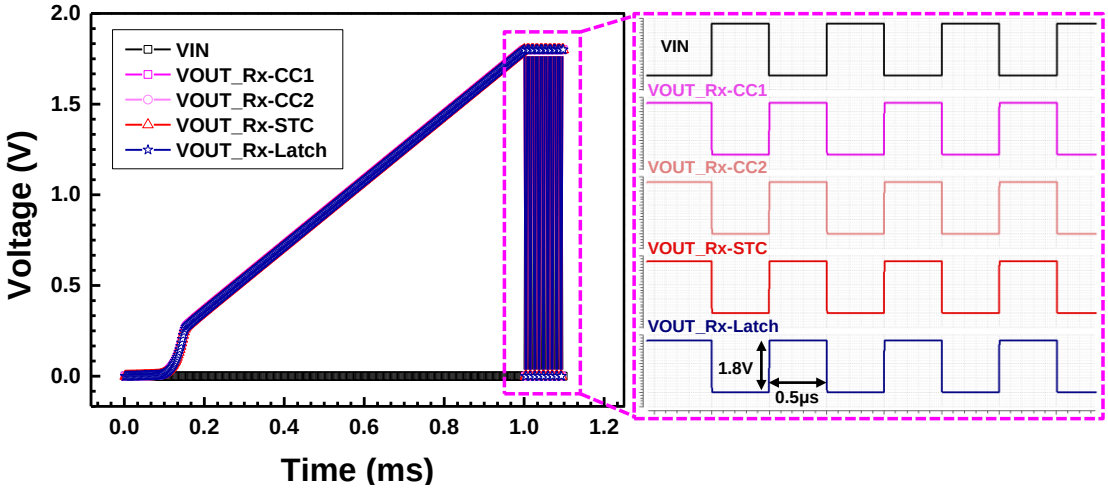


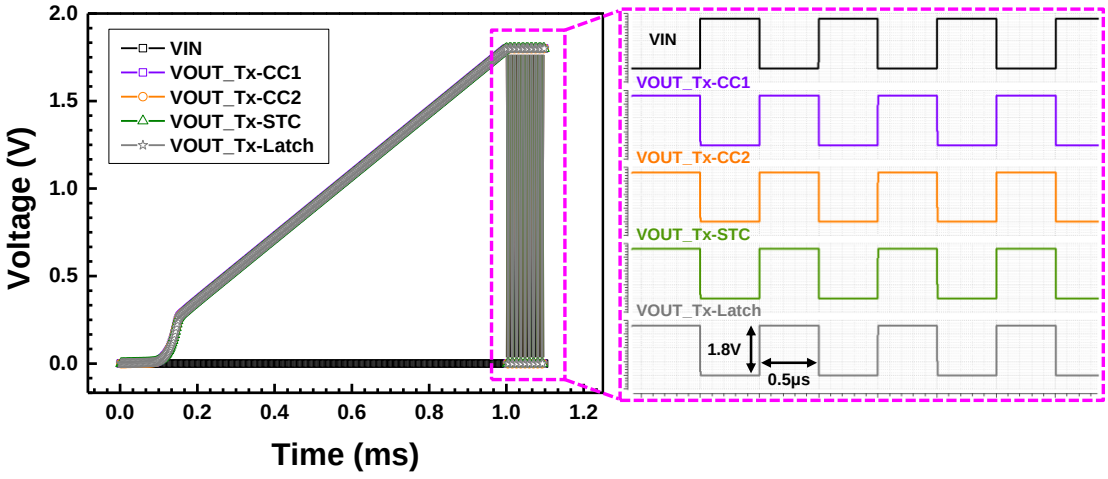
Fig. 2.12. Functional simulation set-up under normal power-on condition.



(a)



(b)



(c)

Fig. 2.13. Functional simulation results of the proposed design cross-domain test circuits under normal power-on condition.

As a result, similar functions were verified for each test circuit with different designs. Furthermore, the stacking-MOS structure with different interconnections contributes unequal delay time to the interface circuit, but the internal delay is not easy to be directly observed from the output signal. Hence, as shown in Fig. 2.14, another functional simulation is set for probing the rise time, fall time, and internal propagation delay. The purpose is to compare the performance difference of each test-key, which can be optimized in the circuit-level design, and explore the trade-offs in practical application. The comparisons of the test-keys are listed in Table 2.8.

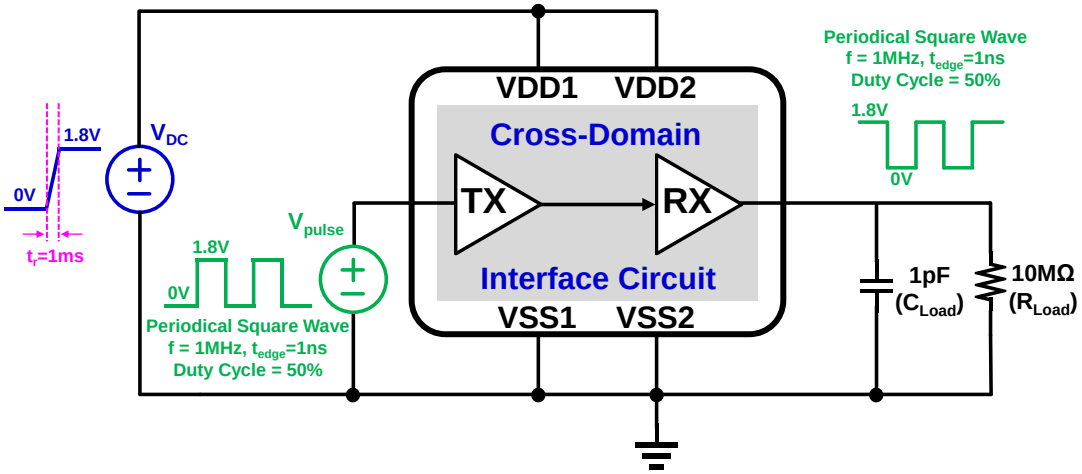


Fig. 2.14. Additional functional simulation set-up for comparing the performance difference of each test-key under normal power-on condition.

Table 2.8

The List of Performance Differences of Proposed Designs Embedded in Cross-Domain Test Circuits

Design Parameter	Unit	Baseline		Rx-CC1		Rx-STC		Tx-CC1		Tx-STC	
		Pre-Sim.	Post-Sim.	Pre-Sim.	Post-Sim.	Pre-Sim.	Post-Sim.	Pre-Sim.	Post-Sim.	Pre-Sim.	Post-Sim.
Frequency	Hz	1M	1M	1M	1M	1M	1M	1M	1M	1M	1M
Duty-Cycle	%	50.60	49.67	51.05	49.33	51.05	49.33	50.61	49.69	50.61	49.69
Rise-Time (t_r)	ns	0.105	0.109	0.202	0.210	0.202	0.211	0.105	0.105	0.105	0.105
Fall-Time (t_f)	ns	0.109	0.111	0.176	0.178	0.176	0.178	0.109	0.109	0.109	0.109
Propagation Delay-Time (t_{DLH})	ns	5.45	5.636	10.44	10.91	10.44	10.9	5.456	5.457	5.456	5.456
Propagation Delay-Time (t_{DHL})	ns	3.207	3.256	4.91	4.965	4.91	4.965	3.246	3.255	3.246	3.254
Dynamic Power	uW	3.636	3.637	3.623	3.624	3.623	3.625	3.551	3.539	3.551	3.539

Design Parameter	Unit	Rx-LD		Rx-CC2		Rx-Latch		Tx-CC2		Tx-Latch	
		Pre-Sim.	Post-Sim.	Pre-Sim.	Post-Sim.	Pre-Sim.	Post-Sim.	Pre-Sim.	Post-Sim.	Pre-Sim.	Post-Sim.
Frequency	Hz	1M	1M	1M	1M	1M	1M	1M	1M	1M	1M
Duty-Cycle	%	49.92	49.9	51.05	49.33	51.05	49.33	50.60	49.69	50.61	49.69
Rise-Time (t_r)	ns	0.00475	0.00487	0.202	0.210	0.202	0.210	0.105	0.105	0.105	0.105
Fall-Time (t_f)	ns	0.00490	0.00259	0.176	0.178	0.176	0.178	0.109	0.109	0.109	0.109
Propagation Delay-Time (t_{DLH})	ns	0.316	0.329	10.47	10.9	10.44	10.89	5.492	5.488	5.457	5.457
Propagation Delay-Time (t_{DHL})	ns	0.33	0.34	4.92	4.962	4.91	4.96	3.264	3.271	3.246	3.255
Dynamic Power	uW	3.9	3.924	3.632	3.631	3.623	3.625	3.64	3.629	3.551	3.539

2.2.2 Predictive Cross-Domain Voltage Under CDM-Like Simulation

In this subsection, the referring CDM simulation method [23] is simplified as a CDM-like current pulse injected from VSS2/VSS1 pin and grounded VDD1/VDD2 pin to qualitatively analyze the cross-domain circuit. The influence of different designs on CDM cross-domain voltage is discussed as well. Note that, the simulation approach can also analyze the CDM failure by applying the measured CDM current peak to the circuit to determine the failure location and find out the victim device.

A. CDM-Like Simulation Setup

As shown in Fig. 2.15, CDM-like simulations have been performed on the VDD1/VDD2 from each power domain to simulate the cross-domain CDM events. Among them, the CDM-like current pulse will be injected from the VSS2/VSS1 pin and switch the VDD1/VSS2 pin to the ground. Assume the CDM charge originally stored in the common p-substrate or accumulated on the VDD/VSS metal wire, the VDD pin is grounded instantly as charge transfer. In principle, expect VDD1/VDD2 pins, else pins maintain the floating state, which is represented as N.C. pin here. During the discharging procedure, the cross-domain voltage will change instantly, causing the interface circuit to suffer transient overstress, especially the receiver module. The main purpose is to estimate the failure location inside the interface circuit and to compare the performance under different test conditions in detail.

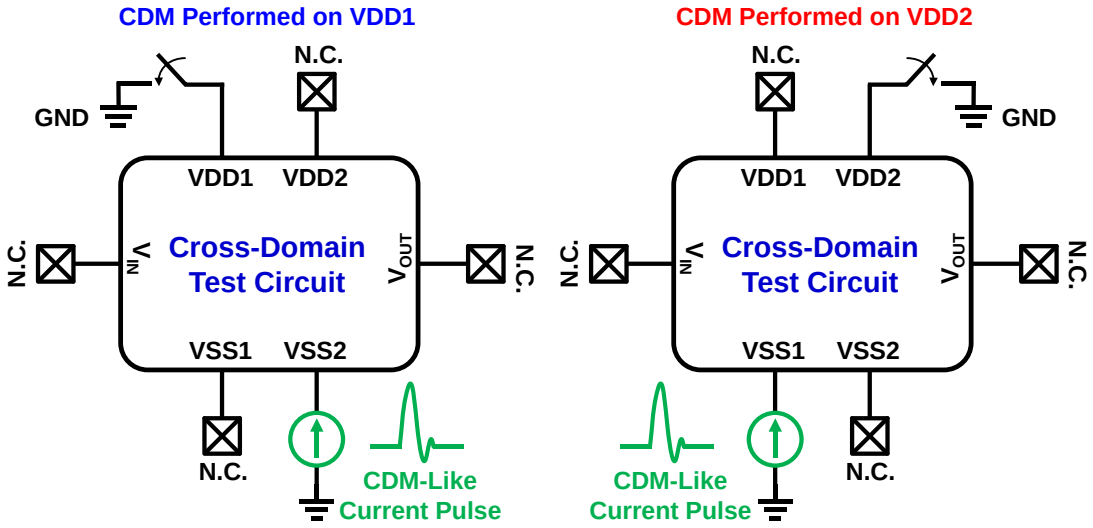


Fig. 2.15. CDM-like simulations have been performed on the VDD1/VDD2 from each power domain to simulate the cross-domain CDM events

A typical CDM discharge current waveform is shown in Fig. 2.16 The parasitic RLC impedance makes the current waveform oscillate and attenuate. The relevant values have been detailing discussed in Chapter 1.4. By modeling the test bench of the

CDM simulator, similar waveforms can be achieved, but not facilitate to analyze. Hence, the ideal piece-wise linear current pulse was adopted, to ignore the impedance matching problem caused by the combination of CDM simulator and test circuits. The CDM current peak is selected 5A with a 200-ps rise time to meet the small capacitance module in JEDEC standard [18]. (see Fig. 2.17.) The current pulses with dual-polarity are continuously applied to the VSS pin as the positive and negative CDM charge displacement. Setting the pulse width to 1.6-ns is easy to observe the instantaneous overvoltage and evaluate the mean value.

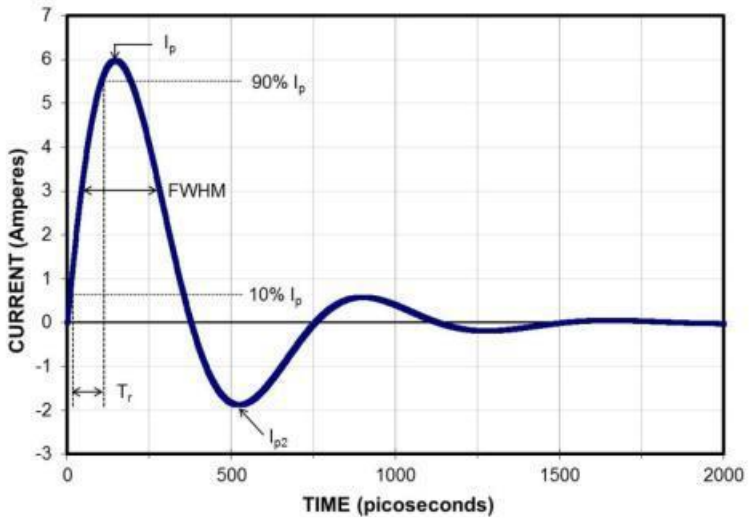


Fig. 2.16. The typical CDM discharge current waveform and parameters.

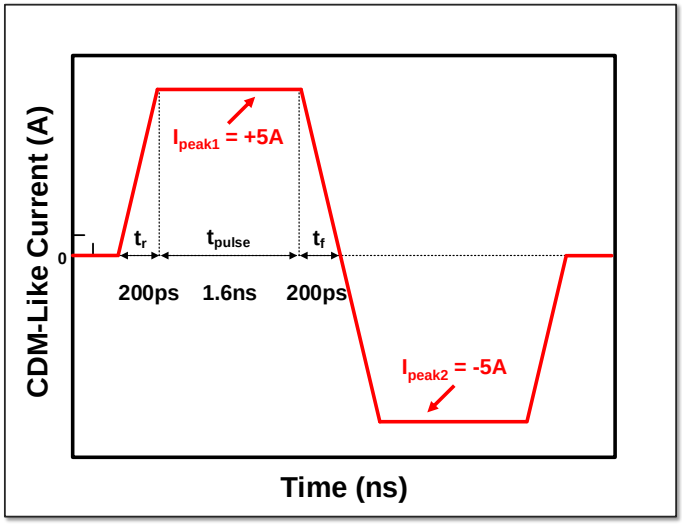


Fig. 2.17. A CDM-like current pulse with 5A peak value, 200-ps rise time, and 1.6-ns duration time.

B. CDM Current Distribution

In general, the CDM current path depends on discharging VDD1 or VDD2, and the current distribution has differences, which depend on discharge mode and conduction impedance of ESD devices. As shown in Fig. 2.18, the currents of the cross-domain test circuit will be observed and help to design the discharge path and the floor plan.

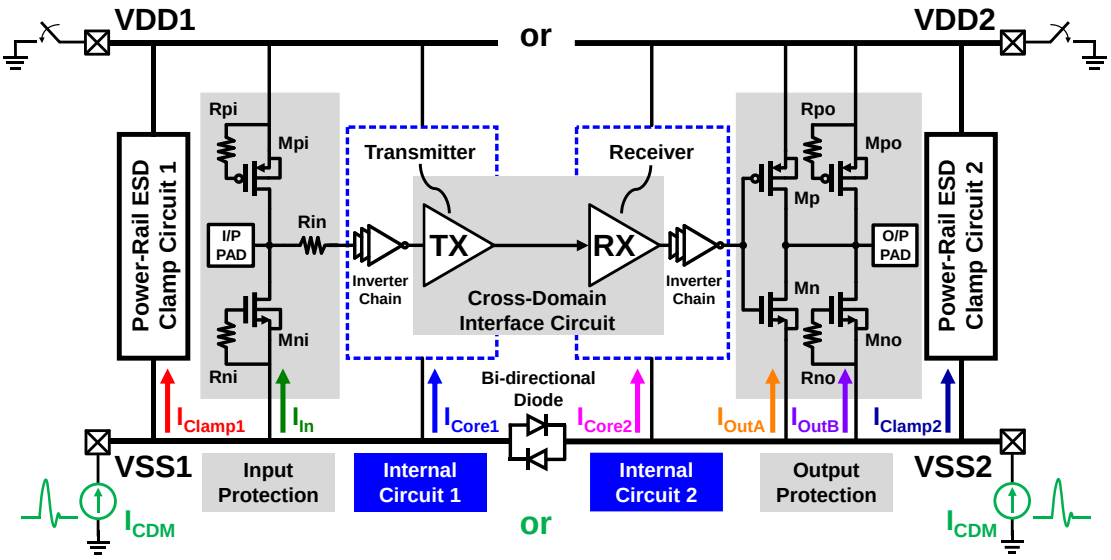


Fig. 2.18. Schematic illustrations of CDM current distributions under CDM-like simulations.

First of all, when CDM simulation was performed on VDD1, the CDM current distribution is shown in Fig. 2.19. Due to separated VDD rails, all currents in the VDD2/VSS2 domain are almost negligible. During the positive pulse period, the CDM current will be dispersed in the power-rail ESD clamp circuit 1 and the input protection, because of the conduction of the large-area parasitic body diode. The other currents through the parasitic path of internal circuit 1 are small enough to be ignored, and the turn-on resistance is determined by all discharge paths in parallel. On the contrary, during the negative pulse period, the CDM current is concentrated in power-rail ESD clamp circuit 1, because the main ESD device is normally turned on. The turn-on

resistance will mostly depend on the ESD clamp circuit 1, which may contribute to more voltage drop. Intuitively, this will be the worst case.

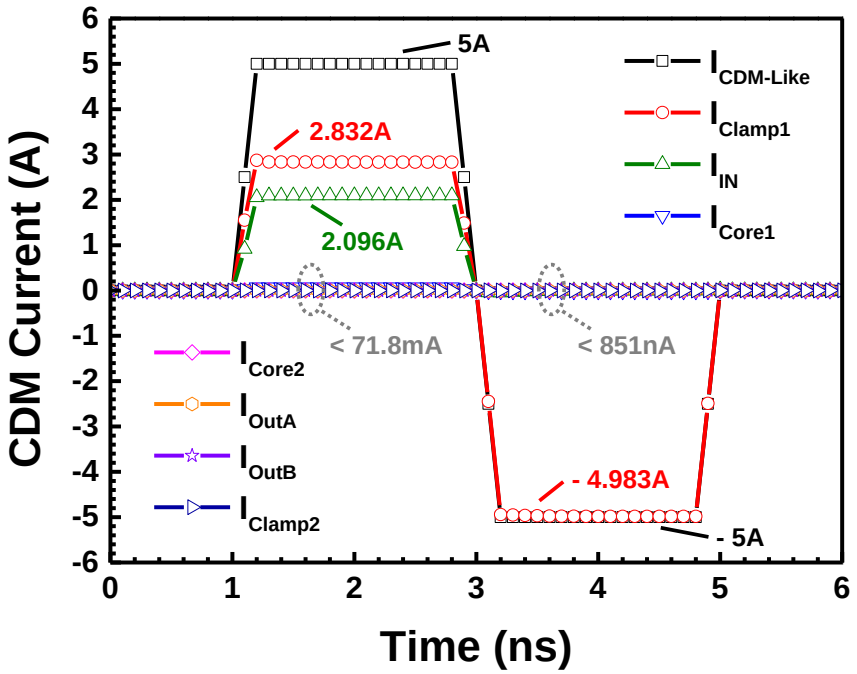


Fig. 2.19. The CDM current distributions when CDM simulation was performed on VDD1. (grounded VDD1 and current injected VSS2)

Second, when CDM simulation was performed on VDD2, the CDM current distribution is shown in Fig. 2.20. Due to separated VDD rails, all currents in the VDD1/VSS1 domain are almost negligible. During the positive pulse period, the CDM current will be dispersed in the power-rail ESD clamp circuit 2 and the output protection. Note that, the current through the power-rail ESD clamp circuit 2 accounts for a high proportion. The other currents through the parasitic path of internal circuit 2 are small enough to be ignored, and the turn-on resistance is still determined by all discharge paths in parallel. On the contrary, during the negative pulse period, the CDM current is concentrated in the power-rail ESD clamp circuit 2, because the main ESD device is normally turned on. The turn-on resistance will mostly depend on the power-rail ESD

clamp circuit 2, which may contribute to more voltage drop. Intuitively, this will be the worst case.

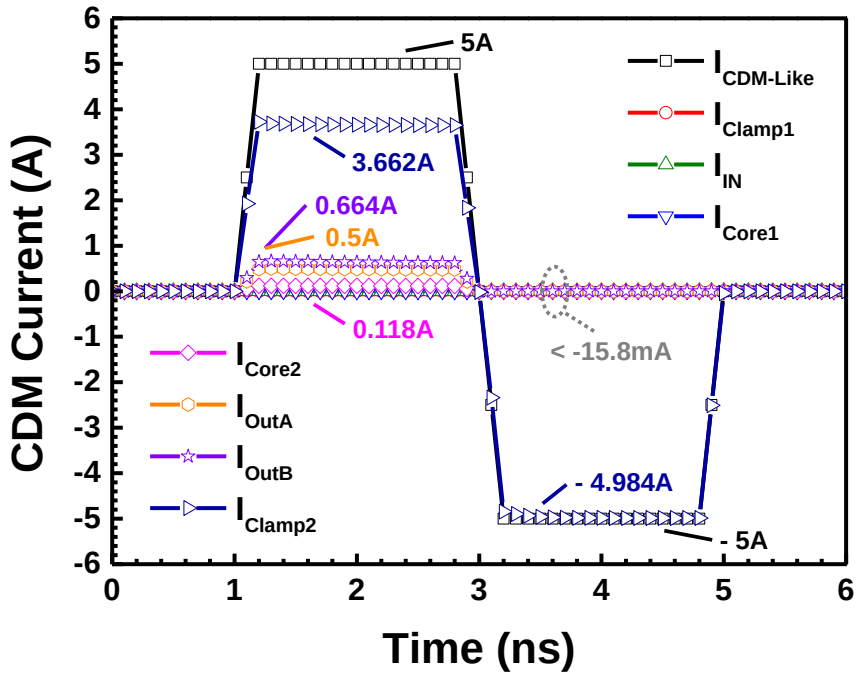


Fig. 2.20. The CDM current distributions when CDM simulation was performed on VDD2. (grounded VDD2 and current injected VSS1)

C. Transient Overvoltage Analysis (Grounded VDD1 and injected I_{CDM} from VSS2)

While CDM simulation was performed on VDD1, the cross-domain voltage waveforms of the RX module with different designs as shown in Fig. 2.21. During the positive CDM period, all the peak voltages V_{gs_MnR} (including V_{gs_MnR1} and V_{gs_MnR2}) across the RX-NMOS gate-oxide, and the peak voltages V_{gs_MpR} (including V_{gs_MpR1} and V_{gs_MpR2}) across the RX-PMOS gate-oxide, are lower than the measured gate-oxide breakdown voltages $|BV_{ox,n}|$ and $|BV_{ox,p}|$, which are the boundary of the safe region. Similarly, during the negative CDM period, all peak voltages V_{gs_MnR} and V_{gs_MpR} which across the gate-oxide of the receiver module are lower than $|BV_{ox,n}|$ and $|BV_{ox,p}|$. In general, inspecting the cross-domain voltage of test circuits in different polarity modes clearly shows that the Rx-NMOS is the victim device and more vulnerable under the negative CDM condition. For easier comparison of the reference design and proposed designs, the zoomed-in views of the cross-domain voltages under positive and negative CDM periods are shown in Fig. 2.22 (a) and Fig. 2.22 (b), respectively.

However, this kind of simulation is too ideal. A more accurate method is introduced: First, extract the parasitic metal resistance and capacitance on the ESD dispassion path from the physical layout. Second, lump complex RC networks into a simple model. Third, bring the simple RC model back to the circuit for re-simulation. Therefore, the actual instantaneous overvoltage must higher than the existing simulation results and even exceed the safe region.

In Fig. 2.22 (a), during the positive CDM period, different designs have some differences. In particular, the test-keys of RX modification have a better voltage-divided effect, which helps to improve the gate-oxide transient overvoltage issue. The other test-keys do not have much benefit at all. Note that, the peak voltages across the gate-oxide of RX-NMOS and RX-PMOS fall in the range of -6.5V to -7.5V. In Fig. 2.22 (b), during the negative CDM period, different designs also have some differences. In particular,

the test-keys of TX modification have a better voltage-divided effect, which helps to improve the gate-oxide transient overvoltage issue. The test-keys of receiver modification can also gain some benefits except Rx-LD and Rx-CC2 designs, which have no obvious benefits on the cross-domain voltage.

Overall, the VDD2 (-) stress could be predicted as the worst-case for all designs. The victim devices were M_{pR} or M_{pR1}, where the failure analysis in Chapter 3 seems to support that as well. Although the stacking-MOS designs were adopted, the difference was slightly between the reference and proposed RX modification designs. Since the header PMOS MpR2 will be turned on during the negative period, cause the stacking-MOS protection design invalid to form a perfect voltage divider.

Note that, the peak voltages across the gate-oxide of RX-NMOS and RX-PMOS fall in the range of 7V to 10V. As a result, during both CDM periods, the stacking-MOS structure designs are respectively used in RX and TX to improve the CDM robustness. The detailed root cause will be discussed below (see Fig. 2.23).

In Fig. 2.23, for the positive CDM period, the parasitic body diode of M_{nT} and M_{pT} were forward conduction because of exceeding the cut-in voltage. The positive CDM charge will be transported by the body diode, thereby increasing the local potential of the floating capacitor on the signal line. Although using stacking-MOS structure designs in TX, similar results will be obtained. On the contrary, if use stacking-MOS structure designs in RX, the footer NMOS M_{nR2} will be turned off to form a high impedance, and activate the voltage divider to slow down the transient overvoltage of M_{nR1}. For the negative CDM period, M_{nT} will be completely turned on and enter the linear region, and the negative CDM charge will be transported by transistor channel, thereby reducing the local potential of the floating capacitor on the signal line to close VSS1. While using stacking-MOS structure designs in TX, the header PMOS M_{nT2} will be turned off to form a high impedance. If using stacking-MOS structure designs in RX, the footer NMOS

M_{nR2} will be turned off at the same time, forming a high-impedance voltage divider to protect M_{nR1}. The simulation waveform can be observed that there are slight differences in the peak voltage of each design, that confirm the proposed design solution is effective.

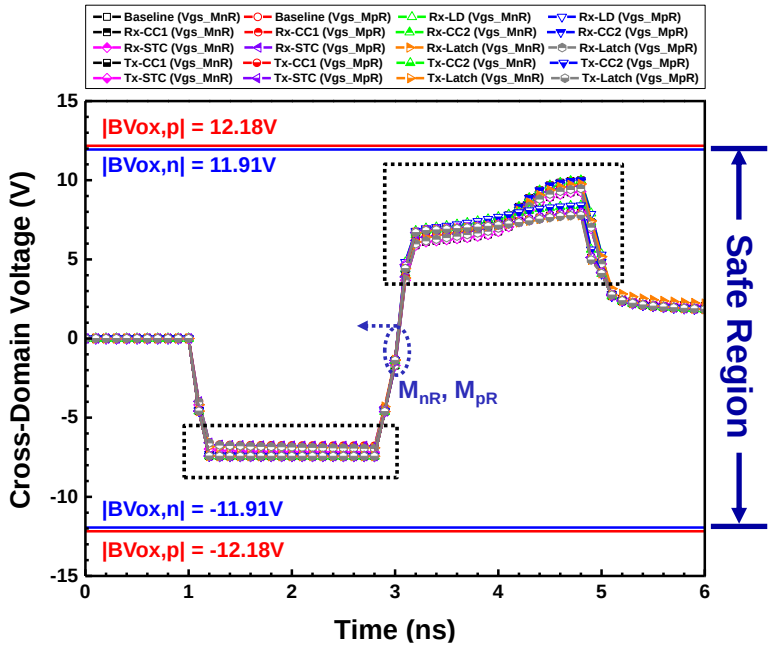
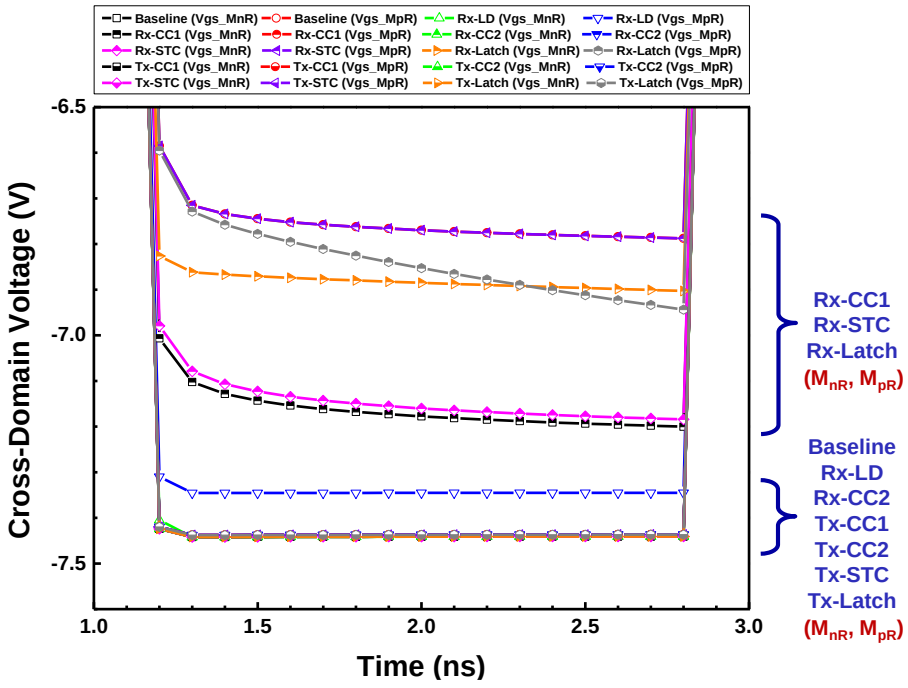
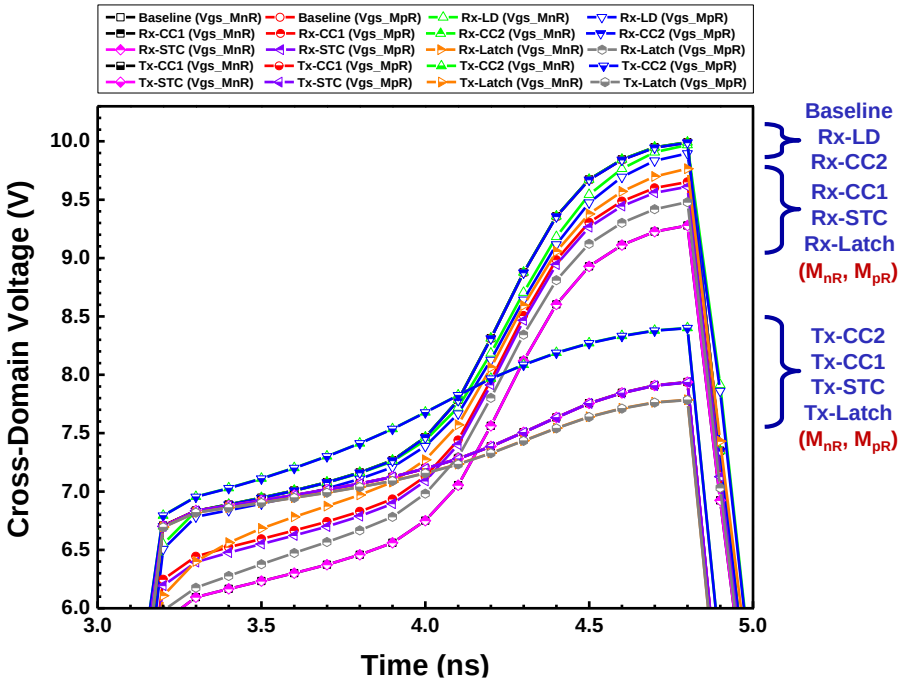


Fig. 2.21. The cross-domain voltage waveforms of RX with different designs, while CDM simulation was performed on VDD1. (grounded VDD1)



(a)



(b)

Fig. 2.22. The zoomed-in illustrations of the cross-domain voltages under (a) positive and (b) negative CDM periods.

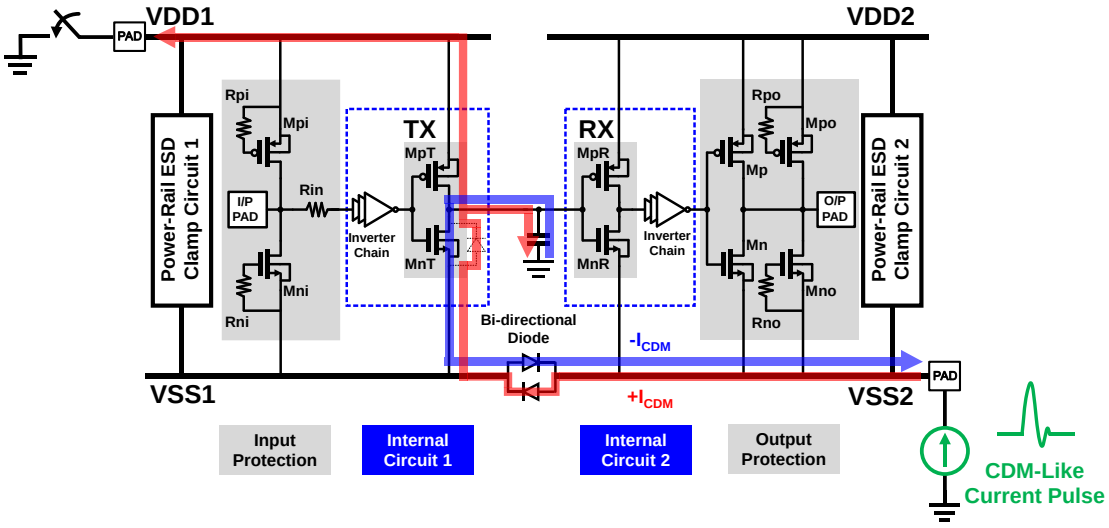


Fig. 2.23. The schematic illustration of parasitic current paths under CDM-like simulation was performed on VDD1. (grounded VDD1)

Additionally, the transient overvoltage of TX was also investigated. The cross-domain voltage waveforms of TX with different designs as shown in Fig. 2.24. During the positive CDM period, the peak voltages V_{gs_MnT} (including V_{gs_MnT1} and V_{gs_MnT2}) across the TX-NMOS gate-oxide, and the peak voltages V_{gs_MpR} (including V_{gs_MpR1} and V_{gs_MpR2}) across the RX-PMOS gate-oxide, are lower than the measured gate-oxide breakdown voltages $|BV_{ox,n}|$ and $|BV_{ox,p}|$. Similarly, during the negative CDM period, all peak voltages across the TX-NMOS gate-oxide and TX-PMOS gate-oxide are lower than $|BV_{ox,n}|$ and $|BV_{ox,p}|$. As a result, during the negative CDM period, TX-MOS gate-oxide transient overvoltages will be slightly serious, but still in the deep safe region. For easier comparison of the reference design and proposed designs, the zoomed-in views of the cross-domain voltages under positive and negative CDM periods are shown in Fig. 2.25 (a) and Fig. 2.25 (b), respectively.

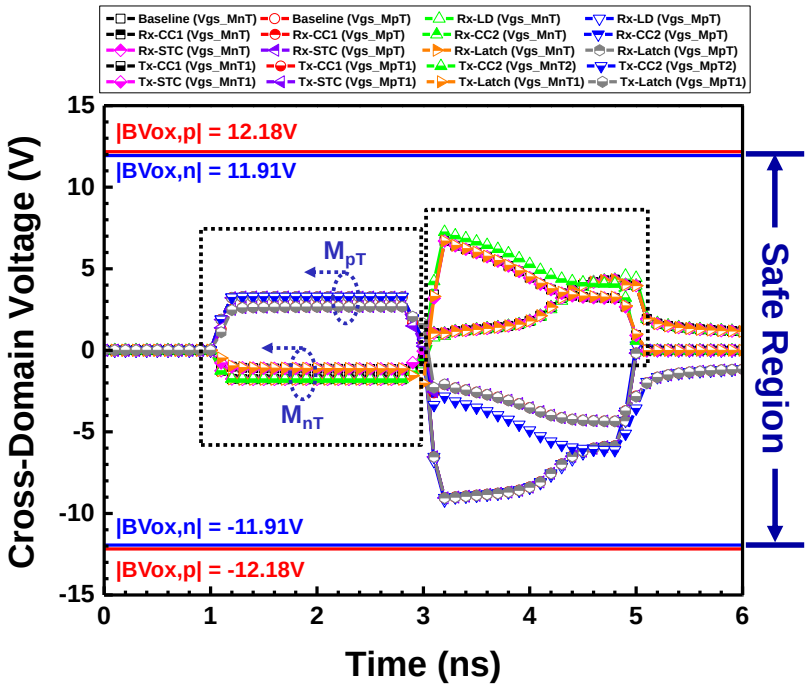
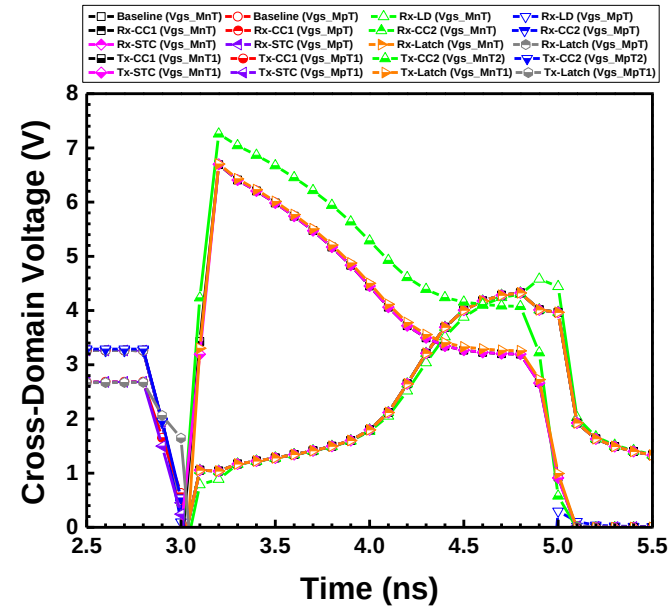
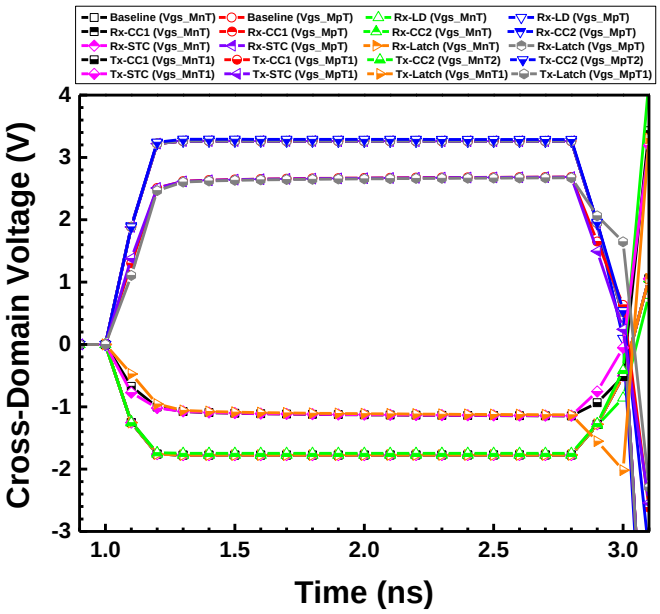


Fig. 2.24. The cross-domain voltage waveforms of TX with different designs, while CDM simulation was performed on VDD1. (grounded VDD1)

In Fig. 2.25, for dual CDM periods, RX modification and TX modification have different characteristics, but no key factor to show specific correlation and trend. Fortunately, the peak voltages of TX-NMOS and TX-PMOS are far away from the safe region boundary. Therefore, the transient overvoltage of TX-MOS does not need to be discussed and concerned in detail.



(a)



(b)

Fig. 2.25. The zoomed-in illustrations of the cross-domain voltages under (a) positive and (b) negative CDM periods.

D. Transient Overvoltage Analysis (Grounded VDD2 and injected I_{CDM} from VSS1)

To repeat, while CDM simulation was performed on VDD2, the cross-domain voltage waveforms of RX with different designs as shown in Fig. 2.26. During the positive CDM period, the peak voltages V_{gs_MnR} (including V_{gs_MnR1} and V_{gs_MnR2}) across the RX-NMOS gate-oxide are lower than the $|BV_{ox,n}|$, but the peak voltages V_{gs_MpR} (including V_{gs_MpR1} and V_{gs_MpR2}) across the RX-PMOS gate-oxide are closer to the $|BV_{ox,p}|$. Likewise, during the negative CDM period, the peak voltages V_{gs_MnR} are lower than the $|BV_{ox,n}|$, but the peak voltages V_{gs_MpR} are much higher than the $|BV_{ox,p}|$. So, the RX-PMOS gate-oxides suffer from severe transient overvoltage in different CDM periods, especially the negative period. In contrast, the peak voltages of RX-NMOS are much smaller than the safe region boundary. Therefore, it can be identified that RX-PMOS gate-oxides will be damaged first and accompanied by a very low CDM level. As a result, inspecting the cross-domain voltage of test circuits in different polarity modes clearly shows that the Rx-PMOS is the victim device and more vulnerable under the negative CDM condition. For easier comparison of the reference design and proposed designs, the zoomed-in views of the cross-domain voltages under positive and negative CDM periods are shown in Fig. 2.27 (a) and Fig. 2.27 (b), respectively.

In Fig. 2.27 (a), during the positive CDM period, only part of the RX modifications (Rx-CC1, Rx-STC, Rx-Latch) have a better voltage-division effect, which helps to improve the gate-oxide transient overvoltage issue. But, the other test-keys do not have much benefit at all. The peak voltages of all RX-PMOS fall in the range of 10V to 12V, while the peak voltages of RX-NMOS fall in the range of 5V to 6.5V. In Fig. 2.27 (b), during the negative CDM period, there is no significant difference between the different designs. In other words, the design of the stacking-MOS structure cannot form a perfect voltage divider and helpless to improve the gate-oxide transient overvoltage issue. The

peak voltages of all Rx-NMOS and Rx-PMOS fall in the range of -14.5V to -15.5V. As a result, only during the positive CDM period, the stacking-MOS structure designs in RX can perform a good effect. The detailed root cause will be discussed below (see Fig. 2.28).

In Fig. 2.28, for the positive CDM period, the parasitic body diode of M_{nT} was forward conduction because of exceeding the cut-in voltage, and the positive CDM charge will transport by the body diode. For the negative CDM period, M_{nT} will be completely turned on into the linear region, and the negative CDM charge will be transported by transistor channel surface. For both CDM periods, the floating parasitic capacitance of the signal line will be coupled to a potential close to VSS1.

Even if the stacking-MOS structure is used in the TX, the conductions of the transistor or parasitic diode were existed, and form a low impedance, which cannot generate a perfect voltage divider. On the other hand, if the stacking-MOS structure is used in the RX (Rx-CC1, Rx-STC, Rx-Latch), M_{pR2} will be turned off during the positive CDM period to form a high impedance, which generates a voltage divider to couple part of voltage to V_p node and slow down the transient overvoltage of M_{pR1}. However, during a negative CDM period, M_{pR2} will be turned on to form a low impedance, and the V_p node will be pulled close to the VDD2 potential (~0V), degenerating the voltage division effect. In the end, the peak voltage will only cross the gate-oxide of M_{pR1}. This phenomenon can be observed from the simulation waveform. As a result, RX-PMOS is the most difficult to be effectively protected under negative CDM stress. Even adopting the proposed design solutions, the intrinsic threats of the ESD dissipation path still exists.

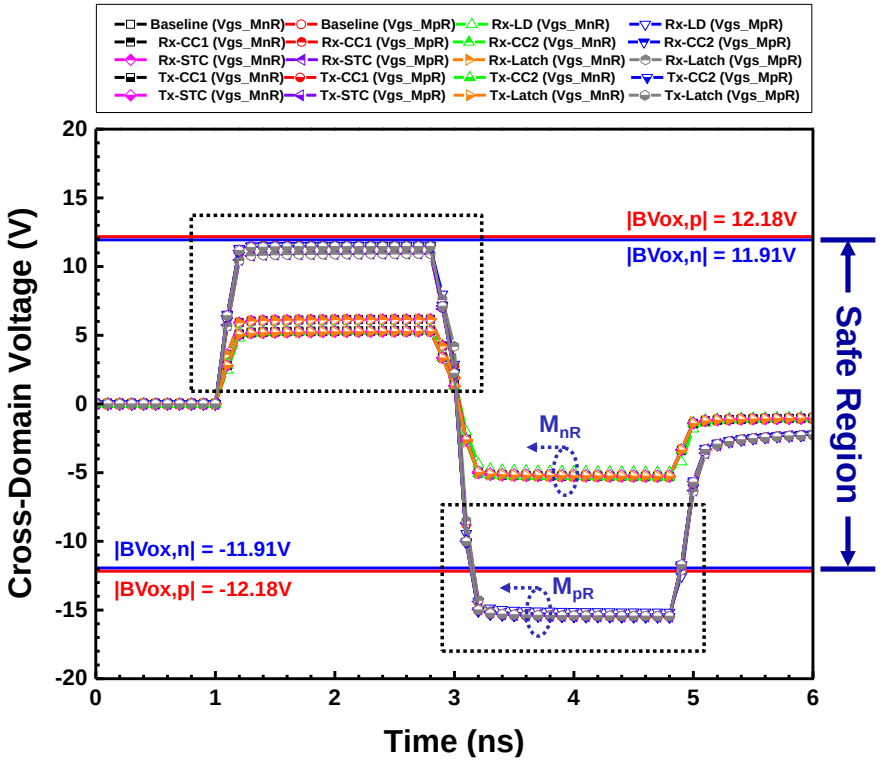
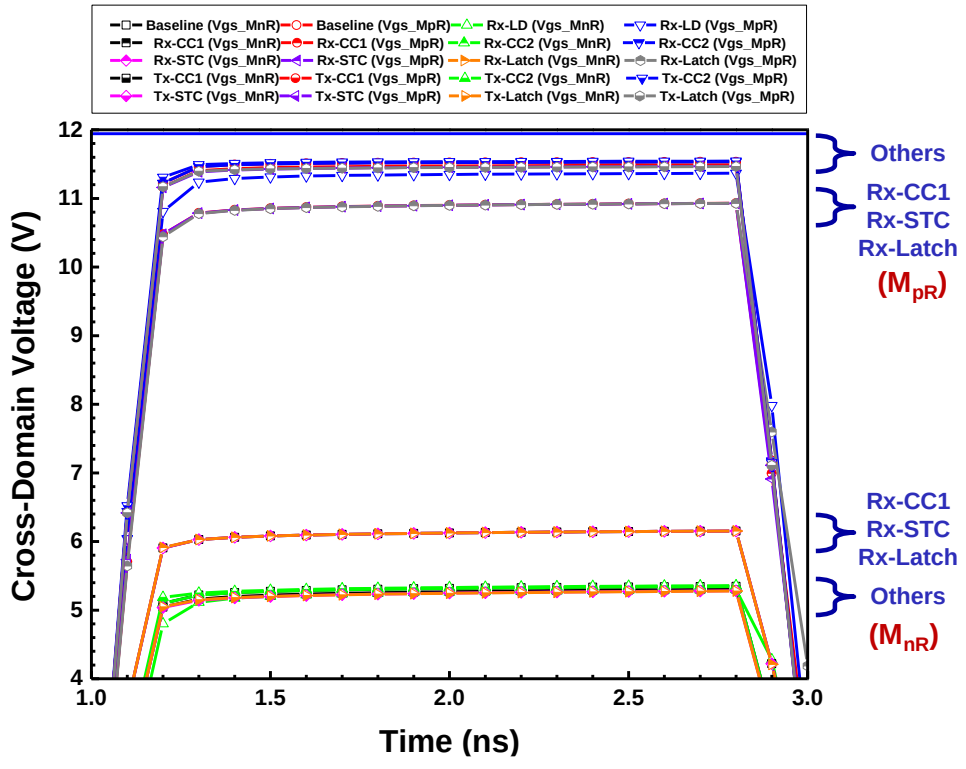
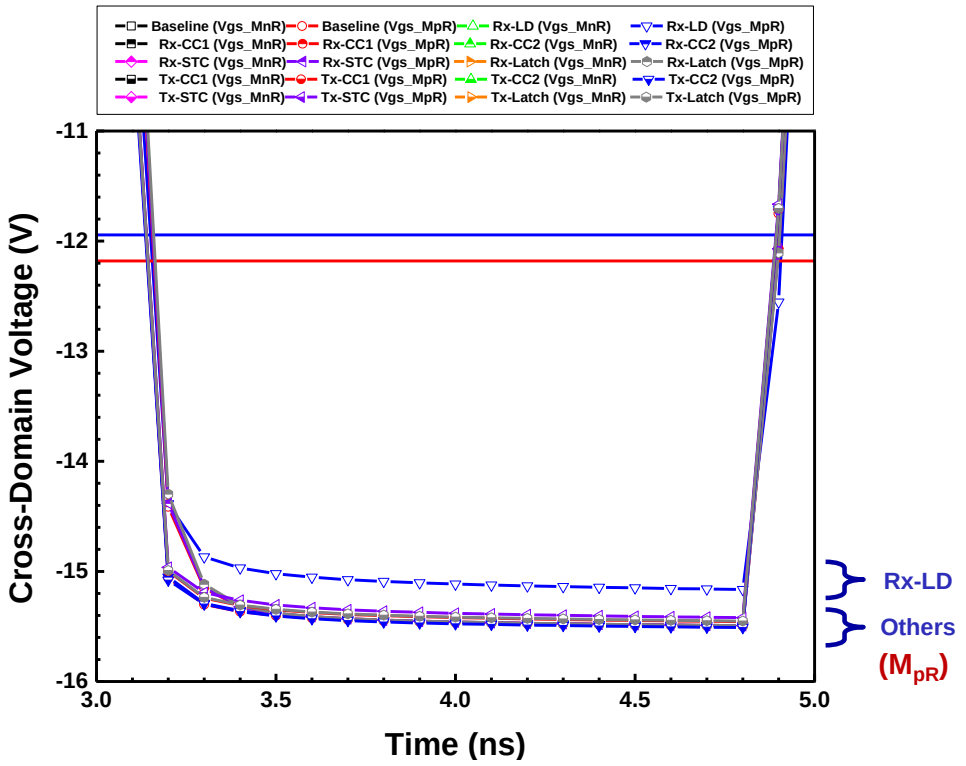


Fig. 2.26. The cross-domain voltage waveforms of RX with different designs, while CDM simulation was performed on VDD2. (grounded VDD2)



(a)



(b)

Fig. 2.27. The zoomed-in illustrations of the cross-domain voltages under (a) positive and (b) negative CDM periods.

(b)

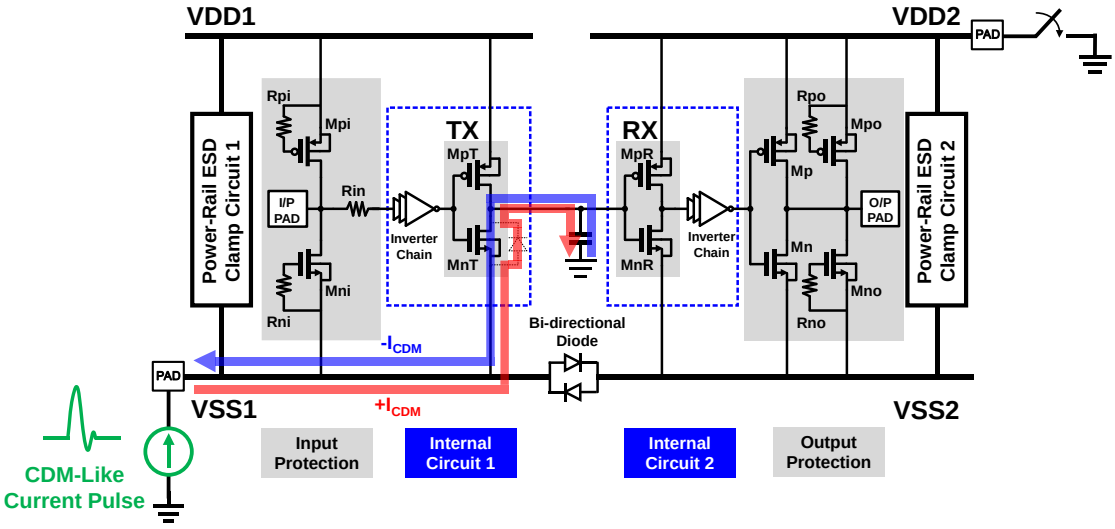


Fig. 2.28. The schematic illustration of parasitic current paths under CDM-like simulation was performed on VDD2. (grounded VDD2)

Additionally, the transient overvoltage of TX was also investigated. The cross-domain voltage waveforms of the Tx module with different designs as shown in Fig. 2.29. During dual CDM periods, the peak voltages V_{gs_MnT} which across the TX-NMOS gate-oxides, and the peak voltages V_{gs_MpR} which across the Tx-PMOS gate-oxides, are much lower than the measured gate-oxide breakdown voltages $|BV_{ox,n}|$ and $|BV_{ox,p}|$. The zoomed-in view of both polarities is shown in Fig. 2.30.

In Fig. 2.30, there is no key factor to show specific correlations and trends. Fortunately, the peak overvoltages of TX-NMOS and TX-PMOS are very far away from the safe region boundary. In other words, only the receiver module has serious transient overvoltage issues. Therefore, the transient overvoltage of TX-MOS does not need to be discussed and concerned in detail.

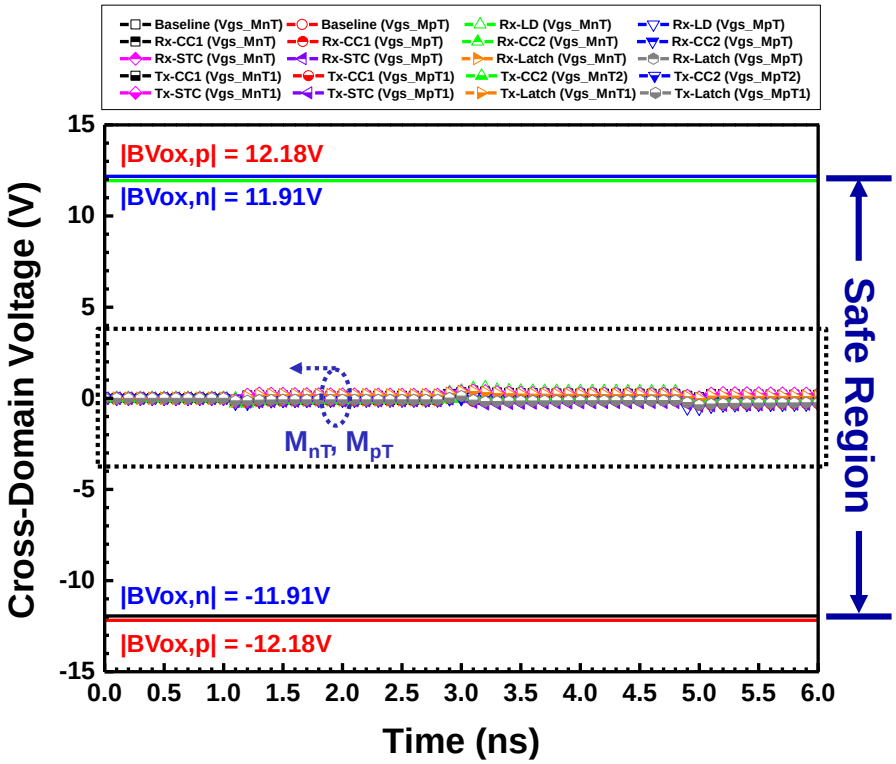


Fig. 2.29. The cross-domain voltage waveforms of TX with different designs, while CDM simulation was performed on VDD2. (grounded VDD2)

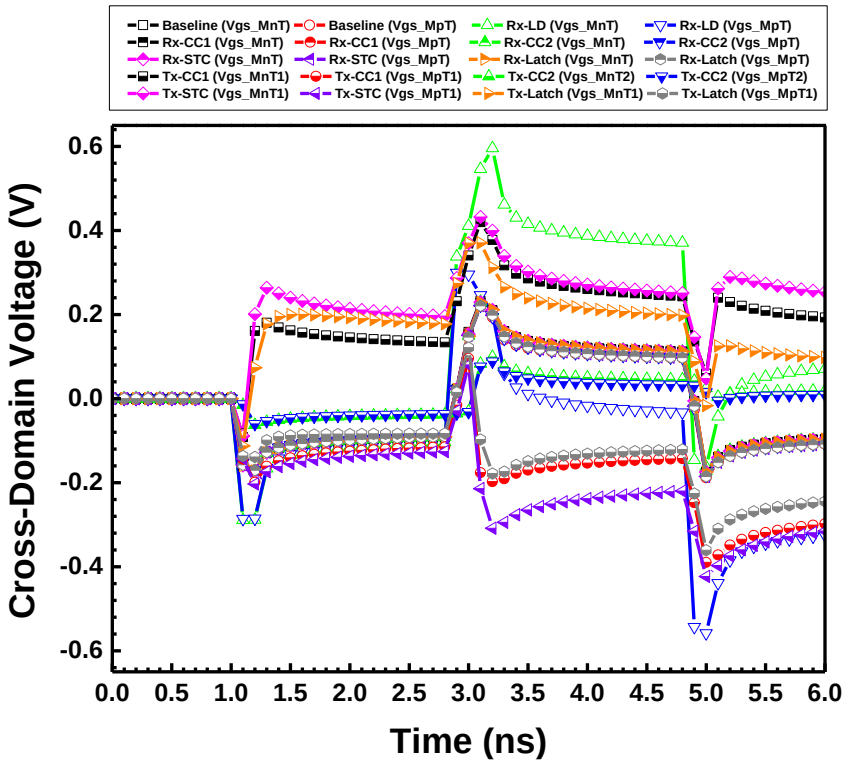


Fig. 2.30. The zoomed-in illustrations of the cross-domain voltages under both positive and negative CDM periods.

2.2.3 Summary

The functional simulation has been used to ensure that different test-keys can be applied to each cross-domain test circuit to achieve the same function. Indeed, no matter the design of the stacking-MOS structure is embedded in the RX or TX, there will be some differences in area, power consumption, or performance. The size can be modulated appropriately to optimize each cell. The predictive CDM-like simulation is also used as a method in circuit-level design to analyze the current distribution of the ESD dissipation path, and monitor cross-domain voltage as an inspection for transient overvoltage issues.

As a result, RX-NMOS/RX-PMOS is the victim while negative CDM is performed on the VDD1/VDD2, the key element comes from the parasitic effects of TX-NMOS, and additional current paths are generated during the transient period of rapid discharge. The local potential on the signal line is disturbed, which affects the transient overvoltage of the cross-domain interface circuits. The simulation results are only used to qualitatively analyze the effect of the protection circuit, which means that the actual CDM ESD performance cannot be guaranteed. Furthermore, the accuracy improvement requires lots of factors: the extraction of parasitic parameters, the estimation of the chip size, the position of the discharge pin, and the packaging form, to build a complete test model, some simulation procedures have been discussed in detail [23]–[24].

2.3 Performance-Area Comparison

The functional simulation setup of cross-domain interface circuits is shown in Fig. 2.12, probing the rise time, fall time, and internal propagation delay time of RX. Moreover, the comparison between proposed designs and prior art designs in terms of die area impact and performance impact has been provided and summarized in Table 2.9 ~ Table 2.11. Indeed, new proposed designs can obtain area advantages, especially Rx-CC1, Rx-CC2, and Rx-Latch, but the speed will be limited by the stacking-MOS structure, which can be traded off by optimizing the size of the transistor. Although the prior art designs occupy more area, the difference in terms of speed is relatively small.

Furthermore, the performance limit (in terms of speed) can be evaluated by maximum frequency (f_{max}) and use the simulation (see Fig. 2.12) to set the frequency of input signal as a variable for scanning. If the logic high level of the output signal is lower than VDD/2, the malfunction will happen in the post-stages, and the input frequency at this time is defined as the f_{max}. The proposed Rx-designs have a relatively low f_{max} in between due to the stacking-MOS structure. However, this can be optimized by sizing the transistor width. In this experiment, the Rx-Latch design still has a stable output at different signal speeds. Therefore, if the transistor size in the latch structure can be well designed, and make sure the function correct by appropriate input patterns, the latch structure will still be a good solution.

Subsequently, other specifications like duty-cycle, DC leakage, and power consumption have been listed for comparison by simulation. The most of designs are within the originally expected range (Table 2.1), and the silicon chip will also provide some measured factors to compare the differences with simulation results.

Table 2.9

Performance-Area Comparison Table of Prior Art Designs

Spec. (Pre-Sim)	Baseline	GGNMOS + GDPMOS M_{nESD} = 10μ/0.18μ M_{pESD} = 10μ/0.18μ R_{ESD} = 200Ω	Dual Diode D_p = 10μ D_n = 10μ (Total Perimeter)	GCT Technique M_{GCT} = 10μ/0.18μ	GC Technique M_{GCN} = 10μ/0.18μ M_{GCP} = 10μ/0.18μ
Process Technology	TSMC 0.18μm 1.8V / 3.3V CMOS process				
Power Supply [V]	VDD1 = VDD2 = +1.8, VSS1 = VSS2 = 0V				
Input / Output Signal Swing [V]	$V_{IN} = V_{OUT}$ = 0 ~ +1.8 (Full Swing)				
Duty-Cycle [%]	50.12	50.12	50.12	50.12	50.12
Maximum Input Clock Frequency (f_{max}) [MHz] (Pure Interface Circuit)	96.4	92.68	94.22	93.13	92.45
DC leakage [nA]	I_{DD1} = 1.292 I_{DD2} = 181.48	I_{DD1} = 1.41 I_{DD2} = 181.49	I_{DD1} = 1.295 I_{DD2} = 181.49	I_{DD1} = 1.41 I_{DD2} = 181.49	I_{DD1} = 1.342 I_{DD2} = 181.49
Power Consumption @ f=1MHz (P_{VDD1}) [μW]	P_S = 0.00233 P_D = 1.26	P_S = 0.00254 P_D = 1.26	P_S = 0.00233 P_D = 1.26	P_S = 0.00254 P_D = 1.26	P_S = 0.00242 P_D = 1.26
Power Consumption @ f=1MHz (P_{VDD2}) [μW]	P_S = 0.327 P_D = 82.69	P_S = 0.327 P_D = 89.24	P_S = 0.327 P_D = 103.49	P_S = 0.327 P_D = 87.14	P_S = 0.327 P_D = 84.95
Pure Interface Circuit Area [μm^2]	29.7	140.95	125.6	119.52	119.52
Internal Circuit Area [μm^2]	96.53	207.43	192.1	186.6	186.6

Table 2.10

Performance-Area Comparison Table of Proposed Rx-Designs

Spec. (Pre-Sim)	Baseline	Rx-LD	Rx-CC1	Rx-CC2	Rx-STC	Rx-Latch
Process Technology	TSMC 0.18μm 1.8V / 3.3V CMOS process					
Power Supply [V]	VDD1 = VDD2 = +1.8, VSS1 = VSS2 = 0V					
Input / Output Signal Swing [V]	$V_{IN} = V_{OUT}$ = 0 ~ +1.8 (Full Swing)					
Duty-Cycle [%]	50.12	50.12	50.13	50.13	50.13	50.13
Maximum Input Clock Frequency (f_{max}) [MHz] (Pure Interface Circuit)	96.4	>1000	48.37	48.71	48.37	48.12
DC leakage [nA]	I_{DD1} = 1.292 I_{DD2} = 181.48	I_{DD1} = 1.292 I_{DD2} = 181.55	I_{DD1} = 1.292 I_{DD2} = 181.49	I_{DD1} = 1.292 I_{DD2} = 181.49	I_{DD1} = 1.292 I_{DD2} = 181.49	I_{DD1} = 1.292 I_{DD2} = 181.49
Power Consumption @ f=1MHz (P_{VDD1}) [μW]	P_S = 0.00233 P_D = 1.26	P_S = 0.00233 P_D = 1.26	P_S = 0.00233 P_D = 1.26	P_S = 0.00233 P_D = 1.26	P_S = 0.00233 P_D = 1.26	P_S = 0.00233 P_D = 1.26
Power Consumption @ f=1MHz (P_{VDD2}) [μW]	P_S = 0.327 P_D = 82.69	P_S = 0.327 P_D = 72.95	P_S = 0.327 P_D = 72.02	P_S = 0.327 P_D = 82.92	P_S = 0.327 P_D = 71.99	P_S = 0.327 P_D = 71.83
Pure Interface Circuit Area [μm^2]	29.7	64.36	33.08	34.15	47.27	33.39
Internal Circuit Area [μm^2]	96.53	136.14	104.86	105.93	119.05	105.17

Table 2.11

Performance-Area Comparison Table of Proposed Tx-Designs

Spec. (Pre-Sim)	Baseline	Tx-CC1	Tx-CC2	Tx-STC	Tx-Latch
Process Technology	TSMC 0.18μm 1.8V / 3.3V CMOS process				
Power Supply [V]	VDD1 = VDD2 = +1.8, VSS1 = VSS2 = 0V				
Input / Output Signal Swing [V]	V_{IN} = V_{OUT} = 0 ~ +1.8 (Full Swing)				
Duty-Cycle [%]	**50.12**	**50.12**	**50.12**	**50.12**	**50.12**
Maximum Input Clock Frequency (f_{max}) [MHz] (Pure Interface Circuit)	**96.4**	**94.25**	**93.37**	**94.16**	**94.16**
DC leakage [nA]	**I_{DD1} = 1.292 I_{DD2} = 181.48**	**I_{DD1} = 1.292 I_{DD2} = 181.49**	**I_{DD1} = 1.28 I_{DD2} = 181.49**	**I_{DD1} = 1.292 I_{DD2} = 181.49**	**I_{DD1} = 1.292 I_{DD2} = 181.49**
Power Consumption @ f=1MHz (P_{VDD1}) [μW]	**P_S = 0.00233 P_D = 1.26**	**P_S = 0.00233 P_D = 1.21**	**P_S = 0.0023 P_D = 1.21**	**P_S = 0.00233 P_D = 1.21**	**P_S = 0.00233 P_D = 1.21**
Power Consumption @ f=1MHz (P_{VDD2}) [μW]	**P_S = 0.327 P_D = 82.69**	**P_S = 0.327 P_D = 90.94**	**P_S = 0.327 P_D = 84.77**	**P_S = 0.327 P_D = 90.94**	**P_S = 0.327 P_D = 90.94**
Pure Interface Circuit Area [$μm^2$]	**29.7**	**53.28**	**55.07**	**69.6**	**53.35**
Internal Circuit Area [$μm^2$]	**96.53**	**125.06**	**126.85**	**141.4**	**125.13**

Chapter 3
Experimental Results and Failure Analysis

This chapter is divided into four sections. The CDM discharge mechanism and test chip design are briefly introduced in 3.1. The introductions of verification methods and failure criteria are illustrated in 3.2. The ESD measurement results are discussed in 3.3. Finally, failure analysis has been done and discussed in 3.4.

3.1 CDM Discharge Mechanism and Test Chip Design

3.1.1 Field Induced-Charge Device Model (FI-CDM) ESD Tester

The CDM ESD test can be roughly classified into socket mode and non-socket mode. The former is to place the IC on the socket, charge the socket with specific energy, and then switch the discharge pin of the device under test (DUT) to the ground. The discharge current is almost affected by the parasitic capacitance of the socket. Different from the former, the latter is to place the IC on the charge plate for electrification, and then transfer the charge to the external ground pin. Thermo Scientific Orion3, is a non-socket mode CDM ESD test system, as shown in Fig. 3.1, suitable for field-induced chip-level or board-level CDM ESD test, and supports all popular industry test standards: JS-002, JEDEC, ESDA, AEC, JEITA, and CCDM methods.

The detailed markings of the experimental setup are shown in Fig. 3.2. First, the DUT is placed on a platform made up of an upper insulator and a downer field plate, with an L Bracket as the initial alignment position of the sample. Usually, packaged ICs are placed on the field plate in the dead bug position. The DUT in the figure takes the chip

on board (COB) as an example, and the exposed metal fingers are normally placed upward. Second, the pogo pin used for discharging is connected to the upside ground plate through a 1Ω resistor. Besides, a high-frequency oscilloscope with a minimum bandwidth (BW) of 9 GHz is also connected to the 1Ω resistor to capture the discharge voltage and current waveform. Third, by energizing the field charging plate, according to the principle of charge induction, the component will be raised to a specific potential with opposite polarity. Finally, through the computer-aided software to set the precise coordinates, combined with the high-resolution dual camera, quickly align the pogo pin to contact the designated pin. The CDM discharge is generally completed in a few nanoseconds, and discharged waveforms are observed by a high-frequency oscilloscope.

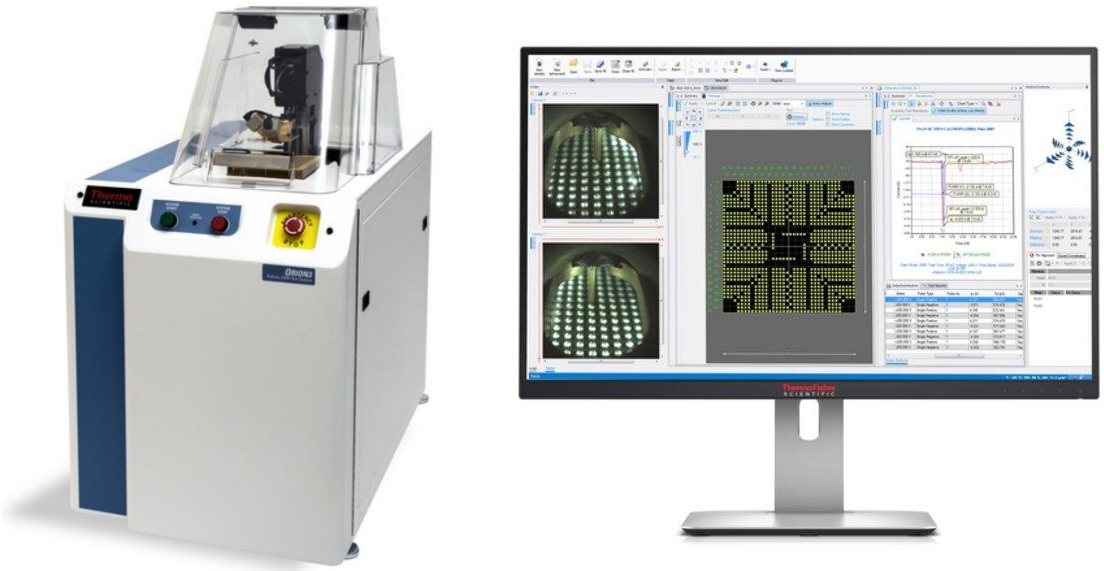


Fig. 3.1. A commercial non-socket mode field-induced CDM ESD test system (Thermo Scientific Orion3).

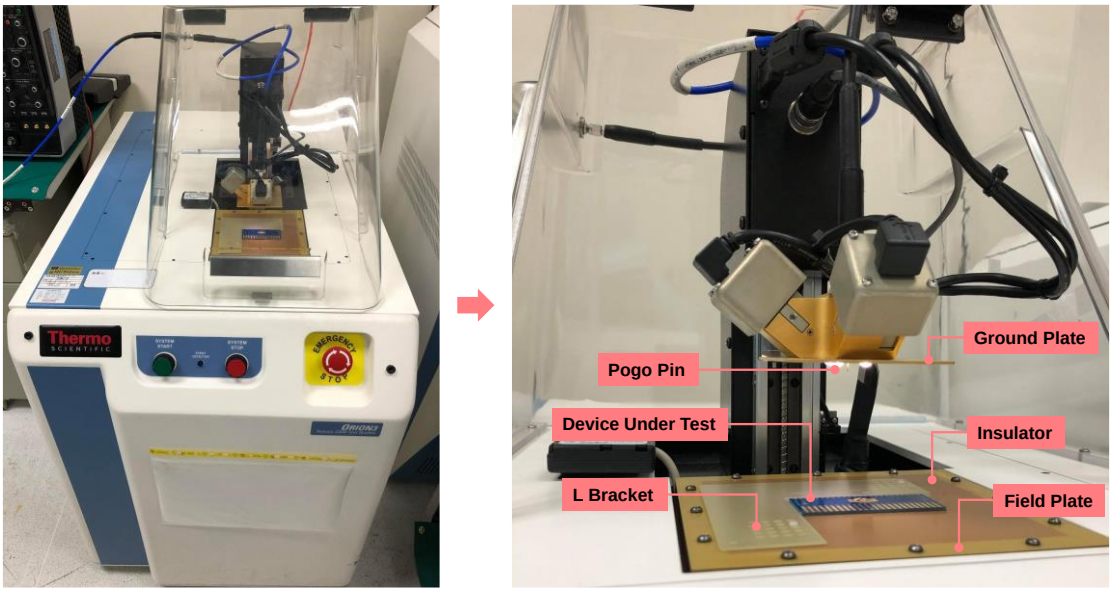


Fig. 3.2. The detailed markings of the experimental setup of Thermo Scientific Orion3.

The CDM ESD tester can be drawn into a simplified diagram with the equivalent circuit as shown in Fig. 3.3. The CDM ESD tester uses CDF, CDG, and CFG capacitors to model: CDF is between DUT and field plate, while CDG is between DUT and ground plate, and CFG is between the field plate and ground plate. The field plate is connected with the charging resistor and then switch to the high-voltage supply or ground to form different current loops, based on the charging procedure. The oscilloscope is connected to the pogo pin with 1Ω R_{eff} to collect the waveform data of each test. The pogo pin to ground connection can be regarded as the parallel combination of 1-ohm R_{eff} and 50-ohm impedance, which is formed by the oscilloscope and coaxial cable. The resistance of the spark which forms between the pogo pin and the DUT is assumed to be a variable resistance. The inductance of the pogo pin and spark are lumped together as a single inductor [18].

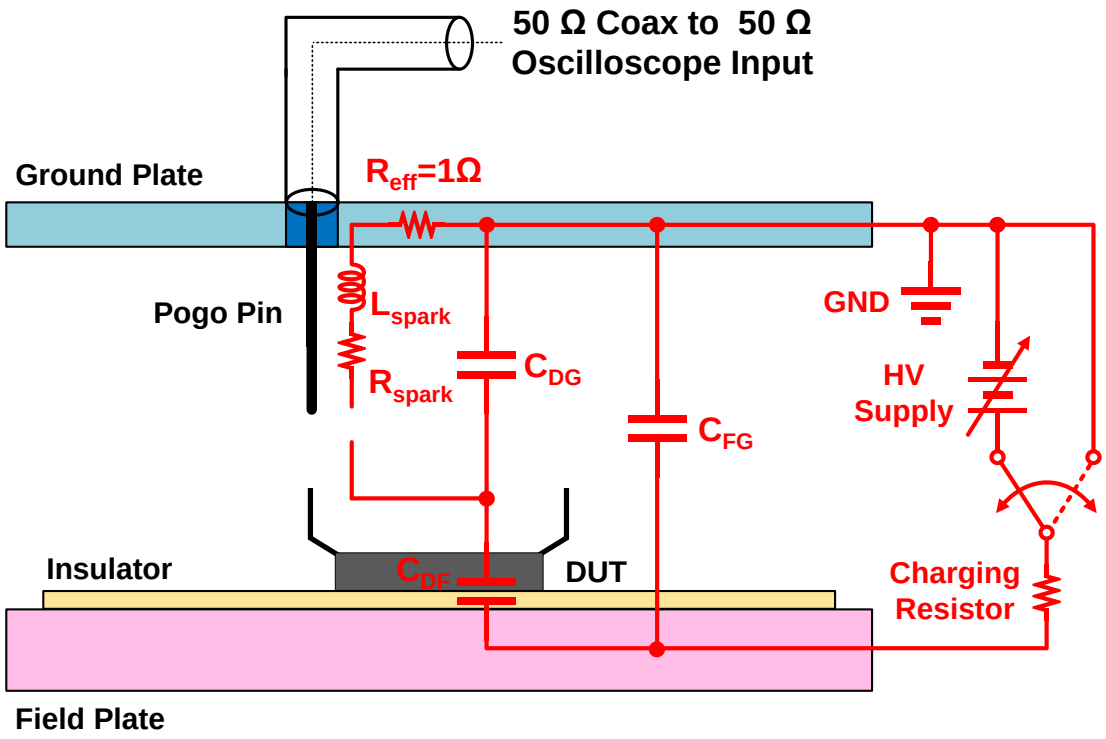


Fig. 3.3. A simplified diagram with the equivalent circuit of the CDM ESD tester.

For more practical expression in another way, the CDM ESD event can be considered as any pin of the IC is suddenly grounded, which leads to a cross-domain CDM issue, as shown in Fig. 3.4. The CDM charge Q_{CDM} stored inside the common p-substrate of an IC can be derived from the charge storage equation:

$$Q_{CDM} = C_{CDM} \times \mathrm{V} \tag{3.1}$$

Note that, the C_{CDM}, represents the total parasitic capacitance of the DUT related to ground and V represents the ESD voltage charged by the HV supply. The equivalent capacitance for C_{CDM} can be formed from the DUT to ground by capacitor series/parallel formula:

$$C_{CDM} = C_{DG} + \frac{C_{FG} \times C_{DF}}{C_{FG} + C_{DF}} \tag{3.2}$$

Next, the CDM discharge current $\mathrm{I_{CDM}}$ can be calculated by differentiating the CDM charge Q_{CDM} to the discharge time t:

$$I_{CDM} = \frac{dQ_{CDM}}{dt} \tag{3.3}$$

Therefore, the CDM peak current mainly depends on the amount of CDM charge (Q_{CDM}) inside the common p-substrate of an IC, that is, the value of the equivalent capacitor (C_{CDM}) under the same charged voltage (V). The C_{CDM} is mainly determined by C_{DF} and C_{FG} in series since C_{DG} is quite small among them. The C_{DF} is proportional to die size, thickness, and package form. For small DUT, which has smaller C_{DF} than C_{FG}, the CDM peak current tends to be more sensitive to the value of the C_{DF}. As C_{DF} becomes larger than C_{FG}, the CDM peak current of the discharge waveform becomes insensitive to C_{DF}.

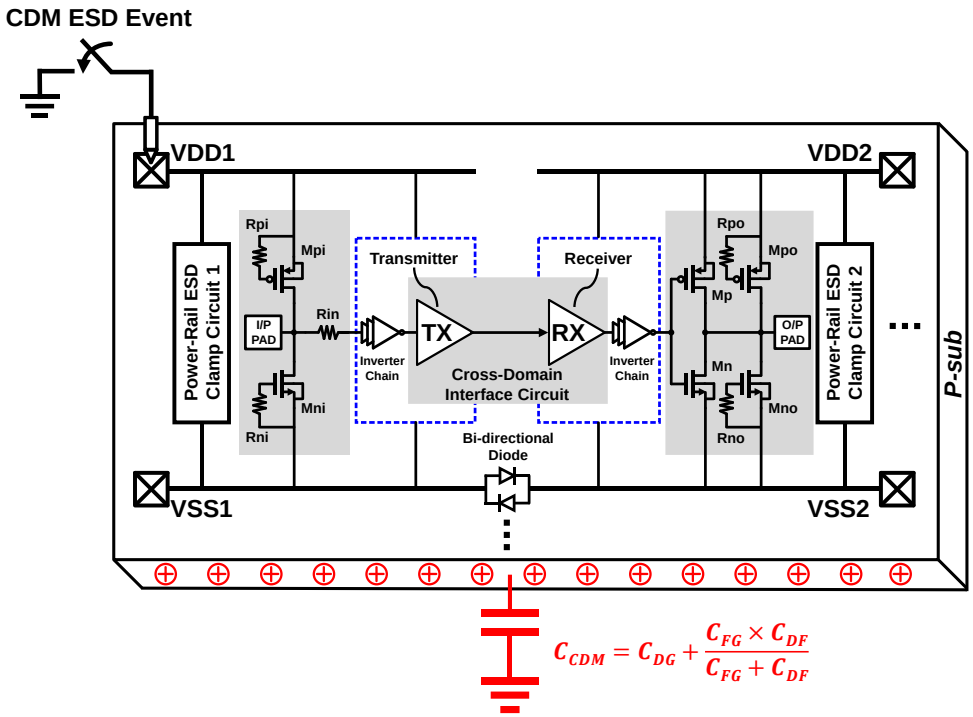


Fig. 3.4. A CDM ESD event: As a certain pin is grounded, the stored static charge determined by equivalent capacitance and charged voltage will be suddenly discharged.

3.1.2 FI-CDM ESD Discharge Procedure

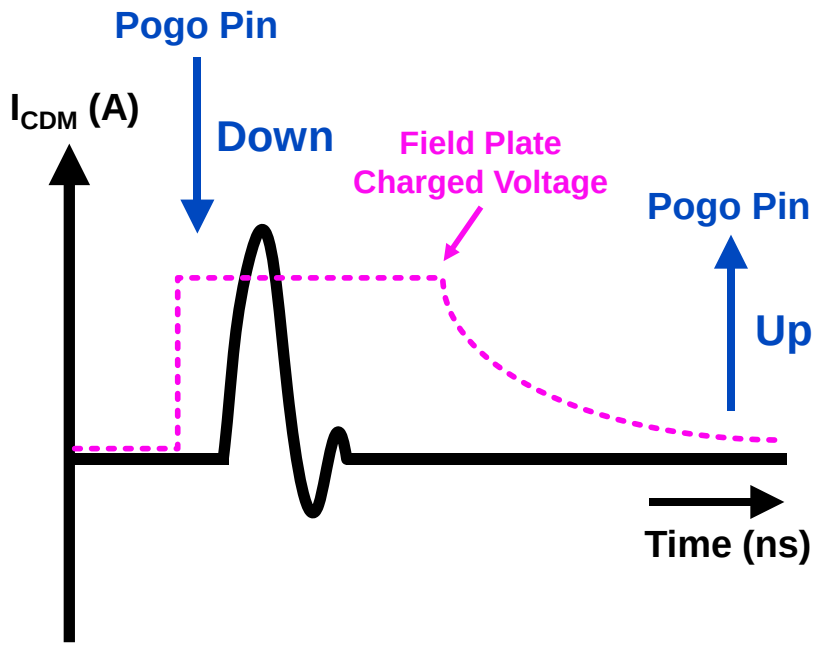
This subsection introduces the two types of discharge procedures used in field-induced CDM test equipment. Both positive and negative stresses can be done together or separately under single field plate charging. First, a detailed description of the single discharge procedure will be mentioned, and then followed by the dual discharge procedure. The auxiliary diagram of the discharge procedures will be shown in Fig. 3.5. Initially, the HV supply is set to zero volts. For a more realistic expression, a packaged chip with lots of cross-domain test circuits is taken as the DUT, and place the uncharged DUT on the field plate. Next, the HV supply is set to a specified stress level, that is, the target level, take +500V for example. The field plate voltage is established by the slow rising rate due to a large charging resistor (~MΩ), ensuring the DUT not to be suffered from unexpected CDM damage before stresses.

The positive charges on the field plate will induce negative charges through the capacitor C_{DF}, and be adsorbed on the bottom of the DUT along the direction of the electric field. Since the DUT is floating and keeps in electrical neutrality, the same amount of positive charge will be repelled by the electric field and far away from the field plate. The induction potential of the DUT will follow the field plate voltage according to equation (3.2). As the pogo pin downs and finally touches the pad or pin of the IC, it can be regarded as a very rapid grounding of the DUT (Fig. 3.5). The charge will be transferred toward the ground through the lowest resistance path and redistributed among the whole chip. Until the positive charge is completely discharged from the IC, the potential of the DUT becomes zero. At this time, the single discharge procedure and dual discharge procedure need to be discussed separately:

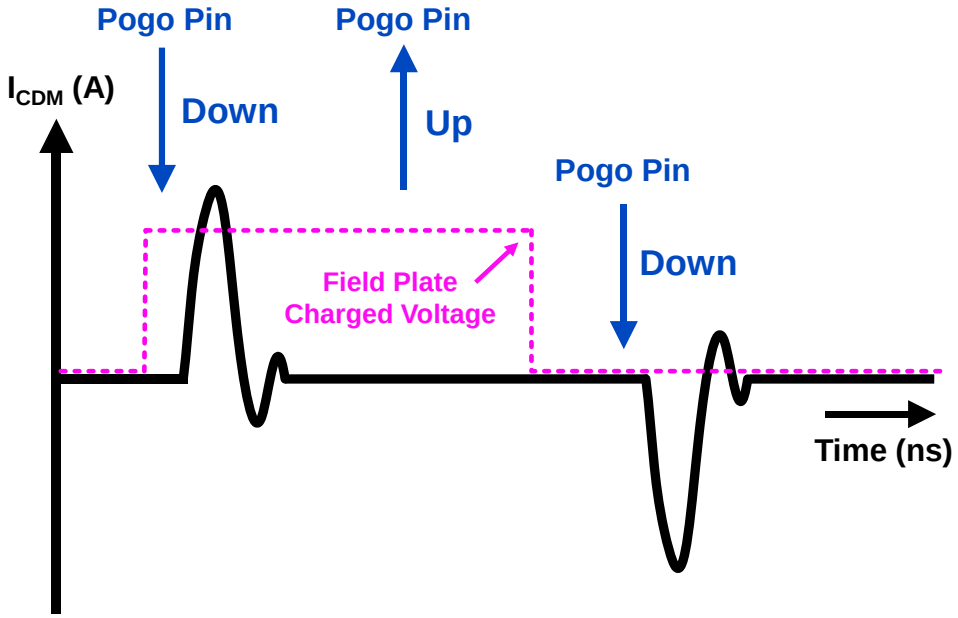
For the single discharge procedure (Fig. 3.5 (a)), keep the pogo pin in contact with the pad or pin of the IC after first discharge, and switch the HV supply to the ground, so that the potential of the field plate will slowly drop through the charging resistor. Further,

the negative charge remaining in the IC will slowly leak to the ground. After the magnetic field plate reaches zero potential, the DUT returns to electrical neutrality, and the pogo pin is raised and moved to the initial position. In the end, the single discharge procedure is finished, and this procedure can be repeated for each pin to be tested.

For the dual discharge procedure (Fig. 3.5 (b)), the pogo pin is raised after the first discharge, so that the DUT is floating as a charged device state. Then switch the HV supply to the ground, the potential of the field plate drops slowly through the charging resistor, and the negative charge remaining in the IC has no release path so that the potential across the C_{DF} is maintained at -500V. Now, push the separated pogo pin down to contact the pad or pin of the IC, and the negative charge starts to discharge from the DUT. Finally, the pogo pin will be removed from the IC again and finished the dual discharge procedure. Note that, the second stress pulse has roughly the same amplitude but opposite polarity as the first one.



(a)



(b)

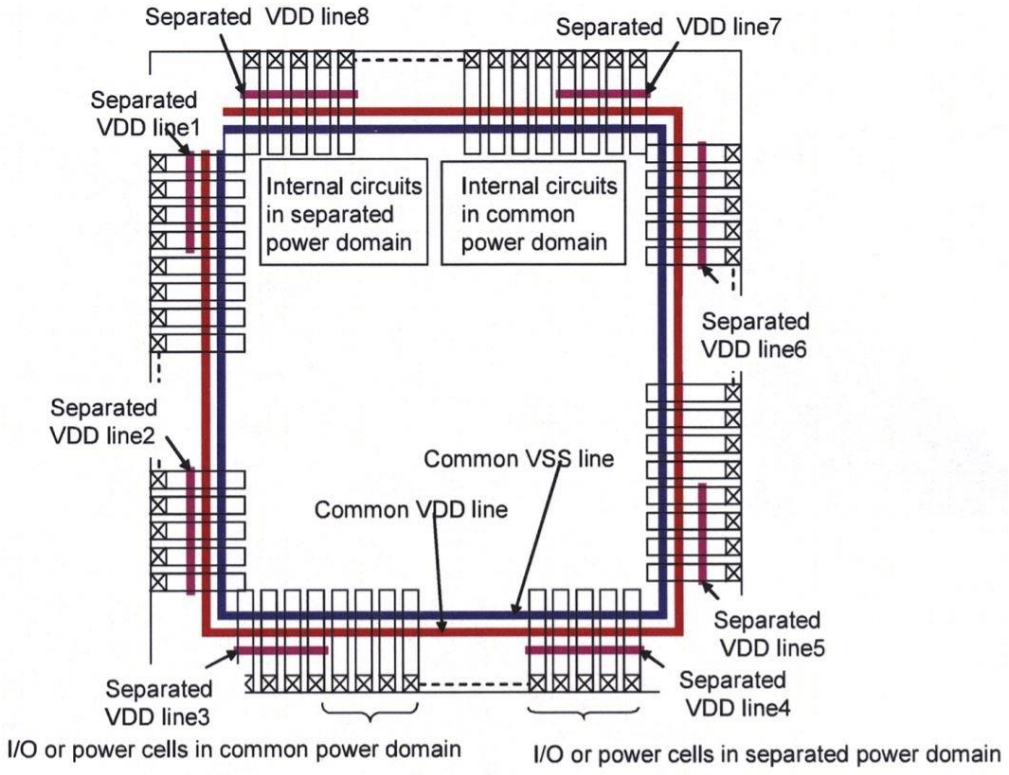
Fig. 3.5. The discharge procedures of (a) single stress and (b) dual stress used in field-induced CDM test equipment.

3.1.3 CDM Test Chip Design and Implementation

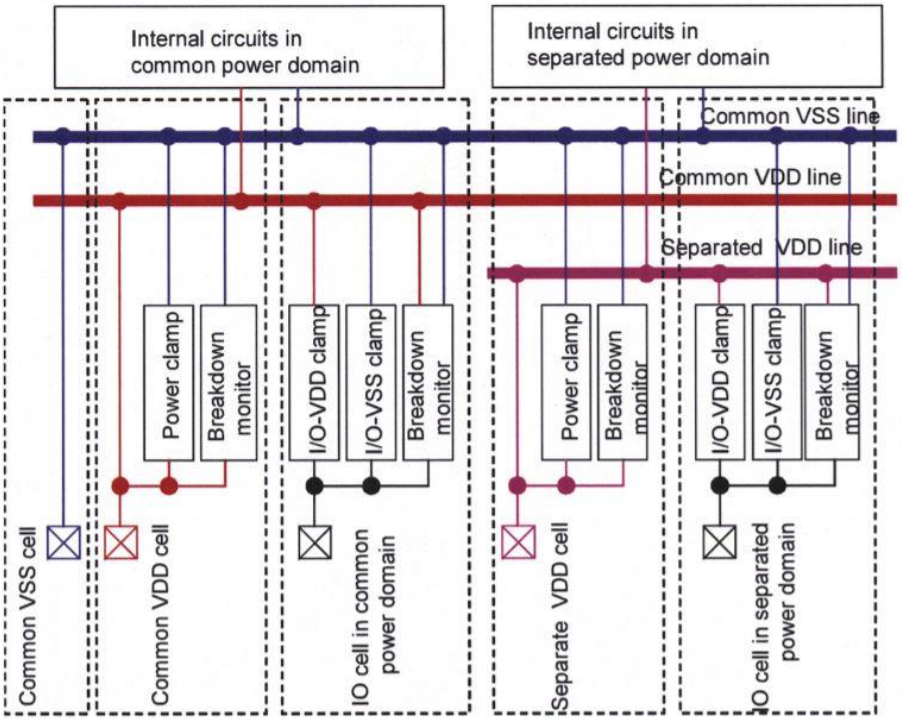
A design to achieve high CDM ESD robustness has become crucial with the progress of technology nodes. Voltage overshoot, which causes a failure of the protected oxide, is observed by Very Fast Transmission Line Pulse (VF-TLP) measurements. Therefore, the power-rail ESD clamp technique between low voltage power and ground rails is important for achieving high CDM robustness. Especially, the separated power domains are difficult to protect because of the small parasitic capacitance between the power and ground rails, which results in a large voltage overshoot. Thus, a design concept of a CDM test chip will be introduced.

The conventional ESD test chip is not suitable for the CDM ESD test. As known, CDM withstands voltage depends on the rise time, duration, and peak current of discharge waveform. Fig. 3.6 shows a floor plan illustration and a circuit diagram of a proposed CDM test chip [25], which can be evaluated by the FI-CDM ESD test. Besides

common power and ground rails, lots of IO ESD protection devices and breakdown monitors are also laid out and configured in between. Note that, internal circuits in common or separate power domain can also be configured with test-keys inside, and then connected to specific power and ground rails through metal wires, which makes the evaluation more accurate. The test chips will be assembled in a package as a product IC. In general, the CDM charges are stored at the power and ground rings, routings in package substrate, bonding wires, and common p-substrate. As a result, low impedance paths from conductor nodes inside the package to external pads are established. By the way, another literature had successfully implemented a more complete CDM test chip and be used to verify some domain-crossing test circuits [26].



(a)



(b)

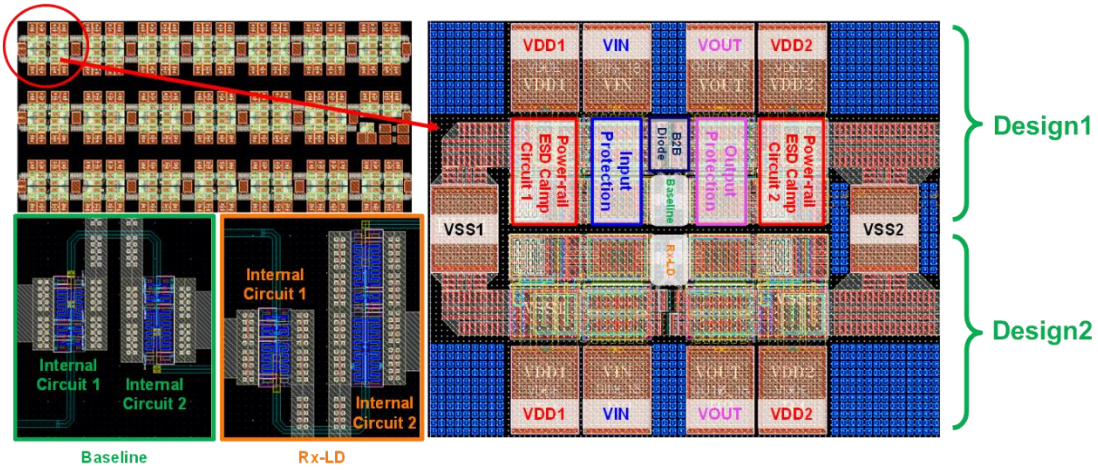
Fig. 3.6. A floor plan illustration and circuit diagrams of a proposed CDM test chip, which can be evaluated by the FI-CDM ESD test [25].

The reference design and the new proposed designs with different structures embedded in the domain-crossing circuits have been fabricated in the TSMC 0.18-μm 1.8-V CMOS process. The CDM test chip layout top view and optical microscope (OM) micrograph of all cross-domain test circuits are shown in Fig. 3.7.

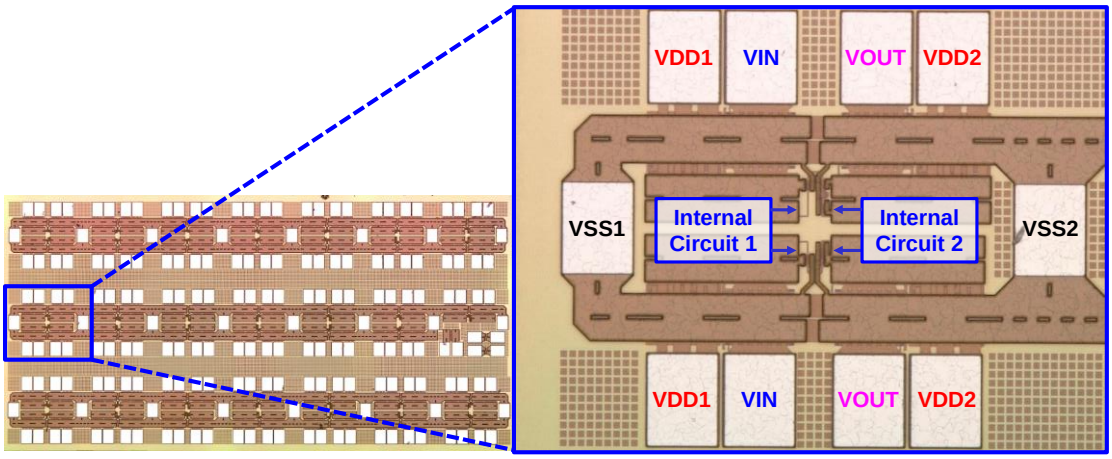
The zoomed-in illustration of the CDM test chip layout top view is shown in Fig. 3.7 (a). Based on the design concepts mentioned earlier, in this experiment, cross-domain test circuits of all designs are on the same silicon chip/IC and assembled in a Side-Braze 48-pins (SB-48) ceramic package for CDM ESD test. For each test circuit, the input/output protection was embedded in the I/O pad, and the power-rail ESD clamp circuit was embedded in the VDD pad. In this experiment, the I/O pads and VDD pads were abutted together, and the I/O pad is kept the same distance from the internal circuit

(test-key). The ground rails of the same power domain, such as VSS1 and VSS2, were connected to a common ground pad to save the layout area. Each pad is connected by bonding wires to the outside for measurement. Because these test circuits are quite symmetrical, consistent, and not far from each other in layout, the deviation of the CDM ESD test may be ignored.

Additionally, the internal circuit also adopts a similar concept to implement between the separated power rails. Note that, the metal routing of the power path should be as symmetrical as possible, and followed current density and antenna rules to successfully established the whole circuit ESD protection for each test circuit. Despite existing potential dual ESD paths in each pair of test circuits, however, it will not affect the comparison of experimental results because the layout was symmetrical and consistent.



(a)



(b)

Fig. 3.7. The CDM test chip (a) layout top view and (b) OM micrograph of all cross-domain test circuits.

3.2 Verification Methods and Failure Criterion

The CDM test chip has been assembled in the Ceramic side-braze 48 pins (SB-48) package with bonding wires as shown in Fig. 3.8, which is widely used for many IC products. The package body size is 1.5-cm*6.1-cm and has 48 lead frames, where pin pitch is 0.25-cm. In the back-end of this chapter, all measurements use the same package form to ensure the consistency of experimental results.

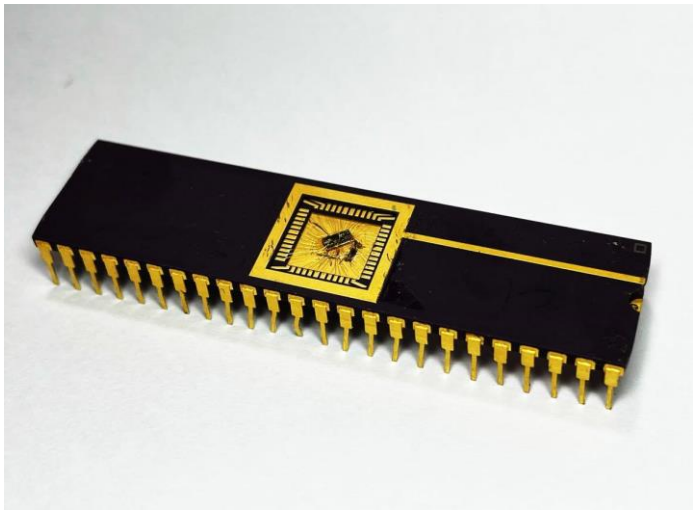


Fig. 3.8. The CDM test chip has been assembled in a Ceramic side-braze 48 pins (SB-48) package with the interconnection of bonding wires.

3.2.1 Measurement Instruments

Agilent B2902A Precision Source/Measure Unit, as shown in Fig. 3.9, dual-channel are connected to VDD/VSS of each power domain to force 1.8V as a power source during functional verification. And the single-channel is connected to any VDD/VSS to sweep the DC I-V curve from 0V ~ 1.8V for each cross-domain test circuit. The B2902A is also used to record transient current, and then calculate leakage/dynamic power.

Keysight 33210A 10MHz Function/Arbitrary Waveform Generator, as shown in Fig. 3.10, is used to provide a 1MHz periodical pulse as the input signal. For signal integrity, the output load could be set as a high impedance (High-Z).

Tektronix MDO3054 Mixed Domain Oscilloscope, as shown in Fig. 3.11, is used to catch output waveform which should be an inverted signal to the input. Other applications like measuring ac parameters, such as rise time, fall time, duty cycle, propagation delay time, and overshoot, etc.

HANWA HED-T5000 TLP Test System and Thermo Scientific Celestron TLP/VF-TLP Test System, as shown in Fig. 3.12 and Fig. 3.13, respectively. Both of them are used to measure secondary breakdown current (I_{t2}), trigger voltage (V_{t1}), and snapback holding voltage (V_h) of ESD protection devices or circuits while monitoring standby leakage and stopping until the current increases significantly. The detailed description is as follows. The TLP system and the device under test (DUT) are grounded together. The HV Generator charges the transmission line and then switches to the DUT to generate a current pulse to stress the DUT, while the energy of the current pulse is continuously increased step by step. At the same time, use the internal DC meter to monitor the voltage and current waveforms of the DUT, after each energy injects the DUT. After a couple of zaps, plot the TLP I-V Curve, until the leakage current of DUT is significantly increased (reaching the current limit), the test is stopped and decide the I_{t2}.

HANWA Compact ESD Tester (HEC-5000), as shown in Fig. 3.14, is a stand-alone ESD test system, which is used to perform HBM, MM, and leakage measurement without a PC or curve tracer. In this experiment, the HEC-5000 was also used to perform cross-domain HBM ESD tests. Note that, HEC-5000 was a simple HBM tester, and lacks the function of calibrating the current waveform under a specified target level.

Fig. 3.9. Agilent B2902A Precision Source/Measure Unit.

Fig. 3.10. Keysight 33210A 10MHz Function/Arbitrary Waveform Generator.

Fig. 3.11. Tektronix MDO3054 Mixed Domain Oscilloscope.

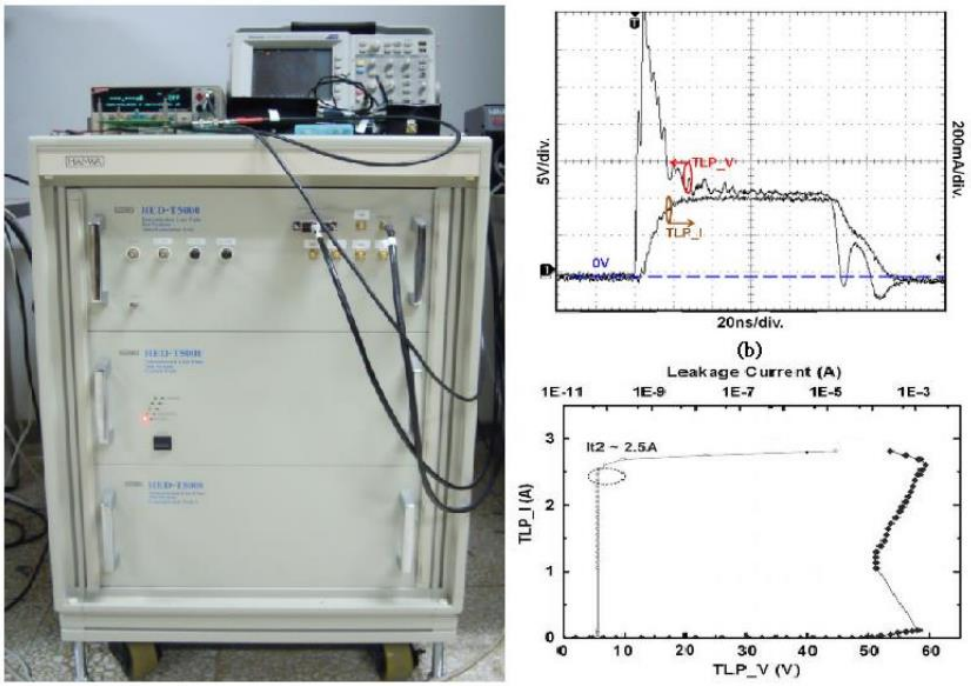


Fig. 3.12. HANWA HED-T5000 TLP Test System.

Fig. 3.13. Thermo Scientific Celestron TLP/VF-TLP Test System

Fig. 3.14. HANWA Compact ESD Tester (HEC-5000)

3.2.2 Electrical Verification

Since the ESD discharge mechanism of CDM and HBM are quite different, causing internal damage is quite complicated. The electrical verification will be through the I-V characteristic of all combinations between any two VDD/VSS pins. Preliminarily observe the leakage of various paths, and trace the components that may be damaged in the interface circuit, which is helpful for failure analysis (FA), subsequently.

For electrical verification, the failure criterion is defined as the leakage current under 1.8 V bias increases over 10 times of magnitude from its original leakage current, or the I-V characteristics shifting more than 30% (sweep from 0V to 1.8V) from its initial curve after each ESD stress level. Each of the DC I-V curves was measured by B2902A Precision Source/Measure Unit (PSMU), respectively.

In a couple of test pin combinations, the two most representative I-V characteristics are VDD1-to-VSS2 and VDD2-to-VSS1, which reflects the damage of the interface circuit. As shown in Fig. 3.15, take the Baseline (reference design) as an example. If the DC I-V characteristic of VDD1-to-VSS2 drifts severely, the probability of damage to M_{pT} or M_{nR} is very high. Additionally, properly switching the I/P pad shunt to anode or cathode to switch the on/off state of M_{pT} can accurately find the damaged component. In contrast, if the I-V characteristic of VDD2-to-VSS1 drifts severely, the damaged device might be M_{pR} since the serious gate-oxide transient overvoltage. The remaining test combinations, including input and output pads, are used to confirm whether unexpected damage occurs outside the interface circuit.

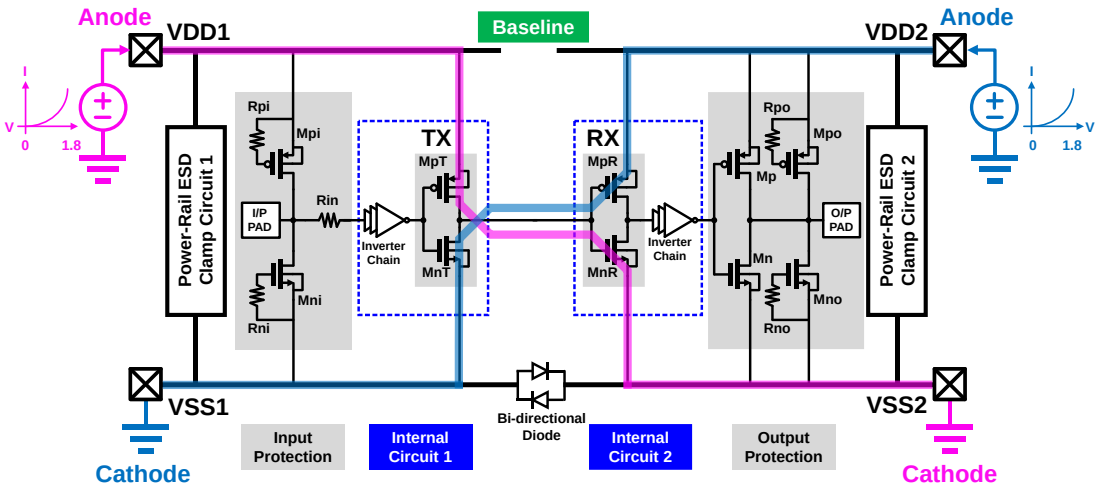


Fig. 3.15. The measurement set-up of electrical verification and illustrations of the two most representative I-V characteristics: VDD1-to-VSS2 and VDD2-to-VSS1.

For example, the traced VDD1-to-VSS2 DC I-V characteristics of the reference design before and after CDM ESD stress are shown in Fig. 3.16. After positive CDM 200V and 300V performed on VDD1, the DC I-V characteristics between VDD1 and VSS2 shifted obviously, and the leakage current increased significantly by more than 10 times under 1.8V bias. The phenomenon reflects the possibility of Rx-NMOS damage.

On the contrary, the traced VDD2-to-VSS1 DC I-V characteristics of the reference design before and after CDM ESD stress are shown in Fig. 3.17. After negative CDM 200V and 300V performed on VDD2, the DC I-V characteristics between VDD2 and VSS1 shifted obviously, and the leakage current increased significantly by more than 10 times under 1.8V bias. The phenomenon reflects the possibility of Rx-PMOS damage.

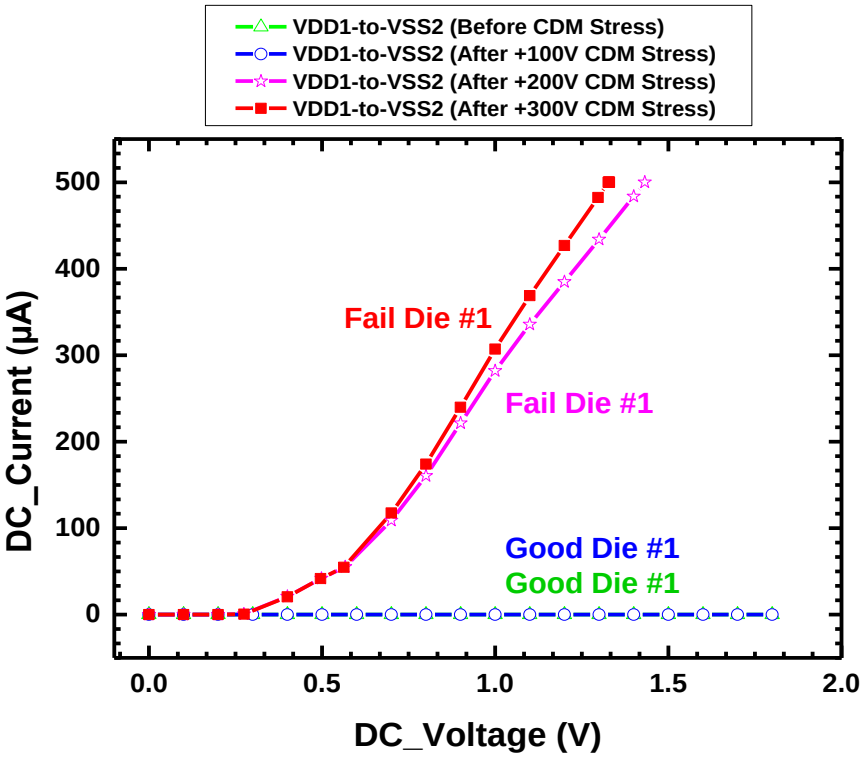


Fig. 3.16. The traced VDD1-to-VSS2 DC I-V characteristics of the reference design before and after CDM ESD performed on VDD1. (grounded VDD1)

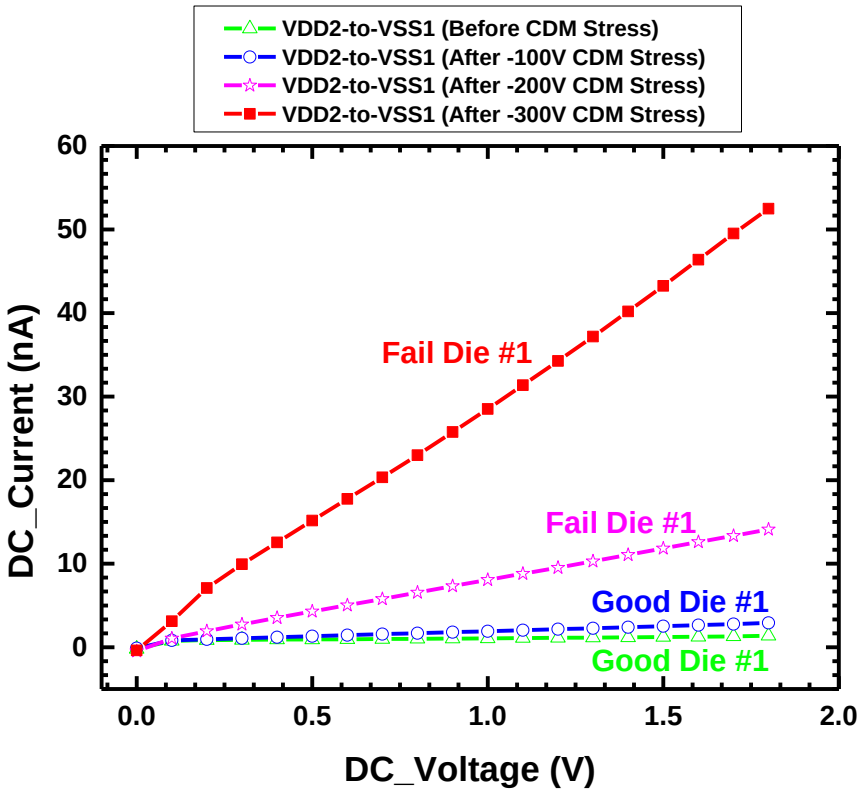


Fig. 3.17. The traced VDD2-to-VSS1 DC I-V characteristics of the reference design before and after CDM ESD performed on VDD2. (grounded VDD2)

3.2.3 Functional Verification

With an odd number of inverter stages, the cross-domain test circuit is used to invert the input signal. To confirm the circuit function, the cross-domain test circuits with multiple designs were verified by observing the output signal integrity. The measurement set-up of functional verification is illustrated in Fig. 3.18, the B2902A PSMU is used to separately force the VDD1 and VDD2 at 1.8 V, while the VSS1 and VSS2 are both separately grounded. The 33210A Waveform/Function Generator is connected to the input terminal, generating a 1MHz periodic square waveform as the clock signal for ensuring the output signal integrity. The input and the output waveform are captured by the MDO3054 Mixed-Domain Oscilloscope.

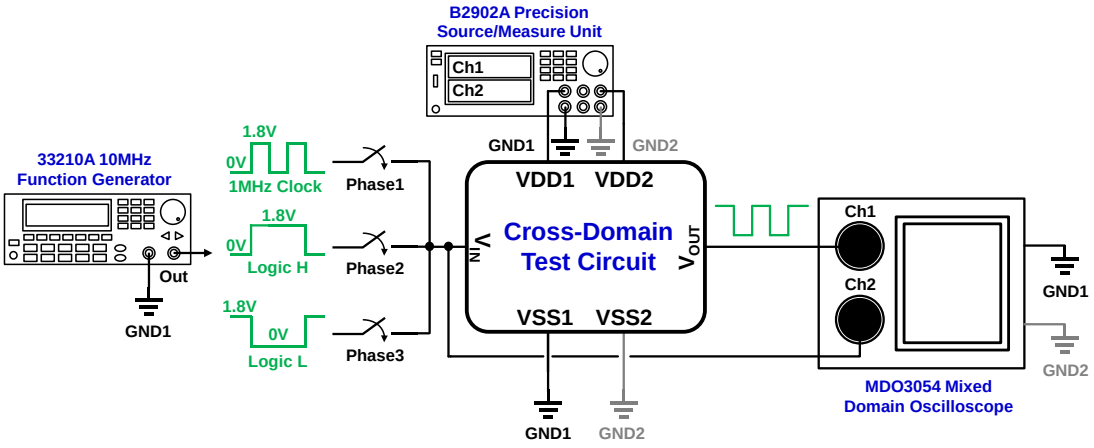


Fig. 3.18. The measurement set-up of functional verification.

For example, the measurement results of the reference design before and after positive CDM ESD stress is shown in Fig. 3.19, respectively. The output impedance of the 33210A set as high impedance can achieve perfect impedance matching at the V_{IN}. The 50-ohm internal resistance of the oscilloscope can not terminate the reflected signal, that is, signal overshoot and undershoot occur at the output terminal due to impedance mismatch. After positive CDM 200V and 300V were performed on VDD1, the measured output signal waveforms show distortions and degradations since the interface circuits were damaged under cross-domain ESD stresses. Moreover, while the function is

abnormal, the driving current increases significantly, especially in the VDD2/VSS2 domain, which means that the Rx module may have gate-oxide damages. As a result, the defects cause the logic level of the interface near to the logic threshold, which is half of VDD, making each stage of driving circuits contributes a huge short circuit current during signal transition periods. The damage of the interface circuit can be traced from the abnormal waveform. This approach becomes another verification mechanism, and the result usually matches the electrical verification.

The definition of soft failure: after cross-domain ESD stresses, the current on VDD1 or VDD2 varies significantly, but no apparent distortions were observed from the output signal. The definition of hard failure: after cross-domain ESD stresses, the current on VDD1 or VDD2 varies significantly, and apparent distortions were observed from the output signal as well.

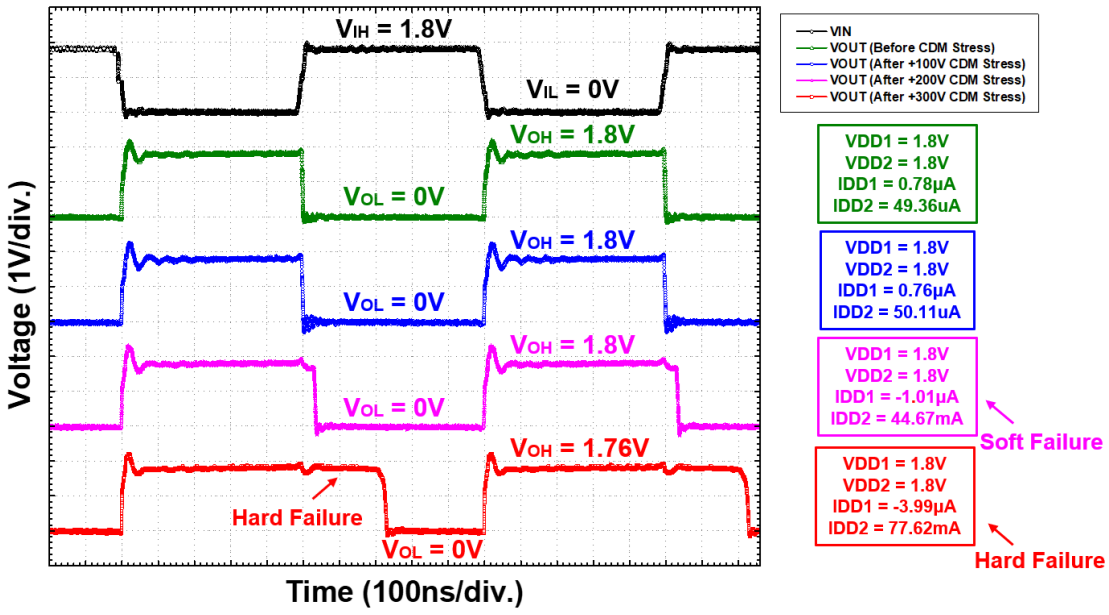


Fig. 3.19. The functional verification results of the reference design before and after positive CDM ESD stresses were performed on VDD1. (grounded VDD1)

On the contrary, the measurement results of the reference design before and after negative CDM ESD stress is shown in Fig. 3.20, respectively. After negative CDM zaps were performed on VDD2, the measured waveforms show a little bit undetectable anomalies even the interface circuits were already damaged under cross-domain ESD stresses. Moreover, the driving current nearly unchanged on both channels, that is, difficult to speculate the locations of gate-oxide damage. As a result, by confirming the electrical and functional verification mechanisms, unless the leakage rise is obvious, the circuit function will not occur errors but may be accompanied by larger current consumption. The main reason is that because the dimension and driving strength of the Tx module was huge enough to drive the Rx module in a logic high/low state, even if the Rx module was damaged, it will not cause serious errors in the function.

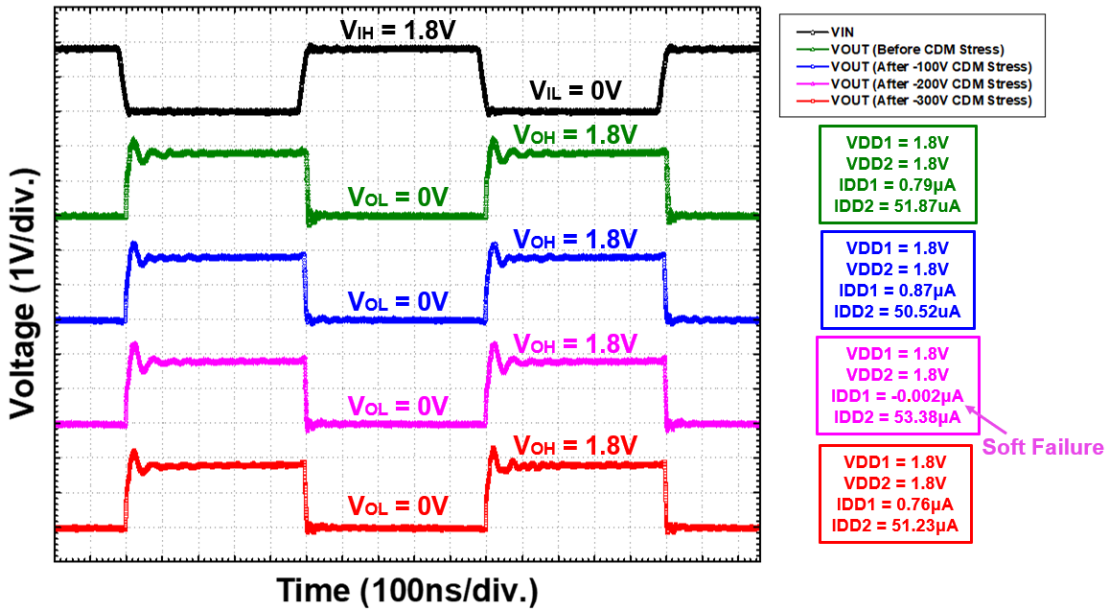


Fig. 3.20. The functional verification results of the reference design before and after negative CDM ESD stresses were performed on VDD2. (grounded VDD2)

3.2.4 Failure Criterion

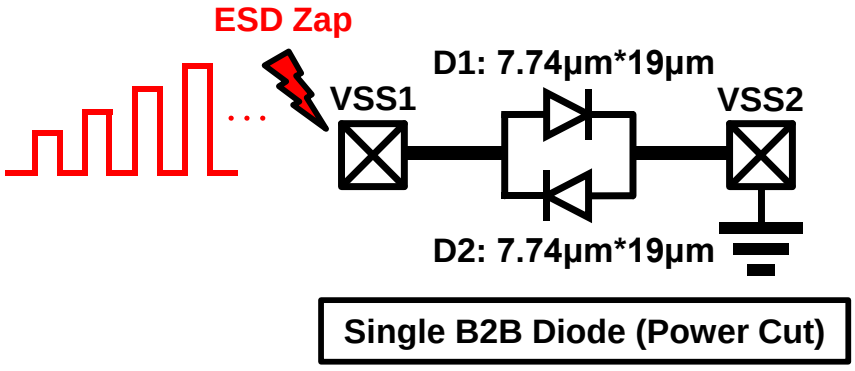
After ESD tests, the failure criterion depends on electrical verification and functional verification to judge the specific I/O pin of the device under test (DUT) is passed or failed. In most cases, the magnitude of leakage must be inspected first. Additionally, three types of verification are also helpful to detect failures: increased input leakage, stuck at one or zero faults, and reduced maximum frequency [26]. By the verification results, comparisons of the ESD robustness under different architectures are provided as follows.

3.3 ESD Measurement Results

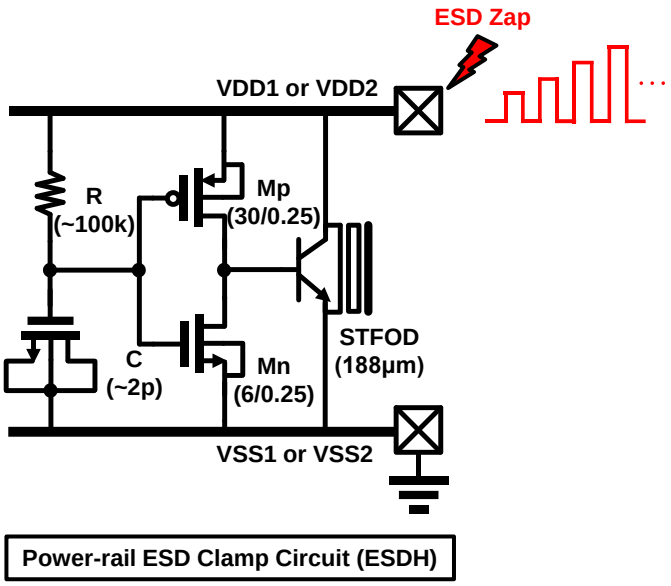
3.3.1 ESD Protection Circuits Characterization

Before measuring the ESD characteristics of the cross-domain test circuit, characterizing the ESD protection cells, which are called from the I/O library, is necessary, which helps to evaluate the maximum ESD energy that the main dissipation path can withstand. To avoid destroying the ESD protection cells during the cross-domain ESD test which may cause the possibility of misjudgment. Therefore, the first task is to characterize the ESD level of each protection cell.

As shown in Fig. 3.21, the ESD measurement methods of the bi-directional diodes pair (Power Cut) and the power-rail ESD clamp circuit (ESDH) are illustrated. For Power Cut, the characteristics of the bi-directional structure can be tested by selecting one pad as the anode and the other pad as the cathode. For ESDH, choosing the VDD rail as the anode and the VSS rail as the cathode will be a worse case than the opposite direction, since the clamp voltage will be increased by R_{on} of STFOD and ESD current, which contribute a lot of power heating. Eventually, the ESD device will exceed the physical limit and form irreversible damage.



(a)



(b)

Fig. 3.21. The illustrations of ESD measurement methods of the Power Cut and ESDH.

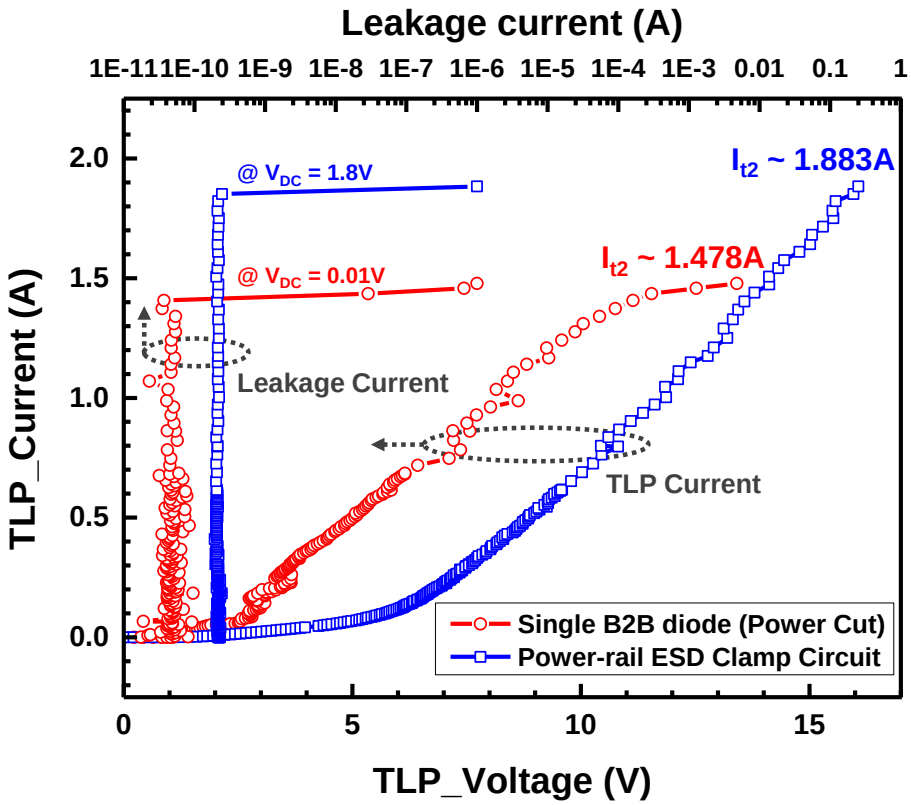
The measurement results of transmission line pulse (TLP) and very fast-transmission line pulse (VF-TLP) are shown in Fig. 3.22. Note that, the leakage monitoring of Power Cut is under 0.01V dc bias to ensure the bi-directional diodes out of the forward active region. The estimation of the second breakdown current (I_{t2}) is the corresponding TLP current value when the leakage current increases significantly.

Observed from the TLP I-V characteristics, the Power Cut has a very low starting voltage (~1V), while the ESDH has a higher starting voltage (~6V). Both of them have similar turn-on resistance. The superposition of the I-V characteristics can be calculated

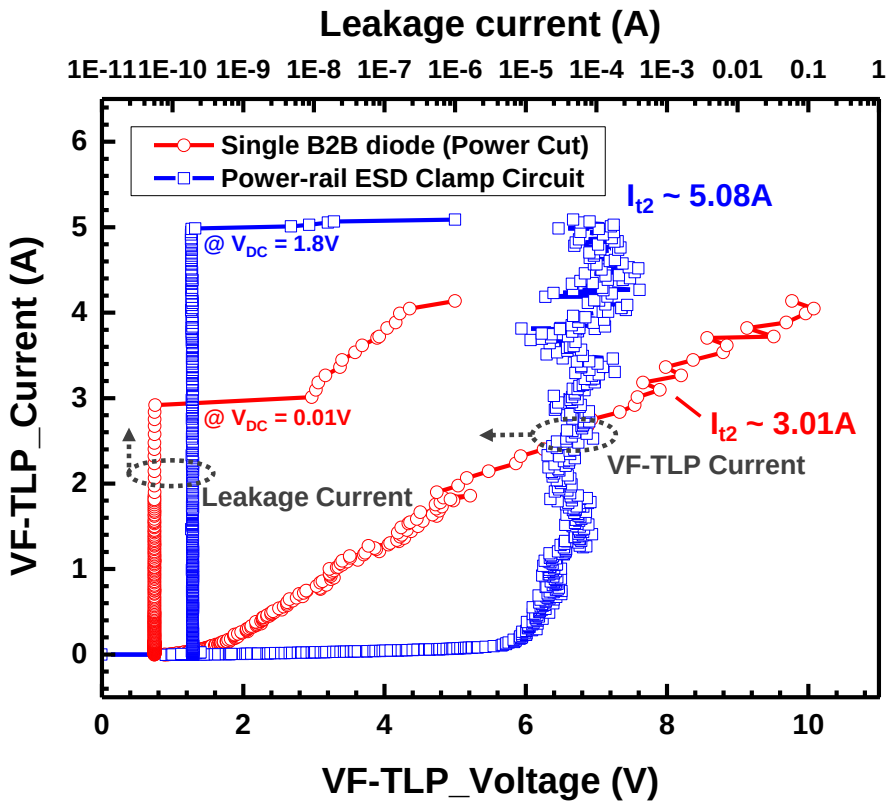
the voltage drop for the long discharge path, and be used to quantitatively evaluate the cross-domain voltage under the HBM ESD test of the interface circuit. Finally, the I_{t2} could be converted to HBM level, which exceeds the 2kV for both.

Compared with TLP I-V from VF-TLP I-V characteristics, the Power Cut has similar conduction behavior and lower conduction resistance. Similarly, the ESDH has a similar starting voltage but smaller turn-on resistance. By means, during the fast transient discharge, both ESD cells have lower IR drop, and the energy duration is very short, the power heating generated becomes smaller, reflecting the higher I_{t2}. However, the VF-TLP I-V characteristic is not suitable for precisely estimate the actual CDM level.

Then, after the HBM ESD test, the DC I-V characteristics are also swept to be judged the actual HBM level when significant DC curve shifting, as shown in Fig. 3.23. As a result, the HBM levels of Power Cut and ESDH are exactly higher than 2kV and better than the results estimated by TLP I-V characteristics.

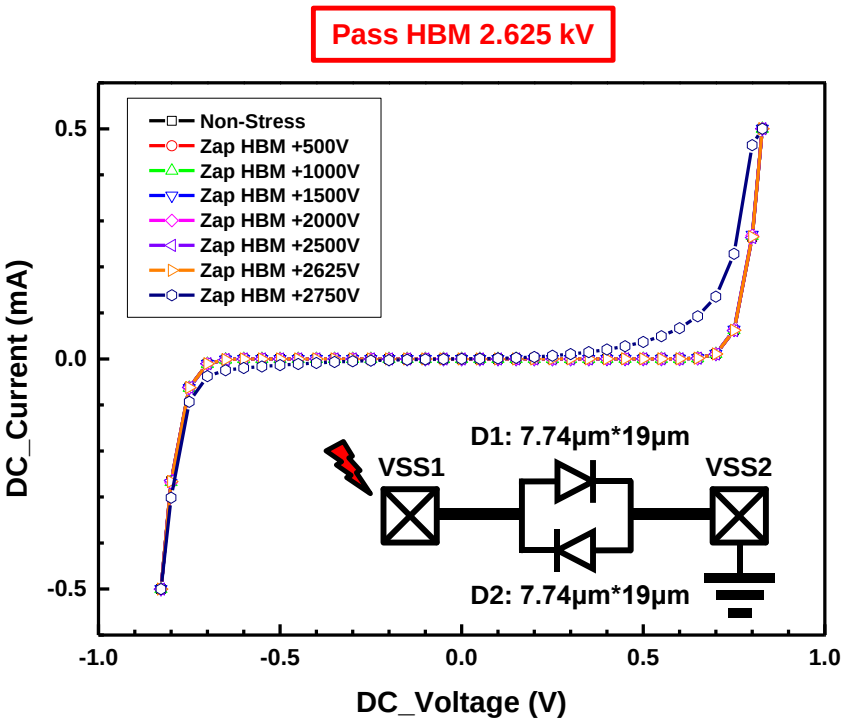


(a)

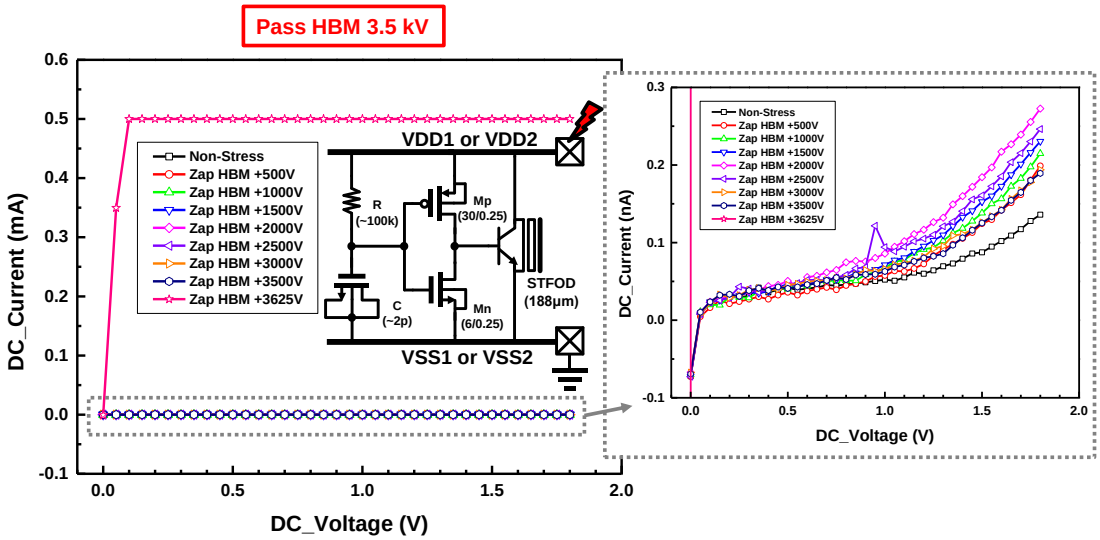


(b)

Fig. 3.22. The TLP and VF-TLP I-V characteristics of the Power Cut and ESDH.



(a)



(b)

Fig. 3.23. After the HBM ESD test, the DC I-V characteristics of Power Cut and ESDH, are swept to be judged the actual HBM level when significant DC curve shifting.

3.3.2 Cross-Domain VF-TLP I-V Characteristics

The I–V characteristics of different protection designs of cross-domain test circuits described in the previous chapter were measured by the very-fast transmission-line-pulse (VF-TLP) system, which generated the current pulses with 5-ns duration time and 0.3-ns rise time to obtain the circuit or device characteristics under cross-domain stresses. The voltage and current waveforms are calibrated by 50-ohm characteristic impedance in the time-domain are shown in Fig. 3.24.

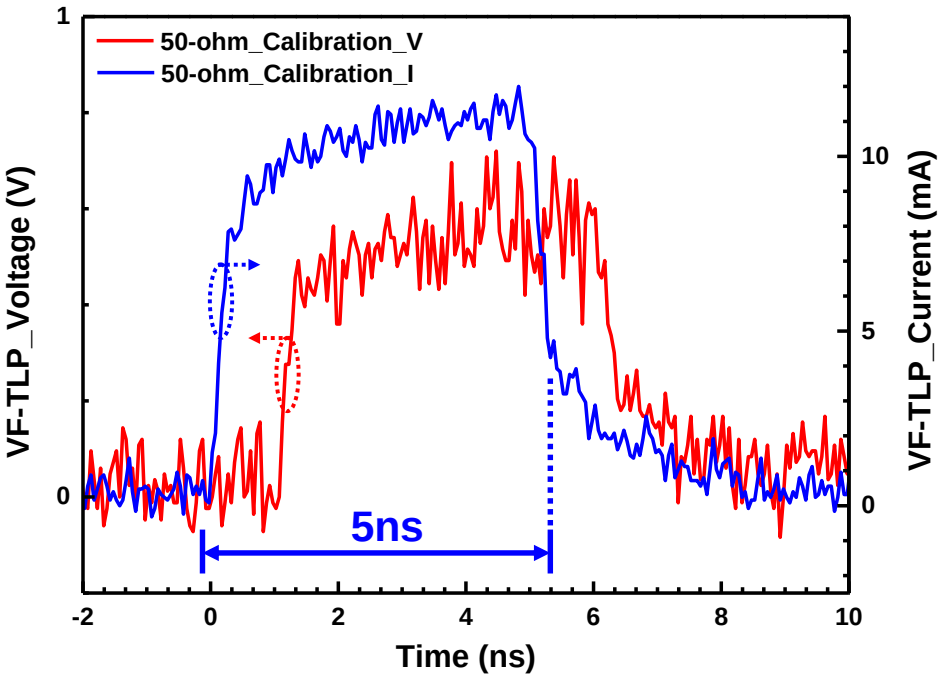
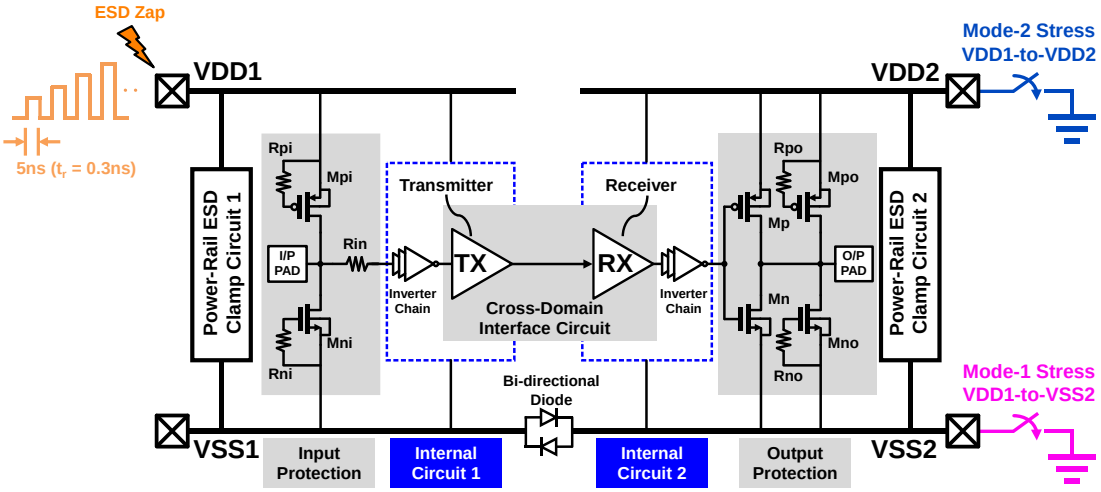
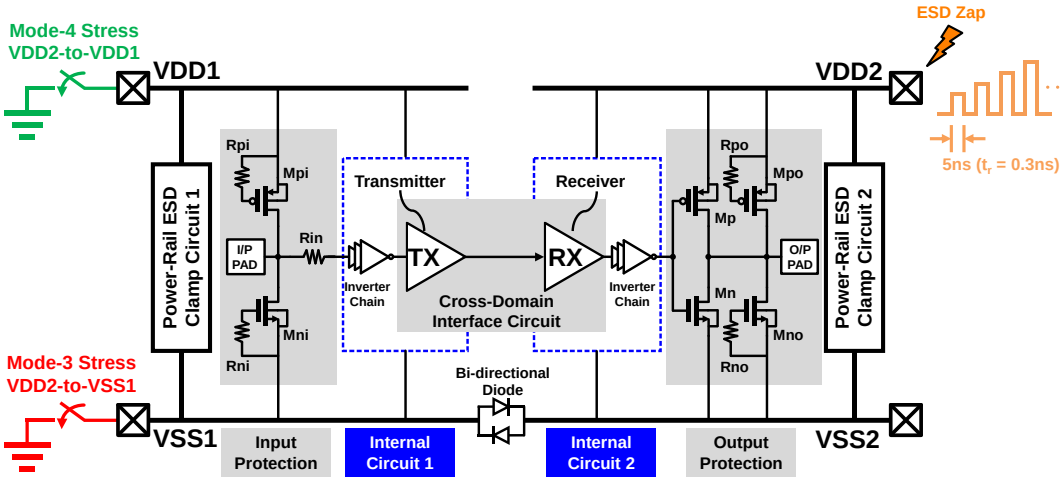


Fig. 3.24. The calibrated voltage and current waveforms by 50-ohm characteristic impedance in the time-domain.

The VDD1-to-VSS2 (Mode-1) stress means that the VF-TLP current pulse was applied at VDD1 with grounded VSS2, and so on. The schematic diagrams of the measurement setup for all test conditions are shown in Fig. 3.25. Moreover, the VF-TLP I–V characteristics of all designs under Mode-1 to Mode-4 stress combinations, were measured and illustrated in Fig. 3.26 ~ Fig. 3.29, respectively, and divided into Rx modification and Tx modification for individual comparison.



(a)



(b)

Fig. 3.25. The schematic diagrams of the measurement setup for (a) Mode-1 and Mode-2 stress and (b) Mode-3 and Mode-4 stress conditions.

Under the VDD1-to-VSS2 (Mode-1) stresses, as shown in Fig. 3.26, all designs presented high second breakdown currents (I_{t2}) and perfect turn-on efficiency. The VF-TLP voltage V_{t2} corresponding to I_{t2} is approximately near the $|BV_{ox}|$. When the main current dissipation path I_{ESD} produces a sufficient voltage drop, it causes gate-oxide damage to the interface circuit, which corresponds to the simulation result. During the discharge, the RC-based power-rail ESD clamp uniformly turns the STFOD on.

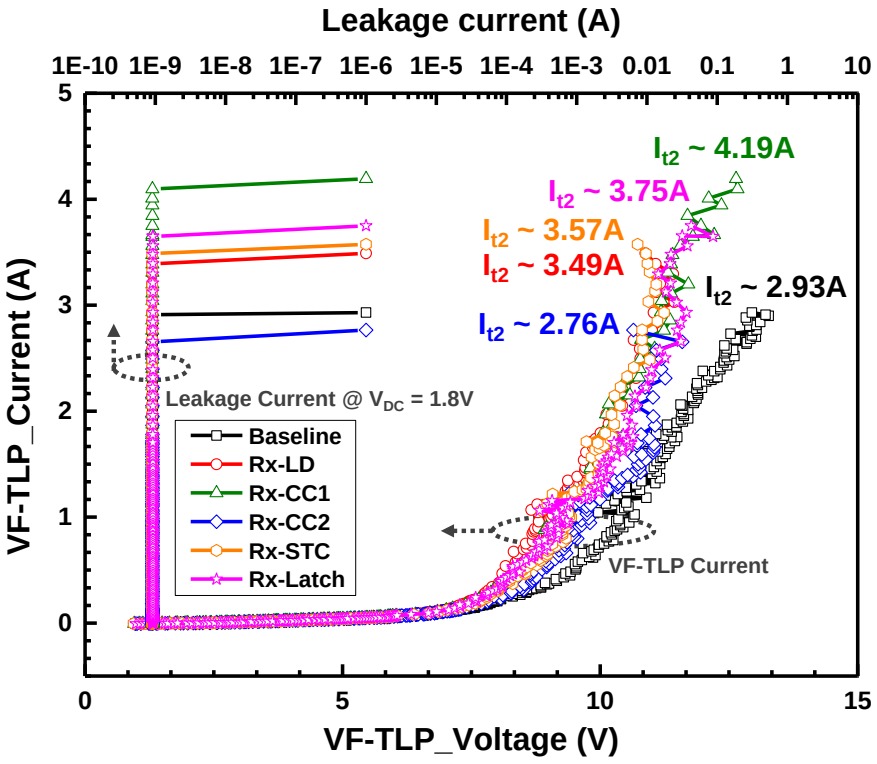
In Fig. 3.26 (a), the Baseline design has the lower I_{t2} and the larger turn-on resistance, which indicates that most designs have better performance. The Rx-LD design with dimension variation shows a larger I_{t2} because the large area can dissipate more electrostatic energy. The Rx-CC1, Rx-STC, and Rx-Latch designs with a stacking structure can enhance the equivalent impedance of the receiver module, and suppress the generation of unexpected current path I_{ESD2} so that most currents can bypass through the I_{ESD} path. Among them, the Rx-CC1 design has the highest I_{t2} value about 4.19 A, which means that the gates are directly connected to VDD2/VSS2 rails can also get well performance, since the header PMOS and footer NMOS will not suffer from gate-oxide transient overstresses. In contrast, the Rx-CC2 design has a lower I_{t2} value than the Baseline design, which means that the header NMOS and footer PMOS are invalid to enhance the equivalent impedance, and the overstresses are still across the gate-oxide of one Rx-NMOS or Rx-PMOS in the Rx module.

In Fig. 3.26 (b), all Tx modification designs are better than the Baseline design but present a clear difference among them. As expected, the Tx-STC and Tx-Latch have the highest I_{t2} value around 7A, which higher than all Rx modification designs, and have the same trend as predictive CDM simulation. Conversely, the Tx-CC1 and Tx-CC2 are relatively poor, since the gates are directly connected to VDD1/VSS1 rails, results in the gate-oxide directly stressed by VF-TLP current injection. By means, try to avoid using cross-coupled interconnections in the Tx module to gain higher ESD robustness.

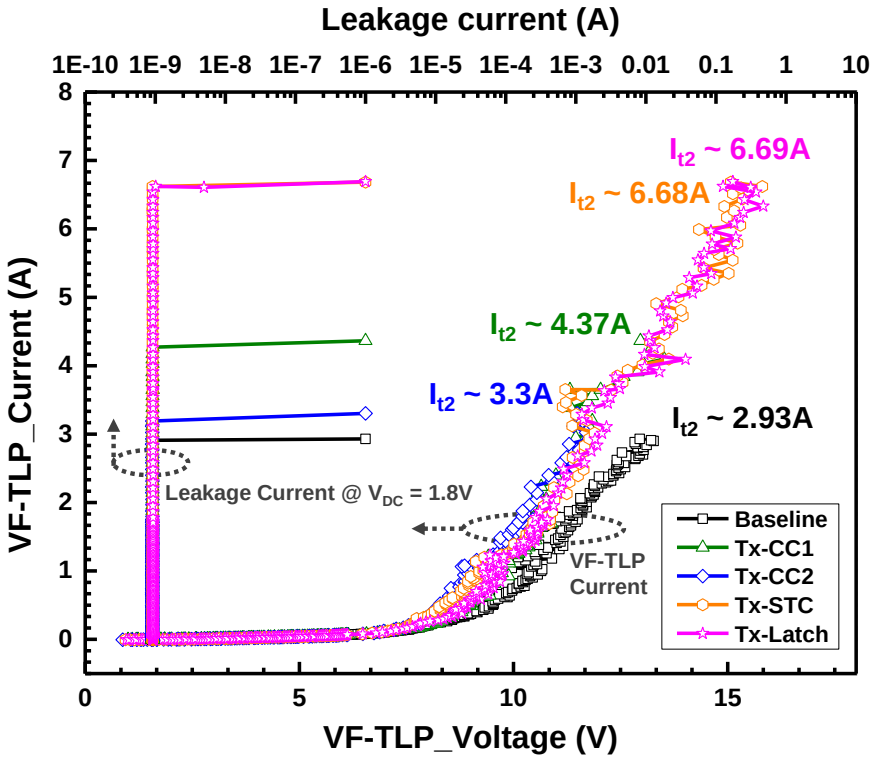
Under the VDD1-to-VDD2 (Mode-2) stresses, as shown in Fig. 3.27, the I_{t2} of all designs presented slightly lower than the Mode-1 stress condition. Mainly due to the longer discharge path, resulting in a larger voltage drop across the ESD path, and causing more serious overvoltage conditions in the interface circuit. The results also confirmed the previous assumptions in chapter 1, and have the same trend but larger R_{on} and trigger voltage (V_{t1}) than the Mode-1 stress condition.

Under the VDD2-to-VSS1 (Mode-3) stresses, as shown in Fig. 3.28, all designs presented lower I_{t2} than the aforementioned stress conditions. Attributable to the parasitic current effect of output protection and complex layout dependent effects under fast transients, and then cause the VDD2 potential rise-up to induce snapback breakdown of the STFOD. The trigger voltage V_{t1} and holding voltage V_h are roughly the same for each design. In the holding region, the non-uniform conduction has a higher R_{on}, resulting in the Rx-PMOS occur gate-oxide breakdown earlier. However, the new proposed designs have a slightly higher I_{t2}, which means that under different directional stress combinations, stacking structures can reduce cross-domain transient overvoltage.

Under the VDD2-to-VDD1 (Mode-4) stresses, as shown in Fig. 3.29, the I_{t2} of all designs presented lower I_{t2} as the Mode-3 stress condition. The snapback breakdown behavior still existed, and have the same trend but larger R_{on} and trigger voltage (V_{t1}) than the Mode-3 stress condition.

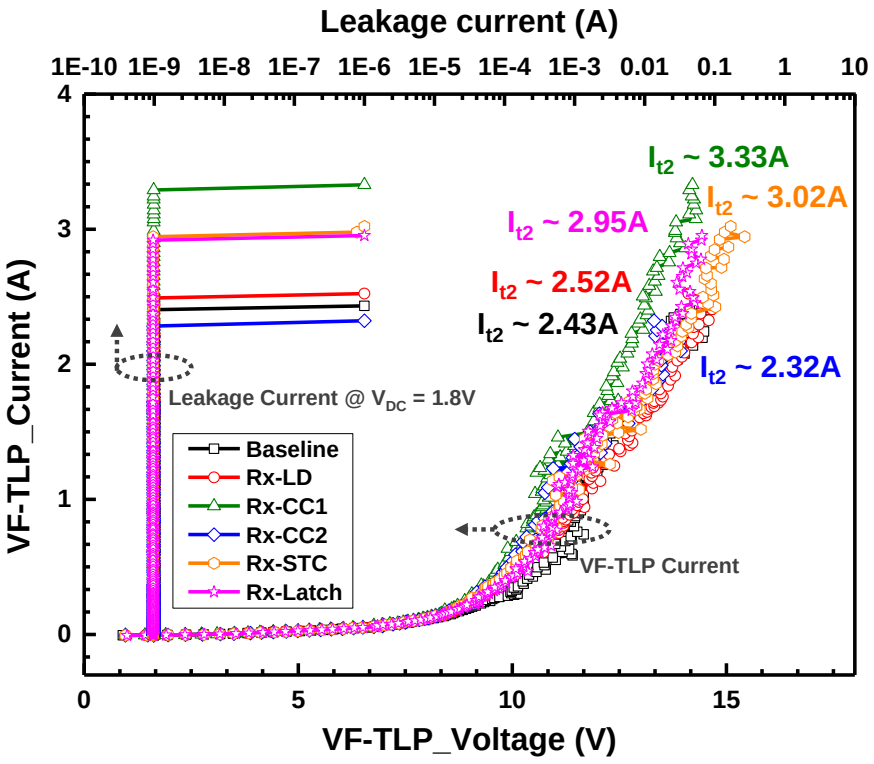


(a)

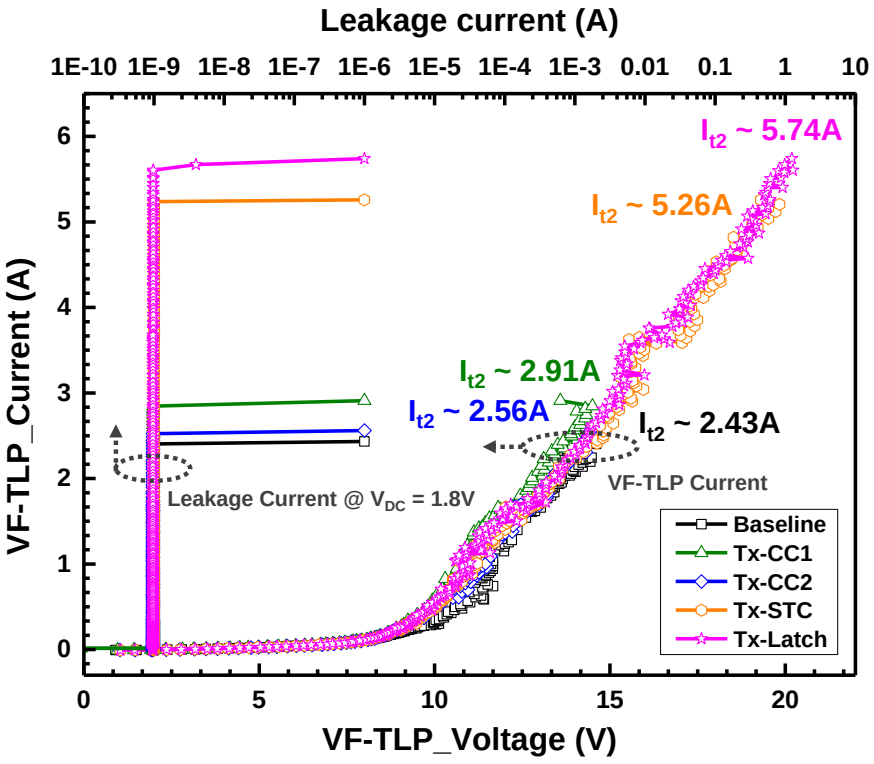


(b)

Fig. 3.26. The cross-domain VF-TLP I–V characteristics of different protection designs embedded in (a) RX and (b) TX under VDD1-to-VSS2 (Mode-1) stress.

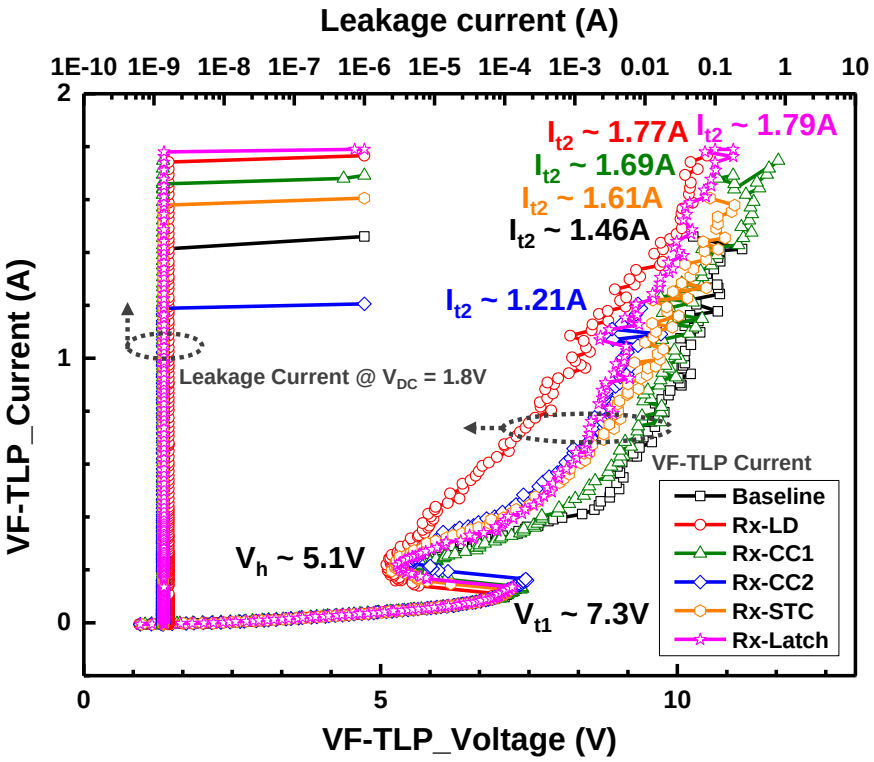


(a)

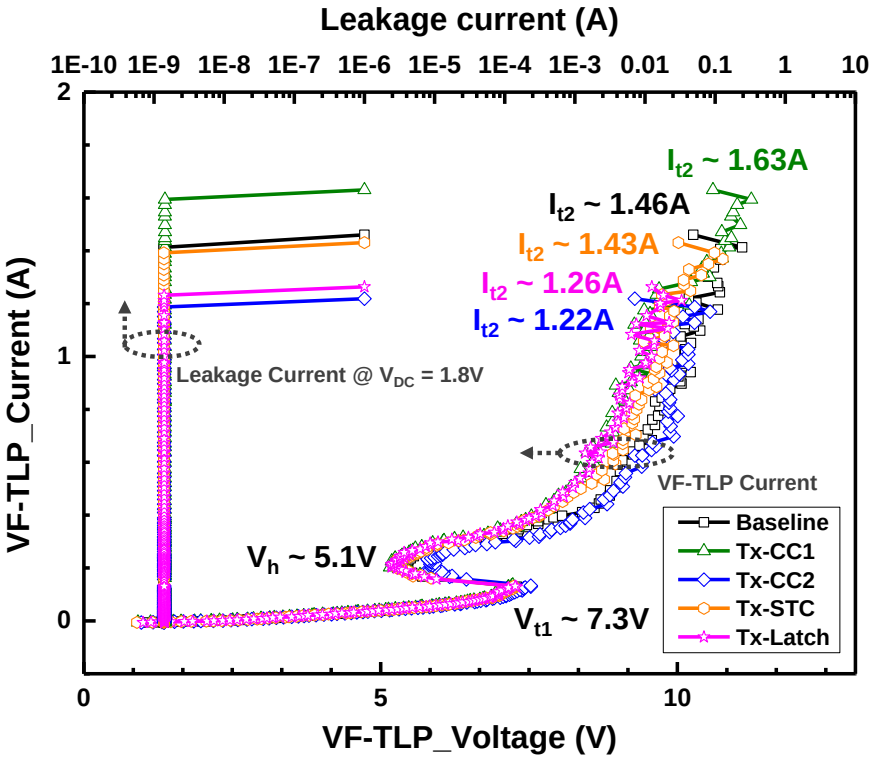


(b)

Fig. 3.27. The cross-domain VF-TLP I–V characteristics of different protection designs embedded in (a) RX and (b) TX under VDD1-to-VDD2 (Mode-2) stress.

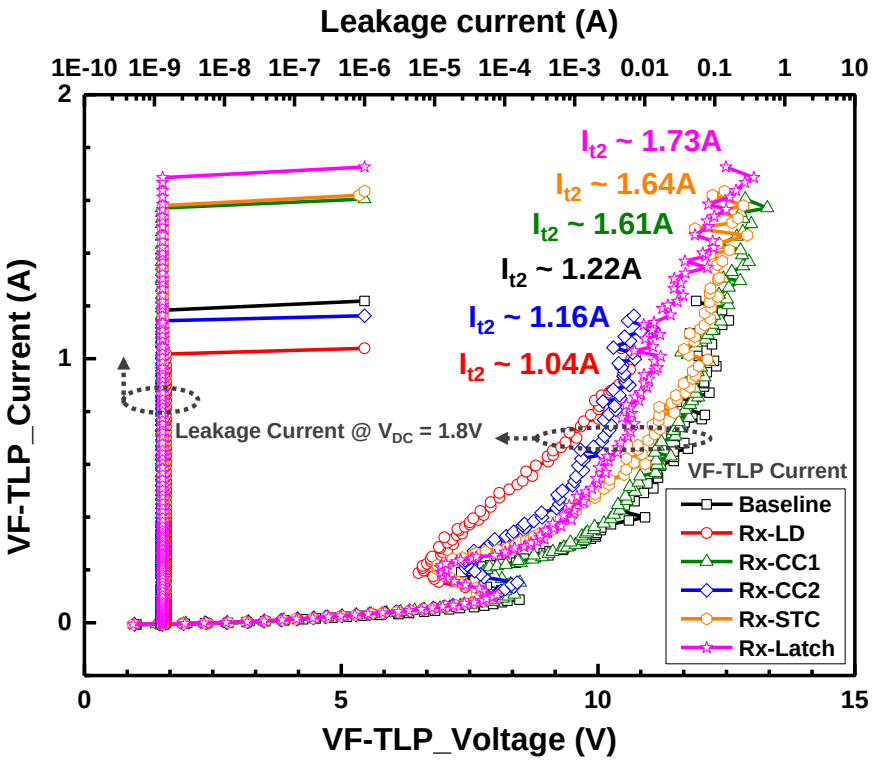


(a)

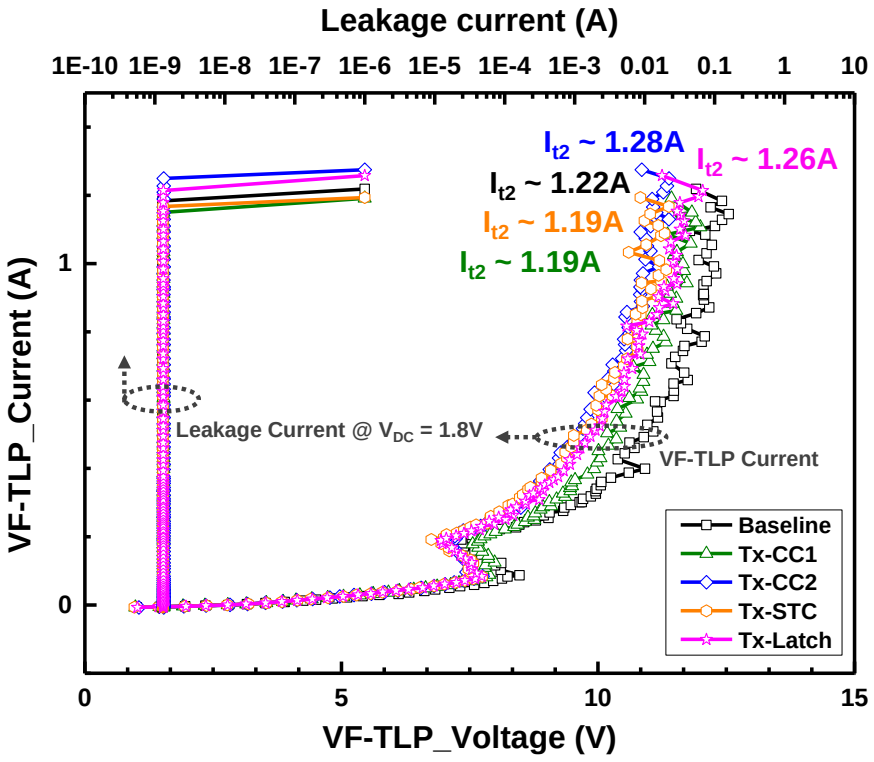


(b)

Fig. 3.28. The cross-domain VF-TLP I–V characteristics of different protection designs embedded in (a) RX and (b) TX under VDD2-to-VSS1 (Mode-3) stress.



(a)



(b)

Fig. 3.29. The cross-domain VF-TLP I–V characteristics of different protection designs embedded in (a) RX and (b) TX under VDD2-to-VDD1 (Mode-4) stress.

The measured cross-domain VF-TLP I_{t2} of all designs are list in Table 3.1. For each mode, the higher It2 is marked in blue, and the lower It2 is marked in red. As a result, the Mode-3 and Mode-4 stresses are much worse and represent poor ESD robustness, due to the power-Rail ESD Clamp Circuit 2 not being designed well for fast transient ESD events.

Table 3.1

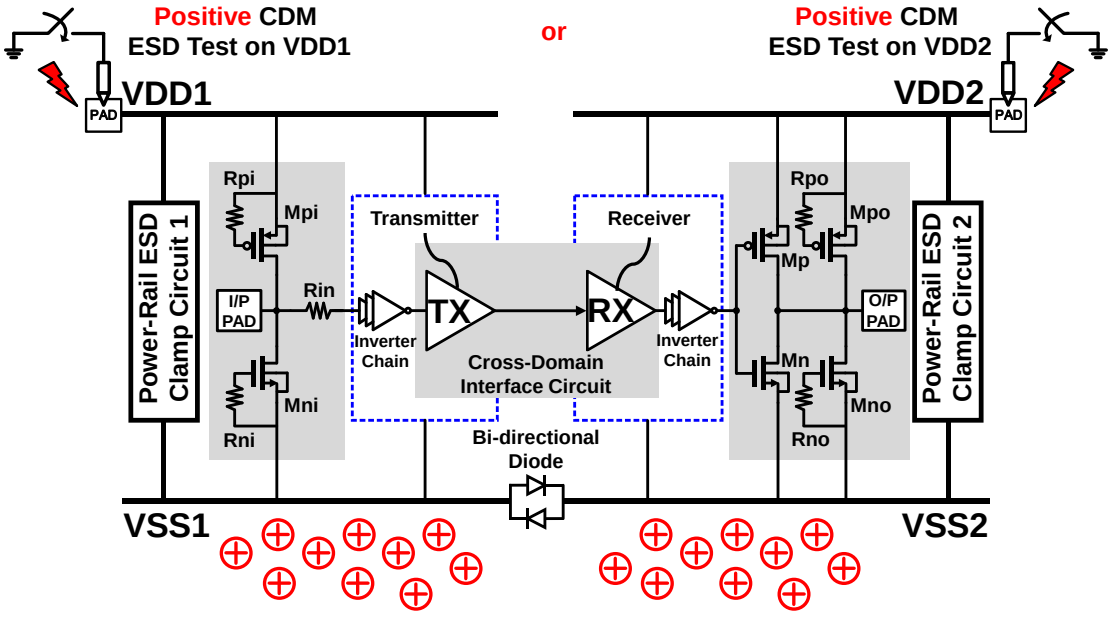
The List of Measured Cross-Domain VF-TLP I_{t2} of All Cross-Domain Test Circuits

Group	Key Factor	Design	VF-TLP I_{t2}(A) [current pulse with 5-ns duration and 0.3-ns rise time]			
			Mode-1 Stress (VDD1-to-VSS2)	Mode-2 Stress (VDD1-to-VDD2)	Mode-3 Stress (VDD2-to-VSS1)	Mode-4 Stress (VDD2-to-VDD1)
Ref. Circuit	General	Baseline	2.93	2.43	1.46	1.22
Test Circuits	Dimension	Rx-LD	3.49	2.52	1.77	1.04
	"Gate connection" (Stack-MOS structure for Rx module)	Rx-CC1	4.19	3.33	1.69	1.61
		Rx-CC2	2.76	2.32	1.21	1.16
		Rx-STC	3.57	3.02	1.61	1.64
		Rx-Latch	3.75	2.95	1.79	1.73
	"Gate connection" (Stack-MOS structure for Tx module)	Tx-CC1	4.37	2.91	1.63	1.19
		Tx-CC2	3.3	2.56	1.22	1.28
		Tx-STC	6.68	5.26	1.43	1.19
		Tx-Latch	6.69	5.74	1.26	1.26

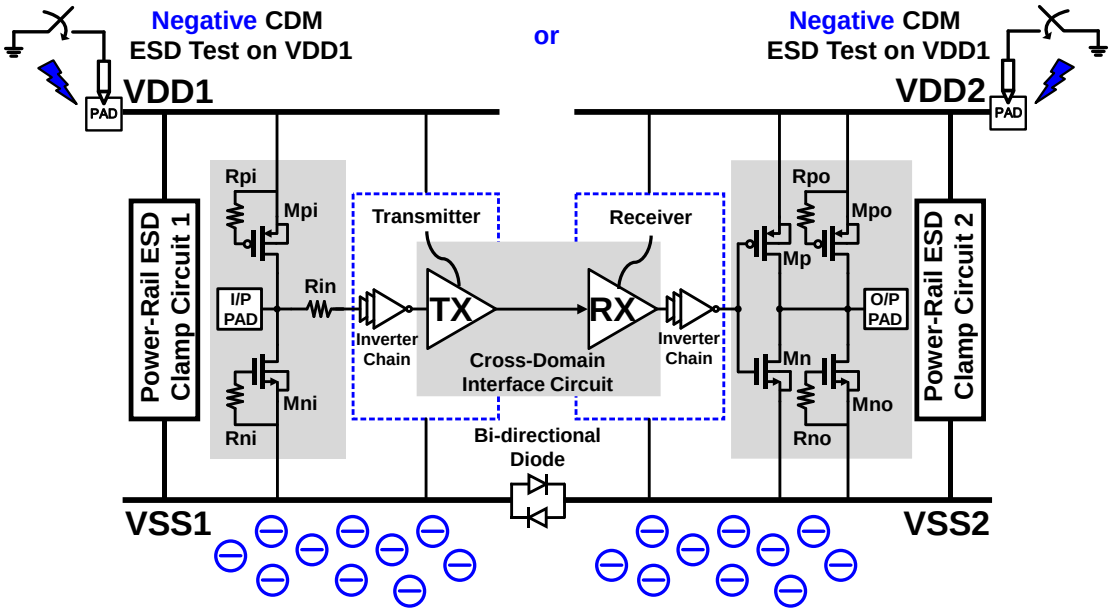
□ **Measured by Thermo Scientific Celestron TLP/VF-TLP Test System**

3.3.3 Cross-Domain CDM Robustness

The cross-domain CDM ESD test is done by pointing the pogo pin on VDD1 (as VDD1-to-VSS2 stress) or VDD2 (as VDD2-to-VSS1 stress). Both positive and negative polarity stress is done for two discharge directions are shown in Fig. 3.30 (a) and Fig. 3.30 (b), respectively. The CDM ESD test step voltage is 100V, and the failure criterion is defined as one of the electrical or function verification results out of specifications. Fig. 3.31 illustrates measured +500V and -500V CDM discharge current waveforms. The CDM test was performed on the CDM test chip, which assembled in the SB-48 package, and the discharge current was measured by a high-bandwidth digital oscilloscope. The CDM discharge current waveforms for the test chip shows longer current pulse duration and rise time than the typical value of the JEDEC standard [18]. The CDM current rise time from 10 % to 90 % was around 1.5ns and the peak value was around 4A. As a result, different package types will affect the parameter of discharge waveform, so the results of simulation and measurement may be different. Moreover, the peak current and rise time might be various from each pin under test (PUT), since the different test-key locations and charge distribution in the whole chip.



(a)



(b)

Fig. 3.30. The illustration of a cross-domain CDM ESD test, which is done by pointing the pogo pin on VDD1 (as VDD1-to-VSS2 stress) or VDD2 (as VDD2-to-VSS1 stress) with (a) the positive or (b) the negative CDM charge.

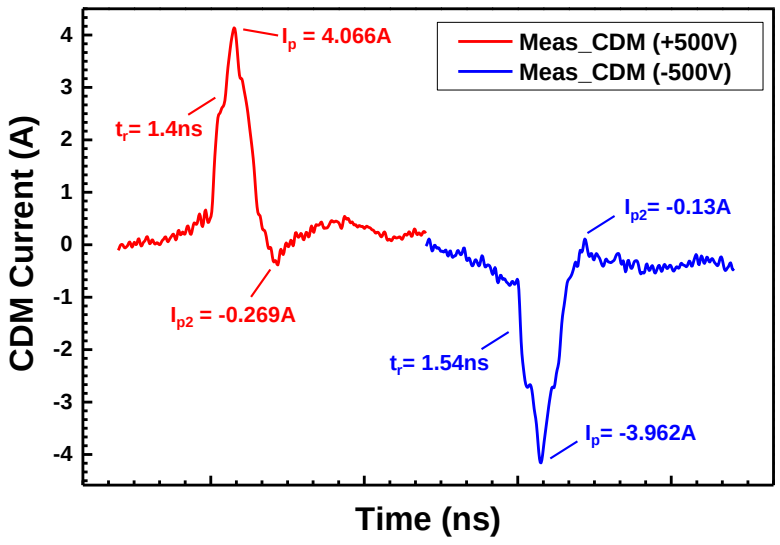


Fig. 3.31. The measured +500V and -500V CDM discharge current waveforms.

All measured results of the proposed design after CDM ESD stress are listed in Table 3.2. The test condition VDD1(+), represents the positive CDM stress performed on VDD1, and so on. For easy inspection, CDM levels exceeding 500V are highlighted in blue, and below 500V are highlighted in red, which should be paid attention to. As expected, the Baseline design shows the worst CDM ESD robustness, about 100V CDM level under three stress conditions.

For the split of dimension variation, the CDM level of Rx-LD design, which adopts a larger aspect ratio of RX, express terrible under VDD1(-) condition but good under other conditions. This proves that the large-size Rx-PMOS could withstand a higher instantaneous electric-field by a larger oxide area, but the large-size Rx-NMOS easily attracts the CDM charge, which is stored in the spacious common p-substrate, to damage the thinner gate-oxide.

For the split of Rx modification, the Rx-CC1 and Rx-CC2 design shows satisfactory and acceptable CDM performance, respectively, despite the gates are directly connected to local VDD/VSS. In other words, compared to the Baseline design, the benefits of the stacking-MOS structure are obvious. Similarly, the Rx-STC, which adopts tie circuits for gate connection, and the Rx-Latch, which adopts latch for gate connection, can maintain better CDM ESD robustness under different conditions. Note that, VDD2(-) shows the worst withstand voltage for all designs, this phenomenon can be correlated with the VF-TLP results under the VDD2-to-VSS1 condition in the previous section, which verifies the correlation between CDM and VF-TLP results.

When compared to Rx-CC2, Rx-STC, and Rx-Latch, Rx-CC1 performs better for the VDD2 (+) stress. Since the stacking footer PMOS (M_{pR2}) was turned off as high impedance while the potential of VSS2 was high enough. So that, a perfect voltage divider was formed on the floating node V_p, and the CDM-like simulation results seem to support this explanation. According to this reason, the gate of M_{pR2} was directly

connected to VSS2 in the Rx-CC1 design, but other Rx modification designs were not. As known, this may cause different impedance characteristics of off-state M_{pR2}. Hence, the Rx-CC1 design will gain better high impedance characteristics of off-state M_{pR2} from interconnections, thereby obtaining better CDM robustness under VDD2 (+) stress.

Note that, the VDD2 (-) stress condition is the worst-case with the lowest withstand voltage among all designs. Because the discharge path of power-rail ESD clamp circuit 2 was not designed well for fast transient ESD events (VF-TLP or CDM). Hence, the ESD path with non-uniform conduction will induce snapback breakdown and high R_{on} of STFOD. Eventually, the VDD2 potential will be raised-up to force the receiver PMOS gate-oxide breakdown earlier.

As a result, the simulation results in Fig. 2.21 only support us to predict that RX-NMOS (M_{nR} or M_{nR1})/RX-PMOS (M_{pR} or M_{pR1}) is the victim while negative CDM is performed on the VDD1/VDD2. But the difference was slightly between the proposed Rx modification designs. However, in the experimental results, Rx-Latch has been shown to perform better for VDD2(-) stress. The root cause is the different interconnections from VSS2 to the gate of M_{pR2}. It could be explained as the M_{pR2} would be unequally turned on via different paths for each design. During VDD2 (-) stress, the turned-on M_{pR2} would cause V_p raised to near VDD2 potential. For Rx-Latch design, the gate of M_{pR2} is connected to VSS2 through the M_{nR2}, smaller than M_{nL}, and the latch structure also needs enough regeneration time to stably turned M_{pR2} on.

The disconnect between CDM-like simulation and experimental results could be explained by two reasons: First, due to the absence of the HSPICE-model of ESD devices, the actual current flow during CDM events may not be represented and modeled correctly. And the existing devices, used to replace ESD devices, may have some impacts on predictive capabilities. Second, the simulation setup seems to be too

simple, and most parasitic effects are ignored in the existing pre-layout simulation. Thus, the parasitic junction capacitances of internal node V_n/V_p have not been accurately estimated, resulting in the internal node V_n/V_p not being maintained at a perfect floating state during the CDM-like simulation.

For the split of the Tx modification, all designs present equal CDM robustness and show the same failure mechanism, including electrical and functional verification. It means that Tx modification designs have apparent benefits, except for the VDD2 (-) condition. However, different gate connection methods without obvious differences, due to the small size of the Rx module almost suffer from overvoltage issues and vulnerable to damage. Especially under the VDD2(-) condition, Tx modifications are not helpful.

Overall, the new proposed designs have a higher CDM robustness, which means that under different directional stress combinations, stacking-MOS structures embedded in either RX or TX module can reduce cross-domain transient overvoltage issues.

Table 3.2

The List of Measured Cross-Domain CDM Level of All Cross-Domain Test Circuits

Group	Key Factor	Design	CDM Level (V) [Pass]			
			VDD1 (+)	VDD1 (-)	VDD2 (+)	VDD2 (-)
Ref. Circuit	General	Baseline	100 V	200 V	100 V	100 V
Test Circuits	Dimension	Rx-LD	400 V	100 V	> 500 V	300 V
	"Gate connection" (Stack-MOS structure for Rx module)	Rx-CC1	> 500 V	400 V	> 500 V	200 V
		Rx-CC2	400 V	300 V	300 V	100 V
		Rx-STC	400 V	400 V	400 V	200 V
		Rx-Latch	> 500 V	400 V	300 V	300 V
	"Gate connection" (Stack-MOS structure for Tx module)	Tx-CC1	300 V	300 V	300 V	100 V
		Tx-CC2	300 V	300 V	300 V	100 V
		Tx-STC	300 V	300 V	300 V	100 V
		Tx-Latch	300 V	300 V	300 V	100 V

- Measured by Thermo Scientific Orion3
- Start Voltage = 100V, Step Voltage = 100V, Zap Interval = 0.5ms, Target Level = 500V
- If passed 100V qualification but failed at 200V, the CDM level was defined as 100V.

3.3.4 Cross-Domain HBM Robustness

Since many results show that MM is redundant for the HBM since similar failure mechanisms are observed by each other, and the ESD robustness of the two models usually tracks each other. Thus, in this experiment, HBM was adopted instead of MM to compare the cross-domain ESD robustness with CDM. The cross-domain HBM ESD test was also done by applying a positive HBM pulse at VDD1 (or VDD2) with grounded VSS2 (or VSS1), as shown in Fig. 3.32. It considers the situation when the I/O ESD protection circuits did not completely dissipate the HBM ESD energy, and residual ESD charge may inject into the internal circuit and cause interface damage. All measured results are listed in Table 3.3. For easy inspection, the better levels are highlighted in blue, and the worse level is highlighted in red, which should be paid attention to. As expected, the new proposed designs have better HBM robustness compared with the Baseline design under the VDD1-to-VSS2 condition. Furthermore, the HBM behavior under the VDD2-to-VSS1 condition different from CDM behavior under VDD2(-), since the longer rise and duration time of HBM pulse, improves the conduction uniformity of the STFOD and alleviates the transient overvoltage issue between interface circuits. Likewise, for the Rx-LD design, which achieves +2750V under the VDD2-to-VSS1 condition, the large-size Rx-PMOS could withstand a higher instantaneous electric-field by a larger oxide area. Usually, the stacking-MOS architecture is suitable for the I/O ESD protection to increase the breakdown voltage.

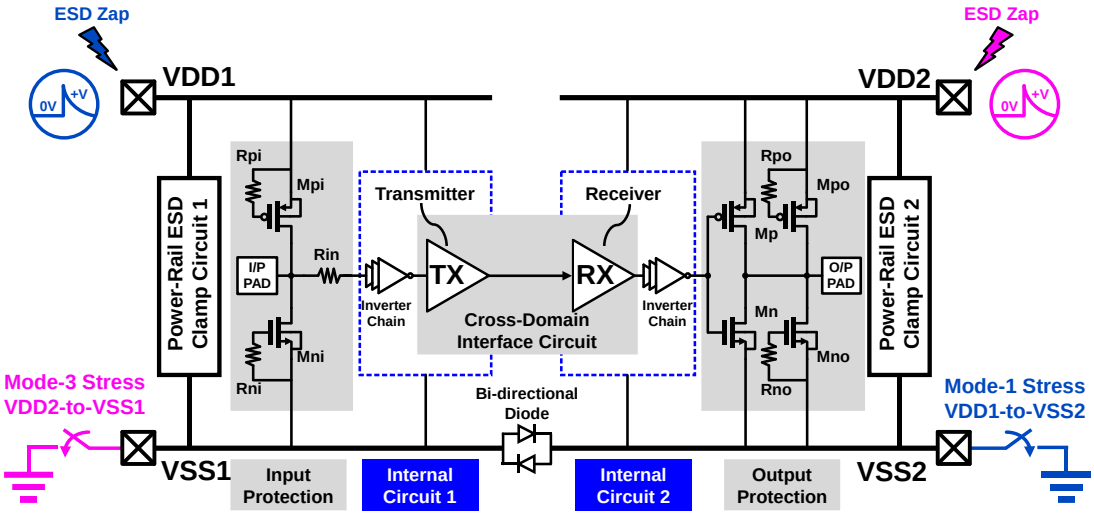


Fig. 3.32. The illustration of a cross-domain HBM ESD test, which is done by applying a positive HBM pulse at VDD1 (or VDD2) with grounded VSS2 (or VSS1).

Table 3.3

The List of Measured Cross-Domain HBM Level of All Cross-Domain Test Circuits

Group	Key Factor	Design	HBM Level (V) [Pass]	
			Mode-1 Stress VDD1-to-VSS2	Mode-3 Stress VDD2-to-VSS1
Ref. Circuit	General	Baseline	+900V	+1750V
Test Circuits	Dimension	Rx-LD	+1500V	+2750V
	"Gate connection" (Stack-MOS structure for Rx module)	Rx-CC1	+1500V	+1750V
		Rx-CC2	+1500V	+1500V
		Rx-STC	+1750V	+2000V
		Rx-Latch	+1500V	+1750V
	"Gate connection" (Stack-MOS structure for Tx module)	Tx-CC1	+1750V	+2000V
		Tx-CC2	+1750V	+1750V
		Tx-STC	+2250V	+1750V
		Tx-Latch	+1750V	+1750V

- Measured by HANWA Compact ESD Tester (HEC-5000)
- For Baseline design: Start Voltage = 500V, Step Voltage = 50V
- For other designs: Start Voltage = 500V, Step Voltage = 250V
- If passed 1750V qualification but failed at 2000V, the HBM level was defined as 1750V.

3.4 Failure Analysis (FA)

3.4.1 Electrical Failure Analysis Results

The InfraRed Optical Beam Induced Resistance Change (IR-OBIRCH), as shown in Fig. 3.33, is used as the electrical FA tool in this experiment to locate the failure point. The principle is using laser scanning IC with a wavelength of 1340nm to partially scan the internal interconnection of the IC and generate a temperature gradient. At the same time, given a constant DC voltage, any material or operating device will have resistance changes due to temperature changes, and through the comparison of resistance changes, to detect the IC defect (or hot spot) location. The IR-OBIRCH can be applied to the IC front-side or back-side, and often used to analyze the internal resistance (high impedance/low impedance) and leakage path inside a chip. The technique can quickly locate defects, such as pin-holes in metal wires, vias, and high resistance regions under vias, it can also effectively detect short circuits or leakage.

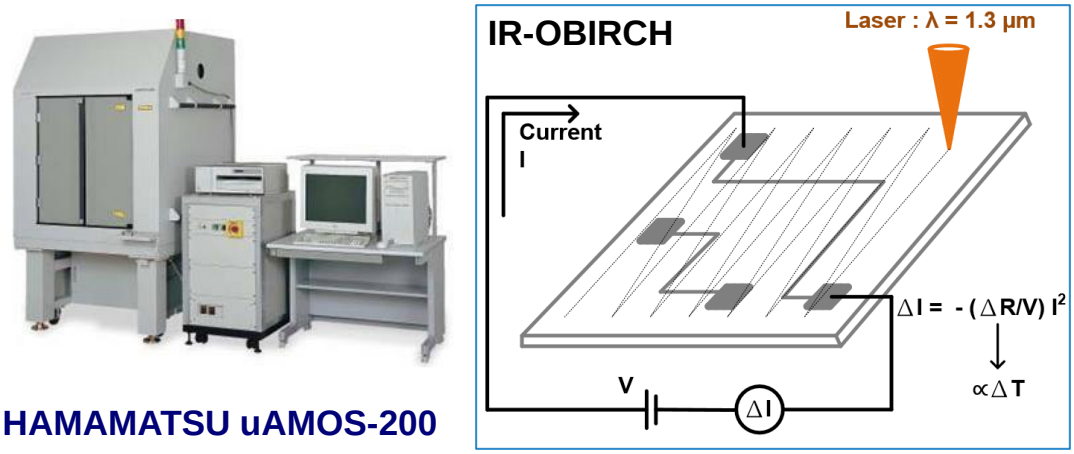
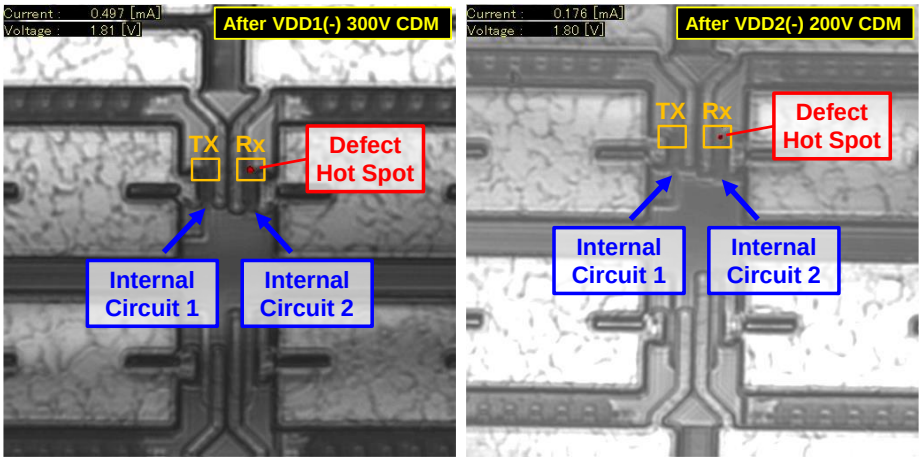


Fig. 3.33. The instrument and schematic diagram of InfraRed Optical Beam Induced Resistance Change (IR-OBIRCH).

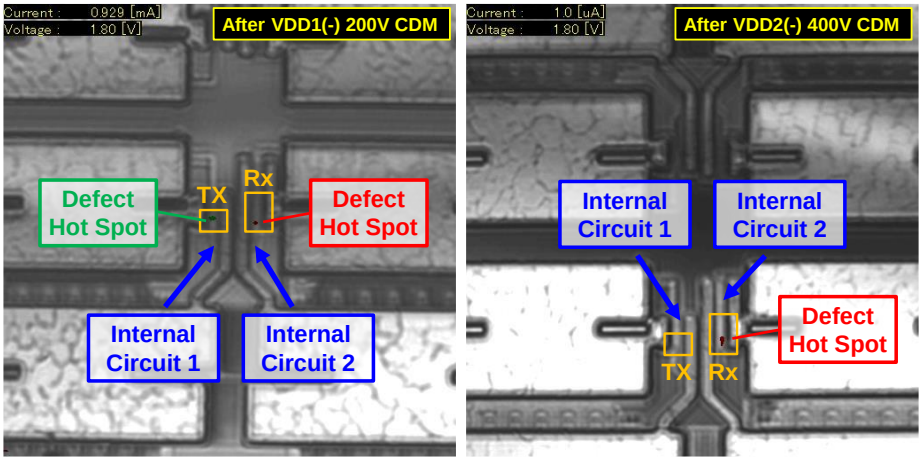
To shorten the time of failure analysis, performed the IR-OBIRCH at the IC front-side in this experiment. By scanning and heating through the surface of a voltage-applied CDM test chip with an IR-laser, the position with impedance variation different from other regions has a higher probability to be considered as the abnormal failure point.

Note that, the green hot spot indicates that the impedance increases, and the leakage decreases; otherwise, the red hot spot indicates that the impedance decreases, and the leakage increases.

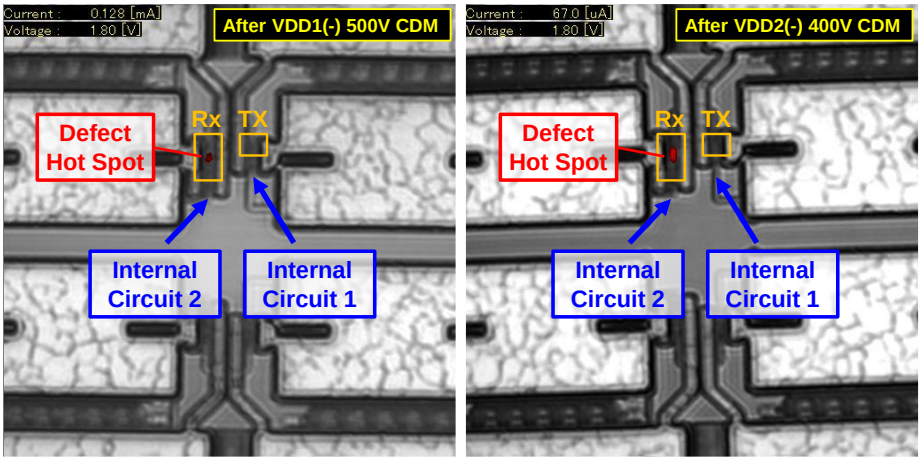
As shown in Fig. 3.34, the Baseline, Rx-LD, Rx-STC, and Tx-STC designs were selected as examples. As known, negative CDM stresses should be critical than positive CDM stresses, so choose two samples, which are stressed VDD1(-) and VDD2(-) conditions respectively, as second worst-case and the worst-case. With 1.8V bias on both power domains, the failure points were detected and located after the negative CDM test on VDD1 and VDD2, respectively. The DC voltage and leakage current were measured from the anode, which connected to VDD1 and VDD2, to the cathode, which connected to VSS1 and VSS2. The key parameters are marked in the picture, including voltage, current, and zap voltage. Since different destruction levels and circuit architectures, each design has a different leakage current after CDM stress. As a result, for all cross-domain test circuits, the defect hot spot, which is located at the Rx module of the cross-domain interface circuit, was concentrated in one point and looks very solid. Unfortunately, due to the small size of the internal circuit components and the limit of machine resolution, the exact damaged devices must be further confirmed through the physical failure analysis (PFA) procedure, which will introduce in detail in the next subsection.



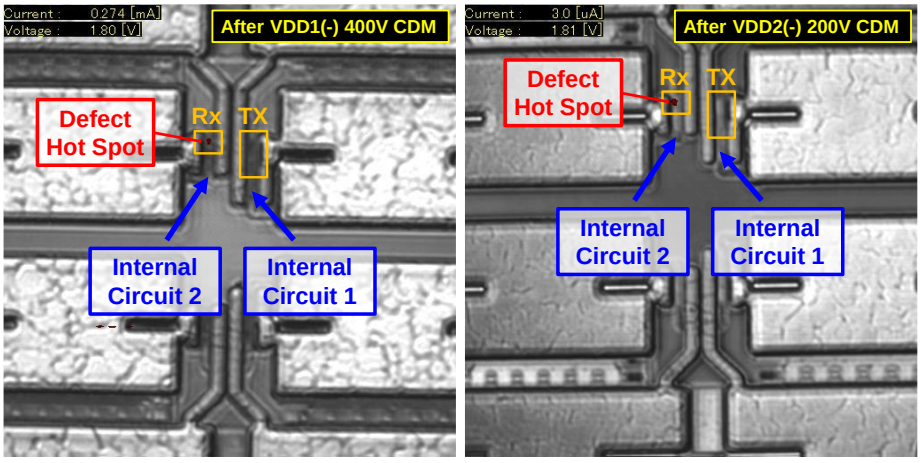
(a)



(b)



(c)



(d)

Fig. 3.34. IR-OBIRCH failure location of the (a) Baseline (b) Rx-LD (c) Rx-STC and (d) Tx-STC designs embedded in cross-domain circuits after CDM ESD tests.

3.4.2 Physical Failure Analysis Results

According to the IR-OBIRCH failure spot locations, then perform the physical FA such as de-layer and Scanning Electron Microscope (SEM). By inspecting the contact anomalies and poly profile by Passive Voltage Contrast (PVC) SEM and High Acceleration Voltage (HKV) SEM respectively, the defect can be analyzed because of gate-oxide breakdown.

The de-layer can be divide into two types: individually de-layer and total de-layer. To carefully inspect the anomalies profile, the individually de-layer technique was adopted in this experiment (see Fig. 3.35), by using chemical acid/gas or polishing, the layers will be removed one by one from the top layer of an IC, and the layers to be removed and retained can be controlled, including metal and oxide layers.

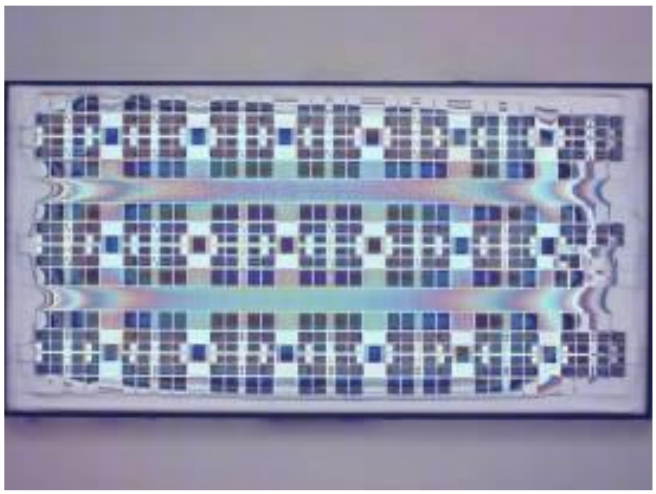


Fig. 3.35. The OM micrograph of CDM test chip after the individually de-layer process.

The principles of PVC-SEM and HKV-SEM are intrinsically similar, the depth of imaging can be controlled by adjusting the energy of the injected electron beam. Both of them impact the IC's surface through a focused electron beam, absorb the reflected or scattered secondary electrons, and achieve the purpose of imaging in a dark environment which reduces the influence of light noise. As shown in Fig. 3.36, the Baseline and the Rx-STC designs are treated as examples, to explain how to distinguish signs of damage.

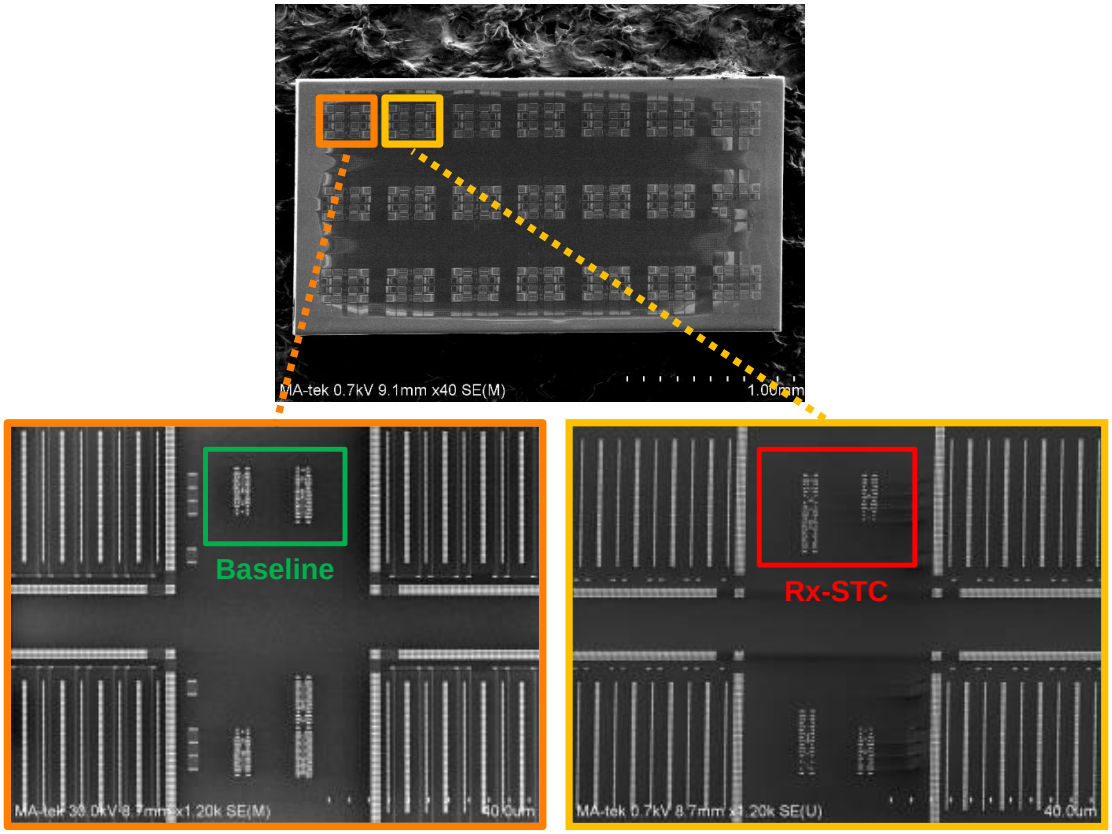
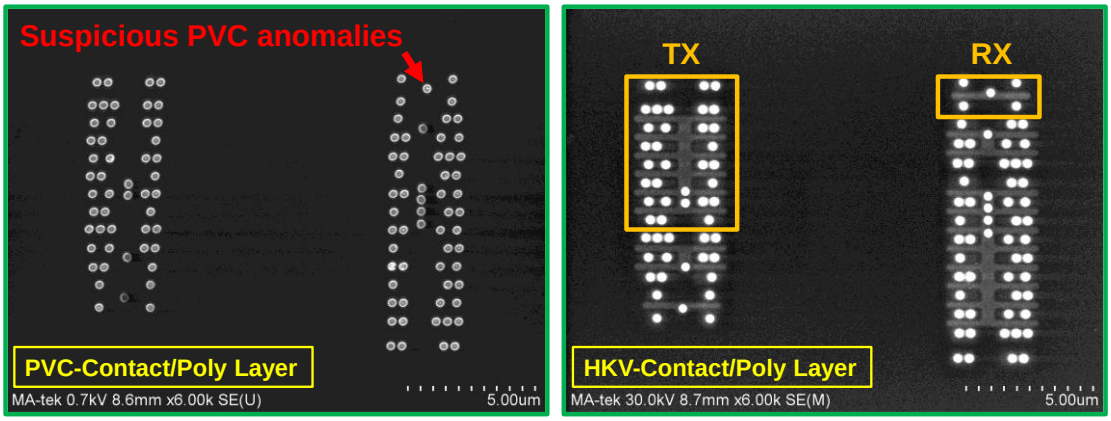
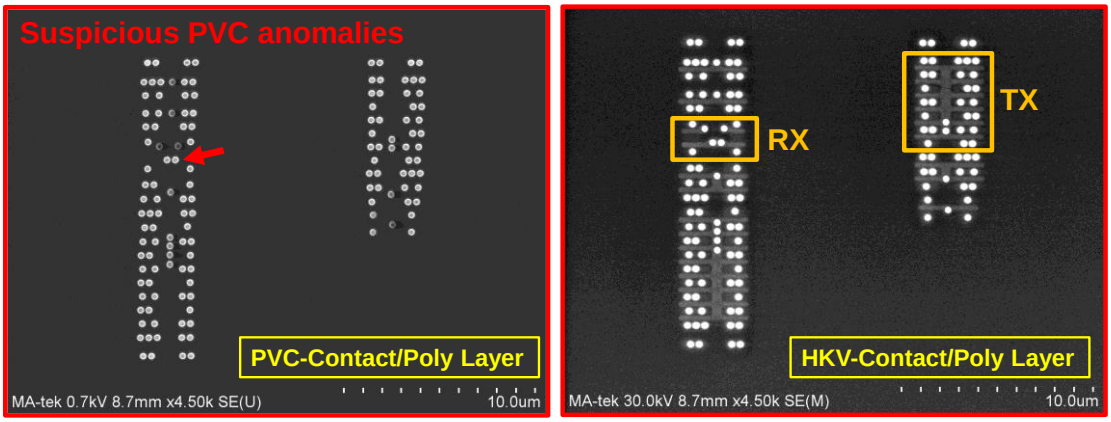


Fig. 3.36. The SEM micrograph and zoomed-in illustrations of CDM test chip after the individually de-layer process.

As shown in Fig. 3.37, when staying in the contact/poly layer, use low-energy PVC to check the poly contact and diffusion contact respectively. In principle, the layer under the poly contact is the insulator, which is a thin oxide. Thus, if it shines abnormally, might be poly burn-out, pinhole, or oxide damage which is considered as suspicious PVC anomalies. On the contrary, the layer under the diffusion contact is the semiconductor material, which normally presents a lighting state. Then use high-energy HKV imaging for comparison. The complete poly profile was looked vaguely at the position of suspicious PVC anomalies, so the possibility of oxide-damage is very high. As expected, the anomalies were surely located at the gates of the Rx module.



(a)

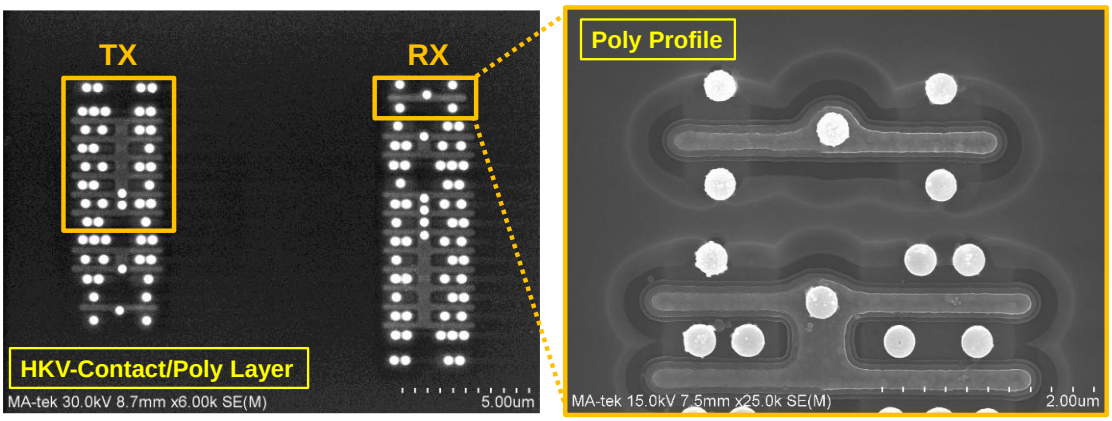


(b)

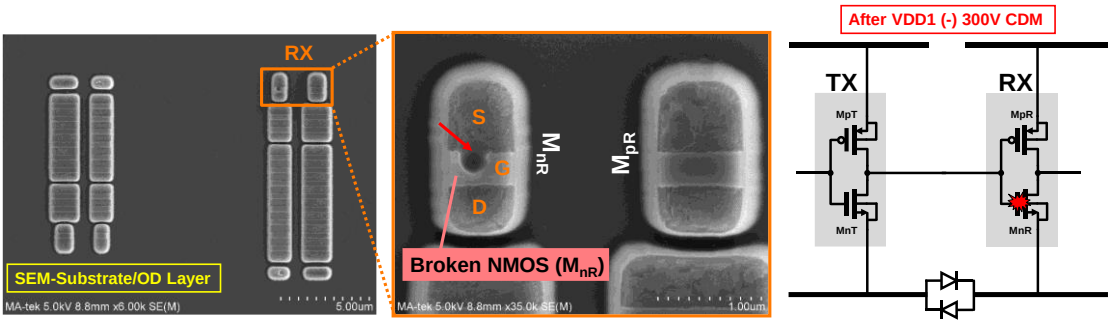
Fig. 3.37. The PVC and HKV-SEM micrographs of the (a) Baseline and (b) Rx-STC designs at the contact/poly layer.

Further removing to the substrate/OD layer, a series of HKV-SEM photos are shown in Fig. 3.38 ~ Fig. 3.47, the top views of internal circuits for all designs displayed clearly and zoom in to inspect. Take Fig. 1. as an example for detailed descriptions, in Fig. 3.38 (a), the poly profile was complete after removing the interlayer dielectric (ILD) layer, and prove that the poly did not burn out. In Fig. 3.38 (b), the Baseline design passed VDD1(-) 200V CDM qualification but failed at VDD1(-) 300V revealed a gate-oxide defect in the Rx module, and breakdown the gate to source overlapped junction first as expected. Significantly, the gate-oxide of RX-NMOS (M_{nR}) in the VDD2/VSS2 domain was broken by large transient overvoltage due to CDM charge transfer, but no damage was observed on the receiver PMOS (M_{pR}). Turning now to Fig. 3.38 (c), the Baseline design passed VDD2(-) 100V stress but failed at VDD2(-) 200V stress by electrical verification, but the gate-oxide defect was disappeared after de-layer procedures since the over-etched. However, none of the other test circuits encountered this problem, and it can be inferred that the actual defect should exist in the gate-oxide of RX-PMOS (M_{pR}). The circuit schematic view was also plotted to assist in correspondence.

In Fig. 3.39 ~ Fig. 3.47, for every cross-domain test circuit, the poly profile, gate-oxide defects of VDD1(-) stress, and gate-oxide defects of VDD2(-) stress were arranged in order. As a result, each broken RX-NMOS/RX-PMOS is connected to the signal line and located in the Rx module of the interface circuit. These results are all related to predictive cross-domain CDM simulation, and corresponding explanations have been discussed. Note that, the serious defects of VDD2(-) 300V stress were shown in Fig. 7(c), including RX-PMOS (M_{pR}) and RX-NMOS (M_{nR}). Since M_{pR} has been damaged after VDD2(-) 200V stress and continuously performed higher stress, resulting in M_{nR} suffering from transient overvoltage issue as well, and M_{pR} was breakdown again.



(a)



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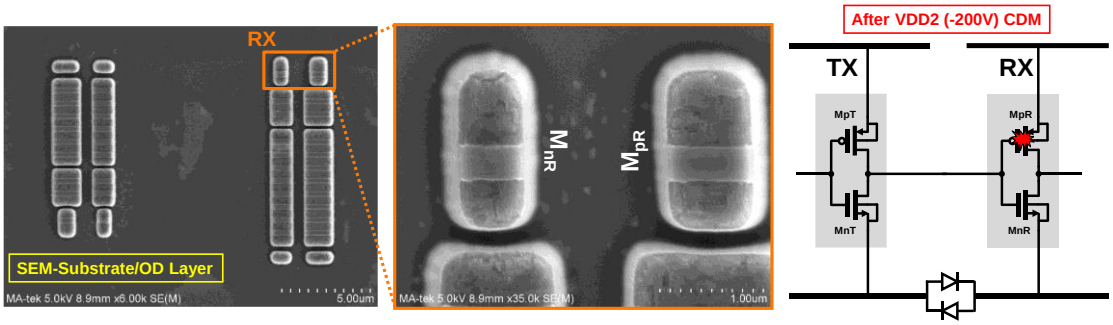
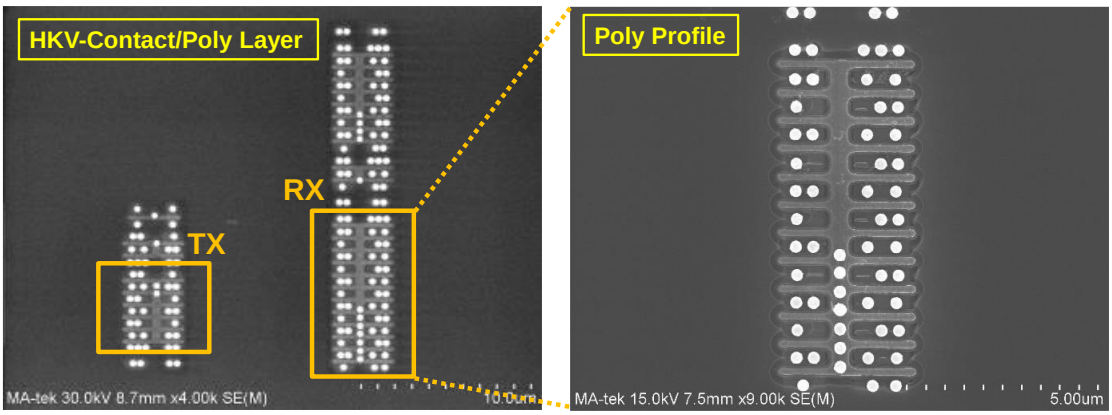
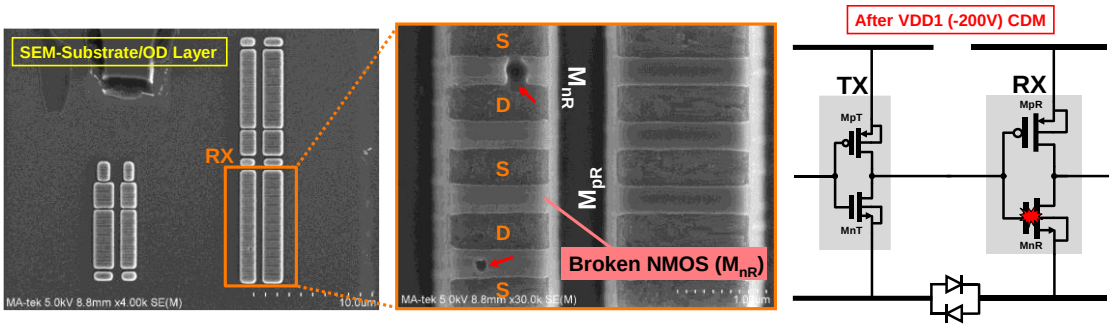


(c)

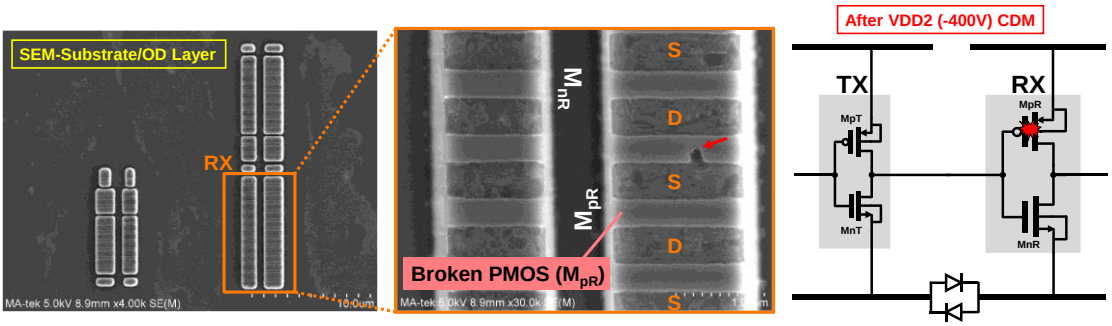
Fig. 3.38. The micrographs of Baseline design scanning (a) HKV-SEM and poly profile at contact/poly layer, and SEM at substrate/OD layer after (b) VDD1(-) CDM stress and (c) VDD2(-) CDM stress.



(a)

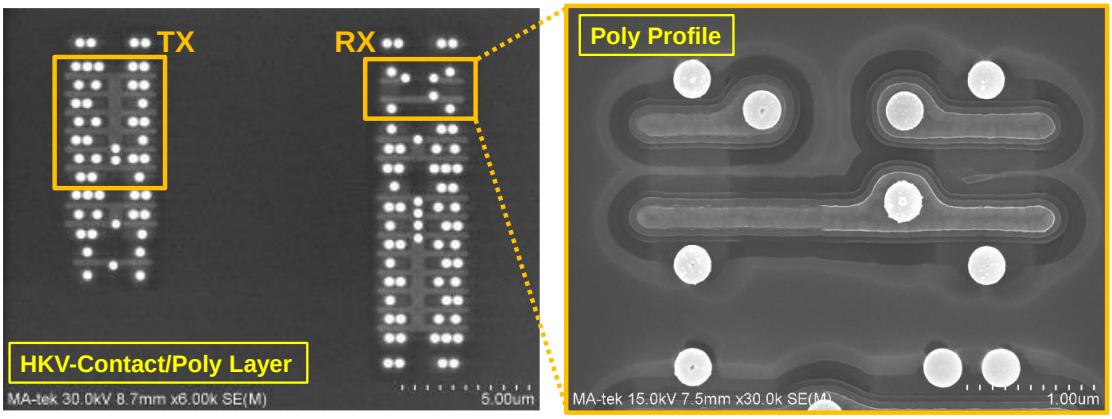


(b)

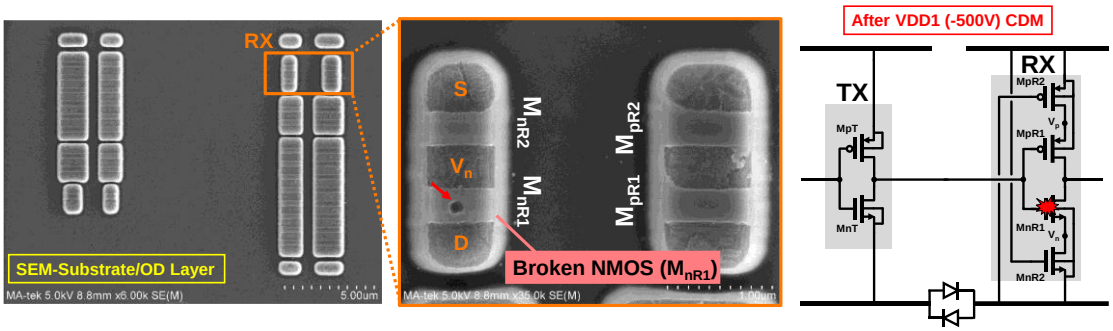


(c)

Fig. 3.39. The micrographs of Rx-LD design scanning (a) HKV-SEM and poly profile at contact/poly layer, and SEM at substrate/OD layer after (b) VDD1(-) CDM stress and (c) VDD2(-) CDM stress.



(a)



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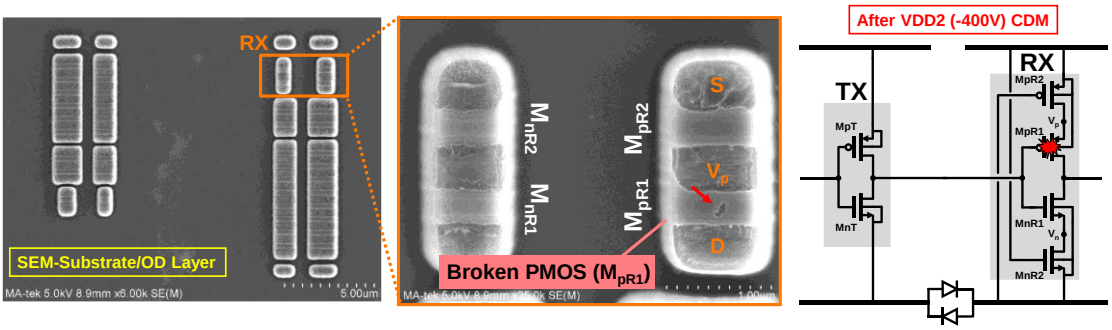
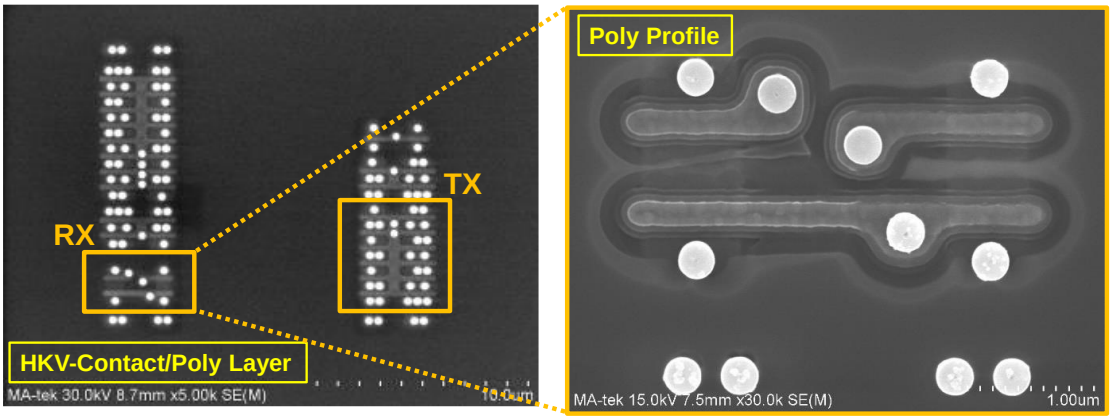
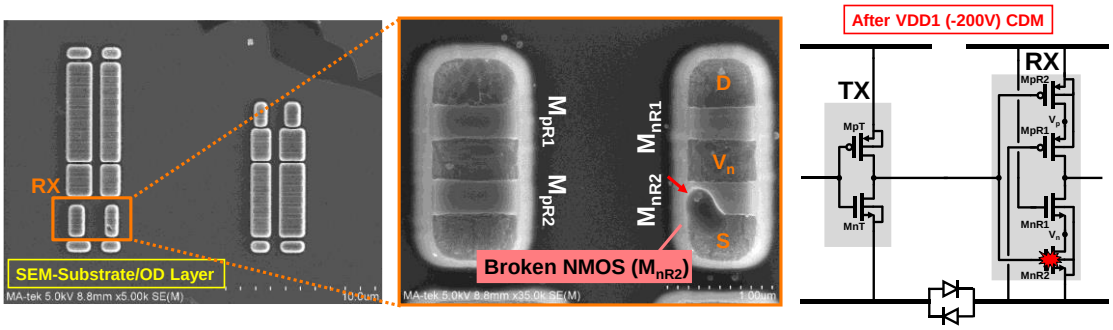


(c)

Fig. 3.40. The micrographs of Rx-CC1 design scanning (a) HKV-SEM and poly profile at contact/poly layer, and SEM at substrate/OD layer after (b) VDD1(-) CDM stress and (c) VDD2(-) CDM stress.



(a)



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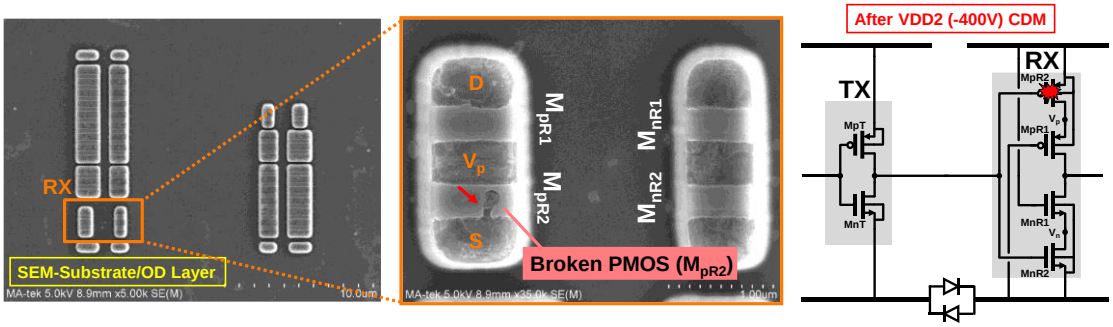
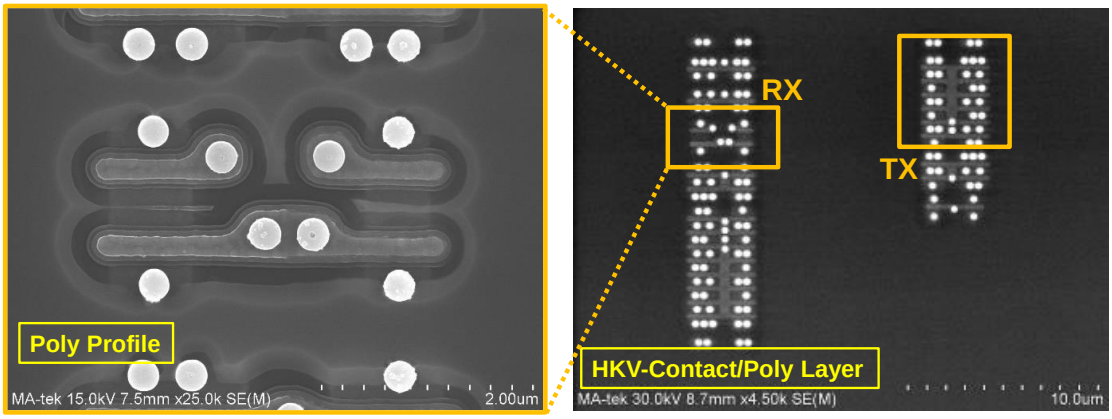
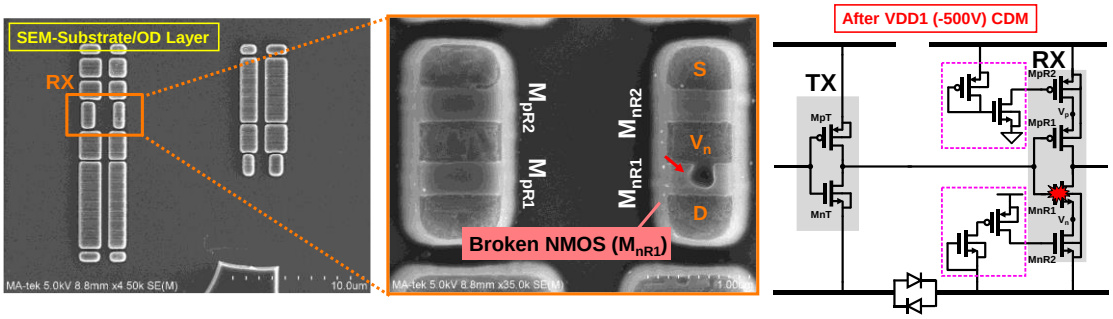


(c)

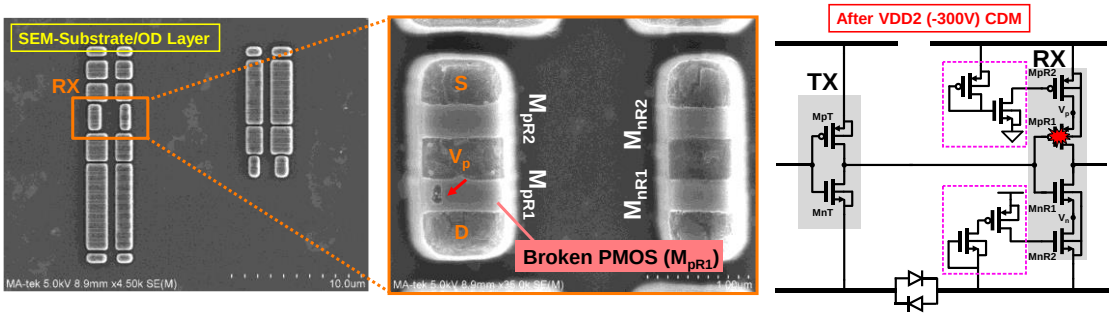
Fig. 3.41. The micrographs of Rx-CC2 design scanning (a) HKV-SEM and poly profile at contact/poly layer, and SEM at substrate/OD layer after (b) VDD1(-) CDM stress and (c) VDD2(-) CDM stress.



(a)

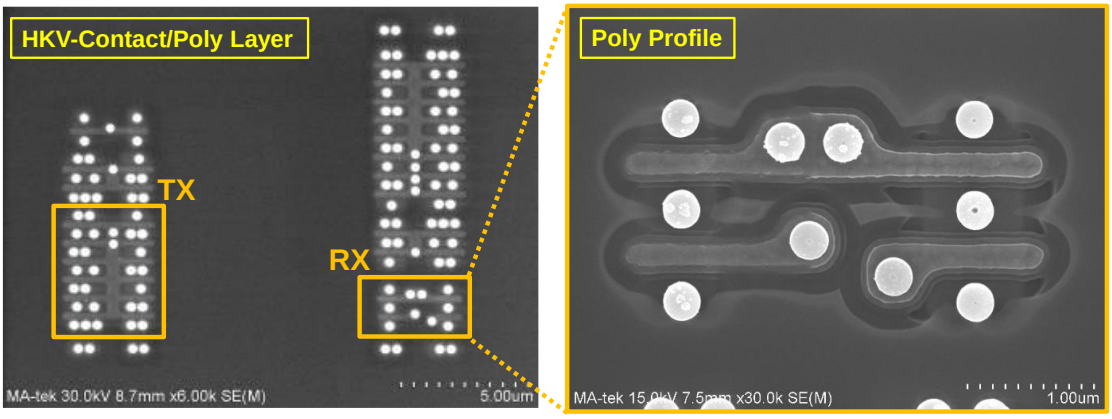


(b)

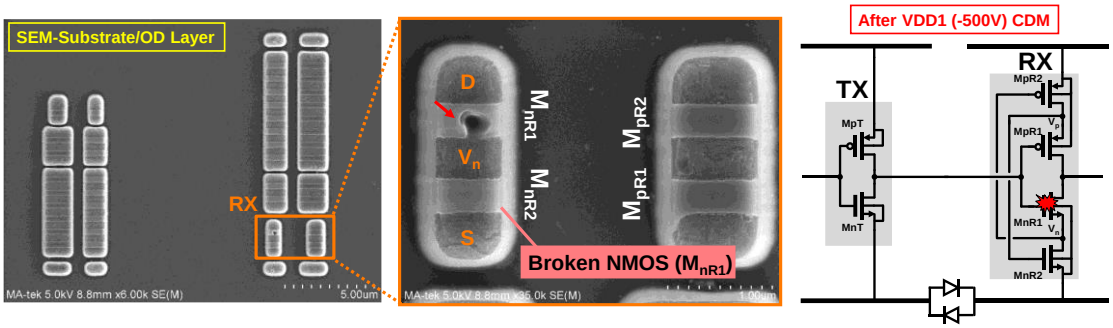


(c)

Fig. 3.42. The micrographs of Rx-STC design scanning (a) HKV-SEM and poly profile at contact/poly layer, and SEM at substrate/OD layer after (b) VDD1(-) CDM stress and (c) VDD2(-) CDM stress.



(a)



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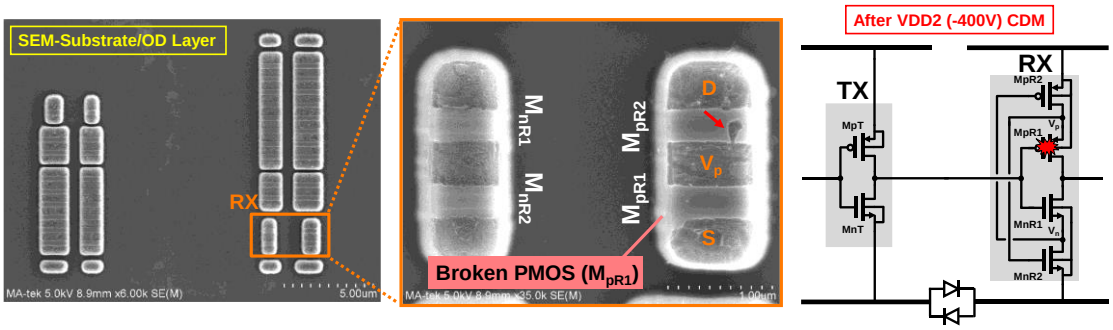
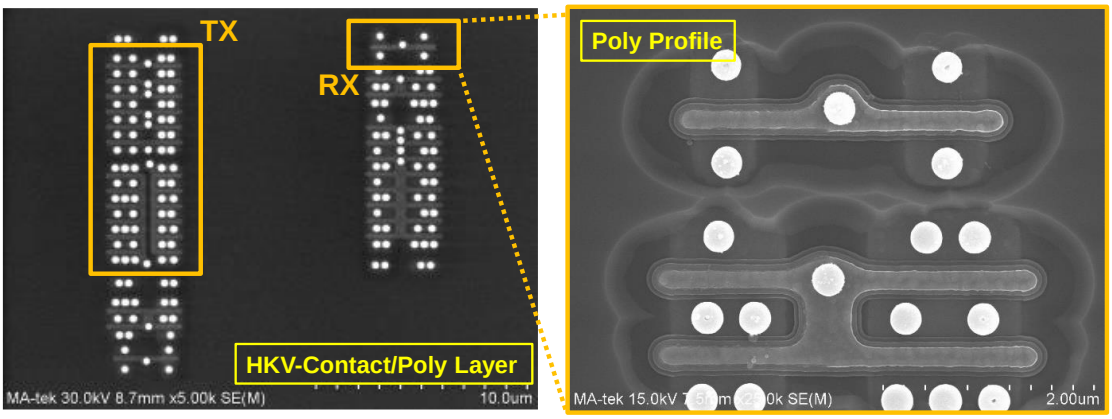
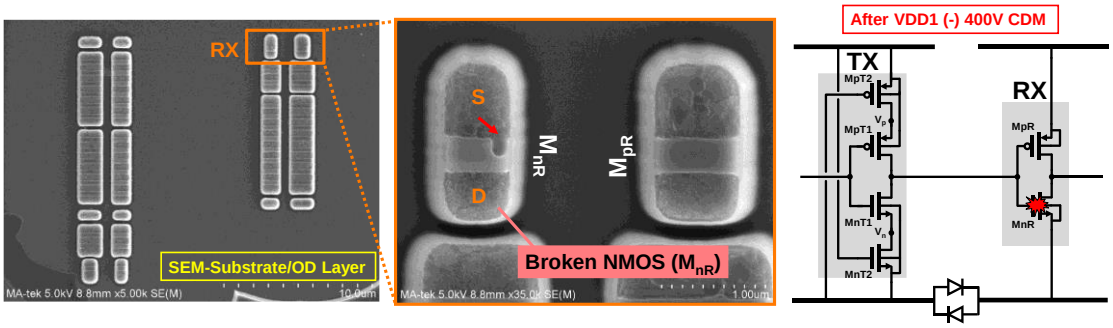


(c)

Fig. 3.43. The micrographs of Rx-Latch design scanning (a) HKV-SEM and poly profile at contact/poly layer, and SEM at substrate/OD layer after (b) VDD1(-) CDM stress and (c) VDD2(-) CDM stress.



(a)



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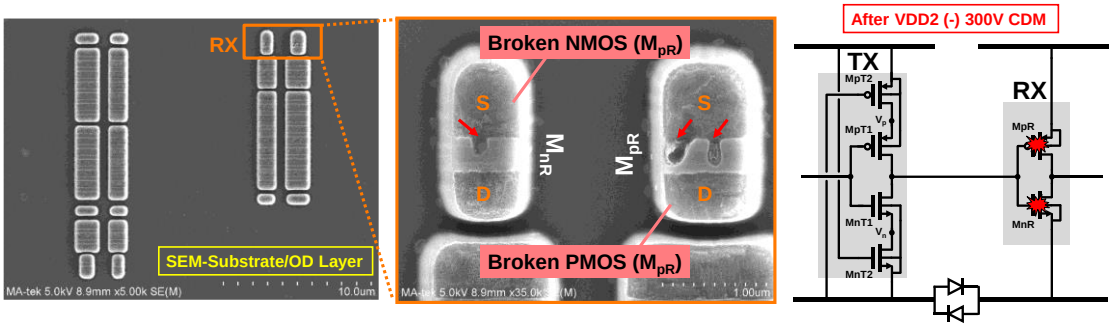
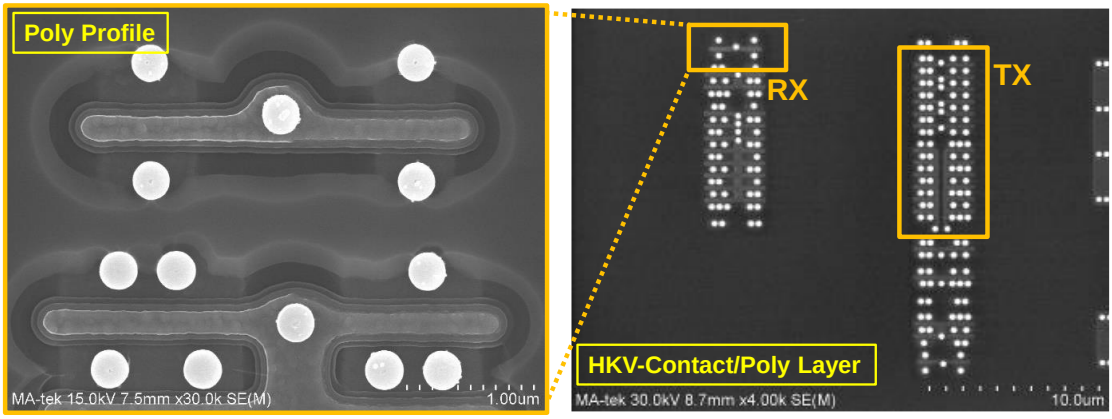
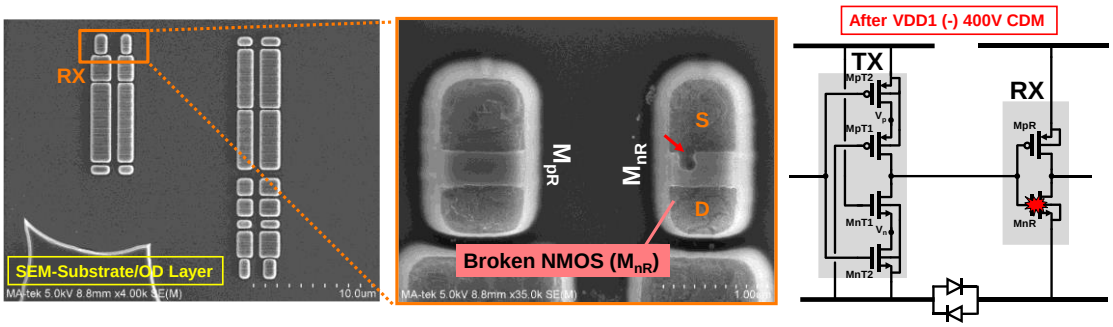


(c)

Fig. 3.44. The micrographs of Tx-CC1 design scanning (a) HKV-SEM and poly profile at contact/poly layer, and SEM at substrate/OD layer after (b) VDD1(-) CDM stress and (c) VDD2(-) CDM stress.



(a)



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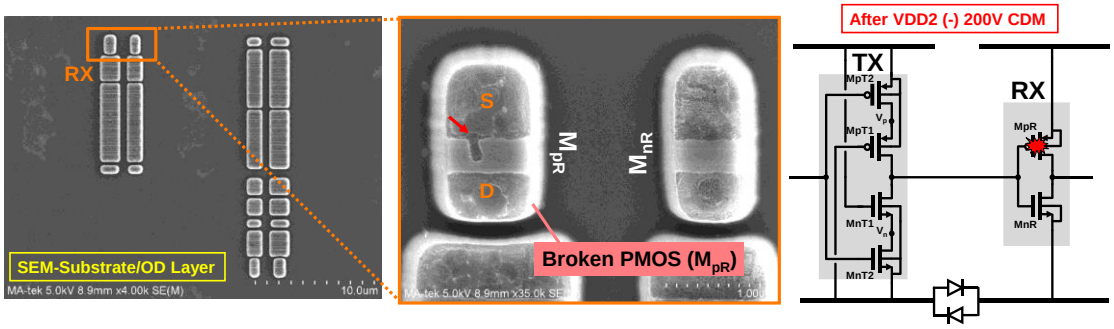
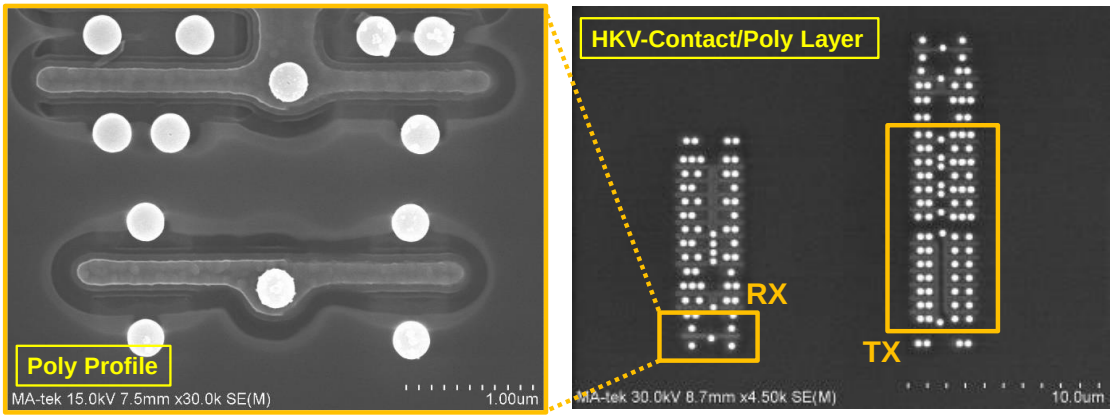
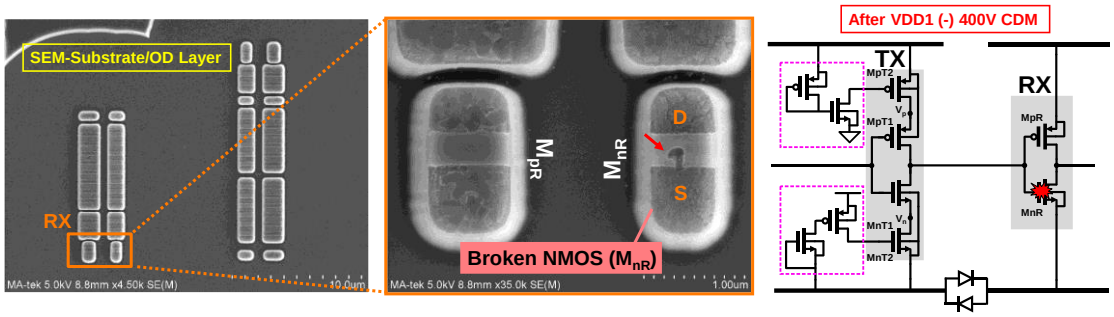


(c)

Fig. 3.45. The micrographs of Tx-CC2 design scanning (a) HKV-SEM and poly profile at contact/poly layer, and SEM at substrate/OD layer after (b) VDD1(-) CDM stress and (c) VDD2(-) CDM stress.



(a)



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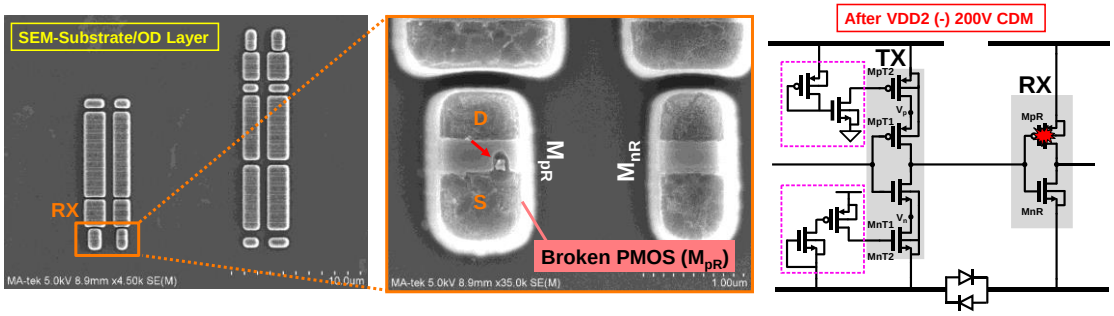
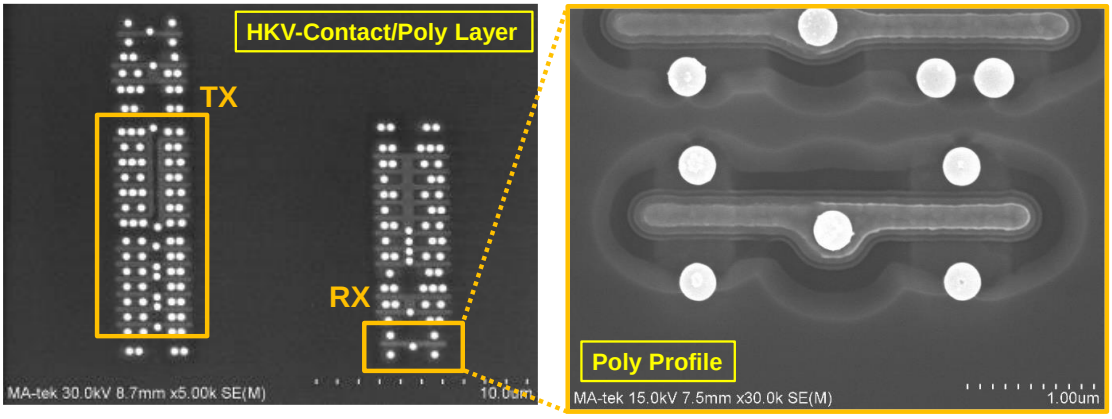
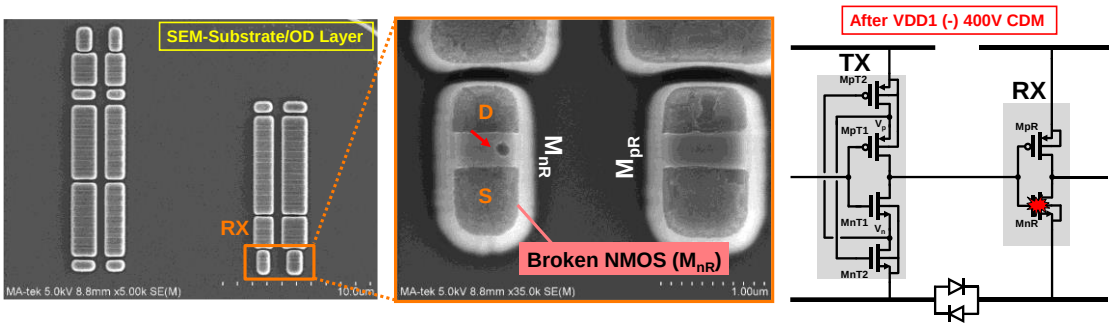


(c)

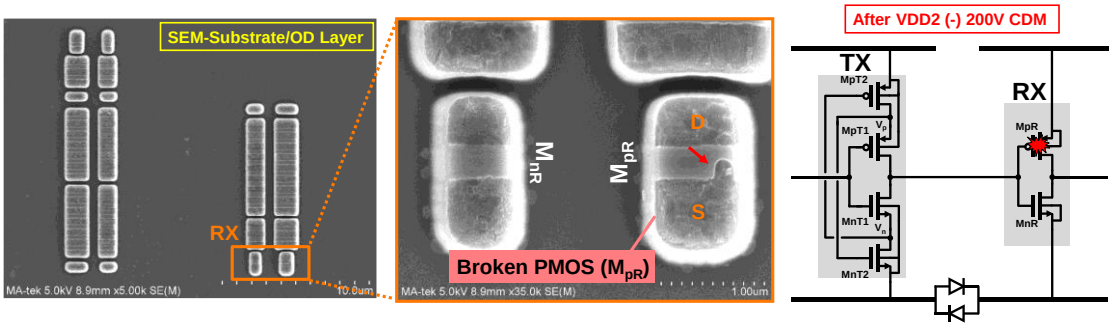
Fig. 3.46. The micrographs of Tx-STC design scanning (a) HKV-SEM and poly profile at contact/poly layer, and SEM at substrate/OD layer after (b) VDD1(-) CDM stress and (c) VDD2(-) CDM stress.



(a)



(b)



(c)

Fig. 3.47. The micrographs of Tx-Latch design scanning (a) HKV-SEM and poly profile at contact/poly layer, and SEM at substrate/OD layer after (b) VDD1(-) CDM stress and (c) VDD2(-) CDM stress.

3.5 Summary

In this chapter, the cross-domain test circuits with different interface structures are fabricated and properly assembled. The failure criterion was briefly decided by two verifications and used to evaluate the cross-domain CDM and HBM robustness. The mode-1 to mode-4 stresses are used in the cross-domain VF-TLP test with detailed discussion. In the cross-domain CDM ESD test, both VDD1 and VDD2 are discharged under positive and negative stress. For all test circuits in multiple test conditions, the CDM performance of the Rx-LD design with dimension variation is the worst, the Baseline design without modification is the second-last, the others taking a stacking-MOS structure for Rx module have better CDM robustness but still have some slight differences, and the others taking a stacking-MOS structure for Tx module have nearly the same level. The summarized values of VF-TLP, HBM, and CDM performance were listed in Table 3.4. Moreover, the measured specifications were also be listed in Table 3.5 ~ Table 3.6. Since the output buffer has a large enough driving capability, even if the speed of the input signal is increased to the upper limit of the function generator, the output waveform can still maintain a full swing 1.8V square wave. Therefore, the maximum frequency test has not been added due to the limitations of the instrument. In the end, failure analysis performed on the IC samples shows the CDM ESD damage locates at the interface circuit and breakdown the gate-oxide from the gate side to the source side.

Table 3.4

The summarized list of Measured Cross-Domain VF-TLP,

HBM, and CDM performance of All Cross-Domain Test Circuits

	VF-TLP I_{t2} (A)				CDM Level (V) [Pass]				HBM Level (V) [Pass]	
Designs	Mode-1	Mode-2	Mode-3	Mode-4	VDD1 (+)	VDD1 (-)	VDD2 (+)	VDD2 (-)	Mode-1	Mode-3
Baseline	2.93	2.43	1.46	1.22	100 V	200 V	100 V	100 V	+900V	+1750V
Rx-LD	3.49	2.52	1.77	1.04	400 V	100 V	> 500 V	300 V	+1500V	+2750V
Rx-CC1	4.19	3.33	1.69	1.61	> 500 V	400 V	> 500 V	200 V	+1500V	+1750V
Rx-CC2	2.76	2.32	1.21	1.16	400 V	300 V	300 V	100 V	+1500V	+1500V
Rx-STC	3.57	3.02	1.61	1.64	400 V	400 V	400 V	200 V	+1750V	+2000V
Rx-Latch	3.75	2.95	1.79	1.73	> 500 V	400 V	300 V	300 V	+1500V	+1750V
Tx-CC1	4.37	2.91	1.63	1.19	300 V	300 V	300 V	100 V	+1750V	+2000V
Tx-CC2	3.3	2.56	1.22	1.28	300 V	300 V	300 V	100 V	+1750V	+1750V
Tx-STC	6.68	5.26	1.43	1.19	300 V	300 V	300 V	100 V	+2250V	+1750V
Tx-Latch	6.69	5.74	1.26	1.26	300 V	300 V	300 V	100 V	+1750V	+1750V

Table 3.5

Performance Comparison Table of Proposed Rx-Designs

Spec. (Measured)	Baseline	Rx-LD	Rx-CC1	Rx-CC2	Rx-STC	Rx-Latch
Process Technology	TSMC 0.18μm 1.8V / 3.3V CMOS process					
Power Supply [V]	VDD1 = VDD2 = +1.8, VSS1 = VSS2 = 0V					
Input / Output Signal Swing [V]	V_{IN} = V_{OUT} = 0 ~ +1.8 (Full Swing)					
Duty-Cycle [%]	50.22	50.31	50.34	50.58	50.48	50.45
DC leakage [nA]	I_{DD1} = 2.47 I_{DD2} = 181.3	I_{DD1} = 1.58 I_{DD2} = 182	I_{DD1} = 5.23 I_{DD2} = 181.4	I_{DD1} = 2.59 I_{DD2} = 182	I_{DD1} = 8.11 I_{DD2} = 182	I_{DD1} = 1.85 I_{DD2} = 181.2
Power Consumption @ f=1MHz (P_{VDD1}) [μW]	P_S = 0.00445 P_D = 1.44	P_S = 0.00284 P_D = 1.942	P_S = 0.00941 P_D = 1.19	P_S = 0.00466 P_D = 1.278	P_S = 0.0146 P_D = 0.925	P_S = 0.00333 P_D = 1.56
Power Consumption @ f=1MHz (P_{VDD2}) [μW]	P_S = 0.326 P_D = 92.45	P_S = 0.328 P_D = 65.97	P_S = 0.326 P_D = 63.67	P_S = 0.328 P_D = 77.04	P_S = 0.328 P_D = 81.63	P_S = 0.326 P_D = 61.11

Table 3.6

Performance Comparison Table of Proposed Tx-Designs

Spec. (Measured)	Baseline	Tx-CC1	Tx-CC2	Tx-STC	Tx-Latch
Process Technology	TSMC 0.18μm 1.8V / 3.3V CMOS process				
Power Supply [V]	VDD1 = VDD2 = +1.8, VSS1 = VSS2 = 0V				
Input / Output Signal Swing [V]	$V_{IN} = V_{OUT}$ = 0 ~ +1.8 (Full Swing)				
Duty-Cycle [%]	**50.22**	**50.27**	**50.19**	**50.27**	**50.31**
DC leakage [nA]	**I_{DD1} = 2.47 I_{DD2} = 181.3**	**I_{DD1} = 2.58 I_{DD2} = 181.6**	**I_{DD1} = 2.16 I_{DD2} = 181.3**	**I_{DD1} = 2.74 I_{DD2} = 183.1**	**I_{DD1} = 2.61 I_{DD2} = 181.8**
Power Consumption @ f=1MHz (P_{VDD1}) [μW]	**P_S = 0.00445 P_D = 1.44**	**P_S = 0.00389 P_D = 1.463**	**P_S = 0.00389 P_D = 1.67**	**P_S = 0.00493 P_D = 1.37**	**P_S = 0.0047 P_D = 1.58**
Power Consumption @ f=1MHz (P_{VDD2}) [μW]	**P_S = 0.326 P_D = 92.45**	**P_S = 0.327 P_D = 77.94**	**P_S = 0.326 P_D = 70.2**	**P_S = 0.33 P_D = 60.66**	**P_S = 0.328 P_D = 73.3**

Chapter 4
Conclusions and Future Work

4.1 Conclusions

First of all, ESD threats on the cross-domain interface circuits between the separated power domains are studied in this thesis. Some new ESD protection designs of different receiver/transmitter modules with stacking MOS transistor structures have been proposed and successfully verified in TSMC 0.18-μm 1.8-V CMOS technology. Additionally, one design of a receiver module with dimension variation has been implemented to investigate the behavior under different kinds of cross-domain ESD stresses. The CDM-like simulation was adopted to predict the failure point and to explain the observed failure mechanism. The robustness difference between HBM and CDM is discussed, and the relationship between VF-TLP and CDM is correlated by I_{t2} and CDM levels. From measurement results, for receiver modules, the Rx-Latch design with a higher CDM level and great area efficiency can be the best solution for practical applications. The Rx-STC design without latch issue is also a good choice, especially for noise-sensitive circuits. For transmitter modules, the Tx-STC and Tx-Latch have similar ESD performance but different area impacts. Thus, the Tx-Latch design is a good choice for better circuit integration, and the Tx-STC design can be used in noise-sensitive circuits. In the end, the IR-OBIRCH, PVC-SEM, HKV-SEM, and the de-layer SEM results showed the gate-oxide damage of the receiver module in each design, verifying the failure mechanism of the interface circuit under cross-domain CDM stresses. Consequently, the proposed designs can be used in IC products with separated

power domains. If allowed, using these approaches in both receiver and transmitter to further enhance the robustness is the best way, which against cross-domain CDM events.

4.2 Future Work

4.2.1 Stacking-MOS Structure with Stacking Number Variation

As mentioned above, the effective breakdown voltage of the receiver and transmitter module can be enhanced by increasing the number of header PMOS transistors and footer NMOS transistors (see Fig. 4.1) [8], respectively. Moreover, the size of the parasitic capacitance will determine the ratio of the voltage divider, and the value of the equivalent breakdown voltage could be well designed by spice simulation and layout extraction. In this work, the impact of the stacking number on cross-domain ESD stresses was not investigated, but the benefits of the stacking structure have been verified from experiment results. However, the increase in the number of stacking will lead to performance degradation and area impact. Additionally, for the analog to digital domain crossing circuits, the number of stacking may be limited by the voltage headroom, which affects the DC bias voltage and operating state of the transistor. Based on the above reasons, the optimization of the stacking number is worthy of research and discussion. If the stacking number has a linear relationship with ESD robustness, the linear equation can be modeled to assist designers in making trade-offs between performance and ESD level. In contrast, if the relationship is nonlinear, the linear extrapolation method can be used to estimate the most appropriate stacking number.

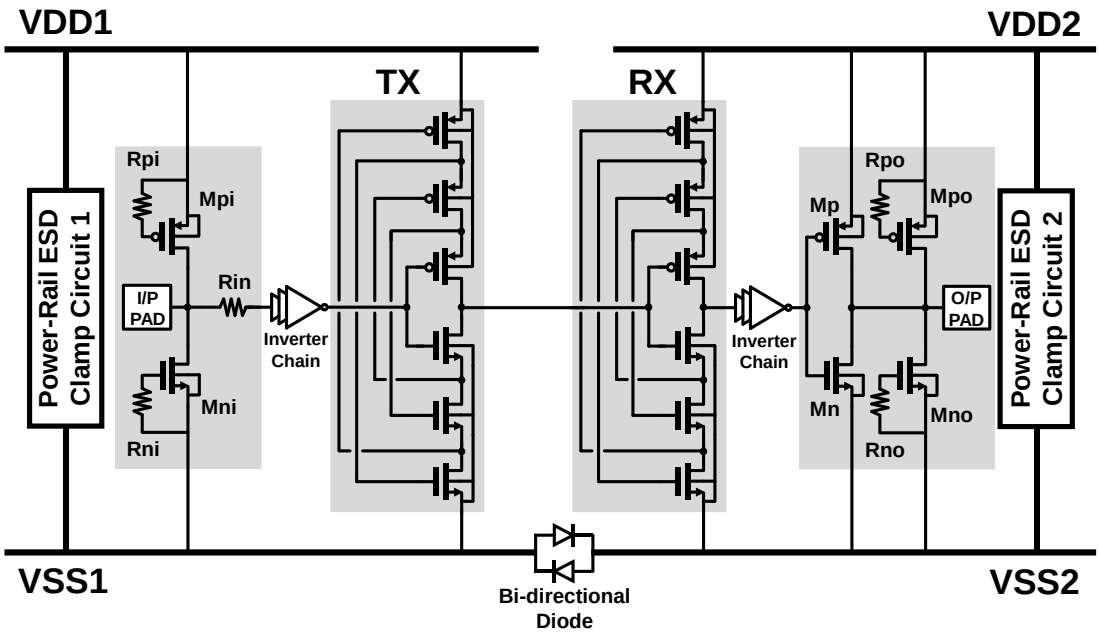


Fig. 4.1. The RX and TX of the domain-crossing circuit can be enhanced by stacking three header PMOS transistors and footer NMOS transistors.

4.2.2 Stacking-MOS Structure with 2nd ESD Clamp Circuit Design

According to the results of CDM robustness, VDD2(-) is the worst-case may be due to the power-rail ESD clamp circuit 2 not being well designed for CDM. Nevertheless, according to the results of failure analysis, the receiver module always suffers from gate-oxide transient overvoltage, and the MOS transistor connected to the signal line is preferentially damaged. Based on the above issues, configure an additional 2nd ESD clamp circuit on the signal line between TX and RX, as shown in Fig. 4.2. The protection design network consists of a series resistor, a pair of gate-ground NMOS (GGNMOS), and gate-VDD PMOS (GDPMOS). In general, the GGNMOS and GDPMOS are added between the signal line and the VSS/VDD rail, respectively. Both transistors are turned off during normal operation since |vgs| is not high enough to invert the conduction channel. When the ESD event occurs, the collector-base junction of the parasitic NPN/PNP BJT becomes reverse biased to the critical electric field and then

induces punch-through breakdown or even avalanche breakdown. As the current flows from the base to the ground through the parasitic resistor, a potential difference will be established across the base-emitter junction, turning on the parasitic NPN BJT and dissipating ESD current. Hence, the 2nd ESD dissipation path is established, and the voltage across the receiver module is clamped as low as possible. The clamped voltage depends on the V_h and R_{on} after the parasitic NPN/PNP BJT breakdown. The 2nd ESD clamp coupled with a stacking-MOS design could be an opportunity to further improve the overall CDM robustness.

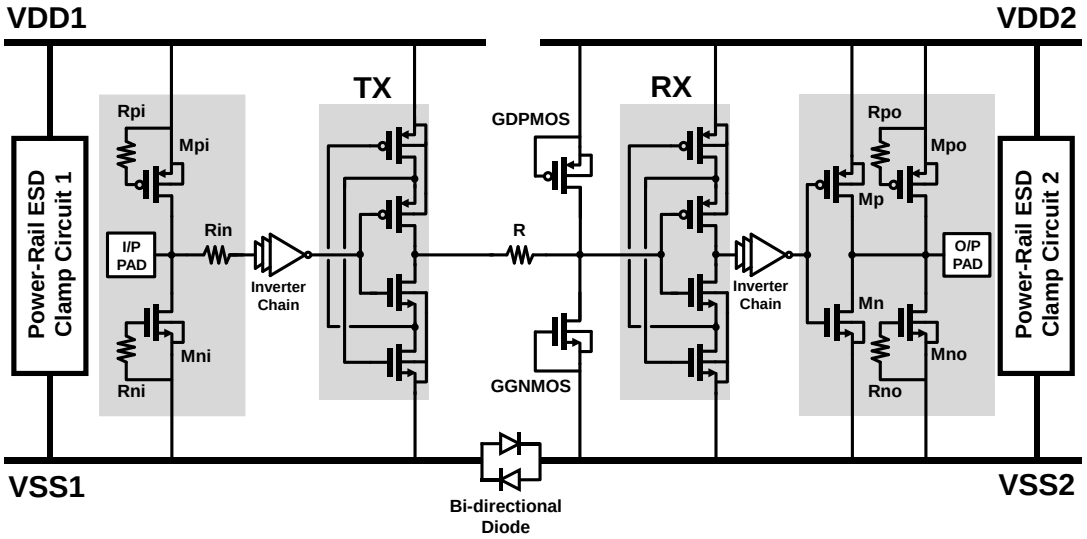


Fig. 4.2. A domain-crossing circuit with latch design on both TX and RX, configure an additional 2nd ESD clamp circuit on the signal line between TX and RX.

4.2.3 Design of Power-Rail ESD Clamp Circuit for CDM-Like ESD Events

According to VF-TLP and CDM results, the STFOD of the power-rail ESD clamp circuit may not suitable for CDM protection. Because the STFOD fabricated in this work has shallow trench isolation (STI) formations inside the device structure, the turn-on time would be too long. Thus, replacing STFOD with large size short-channel NMOS (Fig. 4.3) is a better solution to enhance the driving strength, turn-on speed, and turn-on uniformity of the main ESD device under fast transient ESD events. Although the

reduction of channel length may lead to degradation on the HBM level, the CDM level may be greatly improved. The channel length can be appropriately shrunk to increase the turn-on speed of the main ESD device within a tolerable range, and the common methods for enhancing ESD performance like gate-driven or substrate-trigger design can be adopted for NMOS to further improve not only HBM but CDM. Notably, improving the discharge speed of the power-rail clamp circuit is a straightforward solution for CDM protection. However, the location of domain-crossing circuits and parasitic resistance of power/ground rails are still important factors. If the power-rail clamp circuits are very far away from the interface circuits, a high enough voltage drop may destroy the core devices. Therefore, the self-protection design like stacking-MOS structure will have significant benefits when protection capabilities cannot be effectively provided by whole chip ESD protection circuits.

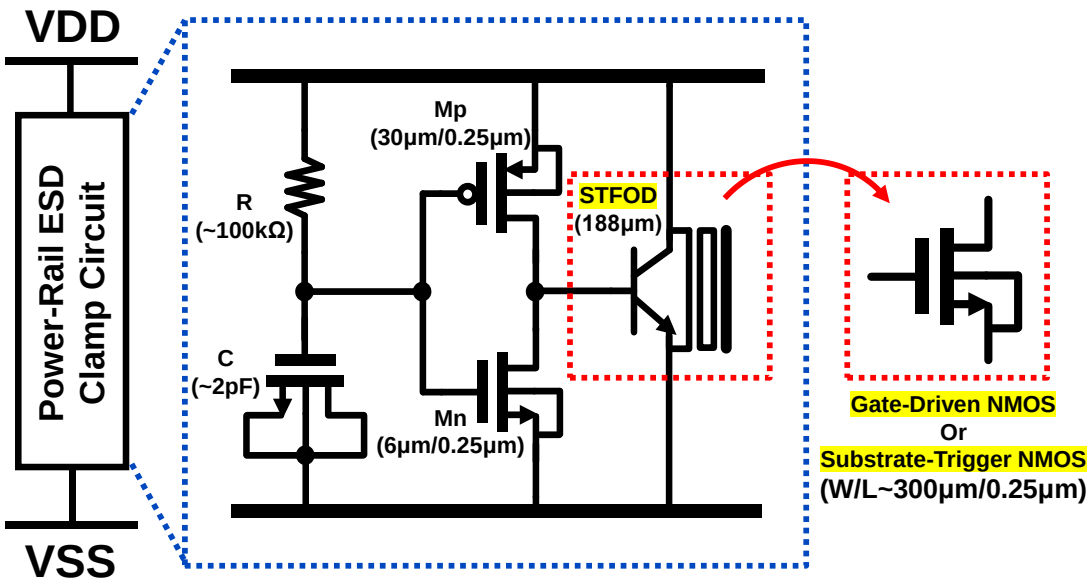


Fig. 4.3 A typical design methodology of power-rail clamp circuit for enhancing the driving strength, turn-on speed, and turn-on uniformity of the main ESD device under fast transient ESD events.

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