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電子研究所

碩 士 論 文

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高壓互補式金氧半製程閂鎖效應之探討與佈局準則建立

Study on the Latch-up Design Rules in a 0.18μm High-Voltage CMOS Process

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摘要

閂鎖效應 (Latch-Up)是 CMOS 積體電路常見的問題，此效應來自於積體電路中的寄生矽控整流器(Silicon Controlled Rectifier, SCR)，當元件被外界電壓或電流的干擾及刺激意外觸發，在電源端和接地端會形成一個低阻抗的路徑，使得大量電流通過這個路徑。此時，可能會因為大電流流過所產生過多的熱而對晶片造成不可回復的損傷，進而影響電路的特性以及正常操作。隨著 CMOS 製程的演進，高低壓元件通常會被一起整合在同一個晶片上，因此許多晶片產品中產生了閂鎖效應，進而影響元件。不只是高低壓，如果同是高壓，也會因為壓差過大而容易產生閂鎖效應。目前已經有半導體廠有規劃一些高壓元件之間的距離的規則，以應對閂鎖效應的發生。然而，此篇論文主要討論，這些元件彼此之間的距離可能可以進一步縮減，但同時保障閂鎖效應不會發生。

本論文的量測元件包括高壓 p 型的金氧半場效電晶體,高壓 n 型的金氧半場效電晶體, 與低壓 n 型的金氧半場效電晶體，其中，高壓 n 型的金氧半場效電晶體又分為完全包覆的內部元件的雙保護環 (Fully-isolated)與並未完全包覆內部元件的雙保護環(Non-fully-isolated). 此外，作者將量測元件分成四類(Type A, Type B, Type C and Type D), 並對這四組元件進行量測。

量測方法利用傳輸線脈衝產生器(TLP)與 Tektronix 370b 進行量測，並且串上電阻以防止元件因大電流燒毀。並將量測結果做計算，得到觸發電壓(trigger voltage)與保持電壓(holding voltage)的數值. 利用不同操作電壓元件之間的壓差與保持電壓進行比較，若壓差大於保持電壓，則不會有閂鎖效應的發生。

根據此論文實驗結果，根據不同的距離調變，得出不同的保持電壓。隨著不同操作電壓元件距離縮小，保持電壓也會跟著變小。作者根據量測數據來進行外推法，得出不同操作電壓元件可以距離彼此的最小距離，在此距離下，不會有閂鎖效應的風險。將這些距離與半導體廠所建議的不同操作電壓元件之間的距離相比，部分元件相較半導體廠所建議之元件距離可以靠的更近。因此，可以在一個固定佈局面積下，擺放更多的元件。

Study on the Latch-up Design Rules in a 0.18μm High-Voltage CMOS Process

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Abstract

Latch-up is a common issue in High-Voltage CMOS technology. This issue happens when the SCR is accidentally triggered by noise. When the SCR is triggered, the resistor of the SCR will become extremely low and result in a huge current passing through the SCR. At the same time, this huge current will wreak havoc on the device or even make the device burn out all of a sudden and therefore influence the normal function of the device. As CMOS technology is being scaled down, more and more devices whether high-voltage or low voltage have been placed on the same chip to save area and to achieve better efficiency or function. The latch-up issue becomes more serious as the device get closer to each other. On the other hand, some foundries have already designed some rules for latch-up. Nonetheless, the author will discuss these rules in detail to see if there is any room for improvement. In short, more devices can be placed in a limited area if the rule is improved.

In this work, HVPMOSs, HVNMOSs, LVNMOSs have been used. HVNMOSs includes non-fully-isolated HVNMOS and fully-isolated HVNMOS. And there is a latch-up path between HVPMOS and HVNMOS. The author separates these devices into four groups, including Type A, Type B, Type C, and Type D. The measured method includes TLP and Tektronix 370b. And an additional resistor will be used to prevent the huge current from wreaking havoc on the devices. Besides, TLP results and DC curve results will show the holding voltage and trigger voltage of devices. The author will compare the holding voltage to the voltage drop between HVPMOS and HVNMOS.

Based on the experiment results, the holding voltage will decrease as the distance between HVPMOS and HVNMOS decreases. The author will use a method called extrapolation to receive a formula, which is about the relationship between the holding voltage and the distance. Based on this extrapolation method, the author can calculate the minimum distance between HVPMOS and HVNMOS. In comparison to the distance suggested by the foundry rule, the distance rule established by this work can be shortened. Therefore, more devices can be placed in a limited layout area.