國立陽明交通大學

電機學院　電子與光電學程

碩　士　論　文

Degree Program of Electrical and Computer Engineering
National Yang Ming Chiao Tung University

Master Thesis

高壓 BCD 製程之 HV-PMOS 與 LV-PMOS 間的閂鎖效應之研究

Study on Latchup between HV-PMOS and LV-PMOS in High-Voltage BCD Technology

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中華民國一一〇年三月

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碩士論文

A Thesis
Submitted to College of Electrical and Computer Engineering
National Yang Ming Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master of Science
in
Electronics and Electro-Optical Engineering
March 2021
Hsinchu, Taiwan, Republic of China

中華民國一一〇年三月

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摘要

閂鎖效應是 CMOS IC 製程中的可靠度問題之一，隨著積體電路持續創新，往元件尺寸微縮進而達成效能提高與成本降低的趨勢，目前高壓元件與低壓元件已可整合在同一晶片中。當 IC 在此複雜的應用環境中，更應該謹慎地被評估。也因如此閂鎖效應路徑不光只發生在 PMOS 與 NMOS 之間，並且也發生在 HV-PMOS 與 LV 元件之間。其中發生在高壓和低壓元件之間的非預期閂鎖路徑就曾被提出。

因此本論文就針對於發生在高壓 BCD 製程中，HV-PMOS 與 LV-PMOS 間的閂鎖效應進行研究與討論，本論文分為四個章節，本論文的第一章，先對閂鎖效應進行簡介，第二章是對 30V HV-PMOS 與 1.8V LV-PMOS 間的 Latchup 防疫能力進行探討，第三章是對 80V HV-PMOS 與 1.8V LV-PMOS 間的 Latchup 防疫能力進行探討，藉由調變元件結構進行 Latchup 防疫能力的探討，例如：增加寄生 SCR 的陽極與陰極的距離(Spacing)、擴增防護環(Guard Ring)的寬度、多增加防護環(Guard Ring)與調變 LV-MOS 的 NBL 結構，探討其對 Latchup 防疫能力的影響，並經由實驗結果找到一符合 JEDEC Standard No. 78E 規範所要求 Immunity Level A(≥100mA)的布局參數，來達成 Latchup 防疫能力並提供給 IC 設計者做為晶片佈局的參考。

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Abstract

Latchup is one of the reliability issues in the CMOS integrated circuits (ICs). With integrated circuits continuing to innovate, the semiconductor dimension is shrunk to achieve performance improvement and cost reduction. Nowadays, high-voltage (HV) devices and low-voltage (LV) devices can be integrated into a chip. The CMOS ICs application in this more complicated environment should be evaluated more carefully. The latchup path exists between the PMOS and NMOS and between the HV-PMOS and LV devices. An unexpected latchup path between the high-voltage device and the low-voltage device was ever reported.

Therefore, the study on the latchup between HV-PMOS and LV-PMOS in the high-voltage BCD technology is presented in this thesis. This thesis is divided into four chapters. The first chapter is an introduction. In chapter 2, the study on the latchup between 30V HV-PMOS and 1.8V LV-PMOS is presented. In chapter 3, the study on the latchup between 80V HV-PMOS and 1.8V LV-PMOS is presented. The latchup immunity is investigated by modulating the structure, such as increasing the spacing between the anode and the cathode of the parasitic SCR, increasing the guard ring's width, adding the guard ring, and modulation NBL structure of LV-MOS, to discuss its impact on latchup immunity. Through experimental results to find out layout parameters that meet the immunity level A (over 100-mA) requirements of JEDEC Standard No. 78E and provide it to the designer as a reference for chip layout.