國立陽明交通大學

電子研究所

碩 士 論 文

**Institute of Electronics**

**National Yang Ming Chiao Tung University**

**Master Thesis**

# 應用於癲癇控制系統晶片顱內腦電圖訊號紀錄具右肢驅動電路之十六通道互補式金氧半類比前端設計

# The Design of 16-Channel CMOS Analog Front-End (AFE) Amplifiers without/with Right-Leg Drive (RLD) Circuit for Electrocorticography (ECoG) Signal Recording in Epileptic Seizure-Control System-on-Chip

研 究 生：涂筱柔 **(Tu, Hsiao Jeu)**

指導教授：吳重雨 **(Wu, Chung Yu)**

柯明道 **(Ker, Ming Dou)**

中華民國一一〇年十一月

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研 究 生：涂筱柔　　Student : Hsiao-Jeu Tu

指導教授：吳重雨 博士　　Advisor : Dr. Chung-Yu Wu

柯明道 博士　　Dr. Ming-Dou Ker

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學生: 涂筱柔　　指導教授: 吳重雨教授、柯明道教授

國立陽明交通大學

電子研究所

# 摘要

近年來隨時隨地健康檢測的重要性與日俱增，歸功於半導體科技及醫學的發展進步，使電子元件得以被縮小進而應用於神經生理訊號檢測系統。在當中，類比前端電路必須要能有效地蒐集放大生理訊號並防止雜訊干擾，才能使整體電路擁有良好的效能表現。

本論文主要針對顱內腦波訊號(ECoG)設計類比前端電路。顱內腦波訊號的頻率約在0.5Hz到100 Hz，振幅大約在0.1 mV到1 mV之間，考量Pseudo電阻值可能造成的非線性效應，故設計的類比前端電路頻寬介於1~100Hz，同時具有三段可調低通頻寬112/512/1.1kHz與三段可調放大增益59.2/69.9/79.9 dB，輸入參考雜訊為0.64 $\mu V_{rms}$。類比前端電路具有十六個通道，。此類比前端放大器包含了低雜訊前端放大器、可調式開關電容低通濾波器、十六通道多功器和開關電容增益放大器。

基於系統體外機的安全規範需求，改版後加上右肢驅動電路使前端放大器在60Hz輸入訊號時的CMRR大於120dB，以及新增低增益模式。此版設計的類比前端電路頻寬介於0.5~100Hz，同時具有三段可調低通頻寬108.6/504.4/1.04kHz與四段可調放大增益34.7/61.8/69.6/79.8dB，頻寬內輸入參考雜訊為1.6$\mu V_{rms}$，雜訊效率因子(NEF)為5.5。此版為測試版本，具有雙通道，包含低雜訊前端放大器、可調式開關電容低通濾波器、和開關電容增益放大器，平均單通道功率消耗為28.4μW，右肢驅動電路所消耗的功率為10.9μW。此類比前端電路由台灣積體電路製造股份有限公司製造以0.18微米製程實現。

關鍵詞：神經生理訊號、顱內腦波訊號、類比前端電路、右肢驅動、低雜訊放大器

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**Student : Hsiao-Jeu Tu** **Advisor : Prof. Chun-Yu Wu**

**Prof. Ming-Dou Ker**

***Institute of Electronics***

***National Yang Ming Chiao Tung University***



## Abstract

This paper presents a 16-channel analog front-end (AFE) circuit for ECoG recording systems and a two-channel test chip AFE with Right-Leg Drive (RLD) Circuit. The former one consists of a 16 channel analog front-end amplifier. It consists 16 analog front-end blocks, including a 1st-order RC high-pass filter, a buffer, a Switched-Capacitor low-pass filter(SCLPF). And a Switched-Capacitor amplifier (SCA) is shared for 16 channels. The latter one has four programmable gains and low-pass corners, with RLD circuit being added. They are designed for amplification and filtering the bio potential signals, these bio potential signals have the characteristics of small amplitudes, low frequency.

The AFE circuits which is fabricated in TSMC 0.18μm CMOS process can adjust gain at three steps (59.2/69.9/79.9 dB) digitally, the high-pass corner can achieve as low as 0.9Hz and low-pass corner can adjust gain at three steps (112/512/1.1k Hz) digitally.

The input-referred noise is 0.64μVrms between 1Hz to 100Hz, and the total harmonic distortion(THD) is 0.24%. The latter one can adjust gain at four steps (34.7/61.8/69.6/79.8 dB) digitally, and low-pass corner can adjust gain at three steps (108.6/504.4/1.04k Hz) digitally with the high-pass corner can achieve as low as 0.33Hz. The input-referred noise is 1.6μVrms between 0.5Hz to 100Hz, and the total harmonic distortion(THD) is 0.29%. The power of whole AFE amplifier with RLD circuit is 28.4μW average per channel and the RLD circuit power is 10.9μW.

Key words: ECoG, RLD, analog front-end amplifier, SCLPF, SCA