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Master Thesis

用於植入式神經調控系統單晶片13.56百萬赫茲

功率與雙向數據傳輸電路之設計

The Design of 13.56-MHz Power and Bilateral Data

Telemetry Circuits for Implantable Neuro-

Modulation System-on-Chips (SoCs)

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摘要

近幾年中，植入式醫療元件被廣泛的應用在難治疾病上。因為植入式元件是植入於人體裡面，能量和數據的傳遞需要透過一組近場線圈來實現。本文採用台積電 0.18um CMOS 工藝製造一個無線功率和雙邊數據遙測系統，其中整合了脈衝式負載鍵移反向遙測電路、二進制相位鍵移正向遙測電路和電源控制電路。脈衝式負載鍵移比傳統的負載鍵移調製方式具有更好的功率轉換效率。隨著內部晶片功率需求增大的情況下，使用脈衝式負載鍵移進行資料傳輸可以正常接收並正確解調出資料。由於改善了包絡檢測器的單位增益帶寬、相位裕度、閉迴路增益和 PSRR，降低了脈衝式負載鍵移遙測電路的 BER。在 115.2Kbps 的數據速率下傳輸數據，脈衝式負載鍵移造成 12.3mW 的功率損耗此時 BER 小於 3.2×10^{-8} 。而最大數據速率可達 500Kbps。二進制相位鍵解調器改為包絡架構降低解調器的功耗，在 211Kbps 的數據速率下 BER 僅 9.3×10^{-7} 。控制電路有 15 種不同的功率大小可以輸出，由 4bit 控制信號 Ctr[3:0] 控制。

另一個提出的設計是集成了 1X 全波整流器的被動相位鍵移反向遙測電路。它也是採用台積電 0.18um CMOS 技術設計和製造。隨著內部晶片功率需求增大，新版被動相位鍵移數據傳輸仍可以正確接收解調。在 115.2Kbps 的數據速率

下傳輸數據，被動相位鍵造成 8.7mW 的功率損耗此時 BER 為 3.2×10^{-7} 。而最大數據傳輸速率可達 600Kbps。

關鍵詞： 植入式裝置、神經調控系統、功率與雙向數據傳輸電路、二進制相位鍵移、脈衝式負載鍵移、被動相位鍵移。

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The Design of 13.56-MHz Power and Bilateral Data Telemetry Circuits for Implantable Neuro-Modulation System-on-Chips (SoCs)

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Abstract

In recent years, implantable medical devices are widely used in the treatment of difficult-to-treat diseases. Because implanted devices are implanted in the human body, near-field coils are adapted to transfer power and data in wireless. In this paper, wireless power and bilateral data telemetry system integrated with BPSK forward telemetry circuit, PLSK backward telemetry circuit and power control circuit has been designed and fabricated in TSMC 0.18um CMOS technology. PLSK modulation scheme brings out better power efficiency than the conventional LSK modulation scheme. As power requirements of internal chip increase, PLSK data transmission can be demodulated normally. Due to improving the unit gain bandwidth, phase margin, close loop gain and PSRR of the envelope detector, the bit error rate of PLSK is decreased. During data transmission, PLSK causes 12.3mW power loss. The BER has been measured and the value is smaller than 3.2×10^{-8} under the data rate of 115.2Kbps. BPSK demodulator is modified as envelope-based structure to decrease the power consumption of the demodulator. The BER has been measured and the value is 9.3×10^{-7} under the data rate

of 211Kbps. The power control circuit can output fifteen different power level which is controlled by 4-bit control signal Ctr[3:0].

Another proposed design is the PPSK modulator integrated with a 1X full-wave rectifier. It has been designed and fabricated in TSMC 0.18um CMOS technology. As power requirements of internal chip increase, PPSK data transmission can be demodulated correctly. During data transmission, PPSK causes 8.7mW power loss. The BER is 3.2×10^{-7} under the data rate of 115.2Kbps and the maximum data rate is 600Kbps.

Keywords : Implantable device, Neuro-modulation system, Power and bilateral data telemetry circuits, BPSK, PLSK, PPSK.

