

國立陽明交通大學

電子研究所

碩 士 論 文

Institute of Electronics

National Yang Ming Chiao Tung University

Master Thesis

應用於癲癇控制系統晶片具正1.2伏共模與正負11毫伏差
模偽影訊號消除及電極組織阻抗量測電路之互補式金氧半
類比前端腦皮層電圖放大器設計

**Design of CMOS Analog Front-End Electrocorticography
(ECoG) Amplifier with +1.2-V Common-mode and ± 11 -
mV Differential-mode Artifact Signals Removal and
Electrode-Tissue Impedance Measurement Circuits for
Epilepsy Control SoC Applications**

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碩士論文

A Thesis

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應用於癲癇控制系統晶片具正1.2伏共模與正負11毫 伏差模偽影訊號消除及電極組織阻抗量測電路之互補 式金氧半類比前端腦皮層電圖放大器設計

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摘要

本論文介紹了一個應用在顱內腦波訊號(EEG)量測且能耐受+1.2V共模刺激雜訊和±11mV差模刺激雜訊並含電極組織阻抗量測電路的類比前端放大器。訊號由輸入保護電路進入後，由第一級放大器放大。第一級放大器採用了有兩個電流補償電路的軌到軌輸入放大器來達到較大的輸入範圍並維持訊號線性度，並以一個差模刺激雜訊消除電路來消除差模刺激雜訊。通過第一級後，會以一個高通濾波器濾除直流雜訊，並用緩衝器降低後級切換電容式濾波器對低頻截止頻率的影響。再來使用了開關電容低通濾波器和開關電容放大器來選擇通道並提供可調變的增益與高頻截止頻率。電極組織阻抗量測電路用來確認類比前端放大器是否有跟電極接合。

此類比前端放大器電路由台灣積體電路製造股份有限公司製造以0.18微米製程實現。在其0.41 Hz到112.8 Hz的頻寬內，具有1.64 μV_{rms} 的輸入參考雜訊和四段可調的放大增益40.18/60.02/70.13/80.0dB。高頻截止頻率為112.8/1.13kHz二段可調。總諧波失真在無刺激的情況下為0.83%，有刺激的情況下為1.37%。在頻帶內，共模訊號拒斥比均大於121dB且在60Hz下為126.2dB，而輸入阻抗均大於153M歐姆，符合安規要求。電極組織阻抗量測電路若偵測到未成功安裝於電極，則輸出會飽和。

關鍵詞：生醫類比前端放大器、偽影訊號消除、電極組織阻抗量測電路、癲癇控制系統晶片、低雜訊放大器。

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Amplifier with +1.2-V Common-mode and ± 11 -mV Differential-
mode Artifact Signals Removal and Electrode-Tissue Impedance
Measurement Circuits for Epilepsy Control SoC Applications**

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Abstract

This thesis presents the Analog Front-End (AFE) Amplifiers tolerant to +1.2V common-mode artifact (CMA) and ± 11 mV differential-mode artifact (DMA) during stimulation with electrode-tissue impedance measurement circuit for Electrocorticography (ECoG) signal recording.

The ECoG signals are first sensed by the electrodes and passed through the stimulator driver, driver input protection circuit (driver IPC), and AFE Amplifier input protection circuit (AFE Amplifier IPC). Then, the ECoG signals are amplified by capacitively coupled instrumentation amplifier (CCIA) with 37dB gain. The CCIA employs a rail-to-rail input folded-cascode (RRFC) op-amp with two current compensation circuits to achieve a large input range while maintaining the linearity of the signal. For DMA cancellation, a differential-mode artifact cancellation loop (DMACL) is proposed.

Afterwards, a high pass filter (HPF) and a filter buffer are used to suppress the DC offset from the output of the CCIA and block the loading capacitor from the next stage. Then the switched-capacitor low-pass filter (SC-LPF) is employed to drive the hold circuit. Finally, the SC amplifier (SC-Amp) selects the channel through enable switches.

The SC LPF and the SC-Amp provide 3/23/43/43 dB tunable gain, 100/1k Hz tunable low pass corner, and continuous channel selection. The right-leg drive (RLD) circuit boosts the CMRR over 120dB at 60Hz common mode signal. The electrode-tissue impedance measurement circuit is implemented to measure the impedance of the electrodes to confirm the electrodes are well attached to the tissue.

The AFE amplifier circuit is fabricated in TSMC 0.18um CMOS Technology. It has 40.18/60.02/70.13/80.0 dB tunable gain, 112.8/1.13k Hz tunable low pass corner, 0.41 Hz high pass corner and 1.64 μ Vrms input-referred noise in the bandwidth of 0.41-112.8Hz. The measured result shows that the THDs are 0.83% under no stimulation and 1.37% under stimulation. The input impedance of the AFE amplifier reaches 153M ohms or above in the bandwidth of 0.41-112.8Hz, which is large enough for the medical implementation. The CMRR is 121.4dB or above in the pass band and 126.2dB at 60Hz. The electrode-tissue impedance measurement circuit is able to monitor the electrode-tissue impedance normally. Once the input of AFE amplifier isn't well connected to the electrode, the output of the AFE amplifier will saturate.

Keywords: Biomedical Analog Front-End Amplifier, Artifact Signals Removal, Electrode-Tissue Impedance Measurement Circuit, Epilepsy Control SoC Applications, Low Noise Amplifier.