國立陽明交通大學

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碩 士 論 文

Department of Electronics Engineering and Institute of Electronics

National Yang Ming Chiao Tung University

Master Thesis

應用於下視網膜植入具全域適應性背景光消除電路180奈米影像感測互補式金氧半256像素光伏供電下視網膜晶片之設計

The Design of 180-nm CIS 256-Pixel Photovoltaic-Powered Subretinal Prosthetic Chips with Global Adaptive Background Cancellation Circuit for Subretinal Prostheses

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A Thesis

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摘要

本論文提出及分析應用於下視網膜植入具全域適應性背景光消除電路提升影像光動態範圍之互補式金氧半太陽能供電256像素晶片，晶片以台積電0.18微米互補式金氧半影像感測器(CIS)製程設計並製作，尺寸為4mm x 3.2mm。在此晶片中，重要創新有全域適應性背景光消除電路以提升影像光動態範圍及使得晶片產生之圖片看起來更加順暢、水窗保護路徑以保護電極跨壓不超過水窗、恆定刺激電流產生器以降低刺激電流在晶片之間的差異值、恆定電流產生器及環式震盪器以降低電路頻率在晶片之間的變化量、雙向共用電極(BDSEs)配合最佳化刺激安排可使串擾電荷降低、使用電荷泵以供給電路所需的電源供應。訊號光源為6093.6 lux確保最大刺激，量測晶片所產生的電刺激，最大刺激電流為7.74uA，最大刺激電荷為9.8nC，而刺激頻率為21.33Hz。

在全域適應性背景光消除電路中，可模擬出周圍的背景光強度，並在刺激時將背景光加以消除以增加晶片之影像光動態範圍，使得影像動態範圍提升至

34.83dB，最大可感測光強度為6094ux。

晶片中使用恆定刺激電流產生器、恆定電流產生器以及環式震盪器，能夠較不受製程飄移影響且降低電流在晶片之間的電流差異，使得刺激電流以及電路頻率更加穩定，刺激電流的變化量被降低至-10.2~-2.1%，電路頻率則為18.91~23.99Hz。晶片採用雙向共用電極(BDSEs)和分區供電(DPSS)，可增加電極面積與刺激電荷並降低功耗，刺激電荷可提升至9.8nC。最佳化刺激安排可降低因串擾所造成的漏電荷，可降低誤刺激的可能性。使用電荷泵以供給電路所需的電源供應，可供應穩定的1.6V給整顆晶片。透過電性量測，已成功驗證所設計具全域適應性背景光消除電路提升影像光動態範圍之下視網膜晶片的功能。

THE DESIGN OF 180-NM CIS 256-PIXEL PHOTOVOLTAIC-POWERED SUBRETINAL PROSTHETIC CHIPS WITH GLOBAL ADAPTIVE BACKGROUND CALCELLATION CIRCUIT FOR SUBRETINAL PROSTHESES

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ABSTRACT

A CMOS photovoltaic-powered 256-pixel subretinal prosthetic chip with global adaptive background cancellation circuit for wide image dynamic range is proposed and fabricated by TSMC 0.18um CIS (CMOS Image Sensor) technology. The chip area is 4mmx3.2mm. In the proposed chip, the new design concepts are global adaptive background cancellation circuit (GABCC), water-window protection path, constant stimulation current generator, constant current generator and ring oscillator, divisional power supply scheme (DPSS) and bi-directional sharing electrodes (BDSEs), optimized stimulation pattern to minimize crosstalk charges and charge pump. The minimum and maximum detectable image illuminance is 110.5 lux and 6093.6 lux, the maximum stimulation current is 7.74uA, the stimulation charge is 9.8nC and the stimulation frequency is 21.33Hz.

The background illuminance can be detected and converted into a current by the

global adaptive background cancellation circuit (GABCC). Then, the image dynamic range can be increased because the current converted from background illuminance can be eliminated by the circuit in the chip. The image dynamic range is increased to 34.83dB.

In this chip, a constant stimulation current generator is designed to reduce the variations of stimulation current from die to die and the variations are reduced to -10.2~ -2.1%. Moreover, a constant current generator and ring oscillator are designed to lower the variations of stimulation frequency. The stimulation frequency varies from 18.91Hz to 23.99Hz. Bi-directional sharing electrodes (BDSEs) and divisional power supply scheme (DPSS) are adopted in this chip to increase the electrode size and stimulation charges while reducing power consumption. The stimulation charge is increased to 9.8nC. The optimized stimulation pattern is designed to reduce the charge leakage of crosstalk. A charge pump is implemented and the output voltage of charge pump is stable at 1.6V for the whole chip. Through electrical measurement, the functions of designed subretinal chip with global adaptive background cancellation circuit for wide image dynamic range have been validated.