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博 士 論 文

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Doctoral Dissertation

次世代通訊應用之矽與三五族異質整合電晶體元件的靜電放電防護研究

RF ESD Exploration in Si/III-V Heterogeneous Integration for 5G/B5G Applications

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中華民國 一一一 年 十 月

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次世代通訊應用之矽與三五族異質整合電晶體元件的靜電放電防護研究

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摘　　要

到了5G/B5G次世代通訊領域，更高資料傳輸速度(更寬的操作頻寬)為主要的通訊規格升級需求。在傳統的CMOS製程下，靜電放電(ESD)保護元件上的寄生電容為設計射頻(RF) ESD保護電路的主要考量，低寄生電容可達到5G寬頻通訊的規格，然而，對於在RF應用下，縮小寄生電容值同時增加ESD耐受度為設計上一大挑戰。另一方面，近年來氮化鎵(GaN)電晶體元件應用在射頻功率放大器電路引起了相關ESD設計討論，其中矽基氮化鎵(GaN-on-Si)製程可提供低成本之異質整合，加上晶圓級(wafer-level)3D封裝技術的引入，使GaN-on-Si製程能與CMOS製程進行進階的異質整合，也因此wafer-level元件充電模型(CDM)之ESD測試機台的發展近年來也受到業界很大的關注。此篇博士論文涵蓋了以下主題: (1) CMOS ESD保護元件優化設計 (2) 人體放電模型(HBM)在GaN-on-Si電晶體元件上之放電機制 (3) wafer-level CDM測試機台校正與模擬。

首先，本論文第三章研究在CMOS製程下之5G寬頻ESD保護電路，其中一種設計是將distributed ESD保護電路架構之第一級(first-stage)二極體元件整合在輸入/輸出焊墊底下(under I/O Pad)，此架構能夠提供更高ESD耐受度卻同時犧牲了RF操作頻寬。經過本論文研究發現，此架構在28奈米CMOS先進製程下之金屬間寄生電容(BEOL capacitance)佔據了整體ESD二極體元件寄生電容高達53%，因此本章節提出使用tapered金屬佈局優化的方式實現在ESD二極體上以降低BEOL capacitance，同時透過此金屬佈局能夠增強元

件ESD耐受度，最後將此tapered金屬架構整合電感等元件組成distributed ESD保護電路，透過SPICE模擬驗證此tapered金屬架構相對於原本無優化之金屬佈局可增進2-GHz頻寬，適合應用在5G寬頻RF ESD保護電路設計。

另外，本論文第四章在GaN-on-Si製程下使用TLP與HBM量測機台，主要在兩種電晶體(HEMT與MIS-HEMT)的汲極端(drain)進行HBM轟擊測試。首先在drain端測試中驗證了MIS-HEMT與HEMT主要透過GaN電晶體之2DEG通道釋放ESD電流，接著首次提出了在drain端測試中有ESD耐受度出現匹配誤差之現象(HBM-TLP mis-correlation)。因此，本章節透過了元件的HBM暫態電流電壓(transient I-V)量測波形，搭配TCAD與SPICE模擬結果，推導出了GaN電晶體獨特的HBM放電機制與模型，並解釋了HBM-TLP mis-correlation根本原因是來自於電晶體在飽和區操作時之2DEG通道電阻調變效應(2DEG resistance modulation)，因此在電晶體操作在飽和區時，需額外考慮元件在ESD放電路徑上的高通道電阻，才能避免HBM-TLP mis-correlation之誤差。最後透過本章節研究結果，可正確得到GaN電晶體元件之ESD耐受度，並提供未來將此GaN電晶體元件整合在GaN全晶片ESD保護電路設計的方向。

最後，本論文第五章針對近年來開發的wafer-level低阻抗(low-impedance)接觸式(contact) CDM (LI-CCDM)機台，使用了Vector Network Analyzer (VNA)進行量測機台參數之校正與使用SPICE模擬進行波形比對，本章節首次提出了LI-CCDM機台之等效電路模型，並驗證此模型能適用在不同大小的金屬校正片(DUT)，以提供CDM電流波形優化，並能進一步對CDM測試規範標準(JS-002)進行匹配，使本機台能與傳統電場感應式機台(Field Induced CDM tester)並存，提供未來wafer-level CDM測試需求。

總結來說，本論文研究涵蓋了現今5G/B5G次世代通訊規格下之ESD重要技術內容，包含在矽與三五族製程下RF ESD保護元件之探討與應用在3D異質整合技術之wafer-level CDM機台發展。本博士論文之研究內容，累計已發表兩篇*IEEE Transactions on Electron Devices*期刊論文，以及四篇國際會議論文(包含一篇IEDM頂尖國際會議論文)。

關鍵字: 1.氮化鎵 2.人體放電模型 3.電晶體 4.二極體 5.射頻 6.元件充電模型

RF ESD Exploration in Si/III-V Heterogeneous Integration for 5G/B5G Applications

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Abstract

When moving to the 5G telecommunication era, higher data rate and thus higher bandwidth are the main requirements to enable this evolution. For RF ESD protection design in traditional CMOS front-end module (FEM) circuits, the parasitic capacitance of the ESD protection devices should be as low as possible to meet the 5G bandwidth requirements. However, it is usually challenging to reduce the parasitic capacitance without sacrificing the ESD performance.

On the other hand, power efficiency of an RF power amplifier (PA) is critical to enhance the overall RF performance. In order to increase the power efficiency of the PA circuits, Gallium Nitride (GaN)-on-Si technology is consequently proposed to design the PA circuit in 5G communication systems. This technology can provide better high-power and high-frequency performances and a low-cost integration with the scaling CMOS process. The GaN PA eventually should be integrated with other CMOS FEM circuits by novel wafer-level heterogeneous integration techniques. When introducing the emerging GaN-on-Si technology and advanced integration techniques, ESD reliability evaluations should be adapted in order to provide appropriate ESD protection methods and evaluation tools in the specific technology.

In this work, first of all, a new tapered back-end-of-line (BEOL) layout structure was proposed and realized in an ESD diode under I/O pad for the RF ESD co-optimization in

advanced 28nm CMOS technology. Eventually, the improvement of the structure can be applied in a broadband ESD distributed protection network to enhance overall bandwidth at the 5G frequency bands.

Also, the ESD Human-Body Model (HBM) discharge model in GaN (MIS)-HEMTs is investigated, and it was found that under the HBM stress at the drain terminal, the HBM conduction path is related to the Two-Dimensional Electron Gas (2DEG) channel conduction, and that the HBM failures show a mis-correlation with the Transmission-Line-Pulse (TLP) test results. By the measured HBM transient I-V characteristics, the special HBM discharge mechanism of the 2DEG resistance modulation is revealed in both GaN MIS-HEMTs and HEMTs to explain the root cause of the HBM-TLP mis-correlation. Finally, the revised HBM correlation is derived with the consideration of the high 2DEG resistance in the saturation mode of the transistors.

In the last part of the thesis, a wafer-level Low-Impedance Contact Charged Device Model (LI-CCDM) tester is proposed for the potential ESD CDM issues in the advanced heterogeneous integrations. This LI-CCDM tester model is calibrated and verified by Vector Network Analyzer (VNA) measurements and SPICE simulations. Eventually, the parameters of the model can provide the instructions to optimize the LI-CCDM setup and to correlate to the JS-002 standard.

In conclusion, this thesis covered state-of-the-art issues of the 5G/B5G RF ESD strategies in the Si/III-V technology options and the development of the wafer-level CDM evaluation tools for the advanced heterogeneous integrations.

Key words: 1. Gallium Nitride (GaN), 2. Human Body Model (HBM), 3. transistor, 4. diode, 5. Radio Frequency (RF), 6. Charged Device Model (CDM).

RF ESD-verkenning in Si/III-V Heterogene Integratie voor 5G/B5G-toepassingen

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Beknopte samenvatting

Bij de transitie naar het 5G telecommunicatietijdperk zijn een hogere datasnelheid en dus een hogere bandbreedte de belangrijkste eisen om deze evolutie waar te maken. Voor het ontwerp van RF ESD-bescherming in traditionele CMOS front-end module (FEM) circuits moet de parasitaire capaciteit van de ESD-beschermingstructuren zo laag mogelijk zijn om aan de 5G-bandbreedtevereisten te voldoen. Het is echter meestal een uitdaging om de parasitaire capaciteit te verminderen zonder de ESD-prestaties op te offeren.

Anderzijds is de vermogensefficiëntie van een RF-vermogensversterker (PA) van cruciaal belang om de algemene RF-prestaties te verbeteren. Om de energie-efficiëntie van de PA-schakelingen te verhogen, wordt de Gallium Nitride (GaN)-on-Si technologie voorgesteld voor het ontwerp van het PA-circuit in 5G-communicatiesystemen. Deze technologie kan zorgen voor betere prestaties met hoog vermogen en hoge frequentie en een goedkope integratie bij het schalen van het CMOS-proces. De GaN PA moet uiteindelijk worden geintegreerd met andere CMOS FEM-schakelingen door nieuwe heterogene integratietechnieken op waferniveau. Ten gevolge van de opkomende GaN-op-Si-technologie en de bijhorende integratietechnieken, moeten de ESD-betrouwbaarheidsevaluaties worden aangepast om te voorzien in passende ESD-beschermingsmethoden en evaluatie-instrumenten in de specifieke technologie.

In dit werk wordt vooreerst een nieuwe tapered back-end-of-line (BEOL) lay-out structuur

voorgesteld en gerealiseerd in een ESD-diode onder I/O pad voor de RF ESD co-optimalisatie in een geavanceerde 28nm CMOS technologie. Uiteindelijk kan de verbetering van de structuur worden toegepast in het breedband ESD-distributienetwerk om de totale bandbreedte op de 5G-frequentiebanden te verhogen.

Verder wordt het ESD Human Body Model (HBM) ontladingsmodel in GaN (MIS)HEMT's bestudeerd en er wordt vastgesteld dat onder de HBM stress bij de drain terminal, het HBM-geleidingspad gerelateerd is aan de Two-Dimensional Electron Gas (2DEG)-kanaalgeleiding, en dat de HBM-falers leiden tot de HBM mis-correlatieproblemen tussen de TLP-testresultaten. Door de gemeten HBM transiënte I-V kenmerken kan een speciaal HBM-ontladingsmechanisme van de 2DEG weerstandsmodulatie onthuld worden, en dit zowel in GaN MIS-HEMT's als HEMT's. Op die manier kan de hoofdoorzaak van de HBM mis-correlatie verklaard worden. Tenslotte wordt de herziene HBM-correlatie afgeleid met inachtneming van de hoge 2DEG-weerstand in de verzadigingsmodus van de transistoren.

In het laatste deel van de thesis wordt een tester op waferniveau voorgesteld met een Lage Impedantie van het Contact Charged Device Model (LI-CCDM), voor de potentiële ESD CDM-problemen in de geavanceerde heterogene integraties. Het LI-CCDM tester model wordt gekalibreerd en geverifieerd door vector netwerk analyzer (VNA) metingen en SPICE simulaties. Uiteindelijk kunnen de parameters van het model de gebruikt worden om de LI-CCDM opstelling te optimaliseren en te correleren met de JS-002 standaard.

In conclusie, dit proefschrift behandelt de state-of-the-art kwesties van de 5G/B5G RF ESD strategieën in de Si/III-V technologie opties en de ontwikkeling van de wafer-level CDM evaluatie-instrumenten voor de geavanceerde heterogene integraties.

kernwoorden: 1. Gallium Nitride (GaN), 2. Human Body Model (HBM), 3. transistor, 4. diode, 5. Radio Frequency (RF), 6. Charged Device Model (CDM).