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博 士 論 文

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Doctoral Dissertation

互補式金氧半積體電路寄生閂鎖效應之探討與晶片上閂鎖防治創新方法之實現

Study on Latch-Up Events in CMOS Integrated Circuits and Latch-Up Prevention by Innovative On-Chip Solutions

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摘　要

由於寄生矽控整流器 (Silicon-Controlled Rectifier, SCR) 結構，閂鎖 (Latch-up) 問題一直是 CMOS 積體電路的固有問題，並且閂鎖狀態會導致不可恢復的晶片故障。隨著製造工藝尺寸的不斷縮小，以及更複雜的電路實現，如混合信號、多個電源、射頻(RF)、系統晶片(SoC)等，CMOS 元件所處的環境將更容易受到來自 IC 內部和外部的高雜訊/高電壓的影響。 此外，在一些惡劣的操作環境中，例如工業應用或車用電子，閂鎖規格要求一個更高的目標。 因此閂鎖問題是 CMOS 積體電路產品中的主要可靠性問題之一。 為了推廣積體電路產品，積體電路公司會為其 CMOS 積體電路產品製定比 JEDEC 標準更高的抗閂鎖干擾之規格。 因此，積體電路行業需要具有成本效益的解決方案來進一步增強閂鎖抗擾度。

在第二章中，用於植入式神經調節應用的電刺激電路需要在正電壓源和負電壓源下工作。為了允許電路在負電壓源下工作，CMOS 工藝中引入了深 n 阱 (Deep N-Well, DNW) 層，將負電壓元件與 p 型襯底隔離開來。為了防止閂鎖和/或降低雜訊，在晶片佈局中，接地的 P+擴散保護環通常畫在 DNW 層周圍。然而，從接地的 p+保護環(p+ GR)到負電壓源偏置的堆疊 NMOS (STnMOS)的 N+擴散的寄生閂鎖路徑可能會導致負電壓源工作的刺激電路存在閂鎖問題。該寄生閂鎖路徑的保持電壓 (Vh) 與 p+ GR 和 STnMOS 的 N+ 擴散之間的間距成正比，隨著 DNW 的隔離環連接到地的串聯電阻增加保持電壓也會下降。此外，當工作溫度升高時，保持電壓也會降低。

在第三章中，由於高壓 (HV) 和低壓 (LV) 電路被整合在同一個的矽襯底中，因此在佈局中間距有限的相鄰 HV 和 LV 電路之間的寄生閉鎖路徑將被觸發到閂鎖狀態，從而導致元件/電路出現不可恢復的故障。採用 0.18-μm HV 雙極 CMOS - DMOS (BCD)技術，提出並驗證了帶有蕭特基 (Schottky) 嵌入結的 HV N-Well (HVNW)/ n-BL(NBL)隔離環提升橫向 HV- to-LV 閂鎖路徑。從所提出的嵌入式蕭特基隔離環的實驗結果來看，蕭特基嵌入式隔離環可以提高橫向高低壓寄生閂鎖路徑的保持電壓(Vh)，使其大於相鄰高低壓電路不同電源之間的電壓差而避免閂鎖風險。因此，相鄰的高壓與低壓電路之間的佈局間距可以顯著減小，以節省晶片佈局面積。因此，提出的蕭特基嵌入式隔離環是一種具有成本效益的解決方案，可以在佈局距離較短的高壓到低壓電路塊之間提供良好的閂鎖免疫。

在第四章中，在 I/O PAD 上的元件必須被保護環包圍，這是由晶圓代工廠設計規則的規定，以克服 I/O PAD 上的閉鎖問題。當觸發電流被施加到 I/O PAD 上時，一部分觸發電流會從保護環中逃逸到矽襯底中，然後沿著內部電路塊流動，導致晶片內部發生的閂鎖問題。本論文提出了一種防止閂鎖發生的自動閂鎖檢測電路實現 I/O PAD 到內部電路的全晶片閂鎖防護，通過在 I/O PAD 和內部電路之間添加一個空穴/電子探測器，可以檢測到注入內部電路導致閂鎖的觸發電流。因此當異常電流從 I/O PAD 注入到內部電路時，該事件可以由所提出的自動檢測電路檢測到，接著自動檢測電路的輸出信號關閉內部電路供電的穩壓器。因此，內部電路中的寄生閂鎖路徑不會導通，從而避免內部電路燒壞故障。當閂鎖觸發電流消失時，穩壓器（電壓調節器）將恢復正常功能，為內部電路提供電源。通過這種提出的電路設計方法，不僅可以實現全晶片的閂鎖防護，而且可以進一步縮短 I/O PAD 與內部電路之間的距離，從而節省矽的面積。

第五章總結了本文的主要研究成果。本節還討論了擬議設計的未來工作和擴展。此外，有關論文已在國際刊物發表或提交。

關鍵字:閂鎖、矽控整流器、蕭特基嵌入式結、隔離環、I/O PAD、電路解決方案、保持電壓。

Study on Latch-Up Events in CMOS Integrated Circuits and Latch-Up Prevention by Innovative On-Chip Solutions

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Abstract

Latch-up issues have been an inherent concern with bulk CMOS ICs due to the parasitic silicon-controlled rectifier (SCR) structure, and the latch-up state can result in unrecovered chip failure. As the development of the manufacturing process size continues to shrink, and more complicated circuitry implementations, such as mixed-signal, multiple power supplies, Radio frequency (RF), system on a chip (SoC), and so on, the environment in which CMOS devices are located will more easily suffer from a high level of noise from both the interior and exterior of ICs. What's more, in some harsh environments, such as industrial applications or automotive applications, the latch-up specification is required to be a higher target. Latch-up is indeed one of the primary concerns regarding the reliability of CMOS IC products. To promote IC products, IC manufacturers may have even stricter specifications than the JEDEC standard for CMOS IC latch-up immunity levels. Hence, cost-efficient solutions are required by the IC industry to further enhance latch-up immunity.

In Chapter 2, the electrical stimulation circuits for implanted neuro-modulation applications were designed to operate with both positive and negative voltage sources. To allow circuit operation with a negative voltage source, a deep n-well (DNW) layer has been introduced to the CMOS process to isolate the negative-voltage devices from the p-type substrate. For latch-up prevention and/or noise reduction, the guard ring of grounded P+

diffusion is commonly drawn around the whole DNW layer in chip layout. A parasitic latch-up path from the grounded p+ guard ring (p+ GR) to the N+ diffusion of the stacked-nMOS (STnMOS) biased at negative voltage source in a DNW may cause a latch-up issue in stimulation circuits operating with negative voltage sources. The holding voltage (Vh) of such a parasitic latch-up path is proportional to the spacing between the p+ GR and the N+ diffusion of STnMOS, as well as to the series resistance that connects the isolation ring of DNW to ground. Furthermore, the magnitude of Vh is decreased when the operating temperature is increased.

In Chapter 3, as the high-voltage (HV) and low-voltage (LV) circuits are integrated together in a common silicon substrate, the parasitic latch-up path between neighboring HV and LV circuits with limited spacing in layout would be triggered into latch-up state to cause unrecoverable failure in the chip. The isolation ring of HV n-well (HVNW) / N-buried layer (NBL) with Schottky-embedded junction to overcome the lateral HV-to-LV latch-up path was proposed and verified in a 0.18μm HV bipolar-CMOS-DMOS (BCD) technology. From the experiment results of the proposed Schottky-embedded isolation ring, the holding voltage (Vh) in the lateral HV-to-LV parasitic latch-up path can be increased to be greater than the voltage difference between the different power supplies of the neighboring HV and LV circuits. Furthermore, the layout spacing between the neighboring HV and LV circuits can be significantly reduced to save chip area. The proposed Schottky-embedded isolation ring is a cost-effective solution to provide good latch-up immunity among the HV-to-LV circuit blocks with a short layout distance.

In Chapter 4, the devices located at the I/O pads must be surrounded by guard rings, as specified by the design rules of the foundry, to overcome the latch-up issues at the pads. When the trigger current was injected to the I/O pad, several portions of the trigger current would escape from the guard rings into the common substrate, and then flow toward the internal core circuit to induce latch-up failure inside the chip. In a 0.18-μm 1.8/3.3-V CMOS technology, a

novel design of an auto-detector circuit to stop latch-up occurrence for latch-up prevention was proposed and successfully verified. By adding a hole/electron detector between I/O pads and internal circuits, the latch-up trigger current injected toward the internal circuits can be detected. When an abnormal current is injected from the I/O pads to the internal circuits, this event can be detected by the proposed auto-detector circuit. The output of the auto-detector circuit is used to shut down the voltage regulator which supplies the power to the internal circuits. Thus, the latch-up current in the internal circuits can be fully stopped to avoid the burned-out failure. When the latch-up trigger current disappears, the voltage regulator will return back to its normal function to supply the power for internal circuits. With this proposed method of circuit design, the whole-chip latch-up prevention can be fully achieved. Moreover, the distance from I/O cells to the internal circuits can be further reduced to save the silicon area.

Chapter 5 summarizes the main results of this dissertation. Future work and the expansion of the proposed designs have also been discussed in this section.

Additionally, the relevant papers have been published or submitted to a number of international publications.

Key words: Latch-up, Silicon-Controlled Rectifier (SCR), Schottky embedded junction, Isolation ring, I/O pad, Circuit Solution, Holding voltage.