Master Thesis

Design of On-Chip Decoupling Capacitor Against CDM ESD and Investigation of CDM Protection Capability Among Power-Rail ESD Clamp Circuits

對抗元件充電模式靜電放電之去耦電容設計與靜電放電箝制電路對元件充電模式防護能力調查

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摘要

電源雜訊抑制與靜電放電防護設計隨著製成演進，逐漸成為在設計晶片時不可忽視的重點。隨著製程技術的進步，電路能操作在更高的頻率和更低的電源供應環境。電壓源(Power Supply)也因此對電源線(Power Lines)上由連接至封裝(Package)的打線(Bonding Wires)之寄生電感(Parasitic Inductance)所產生的暫態/切換雜訊(Transient/Switching Noise)非常敏感。最常被用來抑制電源雜訊的方法，便是在晶片上加入去耦電容(Decoupling Capacitor)；同時，靜電放電事件對積體電路可靠度上無非是個棘手的挑戰；對於由先進製程製作出的積體電路產品，越薄的閘極氧化層(Gate Oxide)在面對元件充電模式(Charged- Device Model)靜電放電事件時特別容易受到損傷。除了對主電路造成傷害，也可能會衝擊到搭配的去耦電容以至於無法發揮去耦電容抑制雜訊的功能；並且在整個晶片中，也都會加上電源箝制電路(Power-rail ESD clamp circuits)去保護內部電路避免靜電放電事件的破壞。

在本次論文中進行兩個部分的研究；第一部分為對不同架構的去耦電容進行對元件充電模式靜電放電事件的耐受度調查，並提出強化對元件充電模式靜電放電事件耐受能力的去耦電容設計且使用無晶片插座之元件充電模式靜電放電測試(Non-Socket Field Induced CDM ESD Stressing)進行驗證。第二部分為對不同架構的電源箝制電路進行元件充電模式靜電放電事件的耐受能力研究，除了與主電路一同整合在晶片上進行元件充電模式靜電放電測試進行驗證以外，同時也對獨立(Stand-Alone)的電源箝制電路進行極快速傳輸線觸波(Very-Fast Transmission Line Pulse)測試。透過量測其相關參數如電路的二次崩潰電流(I_{t2})，電路導通時間(Voltage clamping-down time)等來探討不同結構下電源箝制電路對元件充電模式靜電放電事件的防護能力。

關鍵詞/字 — 電源雜訊、去耦電容、電源箝制電路、元件充電模式靜電放電事件、極快速傳輸線觸波

Abstract

Power-line noise suppression and electrostatic discharge protection design have gradually become the key points that cannot be ignored while chip designing under advanced process technology. The integrated circuits fabricated in the scale-down CMOS processes are able to operate with a higher clock rate and lower power supply voltage. Therefore, the power supply sources are more sensitive to the transient/switching noise induced by the parasitic inductance of bonding wires connecting the power lines to the package. The most commonly used method to suppress power-line noise is adding on-chip decoupling capacitors. Meanwhile, electrostatic discharge (ESD) events are very challenging issues for the reliability of integrated circuits. For the integrated circuit products fabricated in advanced processes, the circuits are particularly vulnerable to the charged-device model (CDM) electrostatic discharge event with thinner gate oxide. Not only do cause damage to the main circuits but may also impact the added-in decoupling capacitors so that the decoupling capacitors are not able to serve the purpose of noise suppressing. Furthermore, the power-rail ESD clamp circuits will also be added to protect the internal circuits from failure caused by electrostatic discharge events.

The study can be divided into two parts in this work; the first part of the study is to investigate the CDM ESD tolerance among decoupling capacitors with different structures. The new design of decoupling capacitor is proposed to strengthen the CDM robustness and verified with non-socket field induced CDM ESD stressing. The second part of this work is the research on CDM robustness among power-rail ESD clamp circuits with different structures. In addition, to be integrated with the main circuits on the chip and verified with CDM ESD testing, the very-fast transmission line pulse stressing is performed on the stand-alone splits of power-rail ESD clamp circuits. Through the measurement of ESD-related parameters such as the secondary breakdown current (I_{t2}) and the Voltage clamping-down time of the testing circuits, the protecting capability of power-rail ESD clamp circuits against CDM ESD events is investigated.

Keywords – Power-Line Noise, Decoupling Capacitors, Power-Rail ESD Clamp Circuits, Charged-Device Model Electrostatic Discharging Event (CDM ESD Event), Very-Fast Transmission Line Pulse.