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Master Thesis

應用於即時閉迴路深腦電刺激系統晶片具輸入阻抗提升輔助路徑、改善差模偽影訊號消除及改善單極電極組織阻抗量測電路之互補式金氧半局部場電位類比前端放大器設計

Design of CMOS Analog Front-End Local Field Potential (LFP) Amplifier with Input Impedance Boosting Auxiliary Path, Improved Differential-Mode Artifact Removal, and Improved Monopolar Electrode-Tissue Impedance Measurement Circuits for Real-Time Closed-Loop Deep Brain Stimulation (DBS) SoC Applications

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摘要

本論文介紹了一個應用在即時閉迴路深腦電刺激系統晶片的類比前端放大電路，並具有單極電極組織阻抗量測電路。在測試晶片的類比前端放大器方面，為了讓電路有更低的雜訊，第一級放大電路使用載波調變技術來移除電路本身在低頻的閃爍雜訊。為提升類比前端放大電路的輸入阻抗，在本電路中使用改善的輔助路徑，以消除載波調變器在切換相位時造成的非理想效應，並在改善的輔助路徑中，使用改善的動態時脈電平轉換器控制載波調變器的時脈訊號來傳輸負偽影訊號到電路內部。在本電路中採用了改善的右腳驅動電路，並取樣軌到軌輸入放大器的輸入電壓回授到人體，以消除市電雜訊，並進一步提升共模抑制比。在消除差模偽影訊號上，此電路使用了類比模板消除技術，設計了一個改善的差模偽影訊號消除電路來消除電極不對稱產生的差模偽影雜訊，並調整差模偽影訊號消除電路中的電容陣列大小，提升差模偽影訊號消除範圍。為了壓抑共模偽影訊號，電路使用改善的動態時脈電平轉換器搭配由I/O元件組成的載波調變器來完整的將帶有偽影訊號的局部場電位訊號傳送到核心電路端。改善的動態時脈電平轉換器中使用了電平轉換器，由-3伏產生-1.8伏的時脈訊號，來傳輸-1.2伏的共模偽影訊號。當共模偽影訊號進入內部電路後，再透過場效電晶體組成的二極體搭配高輸入電壓範圍的訊號放大器來維持後端核心放大器的運作。此放大器採用了有兩個電流補償電路的軌到軌輸入放大器來達到較大的輸入範圍並維持訊號線性度。在第一級電路後，本設計使用了開關電容低通濾波器和開關電

容放大器來選擇通道並提供可調變的增益及低通頻寬。

此類比前端放大器電路使用台積電0.18-μm CMOS混訊/射頻製程技術。輸入阻抗在不同增益下於112Hz頻寬內皆能大於133MΩ，並在DC時達到8.2GΩ。共模拒斥比於60Hz可以達到144dB。總諧波失真在沒有刺激的情況下為0.33%，有±1-V共模和±50-mV差模偽影訊號的情況下為1.28%。在洋菜膠量測中，沒有刺激時的總諧波失真為1.25%，使用±2.2-V定電壓刺激以及±1.6-mA定電流刺激的總諧波失真分別為1.84%和1.69%，都小於規格所訂定的2%。

本論文所提出的改善的單極電極組織阻抗量測電路於測試晶片以及單晶片系統中可以量測單極到地的阻值。為了減少量測單極到地的阻值誤差，在本電路中，使用了源極耦合對電流切換技術，減少電流切換時造成的偏移，並在阻抗量測模式時，類比前端放大器工作於低增益模式，讓電流切換時造成的偏移不會被開關電容低通濾波器和開關電容放大器放大。由於類比前端放大器的輸出偏移較小，本電路可以藉由量測輸出峰值來得到單極的電極組織阻值。在單晶片系統中，考慮電極端於實際應用上會有電極直流漂移，因此於單極電極組織阻抗量測電路中，保留了更長的重置時間讓電極直流漂移穩定。

改善的單極電極組織阻抗量測電路在測試晶片中，量測到的阻值誤差範圍是-7.4% - 7.1%，需要的額外功耗為3.16μW。改善的單極電極組織阻抗量測電路在單晶片系統中，考慮了電極上的電極直流漂移，量測到的阻值誤差範圍是-8.8% - -0.8%，需要的額外功耗為3.63μW。

關鍵字: 類比前端放大器、深腦電刺激、局部場電位訊號、單極電極組織阻抗量測、即時刺激偽影訊號消除。

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Abstract

This paper presents an analog front-end (AFE) amplifier circuit with improved monopolar electrode-tissue impedance (ETI) measurement circuits for real-time closed-loop deep brain stimulation (DBS) SoC applications. In test chip, the auto-reset capacitively-coupled chopper instrumentation amplifier (AR-CCCIA) is used to amplify LFPs and suppress flicker noise. The improved auxiliary path is adopted to obtain a higher input impedance. It can handle negative artifact voltages because the improved dynamic clock level shifter is applied on the choppers in the improved auxiliary path to transmit negative artifact voltages to the internal circuits. The improved right-leg driven (RLD) circuit connected to the input of rail-to-rail input folded-cascode (RRFC) amplifier is adopted to suppress 60-Hz power line interference and obtain a higher common-mode rejection ratio (CMRR). An improved differential-mode artifact

cancellation loop (DMACL) is adopted to remove differential-mode artifact voltage (DMAV) for real-time closed-loop DBS application. The size of the capacitor array in the improved DMACL is optimized to achieve a higher DMAV removal range. Improved dynamic clock level shifter and input chopper that consists of I/O devices are employed to transmit the large common-mode artifact voltage (CMAV) to the internal circuit. Clock level shift circuit is employed to generate a clock voltage level of -1.8V from -3V so that it can transmit -1.2-V CMAV to the internal circuit. After the CMAV enters the internal circuit, clamping diodes and core amplifier with high input common-mode range are also applied to resist the common-mode variations caused by CMAV. The first-stage amplifier employs a RRFC op-amp with two current compensation circuits to achieve a large input range while maintaining the linearity of the signal. After the AR-CCCIA, the switched-capacitor (SC) low-pass filters (LPFs) and SC amplifier (SC-Amp) are then adopted to select channels and provide tunable gains and low-pass corners.

The AFE amplifier circuit is fabricated in TSMC 0.18-um CMOS mixed-signal/RF process. The input impedance under different gains are larger than 133MΩ within 112Hz bandwidth and 8.2GΩ at DC. The CMRR of AFE amplifier with improved RLD circuit is 144dB at 60Hz. The measured THD is 0.33% without stimulation and 1.28% with ±1-V CMAV and ±50-mV DMAV. In the agar test, the THD of the AFE amplifier without stimulation is 1.25%. The THD of the AFE amplifier with ±2.2-V, 130-Hz, and 60-μs pulse width constant voltage stimulation is 1.84%, and the THD of the AFE amplifier with ±1.6-mA, 130-Hz, and 60-μs pulse width constant current stimulation is 1.69%, which is both smaller than 2%.

The proposed improved monopolar ETI measurement circuit in test chip and SoC are both able to measure the monopolar impedance value. To reduce the measurement errors of the measured monopolar impedance values, a source-coupled pair current switching circuit is adopted to minimize the offset voltages caused by current switching, and low gain mode in AFE

amplifiers is used during ETI measurement so that the offset voltages are not amplified by the SC circuit. With small output offset voltages of AFE amplifiers, output peak voltages instead of output peak-to-peak voltages of the AFE amplifiers are measured during ETI measurement. In SoC, the electrode DC offset (EDO) is considered in the equivalent RC circuit of ETI. A longer reset period is reserved in the improved monopolar ETI measurement circuit for EDO settling.

In test chip, the error range is -7.4% - 7.1% with extra power consumption 3.16μW. In SoC with the consideration of EDO, the error range is -8.8% - -0.8% with extra power consumption 3.63μW.

Keywords: analog front-end (AFE) amplifier, deep drain stimulation (DBS), local-field potential (LFP), monopolar electrode-tissue impedance (ETI) measurement, real-time stimulation artifact removal.