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碩士論文

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National Yang Ming Chiao Tung University

Master Thesis

BCD 製程之高壓浪湧防護元件架構改良以及高壓栓鎖特性調查

Improved Device Structure for HV Surge Protection and Investigation of HV Latch-Up Immunity in BCD Process

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摘　　要

近年來，高壓晶片應用領域取得了巨大的發展，成為電子產業中一個關鍵的技術驅動力。這種趨勢包括了眾多的應用領域，例如高壓功率轉換器、驅動面板、以及汽車電子系統等。雖然高壓晶片有著許多優勢，其製程複雜度也造成量產上可靠度的問題，此次研究將專注在高壓領域中常發生的兩個靜電防護難題，浪湧 (Surge) 以及閂鎖 (Latch-up) 事件。

隨著高壓晶片的廣泛應用，浪湧防護設計變得至關重要。浪湧事件可能源於突發性的電壓浪湧或電流浪湧，例如雷擊、電磁干擾或操作中的突然變化，這種情況下，高壓晶片需要有效的保護，以避免損壞或故障。USB 高壓應用更是一個明顯的示例，因為可插拔特點使其特別容易受到浪湧危害，因此 USB 介面上需要嚴格的浪湧防護設計，本篇對晶圓廠提供之高壓積體電路靜電放電防護元件—PNP 雙載子接面電晶體 (PNP BJT) 做出改良架構，提升此元件的浪湧耐受度，為 USB 高壓快充介面提供浪湧防護，以確保穩定和可靠的性能。

此外，高壓晶片應用還面臨另一種潛在的挑戰，即閂鎖問題。閂鎖事件是指積體電路中的寄生矽控整流器 (SCR) 被意外觸發後，會在電源端和接地端會形成一個低阻抗的路徑，形成大量電流。高壓閂鎖事件已經在一些高壓應用中引起了關注，本次將研究不同電源域間所發生的閂鎖問題，以及深溝隔離（DTI）對於閂鎖事件的影響。

關鍵字: 靜電防護、浪湧、PNP BJT、閂鎖、深溝隔離

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Abstract

In recent years, the field of high-voltage (HV) applications has witnessed significant growth, becoming a pivotal technological driver within the electronics industry. This trend encompasses various application areas, including HV power converters, display panels, and automotive electronic systems, among others. While HV integrated circuits (ICs) offer numerous advantages, their complex manufacturing processes pose challenges in terms of production reliability. This research focuses on two common electrostatic discharge (ESD) protection challenges in the HV domain, surge and latch-up events.

With the widespread adoption of HV IC, surge protection design has become crucial. Surge events can result from sudden voltage or current surges, such as lightning strikes, electromagnetic interference, or abrupt operational changes. In such scenarios, HV chips require effective protection to prevent damage or malfunction. A prominent example of surge protection requirement is in USB HV applications, where the hot-plug characteristic makes it particularly vulnerable to surge-related hazards. As a result, stringent surge protection designs are required for USB interfaces. This study improves the structure of HV ESD protection component provided by foundry, the PNP BJT to enhance its surge immunity and provide surge protection for USB HV power delivery interfaces, ensuring stable and reliable performance.

Furthermore, HV applications face another potential challenge, latch-up events. Latch-up events occur when parasitic silicon-controlled rectifiers (SCR) within the IC are unintentionally triggered, creating a low-impedance path between the power supply and ground, leading

to substantial current flow. HV latch-up events have garnered attention in some high-voltage applications. This study investigates latch-up problems occurring between different power domains and the impact of deep trench isolation (DTI) on latch-up events.

Key words: ESD, Surge, PNP BJT, Latch-up, DTI