國立陽明交通大學

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博 士 論 文

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Doctoral Dissertation

應用於即時有效控制帕金森氏症具電刺激偽影訊號消除互補式金氧半局部場電位類比前端放大器與閉迴路深腦電刺激系統晶片之設計

Design of CMOS Analog Front-End Local Field Potential (LFP) Amplifiers with Stimulation Artifact Removal and Closed-Loop Deep Brain Stimulation (DBS) System-on-Chip (SoC) for Real-Time Efficient Control of Parkinson's Diseases (PDs)

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摘 要

本篇論文共提出了兩個具即時電刺激偽影訊號消除能力的放大器電路設計，以及一個由可充電電池供電針對帕金森氏症進行即時有效閉迴路控制的植入式系統單晶片。第二章中提出了一個具有即時電刺激偽影訊號消除功能的同步取樣保持電刺激偽影訊號阻隔（SSAB）類比前端局部場電位擷取單元，同時還提出了右腳驅動電路以提升共模雜訊抑制能力，以及單極電極-組織阻抗測量電路。所提出的擷取單元由台積電 0.18-微米互補式金氧半（CMOS）製程製作並整合於系統單晶片。在±3.6 伏、130 赫茲電刺激情況下，製作之擷取單元中的切換式電容放大器輸出端所量測到的總諧波失真（Total Harmonic Distortion, THD）為 1.12%。加上右腳驅動電路後，量測信號頻帶中的共模雜訊抑制比（CMRR）為 124 – 145 dB。設計的單極電極-組織阻抗測量電路在額外功耗為 2.65 微瓦的情況下，測量誤差小於 8.3%。

第三章中，設計了一個具有電刺激偽影訊號耐受性的類比前端局部場電位載波調變放大器電路，使用了類比模板去除方法來消除共模偽影電壓和差模偽影電壓以在刺激期間獲得良好的信號線性度，此外亦提出了改進的輸入阻抗增強輔助路徑、改進的右腳驅動電路以及改進的單極電極-組織阻抗測量電路。通過改進的輔助路徑，量測的輸入阻抗在信號頻帶大於 133 MΩ，直流輸入阻抗則達到 8.2 GΩ。加上改進的右腳驅動電路，在信號帶寬中測得的 CMRR 為 131 – 144 dB。在 60-微秒脈衝寬度和 130-赫茲固定電流刺激下，製作之類比前端局部場電位載波調變放大器中的切換式電容放大器輸出端所量測到的總諧波失真為 1.28%。改善的單極電極-組織阻抗測量電路在額外功耗為 3.16 微瓦的情況下，測量誤差小於 7.4%。

第四章中，設計並整合了 16 通道的 SSAB 類比前端局部場電位擷取單元、即時閉迴路控制生物訊號處理器、16 通道單極雙模式電刺激器，以及包括了電池功率管理單元和改進的線性電池充電器的無線雙向資料與電源傳輸電路於系統單晶片中。生物訊號處理器中實現了以 beta 頻帶中峰值功率頻率的±3 Hz 窄頻帶內的平均能量作為生物標記的閉迴路控制演算法。該單晶片系統是在 0.18 微米 CMOS 技術中製作的，晶片面積為 19.67 平方毫米。單晶片系統在電刺激模式下的平均功耗為 7.39 毫瓦。將製作的系統單晶片與圖形化用戶界面整合，形成了可應用於動物實驗的閉迴路深腦電刺激系統，並在藥物誘發帕金森氏症症狀的豬隻身上成功進行了活體內動物實驗，驗證了所製作之系統單晶片的即時閉迴路功能，並可適用於即時高效控制帕金森氏症。

關鍵字— 類比前端局部場電位放大器、單極電極組織阻抗量測、即時電刺激偽影訊號消除、即時閉迴路深腦電刺激系統單晶片、植入式生醫裝置、活體動物實驗、帕金森氏症。

Design of CMOS Analog Front-End Local Field Potential (LFP) Amplifiers with Stimulation Artifact Removal and Closed-Loop Deep Brain Stimulation (DBS) System-on-Chip (SoC) for Real-Time Efficient Control of Parkinson's Diseases (PDs)

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Abstract

In this dissertation, two analog front-end (AFE) local-field potential (LFP) amplifier circuits with real-time artifact removal and an implantable closed-loop deep brain stimulation (DBS) SoC powered by a rechargeable battery are proposed for real-time efficient control of Parkinson's diseases (PDs). In chapter 2, a synchronized sample-and-hold stimulation artifact blanking (SSAB) AFE LFP acquisition unit with real-time artifact removal, right-leg-driven (RLD) circuit and monopolar electrode-tissue impedance (ETI) measurement circuit is designed and fabricated in TSMC 0.18-um CMOS technology. Under ±3.6V, 130-Hz stimulation, the measured total harmonic distortion (THD) at the SC amplifier output of fabricated acquisition unit is 1.12%. With the RLD circuit, the measured CMRR is 124 – 145 dB in the signal bandwidth. The fabricated monopolar ETI measurement circuit has a measurement error less than 8.3% with an extra power consumption of 2.65 μW.

In Chapter 3, a CMOS AFE LFP chopper amplifier is designed with analog template artifact removal method to achieve good signal linearity during stimulation. Input impedance boosting auxiliary path, improved RLD circuit and improved monopolar ETI measurement circuit associated with the chopper amplifier are also proposed. With the improved auxiliary path, the measured input impedance is larger than 133 MΩ in the signal bandwidth and reaches 8.2 GΩ at DC in the fabricated AFE LFP chopper amplifier. The measured CMRR is 131 – 144 dB in the signal bandwidth. Under 60-μs pulse width and 130-Hz constant current stimulation with ±1-V CMAV and ±50-mV DMAV, the measured THD at the amplifier output is 1.28%. The improved monopolar ETI measurement circuit has a measurement error less than 7.4% with an extra power consumption of 3.16 μW.

In chapter 4, the 16-channel SSAB AFE LFP acquisition unit with artifact tolerance, a real-time closed-loop control bio-signal processer (BSP), a 16-channel monopolar dual-mode stimulator, and a wireless bidirectional data and power telemetry including a battery power management unit were designed and integrated in the proposed SoC. The closed-loop control algorithm with the averaged power over the narrow band of ±3 Hz around the peak-power frequency in the beta-band as a biomarker are implemented in the BSP. The proposed SoC was fabricated in a 0.18-μm CMOS technology with the chip area of 19.67 mm^2. The measured averaged power consumption of the SoC in the stimulation mode is 7.39 mW. The fabricated SoC is integrated with the graphical user interface (GUI) to form a closed-loop DBS system for animal tests. I*n-vivo* animal experiments on mini-pigs with induced PD symptoms have been performed successfully to verify the real-time closed-loop functions of the fabricated SoC. The proposed closed-loop DBS SoC is suitable for real-time efficient control of PDs.

Keywords— analog front-end local-field potential amplifier, monopolar electrode-tissue impedance measurement, real-time stimulation artifact removal, real-time closed-loop deep barin stimulation system-on-chip, implantable biomedical device, in-vivo animal test, Parkinson's disease.