國立陽明交通大學

前瞻半導體研究所

博 士 論 文

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Doctoral Dissertation

特定應用積體電路之靜電放電防護與閂鎖防治的可靠度優化設計

Reliability Optimization on ESD Protection and Latch-Up Prevention in Application Specific Integrated Circuits

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摘　要

因為各式各樣實際應用上的需求，積體電路的功能與規格也更多樣化，IC 設計公司紛紛提出高度客製化的積體電路產品，以搶佔甚至獨佔市場。這種客製化應用的積體電路，除了特定的電性功能之外，也經常被要求需具備高水平的可靠度，其中靜電放電耐受能力 (ESD robustness) 與閂鎖免疫能力 (Latch-up immunity) 更是高度競爭下各廠家比價殺價的重要指標。因此，特定應用積體電路之靜電放電防護與閂鎖防治可靠度的提昇與優化，是極具產業應用價值的重要技術。

本論文針對積體電路 (IC) 中靜電放電 (ESD) 和栓鎖效應 (Latch-up) 的可靠性挑戰進行深入探討。由於積體電路應用和規格的多樣性，ESD 和 Latch-up 問題必須針對特定的應用需求進行「因地制宜」的設計，而非統一標準。本論文共有七個章節，各章節間的研究背景差異性較大，主要在探討各種特定應用積體電路 (ASIC) 中可靠度之優化。第二、三章節專注於雙向靜電放電防護之解決方案，第四、五、六章節則集中於栓鎖效應免疫度的提升策略。各章節針對工業界實際遇到的問題進行了詳細研究與探討，並且都實作矽晶片來進行驗證。

在第二章中，本論文探討了針對高壓 FlexRay 應用設計的雙向 PNP (Bi-PNP) ESD 保護元件，並進行了設計優化以滿足±60V 的需求。此外，在第三章，本文提出並驗證了一個針對雙向 ESD 應用的創新電路設計，並在±20V 的應用下實作。這些設計不僅滿

足了特定應用需求，還在設計靈活性、尺寸縮小和多輸入應用適應性方面實現了顯著改進。

在栓鎖效應防護方面，第四章提出了 5V 耐壓輸入輸出電路應用中的嵌入式肖特基隔離環 (Schottky-Embedded Isolation Ring) 設計，避免了栓鎖風險。第五章則探討了多功能 I/O 緩衝器應用中的栓鎖故障模型，並提出使用嵌入式深 N 井集電極 (Deep N-well Collectors) 來提升栓鎖免疫力。最後，在第六章中，本文分析了線性穩壓器 (LDO) 在栓鎖效應電流測試 (I-test) 中導致的低壓核心電路過度電性應力 (EOS) 故障，並提出了深 N 井隔離的解決方案。

本論文強調了在特定應用積體電路 (ASIC) 中，以及高可靠度規格下，特殊客製化設計對產品成本、面積效益及防護效果的改善。第五、六章節透過產學合作計畫及工業界合作的實際案例，展示了學術界與工業界合作在解決高可靠度要求和實現量產目標中的重要性。通過產學合作，本研究不僅成功達成了高可靠度要求，也讓積體電路產品能夠達到工業界的量產標準，為積體電路的可靠度優化設計提供了寶貴的實踐經驗。

關鍵字： 靜電放電 (ESD)、栓鎖效應 (Latch-up)、積體電路 (IC)、雙向 ESD 保護、肖特基隔離環、深 N 井集電極、過度電性應力 (EOS)、半導體可靠度

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Abstract

Due to various practical application needs, the functionality and specifications of integrated circuits have become more diverse. Integrated circuits (IC) design companies have been proposing highly customized integrated circuit products to capture or even monopolize the market. These customized application-specific integrated circuits (ASICs), in addition to specific electrical functionalities, are often required to have a high level of reliability. Among these, Electrostatic Discharge (ESD) robustness and Latch-up immunity are critical benchmarks in the fierce competitive landscape. Therefore, improving and optimizing the reliability of ESD protection and Latch-up prevention in ASICs is a key technology with significant industrial application value.

This dissertation delves into the reliability challenges of ESD and latch-up in ICs. Given the diversity of IC applications and specifications, ESD and latch-up issues must be addressed with "tailor-made" designs for specific application needs, rather than a one-size-fits-all approach. The dissertation consists of seven chapters, each addressing different research backgrounds, primarily focusing on the reliability optimization of various ASICs. Chapters 2 and 3 focus on solutions for bidirectional ESD protection, while Chapters 4, 5, and 6 concentrate on strategies for enhancing Latch-up immunity. Each chapter thoroughly investigates and

addresses issues encountered in the industry, with silicon chip implementations for verification.

In Chapter 2, this dissertation explores the design and optimization of a bidirectional PNP (Bi-PNP) ESD protection device for high-voltage FlexRay applications, meeting the ±60V requirement. Additionally, in Chapter 3, an innovative circuit design for bi-directional ESD applications is proposed and verified, implemented under ±20V conditions. These designs not only meet specific application needs but also achieve significant improvements in design flexibility, size reduction, and adaptability for multi-input applications.

In terms of Latch-up protection, Chapter 4 proposes an embedded Schottky Isolation Ring design for 5V-tolerant I/O circuit applications to prevent Latch-up risks. Chapter 5 discusses Latch-up fault models in multi-function I/O buffer applications and proposes the use of embedded deep N-well (DNW) collectors to enhance Latch-up immunity. Finally, Chapter 6 analyzes excessive electrical overstress (EOS) failures in low-voltage core circuits caused by latch-up testing (I-test) in linear regulators (LDOs) and proposes a DNW isolation solution.

This dissertation emphasizes the improvement in product cost, area efficiency, and protective effects through specialized custom designs under high-reliability standards in ASICs. Chapters 5 and 6 showcase the importance of academia-industry collaboration in achieving high-reliability requirements and mass production goals, with practical case studies from industrial collaborations. Through such collaborations, this research not only successfully met high-reliability requirements but also enabled IC products to reach industry mass production standards, providing valuable practical experience for reliability optimization in IC design.

Keywords— Electrostatic Discharge (ESD), Latch-Up , Integrated Circuits (ICs), Bidirectional ESD Protection, Schottky Isolation Ring, Deep N-well Collector, Electrostatic Overstress (EOS), Semiconductor Reliability.