


國立交通大學

電子研究所

博士論文

生醫應用之具有電荷平衡和節能特性的高
壓共容刺激器電路設計與實現



Design of High-Voltage-Tolerant Stimulators
in Low-Voltage CMOS Process with
Charge-Balanced and Energy-Efficient
Properties for Biomedical Applications

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中華民國一〇六年五月

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A Dissertation

Submitted to Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering

May 2017

Hsinchu, Taiwan, Republic of China

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癲癇是種常見的神經疾病，因大腦某特定部位的異常放電而引起。大部分癲癇病人能夠採用藥物治療，但是有大約 30% 的病人具有耐藥性。因此具有監測腦電波功能的閉環式深腦層電刺激系統是一種新型研究的治療癲癇的方法。在設計深腦層電刺激的電路系統時，電路工程師將面臨諸如提高系統的集成度、效率、降低系統的成本、以及確保電脈衝刺激的安全性等問題的挑戰。

本論文提出了四種全新的方法來提升刺激器的集成度、電荷平衡度、電源效率以及降低系統尺寸和成本等關鍵性能指標。首先，介紹並分析了一種平滑電荷泵輸入電流的新方法。該方法能有效降低電源線上的濾波電容的容值，進而降低系統的尺寸。同時也可以降低系統的電磁干擾。本論文對此提出詳細的理論分析，結果顯示將三級電荷泵的每一級時鐘電路依次均勻錯開能最大化平滑電荷泵的輸入電流。基於這種新的方法，採用 0.18- μm 1.8-V/3.3-V 的 CMOS 製程設計了一個三級電荷泵電路。實際量測結果與傳統的時鐘電路的電荷泵相比，輸入電流的峰值減小了近 3 倍。

其次，本論文介紹並分析了一種全新的基於低壓器件的提升電路系統耐壓程度的方法。採用堆疊具有深 N 阱層的低壓器件可將電路系統的工作電壓提升到 12 V。再次，本論文介紹並分析了一種低功耗型高精度電荷平衡的方法。基於這兩種全新的方法，採用 0.18- μm 1.8-V/3.3-V 的 CMOS 製程設計了一個高壓共容的刺激器，試驗證實該電路在 12 V 電源電壓下能可靠的工作。採用低壓 CMOS 製程設計的刺激器能和微處理器、生醫信號處理器等集成在一個晶片上，提高系統的集成度，降低系統的尺寸。採用雙回路校準和漏電電流補償的電流記憶體能確保刺激器的電荷失配度小於 0.25%，搭配放電操作，殘留的直流電流小於 6.6nA。

此外，為了提高刺激器系統的效率，本論文介紹並分析了一種數位化的動態電源調整的方法。現有的電源動態調整電路中採用了很多的類比電路，例如衰減器、模數轉換器，放大器、比較器等等。採用這些類比電路會增加系統的佈局面積和功耗。相反地，本論文提出的全新的動態電源調整方法採用簡單的反相器對電流產生器的工作狀態進行監測，電荷泵的輸出由數位電路控制，整個回饋電路由數位電路構成。此方法能有效地降低系統的面積、功耗，且基於此方法，採用 0.18- μm 1.8-V/3.3-V 的 CMOS 製程成功設計了一個 16 通道的刺激器。測試結果表明這種動態電源調整方法能有效提升電源效率。

最後，設計的所有刺激器都完成了動物實驗。所設計的刺激器輸出的特定電刺激脈衝能有效地抑制動物癲癇的發作。

Design of High-Voltage-Tolerant Stimulators in Low-Voltage CMOS Process with Charge-Balanced and Energy-Efficient Properties for Biomedical Applications

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Abstract

Epilepsy is a group of neurological disorders resulting from excessive and abnormal discharges in the brain. Most epilepsy patients can be cured by the antiepileptic drugs (AEDs). However, approximately 30% of patients suffer from medically refractory epilepsy. Deep brain stimulation (DBS) therapy is a fairly new treatment for epilepsy and is being researched. A closed-loop DBS system that continuously monitors the brain's activity is an ongoing engineering technology. However, a circuit designer faces a number of challenges while designing a stimulator, such as the realization of high-level integration, the efficient power delivery to the stimulators, the delivery of the safe electrical stimulation, and the reduction of medical costs.

In this thesis, I have presented four new techniques to enhance some key specifications of stimulator such as enhancing the integration, reducing the size, improving the charge balance, and improving the power efficiency. First, a new technique for smoothing the charging current of charge pump is introduced and described. This technique is capable of reducing the smoothing capacitance in the power line, reducing the transient noise in the power supply line, and improving the electromagnetic emission (EME) behavior of the implantable devices. The theoretical analyses indicate that the charging current of 3-stage cross-couple charge pump can be smoothed greatly when the clock signals are separated averagely to each other. The

charge pump with this new clocking scheme has been designed and successfully verified in a 0.18- μm 1.8-V/3.3-V CMOS process. Experimental results show that the charging current ripples of the charge pump are reduced by a factor of three. In addition, the power efficiency is improved.

Second, a high-voltage-tolerant technique is introduced and described. The use of the stacked transistors with deep n-well layers made it possible to increase the operation voltage of the proposed stimulator to 12 V. Third, a precise charge-balanced technique is introduced and described. The stimulator with this new high-voltage-tolerant technique and precise charge-balanced technique has been designed and successfully verified in a 0.18- μm 1.8-V/3.3-V CMOS process. The reliability measurement results have verified that the proposed stimulator is robust. The stimulator can be fully integrated with the microcontroller or the biomedical signal processor into an SoC chip fabricated by using the LV CMOS technology for enhancing integration and reducing the size. The current memory cell with dual calibration loops and leakage current compensation ensures that the charge mismatch of stimulator is less than 0.25% and the residual average dc current is less than 6.6 nA with shorting operation.

Four, a digitally dynamic power supply technique for multi-channel stimulator is introduced and described. The existing stimulators with dynamic power supplies use too much analog circuits, such as attenuator, ADC, amplifier, comparator, which lead to large layout area and power dissipation. In contrast, the proposed digitally dynamic power supply technique examines the operating region (triode vs. saturation) of the current generator by a simple PMOS inverter. The output of the charge pump is driven by a digital input, eliminating the need of decision-making analogue circuits. High power efficiency is achieved by optimising the efficiency of each circuit module and using the adaptive power supply. A 16-channel 12V-tolerant stimulator with this digitally dynamic power supply technique has been designed and successfully verified in a 0.18- μm 1.8-V/3.3-V CMOS process. The experimental results have shown that the proposed new digitally dynamic power supply technique for multi-channel stimulator can greatly improve the power efficiency.

Final, the *in vivo* experiments verified that epileptic seizures could be suppressed by the electrical stimulation with certain stimulation parameters provided by the proposed stimulator.