國立交通大學

電子研究所

碩　士　論　文

用於植入式生醫應用之

多通道單端雙相電壓刺激器設計

Design of Multi-Channel Monopolar Biphasic Voltage Stimulator for Implantable Biomedical Applications

研 究 生：謝佳琪　　(Chia-Chi Hsieh)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國 一〇七年 六月

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中 華 民 國 一〇七 年 六 月

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摘要

腦中神經系統的不正常放電現象，可能會進一步影響運動神經，讓身體發生無法控制的抖動，像是帕金森氏症及癲癇等疾病，而世界上約有七千萬人口患有此類症狀。近年來，電刺激技術漸漸取代藥物治療，被用於醫療方面，透過在異常的神經部位給予電刺激的方式，可以使身體恢復部分機能。並且，隨著積體電路與生醫電子的發展，在單晶片上整合智慧型仿生系統的目標可被實現，結合微電子技術、醫學以及生物化學，能夠發展出應用於不同治療的生物晶片，例如：閉迴路深層腦部刺激 (Deep brain stimulation) 系統、植入式單晶片癲癇抑制系統以及電子耳的應用。

根據本生醫研究團隊為治療帕金森氏症的前提，本篇提出一多通道的電壓刺

激器，藉由單一輸出對植入式起搏器 (Implantable pulse generator) 機殼送出雙相位的定電壓，來完成每次的電壓刺激。為因應電極與人體組織阻抗的變動，考慮負載適應性，此刺激器設計了±0.5V~±8V 的大範圍電壓輸出，搭配 4 位元的控制訊號，有 16 種電壓大小可以調整，因此系統可根據不同的應用輸出適當的刺激電壓。像是帕金森氏症的治療，通常使用不超過 3.5V 的電壓刺激，但在電子耳的動物實驗中，卻可能需要大於 5V 的電壓刺激。

對於植入式單晶片的整合而言，設計時需考量安全性、功率消耗與可靠度，而刺激器的電源供應，會由前級的電荷幫浦系統提供±10V 的高電壓來維持整體電路的正常操作。刺激器電路在 0.25-μm 2.5-V/5-V/12-V 的高電壓製程下實現，即使在必須承受 20V 耐壓的狀況下與負電壓的操作中，電路也不會有 p-n 接面的崩潰、p-n 接面的順向導通或元件過壓等問題。

Design of Multi-Channel Monopolar Biphasic Voltage Stimulator for Implantable Biomedical Applications

Student: Chia-Chi Hsieh **Advisor: Prof. Ming-Dou Ker**

Institute of Electronics
National Chiao-Tung University

Abstract

Neurological disorder causes unusual electrical activity in the brain that further affects the motor system, such as Parkinson's disease and epilepsy, and there are seventy million population around the world suffer from these symptoms. Instead of drugs, electrical stimulation therapy has been proven to effectively restore some physical functions of patients by stimulating the abnormal nerve sites. With the development of CMOS process and bioelectronics, an implantable system-on-chip (SoC) device is able to be realized. Combing with microelectronics, medicine and biochemistry, the biomedical chip is made for different therapeutic applications. For example, closed-loop deep brain stimulation (DBS) system, implantable SoC for seizure control, and cochlear implant.

According to the research of our biomedical group, a multi-channel voltage stimulator is proposed for Parkinson's disease treatment. It completes every

stimulation by delivering biphasic stimulus voltage to implantable pulse generator (IPG) case from one of the stimulator outputs. Considering of loading adaptation due to electrode-tissue impedance variation, a wide-range of stimulus voltage from ±0.5V to ±8V is designed. The adjustable output voltage is controlled by 4-bit binary code, which allows the system to generate 16 different amplitudes. Therefore, the proposed stimulator can be used in many biomedical applications through providing a proper stimulus voltage. In the treatment of Parkinson's disease, voltage stimulation under 3.5V is often used. However, a voltage that is larger than 5V might be needed in the animal experiment of cochlear.

For implantable SoC integration, safety, power consumption, and reliability have to be taken into consideration. A multi-charge-pump (MCP) system, which serves as power supply to stimulator and provides ±10V to support the circuit operation. The whole stimulator circuit has been fabricated in TSMC 0.25-μm HV USG 2.5-V/5-V/12-V CMOS process without device overstress, p-n junction breakdown issue, or p-n junction forward-leakage problem under 20V compliance voltage and negative voltage operation.

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謝　佳　琪

謹誌於　竹塹交大　戊戌　夏

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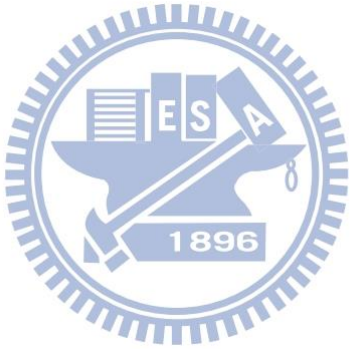

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Chapter 1

Introduction

1.1 Motivation

Neurological disorder causes abnormal electrical activity in the brain that further affects the motor system, such as Parkinson's disease and epilepsy that affect almost seventy million people, over 1% of the world population. Fortunately, as biomedical science and electronics have been developed rapidly, we are able to combine these two magnificent fields to the new technology known as bioelectronics. Nowadays, bioelectronics devices are used to replace drug treatment to avoid its side effects such as dyskinesia which influences the patient's quality of life. Furthermore, there are nearly one-third of the epilepsy patients remain either drug-resistant or develop limiting adverse effects.

Several applications like the resonance imaging (MRI) [1], electroencephalography (EEG) [2], electrocorticography (ECoG) [3], and deep brain stimulation (DBS). The biomedical implant device are proposed are helpful not only to patients but also doctors in the surgery. According to the research of neuroscience, some physical dysfunctions can be restored by functional electrical stimulation (FES) [4]. For instance, cochlear implants for treating profound hearing loss [5], retinal prostheses for treating blindness [6], spinal cord stimulators for blocking chronic pain [7], closed-loop electrical stimulation for epileptic seizure control [8], [9], and deep brain stimulators for treating Parkinson's disease [10].

1.2 Thesis Organization

This thesis consists of five chapter.

Chapter 1 includes motivation of this work and organization of the thesis. In chapter 2, basic introduction of neuro-stimulation therapy and implantable SoC device is presented. After that, some prior works of stimulator will be discussed in chapter 3, which also includes the design considerations and details of this proposed stimulator circuit. And then chapter 4 shows measurement results and in-vivo animal experiment tests. The last chapter, chapter 5, provides the conclusion of above chapters and three research directions for the future work of stimulator structure.

Chapter 2
Introduction of Implantable Device and Stimulation Therapy

2.1 Introduction of Implantable SoC

Implantable devices are developed recently for electrical stimulation therapy. However, open-loop stimulation type dissipates higher power and has to change the battery often, and disrupt pathological neural synchrony. Several researches has proposed that closed-loop is a better way of treatment comparing to open-loop [10]-[12]. Fig. 2.1 shows block diagram of closed-loop implantable DBS SoC with wireless telemetry [13]. The external monitor system is a user-friendly interface for medical personnel that can communicate to the implant part inside human body from outside. The implanted DBS electrodes is for stimulating and detecting the behavior of brain. Take Parkinson's disease as an example, the β-band (12-30Hz) activity of local field potential (LFP) in subthalamic nucleus (STN) can be detected through electrodes, this bio-signal will be obtained by local field potential acquisition unit in Fig. 2.1, and then the bio-signal processer will give commands to stimulator. The power of implantable SoC is provided by power system and can be recharged by wireless power system.

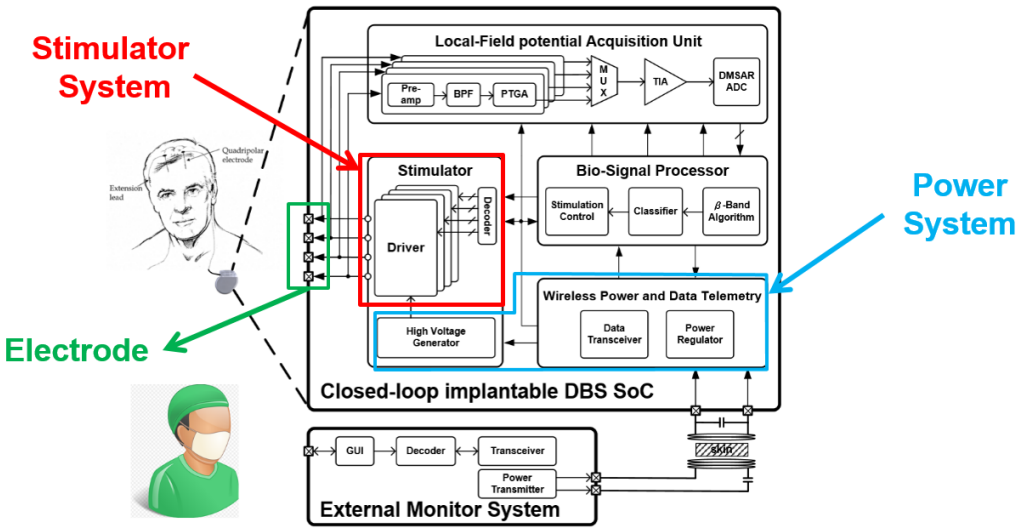
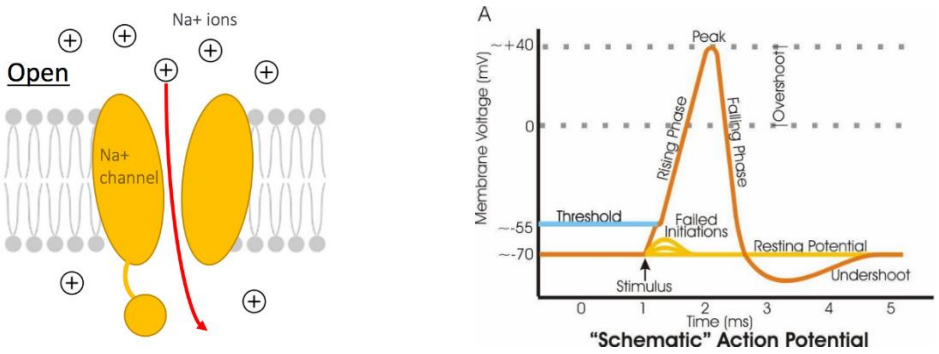


Fig. 2.1 Block diagram of closed-loop implantable DBS SoC with wireless telemetry.

2.2 Introduction of Neuromodulation

Electrical stimulation seen as an effective way on suppressing those abnormal activities of the cell. Fig. 2.2 explains the phenomenon of neurons behavior. At first, the cell is resting, so the membrane potential remains negative. When it needs to be activated for passing messages to other cells, depolarization phase caused by Na+ channel is opening, as long as membrane potential exceed the threshold voltage of –55mV, the cell starts to work and an action potential is able to be observed [14].



(a) (b)

Fig. 2.2 Bio-reaction of nerve cells. (a) The behavior of nerve cells when Na+ channel is opened opened. (b) Action potential.

If unpredictable depolarization of cell happens, it will disturb normal cell and affects the nervous system. In implantable SoC system, unusual rising membrane potential can be detected, and it delivers biphasic (cathodic/anodic) stimulation pulse shown in Fig. 2.3 to suppress the changing of membrane potential. The cathodic stimulation usually starts first to elicit a desired neural response [15], while the anodic pulse, cancels charge across stimulating electrode pair. The interphase delay separates the cathodic/anodic pulse so that anodic pulsed does not reverse the physiological effect of the cathodic current. No matter which stimulator structure is required, the biphasic pulse is needed for minimizing redundant charges in the body to avoid physiological harm [16]

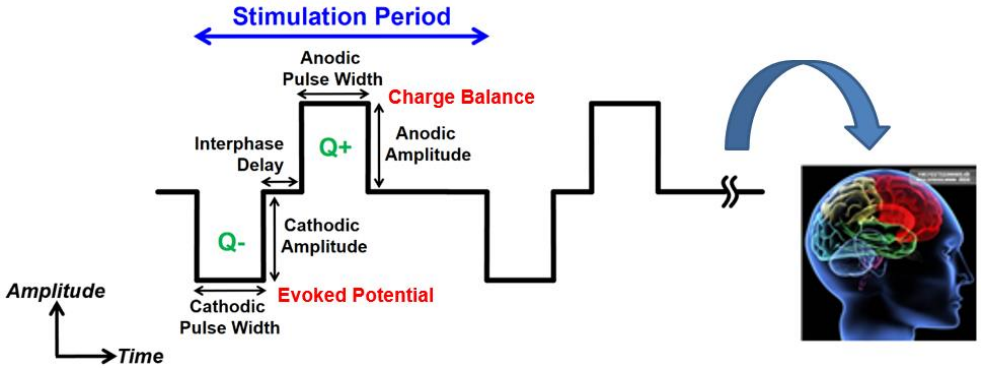


Fig. 2.3 Biphasic stimulation pulse known as FES.

2.3 Introduction of Electrode-Tissue Impedance Model

Since the metal electrode will be implanted to human body, there is an interface between these two. According to [6], [17], the electrode-tissue impedance can be modeled as right-hand side of Fig. 2.4. In the model, R_S is the solution spreading resistance decided by the resistivity of the tissue fluid (set by ionic species in solution). C_{dl} represents the double-layer capacitance, which is created by the accumulation of tightly adsorbed ions at the electrode surface and more loosely attracted ions in a diffusion layer behind it. The Faradaic resistance, R_f is determined by diffusion of reactive species to the electrode for charge-transfer reactions. The R_f indicated as a time-varying variable resistor because its value varies based on the dynamics of redox charge-transfer reactions occurring at the electrode.

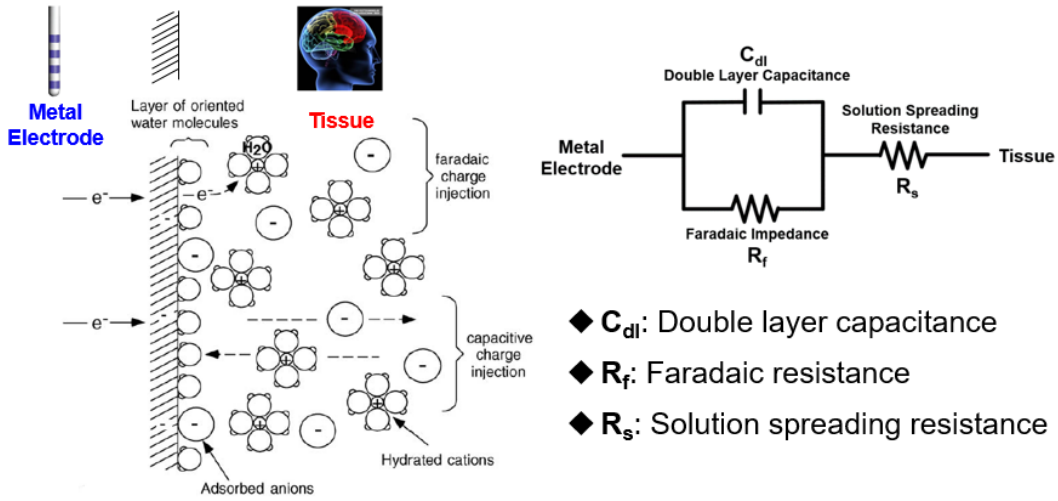
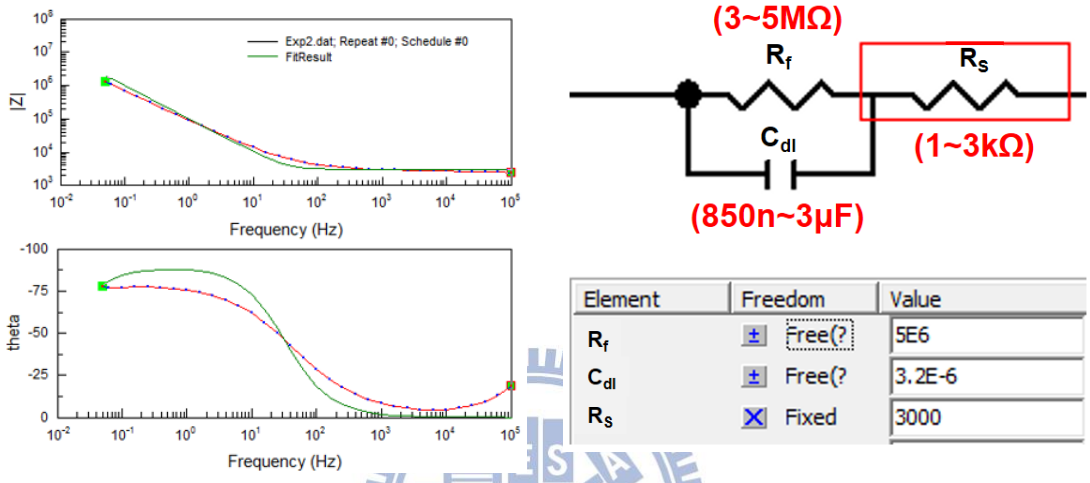


Fig. 2.4 Equivalent circuit model of electrode-tissue impedance to illustrate the interface of metal electrode and tissue.

For implantable biomedical application, electrode-tissue impedance vary with the size and position of the electrode, but the scale of R_S, C_{dl}, and R_f can be measured. Fig. 2.5 shows the measurement result of human brain measured from Solartron SI

1260A Impedance Analyzer. The electrode used in this case is platinum material. The impedance analyzer sweeps frequency from 0.05 to 10^5 Hz and the sets ac amplitude 0.1V. The result is shown in red line in Fig. 2.5 (a), and then the component model of Fig. 2.6 (b) is selected to be fitted. Finally, all the values of the equivalent circuit will be obtained (the green line in Fig. 2.5 (a) is the fitting result).



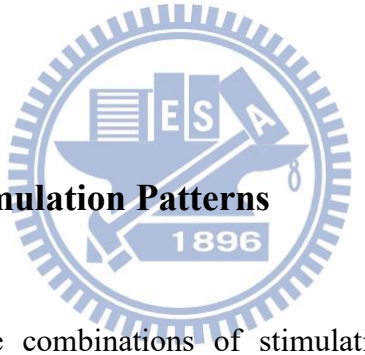
(a) (b)

Fig. 2.5 Electrode-tissue impedance measurement result. (a) The curve fitted by impedance/gain-phase analyzer and converted to (b) typical value of human brain impedance.

Every kind of electrode metal material has its own safety ΔV margin in case of hydrolysis and it is called "water window" of the specific material. That is to say, the voltage difference on double layer capacitance C_{dl} must not exceed this range. Table 2.1 presents the charge-injection limits of several types of electrode material that are common used in-vivo [18]. The ΔV from –0.6V to 0.6V is the safest region.

Table 2.1 Charge-injection limits of electrode materials

Material	Mechanism	Maximum Q_{inj} (mC cm^{-2})	Potential Limits V versus Ag|AgCl	Comments	References
Pt and PtIr alloys	Faradaic/capacitive	0.05–0.15	−0.6–0.8		71
Activated iridium oxide	Faradaic	1–5	−0.6–0.8	Positive bias required for high Q_{inj}. Damaged by extreme negative potentials (<−0.6 V)	72, 73
Thermal iridium oxide	Faradaic	~1	−0.6–0.8 V	Positive bias required for high Q_{inj}	74
Sputtered iridium oxide	Faradaic	1–5	−0.6–0.8 V	Benefits from positive bias. Damaged by extreme negative potentials (<−0.6 V)	75; S.F. Cogan, J. Ehrlich, T.D. Plante, A. Smirnov, D.B. Shire, M. Gingerich, J.F. Rizzo, unpublished
Tantalum/Ta_2O_5	Capacitive	~0.5		Requires large positive bias	76, 77
Titanium nitride	Capacitive	~1	−0.9 to 0.9	Oxidized at positive potentials	78
PEDOT	Faradaic	15	−0.9 to 0.6	Benefits from positive bias	79



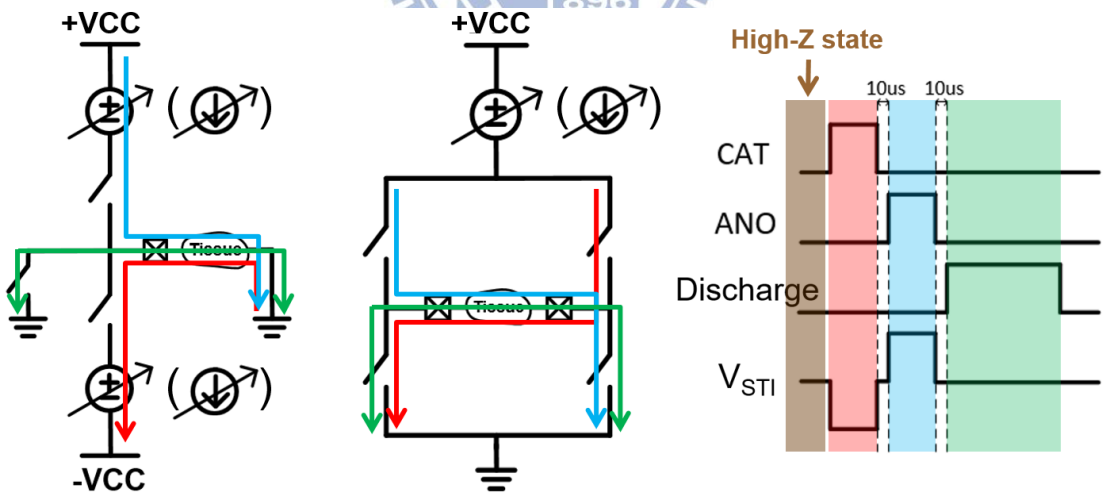
2.4 Introduction of Stimulation Patterns

Table 2.2 lists all the combinations of stimulation patterns, there are two stimulation methods (voltage and current), two system configurations (monoplar and bipolar), and two kinds of stimulation pulses (monophasic and biphasic). Difference between voltage and current stimulation is that distinct type of source of the circuit will be delivered to tissue, which shown as Fig. 2.6, both the stimulation methods are used in clinical treatment. But the therapeutic effects of bipolar or monopolar stimulation had been discussed in some articles [10], [19], and the monopolar configuration was a general usage in laparoscopic electrosurgery [20]. As for stimulation pulses, biphasic pulse is preferred since the charge can be balanced after stimulation. Even though the amplitude of anodic and cathodic pulse are not the same [21], it can still remain charge balance by adjusting the pulse width of stimulation.

Table 2.2 Combination of stimulus pulse

Stimulation Methods : Voltage / Current	
Stimulation Configurations	**Stimulation Pulses**
Monopolar Electrode Model — Tissue Impedance	Monophasic or Biphasic (Lilly pulse)
Bipolar Electrode Model — Tissue Impedance — Electrode Model	

After summarized all the stimulation patterns above, brief circuit structure of monopolar and bipolar with voltage (current) stimulation, and the biphasic output waveform are illustrated in Fig. 2.6



(a) (b) (c)

Fig. 2.6 Brief circuit structure of stimulation configurations with voltage (current) stimulation. (a) Monopolar configuration. (b) Bipolar configuration. (c) Biphasic output waveform generated by (a) and (b).

Basically, monopolar configuration needs two high voltage power supplies to realize the biphasic stimulation, where the positive one (+VCC) is for anodic pulses and the negative one (–VCC) is for cathodic pulses. Although one more power supply is needed as comparing to the bipolar configuration, the characteristic of one interconnect lead per site reduces the risk during surgery [16]. Besides, monopolar system generates biphasic pulse through one channel that can be realized with half of the number of stimulator drivers and less the chip area, as comparing to the bipolar configuration.

The design consideration of two stimulation methods is that for current stimulator, output voltage is decided by the product of stimulus current and impedance value. However, if the loading impedance becomes larger due to tissue fluid between electrodes and tissue surface, the desired stimulus current will be limited by the voltage headroom of output driver. On the other hand, as long as the voltage stimulator can deliver an expected stimulus voltage to ideal impedance, when wide range of stimulus voltage is designed, it may be more suitable to cover impedance variation.

Chapter 3
Design of Monopolar Biphasic Voltage Stimulator

3.1 Prior Works of Stimulator

In the last chapter, simple circuit structures of stimulator have been introduced. As the development of electrotherapy, a variety of implantable stimulators have been researched and presented. Here, several stimulus drivers will be shown as examples of bipolar and monopolar stimulation configuration.

3.1.1 Bipolar Configuration

Fig. 3.1 is an example of bipolar voltage driver [5]. This work is used for cochlear device, and is realized in 0.18-μm LV CMOS process. The high voltage (VDDH) in this design is +8.4V and output range from 1V to 7V. The driver can be divided into three parts, high-voltage-tolerant amplifier, output stage, and dynamic bias circuit. By feedback loop of the amplifier and R_1, R_2, V_{OUTP} is able to deliver desired stimulus voltage. Realized by LV CMOS process but to support stimulus voltage of 7V, it needs a proper gate bias in output stage. The dynamic bias circuit can prevent MOSFETs in output stage from overstress with a logic gate when the most significant bit (MSB) of amplitude signal is logic high.

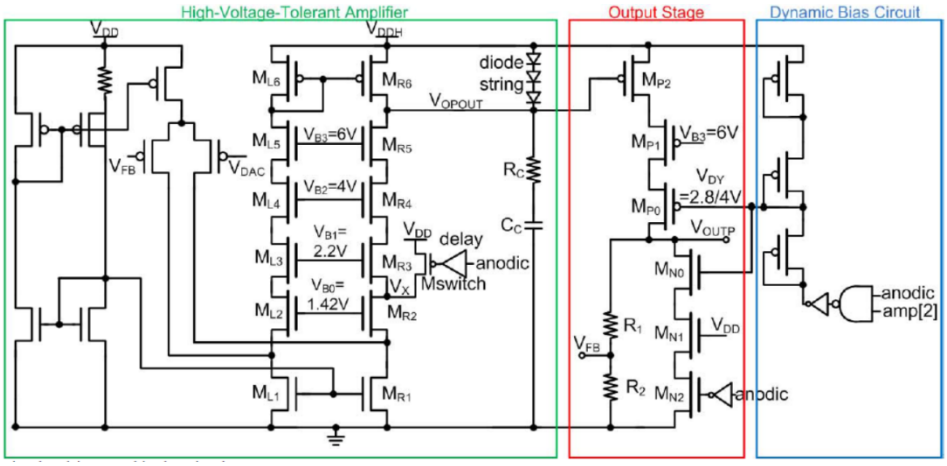


Fig. 3.1 Bipolar configuration with biphasic voltage stimulation.

The next prior work of bipolar configuration shown in Fig. 3.2 is a dual-mode driver structure, which implies voltage or current stimulation are able to be delivered [22]. Due to high output specifications of 10V and 5mA, the stimulus driver is proposed in 0.25-μm HV CMOS process with power supply 18V. When in voltage-mode stimulation, Vin that is generated by voltage source will be delivered to tissue model through high voltage op and feedback capacitors controlled by voltage mode switches. However, in current-mode stimulation, only current mode switches are used, and a current sink source is used to generate stimulus current.

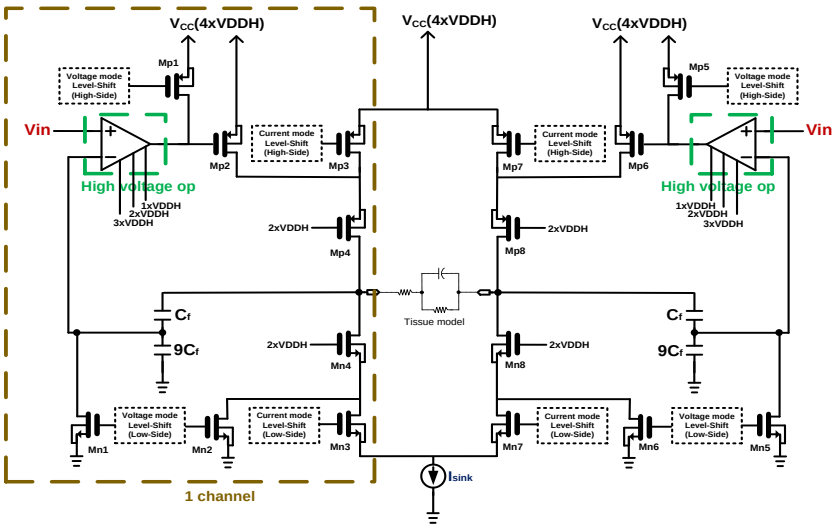


Fig. 3.2 Bipolar configuration with biphasic voltage or current stimulation.

3.1.2 Monopolar Configuration

Different from bipolar configuration stimulus driver, they output the biphasic stimulation pulses on tissue with positive and negative voltage or current relatively. If a monopolar configuration driver has to deliver the biphasic pulses, it has to be capable of driving the anodic stimulation to tissue and urging the cathodic stimulation back from tissue. Typically, monopolar circuit design included positive and negative high voltage to achieve the biphasic output.

Fig. 3.3 shows a monopolar stimulus driver with positive and negative high voltage (VDD is +5V and VSS is −5V) exist simultaneously [23]. By controlling the switches, biphasic current stimulation can be completed. It realized in 0.35-μm HV CMOS process. To minimize current mismatch between cathodic and anodic stimulation pulses for achieving the charge balance, this work describes a compact negative feedback self-calibration technique. Thus, maximum output current 1mA can be provided with current mismatch is less than 0.3μA.

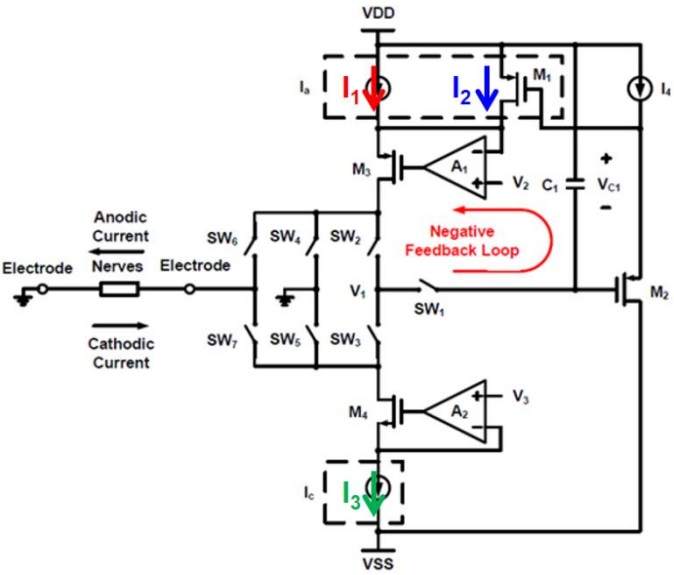


Fig. 3.3 Monopolar configuration with biphasic current stimulation when positive and negative high voltage exist simultaneously.

Fig. 3.4 is also a monopolar stimulus driver that can deliver biphasic stimulus current [24]. Different to the design in Fig. 3.3, the positive and negative high voltage (+7.2V and −7.2V) do not exist simultaneously. Thus this work can be fabricated in 0.18-µm LV CMOS process because the power domain is 0V to +7.2V during anodic stimulation and becomes 0V to −7.2V for cathodic stimulation. With high output loading impedance (kΩ scale) in this application, the maximum output of the driver is 50µA. Also, it has dynamic gate bias technique included to prevent device overstress, the value before "/" in Fig. 3.4 is the bias condition of anodic stimulation while the number after "/" represents the bias voltage of cathodic stimulation.

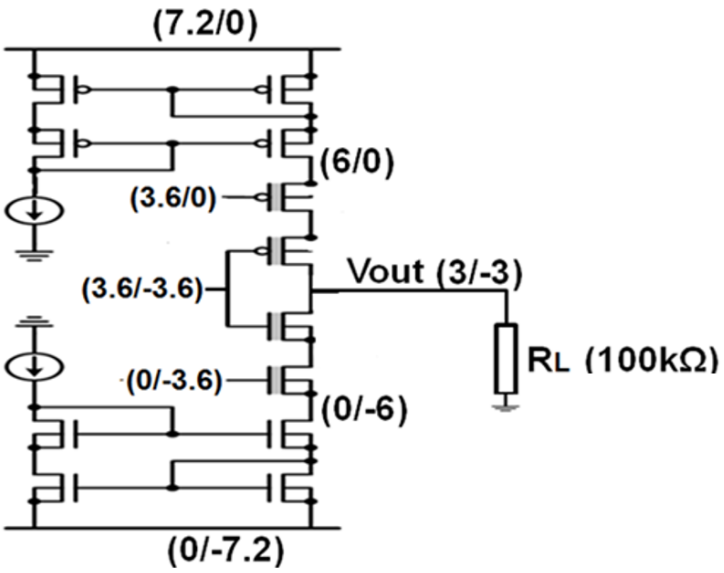


Fig. 3.4 Monopolar configuration with biphasic current stimulation when positive and negative high voltage do not exist simultaneously.

3.2 Specifications and Design Considerations of Stimulator

The stimulator is designed for biomedical applications with SoC integration, so the operating voltages of 1.8V and 3V are provided from power management unit. For negative output, a negative DAC is contained to generate a negative reference voltage, thus a low negative voltage supply (−3V) is needed. A MCP system, consisted with a positive charge pump and two negative charge pumps, serves as voltage generator to provide the desired positive and negative voltages. Because the high voltages +VCC and −VCC exist simultaneously, the driver voltage compliance is as high as 20V. Table 3.1 lists the specifications of stimulator.

Table 3.1 Specifications of stimulator

Process	**0.25-μm 2.5V/5V/12V CMOS process**
Electrode Configuration	**Monopolar**
Mode	**Voltage** (Biphasic)
Supply Voltage	**1.8V, 3V** (From power management unit) **-3V, ±10V** (From charge pump)
Stimulation Amplitude	**±0.5V ~ ±8V** (Amplitude step: 0.5V)
Pulse Width	**20 ~ 450μs**
Stimulation Frequency	**2 ~ 250Hz**
Channel Number	**4 channels**
Output Resistance Load (R_S)	**≥ 500Ω**

Fig. 3.5 shows monopolar configuration of stimulus driver. With the maximum output voltage of ±8V, the voltage difference between +VCC (–VCC) and Vout can be as large as 18V if the ±10V power supplies are given. For Gsw, Vout is either a positive or negative voltage, but the other side of the switch is always grounded, so in this work, a different way of discharge operation will be used instead of connecting

Vout to ground directly. Because of the negative voltage is including in the design, it has been realized in a 0.25-μm 2.5-V/5-V/12-V CMOS process with the grounded p-type substrate.

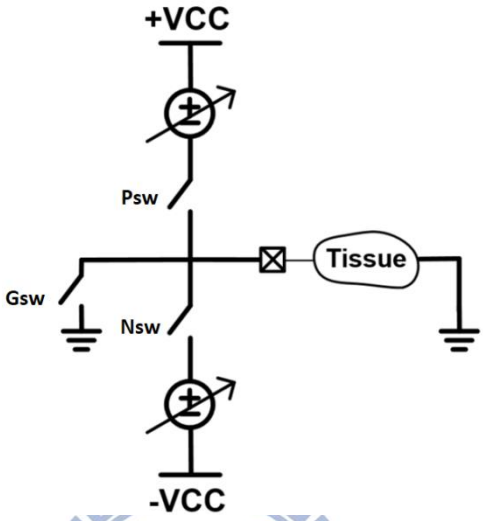


Fig. 3.5 Monopolar configuration of stimulus driver.

3.2.1 Negative Voltage Operation Analysis

With negative voltages involved, p-n junction breakdown and forward-leakage issues have to be taken into design considerations, when the p-type substrate is grounded instead of the most negative voltage in the system.

Table 3.2 is the cross section view of LV devices. It can be seen that if P-substrate is 0V, PMOS will be dysfunctional due to junction forward-leakage between P-substrate and N-Well (the bulk biased at a voltage less than 0V). Even if the bulk is biased at 0V, the four terminals (source, gate, drain, and bulk) of the PMOS may suffer from device overstress. As for NMOS, it can be surrounded by deep N-Well to deal with negative voltage situation [25]. However, for LV device, the junction breakdown voltage of P-Well and N-Well is less than 15V, and that is not

enough to support this design. Hence, HV MOSFETs are needed for the proposed stimulator due to their high breakdown voltage. Table 3.3 indicates the cross section view of 12-V HV devices. With suitable HVPW and HVNW bias of 12-V devices, the driver can avoid three difficulties that LV devices may face of, device overstress, p-n junction breakdown issue, and p-n junction forward-leakage problem.

Table 3.2 Cross section view of LV devices

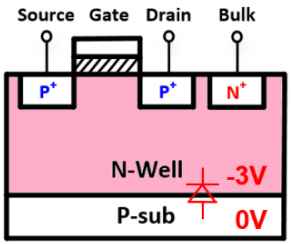
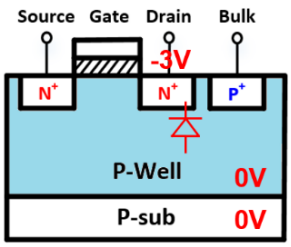
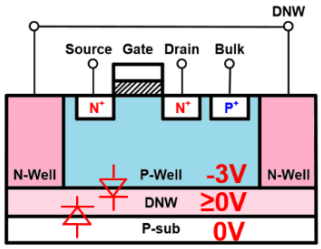
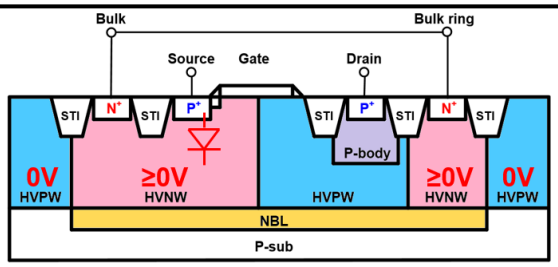
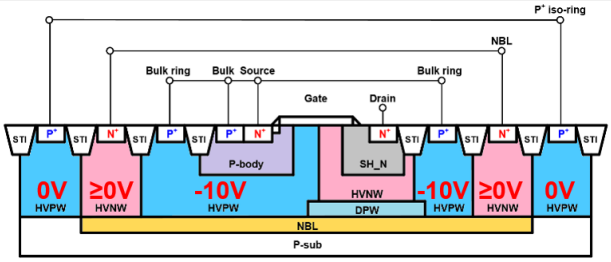
LV PMOS	LV NMOS	LV NMOS with Deep N-Well
		

Table 3.3 Cross section view of 12-V HV devices

HV PMOS (12V)	
HV NMOS (12V)	

3.3 Design of Stimulator

The block diagram of proposed monopolar biphasic voltage stimulator is shown in Fig. 3.6. The system consists of control circuit, DACs, switch control circuits (high-side level shifter), bias circuit, and the stimulus driver. And there are three kinds of devices in the 0.25-μm are used in this design, 2.5-V/5-V LV CMOS and 12-V HV CMOS. Their symbols are indicated in Table 3.4 to explain following circuit blocks.

Table 3.4 Device symbols of 0.25-μm CMOS for following circuit blocks

	2.5V	5V	12V
PMOS	Source / Gate / Bulk / Drain	Source / Gate / Bulk / Drain	Source / Gate / Bulk / Drain
NMOS	Drain / Gate / Bulk / Source	Drain / Gate / Bulk / Source	Drain / Gate / Bulk / Source

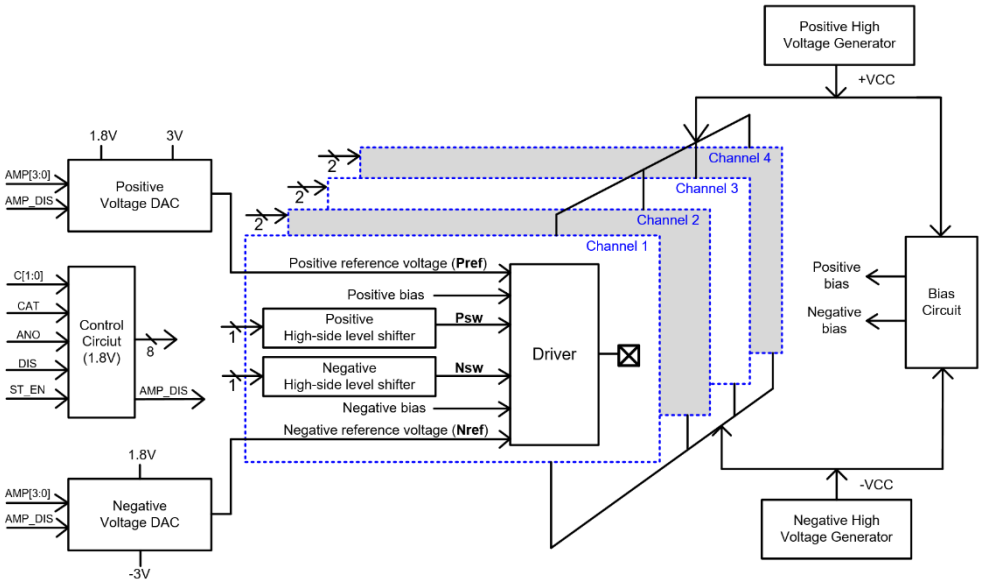
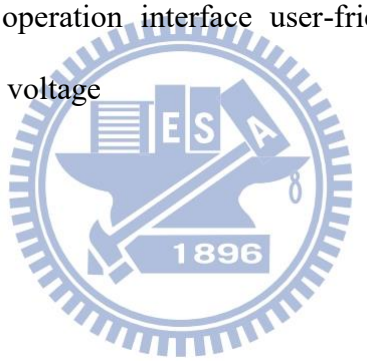


Fig. 3.6 Block diagram of proposed stimulator system.

To minimize the leakage current, all stimulus drivers remain to high-Z state when enable signal (ST_EN) is logic low, i.e. the three switches Psw, Nsw and Gsw in Fig. 3.5 are open. During stimulation period, where ST_EN is logic high, the parameters such as frequency, pulse width, amplitude, and cathodic/anodic pulse order are programmable, and one of the four channels will be selected to deliver biphasic pulses. Digital input signals will be processed through control circuit block, then those signals serve as one of the input signal to DAC or pass to the drivers for switches control. There are 2-bit channel choosing signals defined by C[1:0] in Fig. 3.6. The output waveform is decided by the input information of cathodic (CAT), anodic (ANO), discharge (Discharge), and 4-bit amplitude (AMP[3:0]) signals. Control circuit makes the operation interface user-friendly with simple setup to produce the desired stimulus voltage



3.3.1 Stimulus Driver

There are four driver channels within the stimulator, where the driver circuit of one channel is shown in Fig. 3.7. The 12-V HV PMOS and NMOS are used for 20-V high-voltage-tolerant design. Each driver comprises a pair of folded cascade Op-amps, switches (Mp1 and Mn1), power MOSFETs (Mp2 and Mn2), and stack transistors (Mp3 and Mn3). A feedback loop is built in the driver, and the ratio of feedback resistors is ten times of the reference voltages (Pref and Nref), that are connected to the input of Op-amps. Thus, the driver output voltage at the Vout node can be locked at the expected stimulus voltage. Psw and Nsw are the input signals of driver those coming from control circuit. By passing through high-side level shifter which will be explained in section 3.3.2, the voltage level of control circuit output is shifted from

1.8V to +VCC or to –VCC, so 0V remains logic low to positive side but becomes logic high to negative side

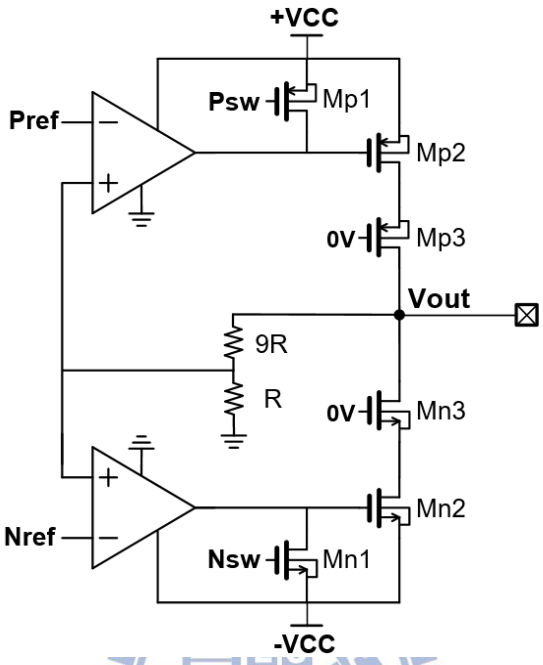


Fig. 3.7 Circuit implement of one-channel stimulus driver.

Before the stimulation begin (ST_EN signal is logic low) or for those channels that are not selected, stimulus driver is in high-Z state. At this time, Psw is logic low and Nsw is logic high (both ANO and CAT signal are logic low), that turned off both power MOSFETs Mp2 and Mn2. With unit R is designed as 100kΩ, there will be 1MΩ impedance and two open circuit seen from Vout, a high-Z state and low leakage situation is completed.

When Psw of a specified channel is logic high, that implies this channel is selected for anodic stimulation. Mp1 turned off due to gate voltage level equals to +VCC, thus the Pref at the input of OP-amp, Mp2, and resistors compose a complete LDO feedback loop. At the meantime, Nsw for cathodic stimulation is also logic high, that makes Mn1 on and Mn2 off since the gate of Mn2 is biased at –VCC. Therefore, break the loop of Nref at the input of Op-amp, Mn2, and feedback resistors.

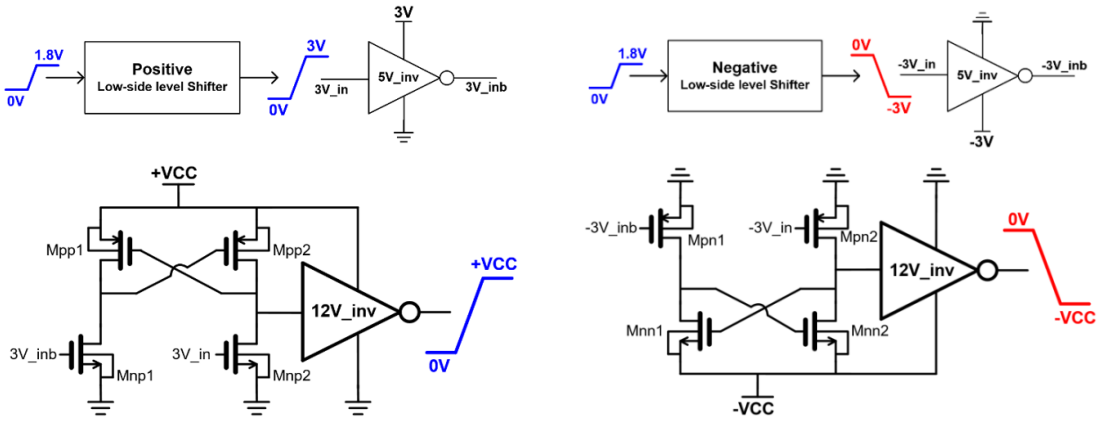
Cathodic stimulate operation is similar, but the logic states of Psw and Nsw are opposite to anodic stimulation. When cathodic stimulus voltage is delivered, Nsw is logic low and makes Mn2 on while Psw becomes logic low to turn off Mp2. As a result, a totally contrary operation to anodic stimulation will be realized.

During discharge phase, all switches in DACs are turned off, thus the Pref and Nref are biased at a voltage level of 0V, and then 0V will be pass to Vout by negative side feedback loop to make sure that the Vout pad is grounded.

As aforementioned, Vout can be as large as 18V if the ±10V power supplies are given. To prevent device overstress, the Mp3 and Mn3 are stacked there and biased at 0V regardless of the positive or negative output. And thanks to the stack MOSFETs, even if Vout of disable channels with some variation due to the stimulation voltage at the enabled neighborhood channel under high-Z circumstance, all the driver devices do not suffer from overstress issue. The drain voltage of Mp3 and Mn3 is changing either positive or negative, but with suitable HVPW/HVNW bias of 12-V devices, the driver can avoid p-n junction forward-leakage when the P-substrate is 0V.

3.3.2 Driver Switch Control

To control the driver switches (Mp1 and Mn1 in Fig. 3.7), the control signal 0V~1.8V are shifted to the voltage level that is needed by the circuit named high-side level shifter in Fig. 3.6. In brief, positive high-side level shifter shifts “0V to 1.8V” to “0V to +VCC”, and negative high-side level shifter shifts “0V to 1.8V” to “0V to –VCC” which shown in Fig. 3.8



(a) (b)

Fig. 3.8 Control signals used in driver circuit control with (a) digital input 1.8V shifted to +VCC as logic high and (b) digital input 1.8V shifted to –VCC as logic low.

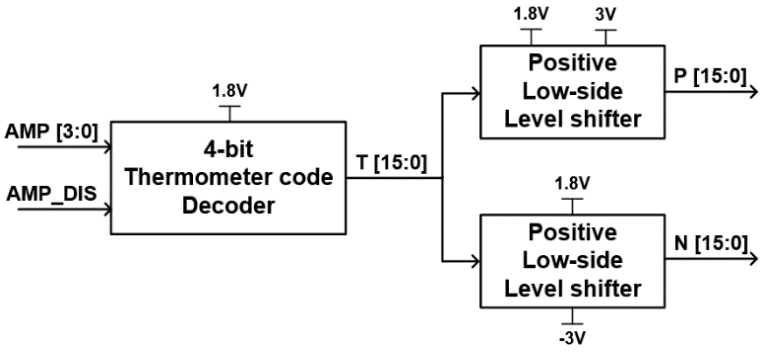
Since the threshold voltage of 12-V device is high, 3V and –3V are created first from the positive and negative low-side level shifter to serve as input voltage to the high-side level shifter. Both the level shifter circuits are a common structure of level shifter. The key point of design concept is that the size of input pair transistors (Mnp1, Mnp2, Mpn1, and Mpn2) must be larger than cross coupled pair (Mpp1, Mpp2, Mnn1, and Mnn2). So that input pairs are able to pull their drain voltage low enough to 0V when they are on. Through the cross coupled pair, the positive feedback will turn on Mpp1 and Mnn1, and then Mpp2 and Mnn2 will be turned off when the input of 12V inverter begins to be lower. Finally, the input of 12V inverter will have a full swing and the output can transit 0V to +VCC and 0V to –VCC.

Main difference of these two high-side level shifters is that positive one use NMOS as input pair, but negative one use PMOS as input pair. That is because if NMOS are used in negative level shifter, both 0V and –3V concerned as high voltage to –VCC, therefore they will lose their judgement on logic state. After 0V to 1.8V shifted by positive high-side level shifter, the input signal becomes 0V to +VCC, so logic low keeps at 0V and logic high turns into +VCC. On the other hand, 0V to 1.8V

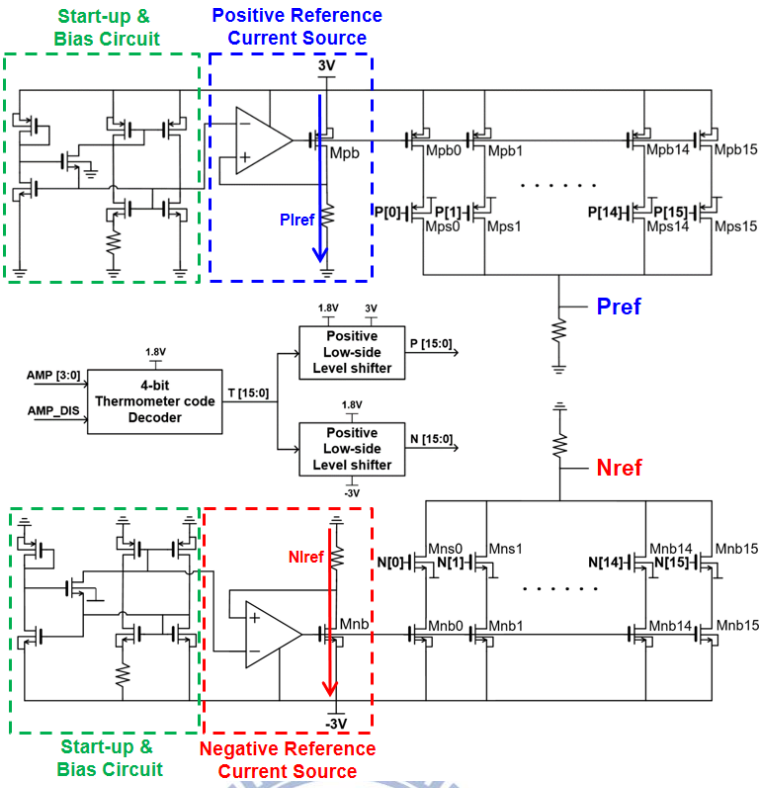
turned into 0V to −VCC by negative high-side level shifter, under this circumstance, 0V becomes logic high while 1.8V changes to logic low (−VCC).

3.3.3 Voltage Reference DAC

Fig. 3.9 presents the DAC circuit in detail. With 4-bit of amplitude input, the stimulus voltage can be provided from ±0.5V to ±8Vwith step amplitude of 0.5V. In order to deliver the target voltage, the positive and negative reference voltages (Pref and Nref) will be generated first. Different from traditional binary code DAC, thermometer code DAC is used owing to the advantage of reducing glitch current [26]. Besides, same weighted of MOSFETs in the thermometer code DAC is beneficial to layout matching and array arrangement, thus output accuracy is also improved. Another input signal called AMP_DIS in Fig. 3.9 (a) is related to discharge. In discharge phase, AMP_DIS is logic high to turn off all switch transistors in the DAC.



(a)



(b)

Fig. 3.9 Voltage reference DAC circuit including (a) control circuit of DAC and (b) positive voltage DAC (upper part) and negative voltage DAC (lower part).

Positive voltage DAC will be explain first. In the beginning, digital inputs transfer to 16-bit thermometer code by the decoder. However, low-side level shifter is required to shift 1.8V to 3V for correct logic control of DAC. Next, a reference current source is generated by a structure similar to LDO. Output voltage of the amplifier used as bias voltage of Mpb0 to Mpb15 (PMOS string). By sizing the ratio of Mpb to PMOS string and controlling turn-on or turn-off operations of Mps0 to Mps15 (PMOS switches), a corresponding current is provided and converted to the positive reference voltage (Pref) by resistor.

Second, we talk about negative voltage DAC. The operating principle of negative voltage DAC is similar to that of positive voltage DAC. The major difference is to change PMOS string by NMOS string (Mnb0 to Mnb15), and

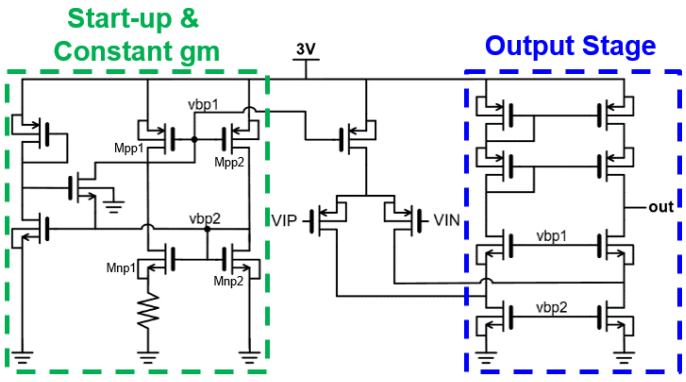
replacing PMOS switches by NMOS switches (Mns0 to Mns15). Under the circumstance of negative voltage operation, unlike the LV NMOS that can be surrounded by deep N-well, the PMOS device may suffer from N-well and P-substrate junction forward-leakage when P-substrate voltage is 0V. To avoid the leakage issue, all the bulk voltage of LV PMOS should be biased at 0V, which has to be careful of overstress issue and junction breakdown problem with consideration of process limitation. Another reason for using NMOS of negative DAC is that NMOS switches turn on with gate bias at high, therefore voltage level of 0V and −3V act as logic high and logic low to negative DAC. On the contrary, PMOS switches turn on with a lower gate voltage which is more negative than −3V.

3.3.4 Folded Cascode Op-amp

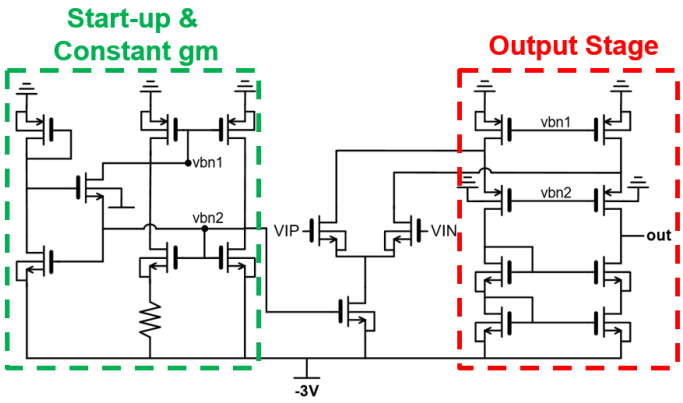
There are Op-amps in DACs and stimulus driver, both included a positive and a negative Op-amp (in Fig. 3.10 and Fig. 3.11). In DACs, they are used to bias PMOS and NMOS string, and in driver, they are used to complete voltage stimulation. All the Op-amps in this design are folded cascade structure [27], because the circuit can fit low voltage region and high voltage region simultaneously. The left part of Op-amps are low voltage operation region (marked as green area in Fig. 3.10 and Fig. 3.11), it contains start-up circuit (three MOSFETs left in green area) and constant gm circuit (four MOSFETs right with named in green area and a resistor). Constant gm circuit can generate current source [28], and this current is decided by the size of Mnp1 (Mnn1), Mnp2 (Mnn2), and the value of R in positive (negative) Op-amp. However, there is a probability that constant gm circuit will not work correctly. When power on, the gate voltage of PMOS is high and is low for NMOS due to parasitic capacitance.

If this situation just happened, the constant gm circuit cannot produce any current, in other words, the current is zero. Thus a start-up circuit is added to constant gm circuit in order to avoid the failure. After adding start-up circuit, it will pull down the gate voltage of PMOS and pull up the gate voltage of NMOS to prevent zero current circumstance.

Both Op-amps in DAC used 5-V LV devices, but in negative DAC, the bulk terminal of PMOS has to connect to ground (the highest voltage of negative part) to prevent junction leakage issue. The Op-amp of positive side feedback loop in the stimulus driver also used 5-V LV devices, to enhance the gain of folded cascode structure, the output stage of this Op-amp added two more pairs of NMOS compare to the Op-amp in positive DAC. Both gain of Op-amps in stimulus driver are designed as 100dB high to make sure they are able to push the loading. However, the Op-amp of negative side feedback loop in stimulus driver used two pairs of 12-V HV PMOS to replace the 5-V LV PMOS in output stage. That is because even if HV PMOS has its HV-ring which makes it functional under negative voltage operation, this HV-ring cannot be used on LV PMOS. Thus, for avoiding device overstress, HV device is used instead of LV device.

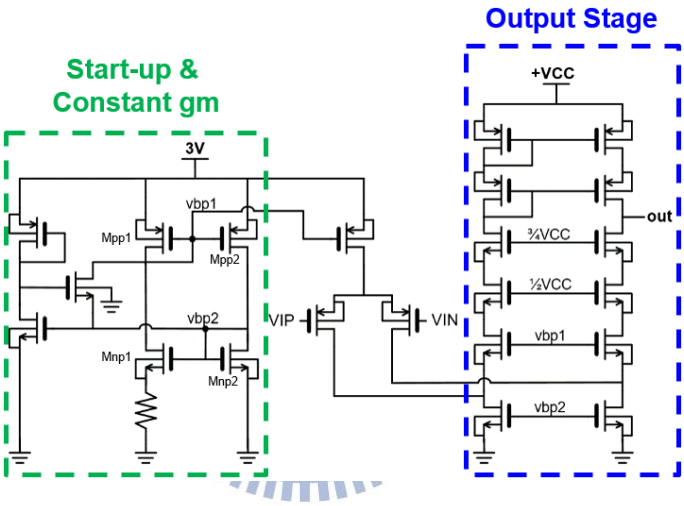


(a)

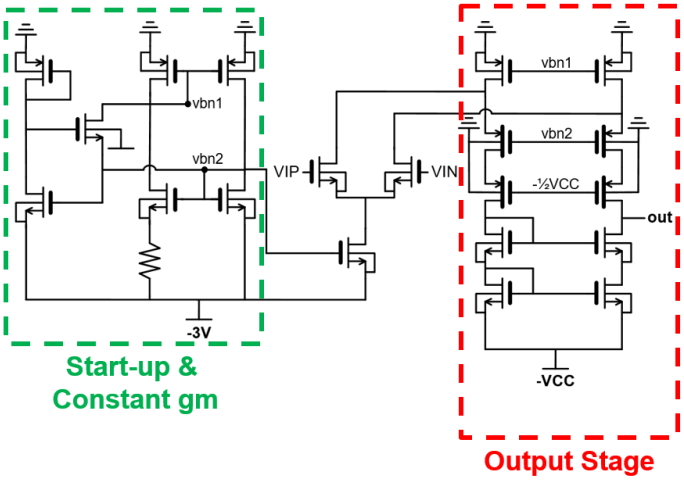


(b)

Fig. 3.10 Folded cascode Op-amps in DAC circuit. (a) Op-amp used in positive DAC and (b) Op-amp used in negative DAC.



(a)



(b)

Fig. 3.11 Folded cascode Op-amps in stimulus driver. (a) Op-amp of positive side feedback loop in driver and (b) Op-amp of negative side feedback loop in driver.

Chapter 4

Simulation Results and Measurement Results

4.1 Simulation Results

The proposed stimulator had been simulated in HSPICE with TSMC 0.25-μm HV USG 2.5-V/5-V/12-V CMOS process. First, the output waveforms of stimulator will be demonstrated. Next, the simulation results of 12-V HV devices overstress test in the stimulus driver under three circumstances are going to be shown.

Despite several control signals decide the output waveform of stimulator, ST_EN dominates whether there is output signal delivered to the tissue or not. Fig. 4.1 shows that even though the logic state of CAT, ANO, and Discharge signals are changed, as long as ST_EN remains logic low, Vout stays 0V. Once ST_EN is logic high, with combination of CAT, ANO, and Discharge input pulses, biphasic output voltage can be seen continuously at Vout.

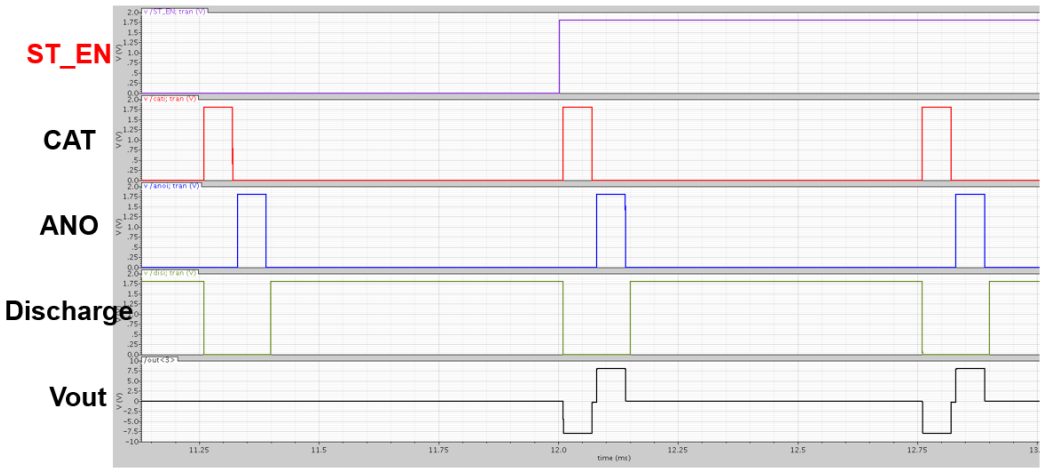
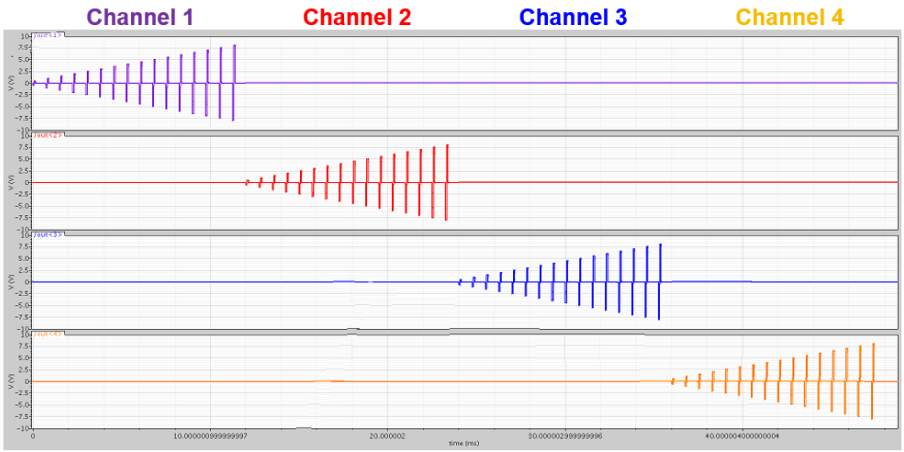
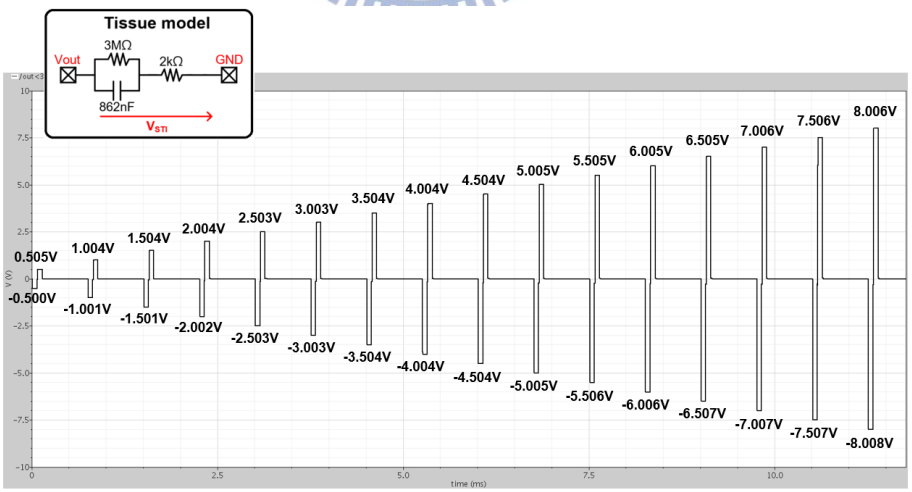


Fig. 4.1 Waveform of input signal ST_EN, CAT, ANO, Discharge, and output signal Vout.

With programmable digital inputs, the output of stimulator is able to be generated in different ways. Fig. 4.2 (a) is an example for delivering all the scales of stimulus voltage with output channel vary from channel 1 to channel 4, and Fig. 4.2 (b) enlarges the waveform of 16 steps biphasic pulses from ±0.5V to ±8V. Although one channel outputs stimulus pulse at once, during next stimulation period, changing output channel and adjusting the amplitude of stimulus voltage are achievable.



(a)



(b)

Fig. 4.2 (a) Simulation results of biphasic stimulus voltage output with different input signals of channel (C[1:0]) and amplitude (AMP[3:0]). (b) Enlarge waveform of all scale stimulus voltage pulse from (a).

The driver circuit is designed by 12-V HV devices, and overstress test is necessary for reliability concern. Thus the voltage difference between any two points of the device has to be within 12V to prevent gate oxide breakdown or junction breakdown. Following pictures are overstress test results which show the voltage between drain, gate, source, and bulk of all transistors in stimulus driver under three different situation.

To make the system work, it needs to be power on at first. At the meantime, driver circuit is at high-Z state to minimize the power consumption. Fig. 4.3 shows the overstress test result of stimulus driver when power on, and it tells all 12-V HV devices will not suffer from overstress problem.

After the power (±VCC) are given, the system is ready for stimulation. During stimulation phase, no matter which amplitude of biphasic stimulus voltage is generated at Vout, as shown in Fig. 4.4. The voltages between gate-to-source, gate-to-drain, source-to-drain, and bulk to one of three terminals (drain, gate, and source) of all 12-V transistors are also indicated in Fig. 4.4. It proves that none of HV devices overstressed.

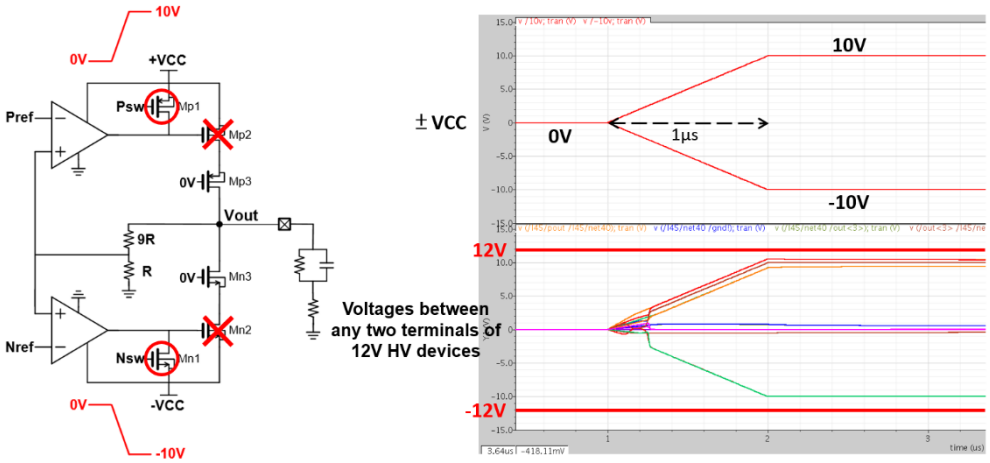


Fig. 4.3 Driver overstress test when power on.

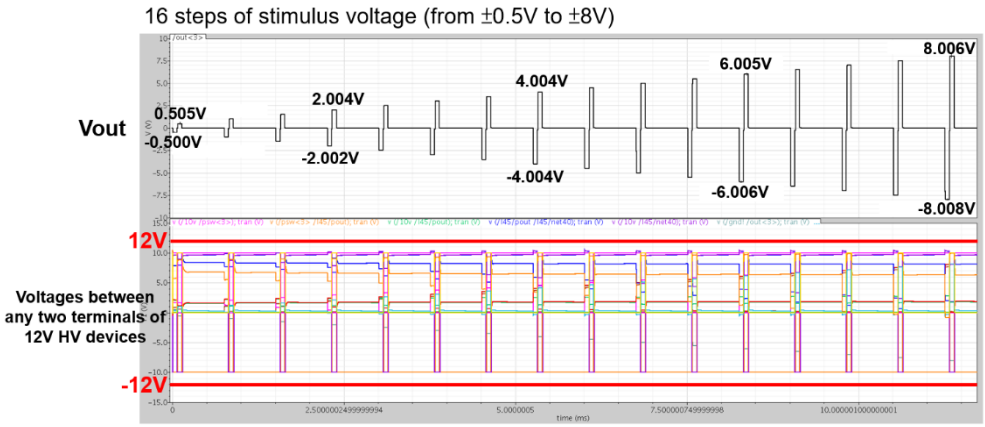


Fig. 4.4 Driver overstress test when stimulation.

There are four output channels, but simultaneously stimulation is not provided. Therefore, the third circumstance of overstress test simulates those channels who are not enabled, but their Vout may have some variations due to the stimulus voltage at the enabled neighborhood channel. The result is shown in Fig. 4.5, by putting a biphasic signal of maximum amplitude ±10V into Vout with turning-off Mp2 and Mn2 to make the driver disable, 12-V devices remain stable without any overstress issue.

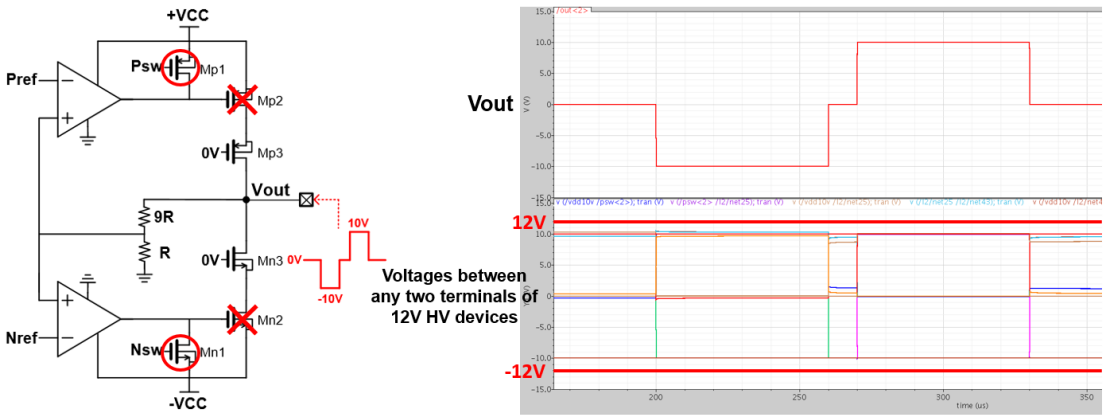


Fig. 4.5 Driver overstress test under multi-channel consideration.

4.2 Measurement Results

The proposed monopolar biphasic voltage stimulator has been fabricated in TSMC 0.25-μm HV USG 2.5-V/5-V/12-V CMOS process, and the microphotograph of the chip is shown in Fig. 4.6, which consists of 4 stimulus drivers, switch control circuits, positive voltage DAC, negative voltage DAC, bias circuit, and decoder. Total area of the silicon chip is 1.952 × 1.317mm^2, and it has been bonded on PCB for measurement.

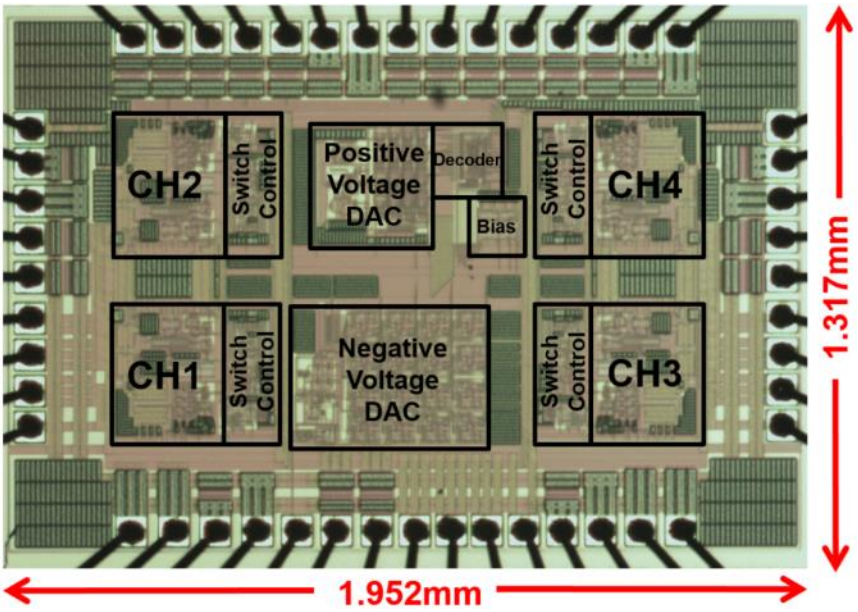
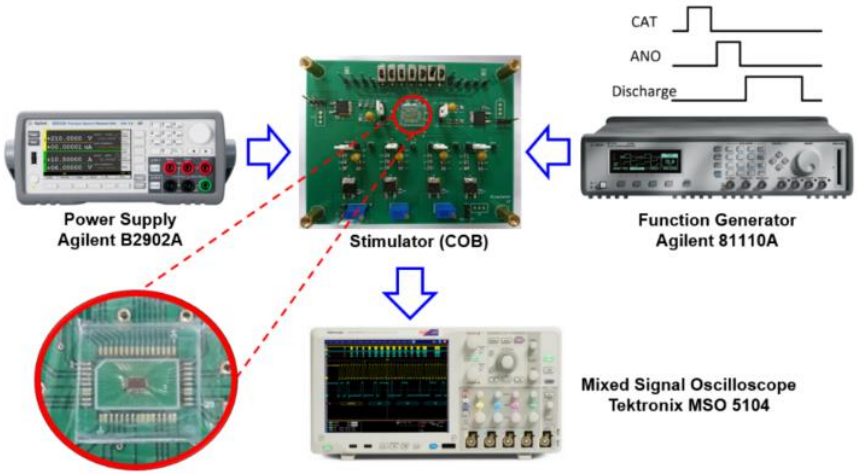
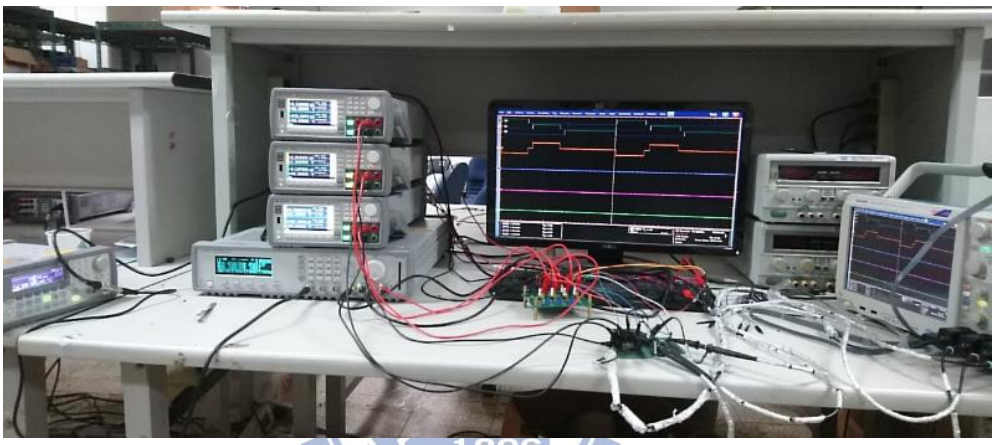


Fig. 4.6 Microphotograph of the 4-channel stimulator chip with a die size of 2.57mm^2, which was fabricated in a 0.25-μm 2.5-V/5-V/12-V CMOS process.

Fig. 4.7 (a) shows the measurement setup. All powers of the chip are provided by Agilent B2902A, so it is also used to measure power consumption. Input pulse signals CAT, ANO, and Discharge are controlled by function generator, Agilent 8110A. Tektronix MSO 5140 is used to observe the waveforms of the stimulation. The whole measurement environment is shown in Fig. 4.7 (b).



(a)



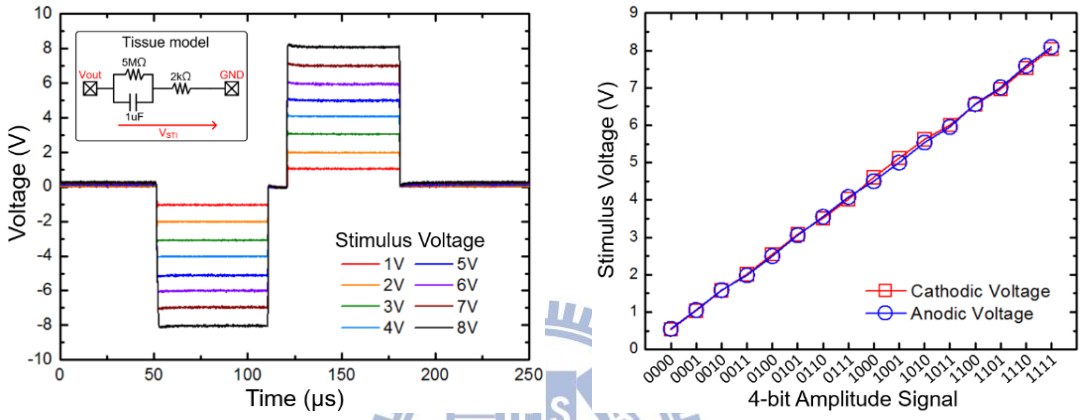
(b)

Fig. 4.7 The measurement setup. (a) Input/output relationship between power supply, function generator, oscilloscope, and the chip. (b) The measurement environment. The outputs of stimulator are connected to test electrode-tissue equivalent circuit.

Loading impedance value of electrode-tissue in the measurement are R_f=5MΩ, C_{dl}=1μF, and R_S=2kΩ. The pulse width of CAT and ANO signals are 60μs, and 110μs duration is set for Discharge signal, and a 10μs delay between CAT to ANO, and ANO to Discharge. The 4-bit digital input AMP[3:0] and responding output voltage amplitudes are in Table 4.1, and Fig. 4.8 (a) shows 8 different voltage levels of stimulator output. Besides, the line photo of 16-step cathodic/anodic voltages is shown in Fig. 4.8 (b), and there are small mismatching between cathodic/anodic voltages.

Table 4.1 4-bit digital input AMP[3:0] and responding output voltage

AMP[3:0]	0000	0001	0010	0011	0100	0101	0110	0111
Output Voltage	0.5V	1V	1.5V	2V	2.5V	3V	3.5V	4V
AMP[3:0]	1000	1001	1010	1011	1100	1101	1110	1111
Output Voltage	4.5V	5V	5.5V	6V	6.5V	7V	7.5V	8V



(a) (b)

Fig. 4.8 The measurement result of stimulator output. (a) Biphasic stimulus voltage under R_S=2kΩ. (b) Line photo of cathodic/anodic voltages with 4-bit amplitude signal.

Although the 4 channels cannot be chosen simultaneously, they can be programmed to change rapidly, as the function verified in Fig. 4.9. The 2-bit C[1:0] control signals make the stimulator more flexible to different stimulation spots.

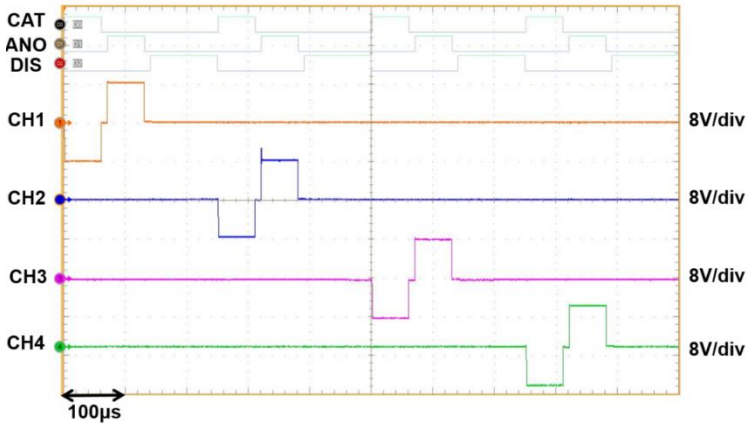
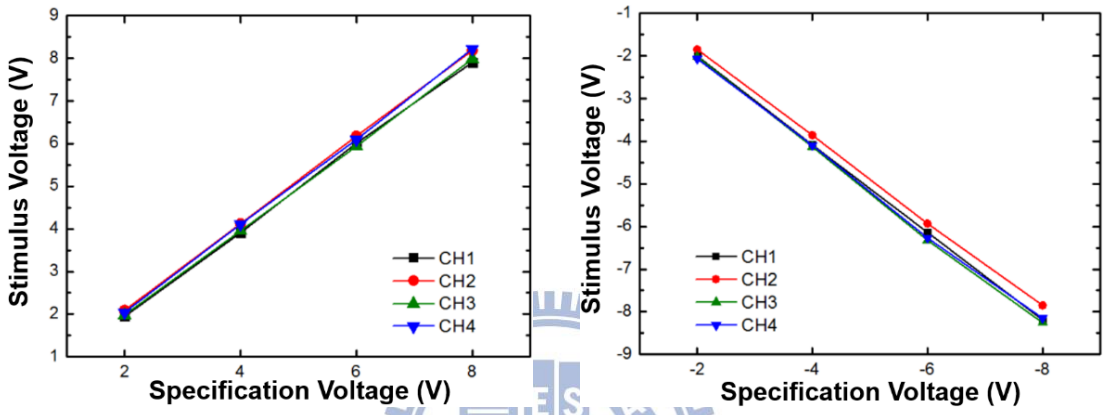


Fig. 4.9 Changing operation among different output channels of the stimulator.

A comparison of 4 output channels of one chip is in Fig. 4.10, from the measurement results it can be observed that small variations exist among those channels. And the percentage of cathodic/anodic stimulus voltage mismatching is calculated by Eq. (4-1), which also shown in Fig. 4.11 is under 4.3%.

$$\text{Voltage Mismatch}=\frac{||V_{CAT}|-V_{ANO}|}{|V_{CAT}|}\times 100\% \quad (4\text{-}1)$$



(a) (b)

Fig. 4.10 Output voltages of each channel. (a) Positive outputs. (b) Negative outputs.

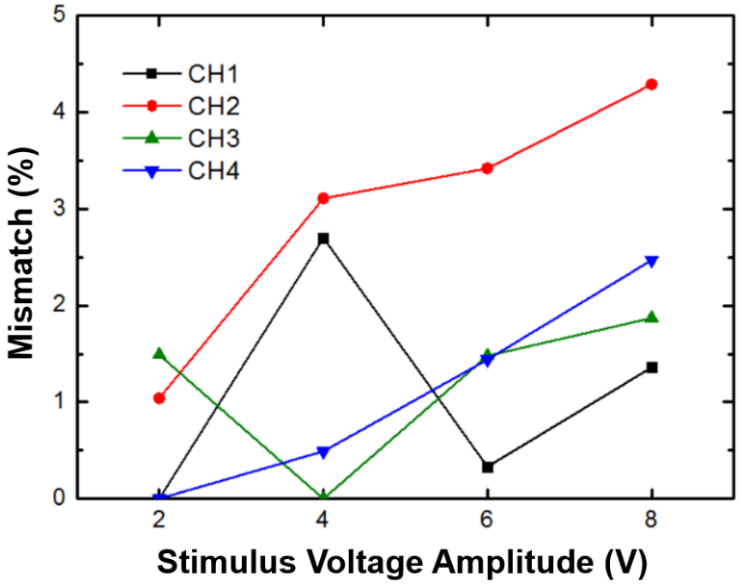


Fig. 4.11 The mismatch of cathodic/anodic stimulus voltage of each channel.

Discharge function designed is for remedying the mismatch. The residual charges on C_{dl} can be minimized after discharge phase. If there is no discharge, the residual charges ($Q_{w/o\ dis}$) can be obtained by Eq. (4-3), which ΔV equals to the voltage difference between absolute value of cathodic/anodic stimulus voltage (Eq. (4-2)), and also can be calculated from Eq. (4-1).

$$\Delta V=|V_{CAT}|-|V_{ANO}|=|V_{CAT}|\times \text{Voltage Mismatch} \quad (4\text{-}2)$$

$$Q=C_{dl}\times\Delta V \quad (4\text{-}3)$$

Under the worst case, stimulus voltage is ±8V and voltage mismatch is 4.3%, which cause the ΔV=344mV. With C_{dl} of electrode model is 1μF in the measurement, $Q_{w/o\ dis}$ is 344nC. The residual charges decrease as Eq. (4-4).

$$Q(t)=Q(0)\times e^{\frac{-t}{RC}} \quad (4\text{-}4)$$

R_S is 2kΩ, so the time constant (RC) equals to 2ms. In measurement, stimulus period is set to 250μs, cathodic stimulus pulse width is the same duration as anodic pulse, which is 60μs, and the interphase delay cathodic to anodic is 10μs, thus the time left for C_{dl} to discharge itself is 250μs−(60μs+10μs+60μs)=120μs. As a result, it can only decrease by $e^{-0.06}\approx0.942$ times of the residual charges. $Q_{w/o\ dis}(t)\approx324$nC.

With discharge, ΔV can be reduced after anodic stimulation. According to measurement results, ΔV will be less than 10% of the above value. Take 34.4mV as an example, the residual charges Q_{dis} is only 34.4nC left.

In real treatment for Parkinson's disease, a stimulation frequency usually sets to 130Hz (≈7.6923ms) [10], assume all the durations of cathodic, anodic, and discharge are as above, there is still 7.4423ms allows the residual charges Q_{dis} to decrease $e^{-3.72115}$ times, in other words, 2.4% of 34.4nC will left. The rest of charge is less than 0.9nC, which is safe enough for biomedical application according to [29] and [30] indicate that the safe charge density of Pt electrode is less than 50μC/cm^2.

After charge balance has been discussed, we talk about water window during cathodic/anodic stimulation. The water window of the electrode should be within a specific range as mentioned in chapter 2.1, and the range of –0.6V~0.6V is safe for all materials. Fig. 4.12 shows the measurement result of water window under ±8V, and Table 4.2 presents the ΔV of C_{dl} under different loading with ±8V stimulus voltage, both results confirm the safety issue of implantable electrodes.

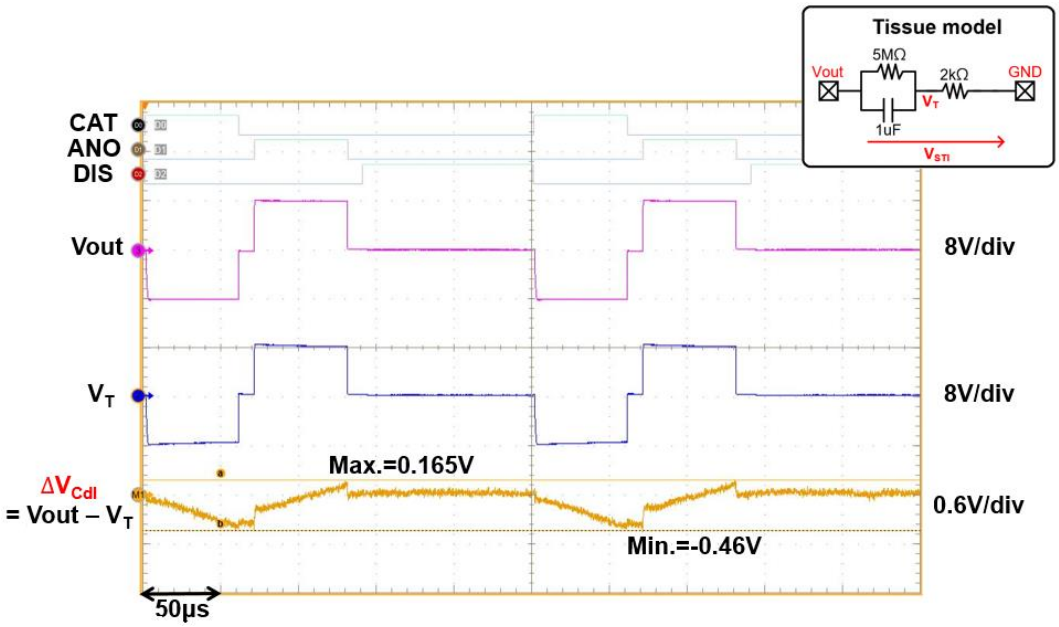
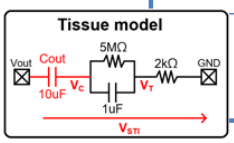


Fig. 4.12 Water window test of electrodes under ±8V.

Table 4.2 Water window test under different loading with ±8V stimulus voltage

Load	ΔV of C_{dl}
R_S=1kΩ	-0.588V ~ 0.181V
R_S=2kΩ	-0.46V ~ 0.165V
R_S=2kΩ, w/ Cout	-0.305V ~ 0.653V



If Eq. (4-3) is changed to Eq. (4-5), then the relationship between stimulus voltage and water window of double layer capacitor can be calculated. In Eq. (4-5), I_{sti} means the stimulus current, which is equivalent to stimulus voltage V_{sti} divided by output load resistor R_S (2kΩ). And Δt represents the pulse width of cathodic/anodic stimulation pulse, as mentioned before, 60μs will be used for the calculation. Since the water window has a limitation of −0.6V~0.6V, ΔV in Eq. (4-5) defined as 0.6V.

$$Q=I_{sti}\times\Delta t=\frac{V_{sti}}{R_S}\times\Delta t=C_{dl}\times\Delta V \tag{4-5}$$

From Eq. (4-5), we obtain the result as $\frac{V_{sti}}{C_{dl}}=0.6V\div 60\mu s\times 2k\Omega=2\times 10^7$. If C_{dl} is moved to the right hand side of the equation, it causes that $V_{sti}=2\times 10^7\times C_{dl}$. It can be told from the result that the maximum stimulus voltage will be decide by the value of double layer capacitor, and it's a linear relation. In this case, C_{dl}=1μF, which means the maximum stimulus voltage for the safety consideration cannot larger than 20V, and the maximum equivalent stimulus current is 10mA.

The MCP system serves as high-voltage generator, it provides ±9V to the stimulator, and in the following measurement result shows in Fig. 4.13, full-scale of ±8V stimulus voltage can still be delivered by stimulator under the tissue loading R_S=500Ω. Also, considering SoC integration with other circuit blocks, the ±VCC power of the stimulator may not be so stable, thus the results of power variation test are indicated in Table 4.3, where proves the chip has a good ability against power variation.

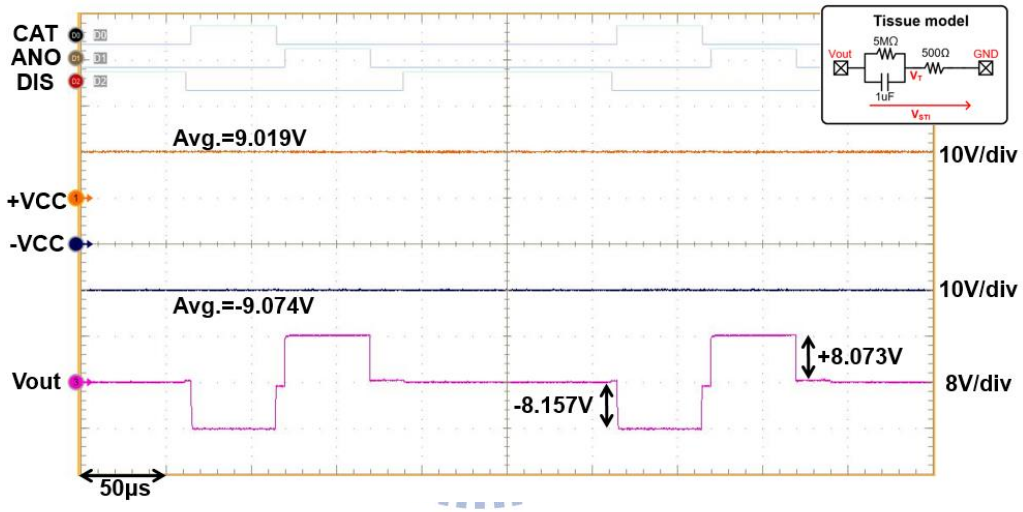


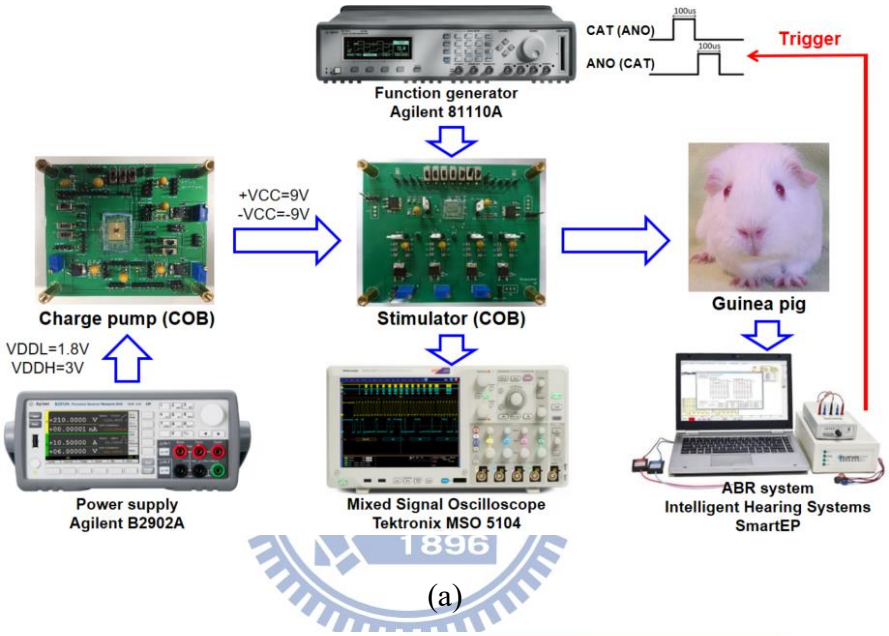
Fig. 4.13 ±VCC (±9V) provided by MCP system for stimulator to deliver ±9V under R_S=500Ω.

Table 4.3 Power variation test of maximum stimulus voltage

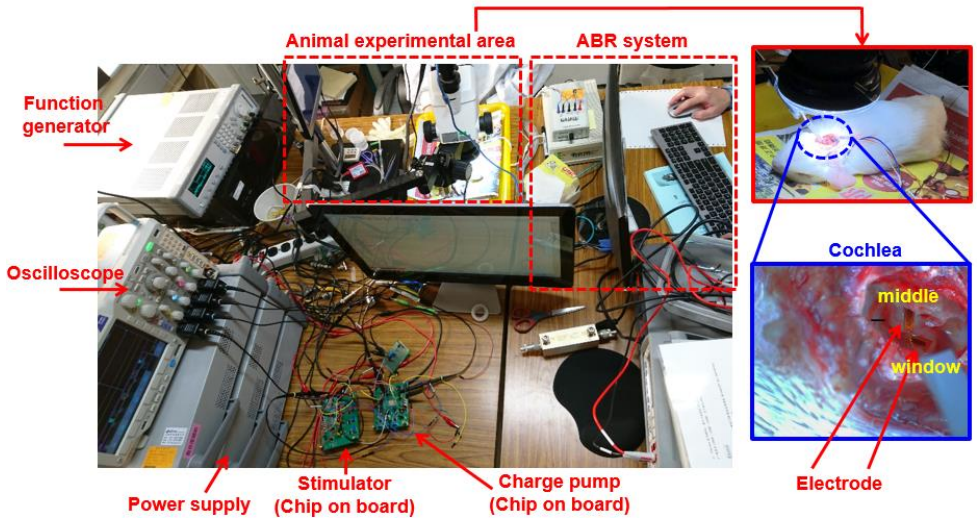
Supply Voltage	Stimulus Voltage (Cathodic/Anodic)
±10V	-8.019V / 8.171V
±9V	-8.027V / 8.166V
±8.5V	-7.974V / 8.003V

4.3 Animal Experiment Results

Functions of the proposed stimulator chip are verified with both electrical measurements and in-vivo animal tests. Fig. 4.14 (a) is the block diagram of experimental setup, and Fig. 4.14 (b) shows the experimental environment.



(a)



(b)

Fig. 4.14 (a) Experimental setup of in-vivo test. (b) The whole experiment environment under in-vivo test.

Under in-vivo test on guinea pigs, the origin commercial stimulator (Isolated pulse stimulator A-M Systems Model 2100) is replaced by the stimulator chip. And the power of stimulator (±VCC), are generated by MCP system directly. Then the plate electrodes (length=1.397mm, width=0.392mm, used Pt+IrO_2 as material) are placed on the surface of cochlear bone and round window.

After deciding the stimulation channel and setting a proper stimulus voltage, the computer delivers continuous command to auditory brainstem response (ABR) system, and then the ABR system triggers the function generator to make stimulator chip generate biphasic stimulation pulses. Once the electrical stimulation is done, the action potentials are recorded by the ABR system. By observing the Wave IV of evoked ABR (EABR) waveforms [31] in Fig. 15, and calculating the action potential amplitude as shown in Fig. 16 [32]-[34], it can be proved that the proposed stimulator chip is as good as the commercial stimulus equipment for biomedical applications.

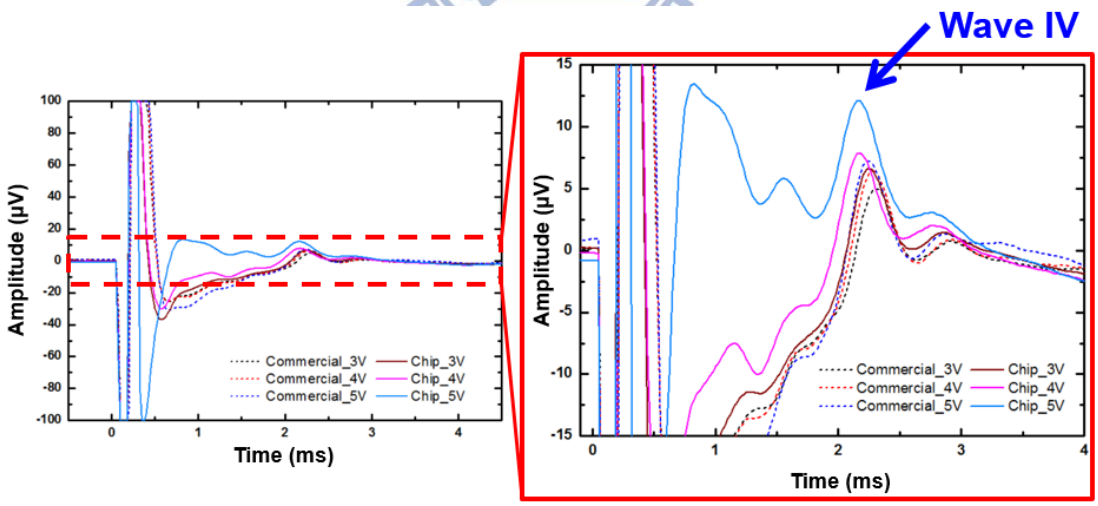


Fig. 4.15 The evoked Wave IV of EABR waveforms on guinea pig induced by the commercial stimulator and the proposed stimulator silicon chip.

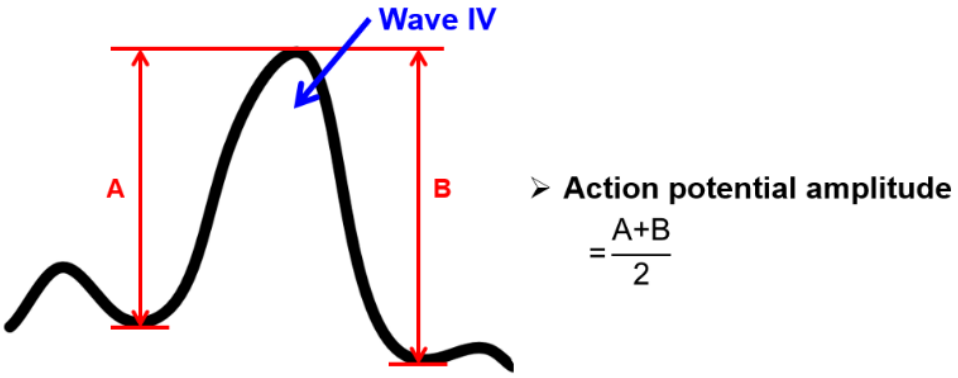
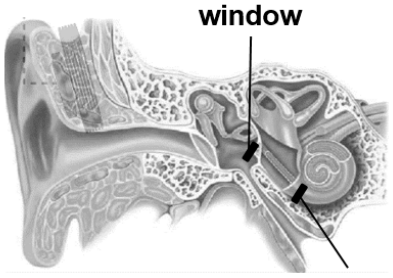
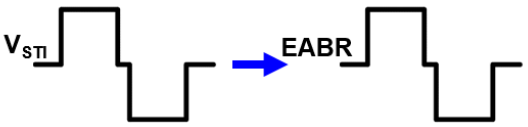
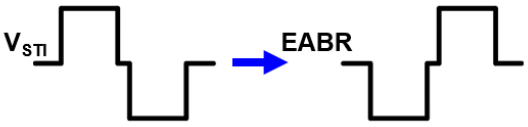


Fig. 4.16 The method of calculating action potential amplitude.

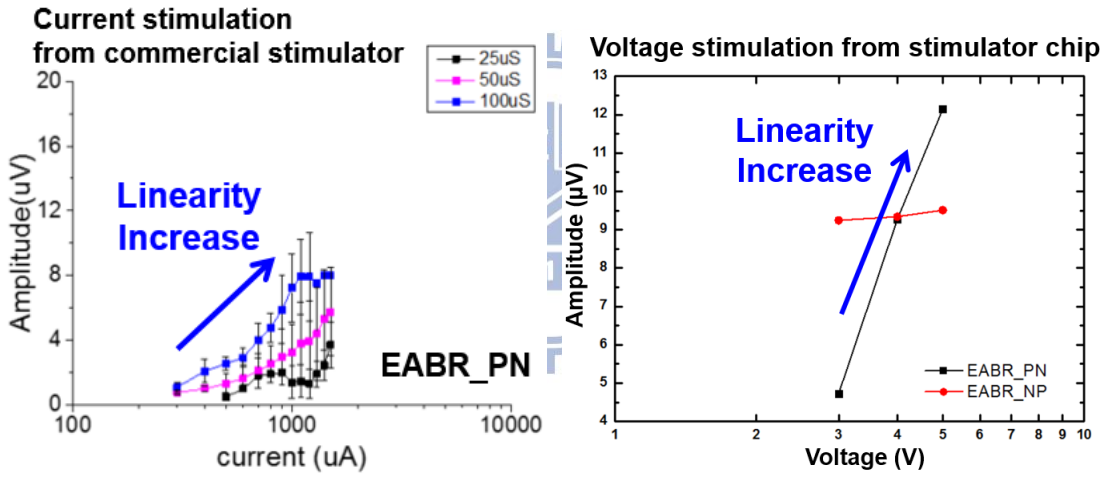
During the experiment, it has been found that if electrode GND is placed on round window, EABR signal will be same phase as stimulation pulse at first. On the contrary, EABR will be opposite phase to stimulation pulse at first when electrode GND is on middle, as illustrated in Table 4.4.

Table 4.4 Corresponding EABR waveform to electrode GND position

Electrode GND position (Placed on window or middle)	Stimulation pulse vs. EABR waveform (Evoked Auditory Brainstem Response)
	GND on window (PN→PN) 
	GND on middle (PN→NP) 

For observing convenience, the EABR waveform is preferred to react positive to negative (PN) than negative to positive (NP), because the waveform shows in NP will hide the Wave I (the first peak) of EABR reaction. Also, the action potential amplitude of Wave IV (calculated by Fig. 4.16) indicates that waveform shows in PN

increase linearity when stimulus amplitude (the X axis) is in log scale, which is more reasonable than waveform is in NP as shown in Fig. 17 (b). Fig. 17 presents the action potential reaction stimulate by commercial stimulator delivering current stimulation and stimulator chip delivering voltage stimulation. In Fig. 17 (a) different pulse widths are given, it can be told from the amplitude of action potential that 100μs cathodic/anodic pulse width has the best therapeutic effect under current stimulation. However, both curves in Fig. 4.17 (b) are stimulated by 100μs cathodic/anodic pulse width. As a result, the action potential amplitude evoked by stimulus voltage (Fig. 17 (b)) seems larger than those induced by stimulus current (Fig. 17 (a)).



(a) (b)

Fig. 4.17 Action potential amplitude stimulate by (a) commercial stimulator with current stimulation using different cathodic/anodic pulse widths and (b) stimulator chip with voltage stimulation using 100μs cathodic/anodic pulse width.

4.4 Measurement Results of Other Applications

4.4.1 Modified for Bipolar Stimulator

With two stimulator chips, the proposed monopolar stimulator can be used as bipolar configuration. Fig. 4.18 illustrates the output driver that includes two chips.

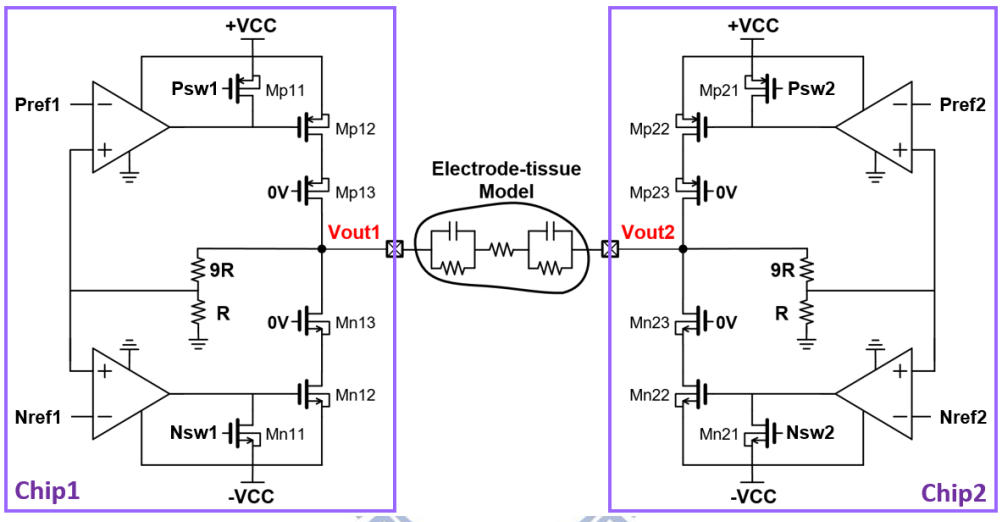


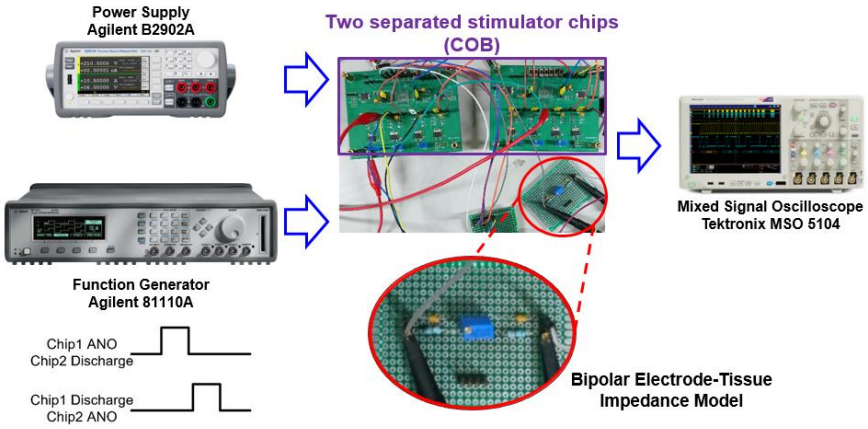
Fig. 4.18 Output driver includes two chips for bipolar configuration.

Using as bipolar stimulator, negative output voltage is no longer needed. By delivering bi-direction stimulus voltage to electrode-tissue model, biphasic stimulation pulses can pass through the impedance. As a result, Nref1 and Nref2 will be 0V at most of the time, which means both negative DACs are off.

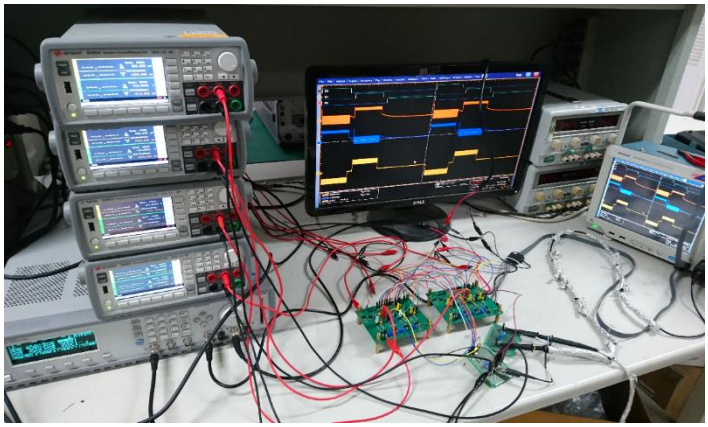
There are also four states in bipolar operation, high-Z state, cathodic stimulation, anodic stimulation, and discharge. During high-Z state, both drivers in two chips are in high-Z. All switches (Psw1, Nsw1, Psw2, and Nsw2) are on, and break the feedback loop as explained in section 3.4. When in stimulation mode, if we define the voltage pass from chip1 to chip2 as cathode, the inverse direction will be anode. For bipolar cathodic (anodic) stimulation, chip1 (chip2) delivers the stimulus voltage to

Vout1 (Vout2), meanwhile chip2 (chip1) is in discharge operation to make Vout2 (Vout1) 0V. Stimulus voltage at Vout1 (Vout2) comes from Pref1 (Pref2), by turning off Psw1 (Psw2), Mp12 (Mp22) serves as power MOSFET and the positive side feedback loop is functional. In the phase of bipolar discharge, both positive side feedback loop are break due to Psw1 and Psw2 are on, but Nsw1 and Nsw2 are off to make negative side feedback loops work. The reference voltage (Nref1 and Nref2) are biased at 0V and thus the impedance is grounded since Vout1 and Vout2 are 0V.

The measurement setup is a little different from monopolar configuration, which is shown in Fig. 4.19.



(a)



(b)

Fig. 4.19 Bipolar stimulator measurement. (a) The measurement setup. (b) The measurement environment.

The impedance is the same as monopolar measurement, both R_S=2kΩ. Since it is bipolar configuration, there are two electrode model instead of one, as in Fig. 4.19 (a), which includes two pairs of C_{dl} and R_f. The measurement result is shown in Fig. 4.20, the biphasic pulses do generate between Vout1 and Vout2, but the visible ripples exist.

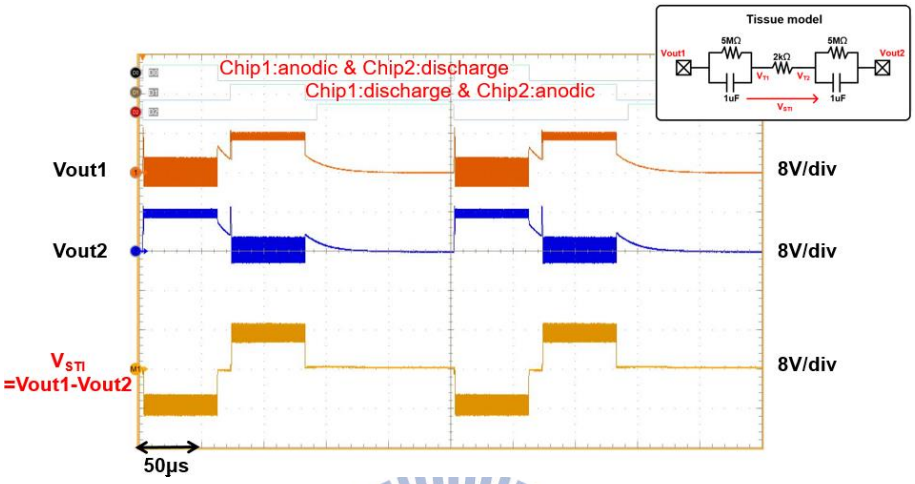
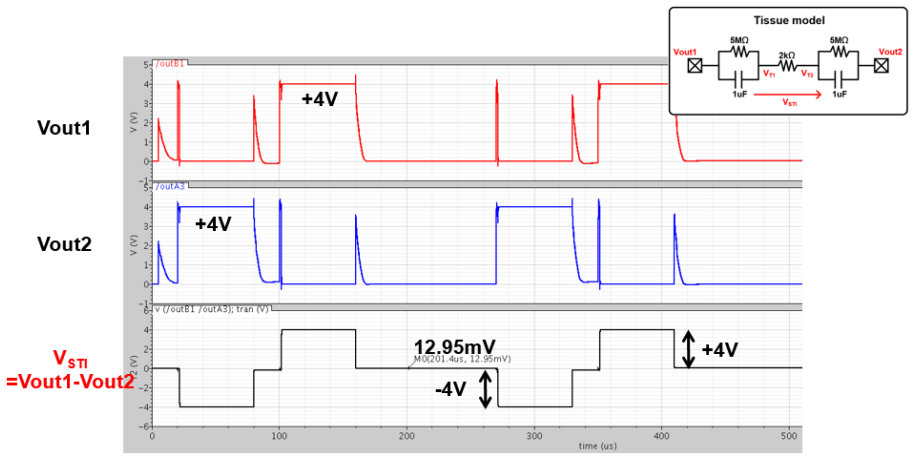
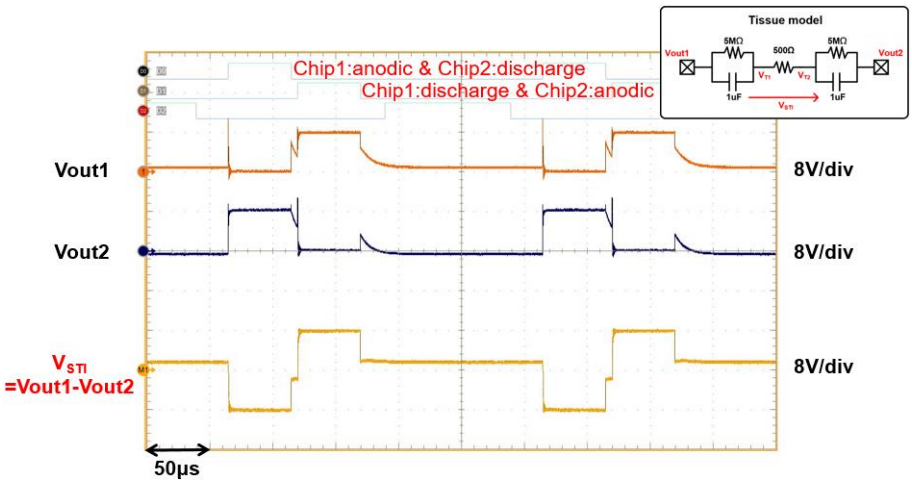


Fig. 4.20 Measurement result of bipolar stimulator with R_S=2kΩ.

Those ripples are about 3MHz, it may happened because of the discharge operation is not exactly grounded by a switch connects to GND, but similarly grounded by delivering 0V to Vout1 or Vout2 through feedback loop. Therefore, the simulation has been checked with R_S=2kΩ, and a smaller impedance R_S=500Ω has used to replace the original one in the measurement. Both results in Fig. 4.21 show there are no ripple in the stimulus voltage.



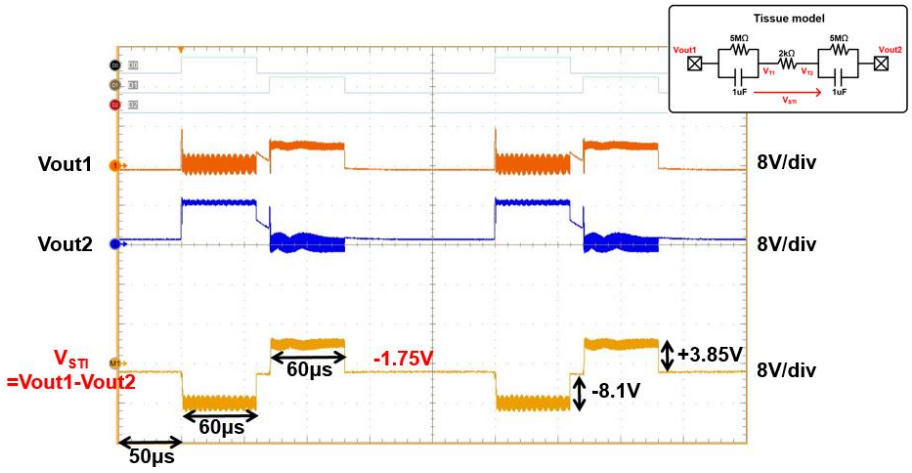
(a)



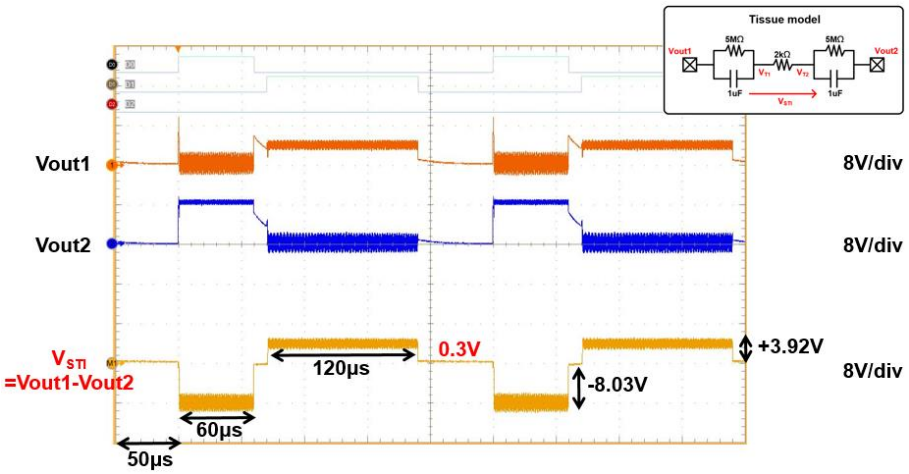
(b)

Fig. 4.21 (a) Simulation result of bipolar stimulator with R_S=2kΩ. (b) Measurement result of bipolar stimulator with R_S=500Ω.

By using two chips to complete the stimulation, Pref1 and Pref2 are from separate positive DAC, so the amplitude of the cathodic/anodic stimulus voltage can be different. Under the following measurement, cathodic pulse width is 60μs with amplitude ±8V. The amplitude of anodic voltage is set to +4V (half of the amplitude of cathodic voltage) with 60μs pulse width in Fig. 4.22 (a) and 120μs pulse width in Fig. 4.22 (b). Comparing the results in Fig. 4.22, ΔV decreases a lot when the anodic pulse width is twice than cathodic, thus reduces the unbalanced charge to micro-Coulomb level [35].



(a)



(b)

Fig. 4.22 Unbalanced charge left when cathodic pulse width is 60μs with amplitude −8V and anodic voltage is +4V with (a) pulse width 60μs and (b) pulse width 120μs.

4.4.2 8-Channel Monopolar Stimulator System

This design based on the idea of portable usage. As mentioned, the high-voltage generator provides ±VCC to the stimulator, which realized in another silicon chip called MCP system. Fig. 4.13 is measured when stimulator chip and MCP chip are bonded on their own PCB. In other words, two separate systems connected by wires. Now, they are related to each other since they are bonded on a piece of PCB. And two stimulator chips extend the output channels from 4-channel to 8-channel. This PCB also contains micro-USB socket, so it can be powered like our cellphone. During the whole measurement, power supply machines are replaced by USB charger. Fig. 4.23 illustrates the block diagram of 8-channel monopolar stimulator system, and Table 4.5 lists the specifications of the proposed system.

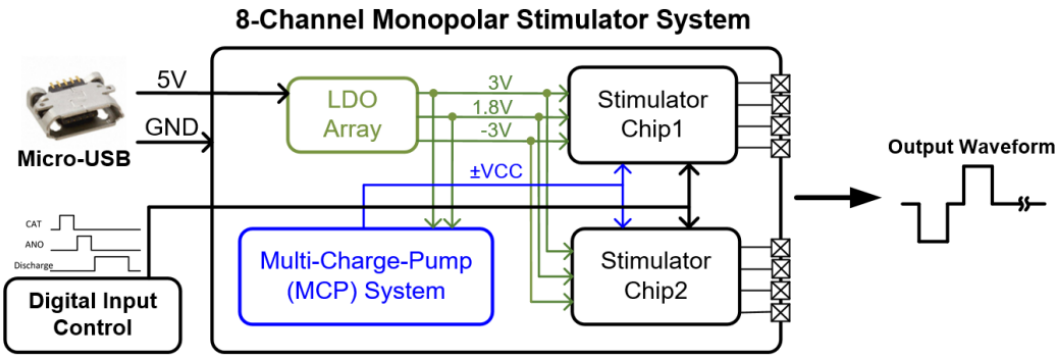
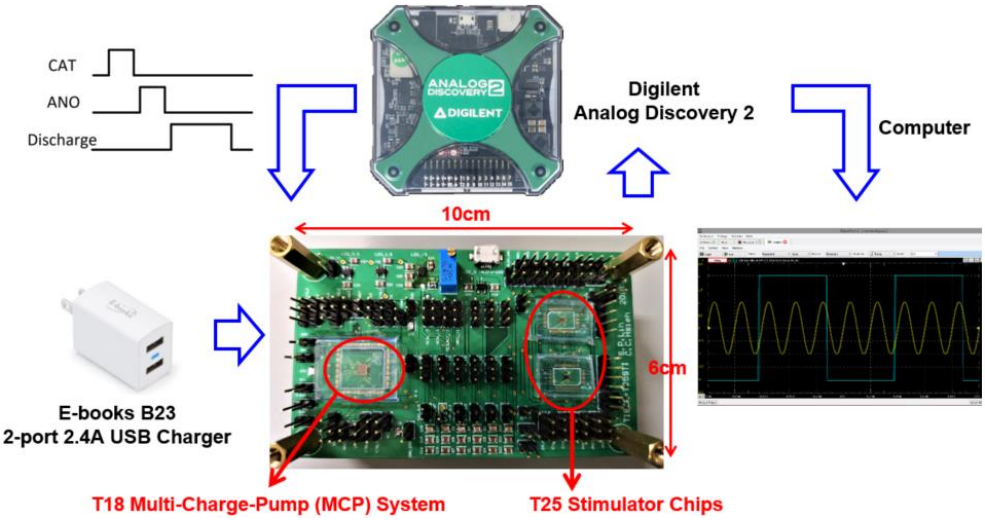


Fig. 4.23 Block diagram of proposed 8-channel monopolar stimulator system.

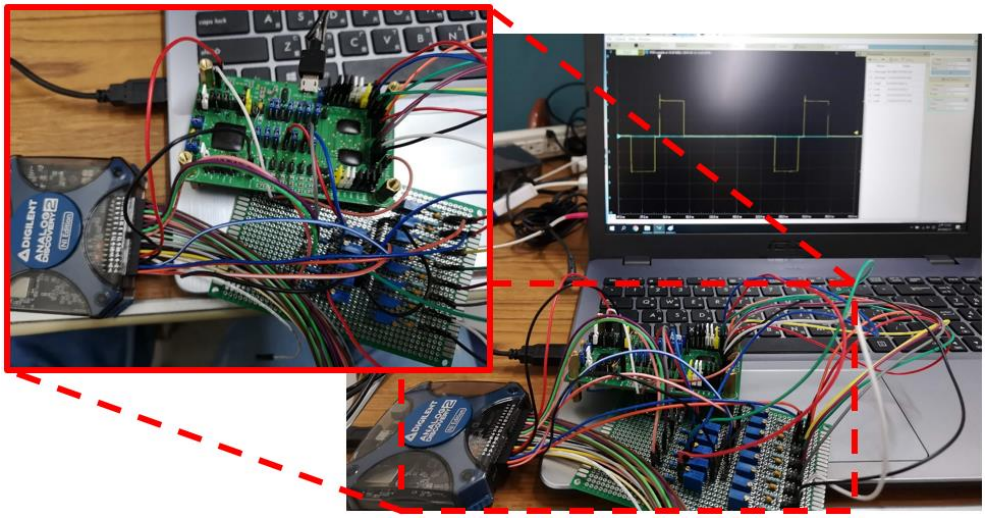
Table 4.5 Specifications of the proposed stimulator system

Process	**0.18-μm 1.8V/3.3V CMOS process** (MCP) **0.25-μm 2.5V/5V/12V CMOS process** (Stimulator)
Stimulation Pattern	**Monopolar Biphasic Voltage**
Supply Voltage	**5V** (From USB)
Output Amplitude	**±0.5V ~ ±8V** (Amplitude step: 0.5V)
Pulse Width	**20 ~ 450μs**
Stimulation Frequency	**2 ~ 250Hz**
Channel Number	**8 channels**
Output Load Range	**R_S ≥ 500Ω**

Not only is the PCB designed for easy carrying, the function generator and oscilloscope also replaced by a small device known as Analog Discovery 2 (AD2). All you have to do is to download the "WaveForms" from the official site of Digilent, and install the software on your computer, then it can be served as a multi-functional device. The measurement setup and measurement environment are shown in Fig. 4.24.



(a)



(b)

Fig. 4.24 Measurement for 8-channel stimulator system by AD2. (a) Measurement setup. (b) Measurement environment.

Fig. 4.25 is the control signals CAT, ANO, and Discharge given by AD2 as shown in Fig. 4.24 (a), with this input pulse pattern, biphasic output pulses can be generated. But first, the outputs of MCP system are measured in Fig. 4.26 to make sure ±VCC achieve the specifications. After the supply powers of stimulator have been confirmed, Fig. 4.27 demonstrates stimulator output amplitude with low, middle, and high voltage levels.

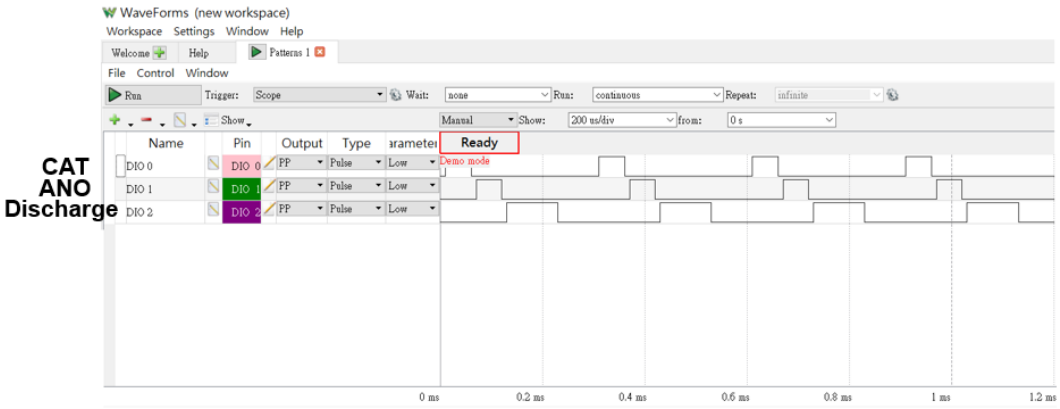


Fig. 4.25 Control signal CAT, ANO, and Discharge given by AD2.

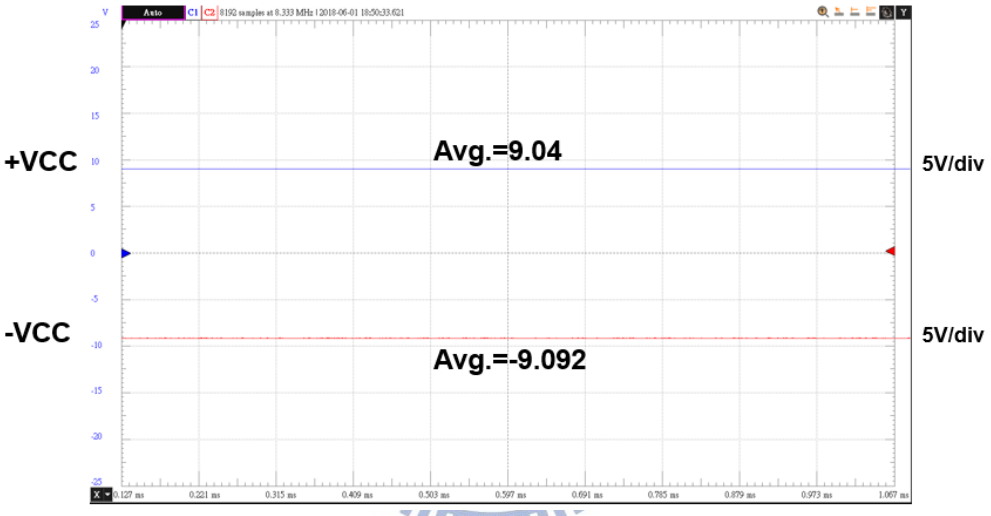
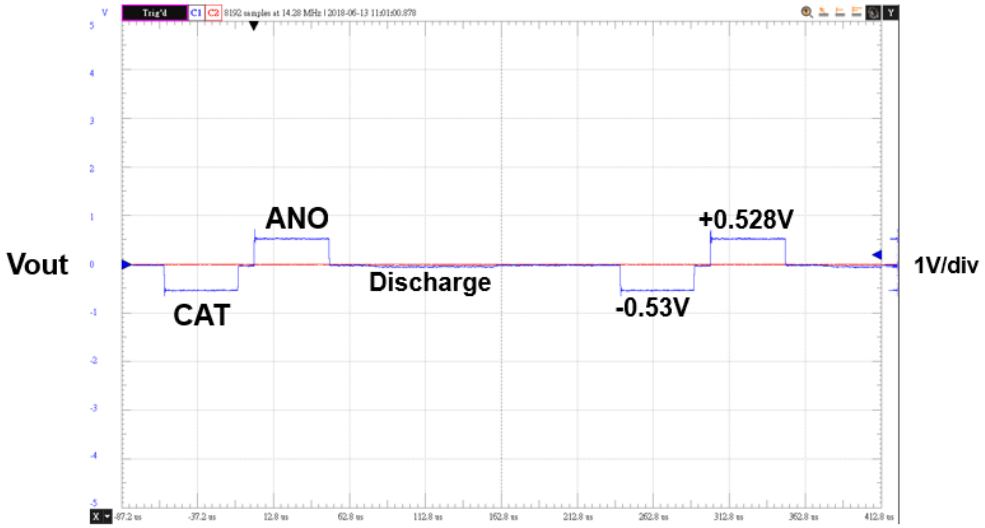
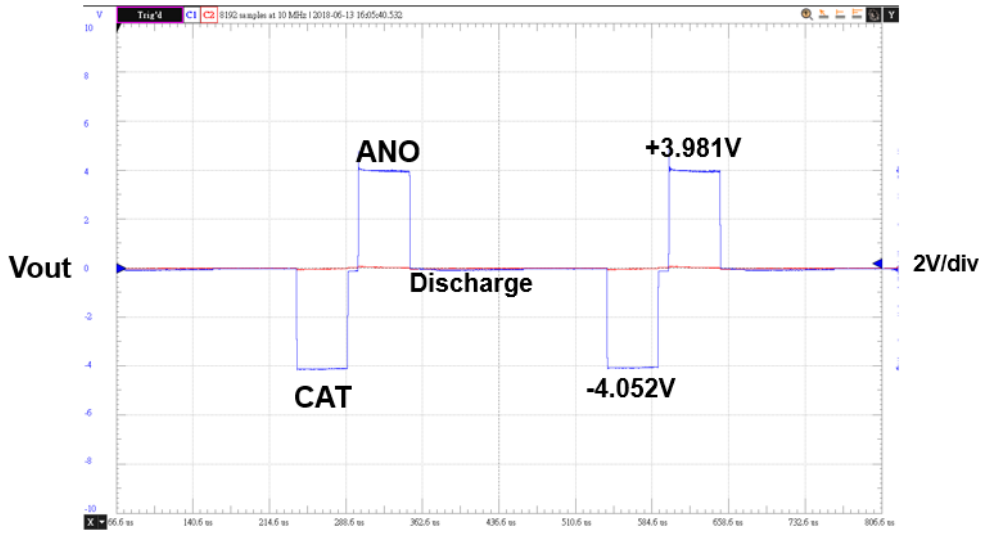


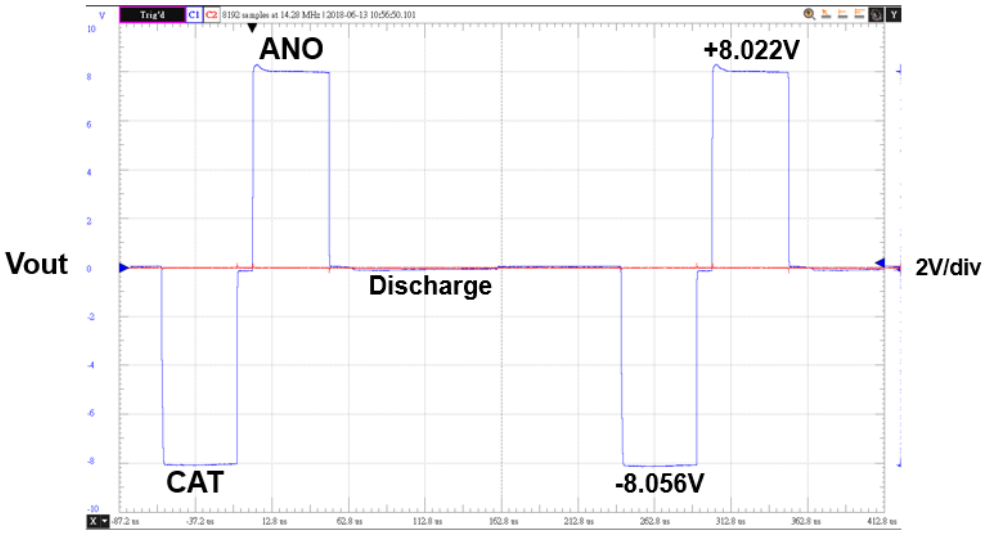
Fig. 4.26 ±VCC (±9V) provided by MCP system.



(a)



(b)



(c)

Fig. 4.27 Stimulator output amplitude with different voltage levels. (a) Low level, ±0.5V. (b) Middle level, ±4V. (c) High level, ±8V.

4.5 Summary

The performances of the stimulator chip are summarized in Table 4.6. The measurement results are close to the simulation results and stick to the specifications. The standby power increase may due to the leakage of voltage reference DAC circuit, but it can be reduced by adding enable switch. Table 4.7 lists the performance of this work and compare to other related designs.

Table 4.6 Summary of the fabricated stimulator chip

	Spec.	Pre-layout Simulation	Post-layout Simulation	Measurement Results
V_{DD} (From power management unit)	1.8V / 3V			
V_{CC} (From charge pump)	-3V / -10V / 10V			
Stimulus Voltage Amplitude (V) (Amplitude step=0.5V, Under R_S=2kΩ)	±1.0, ±2.0, ±3.0, ±4.0, ±5.0, ±6.0, ±7.0, ±8.0,	-1.001, 1.004, -2.002, 2.004, -3.003, 3.003, -4.004, 4.004, -5.005, 5.004, -6.006, 6.005, -7.007, 7.006, -8.008, 8.006,	-1.012, 1.010, -2.006, 2.002, -3.015, 3.009, -4.008, 4.007, -5.013, 5.008, -6.010, 6.001, -7.001, 7.002, -8.011, 8.013,	-1.037, 1.055, -2.012, 1.985, -3.080, 3.057, -4.021, 4.080, -5.119, 5.000, -6.006, 5.954, -6.968, 7.016, -8.038, 8.096,
Cathodic / Anodic Matching	Minimum	<1%	<1%	<4.3%
Standby Power	Minimum	520μW	636μW	853μW
Process	TSMC 0.25-μm HV USG 2.5V/5V/12V CMOS Process			

Table 4.7 Performance comparison

	[40] 2013 TBCAS	[41] 2007 JSSC	[42] 2010 JSSC	This work
CMOS Process	0.18μm HV	0.35μm HV	0.18μm HV	0.25μm HV
Max. Voltage	11.5V	20V	±10V	±8V
Cathodic/Anodic Mismatching	<0.45%	<5%	<2.9%	<4.3%
Supply Voltage	0~12V	0~22.5V	±1.8V/±12V	1.8V/±3V/±9V
Standby Power	NA	>100μW	NA	853μW

Chapter 5
Conclusions and Future Works

5.1 Conclusions

A silicon chip for neuromodulation stimulation has been designed, fabricated, and verified with both electrical measurements and in-vivo animal tests successfully. Without device overstress, p-n junction breakdown issue, or p-n junction forward-leakage problem under 20V compliance voltage and negative voltage operation. The proposed chip is able to deliver adjustable stimulus voltage from ±0.5V to ±8V (±0.5V per step) with monopolar configuration for biomedical applications against wide range of loading impedance (R_S above 500Ω).

The advantage of flexible inputs control and tiny physical dimension (the die size is only 1.952×1.317mm^2) makes the stimulator chip can be integrated with other circuit blocks together into a SoC for implantable usage easily. Moreover, as demoed in section 4.4, the proposed chip is able to transform to different applications with proper hardware.

5.2 Future Works

5.2.1 Parkinson's Disease Application

By using digital control such as Verilog coding, the input signal CAT, ANO, Discharge, and AMP[3:0], as illustrated in the top of Fig. 5.1, the biphasic output pulses will become stepwise biphasic ramp waveform [10]. When the enable signal of stimulator is rising edge, the stimulus waveform should ramp up. As long as the enable signal maintain logic high state's time is long enough, the target stimulus amplitude should hold after ramp up. Otherwise, the output waveform will ramp down immediately when enable signal is falling edge. Fig. 5.1 shows the detail of output waveform (Vout), and the pattern of ramp pulse is decided by the rising, falling edge, and logic high state's time of enable signal.

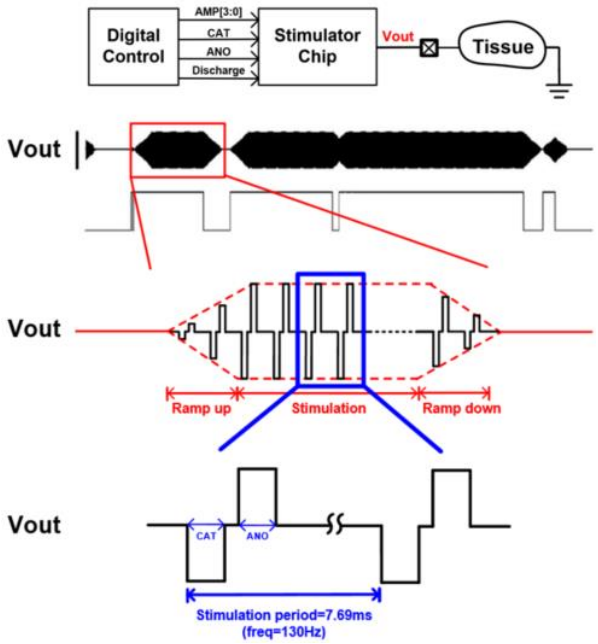


Fig. 5.1 Ramp stimulation pattern for Parkinson's disease application.

5.2.2 Stimulator with Output Capacitor

Some research indicates that adding DC blocking capacitor at the output of stimulus driver can ensure there is no unpredictable current flows into body [36], [37]. Fig. 5.2 shows three different stimulation patterns by using DC blocking capacitor ((a) monopolar biphasic stimulation, (b) bipolar biphasic stimulation, and (c) monopolar monophasic stimulation). But unfortunately, those capacitors are usually in micro-scale level for desired stimulus current outputs from stimulus driver completely due to RC time constant from the tissue impedance (R_S) and DC blocking capacitor. For micro-scale capacitance, it is difficult to be realized on-chip. Furthermore, even if those capacitance will be add off-chip, a longer duration of discharge time is needed to discharge the residual charge on tissue (also can be calculated by the formula of RC time constant). To reduce the scale of blocking capacitor, a high-frequency current-switching (HFCS) technique is used, and it can scale down those capacitor to pico-scale level. Fig. 5.3 shows the circuit design based on monopolar monophasic stimulation [38], [39].

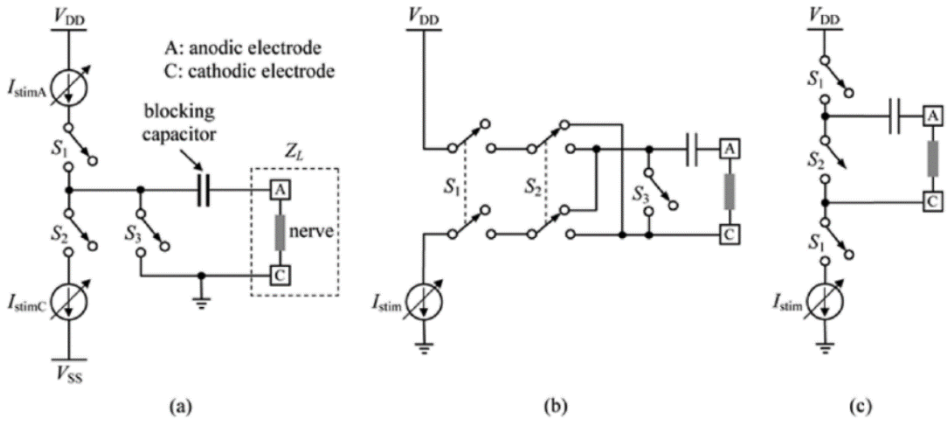


Fig. 5.2 Conventional stimulator output stage configurations for two-electrode setup. (a) Dual supplies with active cathodic and active anodic phases. (b) Single supply with active cathodic and active anodic phases. (c) Single supply with active cathodic phase and passive anodic phase.

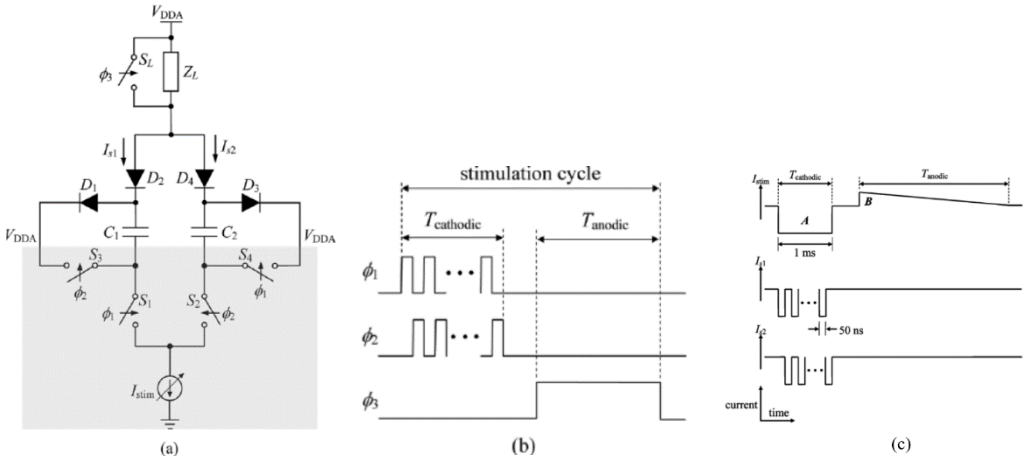


Fig. 5.3 (a) HFCS technique stimulus driver. (b) Timing waveforms. (c) The results of stimulation.

After adding a DC blocking capacitor at output of stimulator, the monopolar structure shown in Fig. 5.4. With the output capacitor Cout, redundant DC leakage will not pass from Vout to V_T, thus improved the safety concern when used in human body. When stimulation is happening, Cout will couple the voltage of Vout to V_T, so this extra capacitor will not have impact on stimulus waveform that is delivered to tissue.

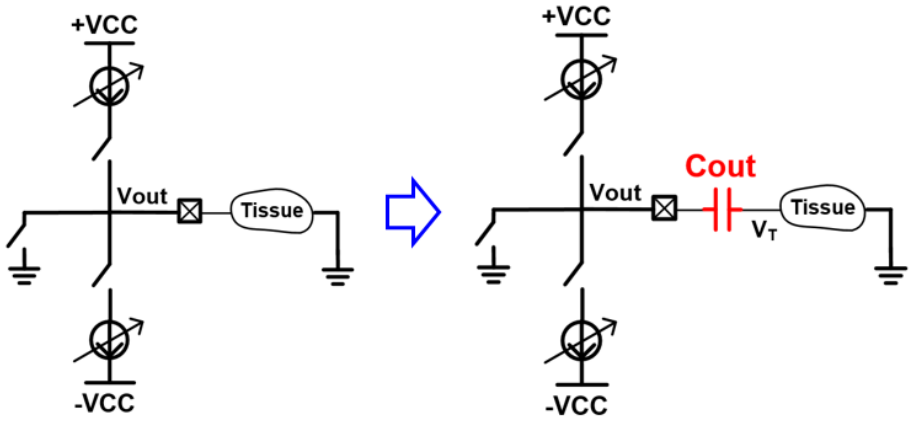


Fig. 5.4 Stimulus driver of monopolar configuration with output capacitor Cout.

Another design consideration is that negative power supply (–VCC) is no longer needed due to the characteristic of charge storage of capacitance. Under the situation indicates right in Fig. 5.5, if Vout biased at a voltage first, ΔV of Cout equals to this voltage because the tissue is grounded. For instance, R_S=2kΩ (tissue impedance), +VCC=6V, –VCC=–6V, +2VCC=12V, and a 6V bias voltage is delivered from node V_{bias}. In this case, the left-hand side structure in Fig. 5.5 is able to deliver a maximum stimulus current of ±3mA as explained in previous paragraph. As for the right-hand side, the ΔV of Cout is 6V. Therefore, if +2VCC is delivered, Vout equals to 12V, at the same time, V_T will rise to 6V since the ΔV on Cout. On the contrary, if 0V is delivered to Vout, V_T will be pulled to –6V. Consequently, ±3mA stimulus current can be generated at V_T without negative power supply, which may easier the design on monopolar stimulus driver.

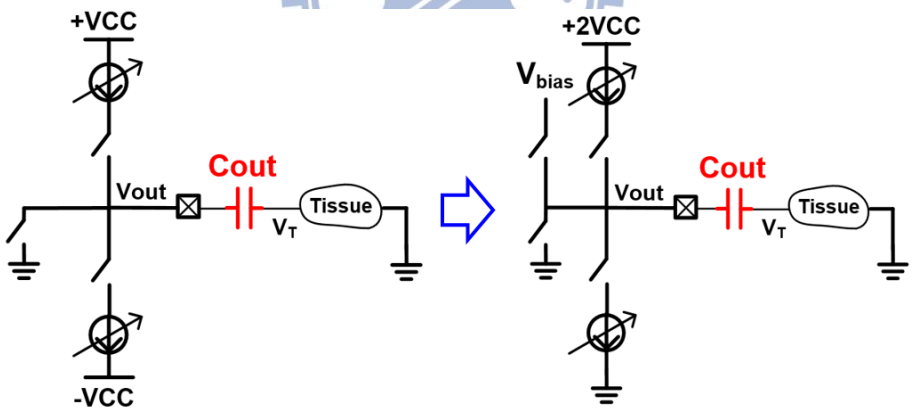
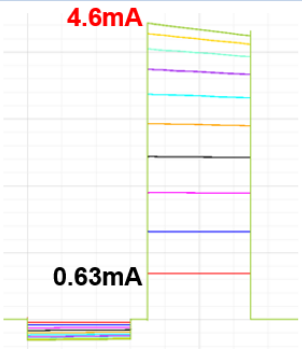
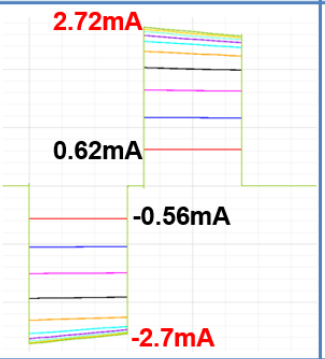
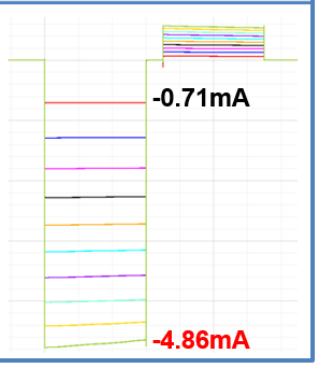


Fig. 5.5 Stimulus driver of monopolar configuration with output capacitor Cout but without negative voltage.

An advanced test of different bias voltages on Vout are in Table 5.1. It can be told from Table 5.1, if Vout biased at half of +2VCC (i.e. +VCC=6V), the stimulus current remain symmetrical biphasic output due to 6V voltage headroom to +2VCC and GND. The left column shows the result when Vout biased at 0V which means that

there is no charge be stored on Cout, so only positive stimulus current can be delivered to V_T since the voltage headroom to +2VCC is 12V but 0V to GND. And the right column shows completely opposite result when Vout biased at +2VCC (12V).

Table 5.1 Initial bias voltage of Vout vs. stimulus output current on V_T

Vout biased at 0V (GND)	Vout biased at 6V (VCC)	Vout biased at 12V (2VCC)
		

Overall, stimulator with output capacitor has its pros and cons. The advantage of DC blocking capacitor can enhance the safety level on bio-applications, but pre-charge (the structure needs initial biased on Vout) time, discharge time and the power consumption of a micro-scale level capacitor have to be taken into account.

5.2.3 Design of Dual-Configuration and Dual-Mode Stimulator

The proposed circuit structure combines monopolar and bipolar configuration, and either current or voltage stimulation can be chosen. And of course, no matter what configuration and stimulus mode is decided, all the stimulations are able to be monophasic or biphasic pulse. That means, it supports 8 stimulation patterns.

A brief driver circuit of one channel is shown in Fig. 5.6. Compare to the monopolar voltage stimulator in chapter 2, three more switches (Csw and Gsw) are added. In previous work, discharge function achieved by pass 0V to Vout, but now Gsw serves as a switch connects to ground. Since the upper terminal of Gsw (node Vout) can be positive or negative voltage during stimulation, it has to be realized by HV PMOS with dynamic bulk bias to prevent junction forward-leakage when P-substrate is 0V.

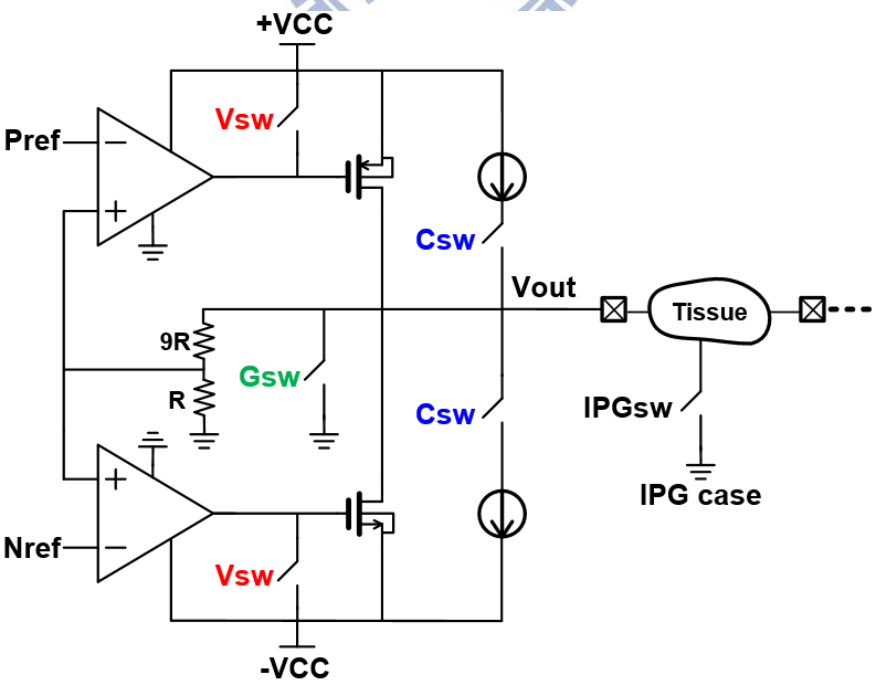


Fig. 5.6 Driver circuit of one channel dual-configuration and dual-mode stimulator.

For using as monopolar configuration, only one channel will be chosen, as the diagram in Fig. 5.6. Those Vsw are for voltage output while Csw are for current output, and the stimulus pulse will be deliver through tissue to IPG case (GND). That is to say, IPGsw is for monopolar stimulation. The upper part of the driver is for anodic stimulation, and the lower part is for cathodic stimulation.

If the driver is chosen as bipolar configuration, a pair of drivers will be operated at the same time. However, only the upper part of the driver is functional as illustrated in Fig. 5.7, since bipolar completes biphasic stimulation with bi-directional voltage or current from two chosen drivers. As a result, Gsw here replace the IPGsw for connecting to ground during stimulation and also serve as discharge switches.

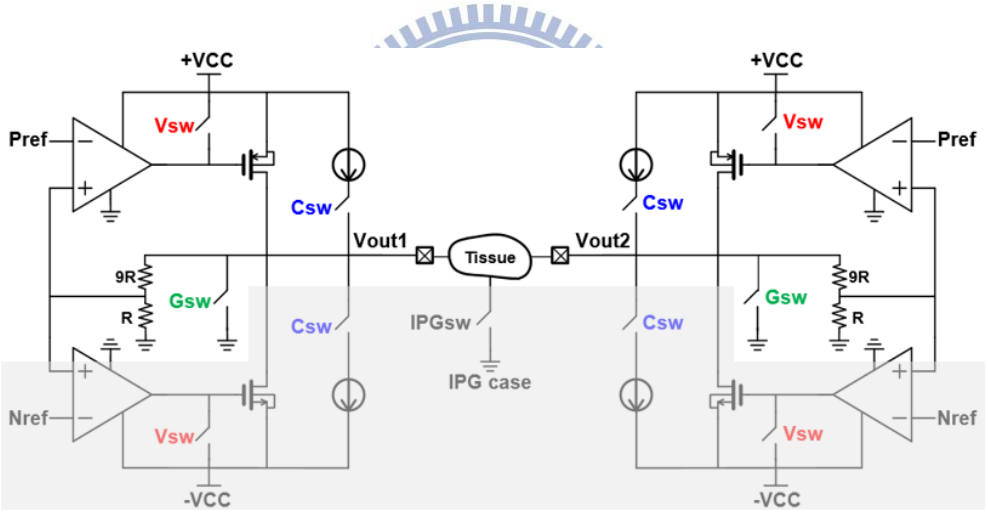


Fig. 5.7 Driver circuit using as bipolar configuration.

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