# 國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

**應用於2.4GHz T/R開關前端電路之**

**靜電放電防護設計**

**ESD Protection Designs for 2.4GHz T/R Switch**

**Front-End Circuits**

研 究 生：劉睿閎　　(Rui-Hong Liu)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國一〇四年十月

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碩士論文

A Thesis
Submitted to Department of Electronics Engineering and Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master of Science
in
Electronics Engineering
October 2015
HsinChu, Taiwan, Republic of China

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## 摘要

隨著 CMOS 技術的進步與發展，射頻積體電路 (radio-frequency integrated circuits, RF ICs) 也逐漸廣泛實現在 CMOS 製程中。因此不但可以有效提高晶片的整合度並且降低成本。在 CMOS 製程中，靜電放電 (electrostatic discharge, ESD) 對於積體電路一直是一項相當重要的可靠度問題，而靜電放電防護設計也非常重要。然而對於射頻積體電路，靜電放電防護設計會帶來不需要的寄生效應，因此能應用在射頻積體電路之靜電放電防護設計除了要有好的靜電放電耐受度之外，還必須要能將其寄生效應的影響降至最低。

本論文提出兩種針對 T/R 開關前端電路 (T/R switch font-end circuit) 的靜電放電防

護設計，第一種靜電放電防護設計可以減少寄生效應的影響，並承受一定的靜電放電轟擊，第二種靜電放電防護設計可以不外加任何靜電放電防護元件，便可以承受一定的靜電放電轟擊。兩者皆可以運用於 2.4GHz 的 T/R 開關前端電路。

本論文也提出一種針對傳統 T/R 開關前端電路的靜電放電防護設計，除了可以減少外加的靜電防護元件，還將矽控整流器 (silicon-controlled rectifier, SCR) 嵌入 T/R 開關中，並由電源端到地端間靜電放電箝制電路 (power-rail ESD clamp circuit) 的偵測電路提供觸發訊號。因此，此架構可以藉由矽控整流器及寄生二極體作為靜電放電路徑，並且運用於 2.4GHz 傳統 T/R 開關前端電路。

# ESD Protection Designs for 2.4GHz T/R Switch Front-End Circuits

**Student: Rui-Hong Liu** **Advisor: Prof. Ming-Dou Ker**

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## Abstract

As the CMOS technology develops so fast, radio-frequency integrated circuits (RF ICs) has been widely implemented in CMOS process. It has the advantage of a high integration and a low cost. Electrostatic discharge (ESD) has been one of the most serious reliability issues of CMOS processes, so ESD protection design is very important. However, undesirable parasitic effect is induced by the ESD protection design in RFICs. Consequently a successful RF ESD protection design needs well ESD protection ability and small parasitic effect.

In this thesis, two RF ESD protection designs for T/R switch front-end circuit are proposed. The first one can reduce the parasitic effect and sustain ESD stress. The second one can sustain ESD stress without extra ESD protection device. Both ESD protection designs are applied to 2.4GHz T/R switch front-end circuit.

An RF ESD protection design for traditional T/R switch front-end circuit is also proposed

in this thesis. The number of the ESD protection devices is reduced in this design. Besides, silicon-controlled rectifier (SCR) is embedded in T/R switch, and the detection circuit, which is used in power-rail ESD clamp circuit, can sent trigger signals to trigger the SCR. The embedded SCR and parasitic diode can provide ESD discharge paths. Moreover, this ESD protection designs are applied to 2.4GHz traditional T/R switch front-end circuit.

# Acknowledgment

首先要先感謝我的指導教授柯明道老師以及林群祐老師，在碩士班求學過程中給予研究上的指導與鼓勵。柯明道老師在靜電放電防護領域方面有深厚的專業知識與實務上的經驗，讓我在兩年之中學到了許多東西，而在專業領域之外，老師認真的研究態度與方法，特別是追求研究的完整性與嚴謹性也讓我獲益良多。

林群祐老師在對於運用於 RF ESD 設計方面擁有專業的知識，在此領域也有相當卓越的成就。非常感謝林群祐老師在繁忙的事物中撥空和我討論研究上的問題，也幫忙我解決不少問題。特別在模擬設計和實作量測等等各方面都給予我極大的幫助與實質上的建議。

感謝實驗室的學長們，戴嘉岑學長、羅志聰學長和陳界廷學長，在研究生活各方面的不吝幫忙。不論是在學術研究、儀器量測使用或是其他大大小小的問題都能幫我解決。

感謝跟我同屆的黃義傑、廖顯峰、楊子毅和鄭莞學四位研究夥伴，一起修課，做研究，互相討論問題，分享電路設計與量測的經驗，在閒暇之餘一起到體育館運動。這些種種都讓我的研究所生活變得更充實。也感謝學弟妹的陪伴，讓實驗室變得更歡樂。

最後當然要感謝在背後支持我的家人，能在艱苦的時刻，依然無條件對我付出，讓我可以順利完成學業。感謝這一路上陪伴我的所有人，願大家都能平安健康，謝謝。

劉睿閎

104 年 10 月於交大

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# Chapter 1
# Introduction

## 1.1 Motivation

In the recent decades, wireless technologies is growing rapidly and explosively. The RF products such as smart phones have become necessary. Because of the advantage of high integration and low cost for mass production, radio frequency integrated circuits (RFICs) have been widely designed and fabricated in CMOS processes [1].

Electrostatic discharge (ESD) is one of the most important reliability issue in IC products. As the feature size in CMOS technology shrinks rapidly, ESD issue becomes more serious and must be taken into consideration. ESD-induced failure results in unbearable energy bursts, either huge transient current or large voltage surge, which can easily damage any integrated RF devices, circuits, and systems [2]. Therefore, good ESD protection design is required for RFICs in real-world application.

ESD protection devices are usually applied to the input/output (I/O) interfaces of ICs. For RF receiver, the low-noise amplifier (LNA) is the first stage. For RF transmitter, the power amplifier (PA) is the last stage. They are often exposed to the risk of electronic charge directly. Once the RF front-end circuit is damaged by ESD, it cannot be recovered, and the RF functionality is lost. Thus, ESD protection design for CMOS LNA and PA are necessary. Unfortunately, such design would degrade the RF performance of core circuits because of the parasitic effects of the ESD protection [3].

To prevent core circuits form ESD stress, conventional ESD protection design, which

consists of a power-rail ESD clamp circuit and a pair of ESD protection devices between I/O pads and VDD or VSS can provide whole-chip ESD protection [4].

The larger dimensions of ESD protection devices, the better ESD protection robustness, but their large parasitic capacitance causes signal loss from pad to ground. Moreover, the parasitic capacitance also changes the input matching condition. It is a great challenge to design effective ESD protection circuits, which simultaneously have excellent ESD protection robustness and do not degrade RF performance.

The parasitic capacitances caused by the ESD protection devices are main obstacle to RF ESD protection design. There is a trade-off between the ESD protection robustness and RF performance. To minimize the negative impact caused by the parasitic capacitances, some methods have been proposed. The inductors and capacitors are chosen to tune out the parasitic capacitances of ESD protection devices [5]-[7]. The better solution is using ESD-RF co-design techniques, which take ESD protection designs into RFICs [8]. So, well design ESD protection circuit can not only have good ESD protection robustness stress but also reduce the degradation of RF performance.

Recent publications show a trend of integrating the low noise amplifier (LNA) and power amplifier (PA) on the same chip [9]. To increase the level of integration and reduce cost, transmit/receive (T/R) switches must be added into RFICs. However, the high frequency of RFICs makes the parasitic capacitance of ESD protection devices be more strictly limitation. Moreover, the first stage for RF receiver is the T/R switch instead of the LNA, and the last stage for RF transmitter is also the T/R switch instead of the PA. The T/R switch in the RF front-end circuit may be stressed by ESD. Therefore, the co-design of ESD protection and T/R switch is a good method.

Utilize the ESD/matching network co-design approach to optimize the ESD protection robustness and RF characteristic. Two new ESD protection solutions are proposed and fabricated in 2.4GHz T/R switch front-end circuits. One is using stacked diodes, which consist

of the embedded diode of switching transistor and ESD protection diode. The other is also using stacked diodes, which consist of diodes embedded T/R switch, and this structure does not need any extra ESD protection devices. All the ESD-protected T/R switch front-end circuits with ESD protection strategy consists of power-rail ESD clamp circuits have been designed and realized in 180-nm 1P6M CMOS process. The measurement results prove that the ESD protection designs can protect core circuit from ESD stress and provide desired ESD robustness.

Another ESD protection design for a traditional T/R switch structure is proposed in this work. In the 2.4GHz traditional T/R switch structure, both the series and shunt transistors are NMOS transistors. For the proposed ESD protection circuit, the traditional T/R switch with embedded silicon controlled rectifiers (SCRs) is used. The embedded SCRs with RC-inverter-triggered have great ESD robustness and low parasitic capacitances within a small layout area. Furthermore, this ESD protection structure just only needs an extra ESD protection diode. This structure considerably reduces the inherent parasitic effect. The simulation results prove that this ESD protection design can mitigate the degradation of RF performance and expectantly improve the ESD robustness.

## 1.2 Thesis Organization

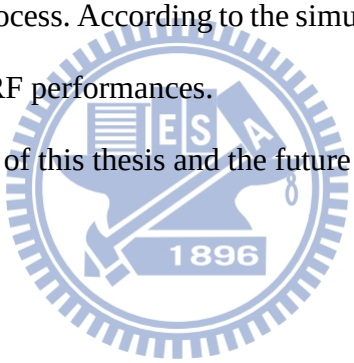
Chapter 2 introduces the basic principles and the considerations of RF ESD protection design. This chapter also provides a brief description of the basics of RF LNA, RF PA, and RF T/R switch. The issues of RF ESD protection designs are investigated. Some practical RF ESD protection designs are presented.

Chapter 3 exhibits ESD protection designs for 2.4GHz T/R switch front-end circuit. The proposed ESD protection designs with and without extra ESD protection devices are appropriate for the T/R switch front-end circuits, and the architectures of them are presented in

detail. Both un-protected T/R switch front-end circuit and ESD-protected T/R switch front-end circuits are fabricated in a 180-nm CMOS process. According to the measurement results, the proposed designs indeed have enough ESD protection ability without degrading the RF performances of the 2.4GHz T/R switch front-end circuits.

Chapter 4 exhibits ESD protection designs for 2.4GHz traditional T/R switch front-end circuit. The traditional T/R switch with embedded ESD protection silicon-controlled rectifier (SCR) is proposed to improve the ESD level in PS mode. The proposed ESD protection design without extra trigger circuit is appropriate for the traditional T/R switch front-end circuit. The architecture of them and simulation results are presented in detail. Both un-protected traditional T/R switch front-end circuit and ESD-protected traditional T/R switch front-end circuit are fabricated in a 180-nm CMOS process. According to the simulation results, the proposed design can mitigate degradation of the RF performances.

Chapter 5 is the conclusions of this thesis and the future works on this topic.



# Chapter 2

# Basics of RF and ESD Protection

## 2.1 General Considerations of LNA Design

### *2.1.1 S-Parameters*

To deal with a high-frequency network, conventional method of measuring voltage and current is no longer suitable. Direct measurement under high-frequency conditions usually involves the magnitude and phase of a traveling wave, so the concepts of equivalent voltage, equivalent current, and the related impedance and admittance become abstract. Scattering parameters (S-parameters) with the concepts of incident, reflected, and transmitted waves are more suitable and widely used to describe the characteristics and behaviors of high-frequency networks [10]-[11].

As illustrated in Fig. 2.1, a two-port network was characterized by S-parameters. These four quantities are related to one another through the S-parameters of the network:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.1}$$

which can also be represented as

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 \\ b_2 = S_{21}a_1 + S_{22}a_2 \end{cases} \tag{2.2}$$

where $a_1$ and $a_2$ represent the incident waves of each port; $b_1$ and $b_2$ represent the reflected waves of each port, respectively.

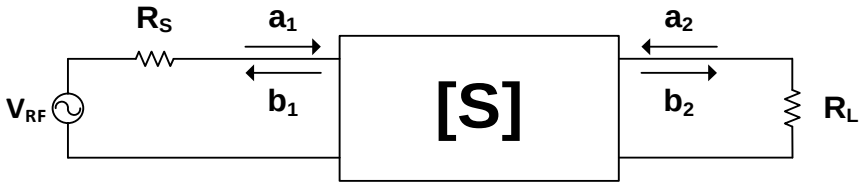



Fig. 2.1. A two-port network described with S-parameters.

Each tern in the Scattering matrix can be defined in

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \quad (2.3)$$

$S_{11}$ is the ratio of the reflected and incident waves at input port, and it is also called refection coefficient. $S_{12}$ is the ratio of the reflected wave at input port to incident wave at output port, and it is also called reverse gain. $S_{21}$ is the ratio of the incident wave at output port to reflected wave at input port, and it is also called forward gain. $S_{22}$ is the ratio of the reflected and incident waves at output port, and it is also called refection coefficient

In high-frequency measurement, $S_{11}$ represents the accuracy of the input matching, and $S_{22}$ represents the accuracy of the output matching. $S_{21}$ represents the forward gain of the circuit, and $S_{12}$ characterizes the reverse isolation of the circuit.

### *2.1.2 Stability*

Usually, the user of a cell phone wraps his/her hand around the antenna, so the antenna impendence may changes. Moreover, the input and output impendences are generally frequency dependent, and the stability condition is also frequency dependent. In a receiver, the low noise amplifier (LNA) must be stable for all source impendence at all frequency [11]. The sufficient

and necessary conditions for unconditionally stability are:

$$|\Gamma_L| < 1 \tag{2.4}$$

$$|\Gamma_S| < 1 \tag{2.5}$$

$$|\Gamma_{IN}| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}\right| < 1 \tag{2.6}$$

$$|\Gamma_{OUT}| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S}\right| < 1 \tag{2.7}$$

where $\Gamma_L$ is load reflection coefficient; $\Gamma_S$ is source reflection coefficient; $\Gamma_{IN}$ is input reflection coefficient; $\Gamma_{OUT}$ is output reflection coefficient.

These equation can be further deriver to

$$\mathrm{K} = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.8}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.9}$$

If K>1 and Δ>1, the circuit dose not oscillate at any frequency.

### *2.1.3 Noise Figure*

Generally, the performance of RF system is limited by noise, noise is an important concern for RF receivers. The signal-to-noise ratio (SNR) is defined as the signal power divided by the noise power. Noise factor (F) is a measure of SNR degradation due to the added noise from the system. It is helpful to know how the signal-to-noise ratio degrades as the signal passes through the described system. Noise factor is defined as

$$\mathrm{F} = \frac{SNR_i}{SNR_o} \tag{2.10}$$

where $SNR_i$ represents the signal-to-noise ratio measured at input, and $SNR_o$ represents the signal-to-noise ratio measured at output. A commonly used figure of merit named noise figure (NF) is

$$\mathrm{NF} = 10\log F\ (dB) \tag{2.11}$$

The physical meaning can be realized as

$$\mathrm{NF} = 1 + \frac{N_{add}}{N_i} = \frac{Total\ output\ noise\ power}{Output\ noise\ due\ to\ source\ only} \tag{2.12}$$

Form (2.12), if the described system adds no noise of its own, the output SNR is equal to the input SNR, i.e., NF would be zero. In reality, the finite internal noise of a system degrades the SNR, so the noise factor is always larger than one.

Consider a cascade multi-stage system shown in Fig. 2.2 that both the noise factor (F) and the gain (G) of a circuit contribute to the total system output noise power. The system noise factor can be characterized by Friis formula

$$\mathrm{F}_{sys} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \tag{2.13}$$

It is clear that noise of a multi-stage system is mainly contributed by the first stage. For this reason, LNA, which is the first stage of an RF receiver, needs much consideration on noise.

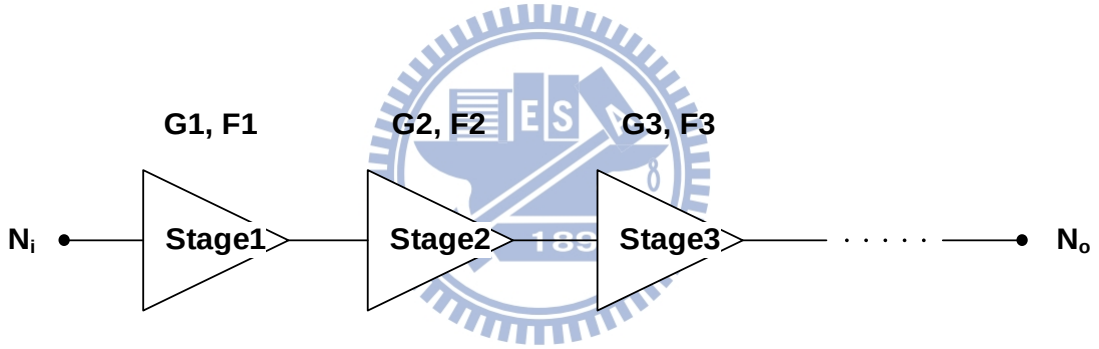



Fig. 2.2. A cascade multi-stage RF system described with gain and factor.

## 2.2 General Considerations of PA Design

### *2.2.1 Efficiency*

Power amplifier (PA) is used to simultaneously amplify and deliver RF power to a load, as shown Fig. 2.3. Since PA is the most power-hungry building block of RF transmitter, the efficiency of the PA is needed to be concerned. Some figures of merit can help evaluating the efficiency.

The drain efficiency is defined as

$$\eta_d = \frac{P_{OUT}}{P_{DC}} \tag{2.14}$$

The power added efficiency (PAE) is defined as

$$\eta_{PAE} = \frac{P_{OUT}-P_{IN}}{P_{DC}} = \eta_d(1 - \frac{P_{IN}}{P_{OUT}}) \tag{2.15}$$

The total efficiency is defined as

$$\eta_{total} = \frac{P_{OUT}}{P_{DC}+P_{IN}} \tag{2.16}$$

where $P_{IN}$ represents RF input power, $P_{OUT}$ represents RF output power, and $P_{DC}$ represents the average power drawn from the supply voltage. Consequently, PAE is smaller than drain efficiency at high frequency, and it is usually used indication of PA performance about efficiency.

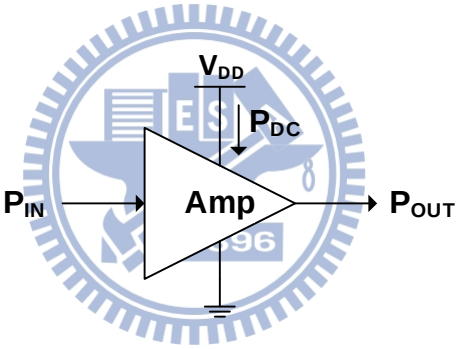



Fig. 2.3. A simple power amplifier described with power delivery and loss.

### *2.2.2 Large Signal Behavior and Gain Compression*

An ideal RF amplifier is considered as a linear amplifier, and it means that the relationship between output power and input power is linear. The small-signal gain of an RF circuit is not accurate enough because harmonics are negligible. As the signal amplitude increases, the gain begins to vary. That cause the RF circuit to be nonlinear. Therefore, large-signal behavior is important concern. For the large-signal, as input power increases larger and larger, the output power starts to gradually saturate. This makes the linear transfer relationship between input power and output power no longer be constant. Furthermore, under operating conditions, nonlinear effects refer to distortion of the signal waveform which is caused by the limitation

behavior of the MOS device. That is why the output power will be gradually compressed. To defended output power compressed, 1-dB gain compression point is commonly used to estimate the upper limitation of the linear operating region of PA.

As shown in Fig. 2.4, $IP_{1dB}$ is the input power at $P_{1dB}$. At 1-dB gain compression point ($P_{1dB}$), the power gain is 1 dB smaller than the constant power gain. As shown in Fig. 2.5, $OP_{1dB}$ represents the output power at $P_{1dB}$, and $P_{sat}$ represents saturated output power.

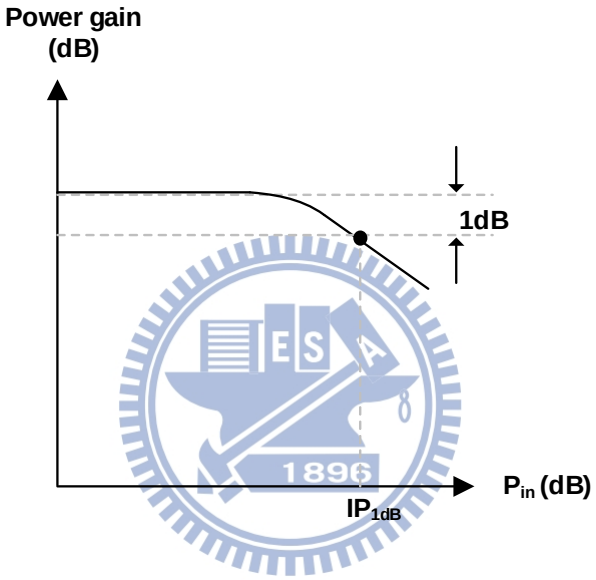



Fig. 2.4. The plot of power gain versus input power.

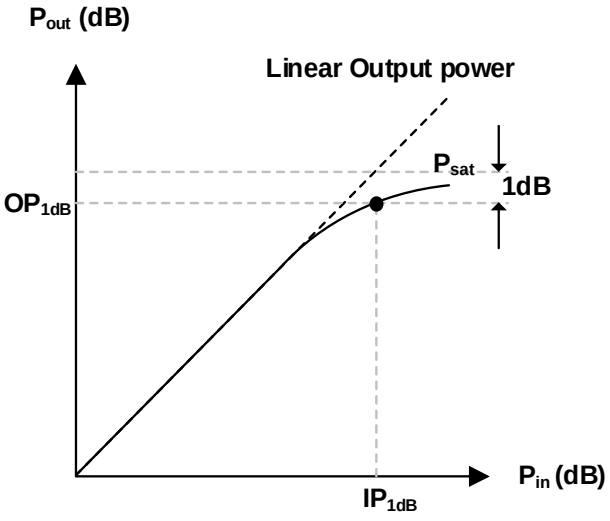



Fig. 2.5. The plot of output power versus input power.

### *2.2.3 Load-Line Theory and Load-Pull Characterization*

For linear RF amplifier such as LNA, the output matching network often is designed by using conjugate matching method. But, for the linear PA, the device has to be present with a power match on the output in order to extract the maximum power [12]. Therefore, for such physical restriction, another matching method named “load-line match” is chose to obtain maximum output power for a PA.

A simple generator, as shown in Fig. 2.6 and Fig. 2.7, delivers maximum power into external load. To better understand the difference between conjugate matching and load-line matching, for example, the current generator can supply a maximum output current of 1 A and an output resistance ($R_s$) of 100 Ω.

Applying the conjugate match method, the load resistance ($R_L$) should be chosen as 100 Ω. But the voltage across the terminals of the generator would be 50 V.

The large voltage may damage the output transistor of a PA, and the large voltage exceeds the maximum output voltage handling capability of the device, which assume the voltage is 10V. On the other hand, according to the load-line match method, the optimal load resistor ($R_{L,opt}$) is chosen as

$$R_{L,opt} = \frac{V_{max}}{I_{max}} = 10\Omega \tag{2.17}$$

where $R_s$ can be neglected because of that $R_s >> R_{L,opt}$. To maximize the RF voltage and current swing out of driving source, the load-line match is necessary for a PA to provide maximum output power, $P_{max}$.

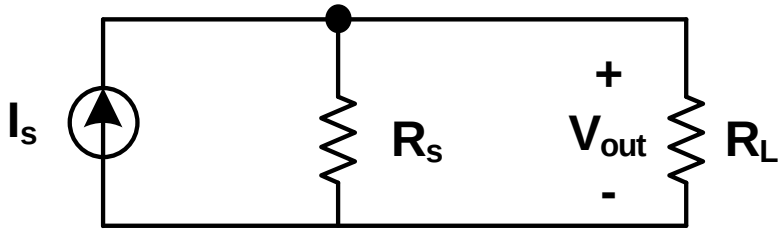



Fig. 2.6. A simple current generator

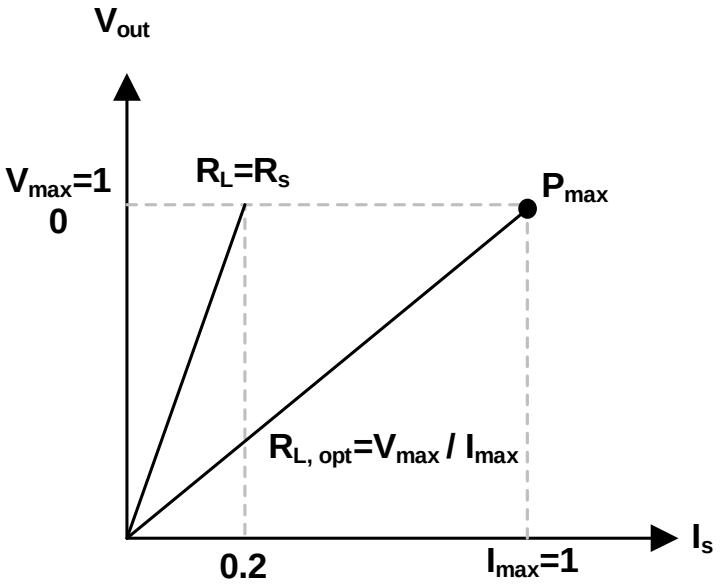



Fig. 2.7. The comparison of its two output matching methods.

Load-pull measurement is commonly method to obtain the optimal output impedance. The simple architecture of the load-pull measurement is shown in Fig. 2.8. In this architecture, the output tuner is lossless variable passive network which can present device under test (DUT) a complex load impedance, $Z_1$. And, the input tuner is adjusted to obtain conjugate matching for $Z_{in}$ and reduces the degradation of power gain caused by variation of $Z_1$. Adjust repeatedly $Z_1$ to get a constant output power which is lower than the maximum output power by 1 dB. A constant power contour would be presented on Smith Char. For PAE, this procedure needs to be done again, since the optimal output impedance for maximum output power is different from the optimal output impedance for maximum PAE. Two sets of contour are shown on Smith Chart, as shown in Fig. 2.9. The optimal output impedance for a well balance between output power and PAE can be chosen with the load-pull system.

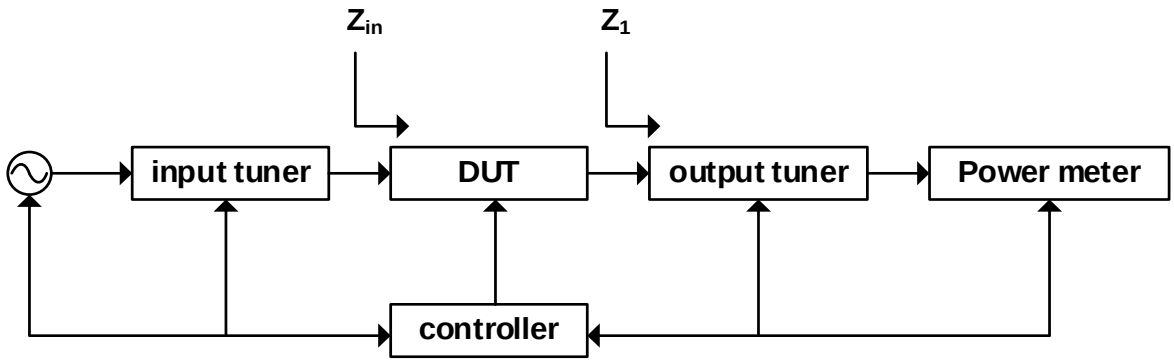



Fig. 2.8. Typical Load-pull system.

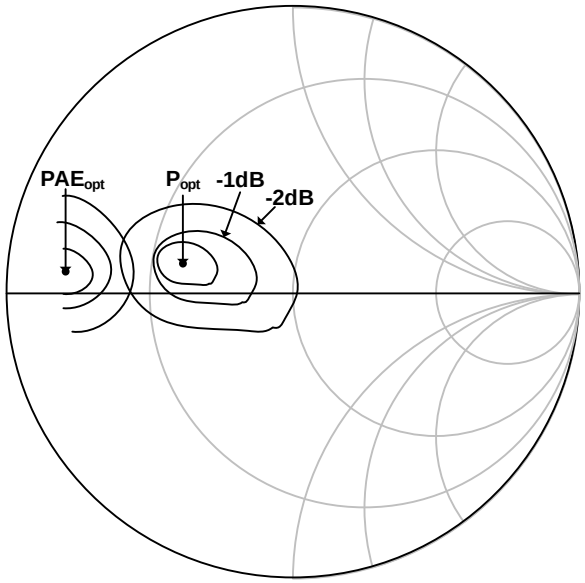



Fig. 2.9. Load-pull contour – delivered power contour.

### *2.2.4 Classes of Conventional Linear PA*

Power amplifiers have been categorized under many class: A, B, AB, C, D, and E.

In class A type, chose a suitable bias point to make transistors operate in active region at all time, and the transistors always have maximum current and voltage swing, but dissipate power. The theoretical maximum drain efficiency of class A is 50 %. So, class A PA provides good linearity but poor efficiency

In class B type, chose a suitable bias point to make transistors have zero quiescent current, and the amplifier conduction angle is 180°. The product of the drain voltage and current of class

B operation is not always positive, and the power dissipation would diminish. The theoretical maximum drain efficiency is 78 %. So, class B PA has worse linearity in exchange of better efficiency.

In class AB type, chose a suitable bias point to make quiescent current of the transistors between class A and class B, and the amplifier conduction angle is between 180° and 360°. The class AB power amplifier has better efficiency than class A power amplifier, and better linearity than class B power amplifier.

In class C type, chose a suitable bias point to make to make quiescent current of the transistors below the cut-off region, and the amplifier conduct angle less than 180°. As the conduction angle decreases to zero, the efficiency can achieve toward 100 %, but the gain and output power decrease to zero.

In class D type, chose a suitable bias point to make transistor be a switch, and the phase difference between output voltage curve and current curve is 180°.Because the switch voltage waveform is a square wave, it is clear that no power is being dissipation. The theoretical maximum drain efficiency is 100 %. But, slow switching at high frequency due to parasitic drain-source capacitance. It is not suitable for RF circuit.

In class E type, chose a suitable bias point to make transistor be a switch, which is shunted by a capacitor. When the switch is turn on, the drop voltage of shunt capacitor $V_c$ and $dV_c/dt$ are zero. So, the voltage curve and current curve are non-overlapping. The theoretical maximum drain efficiency is 100 %.

Each different types of PA has different optimal output impendence. Their load lines of PA on MOS I-V curves are shown in Fig. 2.10. $I_{max}$ represents the maximum output current of a transistor, $V_{max}$ represents the maximum voltage drop across the transistor drain and source, and $V_{knee}$ represents the knee voltage of the transistor.

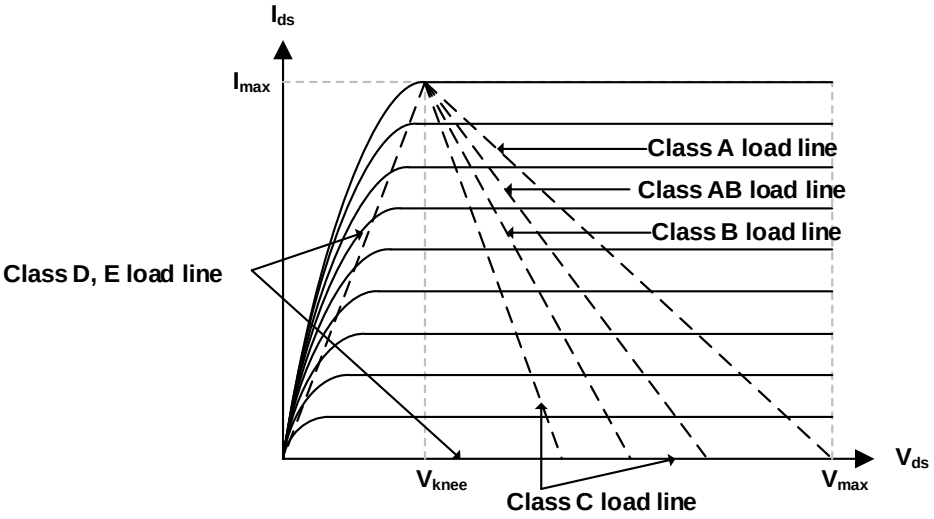



Fig. 2.10. Comparison among different bias points and there corresponding types of PA.

## 2.3 General Consideration of T/R Switch Design

### *2.3.1 Insertion Loss*

As shown in Fig. 2.11, RF transmit/receive switches (T/R switches) are one of the key blocks in radio and communication systems and they can be integrated with other RF circuits. ANT represents an antenna, RX represents a receive terminal, and TX represents a transmit terminal.

In order to design a better RF switch, the impact of substrate resistance, parasitic capacitance, and on-resistance, insertion loss has been analyzed. Insertion loss (IL) measures the small signal power loss though an RF switch when the switch is turned on. As shown Fig. 2.12, if both load and source are terminated with the characteristic impendence ($Z_0$) and the transistor operates in the linear region, IL can be defined as

$$\mathrm{IL} = \frac{Power\ Available\ form\ Source}{Power\ Delivered\ to\ Load} = \frac{P_{AVS}}{P_L} \tag{2.18}$$

IL can also be shown to be the reciprocal of the magnitude square of forward gain ($|S_{21}|^2$) [13].

$$\mathrm{IL} = \frac{1}{|S_{21}|^2} \tag{2.19}$$

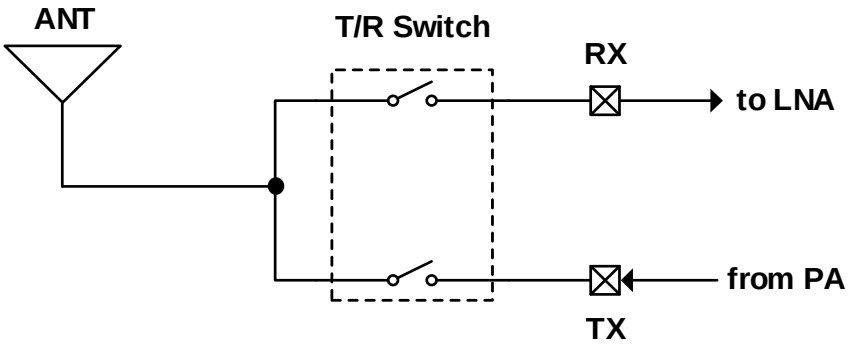



Fig. 2.11. Simple architecture of traditional T/R switch.

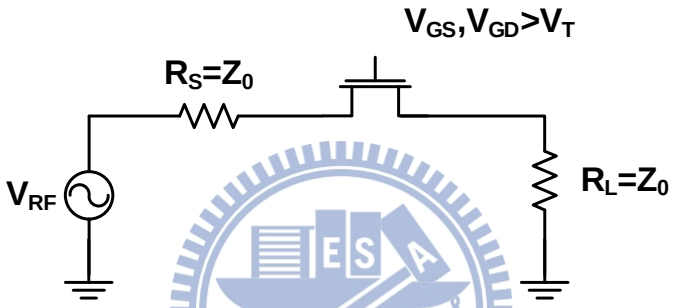



Fig. 2.12. MOS transistor switch in a 50Ω system.

To obtain lower IL, decreasing the on-resistance of the transistor is a good choice. However, large device has significant parasitic capacitances, causing considerable effect to circuit matching and eventually limiting the switch's bandwidth. Moreover, the parasitic capacitances would couple the RF signal to substrate resistance at high frequency. There is an inevitable trade-off between the on-resistance and the parasitic capacitances in choosing the optimal switch size for lower IL.

### *2.3.2 Power Handling and DC Bias*

A large RF signal swing can result in high drop voltages of $V_{GD}$ and $V_{GS}$ of the transistors. These drop voltages not only affect the on-resistance of the transistor but also may lead to excessive voltage across the gate dielectric and cause breakdown.

AC-floating technique is a good method to improve DC bias isolation by adding a large resistor. RF switch without gate resistor in off state is shown in Fig. 2.13 (a). The signal voltage, $V_{IN}$, would be compressed by the drop voltage between the drain and the gate, and the estimated maximum of $V_{IN}$ is

$$\left|V_{IN} - V_g\right| = |V_{IN}| < V_t \tag{2.20}$$

$$|V_{IN}|_{max} = \sim V_t \tag{2.21}$$

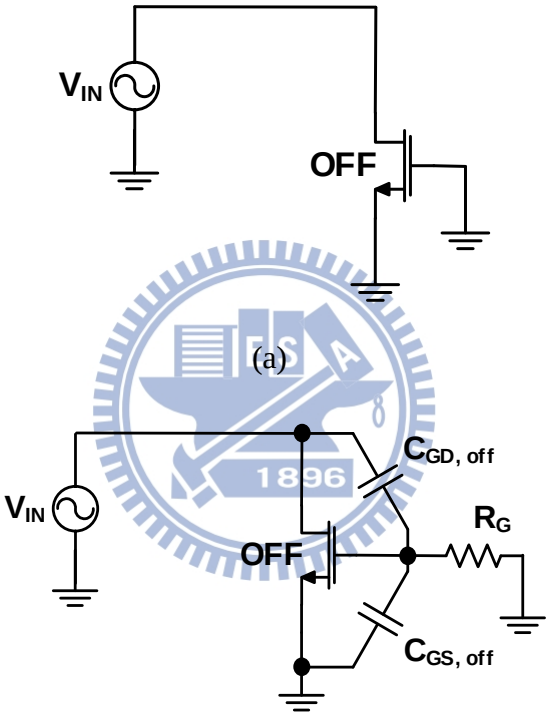



Fig. 2.13. MOS transistor switch (a) without gate resistance and (b) with gate resistance.

In the other case is RF switch with gate resistor, as shown in Fig. 2.13 (b). The gate resistor is large enough to let the gate ac-floating. Therefore, the signal voltage would be divided between the gate capacitance $C_{GD,\,off}$ and $C_{GS,\,off}$. The estimated maximum of $V_{IN}$ is

$$\left|V_{IN} - V_g\right| = \frac{|V_{IN}|}{2} < V_t \tag{2.22}$$

$$|V_{IN}|_{max} = \sim 2V_t \tag{2.23}$$

By using AC-floating method in RF switch cannot only prevent the RF signal from leaking into ac ground, but also enhance the voltage handling ability from $V_t$ to $2V_t$ [14].

The DC bias for TX node and RX node also can improve the power handling capability and decrease the insertion loss. This reverse biases the source/drain-to-body junctions which reduces the junction capacitance and RF signal coupled the substrate and thus decreases insertion loss. For power handling capability, if the DC voltage for TX node and RX node is zero, the RF input signal easily forward bias the source/drain-to-body junctions which would cause the RF signal clipped. However, if the DC voltage for TX node and RX node is positive voltage, the amplitude of the RF input signal could be increased before forward bias the source/drain-to-body junctions. So, biasing a positive voltage for T/R switch can improve the power handing capability.

## 2.4 Conventional ESD Protection Design

### *2.4.1 Architecture of Conventional Whole-Chip ESD Protection Design*

A whole-chip ESD protection design with $V_{DD}$-to-$V_{SS}$ ESD clamp circuit is proposed, and this design can prevent internal circuits form ESD stress efficiently [13]. The typical design, as shown in Fig. 2.14, consists of a pair of ESD protection devices and a power-rail ESD clamp circuit. Generally, the ESD protection devices are inserted among the I/O pad and power lines, and they provide ESD discharge paths when the I/O pad or power lines is zapped by ESD. The power-rail ESD clamp circuit is placed between power lines, and it can clamp the ESD voltage across $V_{DD}$ and VSS power lines and provide an ESD discharge path before internal circuits damage.

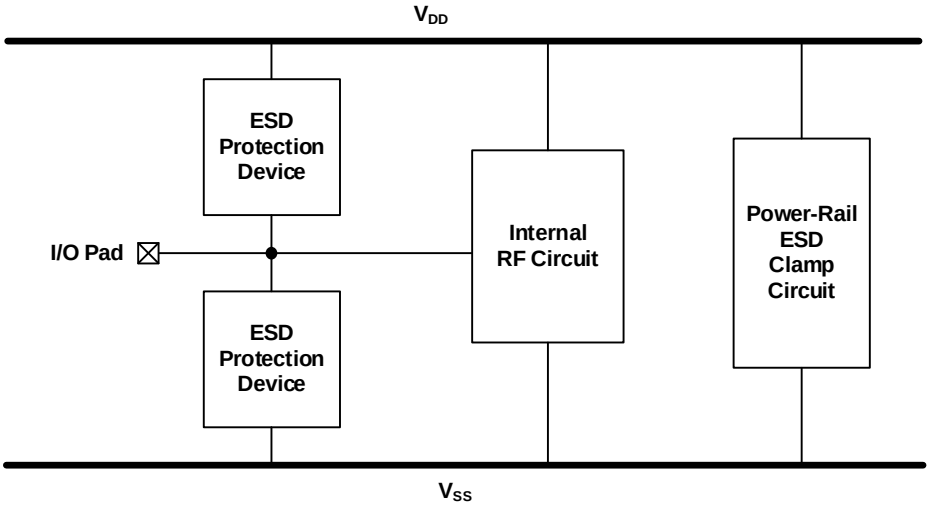



Fig. 2.14. Architecture of whole-chip ESD protection design.

### *2.4.2 Power-Rail ESD Clamp Circuit and I/O ESD Clamp Circuit*

The conventional whole-chip ESD protection design circuit is shown in Fig. 2.15. An RC-based $V_{DD}$-to-$V_{SS}$ power-rail ESD clamp circuit consists of an ESD-transient detection circuit and an ESD-clamping NMOS ($M_{ESD}$). The ESD-transient detection circuit is designed to detect the ESD events and send a control voltage to the gate terminal of the ESD-clamping NMOS. When the ESD-clamping NMOS is turned on, it would provide a low-impedance ESD discharge path from $V_{DD}$ to $V_{SS}$. Because ESD-transient detection circuit is RC-detector, the RC time constant must be concern. The pulse rise time of ESD events is on the order of nanosecond but that of the normal power-on events is on the order of millisecond. The RC time constant of the RC-detector should be designed about microsecond. Therefore, the ESD-clamping NMOS can be kept off to avoid power loss from $V_{DD}$ to $V_{SS}$ in the normal operating conditions and able to discharge the ESD current in the ESD stress conditions. To efficiently clamp the voltage across $V_{DD}$ and $V_{SS}$ power lines, the ESD-clamping NMOS is designed as large as possible to provide a low-impedance path between $V_{DD}$ and $V_{SS}$ power lines to quickly bypass ESD current.

I/O ESD clamp circuit, which consists of two ESD protection devices, provides ESD discharge paths to protect the internal circuit. Practically, a pair of diodes are inserted among

the I/O pad and power lines as the ESD protection devices. The diodes can be forward biased fast and clamp the voltage of I/O at low voltage efficiently because of low forward voltage. Moreover, the diodes can endure a large amount of current but only small layout area. Before internal circuit is damaged by ESD stress, the ESD current is conducted into the $V_{DD}$ power line or $V_{SS}$ power line through the forward biased diode.

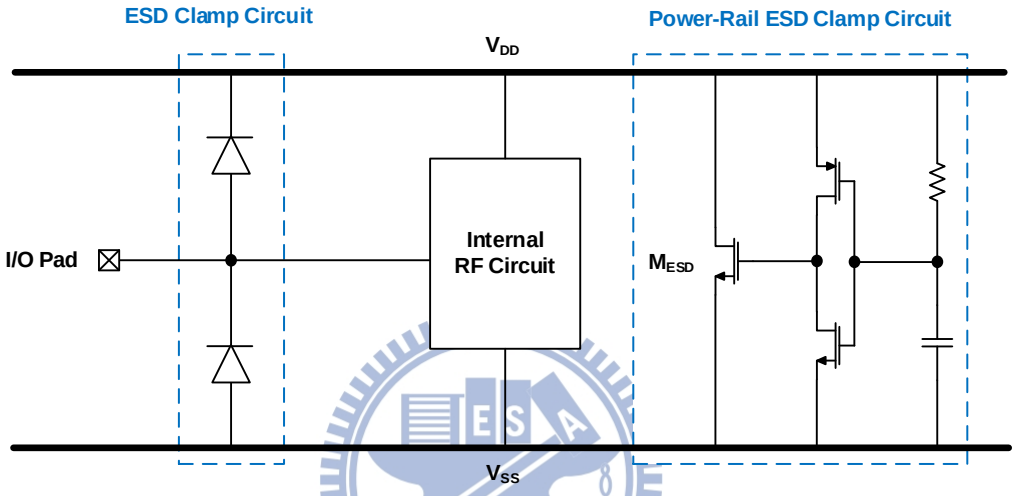
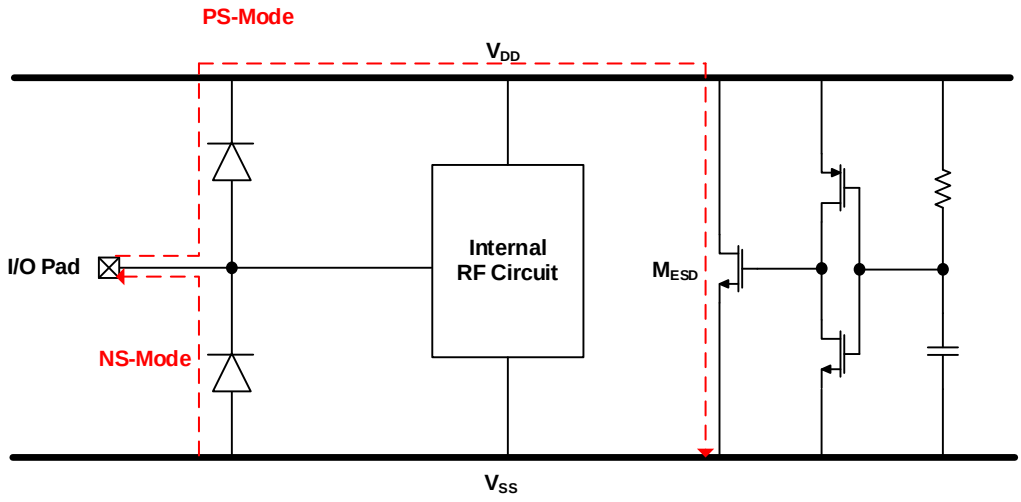
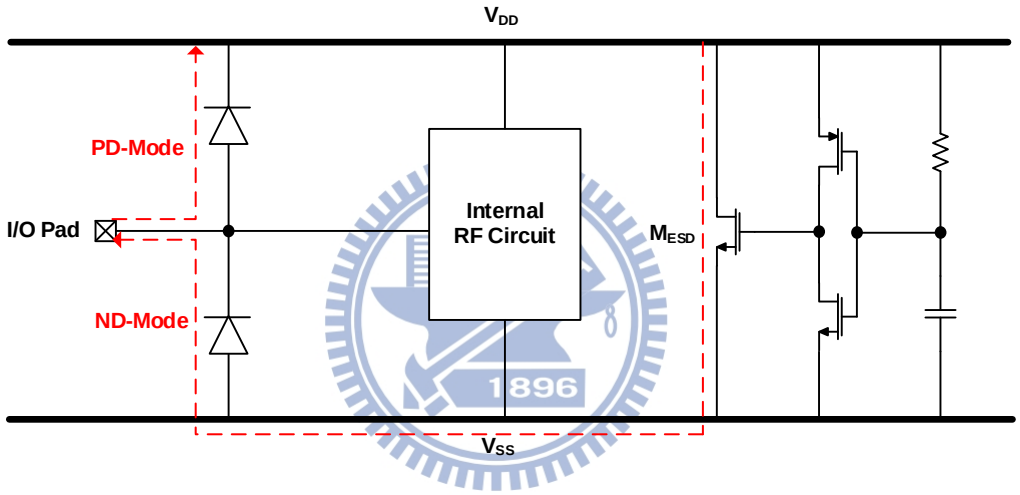



Fig. 2.15. Conventional whole-chip ESD protection design.

To robust ESD stress effectively, well whole-chip ESD protection circuit has to quickly bypass ESD current through the ESD discharge paths. The ESD discharge paths under every ESD zapping mode, which includes positive-to-$V_{DD}$ mode (PD-mode), negative-to-$V_{DD}$ mode (ND-mode), positive-to-$V_{SS}$ mode (PS-mode), negative-to-$V_{SS}$ mode (NS-mode), $V_{DD}$-to-$V_{SS}$ mode, and $V_{SS}$-to-$V_{DD}$ mode, are illustrated in Fig. 2.16.




(a)

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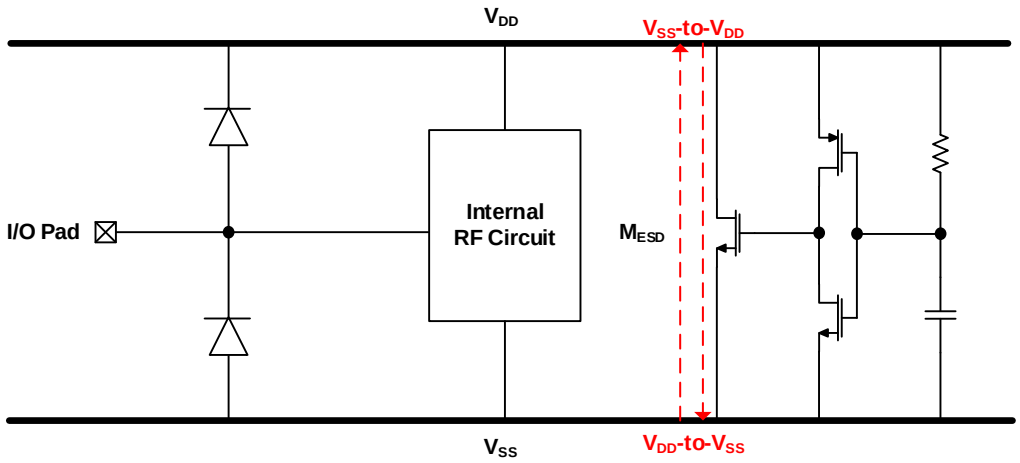



(c)

Fig. 2.16. ESD discharge paths under (a) PD-mode and ND-mode, (b) PS-mode and NS-mode, and (c) $V_{DD}$-to-$V_{SS}$ mode and $V_{SS}$-to-$V_{DD}$ mode.

## 2.5 Issues of RF ESD Protection Design

### *2.5.1 Impacts of ESD Protection Device on RF Performance*

Generally, the ESD protection devices with large dimension are able to sustain higher ESD level. However, they would induce undesired effects and cause RF performance degradation [15]. As shown Fig. 2.17, the parasitic capacitances of ESD protection devices ($C_{ESD}$) cause signal loss from the I/O pad to ac ground. Moreover, the input matching condition would be changed by the parasitic capacitances. Consequently, RF performance is degenerated.

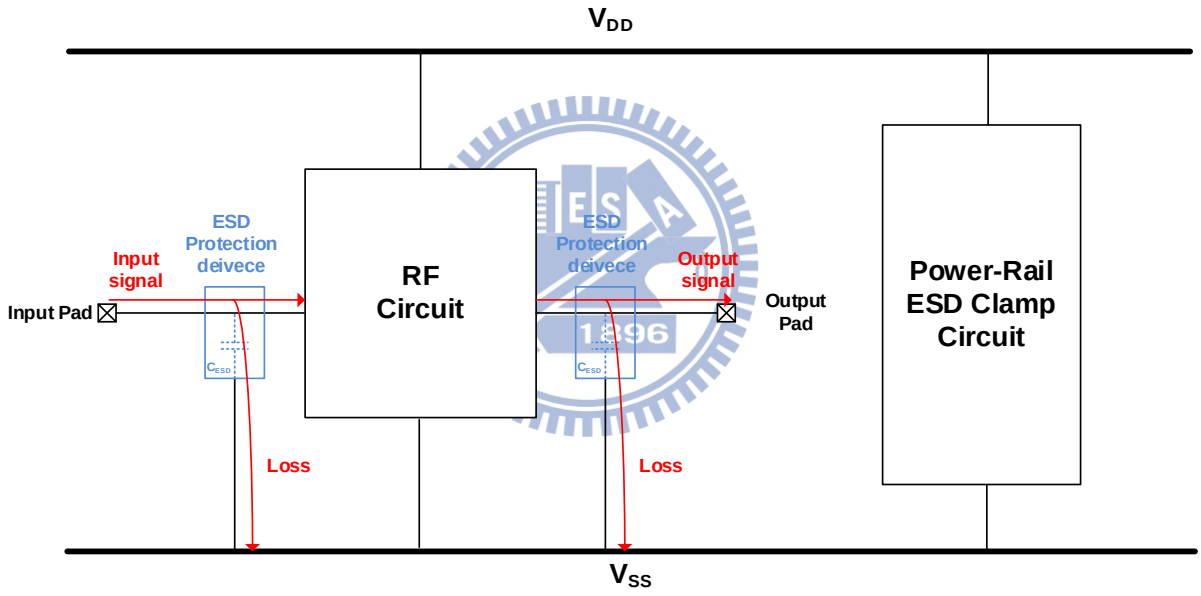



Fig. 2.17. Signal loss at input and output pads of IC with ESD protection circuit.

To mitigate this problem, reducing the dimension of ESD protection device can decrease the $C_{ESD}$ and increase the impedance of ESD protection device ($Z_{ESD}$), which can be expressed as

$$Z_{ESD} = \frac{1}{SC_{ESD}} \tag{2.24}$$

Unfortunately, the dimensions of ESD protection devices cannot be shrunk unlimitedly in

consideration of ESD robustness. Especially for higher frequency of operation, the $Z_{ESD}$ would further decrease and cause the RF performance degradation more critically.

Therefore, designing an effective ESD protection design for RFICs needs to not only think about ESD robustness but also minimize the RF performance degradation caused by ESD protection devices.

### *2.5.2 Conventional RF ESD Protection Design Method*

There are many basic methods, which are trying to cancel or isolate the parasitic capacitances of ESD protection devices and even reduce the parasitic capacitances, to design ESD protection devices and improve the impacts of ESD protection devices on RF performance [2] [16]. Some RF fundamental concepts of these methods for the ESD protection design are as follows:

ESD method of impedance isolation by using LC tank:

This method is using inductor and capacitor in parallel, as shown in Fig. 2.18 [7]. An LC resonator tank in series with an ESD protection device is placed among the I/O pad and power lines. The ESD diodes $D_P$ and $D_N$ are used to block the steady leakage current path from VDD to VSS under normal operation condition. The impedance of LC tank is ideally infinite from the signal path to the ESD diodes at resonant frequency of the LC tank. The resonant frequency is

$$\omega = \frac{1}{\sqrt{L_P C_P}} = \frac{1}{\sqrt{L_N C_N}} \tag{2.25}$$

Therefore, tune the inductors and the capacitances to resonate at application frequency. The loading effect of the ESD protection devices can be reduced and the parasitic capacitance of the ESD protection devices are isolated.

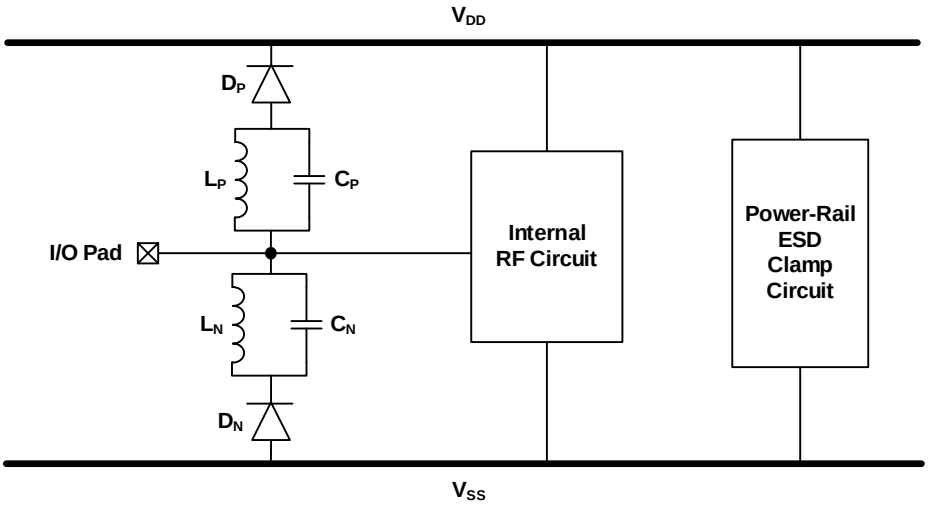



Fig. 2.18. ESD protection design with LC-tanks for RF circuits.

ESD method of impedance isolation by using series LC resonator:

This method is using inductors in series with an ESD diodes, as shown in Fig. 2.19 [6]. The ESD current can be discharge through the inductor and ESD diode when ESD events happen. In normal operating condition, the inductor can resonate with ESD diode at their LC resonant frequency because of the parasitic capacitance of the ESD diode. At the resonant frequency, impedance of the series inductor and diode is small, and the signal loss is very large. However, at frequencies above the resonant frequency, the inductor can sever as a high impedance element. The high impedance of the series LC resonator can reduce signal loss significantly. Therefore, tune the resonant frequency of the series inductor and diode far away from the application frequency of the RF circuit, and the loading effect of ESD protection devices can be mitigated.

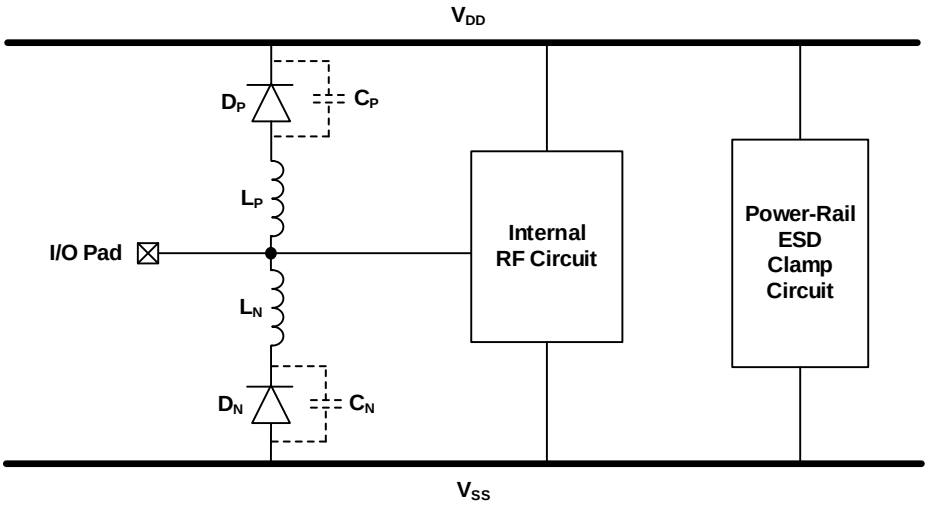



Fig. 2.19. ESD protection design with series diodes and inductors for RF circuits.

ESD method of cancellation:

This method is using RF component and make the ESD element become a part of matching network [17]. So, the loading effect of an ESD protection device can be hidden at the application frequency. As shown in Fig. 2.20, $C_{P,\ ESD}$ is the parasitic capacitance of an ESD protection device which changes the input matching condition. By adding extra capacitor $C_{EX}$ and inductor $L_{EX}$, the input impedance of the internal RF circuit can be changed from $Z_{i1}$ to $Z_{i2}$ of 50Ω. This method can minimize the impact of ESD protection device for the input matching condition and reduce the RF performance degradation caused by the parasitic capacitance of ESD protection devices. In conclusion, by co-designing the ESD protection circuit and the impedance matching network, the ESD protection device can be used to achieve a high ESD robustness without sacrificing the RF performance.

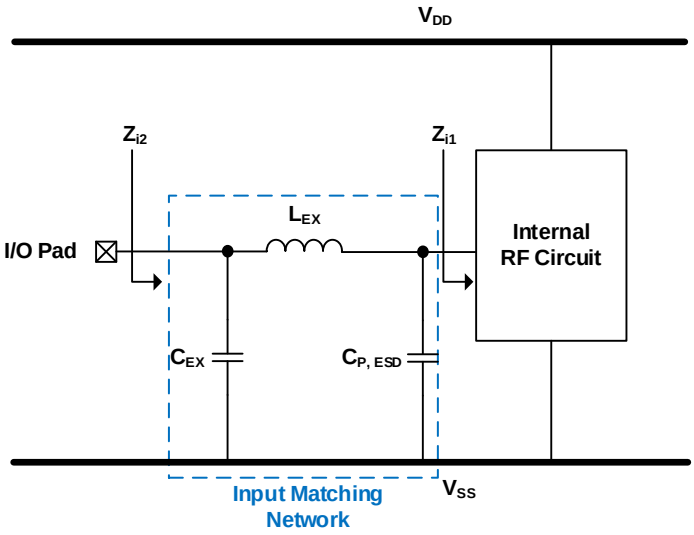



Fig. 2.20. Input matching co-design of RF circuits with ESD protection devices.

The cancellation method is suitable to achieve wideband impedance matching with ESD protection devices. To sustain the ESD robustness and realize wideband application simultaneously, the ESD protection devices are divided into small section and matched by Z components, which are the impedance of transmission lines, coplanar waveguides, or inductors [18]. This is a decreasing-size distributed ESD protection scheme, as shown in Fig. 2.21, which allocates the ESD protection devices with decreasing-size from the I/O pad to the internal circuit. Z1, Z2 and Z3 represent the impedance of Z components. For ESD robustness, it is proved that dividing the ESD protection devices into decreasing-size has better ESD level than dividing them into equal size, because most of ESD current is expected to flow through the first section which is closest to the I/O pad. With larger ESD protection devices close to the I/O pad, ESD robustness can be improved. This architecture successfully combines ESD protection devices with input matching network by using cancellation method for wideband application, moreover, it can provide enough ESD robustness and mitigate RF performance degradation.

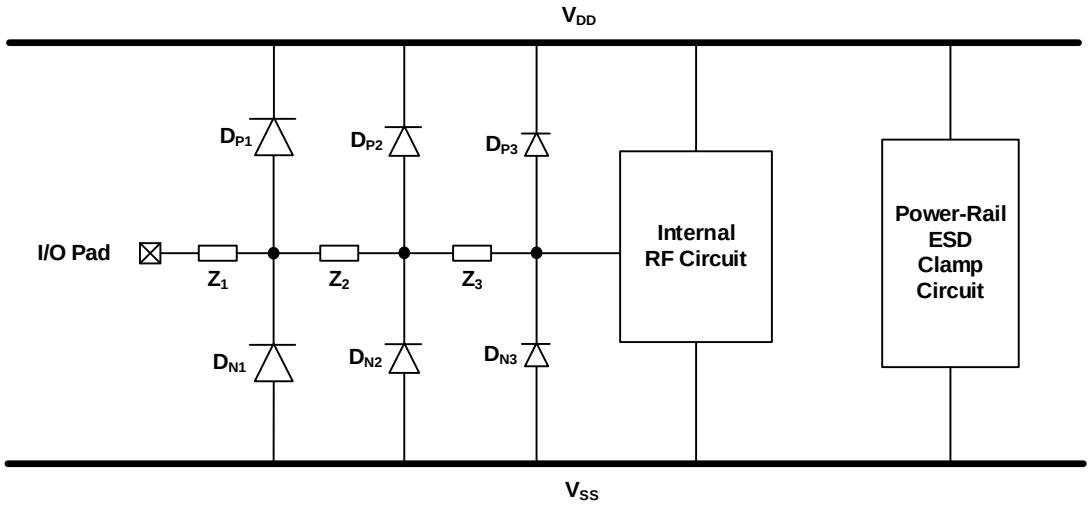



Fig. 2.21. ESD protection devices with decreasing size for broad-band RF circuits.

### *2.5.3 Conventional Structure of Silicon-Controlled Rectifier*

Conventional structure of silicon-controlled rectifier (SCR) device has lower holding voltage when ESD stress, and it can sustain a much higher ESD level with a smaller layout area. Furthermore, the parasitic capacitance induced by SCR device is small and reduces the RF performance degradation. So, the SCR device is suitable to be ESD protection device for RFIC [19].

The cross-section view of the SCR device is shown in Fig. 2.22 (a), and the equivalent circuit schematic of the SCR device is shown in Fig. 2.22 (b). Typically, the SCR device consists of a lateral NPN bipolar transistor ($Q_{NPN}$) and a vertical PNP bipolar transistor ($Q_{PNP}$) to form a four-layer PNPN (P+/N-well/P-well/N+) structure.

The DC I–V characteristics of SCR device under ESD stress is shown in Fig. 2.22 (c). $V_{t1}$ and $V_h$ represent a trigger voltage and a holding voltage of the SCR device. $V_F$ represents a cut-

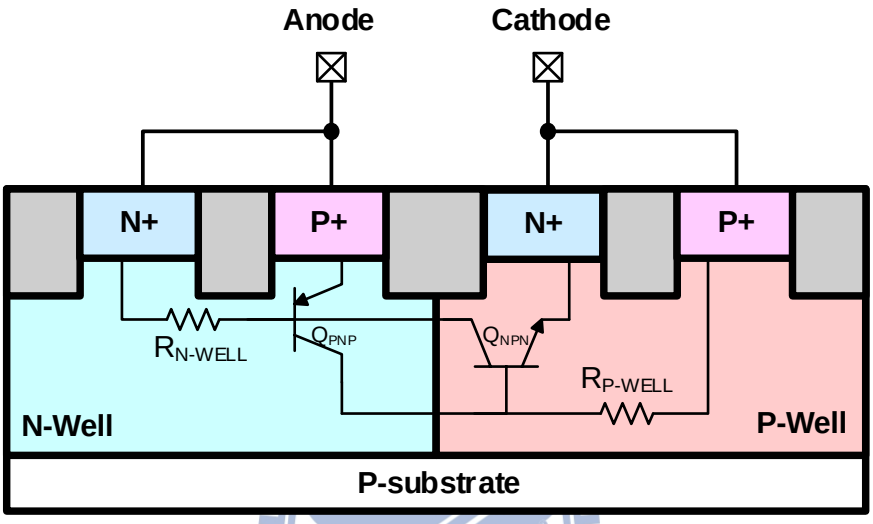
in voltage of the parasitic diode. $I_{t2}$ and $I_{t2'}$ are breakdown point which are the highest ESD discharge capability of the SCR device.

The positive ESD stress is applied to the anode of SCR device, and its cathode is relatively grounded. At the beginning, the voltage applied to the anode is not higher than the breakdown voltage of the N-well/P-well junction, so SCR device acts like an open circuit. However, when the voltage applied to the anode is greater than the breakdown voltage, the hole and electron current would be generated because of the avalanche breakdown mechanism. Hole current flows through the P-well to the P+ diffusion connected to ground; meanwhile, electron current flows through the N-well to the N+ diffusion connected to the anode. If the voltage drops across the P-well resistor ($R_{P\text{-well}}$) (N-well resistor ($R_{N\text{-well}}$)) is larger than 0.7 V, the parasitic NPN (PNP) bipolar transistor will be turned on. Furthermore, the parasitic NPN (PNP) bipolar transistor injects electron (hole) current to bias the PNP (NPN) bipolar transistor, and then the SCR device is successfully triggered into its latching state by the positive-feedback regenerative mechanism, and it has a low holding voltage ($V_h$) ~1.5 V, typically in the bulk CMOS process.

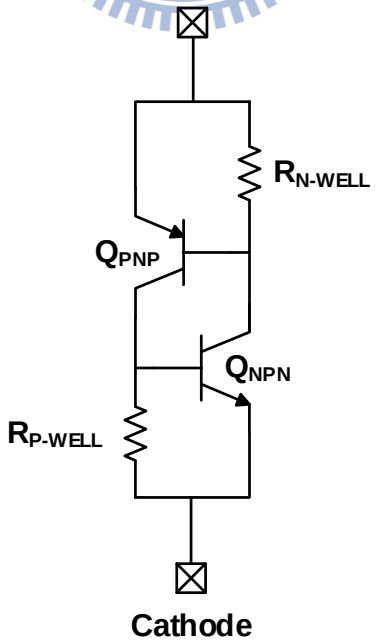
The negative ESD stress is applied to the anode of SCR device, and its cathode is relatively grounded. This negative voltage drops across the parasitic P-well/N-well junction diode in SCR device. As long as the parasitic diode is forward biased, ESD current can be discharged and the negative voltage will be clamped at the low cut-in voltage of the parasitic diode.

SCR provides suitable ESD discharging ability under every ESD events, as described

above. It can provide high ESD protection level within a small layout area in CMOS ICs. A smaller layout area introduces less parasitic capacitance, and therefore it reduces the impact of the RF performance degradation.




(a)

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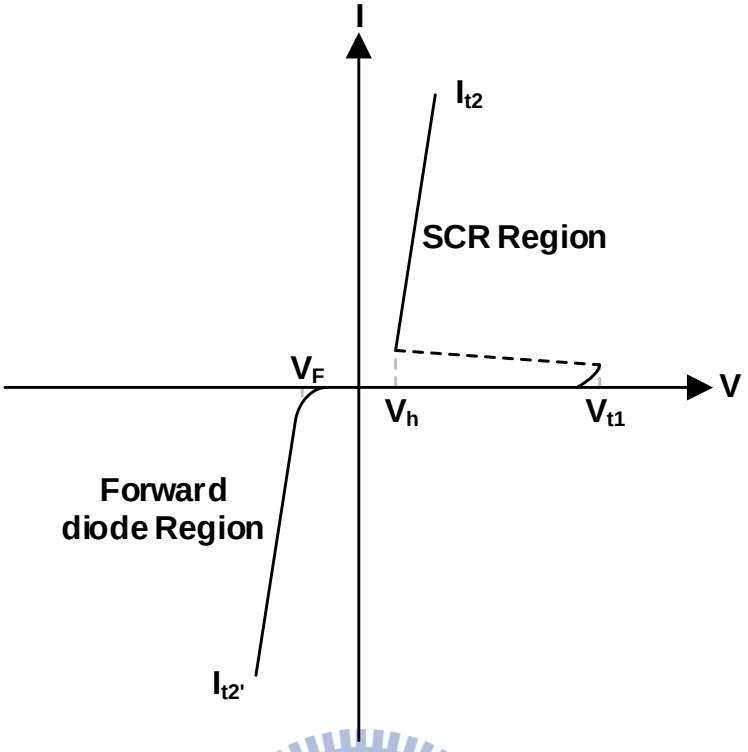



(c)

Fig. 2.22. The (a) cross-section view, (b) equivalent circuit of a typical SCR, and (c) I–V characteristics of SCR device under positive and negative voltage biases.

# Chapter 3

# ESD Protection Designs for 2.4GHz T/R Switch Front-End Circuits

## 3.1 Circuit Design of 2.4GHz CMOS T/R Switch Front-End Circuit

The transmit/receive (T/R) switch front-end circuit, which consists of a low noise amplifier (LNA), a power amplifier (PA), and a transmit/receive (T/R) switch, is designed to operate at 2.4GHz with $V_{DD}$ supply of 1.8V. The circuit schematics and circuit designs are shown below:

Circuit Design of LNA:

The circuit schematic of the LNA is shown in Fig. 3.1. The DC bias $V_G$ is half of $V_{DD}$. The LNA is designed by a cascode configuration with inductive source degeneration. Using cascode structure can have the advantage of good isolation and mitigate the miller effect to provide good stability [20]. Furthermore, the LNA with inductive source degeneration is applied to match the input impedance and reduce the impact of extra noise. The required minimum amplifier gain is 10dB. In the gain stage, the both NMOS transistors size are determined with total width = 450μm and channel length = 0.18μm.

The second stage is used to match the output impedance with drain inductance. The both NMOS transistors size are determined with total width = 35μm and 25μm respectively. So, the LNA has the advantage of good isolation and better capability of simultaneous noise and input impedance matching at high frequency.

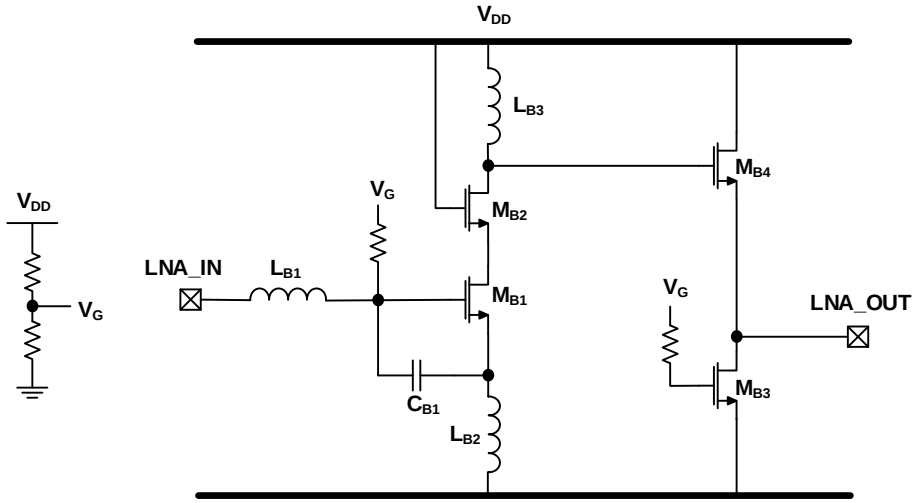



Fig. 3.1. Circuit schematic of low noise amplifier.

Circuit Design of PA:

The PA is chosen as class-E and the circuit schematic of the PA is shown in Fig. 3.2. The PA is designed by a cascode configuration in order to separate the output voltage and mitigate gate oxide stress effect [21]. The drain inductance $L_{a2}$ is RF choke. The L-C filter is tuned to the first harmonic of the input frequency, so that only sinusoidal wave can be transmit to the output load.

The required minimum output power is 5dBm because of switch loss and band pass filter loss. According to the DC I-V curve of the NMOS transistor, the NMOS transistor size is determined with total width = 450μm and channel length = 0.18μm. Chose a suitable bias point $V_B$ to make the transistor be switching transistor.

The input matching network is π-matching for conjugate match, and the output matching network is designed with load-pull simulation.

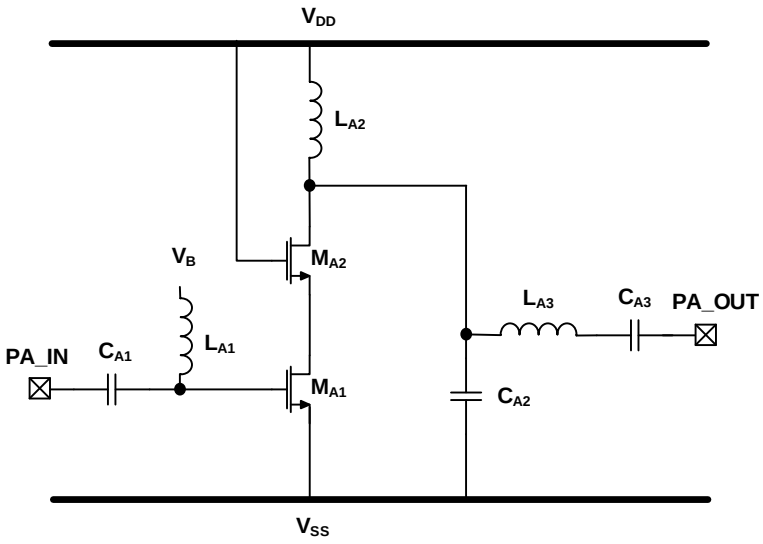



Fig. 3.2. Circuit schematic of power amplifier.

Circuit Design of T/R Switch:

The circuit schematic of the series-shunt T/R switch is shown in Fig. 3.3. In a T/R switch application, the main requirements are low insertion loss and high power handling capability. As presented in section 2.3, in order to increase power handling capability, the gate of switching transistor is biased using large resistor. The suitable DC bias for T/R switch also can get higher power handling capability. Choosing the switching transistor width is important. Generally, as the switching transistor width increases, the insertion loss decreases because the on-resistance of the switch decreases. However, if the switching transistor width increases excessively, the insertion loss increases because the signal loss through the capacitive coupling to the substrate becomes seriously [13]. To minimize the insertion loss, the switching PMOS and switching NMOS transistors size are determined with total width = 400μm and 200μm respectively, and channel length = 0.18μm.

The shunt transistors are used to improve the isolation of the switch. For the shunt transistors, both the PMOS and NMOS transistors size are determined with total width = 25μm.

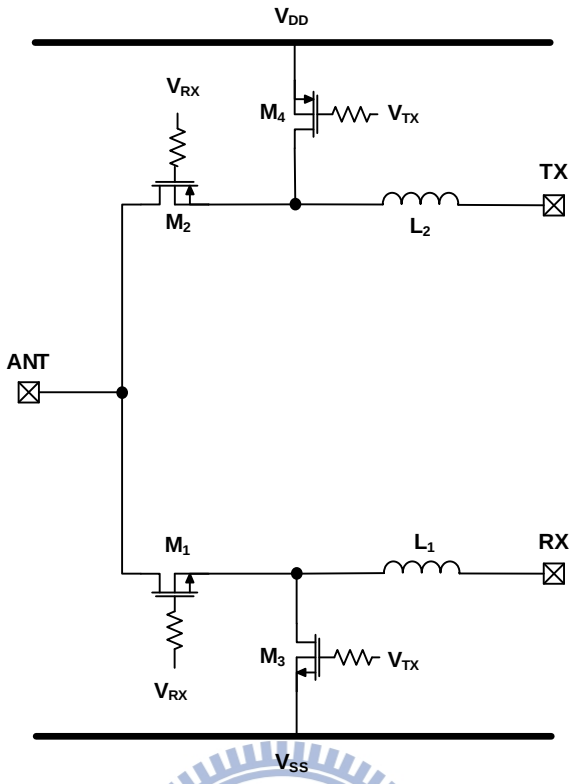



Fig. 3.3. Circuit schematic of series-shunt T/R switch.

Circuit Design of T/R Switch Front-end Circuit:

The T/R switch plays an important role in the RF transceiver front-end circuit because it can integrate with transmitter and receiver. The circuit schematic of the T/R switch front-end circuit is shown in Fig. 3.4. Carefully design impendence matching between switch and PA or LNA for high power delivery and high gain at operation frequency. In the transmit (TX) mode, the transmit path presents a low impedance and the output power of the PA is transmitted to the antenna (ANT). In the receive (RX) mode, the transmit path presents a high impedance, so the RF signal can be sent to the receiver and the transmitter is isolated from ANT. Consequently, this design integrates transmitter and receiver into single chip for purposes of low-power consumption and low-cost.

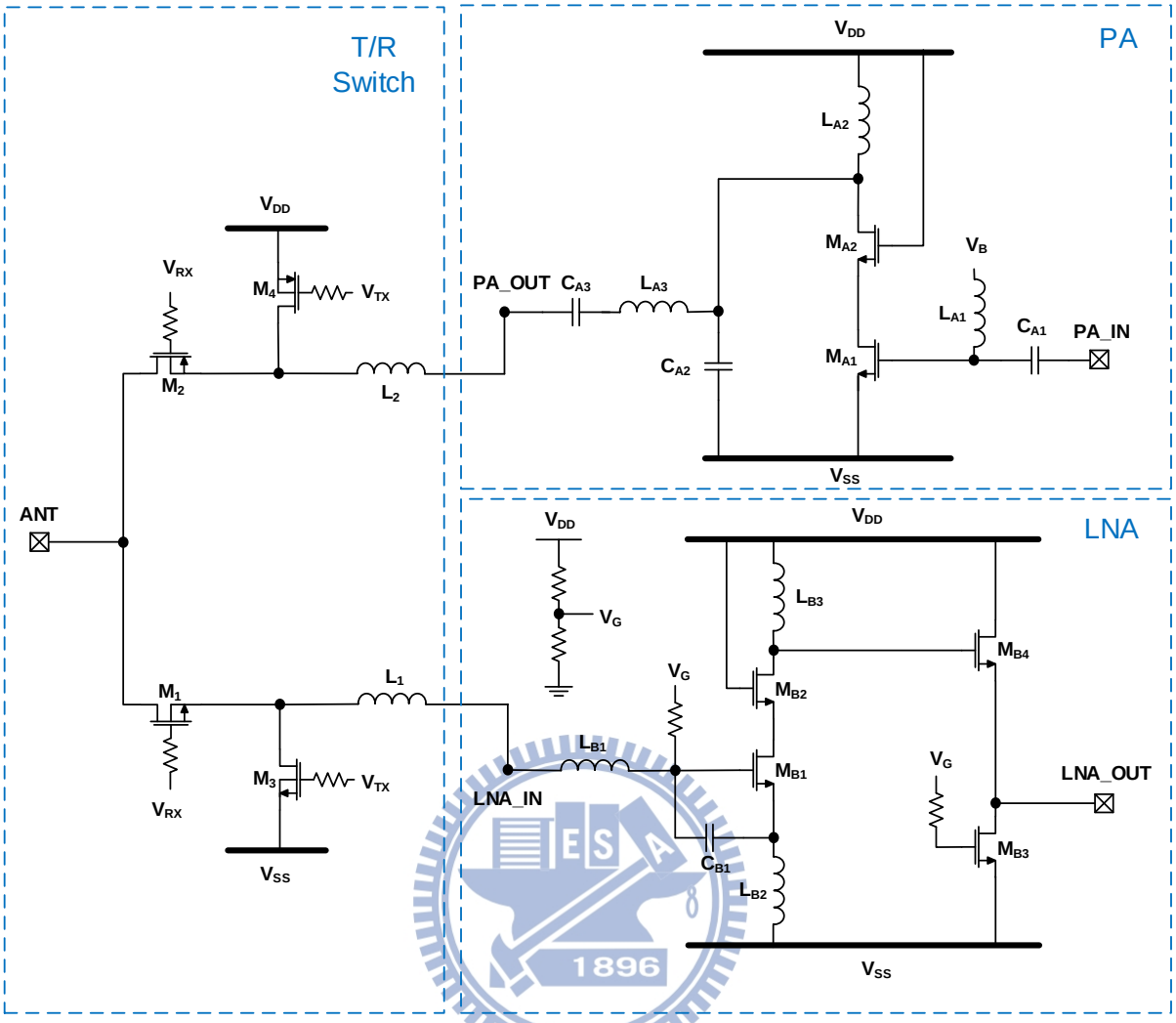



Fig. 3.4. Circuit schematic of T/R switch front-end circuit.

## 3.2 Conventional ESD Protection Design for T/R Switch Front-End Circuit

To prevent the T/R switch front-end circuit from ESD stress, it needs on-chip ESD protection circuit or device. Generally, the ESD protection device is put at I/O pad to protect the core circuit from ESD damage. For T/R switch front-end circuit, the ESD protection device is added to the antenna (ANT) pad, as show in Fig. 3.5. When the ESD events happen, the ESD protection device has to provide a low impedance path to discharge the ESD current. However, the parasitic capacitance of ESD protection device induces the RF signal loss and degrades the RF performance of T/R switch front-end circuit. Therefore, the parasitic capacitance must be

considered for gigahertz circuit design.

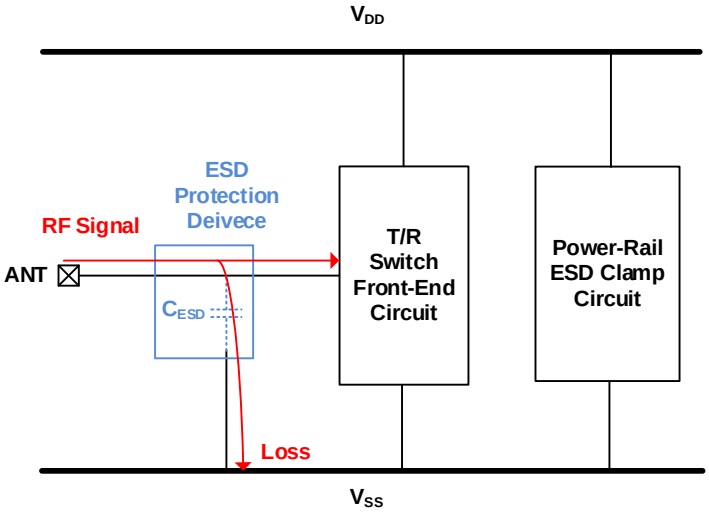



Fig. 3.5. Signal loss at ANT pad of T/R switch with ESD protection design.

The conventional ESD protection scheme for T/R switch front-end circuit is shown in Fig. 3.6, where two ESD protection devices ($D_{P1}$ and $D_{N1}$) are put at ANT pad, and a power-rail ESD clamp circuit is connected between the supply voltages. The ESD protection devices are P+/N-Well junction diode ($D_{P1}$) and P-well/N+ junction diode ($D_{N1}$).

The power-rail ESD clamp circuit, which consists of an RC-detector, a CMOS inverter, and an RC-inverter-triggered NMOS, is used to provide ESD current path between $V_{DD}$ and $V_{SS}$ under ESD stress conditions. To avoid mistrigger the power-rail ESD clamp circuit, the RC-detector is designed to distinguish ESD transients from normal operating conditions. As shown in Fig. 3.6, the R (~100kΩ) and C (~1pF) with time constant of 0.1μs ~ 1μs can meet such requirement, because the rise time of turn-on events are on the order of millisecond whereas that of ESD events are on the order of nanosecond. The NMOS ($M_{ESD}$) with ~3000μm width is used as an ESD clamp device. Since the power-rail ESD clamp circuit is placed between $V_{DD}$ and $V_{SS}$, the impact of parasitic effect of clamp circuit on ANT pad is minor.

The ESD discharge paths for the four different ESD testing modes are also shown in Fig. 3.6. For positive-to-$V_{DD}$ (PD) mode, the ESD current is discharged through the $D_{P1}$. For

positive-to-$V_{SS}$ (PS) mode, the ESD current first goes through the $D_{P1}$, and then it is discharged through the power-rail ESD clamp circuit. For Negative-to-$V_{DD}$ (ND) mode, the ESD current is first discharged from $V_{DD}$ to $V_{SS}$ through the power-rail ESD clamp circuit, and then it goes through the $D_{N1}$. For Negative-to-$V_{SS}$ (NS) mode, the ESD current is discharged through the $D_{N1}$.

However, the conventional ESD protection design with dual diodes causes parasitic capacitance and degrades the RF performance. It is not very suitable for T/R switch front-end circuit.

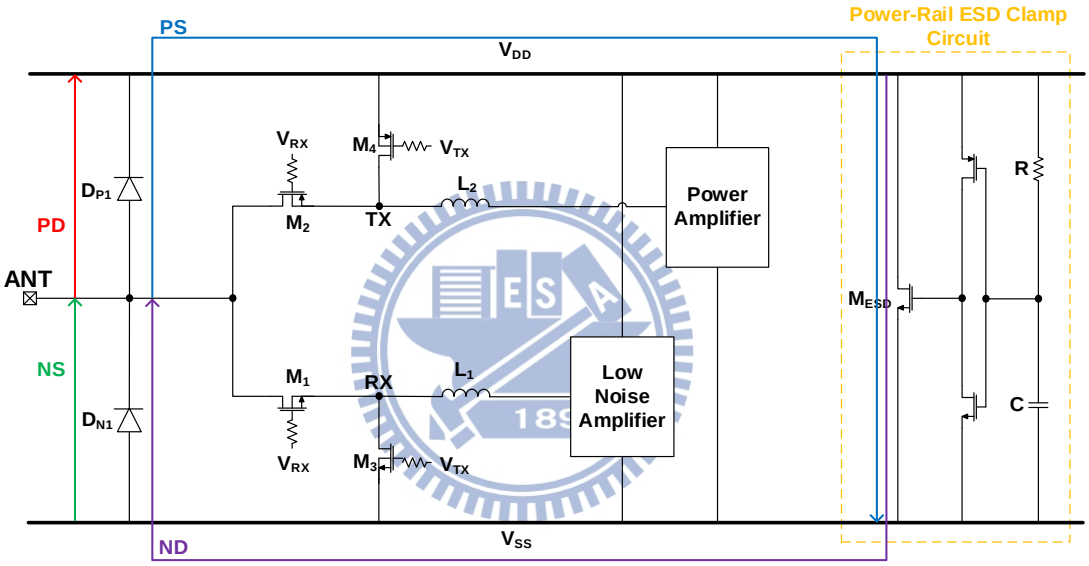



Fig. 3.6. The T/R switch front-end circuit with conventional ESD protection design of dual diodes.

## 3.3 Proposed ESD Protection Design for T/R Switch Front-End Circuit

To reduce the parasitic capacitance, which induced by ESD protection devices, the stacked diodes structure is proper choice. There are two types of ESD protection structure to improve the disadvantage in this section. Type 1 structure is for an ESD protection circuit with extra ESD protection devices. Type 2 structure is for an ESD protection circuit without any extra ESD protection device. The used power-rail ESD clamp circuit is the same as that used in

section 3.2.

Type 1 ESD protection design:

The cross-sectional view of ESD protection scheme with stacked diodes is illustrated in Fig. 3.7. As presented in section 3.1, the size of switching NMOS transistor and PMOS transistor are usually large in T/R switch, so the type 1 structure uses the NMOS body diode and PMOS body diode, which can protect the core circuit from ESD stress. The used ESD protection devices are the same as that used in section 3.2.

As shown in Fig. 3.7, there are stacked diodes, which consist of the embedded diode of switching transistor and ESD protection diode. One is connected between the ANT pad and $V_{DD}$ ($D_{P1}$ and $D_{P2}$), and the other is connected between the ANT pad and $V_{SS}$ ($D_{N1}$ and $D_{N2}$). $D_{P1}$ and $D_{P2}$ consist of P+/N-Well junction. $D_{N1}$ and $D_{N2}$ consist of P-well/N+ junction. Fig. 3.8 indicates the T/R switch front-end circuit with type 1 ESD protection design and shows the ESD discharge paths for the four different ESD testing modes.

Comparing with the conventional ESD protection design, the type 1 ESD protection design provides the whole chip ESD protection for all ESD-test. The stacked-diode structure can reduce the parasitic capacitance and decrease the degradation of RF performance which is induced by ESD protection device.

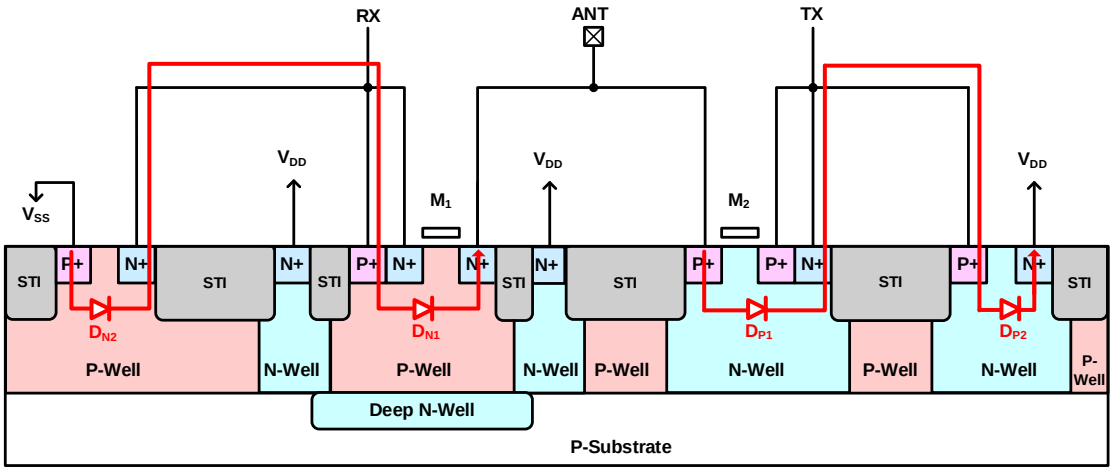



Fig. 3.7. Cross-sectional view of type 1 ESD protection design.

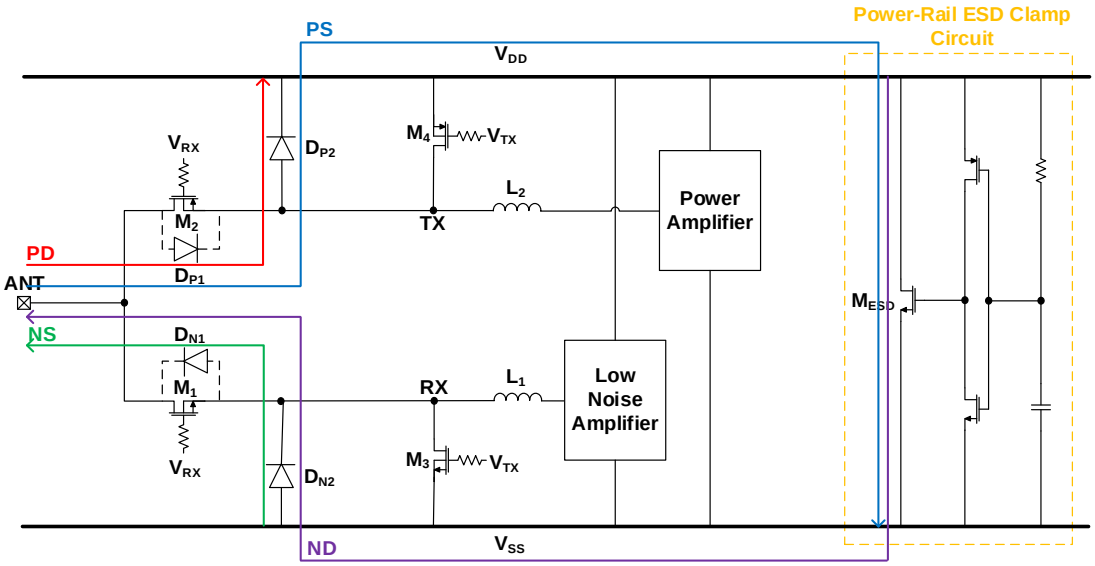



Fig. 3.8. The T/R switch front-end circuit with type 1 ESD protection design.

Type 2 ESD protection design:

The embedded diodes of switching transistors are applied to the type 1 ESD protection structure. To further decrease the degradation of RF performance caused by ESD protection devices, the type 2 structure combines the T/R switch with ESD protection design.

Generally, the shunt transistors in T/R switch cannot provide enough the dimensions of embedded diodes to endure the ESD stress. Therefore, the width of shunt transistors are increased in type 2 structure to ensure the embedded diodes of shunt transistors can increase the ESD robustness. Moreover, if the shunt transistors width increases properly, the isolation of T/R switch can also be improved. In order to balance the RF performance and ESD robustness, choosing the sizes of the shunt transistors and impedance matching network are important for the type 2 structure. Both the sizes of the shunt NMOS transistor ($M_3$) and PMOS transistor ($M_4$) are determined with total width = 75μm.

Similar to the T/R switch without ESD protection design in Fig. 3.3, this design does not need to add extra ESD protection device. The cross-sectional view of ESD protection scheme with embedded stacked diodes is illustrated in Fig. 3.9. The type 2 structure combines two P-well/N+ diodes ($D_{N1}$ and $D_{N2}$) to form an embedded stacked diodes between the ANT pad and

$V_{SS}$, and two P+/N-Well diodes ($D_{P1}$ and $D_{P2}$) to form an embedded stacked diodes between the ANT pad and $V_{DD}$ by using layout skill. Fig. 3.10 indicates the ESD protection design with embedded stacked diodes and the ESD discharge paths for the four different ESD testing modes.

Comparing with the conventional ESD protection design and type 1 ESD protection design, the type 2 ESD protection design provides the whole chip ESD protection for all ESD-test without extra ESD protection device. The embedded stacked diodes structure can not only improve the impact of ESD protection devices on RF performance but also keep the good ESD robustness. The corresponding device parameters in T/R switch circuits are organized in Table 3.1.

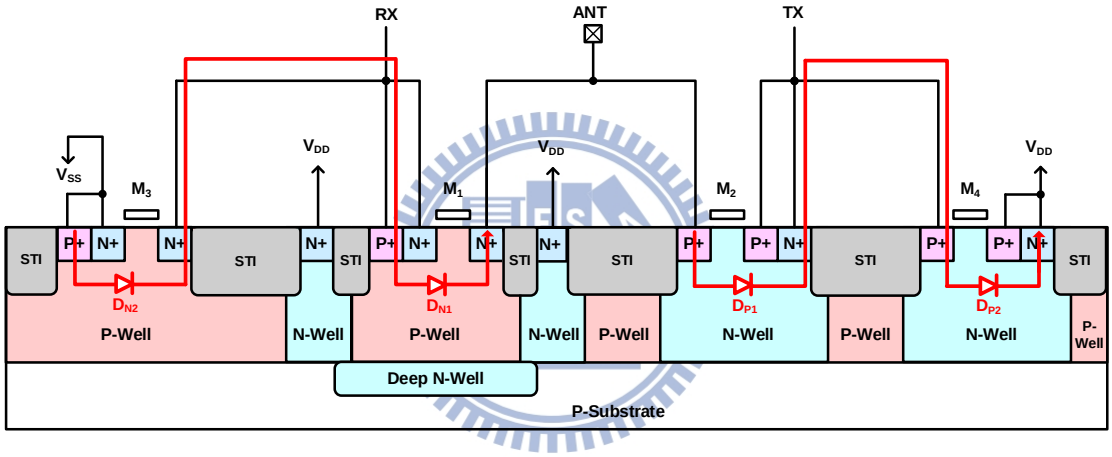



Fig. 3.9. Cross-sectional view of type 2 ESD protection design.

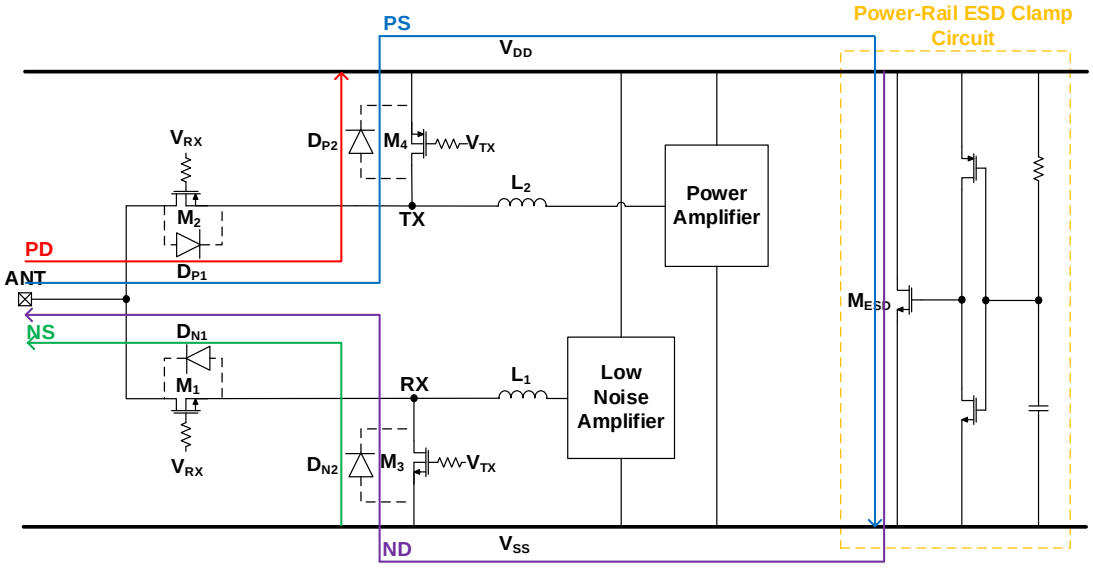



Fig. 3.10. The T/R switch front-end circuit with type 2 ESD protection design.

Table 3.1
Component values and device dimensions of the T/R switch circuits.

| | **Without ESD Protection Design** | **Conventional ESD Protection Design** | **Type 1 ESD Protection Design** | **Type 2 ESD Protection Design** |
|---|---|---|---|---|
| **Active Area of Parasitic Diode ($M_1/M_2/M_3/M_4$) ($\mu m^2$)** | 92.8 / 168 / 11.6 / 11.6 | 92.8 / 168 / 11.6 / 11.6 | 92.8 / 168 / 11.6 / 11.6 | 92.8 / 168 / 32.6 / 32.6 |
| **Active Area of ESD Diode ($D_P/D_N$) ($\mu m^2$)** | N/A | 37.6 / 37.6 | 37.6 / 37.6 | N/A |
| **M1 W/L (μm/μm)** | 200/0.18 | 200/0.18 | 200/0.18 | 200/0.18 |
| **M2 W/L (μm/μm)** | 400/0.18 | 400/0.18 | 400/0.18 | 400/0.18 |
| **M3 W/L (μm/μm)** | 25/0.18 | 25/0.18 | 25/0.18 | 75/0.18 |
| **M4 W/L (μm/μm)** | 25/0.18 | 25/0.18 | 25/0.18 | 75/0.18 |

## 3.4 Experimental Results of T/R Switch Front-End Circuits with ESD Protection Designs

The chip photo of the T/R switch front-end circuit without ESD protection is shown in Fig. 3.11. The chip photo of the T/R switch front-end circuit with conventional ESD protection design is shown in Fig. 3.12. The chip photo of the T/R switch front-end circuit with type 1 ESD protection design is shown in Fig. 3.13. The chip photo of the T/R switch front-end circuit with type 2 ESD protection design is shown in Fig. 3.14.

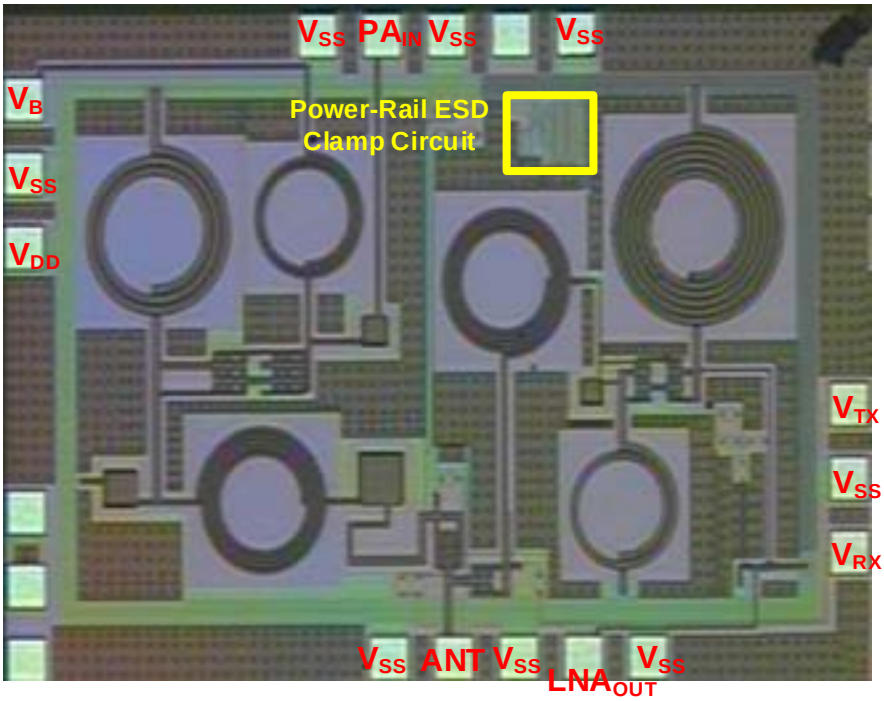



Fig. 3.11. The chip photo of the T/R switch front-end circuit without ESD protection design.

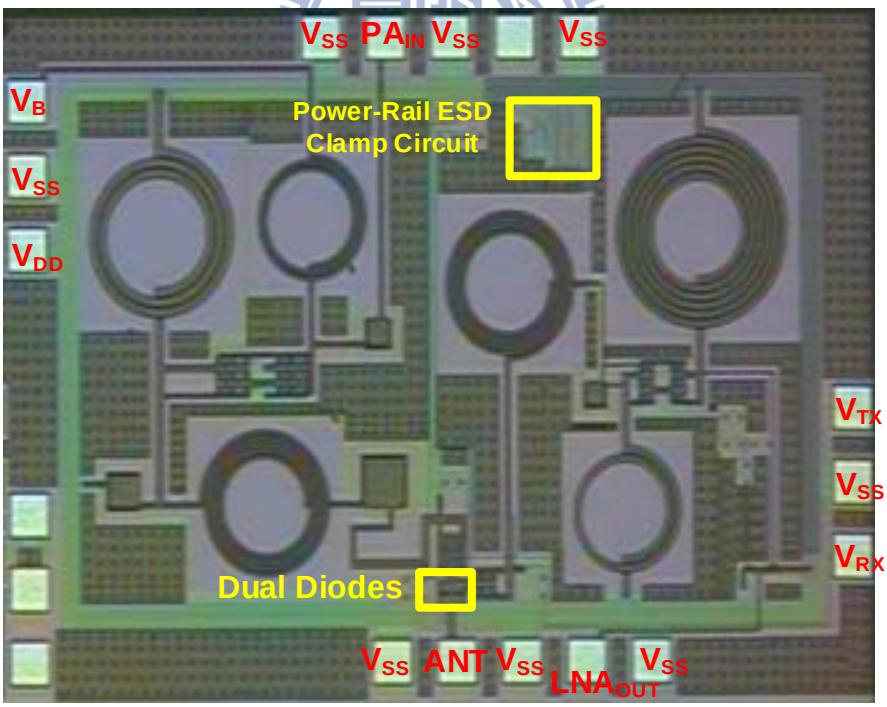



Fig. 3.12. The chip photo of the T/R switch front-end circuit with conventional ESD protection design.

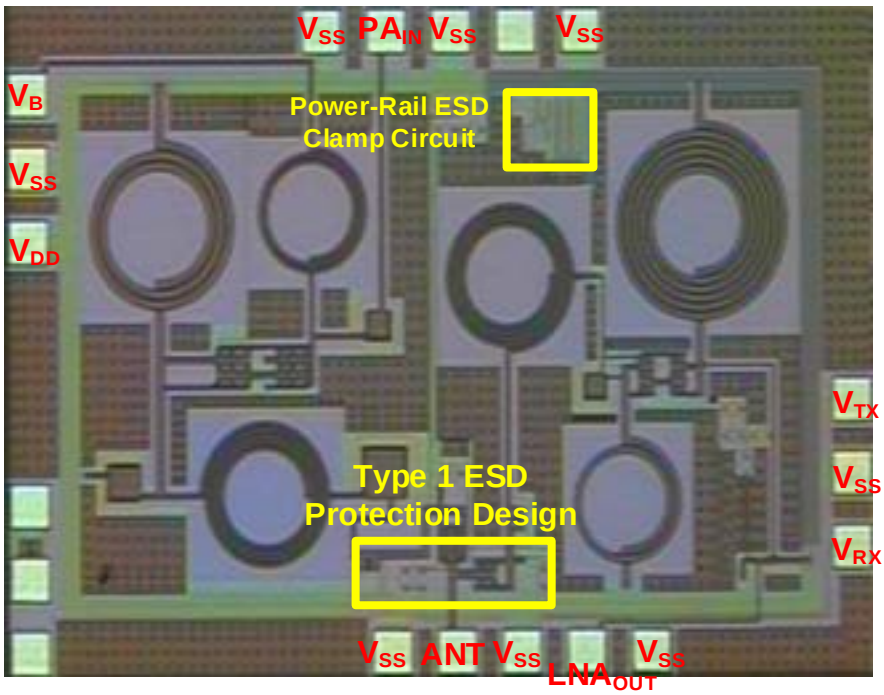



Fig. 3.13. The chip photo of the T/R switch front-end circuit with type 1 ESD protection design.

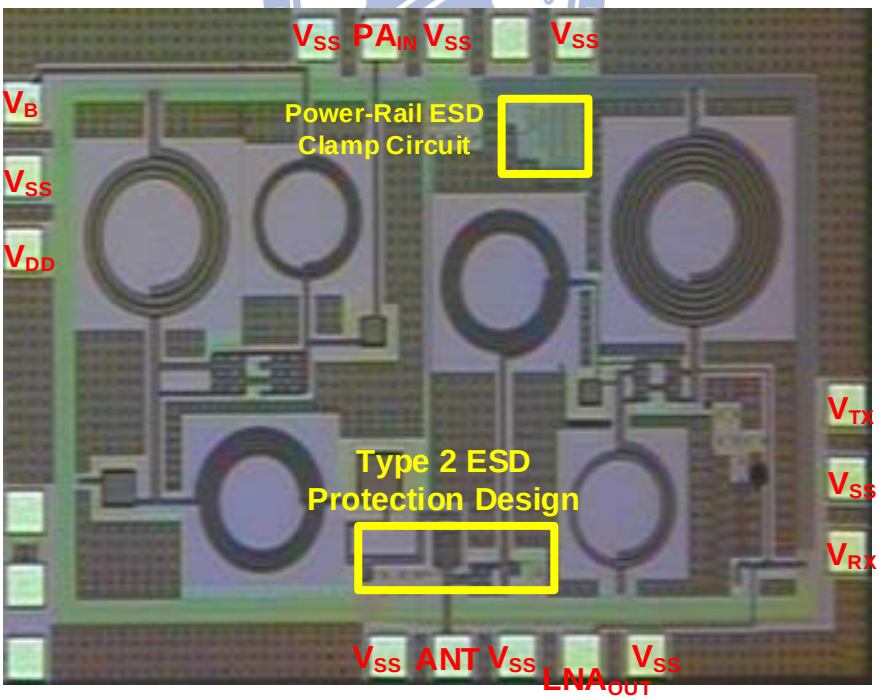



Fig. 3.14. The chip photo of the T/R switch front-end circuit with type 2 ESD protection design.

### *3.4.1 ESD Levels Measured with ESD Tester*

The human-body-model (HBM) level usually represents the ESD robustness of the test circuit. To evaluate the ESD robustness, the ESD pulses are stressed to each test circuit under different ESD stress conditions (PS-mode, PD-mode, NS-mode, and ND-mode) by using Agilent HCE-5000. The failure criterion is defined as the I-V characteristics seen at ANT pad shifting over 30% from its original curve after ESD stress. The ESD robustness of each mode of every test circuit is summarized in Table 3.2.

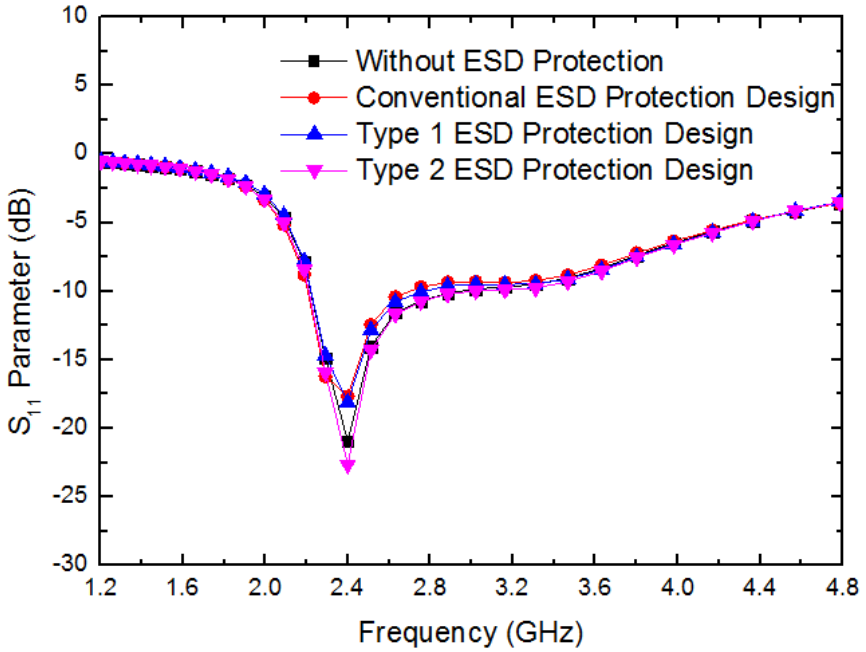
Table 3.2
Measured ESD level of each zapping mode with HBM tester.

| | **PS HBM (kV)** | **PD HBM (kV)** | **NS HBM (kV)** | **ND HBM (kV)** | **$V_{DD}$-to $V_{SS}$ (kV)** |
|---|---|---|---|---|---|
| **Without ESD Protection Design** | 1 | 1.5 | 1.5 | 1.5 | >8 |
| **Conventional ESD Protection Design** | 2.5 | 6 | 6 | 5.75 | |
| **Type 1 ESD Protection Design** | 2 | 5.75 | 5.5 | 4.5 | |
| **Type 2 ESD Protection Design** | 2.5 | 2.75 | 3.75 | 3.25 | |

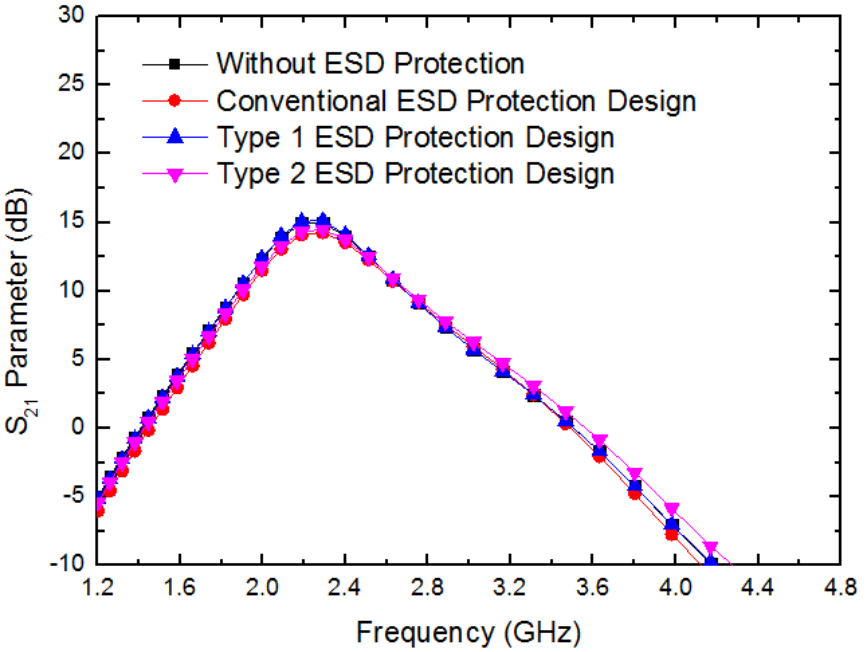
### *3.4.2 Comparison of RF Performances Before ESD Stress*

The S-parameters were measured by using the Agilent 5230A network analyzer. The output power and power gain were measured by using the Agilent E4440A spectrum analyzer with the Agilent E8247C signal generator. The noise figure was measured by using the Agilent N8975A noise figure analyzer with the Agilent 346C noise source. Each T/R switch front-end circuit operates with the $V_{DD}$ supply of 1.8V and is biased at 0.9V.

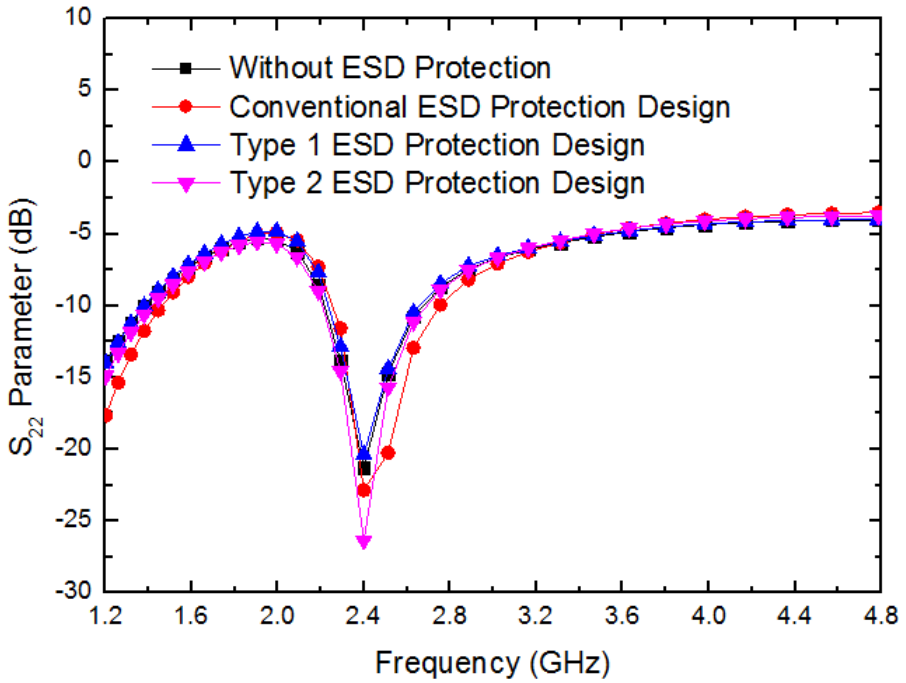
Before ESD stress, the comparison of measurement results of T/R switch front-end circuit with and without ESD protection are demonstrated in Figs. 3.15 to 3.19. In the TX mode, Fig. 3.15 shows the comparison of the measured S-parameters; Fig. 3.16 and Fig. 3.17 show the comparison of the measured output power ($P_{OUT}$) and power gain versus input power ($P_{IN}$), respectively. In the RX mode, Fig. 3.18 shows the comparison of the measured S-parameters; Fig. 3.19 shows the comparison of the measured noise figure.




(a)




(b)




(c)

Fig. 3.15. Comparison of measured (a) $S_{11}$, (b) $S_{21}$, and (c) $S_{22}$ of the T/R switch front-end circuits with and without ESD protection design in TX mode.

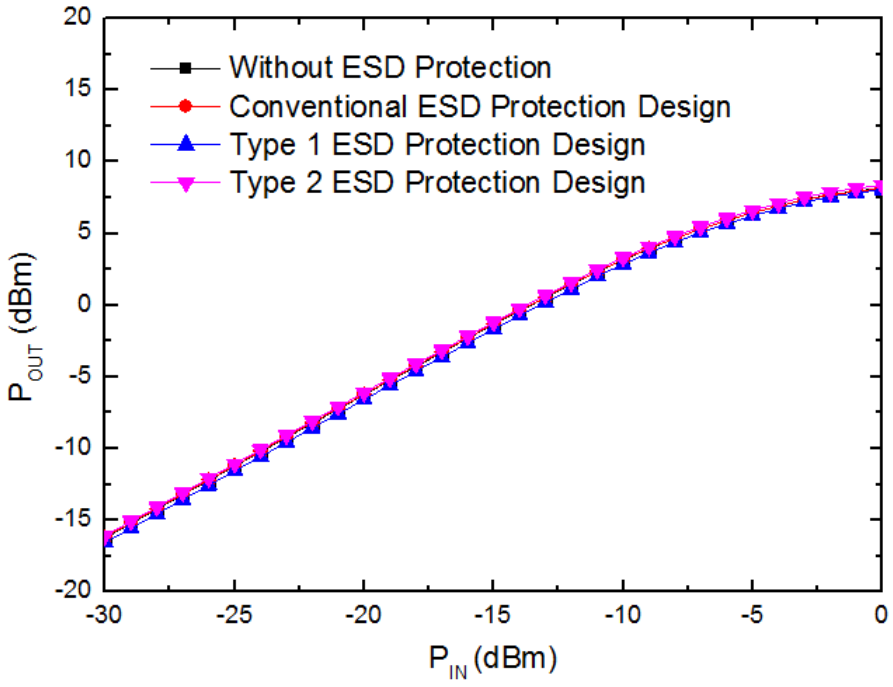



Fig. 3.16. Comparison of measured output power of the T/R switch front-end circuits with and without ESD protection design in TX mode.

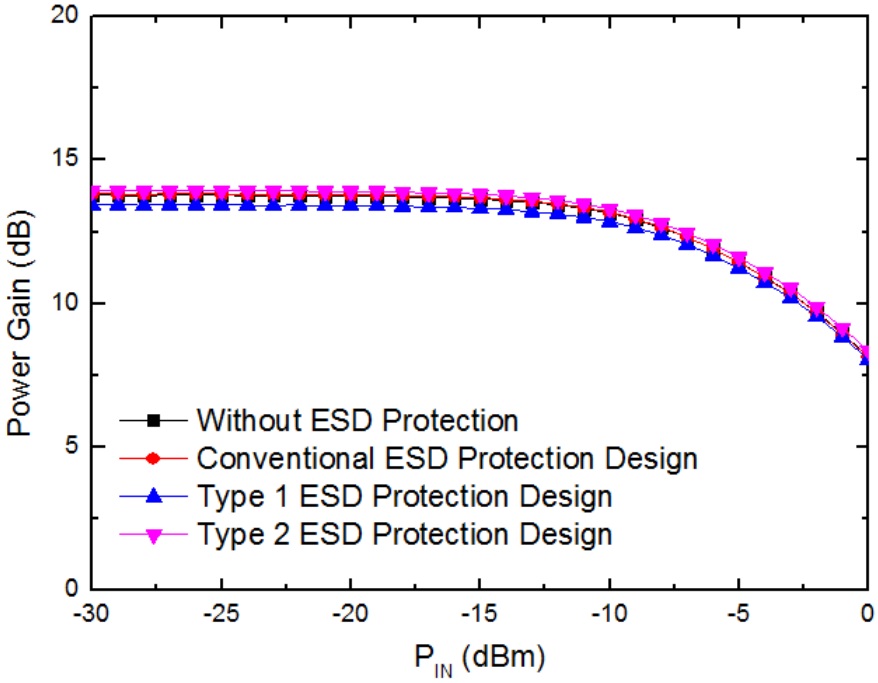
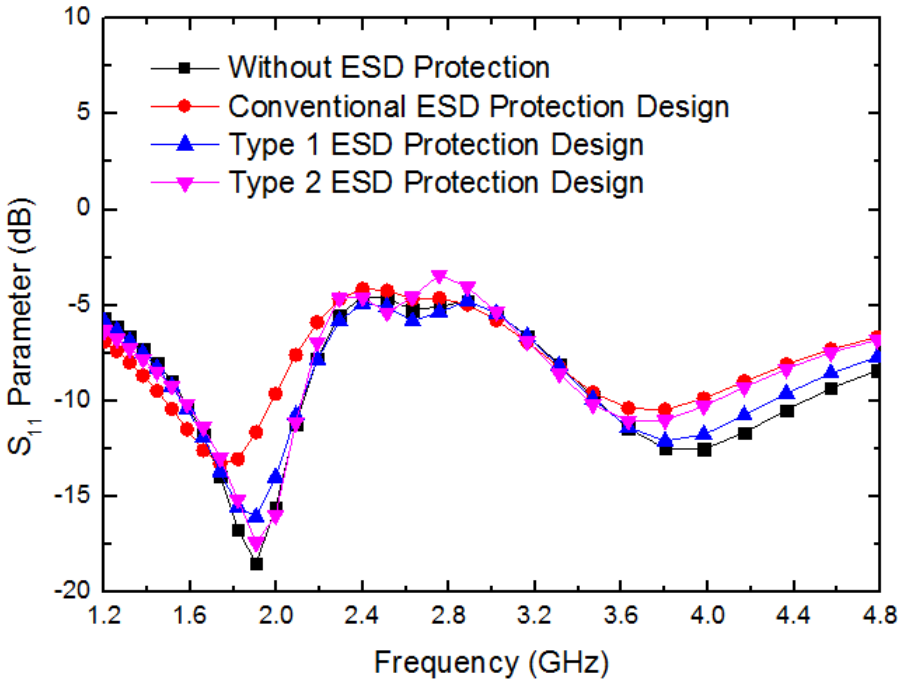
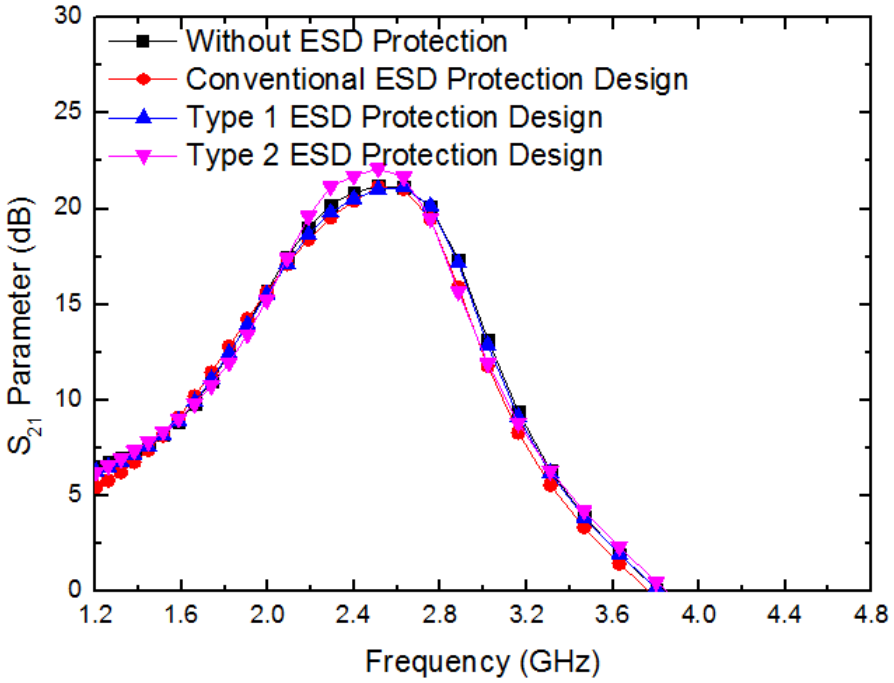


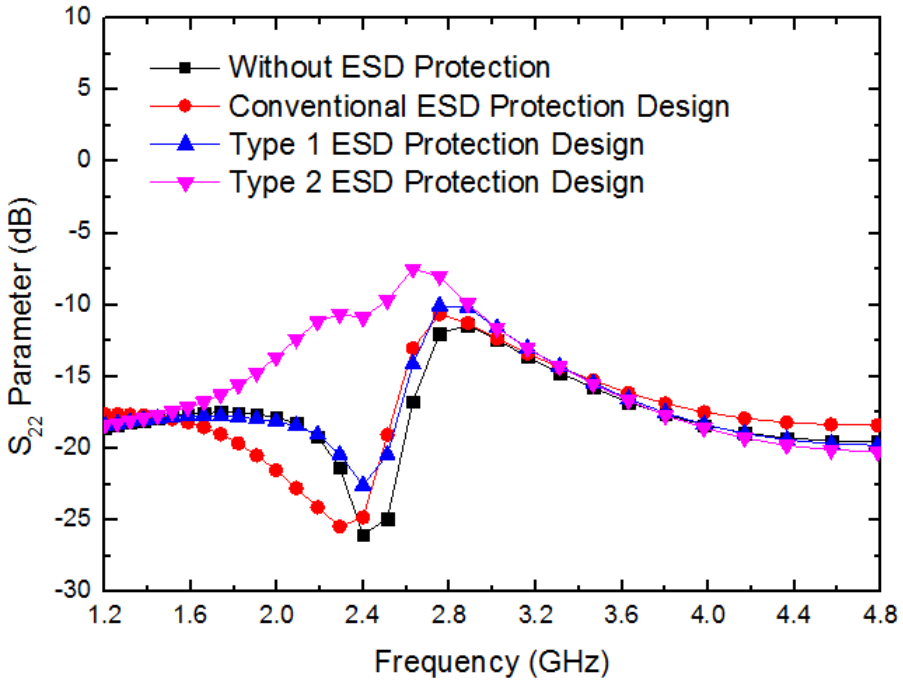

Fig. 3.17. Comparison of measured power gain of the T/R switch front-end circuits with and without ESD protection design in TX mode.




(a)




(b)




(c)

Fig. 3.18. Comparison of measured (a) $S_{11}$, (b) $S_{21}$, and (c) $S_{22}$ of the T/R switch front-end circuits with and without ESD protection design in RX mode.

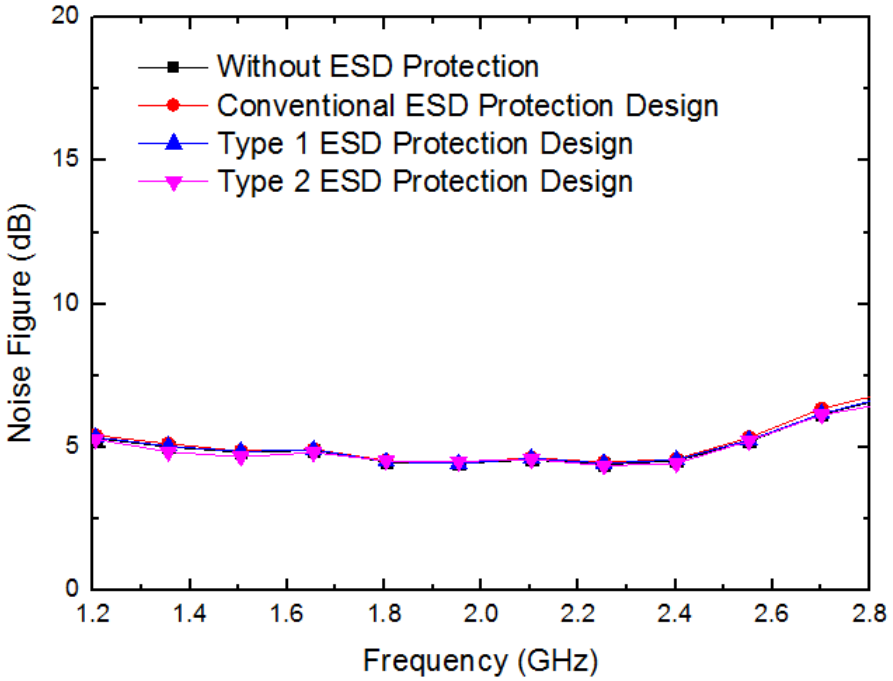



Fig. 3.19. Comparison of measured noise figure of the T/R switch front-end circuits with and without ESD protection design in RX mode.

### *3.4.3 Comparison of RF Performances After ESD Stress*

In order to verify the ability of ESD protection design, the RF performances of all T/R switch front-end circuits have to be re-measured after HBM ESD zapping with every mode (PS-mode, PD-mode, NS-mode, and ND-mode).

Figs. 3.20 to 3.24 show the RF performances of the T/R switch front-end circuit before and after HBM ESD zapping. Figs. 3.25 to 3.29 show the RF performances of the T/R switch front-end circuit with conventional ESD protection design before and after HBM ESD zapping. Figs. 3.29 to 3.33 show the RF performances of the T/R switch front-end circuit with type 1 ESD protection design before and after HBM ESD zapping. Figs. 3.34 to 3.38 show the RF performances of the T/R switch front-end circuit with type 2 ESD protection design before and after HBM ESD zapping. The measurement results are shown in Table 3.3.

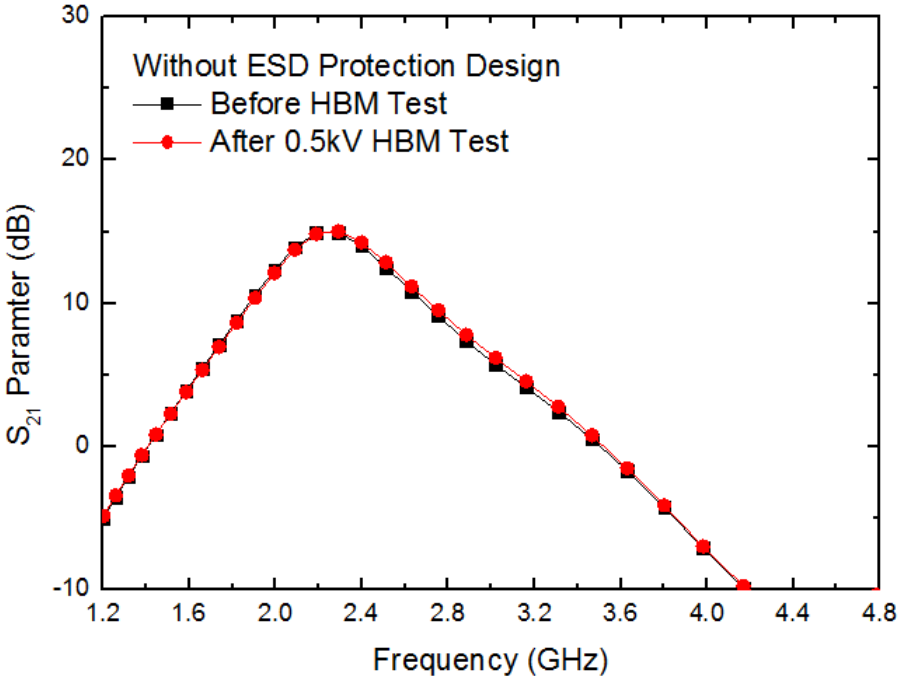



Fig. 3.20. Measured $S_{21}$ of the T/R switch front-end circuit without ESD protection design in TX mode after HBM ESD zapping.

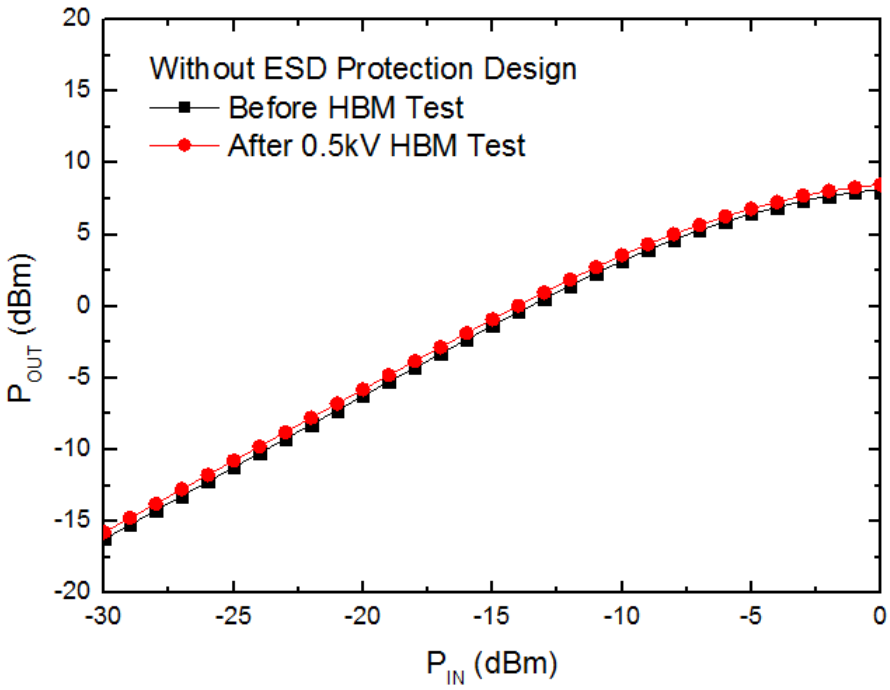



Fig. 3.21. Measured output power of the T/R switch front-end circuit without ESD protection design in TX mode after HBM ESD zapping.

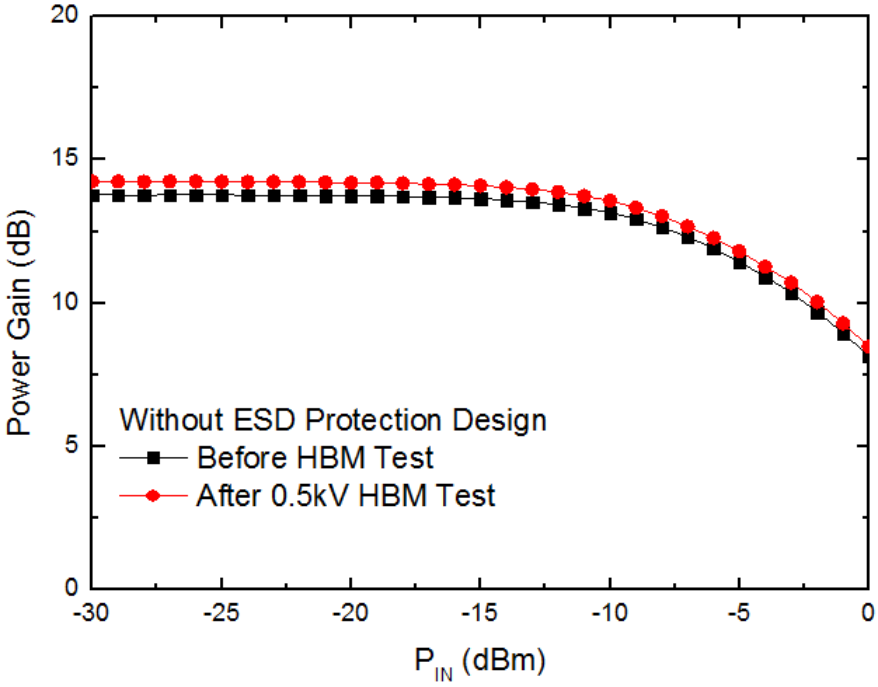



Fig. 3.22. Measured power gain of the T/R switch front-end circuit without ESD protection design in TX mode after HBM ESD zapping.

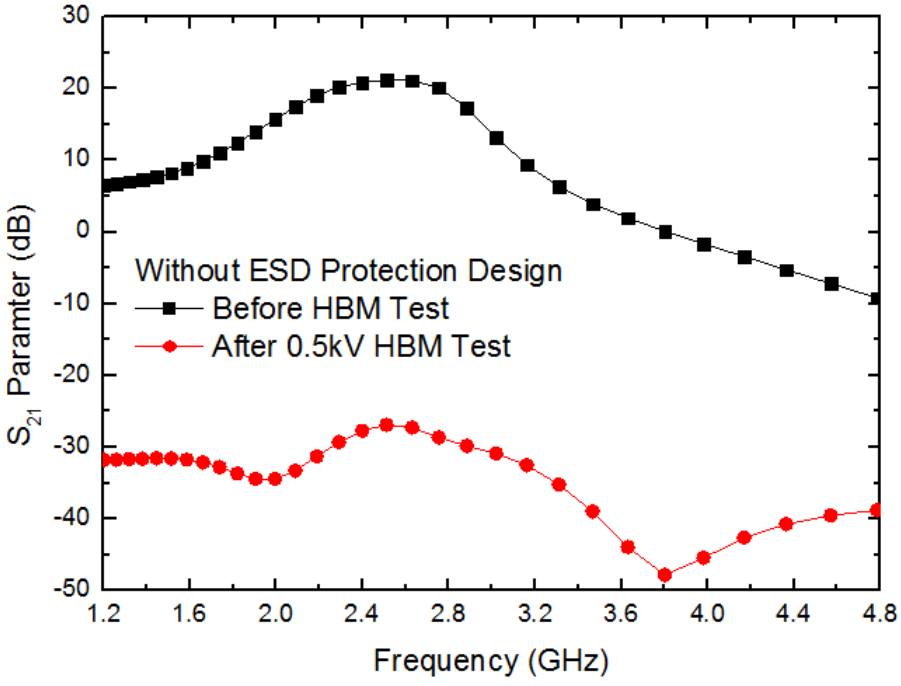



Fig. 3.23. Measured $S_{21}$ of the T/R switch front-end circuit without ESD protection design in RX mode after HBM ESD zapping.

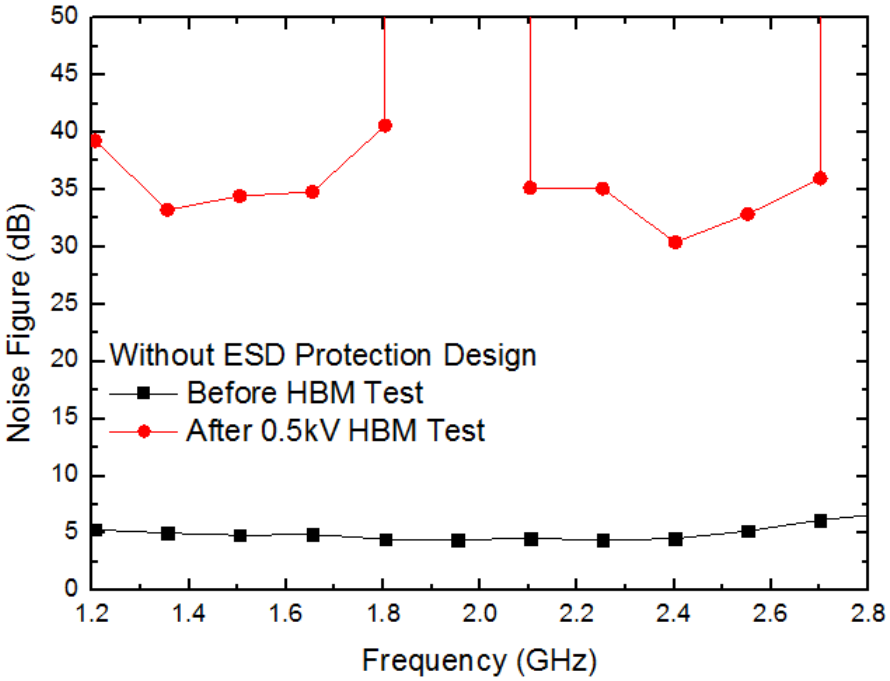



Fig. 3.24. Measured noise figure of the T/R switch front-end circuit without ESD protection design in RX mode after HBM ESD zapping.

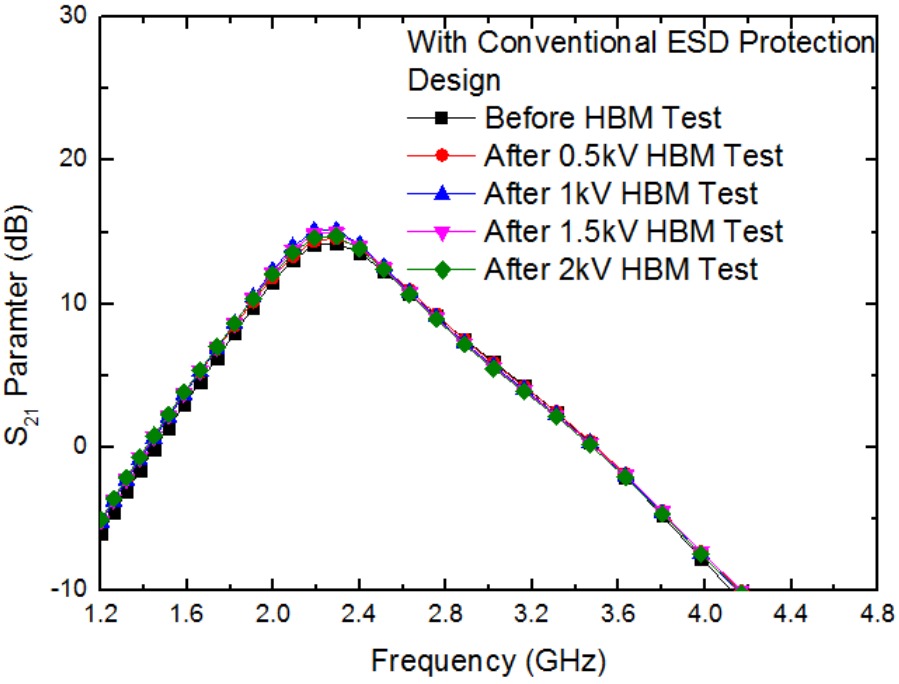



Fig. 3.25. Measured $S_{21}$ of the T/R switch front-end circuit with conventional ESD protection design in TX mode after HBM ESD zapping.

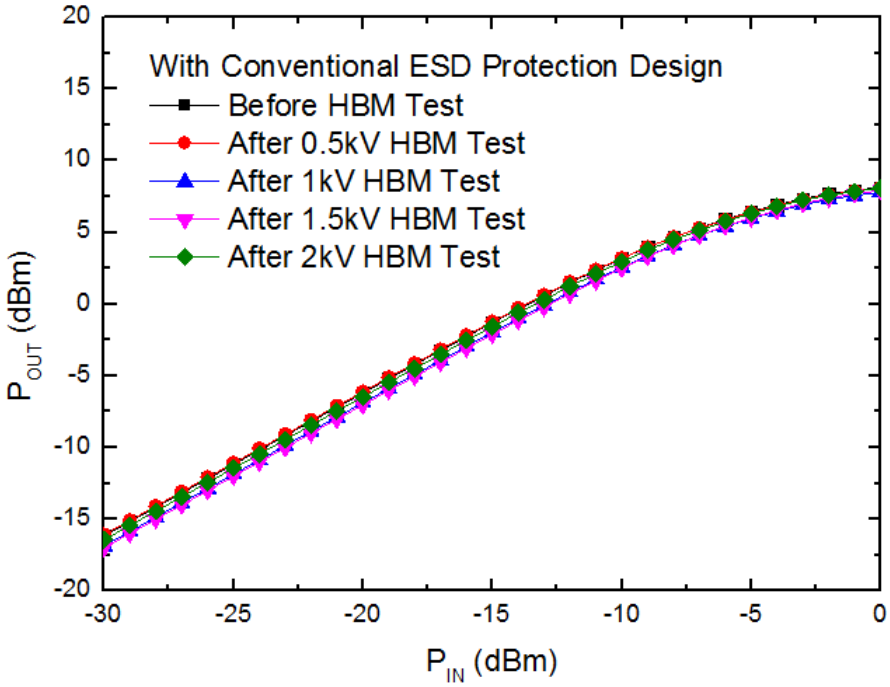



Fig. 3.26. Measured output power of the T/R switch front-end circuit with conventional ESD protection design in TX mode after HBM ESD zapping.

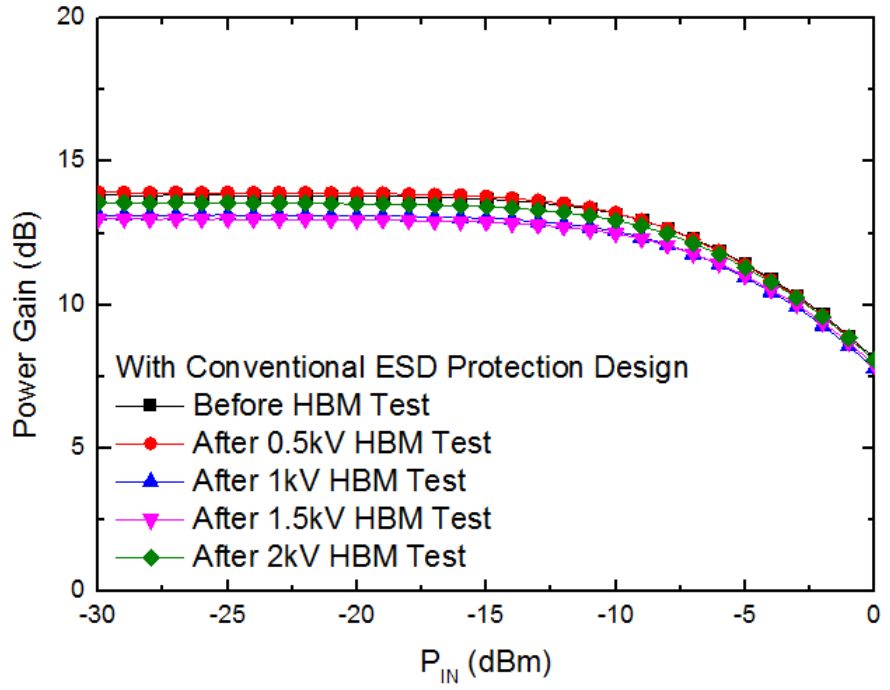



Fig. 3.27. Measured power gain of the T/R switch front-end circuit with conventional ESD protection design in TX mode after HBM ESD zapping.

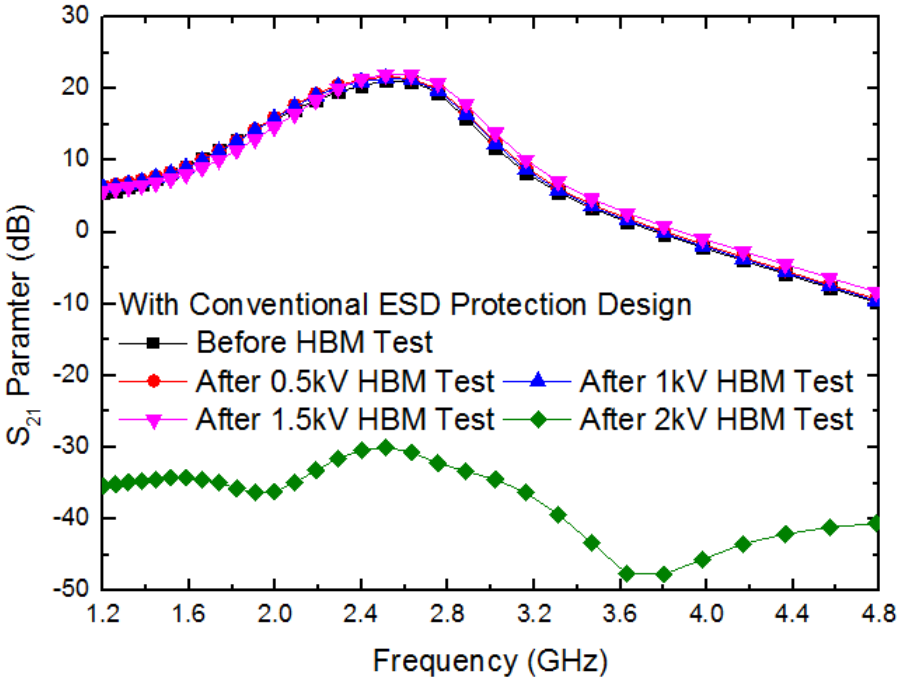



Fig. 3.28. Measured $S_{21}$ of the T/R switch front-end circuit with conventional ESD protection design in RX mode after HBM ESD zapping.

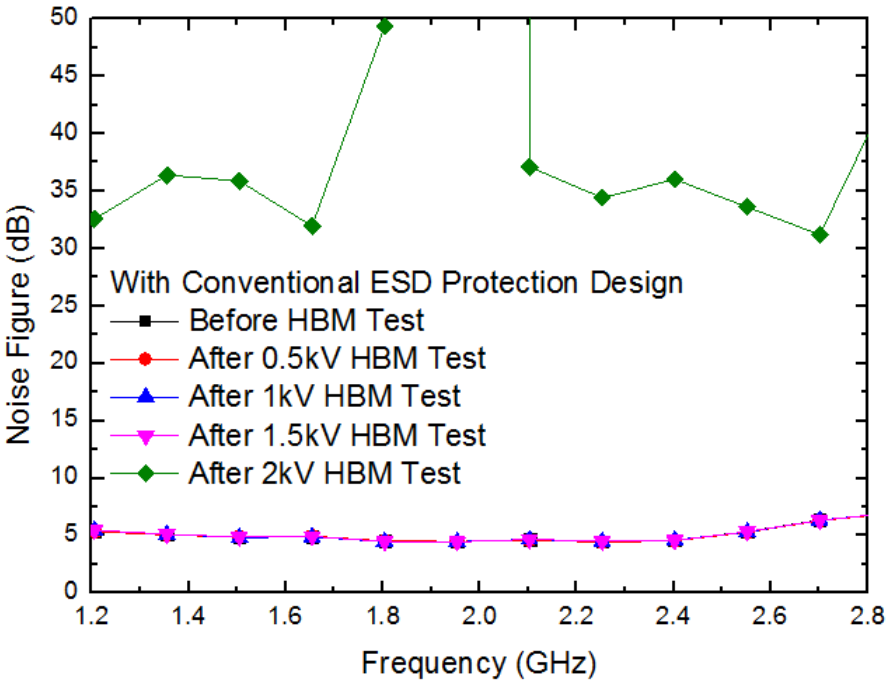



Fig. 3.29. Measured noise figure of the T/R switch front-end circuit with conventional ESD protection design in RX mode after HBM ESD zapping.

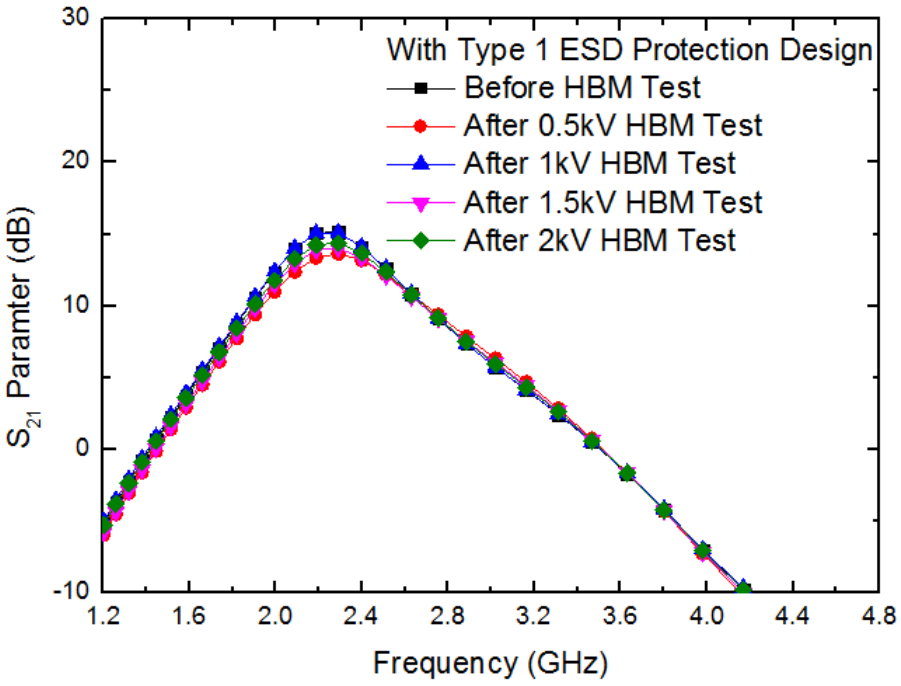



Fig. 3.30. Measured $S_{21}$ of the T/R switch front-end circuit with type 1 ESD protection design in TX mode after HBM ESD zapping.

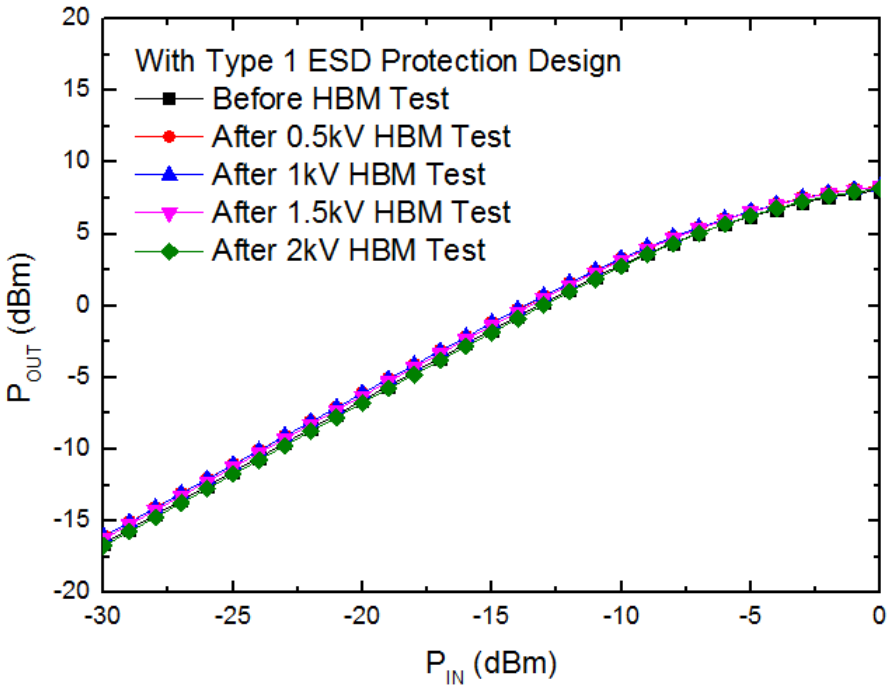



Fig. 3.31. Measured output power of the T/R switch front-end circuit with type 1 ESD protection design in TX mode after HBM ESD zapping.

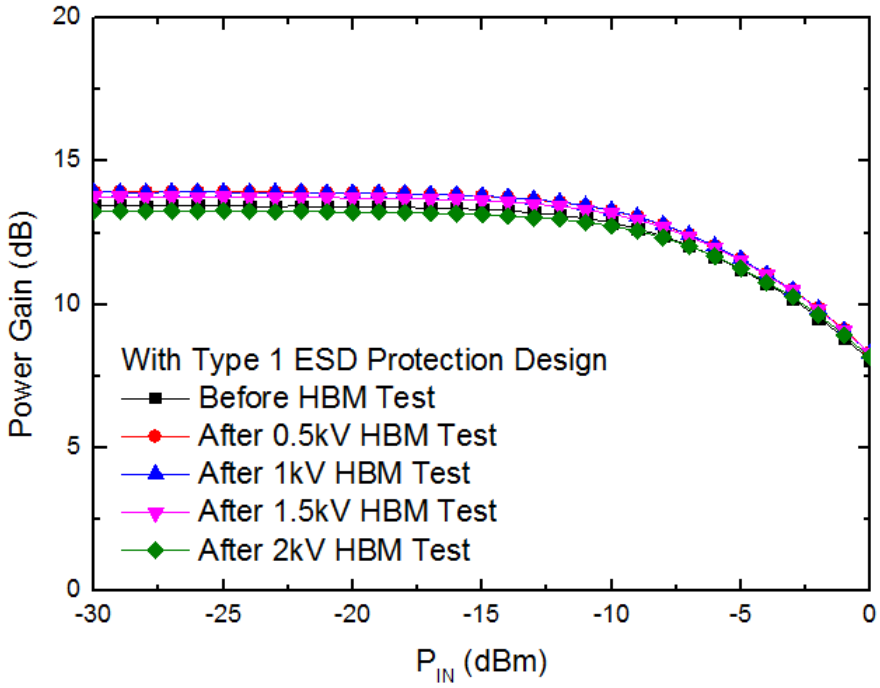



Fig. 3.32. Measured power gain of the T/R switch front-end circuit with type 1 ESD protection design in TX mode after HBM ESD zapping.

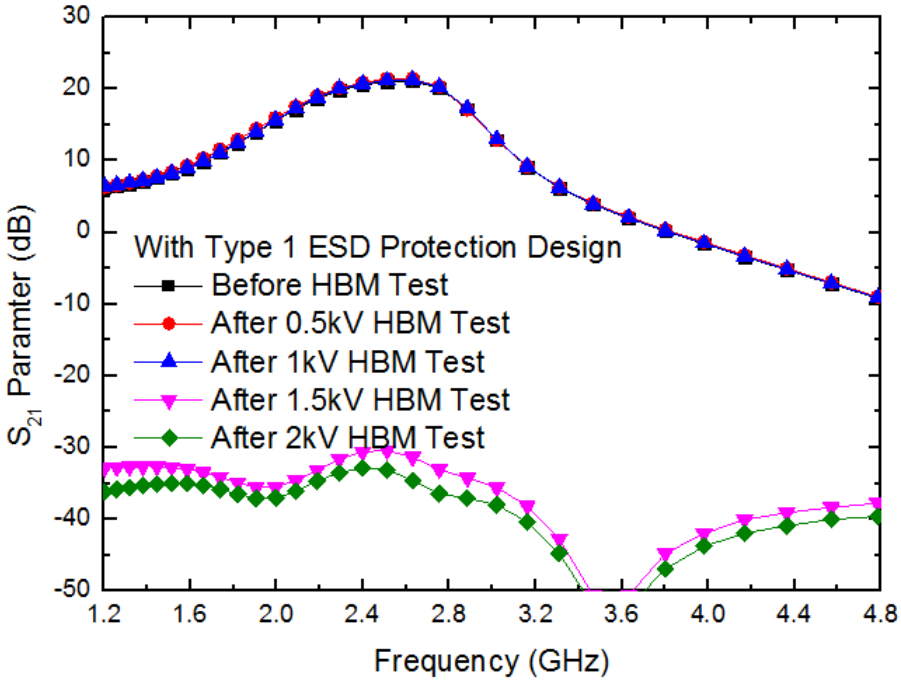



Fig. 3.33. Measured $S_{21}$ of the T/R switch front-end circuit with type 1 ESD protection design in RX mode after HBM ESD zapping.

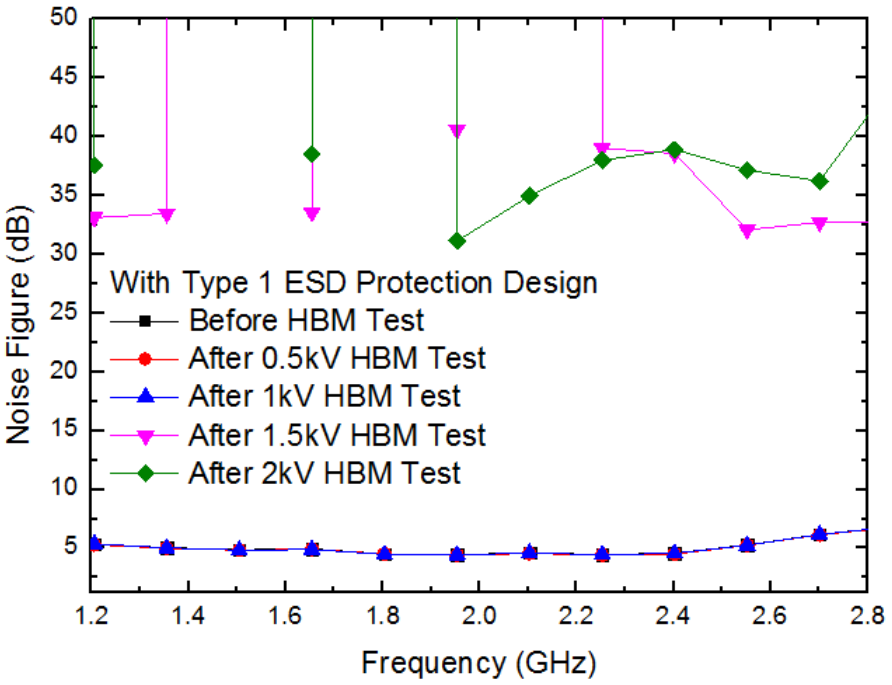



Fig. 3.34. Measured noise figure of the T/R switch front-end circuit with type 1 ESD protection design in RX mode after HBM ESD zapping.

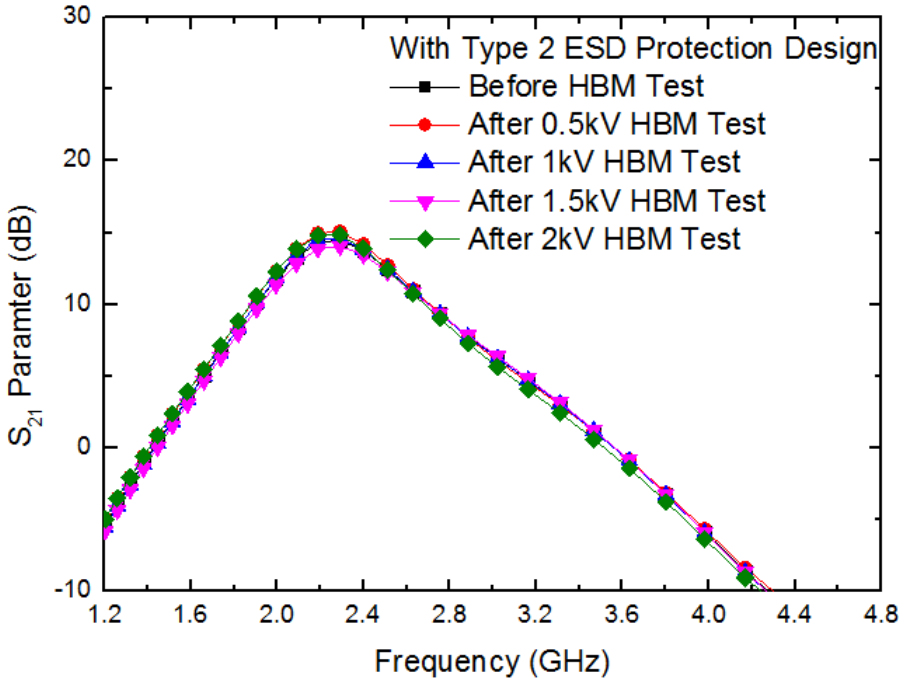



Fig. 3.35. Measured $S_{21}$ of the T/R switch front-end circuit with type 2 ESD protection design in TX mode after HBM ESD zapping.

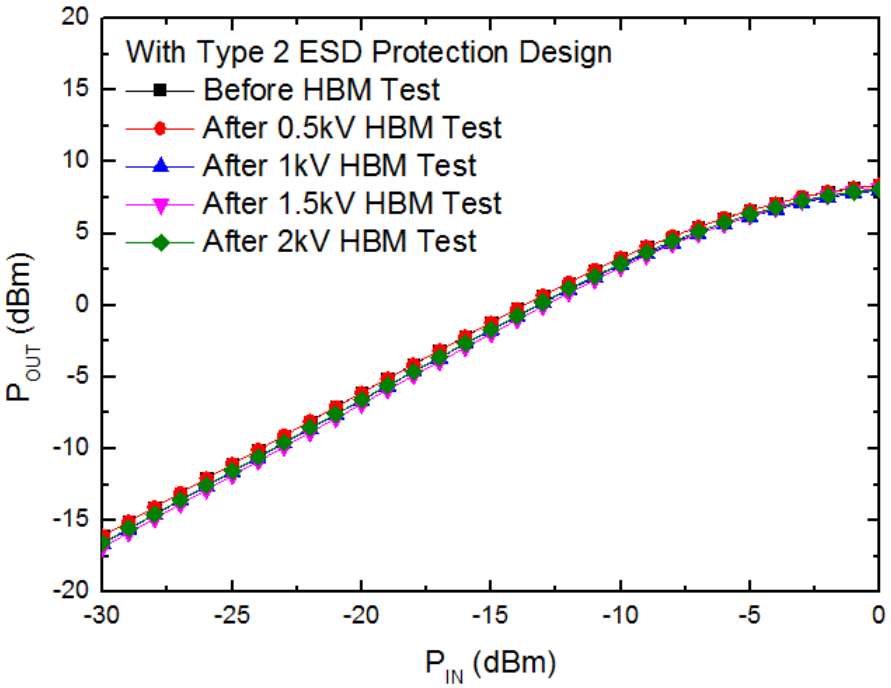



Fig. 3.36. Measured output power of the T/R switch front-end circuit with type 2 ESD protection design in TX mode after HBM ESD zapping.

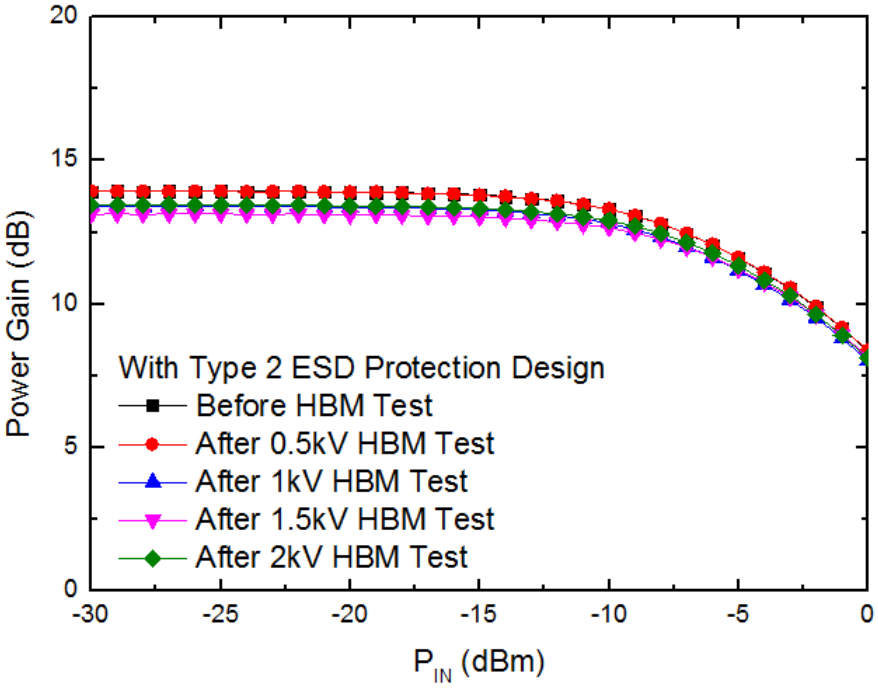



Fig. 3.37. Measured power gain of the T/R switch front-end circuit with type 2 ESD protection design in TX mode after HBM ESD zapping.

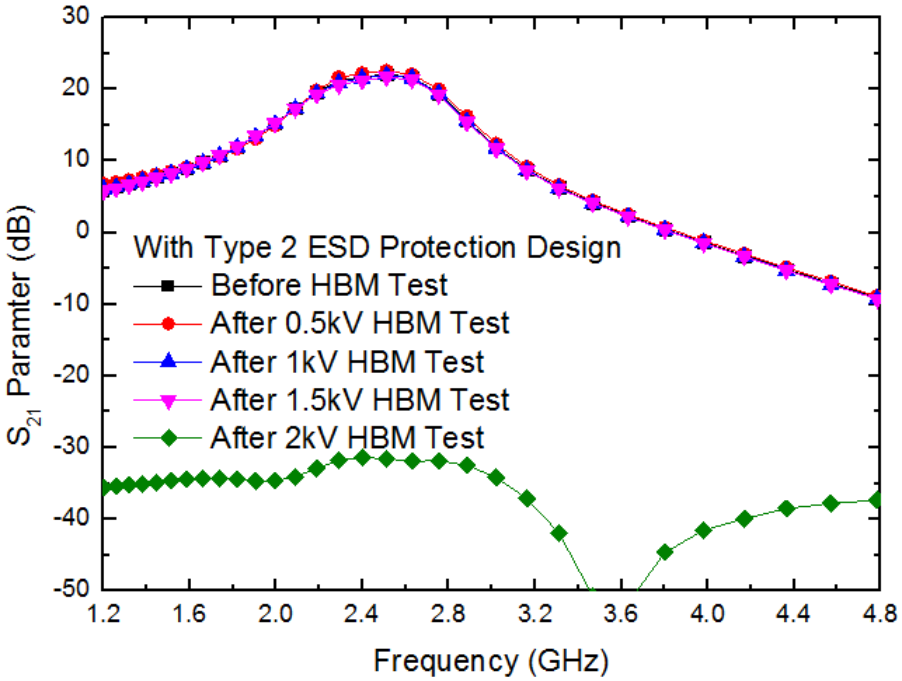



Fig. 3.38. Measured $S_{21}$ of the T/R switch front-end circuit with type 2 ESD protection design in RX mode after HBM ESD zapping.

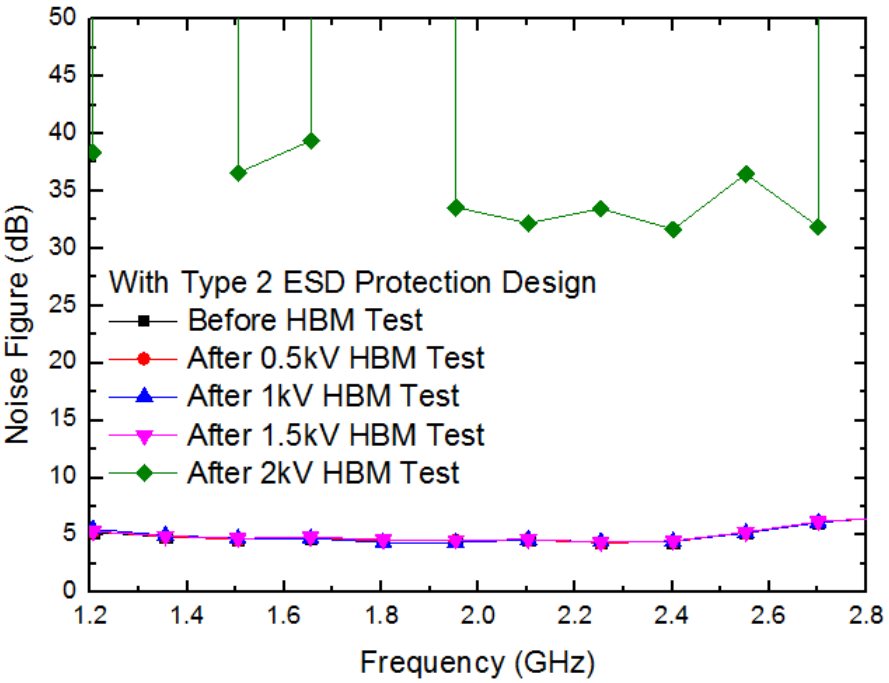



Fig. 3.39. Measured noise figure of the T/R switch front-end circuit with type 2 ESD protection design in RX mode after HBM ESD zapping.

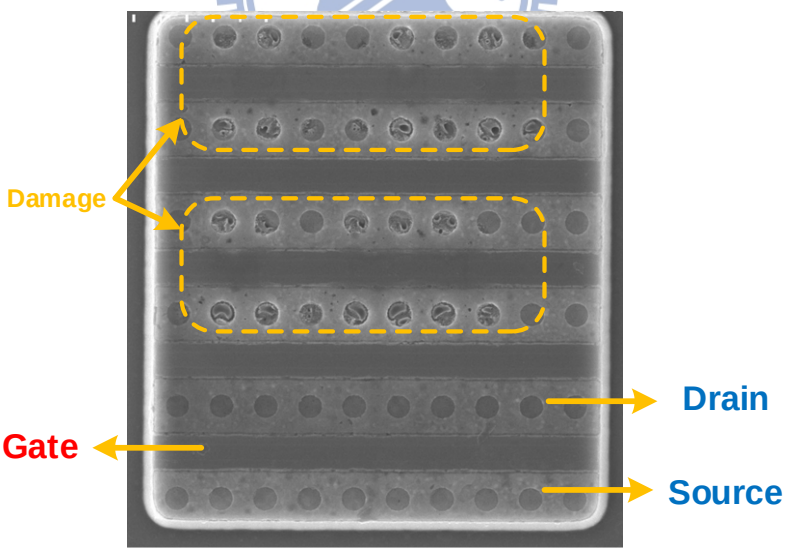
Table 3.3
Summary of RF performances of the T/R switch front-end circuits with and without ESD protection after HBM ESD zapping.

| | | | Before HBM ESD Zapping | After HBM ESD Zapping | | | | HBM ESD Level |
|---|---|---|---|---|---|---|---|---|
| | | | | 0.5kV | 1kV | 1.5kV | 2kV | |
| **Without ESD Protection Design** | **RX mode** | **S21 @ 2.4GHz (dB)** | 20.84 | -27.71 | N/A | N/A | N/A | <0.5kV |
| | | **Noise Figure @ 2.4GHz (dB)** | 4.53 | 30.39 | N/A | N/A | N/A | |
| | **TX mode** | **S21 @ 2.4GHz (dB)** | 14.01 | 14.25 | N/A | N/A | N/A | |
| | | **Maximum Output Power (dBm)** | 8.16 | 8.49 | N/A | N/A | N/A | |
| **Conventional ESD Protection Design** | **RX mode** | **S21 @ 2.4GHz (dB)** | 20.42 | 21.24 | 20.99 | 21.33 | -30.39 | 1.5kV |
| | | **Noise Figure @ 2.4GHz (dB)** | 4.59 | 4.54 | 4.6 | 4.58 | 36.01 | |
| | **TX mode** | **S21 @ 2.4GHz (dB)** | 13.54 | 13.9 | 14.14 | 14.04 | 13.85 | |
| | | **Maximum Output Power (dBm)** | 8.14 | 8.07 | 7.79 | 7.91 | 8.06 | |
| **Type 1 ESD Protection Design** | **RX mode** | **S21 @ 2.4GHz (dB)** | 20.52 | 20.87 | 20.73 | -30.58 | -32.82 | 1kV |
| | | **Noise Figure @ 2.4GHz (dB)** | 4.57 | 4.5 | 4.55 | 38.55 | 38.88 | |
| | **TX mode** | **S21 @ 2.4GHz (dB)** | 14.12 | 13.19 | 14.13 | 13.33 | 13.67 | |
| | | **Maximum Output Power (dBm)** | 8.05 | 8.31 | 8.29 | 8.3 | 8.16 | |
| **Type 2 ESD Protection Design** | **RX mode** | **S21 @ 2.4GHz (dB)** | 21.72 | 22.23 | 21.54 | 21.21 | -31.38 | 1.5kV |
| | | **Noise Figure @ 2.4GHz (dB)** | 4.44 | 4.43 | 4.47 | 4.49 | 31.64 | |
| | **TX mode** | **S21 @ 2.4GHz (dB)** | 13.74 | 14.19 | 13.82 | 13.45 | 13.89 | |
| | | **Maximum Output Power (dBm)** | 8.36 | 8.38 | 8.03 | 8.17 | 8.11 | |

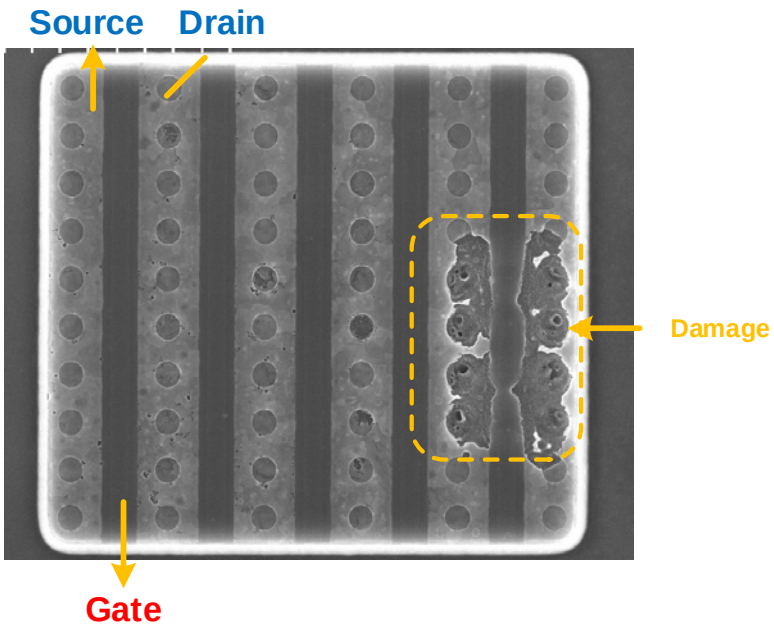
### *3.4.4 Failure Analysis and Discussion*

To further investigate the failure mechanism of the T/R switch front-end circuits with and without ESD protection design, scanning electron microscope (SEM) can be utilized to find the failure location.

Fig. 3.40 shows the SEM photos of the T/R switch front-end circuit without ESD protection after 0.5-kV HBM ESD test. The failure points are located at $M_3$ and $M_4$ in the T/R switch. Fig. 3.41 shows the SEM photo of the T/R switch front-end circuit with conventional ESD protection after 2-kV HBM ESD test. The failure points are located at $M_3$ in the T/R switch. Fig. 3.42 shows the SEM photo of the T/R switch front-end circuit with type 1 ESD protection after 1.5-kV HBM ESD test. The failure points are located at $M_3$ in the T/R switch. Fig. 3.43 shows the SEM photo of the T/R switch front-end circuit with type 2 ESD protection after 2-kV HBM ESD test. The failure points are located at $M_3$ in the T/R switch.




(a)




(b)

Fig. 3.40. SEM photos of (a) $M_3$ and (b) $M_4$ in T/R switch front-end circuit without ESD protection after 0.5-kV HBM ESD tests.

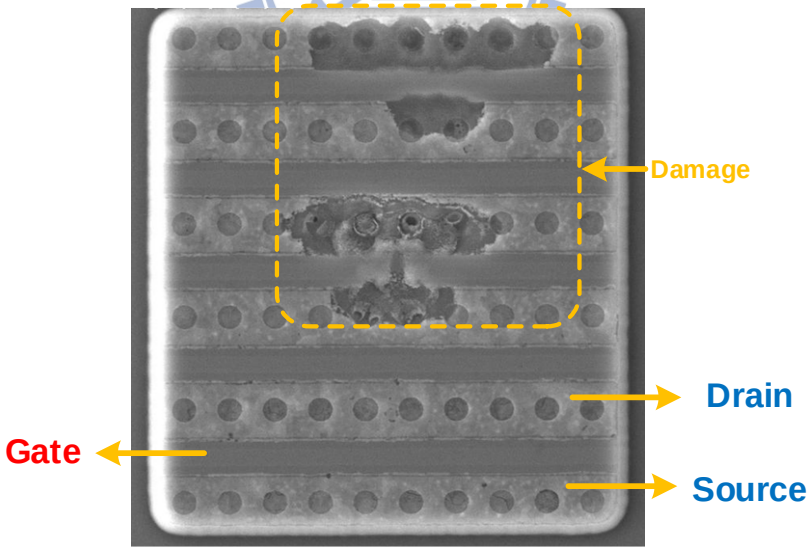



Fig. 3.41. SEM photo of $M_3$ in T/R switch front-end circuit with conventional ESD protection after 2-kV HBM ESD tests.

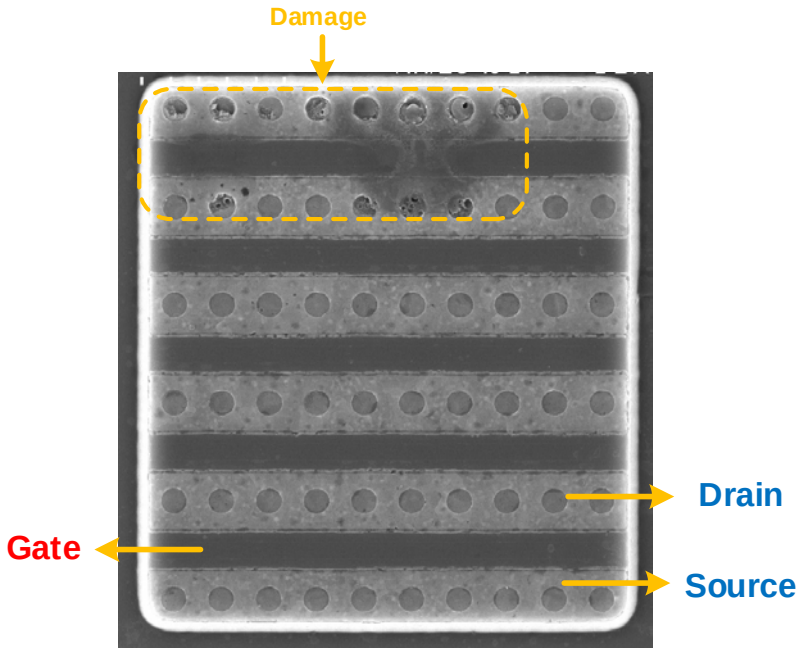



Fig. 3.42. SEM photo of $M_3$ in T/R switch front-end circuit with type 1 ESD protection after 1.5-kV HBM ESD tests.

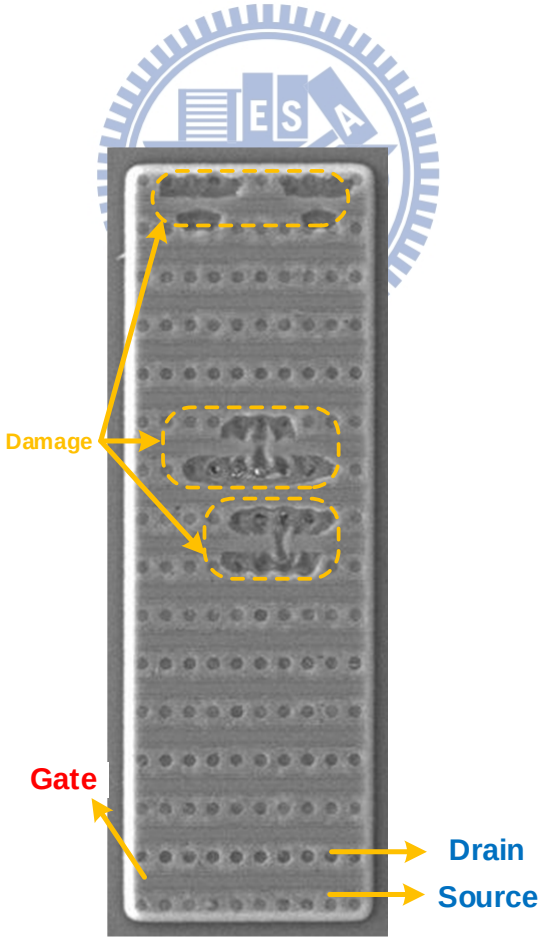
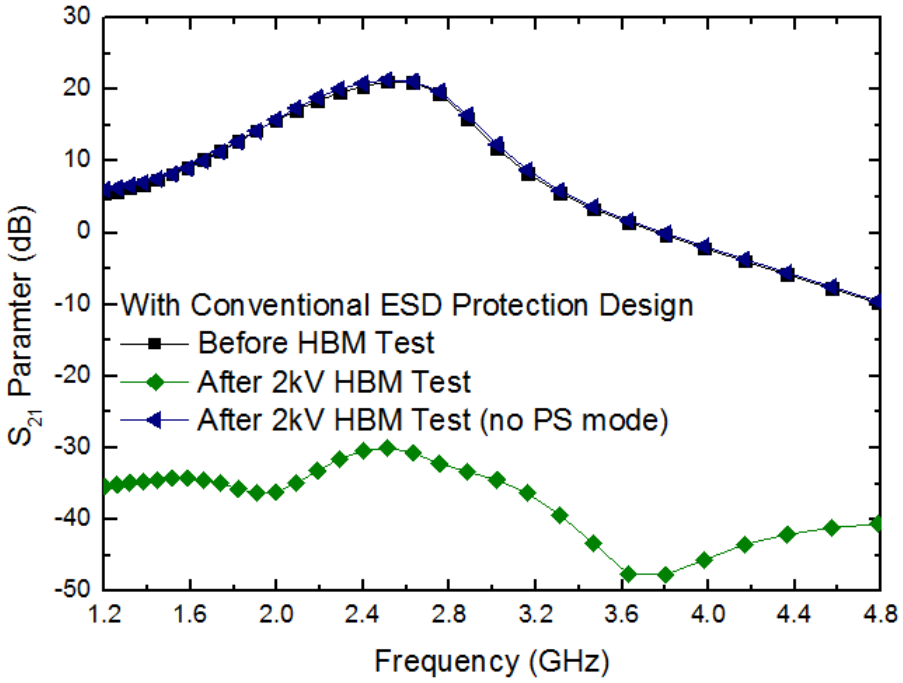
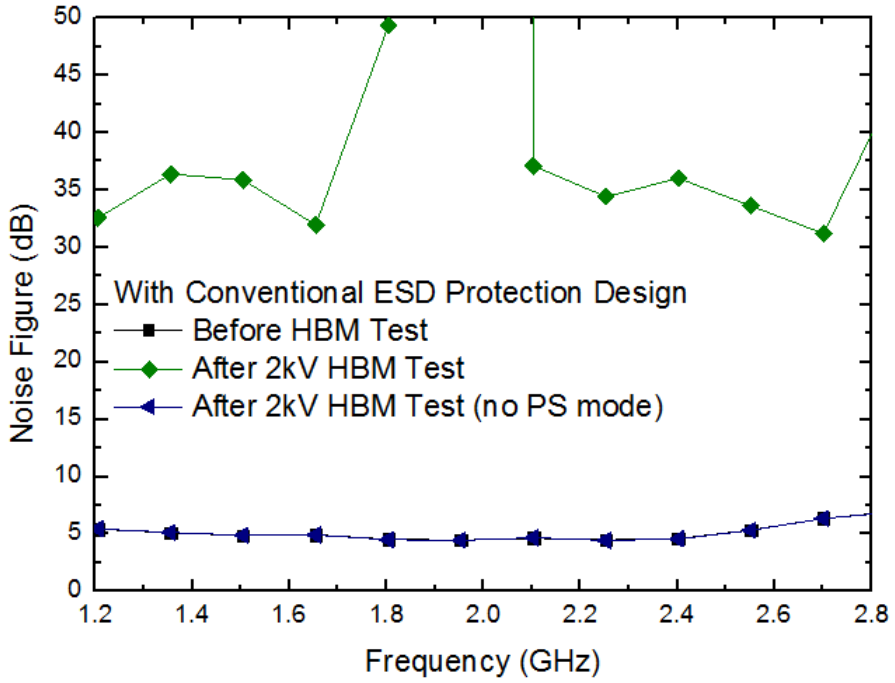



Fig. 3.43. SEM photo of $M_3$ in T/R switch front-end circuit with type 2 ESD protection after 2-kV HBM ESD tests.

To investigate the most critical ESD event for T/R switch front-end circuit, the degradation of RF performances in RX mode is an obvious indication. With conventional ESD protection design, Fig. 3.44 shows the RF performance comparisons of before, after 2-kV HBM ESD zapping of every mode and after 2-kV HBM ESD zapping of every mode except PS mode. With type 1 ESD protection design, Fig. 3.45 shows the RF performance comparisons of before, after 2-kV HBM ESD zapping of every mode and after 2-kV HBM ESD zapping of every mode except PS mode. With type 2 ESD protection design, Fig. 3.46 shows the RF performance comparisons of before, after 2-kV HBM ESD zapping of every mode and after 2-kV HBM ESD zapping of every mode except PS mode. It is clear that the positive-to-$V_{SS}$ ESD stress is the most critical ESD event.

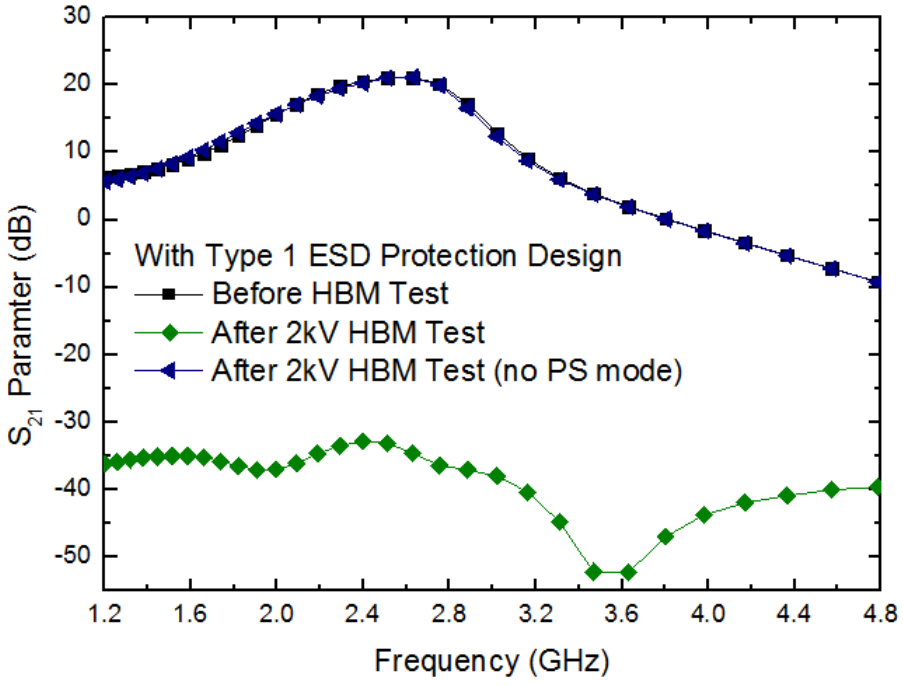



(a)

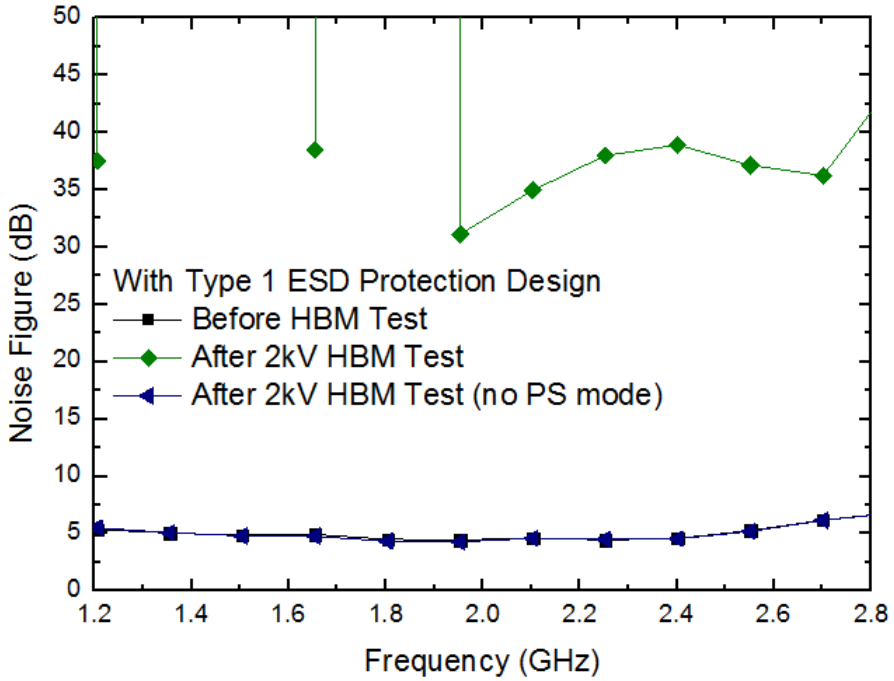



(b)

Fig. 3.44. Measured (a) S21 parameter and (b) noise figure of the T/R switch front-end circuit with conventional ESD protection design in RX mode after 2-kV HBM ESD zapping.

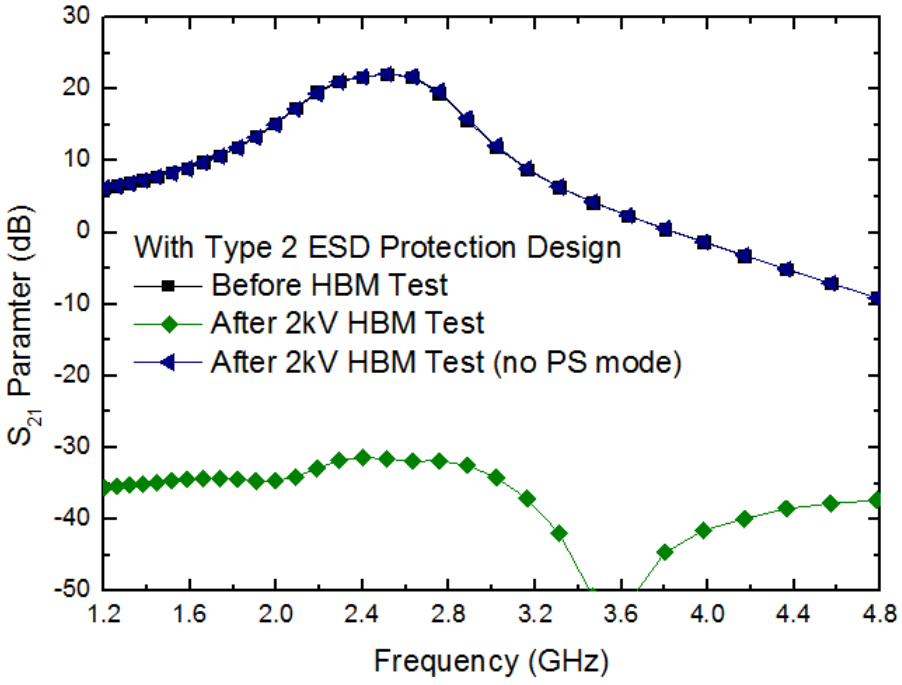



(a)

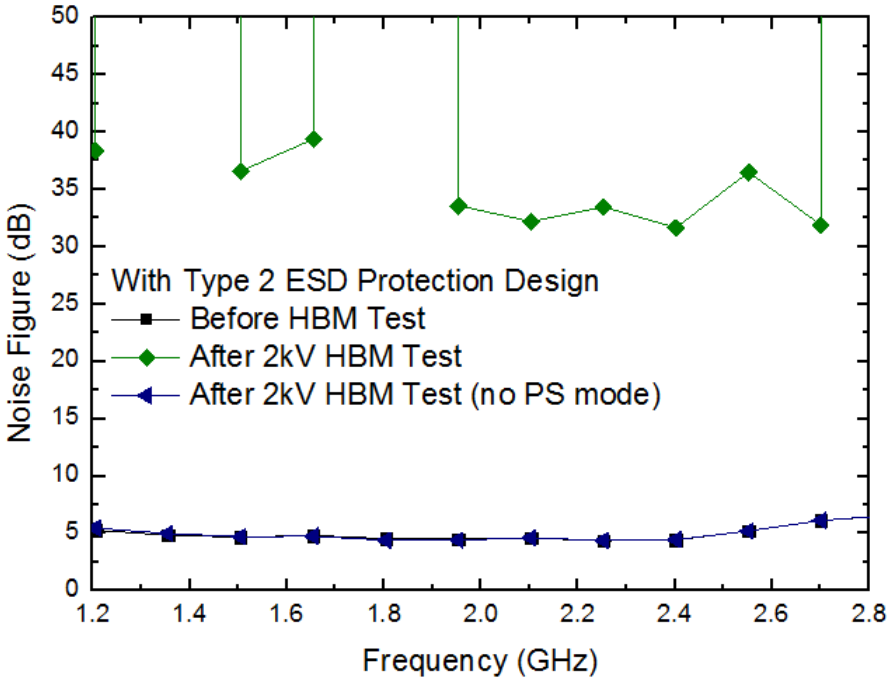



(b)

Fig. 3.45. Measured (a) S21 parameter and (b) noise figure of the T/R switch front-end circuit with type 1 ESD protection design in RX mode after 2-kV HBM ESD zapping.




(a)




(b)

Fig. 3.46. Measured (a) S21 parameter and (b) noise figure of the T/R switch front-end circuit with type 2 ESD protection design in RX mode after 2-kV HBM ESD zapping.

## 3.5 Summary

To verify the ESD level of ESD-protected T/R switch front-end circuits, there are two failure criterions after being zapped by ESD stress. One is over 30% shifting in the I-V characteristic, another one is degradation of the RF performance. It has been demonstrated in [22] that the second method is more suitable and accurate for RF circuits.

The RF performances of the T/R switch front-end circuit without ESD protection is degraded after 0.5-kV HBM test. The RF performances of the T/R switch front-end circuits with the conventional ESD protection design and with the proposed type 1 ESD protection design can achieve 1.5-kV HBM level and 1-kV HBM level, respectively. Without extra ESD protection device, T/R switch front-end circuit with the proposed type 2 ESD protection design can achieve 1.5-kV HBM level and the RF performances of this circuit is not degraded.

The failure analysis of un-protected T/R switch front-end circuit indicates that the failed function after HBM ESD zapping is caused by the damaged $M_3$ and $M_4$. However, the failure analysis of ESD-protected T/R switch front-end circuits indicates that the failed function after HBM ESD zapping is only caused by the damaged $M_3$. The experimental results reveal that the positive-to-$V_{SS}$ ESD stress is the most critical ESD event in the T/R switch front-end circuit.

# Chapter 4

# ESD Protection Designs for 2.4GHz Traditional T/R Switch Front-End Circuits

## 4.1 Circuit Design of 2.4GHz Traditional CMOS T/R Switch Front-End Circuit

Conventional, the T/R switch design follows a series/shunt architecture [13, 23], as show in Fig. 4.1. In the traditional structure, both the series and shunt transistors are NMOS transistors, whereas in the prior structure, as shown in Fig. 3.13, the $M_2$ and $M_4$ are PMOS transistors. The series transistors $M_1$ and $M_2$ perform switch function, whereas the shunt transistors $M_3$ and $M_4$ make the undesired signal grounded and enhance the isolation.

The body floating topology, which adds the large resistance at the bulk of switches ($R_{B1}$ and $R_{B2}$), is used in this design. As the bulk resistance becomes large, the bulk of transistor is floating at high frequency, and RF signal is not easy to couple to the bulk resistance. Consequently, this topology can reduce the substrate loss and improve the T/R switch's linearity and power handling capability.

To minimize the insertion loss, both the switching NMOS transistors size are determined with total width = 200μm, and channel length = 0.18μm. The shunt transistors are used to improve the isolation of the switch. For the shunt transistors, both the NMOS transistors size are determined with total width = 50μm.

The circuit schematic of the traditional T/R switch front-end circuit is shown in Fig. 4.2. The used structures of the PA and LNA are same as that used in section 3.1. To achieve high

power delivery and high gain at operation frequency, the input/output terminal of each circuit are matched to 50Ω.

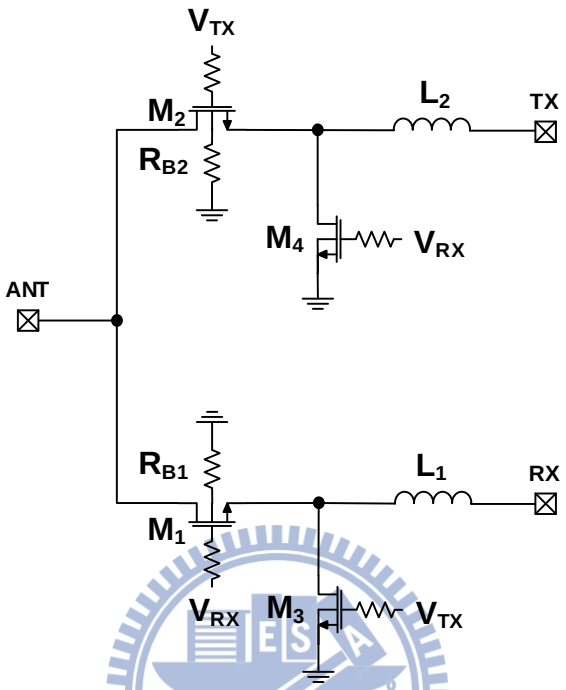



Fig. 4.1. Circuit schematic of traditional T/R switch.

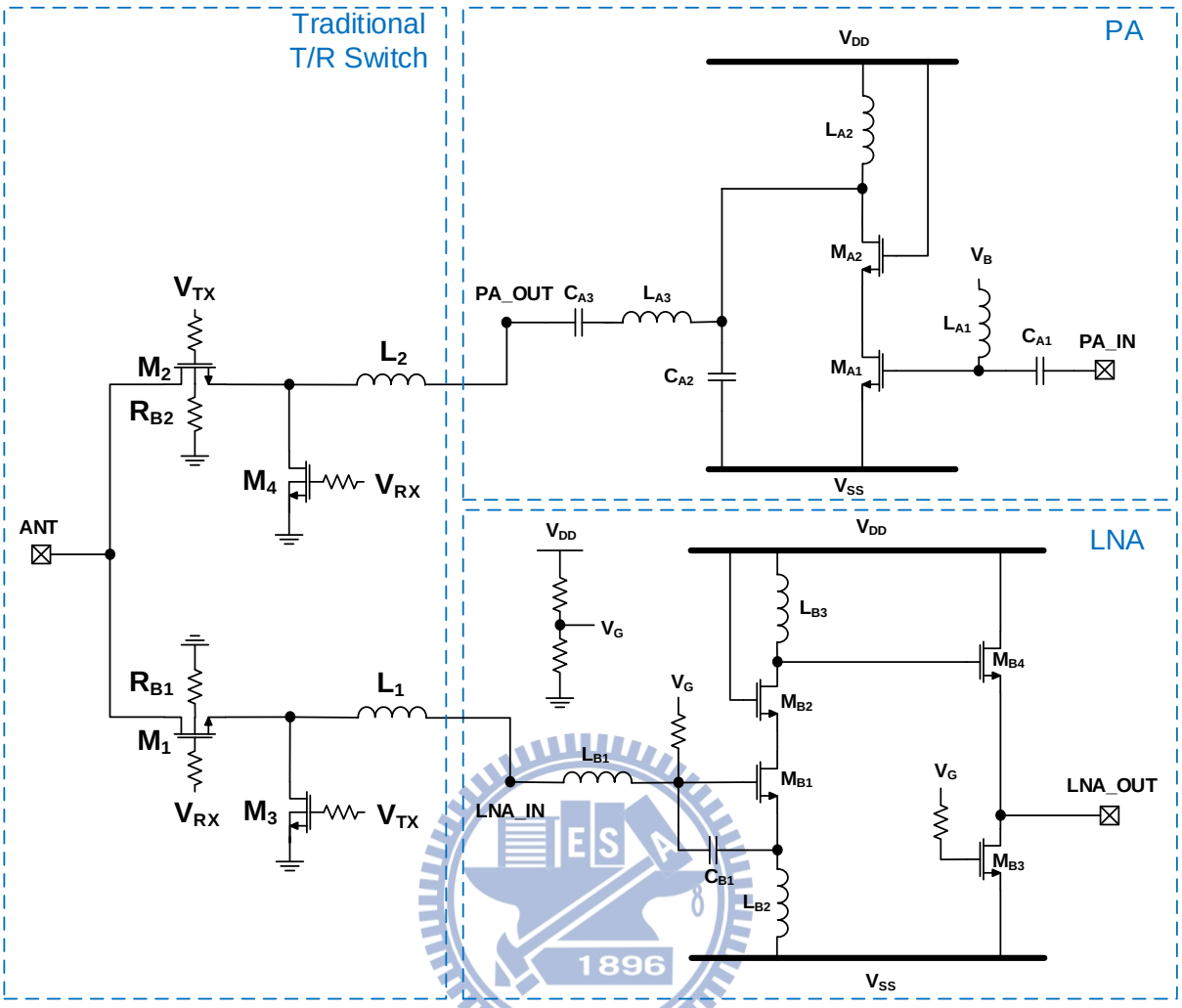



Fig. 4.2. Circuit schematic of traditional T/R switch front-end circuit.

## 4.2 Conventional ESD Protection Design for Traditional T/R Switch Front-End Circuit

The conventional ESD protection scheme for traditional T/R switch front-end circuit is shown in Fig. 4.3. Two ESD protection devices ($D_{P1}$ and $D_{N1}$) are put at ANT pad. The Fig. 4.3 shows the ESD discharge paths for the four different ESD testing modes. As mention in section 3.2, although the conventional ESD protection design with dual diodes can protect core circuit from ESD stress, the caused parasitic capacitances from ESD protection devices degrade the RF performance.

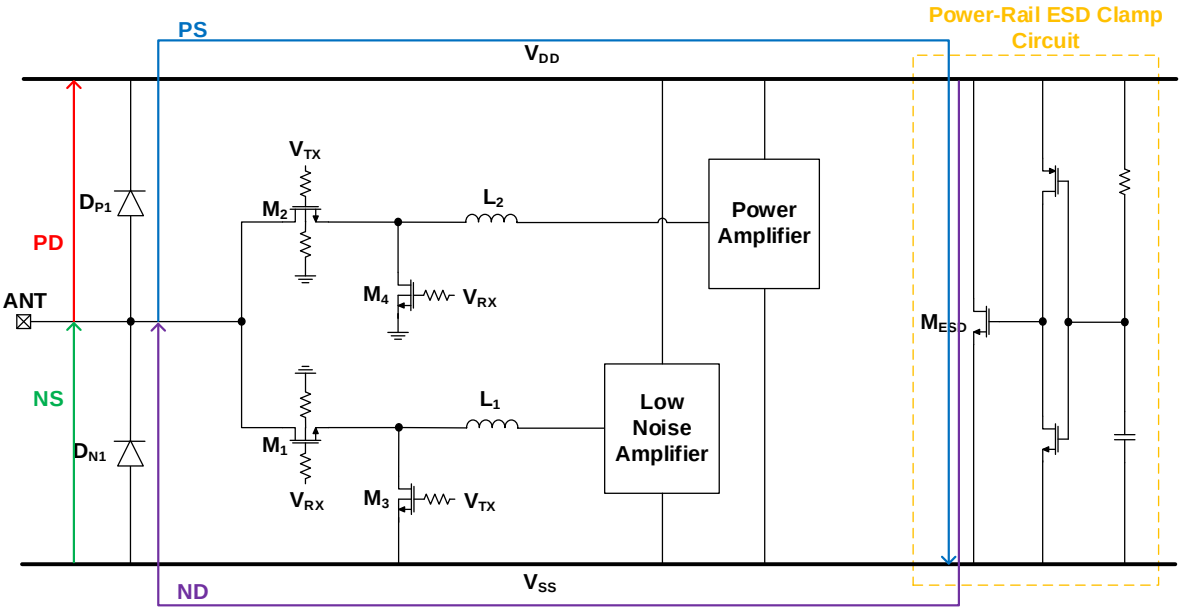



Fig. 4.3. The traditional T/R switch front-end circuit with conventional ESD protection design of dual diodes.

## 4.3 Proposed ESD Protection Design for Traditional T/R Switch Front-End Circuit

The cross-sectional view and the top view of the proposed T/R switch with embedded silicon controlled rectifiers (SCRs), which called type A, are illustrated in Figs. 4.4 to 4.7. The traditional T/R switch is implemented using NMOS transistors with deep N-well to separate the bulks of the NMOS transistors from P-substrate. In this proposed work, P+ is added in the N-well to form embedded SCR, which consists of P+, N-well, P-well, and N+. In the embedded SCR, the ANT pad is connected to the pickup P+, which is formed in the N-well. The $V_{SS}$ pad is connected to the N+ and the pickup P+, which respectively are the transistor ($M_3$ or $M_4$) source and bulk in the same P-well. The parasitic diode $D_1$ consists of P+ and N-well/N+ between ANT pad and $V_{DD}$. The extra ESD protection diode $D_2$ consists of P+/P-well and N+ between ANT pad and $V_{SS}$.

The SCRs are embedded in the traditional T/R switch. All the junction dimensions of

embedded SCR are also shown in Fig. 4.4 and Fig. 4.6. The length of the junction A is 0.94μm and that of the junction B is 0.64μm. The distance of the junction C from the anode of the embedded SCR to the bulk of shunt MOS is 2.7μm. The distance of the embedded SCR path (W) from anode to cathode is 4.56μm.

Fig. 4.8 shows the equivalent circuit of the T/R switch with embedded SCRs in TX path and RX path. To reduce the trigger voltage of the embedded SCRs, the trigger signal can be sent into the base terminal of $Q_{NPN}$ to enhance the turn-on speed. Furthermore, the trigger circuit, which is used to trigger embedded SCRs, is the RC-base detection circuit, which is used in the power-rail ESD clamp circuit.

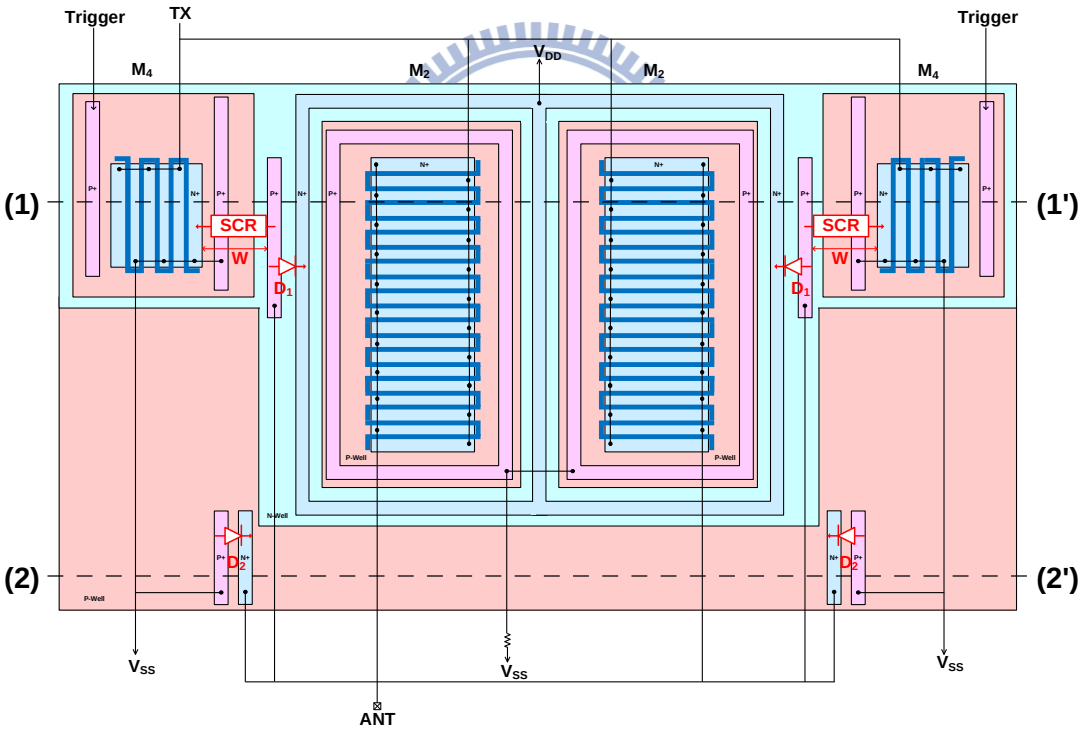
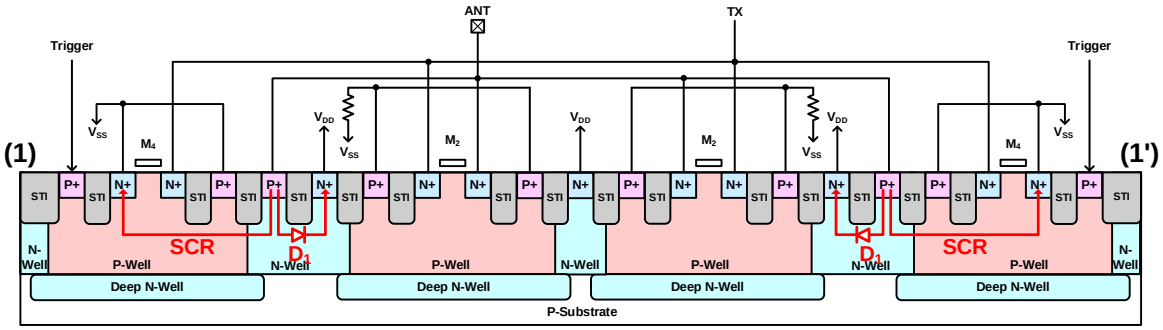
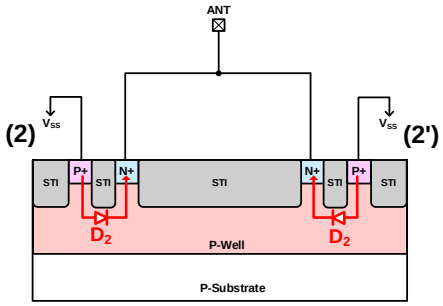



Fig. 4.4. Layout top view of traditional T/R switch with type A ESD protection design in TX path.




(a)




(b)

Fig. 4.5. Cross-sectional view of traditional T/R switch with type A ESD protection design along (a) (1)-(1') and (b) (2)-(2') in TX path.

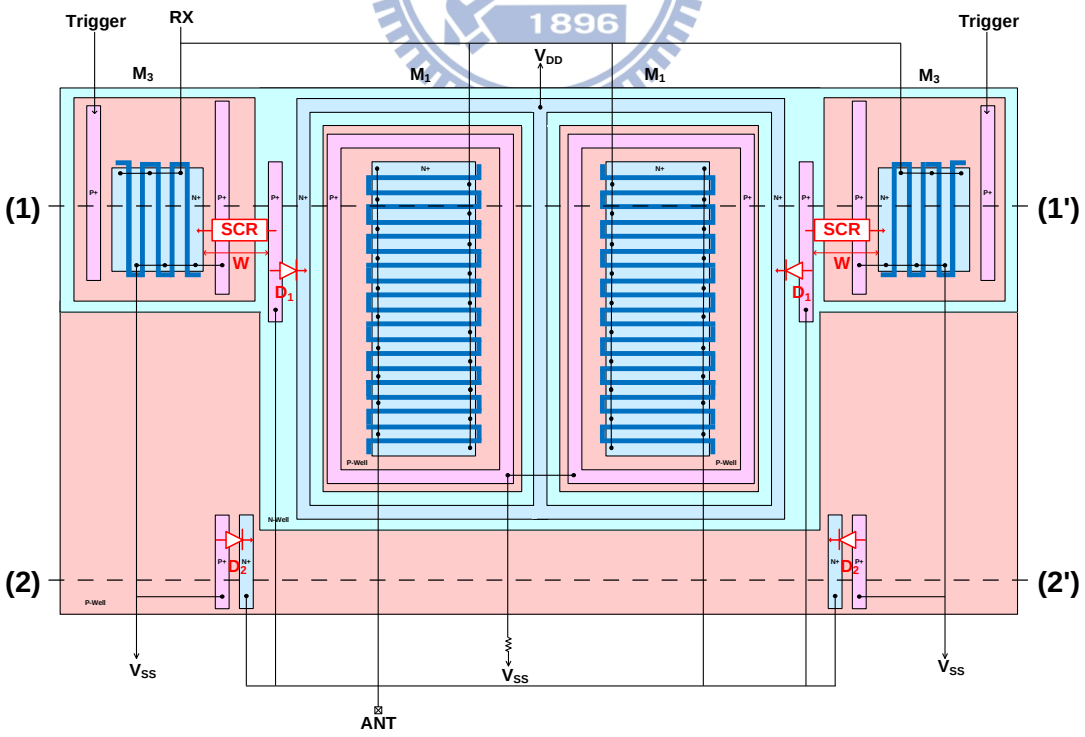
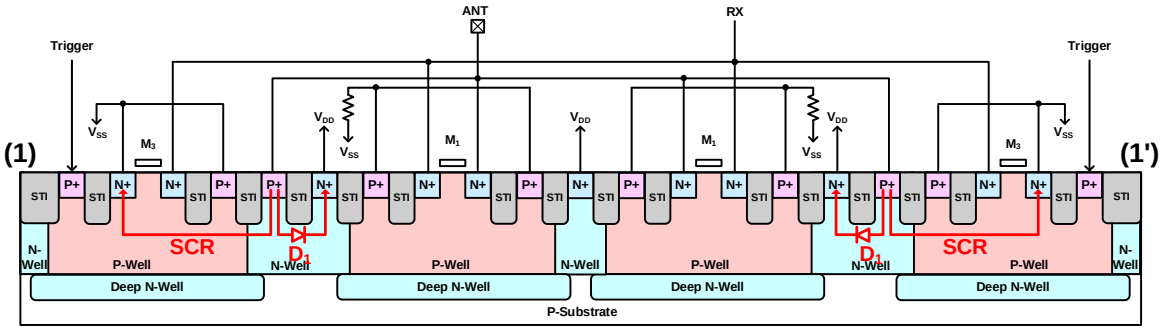
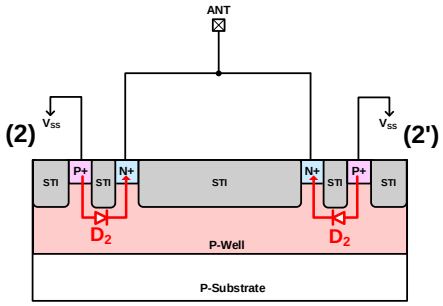



Fig. 4.6. Layout top view of traditional T/R switch with type A ESD protection design in RX path.




(a)




(b)

Fig. 4.7. Cross-sectional view of traditional T/R switch with type A ESD protection design along (a) (1)-(1') and (b) (2)-(2') in RX path.

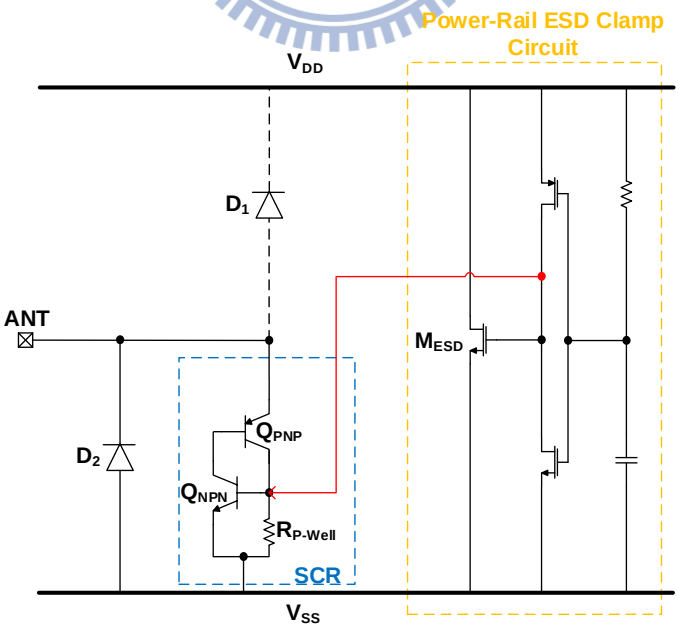



Fig. 4.8. The equivalent circuit of traditional T/R switch with type A ESD protection design.

Fig. 4.9 indicates the traditional T/R switch front-end circuit with type A ESD protection design and shows the ESD discharge paths for the four different ESD testing modes. For positive-to-$V_{DD}$ (PD) mode, the ESD current is discharged through the $D_1$. For positive-to-$V_{SS}$ (PS) mode, the ESD current first passes through the $D_1$ to $V_{DD}$ and then RC-inverter to trigger the embedded SCRs. The major ESD current is discharged by the embedded SCRs from ANT pad to $V_{SS}$. Therefore, the ESD protection ability can be significantly improved. For Negative-to-$V_{DD}$ (ND) mode, the ESD current is first discharged from $V_{DD}$ to $V_{SS}$ through the power-rail ESD clamp circuit and then it goes through the $D_2$. For Negative-to-$V_{SS}$ (NS) mode, the ESD current is discharged through the $D_2$.

Comparing with the conventional ESD protection design, the type A ESD protection design provides the whole chip ESD protection for all ESD-test with only adding ESD protection diode $D_2$. The embedded SCRs structure with RC-inverter-triggered shorten the ESD current path in the PS-mode. In conclusion, the proposed type A structure can not only reduce the impacts of ESD protection devices on RF performance but also improve the ESD robustness. The corresponding device parameters in traditional T/R switch circuits are organized in Table 4.1.

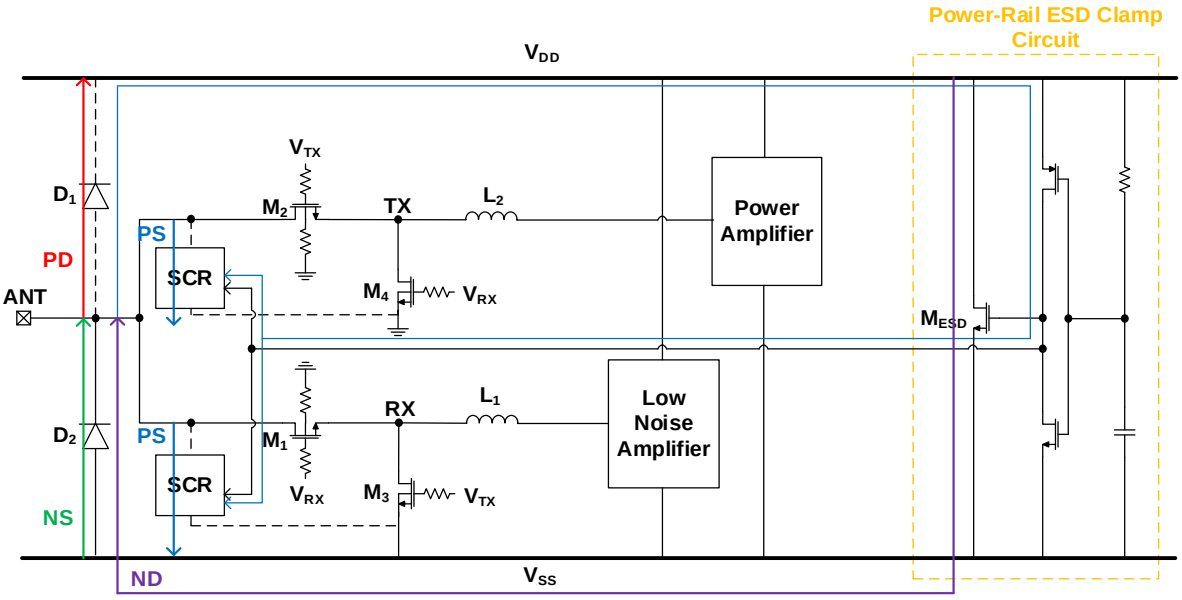



Fig. 4.9. The traditional T/R switch front-end circuit with type A ESD protection design.

Table 4.1
Component values and device dimensions of the traditional T/R switch circuits.

| | **Without ESD Protection Design** | **Conventional ESD Protection Design** | **Type A ESD Protection Design** |
|---|---|---|---|
| **Active Area of ESD Diode ($D_P/D_N$) ($\mu m^2$)** | N/A | 37.6 / 37.6 | N/A |
| **M1 W/L (μm/μm)** | 200/0.18 | 200/0.18 | 200/0.18 |
| **M2 W/L (μm/μm)** | 200/0.18 | 200/0.18 | 200/0.18 |
| **M3 W/L (μm/μm)** | 50/0.18 | 50/0.18 | 50/0.18 |
| **M4 W/L (μm/μm)** | 50/0.18 | 50/0.18 | 50/0.18 |

## 4.4 Post-Simulation Results

Fig. 4.10 shows the layout of traditional T/R switch front-end circuit without ESD protection design. Fig. 4.11 shows the layout of traditional T/R switch front-end circuit with conventional ESD protection design. Fig. 4.12 shows layout of traditional T/R switch front-end circuit with proposed type A ESD protection design, and Fig. 4.13 shows the layout of type A ESD protection design.

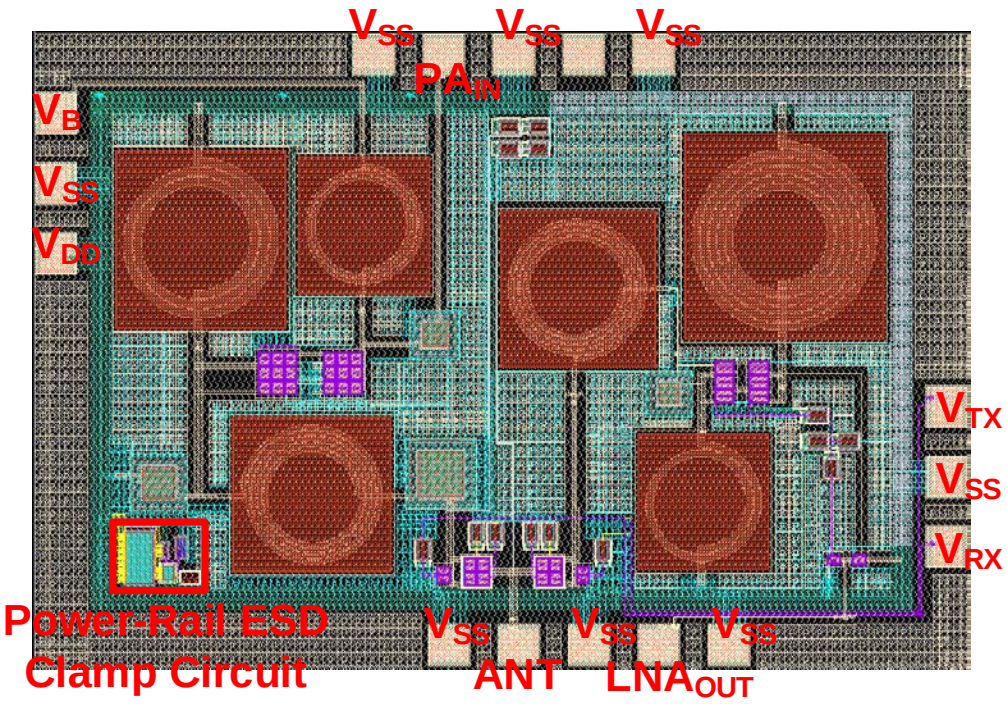



Fig. 4.10. Layout of traditional T/R switch front-end circuit without ESD protection design.

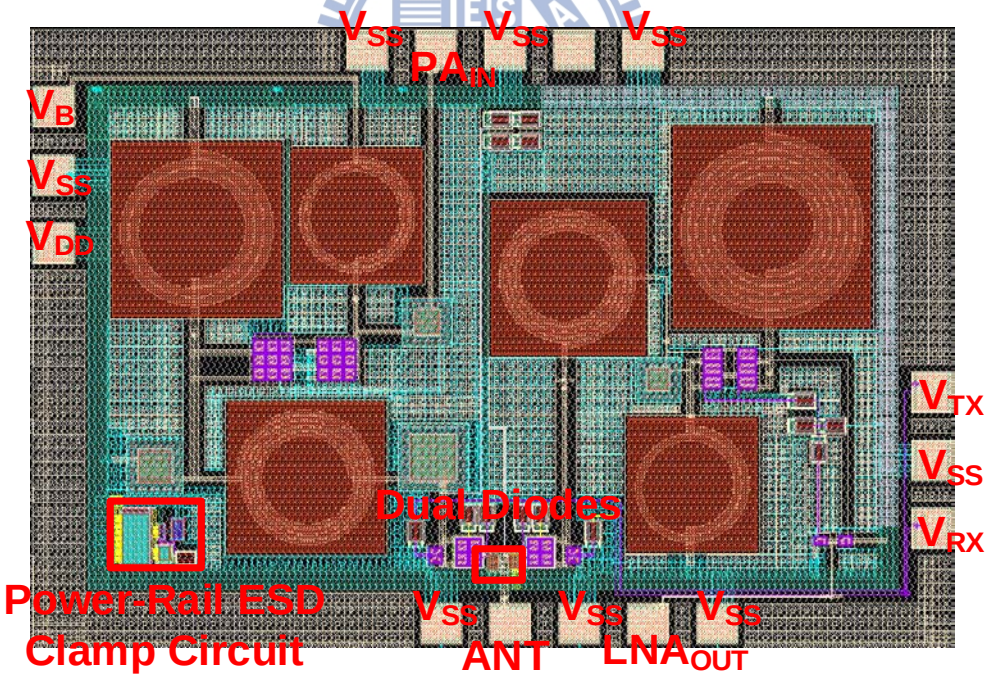



Fig. 4.11. Layout of traditional T/R switch front-end circuit with conventional ESD protection design.

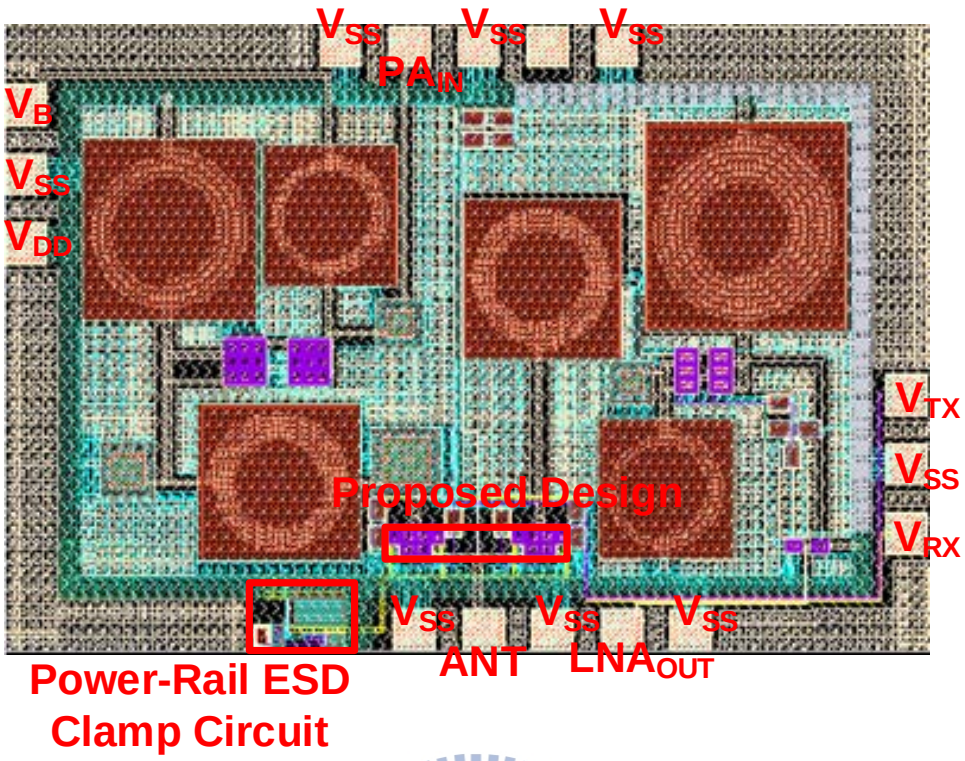
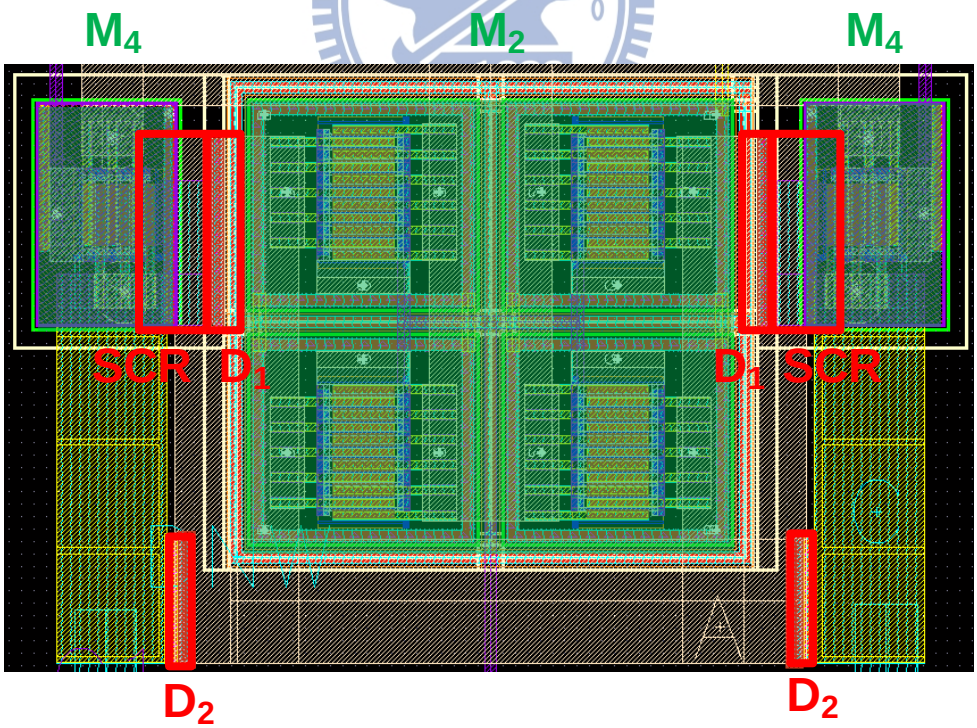
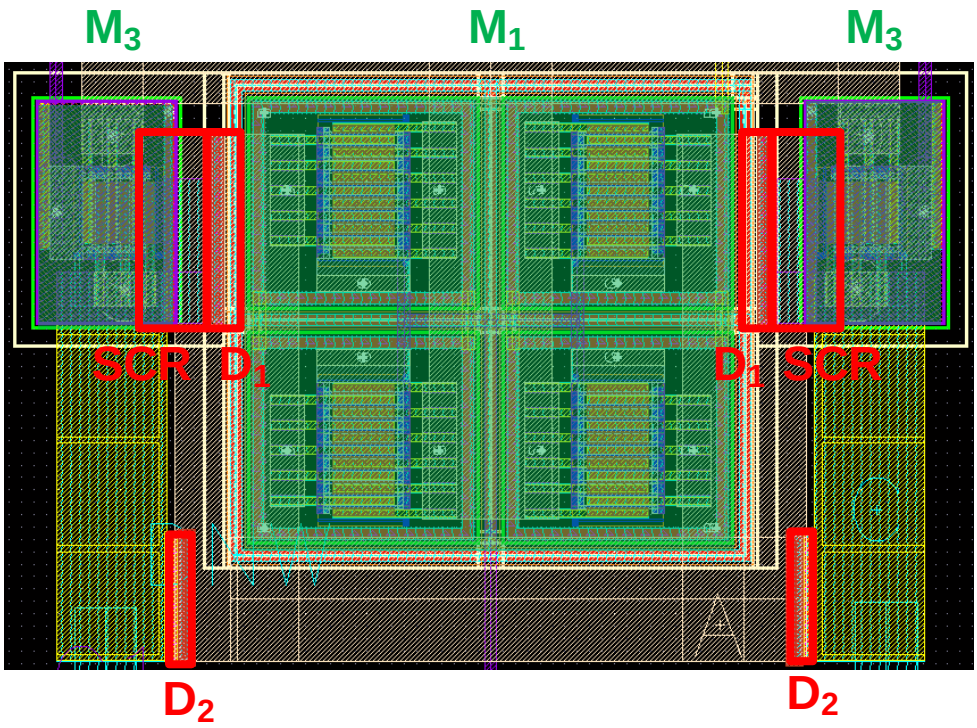



Fig. 4.12. Layout of traditional T/R switch front-end circuit with type A ESD protection design.



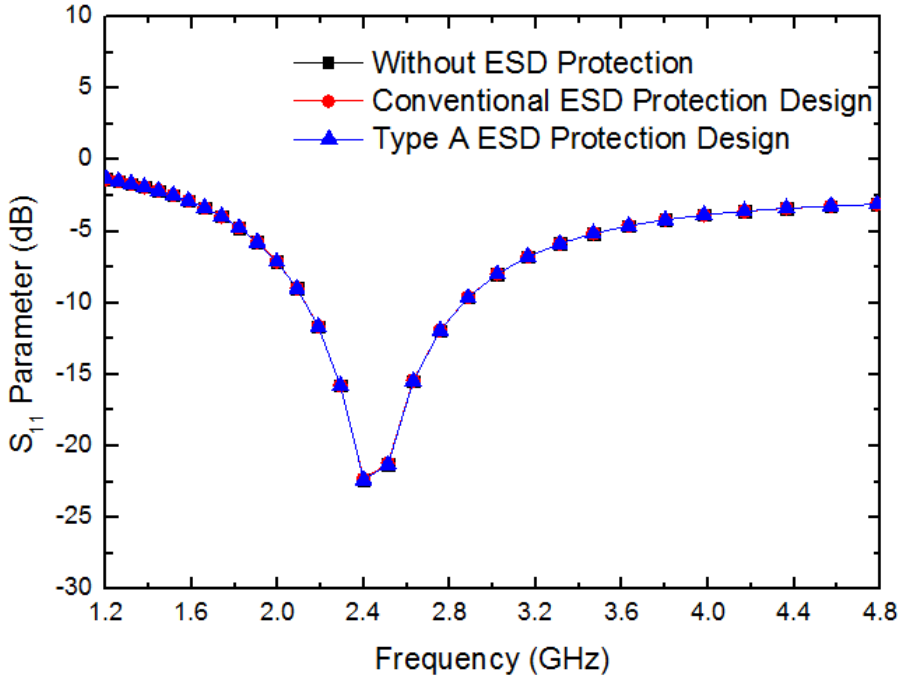

(a)



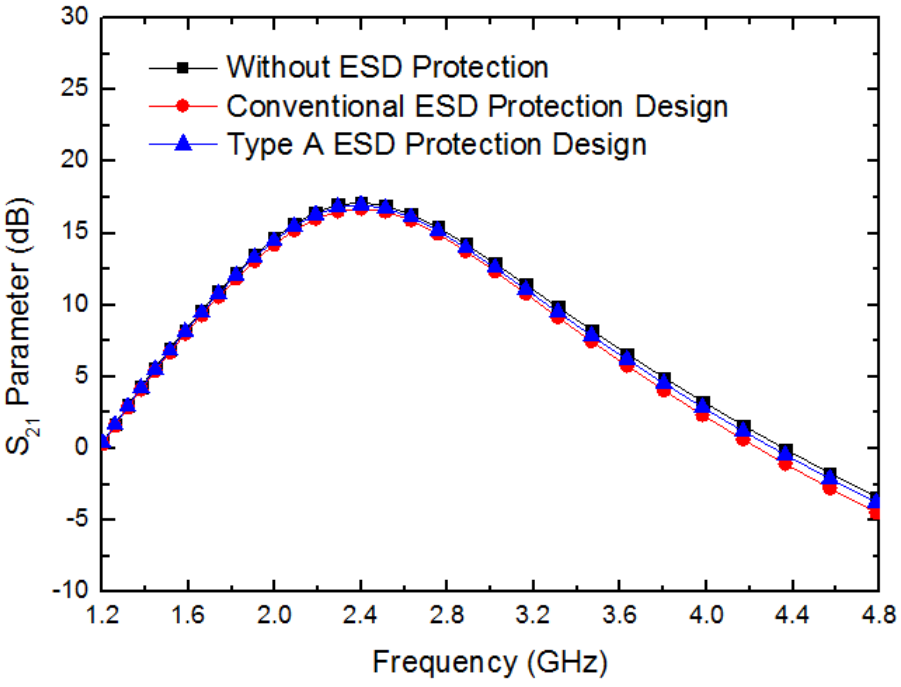

(b)

Fig. 4.13. Layout of traditional T/R switch with type A ESD protection design (a) in TX path and (b) in RX path.

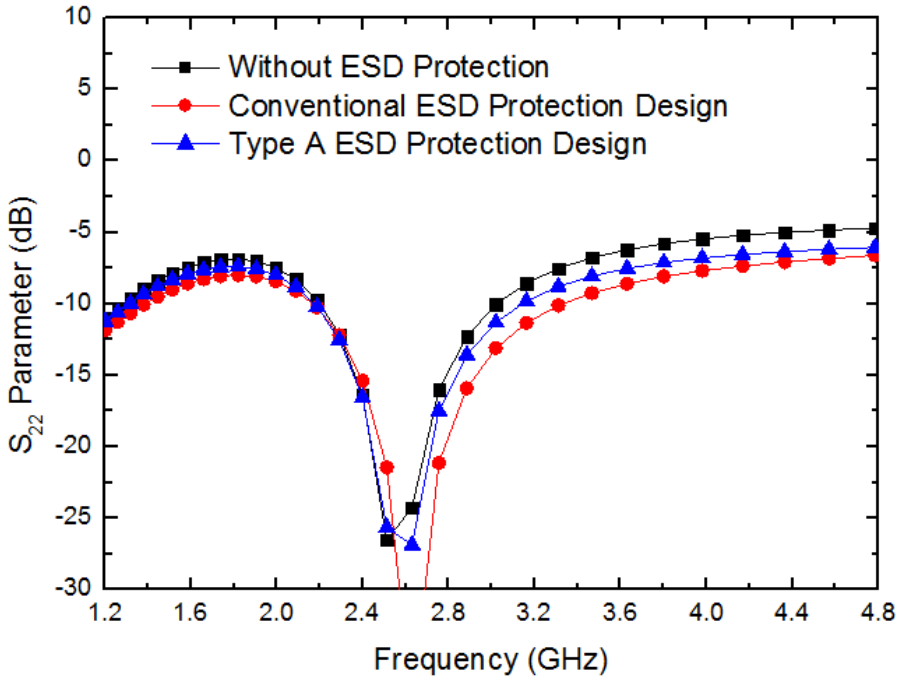
The post-simulation results of traditional T/R switch front-end circuits, which is operated at 2.4GHz, are presented in this section. It is realized in 180-nm 1P6M CMOS process with 1.8V supply voltage, 0.9V bias voltage, and controlled voltages (0V or 1.8V). The post-simulation results are illustrated in Figs. 4.14 to 4.18. In the TX mode, Fig. 4.14 shows comparison of the simulated $S_{11}$, $S_{21}$, and $S_{22}$ parameters. Fig. 4.15 and Fig. 4.16 show comparison of the simulated output power ($P_{OUT}$) and power gain versus input power ($P_{IN}$), respectively. In the RX mode, Fig. 4.17 shows comparison of the simulated $S_{11}$, $S_{21}$, and $S_{22}$ parameters. Fig. 4.18 shows comparison of the simulated noise figure.


Without ESD Protection
Conventional ESD Protection Design
Type A ESD Protection Design
S11 Parameter (dB)
Frequency (GHz)
10
5
0
-5
-10
-15
-20
-25
-30
1.2
1.6
2.0
2.4
2.8
3.2
3.6
4.0
4.4
4.8

(a)


Without ESD Protection
Conventional ESD Protection Design
Type A ESD Protection Design
S21 Parameter (dB)
Frequency (GHz)
30
25
20
15
10
5
0
-5
-10
1.2
1.6
2.0
2.4
2.8
3.2
3.6
4.0
4.4
4.8

(b)




(c)

Fig. 4.14. Comparison of simulated (a) $S_{11}$, (b) $S_{21}$, and (c) $S_{22}$ of the traditional T/R switch front-end circuits with and without ESD protection design in TX mode.

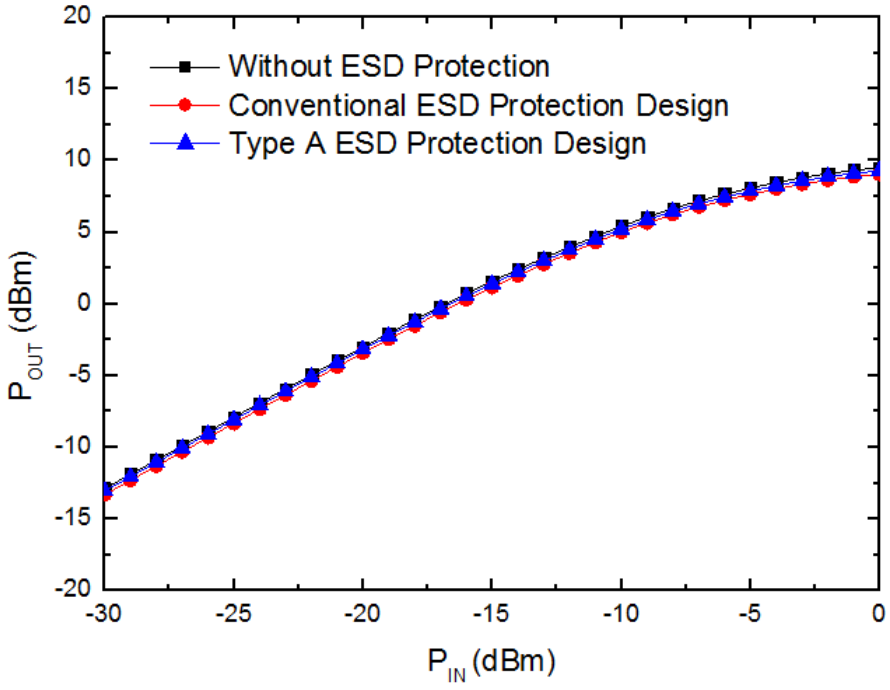



Fig. 4.15. Comparison of simulated output power of the traditional T/R switch front-end circuits with and without ESD protection design in TX mode.

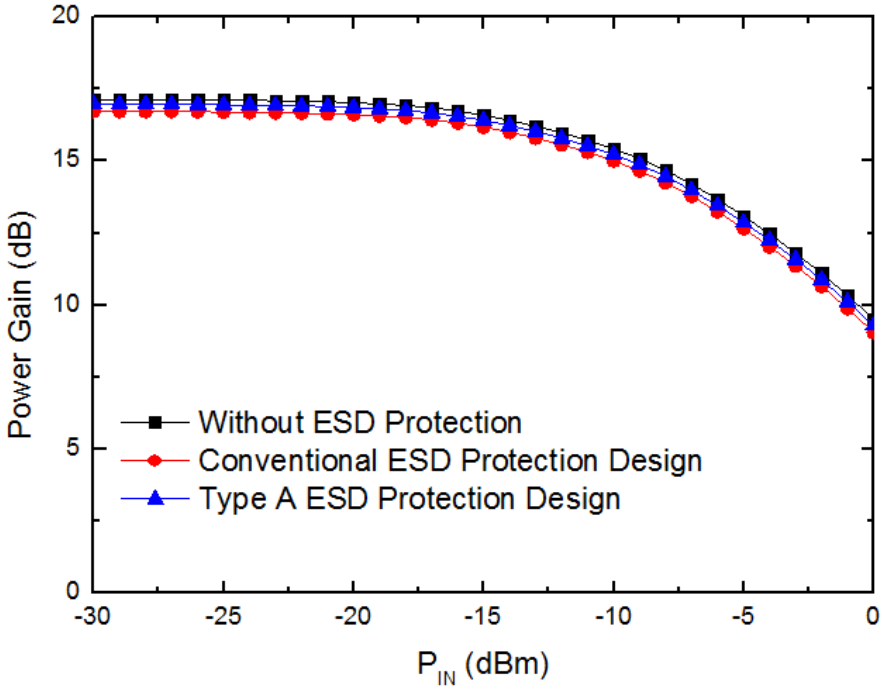
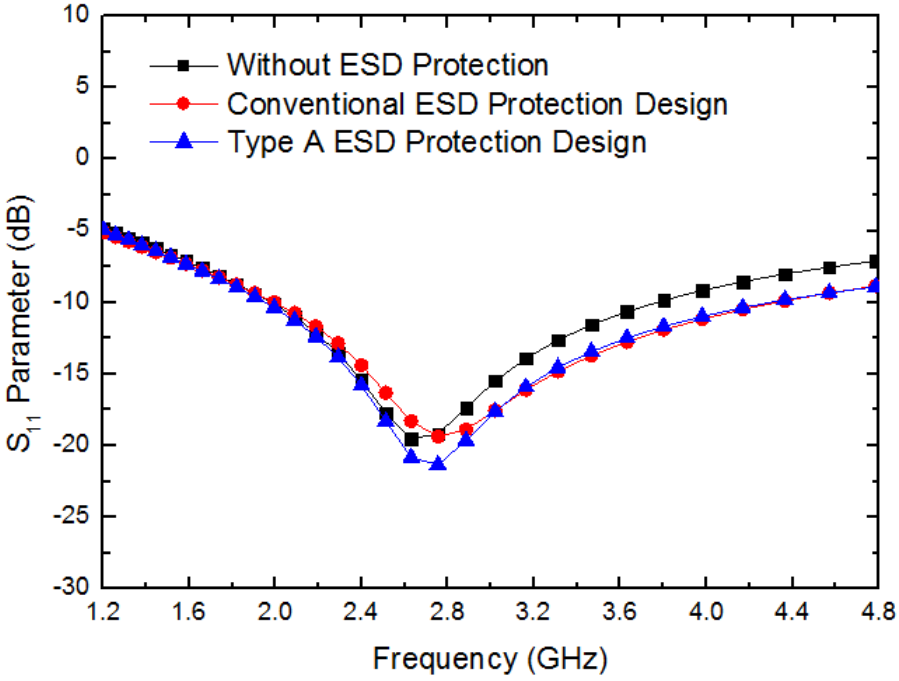
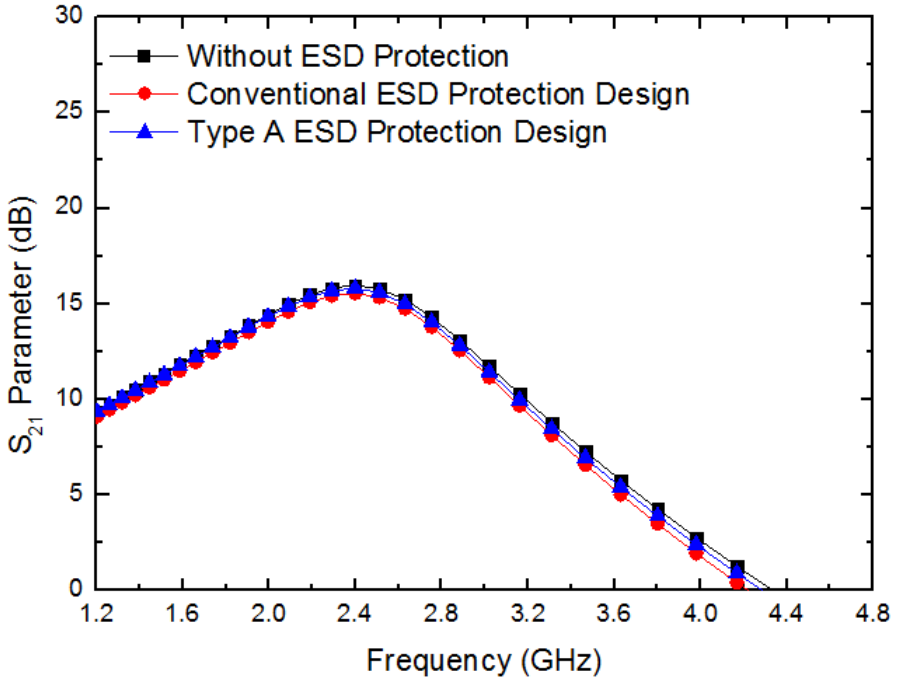


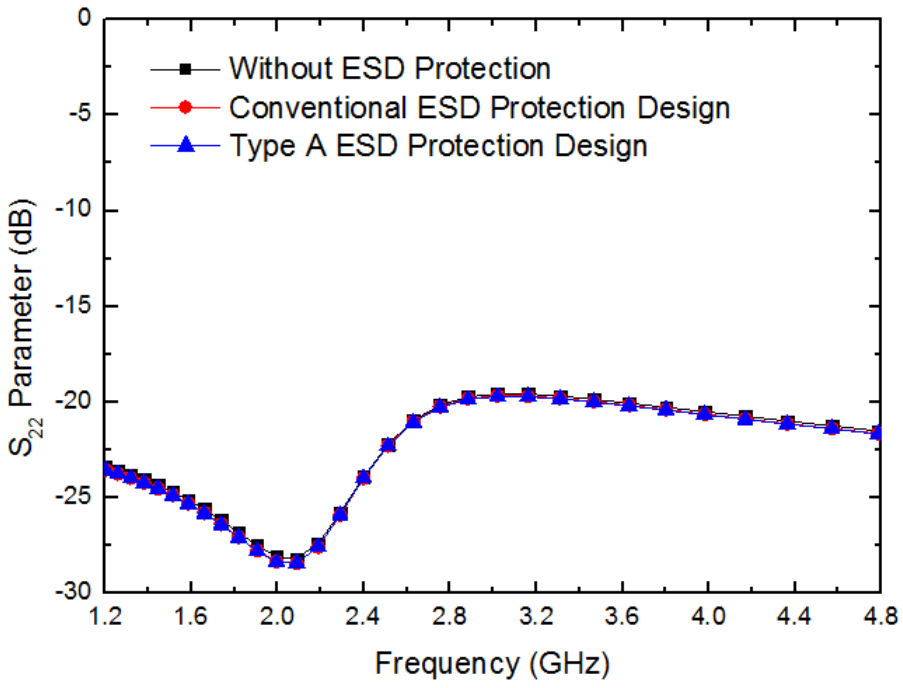

Fig. 4.16. Comparison of simulated power gain of the traditional T/R switch front-end circuits with and without ESD protection design in TX mode.




(a)




(b)




(c)

Fig. 4.17. Comparison of simulated (a) $S_{11}$, (b) $S_{21}$, and (c) $S_{22}$ of the traditional T/R switch front-end circuits with and without ESD protection design in RX mode.

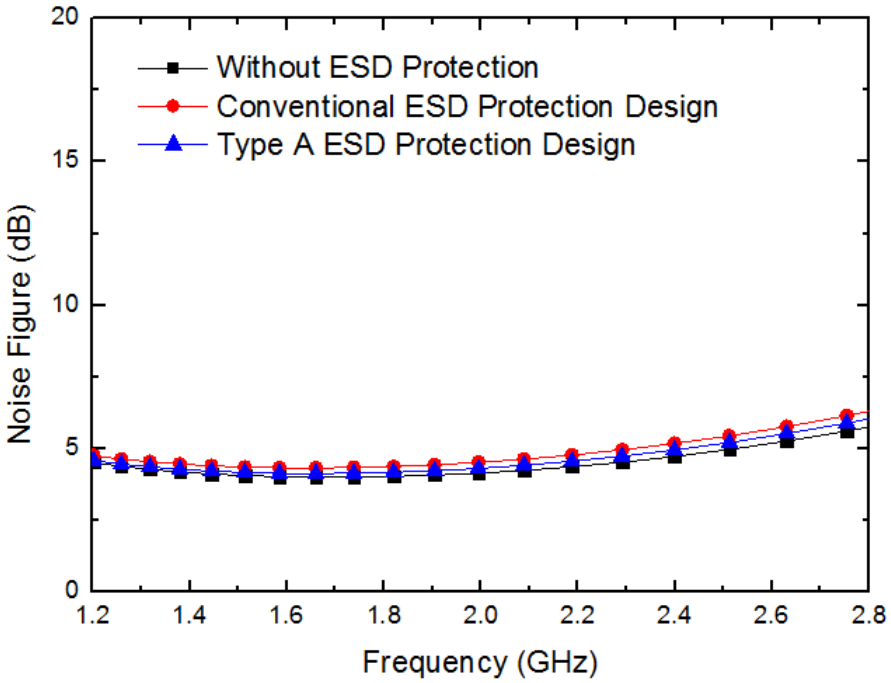



Fig. 4.18. Comparison of noise figure of the traditional T/R switch front-end circuits with and without ESD protection design in RX mode.

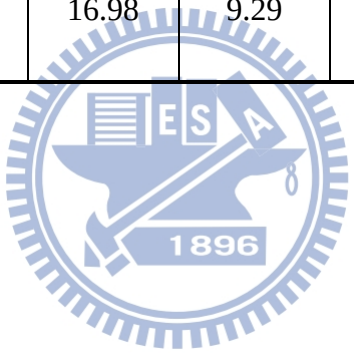
## 4.5 Summary

The proposed type A ESD protection design uses the embedded SCR into T/R switch. Without extra trigger circuit, the used RC-base detection circuit, which is the same with power-rail ESD clamp circuit, can sent trigger signal to enhance the turn-on speed. This design is used in traditional T/R switch front-end circuit. The $S_{21}$ parameters of un-protected circuit and ESD-protected circuits are compared in Table 4.2. The type A ESD design reduces the S21 about 0.18dB in TX mode and 0.2dB in RX mode, while the dual diodes reduces the S21 about 0.41dB in TX mode and 0.42dB in RX mode.

The embedded SCRs structure with RC-inverter-triggered can shorten the ESD current path in the PS-mode and improve ESD level. Therefore, the type A structure can reduce the impacts of ESD protection devices on RF performance and be suitable for on-chip ESD protection T/R switch front-end circuit.

Table 4.2
Comparison of simulation results of the un-protected T/R switch front-end circuit and the ESD-protected T/R switch front-end circuits.

| Structure | Active Area of ESD Diode ($D_P/D_N$) ($\mu m^2$) | TX mode | | | RX mode | |
|---|---|---|---|---|---|---|
| | | S21 @ 2.4GHz (dB) | Pout (dBm) | Power Gain (dB) | S21 @ 2.4GHz (dB) | NF @ 2.4GHz (dB) |
| **Without ESD Protection Design** | N/A | 17.16 | 9.51 | 17.15 | 16 | 4.73 |
| **Conventional ESD Protection Design** | 37.6 / 37.6 | 16.75 | 9.05 | 16.72 | 15.58 | 5.18 |
| **Type A ESD Protection Design** | N/A / 37.6 | 16.98 | 9.29 | 16.98 | 15.8 | 4.96 |



# Chapter 5
# Conclusions and Future Works

## 5.1 Conclusions

This thesis presents the issues of ESD protection design in RFICs. The parasitic effect of the ESD protection design causes signal loss, changes the impedance matching, and degrades RF performance. Therefore, designing RF ESD protection devices or circuits with good ESD level and less influence on RF performance has become a challenge. The RF ESD protection designs integrated with T/R switch are proposed to accomplish this goal.

The T/R switch front-end circuit plays an important role in RF transceiver. However, the ESD protection designs applied in T/R switch have not been widely investigated and discussed. Two RF ESD protection designs are integrated with T/R switch and applied in ESD-protected T/R switch front-end circuits, which have been proposed, fabricated, and examined in a 180-nm CMOS process. The proposed type 1 ESD protection design utilizes stacked diodes, which are embedded diode of switching MOS and ESD protection diode. The parasitic capacitances of ESD protection diodes seen at ANT pad are reduced. Without extra ESD protection device, the proposed type 2 ESD protection design utilizes stacked diodes, which are embedded in T/R switch.

The measurement results show that the un-protected T/R switch front-end circuit has terrible ESD level, while the T/R switch front-end circuit with proposed type 2 ESD protection design has enough ESD level. The failure mechanism indicates that the failed function of T/R switch front-end circuit after HBM ESD zapping is caused by the damaged proposed ESD

protection design. The proposed type 2 ESD protection design has been verified to protect the T/R switch front-end circuit from ESD damage with 1.5-kV HBM ESD robustness.

For traditional T/R switch front-end circuit, the ESD protection solution design is also presented in this thesis. The proposed type A ESD protection design is traditional T/R switch with embedded silicon controlled rectifiers (SCRs). The embedded SCRs structure with RC-inverter-triggered can shorten the ESD current path in the PS-mode and improve the ESD level. According to simulation results, the proposed type A ESD protection design has smaller parasitic effect because of lass extra ESD protection device. Comparing with conventional ESD protection design, the type A ESD protection design can reduce the impacts of ESD protection devices on RF performance and be suitable for traditional T/R switch front-end circuit.

## 5.2 Future Works

### *5.2.1 ESD Protection Designs for Traditional T/R Switch Front-End Circuits*

The traditional T/R switch front-end circuits with and without ESD protection designs have already been taped out and they are fabricated in 180-nm CMOS process. To evaluate the ESD robustness, HBM ESD levels (PS-mode, PD-mode, NS-mode, and ND-mode) need to be measured. In order to verify the ability of ESD protection design, the RF performances of all traditional T/R switch front-end circuits have to be measured before and after HBM ESD zapping with every mode (PS-mode, PD-mode, NS-mode, and ND-mode). In the TX mode, S-parameters ($S_{11}$, $S_{21}$, and $S_{22}$), output power, and power gain need to be measured. In the RX mode, S-parameters ($S_{11}$, $S_{21}$, and $S_{22}$) and noise figure need to be measured.

### *5.2.2 ESD Protection Design for SPMT T/R Switch*

The proposed ESD protection design is for single-pole double-through transmit/receive switch (SPDT T/R switch). Recently, the single-pole multiple-through transmit/receive switch

(SPMT T/R switch), as shown in Fig. 5.1, is more widely used in IC products such as multiple-band smartphones. However, the SPMT T/R switch has many channels and operates at different frequency in each channel. Thus, it is not easy to design matching network with ESD protection design. The proposed on-chip ESD protection may need some modification for application in the SPMT T/R switch.

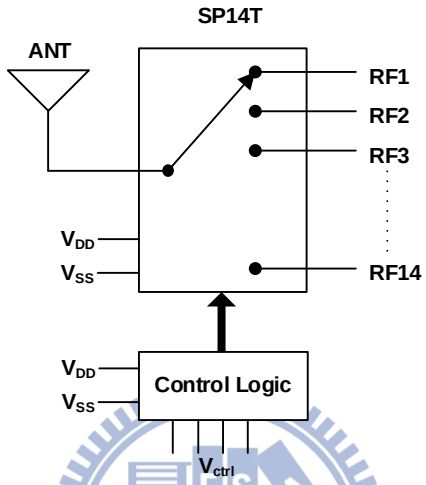



Fig. 5.1. Schematic of SPMT T/R switch [24].

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