國立交通大學

電子研究所

碩　士　論　文

低電壓觸發矽控整流器
在靜電放電防護上的設計與應用

Design of Low-Voltage-Trigger SCR for ESD Protection in 28nm CMOS Process

研 究 生：吳易翰　　(Yi-Han Wu)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國一○五年十月

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摘要

近年半導體製程的發展和製程微縮的發展趨勢下，達到了更低的功率消耗，更高的操作效率及更佳的積體電路整合能力，也微縮了閘極氧化層(Gate oxide, GOX)和通道長度，但元件微縮進入奈米製程後，卻意味著會導致其靜電防護能力的下降，也間接的造成電子產品可靠度上的不穩定性，此外薄閘極氧化層也擁有低崩潰電壓之特性，使得先進製程之靜電放電防護設計更具有挑戰性。

由於在先進製程中單位面積的製程成本非常昂貴，因此增加佈局面積意味著同時增加高額的晶片製造成本，這使得佔用大面積的靜電放電防護電路變得更加昂貴，因此如何設計出低佈局面積並同時具有良好的 ESD 耐受度之靜電放電防護元件，為本論文之主要研究主題。

在典型全晶片靜電放電防護設計架構之中能夠在靜電放電轟擊時，提供有效的電流放電路徑，但在先進製程之下對於典型全晶片靜電放電防護設計架構 Negative to VDD mode (ND mode)和 Positive to VSS mode (PS mode)是較薄弱的放

電路徑，其靜電放電耐受能力主要由電源端與接地端的靜電放電箝制電路所決定，因此，在本論文的第二章提出了新架構的輸入輸出介面的靜電防護元件，利用 PMOS/NMOS 的結構和 Dummy Gate 的方式將傳統的矽控整流器(Silicon-Controlled Rectifier, SCR)加以改良，為了達到快速放電與改善低漏電的目的，利用閘極控制的方式使新設計的 SCR 元件擁有更低的觸發電壓(Trigger voltage, Vt1)，同時利用 Dummy gate 的方式避免了淺溝槽隔離（Shallow trench isolation, STI)結構在元件中放電路徑中形成阻礙，此外使新元件結構同時擁有寄生二極體和寄生矽控整流器的放電路徑，使其更有效的應用於全晶片靜電放電防護設計架構之中，並且同時改善了典型 ND mode 和典型 PS mode 必須透過電源端與接地端的靜電放電箝制電路的缺點。以上研究在 28 奈米的高介電係數/金屬閘極製程下實現。

除了於第二章提出的新型輸入輸出介面靜電防護元件，本論文第三章，將新型元件結構加以改良使其得以應用於電源端與接地端的靜電放電箝制電路，為了能有更好的靜電耐受度與更低的觸發電壓與更快的導通速度，也利用 Silicide Blocking (SAB)的方式來提升元件均勻導通的能力與降低觸發電壓，達到元件最佳化的目的，並且搭配傳統靜電偵測電路，以利於達到低漏電，高 ESD 耐受度，快速導通速度的首要目的，其中也加入了傳統的矽控整流器(Silicon-Controlled Rectifier, SCR)元件和傳統基底觸發矽控整流器(Substrate-Trigger SCR, ST-SCR)進行一系列比較，其中除了優異的靜電耐受度包括人體靜電放電模型(Human-Body Model, HBM)及機器放電模型(Machine-Model, MM)、均勻導通、快速導通、大幅降低佈局面積之特性，同時也可免於栓鎖效應(Latch-up)的危險等優點，因此，此新型元件非常適合使用在製造成本高昂、閘極氧化層厚度越來越薄以及操作電壓越來越低的先進製程中作為靜電放電防護的元件，並於第四章提出未來可以將新元件應用於鰭式場效電晶體之結構。

Design of Low-Voltage-Trigger SCR for ESD Protection in 28nm CMOS Process

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Abstract

With advanced CMOS technology, CMOS devices have been fabricated with thinner gate oxide, and the operation ability of integrated circuits can attain to high speed and low power consumption. However, with the scaling of CMOS technologies, the ESD robustness decreases and the reliability of production is unstable. In addition, ESD protection is more challenge to overcome because thinner gate oxide are equipped with the characteristic of low breakdown voltage.

The layout area of advanced CMOS process would spend a huge cost. In other word, companies will spend a huge additional budget because the layout of ESD protection cells occupies large area. In this thesis, small layout area and decent ESD robustness are our targets to realize on our novel devices.

A typical whole chip ESD protection scheme forms Positive to VDD mode (PD mode), Negative to VDD mode (ND mode), Positive to VSS mode (PS mode) and Negative to VSS mode (NS mod) which modes are discharge paths. However, ND mode

and PS mode have relatively weak ability of ESD robustness, especially in advanced CMOS process. The ability of Power-rail ESD clamp circuits the main reason to influence ND and PS mode of ESD robustness. In chapter 2, we propose novel I/O ESD devices equipped with the advantage of low leakage and low trigger voltage. The I/O ESD devices are modified by Silicon-Controlled Rectifier (SCR). Meanwhile, we add the structure of PMOS/NMOS and dummy gate on our proposed I/O ESD devices. The advantage of gate-control method makes novel SCR devices have low trigger voltage (Vt1), while the benefit of attached dummy gate is Shallow Trench Isolation (STI) structure cannot form in our proposed devices. In addition, our proposed devices contain parasitic diode and parasitic SCR as discharge paths which can be usefully applied on whole chip ESD protection scheme. Moreover, the drawback of typical ND and PS mode are removed. From above all, our proposed design have been realized in 28-nm high-k/metal gate CMOS process.

In chapter 3, we modify the novel devices described in chapter 2 and its modified devices can be applied on Power Rail ESD clamp circuit. Moreover, modified devices with additional Silicide Blocking (SAB) area to acquire better ESD robustness, smaller trigger voltage and faster turn-on speed. Modified devices combing with ESD transient detection circuit can efficiently turn on while ESD phenomenon occurs.

We add traditional Silicon-Controlled Rectifier (SCR) and Substrate-Trigger SCR (ST-SCR) devices to compare with modified devices. Decent ESD robustness for HBM and MM, uniformly and fast trun-on, small layout area and the avert of latch-up risky are advantages for our modified devices in 28-nm CMOS process.

In chapter 4, we predict that our proposed devices can be realized on Fin-FET structures for future investigation.

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吳易翰

105 年 10 月於竹塹交大

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Chapter 1

Introduction

1.1 Introduction of ESD Protection

Nowadays, ESD current can cause integrated circuits destroyed and the reliability of production decreases. In advanced CMOS process, circuits can achieve higher speed, operate in low supply voltage and low power consumption, but short channel and thinner gate oxide (GOX) derive the characteristic of low breakdown voltage. Gate oxide (GOX) possessing the characteristic of low breakdown voltage would decrease the ESD protection reliability for CMOS Integrated circuit in advanced CMOS process.

In traditional ESD protection scheme, we usually design ESD protection between PAD and VSS rather than VDD, which cause unpredictable destruction.

Fig.1.1 is different from traditional ESD protection, which adds another IO ESD devices and power-rail ESD clamp circuit. The typical whole-chip ESD protection scheme designed with efficient VDD-to-VSS ESD clamp circuits is proposed to provide a real whole-chip ESD protection for internal circuits [1].

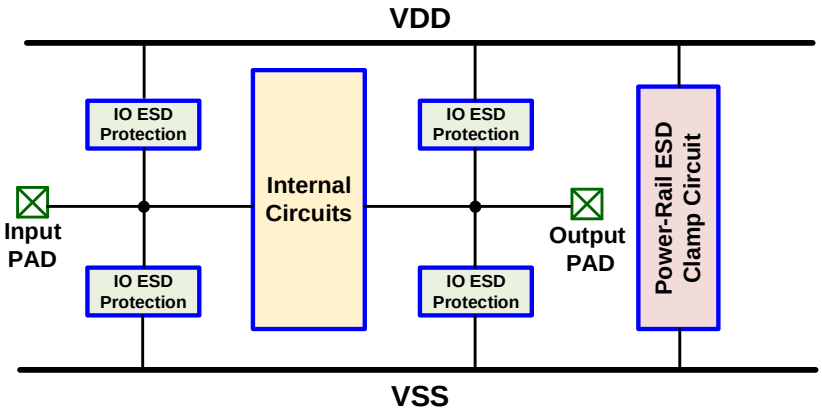


Fig. 1.1. The typical whole-chip ESD protection scheme.

ESD current can occur in several ways. A pulse from positive/negative voltage or internal circuits charge/discharge are possible reason to cause ESD damage. Adding two ESD protection device on I/O pad make the current flow out and avoid destruction for internal circuits. Power clamp ESD device between VDD and VSS would provide ESD discharge path and form the typical whole-chip ESD protection scheme.

There are four ESD current discharge Modes in the typical whole-chip ESD protection scheme. Fig.1.2 shows Positive to VDD mode (PD Mode) and Negative to VSS Mode (NS Mode). PD Mode is that input pad/output pad ESD current flow to VDD by diode Dp1/Dp2, while NS Mode is that input pad/output pad ESD current flow to VSS by diode Dn1/Dn2.

Fig.1.3 shows PS Mode and ND Mode. Positive to VSS mode (PS Mode) is that input pad/output pad ESD current flow to VSS by diode Dp1/Dp2 and power-rail ESD clamp circuit, while Negative to VDD Mode (ND Mode) is that input pad/output pad ESD current flow to VSS by diode Dn1/Dn2 and power-rail ESD clamp circuit.

From above ESD discharge modes, PS mode and ND mode would cause serious ESD damage for internal circuits if whole-chip ESD protection scheme do not have a well power rail ESD clamp circuit to discharge ESD current from VDD to VSS. Therefore, a well-optimized whole-chip ESD protection scheme is a crucial target to discharge current from VDD to VSS.

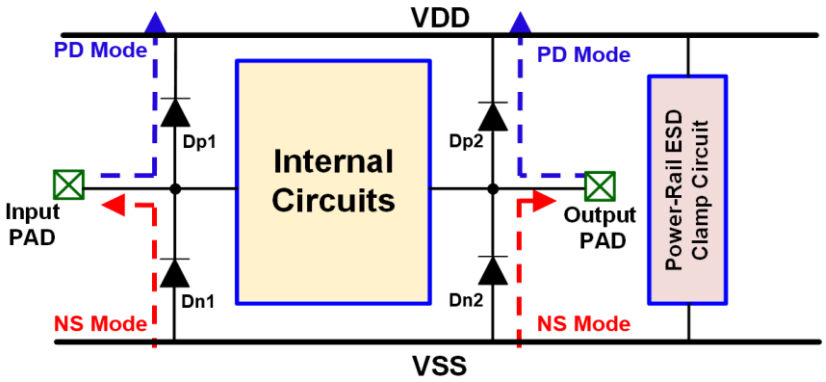


Fig. 1.2. Positive to VDD Mode (PD Mode) and Negative to VSS Mode (NS Mode).

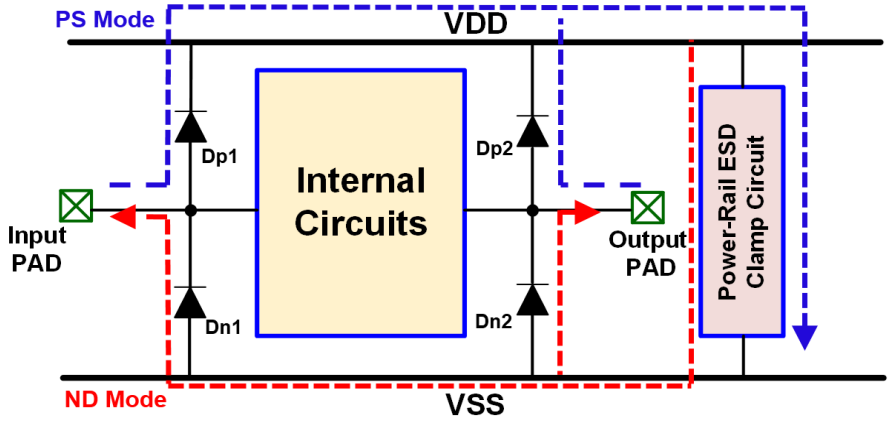


Fig.1.3. Positive to VSS Mode (PS Mode) and Negative to VDD Mode (ND Mode).

1.2 Introduction of ESD Test Models

In the ESD test models, various types of ESD damage affect different integrated circuit results. ESD test models are modeled as charged capacitor and equivalent resistor. Device under test (DUT) are measured by ESD test models. Three types of discharge mode are defined on standard measurement.

The Human-Body Model (HBM) is shown in Fig. 1.4. HBM is that human body accumulates charges from life behavior, causing a damage to chip when human touch the IC pins. Normally, the equivalent resistance of human body is equal to 1.5kΩ and its equivalent capacitance is roughly 100pF [2].

The Machine-Model (MM) is shown in Fig. 1.5. In the MM ESD test model, Machines store charges and discharge current when touching the IC pins is called Machine Model (MM). The value of equivalent resistance is 0Ω and capacitance is 200pF [3]. The discharge waveform of HBM and MM is shown in Fig. 1.6. MM is more influence to chip compared to HBM due to shorter discharge period and smaller equivalent resistor. HBM and MM Waveform Specification are listed in Table 1.1 [2]-[4].

The Charged-Device Model (CDM) is shown in Fig. 1.7. IC accumulates charges in internal circuit. When IC pins touch ground, current discharge to the ground. This

behavior defined as Charged-Device Model [5]. The value of equivalent capacitance and equivalent resistor is various because of external factors.

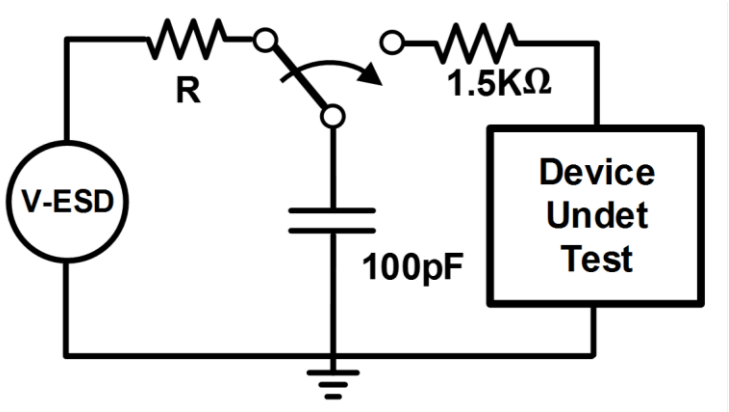


Fig. 1.4. Equivalent circuit of Human-Body Model (HBM) [2].

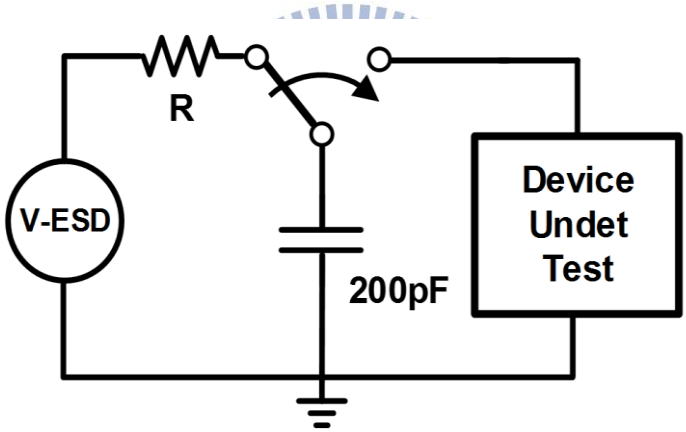


Fig. 1.5. Equivalent circuit of Machine-Model (MM) [3].

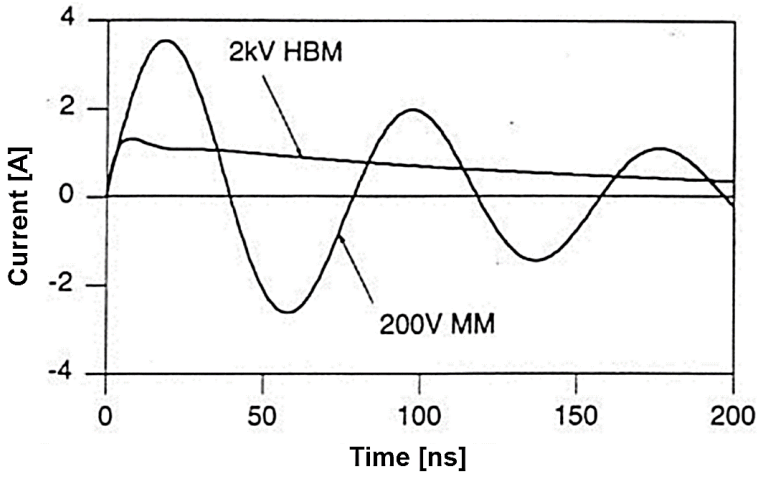


Fig. 1.6. The discharge waveform of HBM and MM [2]-[4].

Table 1.1 HBM and MM Waveform Specification [2]-[4].

HBM Voltage Level (V)	Current Peak for Short (A)
250	0.15 – 0.19
500	0.30 – 0.37
1000	0.60 – 0.74
2000	1.20 – 1.48
4000	2.40 – 2.96
8000	4.80 – 5.86
MM Voltage Level (V)	**Current Peak for Short (A)**
100	1.1– 2.0
200	2.8 – 3.8
400	5.8 – 8.0

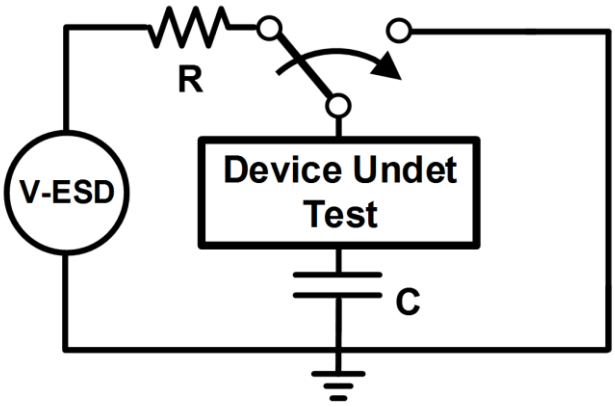


Fig. 1.7. Equivalent circuit of Charged-Device Model (CDM) [5].

1.3 Motivation

Diode, MOS device and silicon-controlled rectifier (SCR) device are mainstream in ESD protection devices. Under demanding of small area and low cost, SCR device is tendency in advanced process to achieve high ESD robustness and low parasitic capacitance in RF circuit. Though SCR device possess a decent ESD protection and small area, high trigger voltage is its disadvantage. Due to its disadvantage, parasitic SCR path cannot efficiently to be turn on. Therefore, references provide series methods to decrease the trigger voltage with different trigger mechanism. Those methods is to improve the SCR trigger voltage so that the intrinsic circuits can be protected by ESD protection [6]-[9].

The characteristic of I-V curve must locate at ESD protection design window range in order to guarantee ESD stability and efficiency. The ESD protection design window is shown in Fig. 1.8. Three ESD device characteristic of I-V curve parameters are discussed. First, Trigger Voltage (Vt1) must be lower than internal breakdown voltage (VBD, internal) so that internal circuits would not fail and be protected well by ESD protection circuit. In addition, holding voltage must higher than operation voltage avoiding internal circuit destroyed and latch-up mechanism. It2 is the second breakdown current and the best standard to assess ESD robustness. The higher It2 current is, the better ESD robustness. Besides, It2 can be determined the size of Ron from ESD device to assess the ESD robustness. ESD protection have a better ability when Ron is smaller [10].

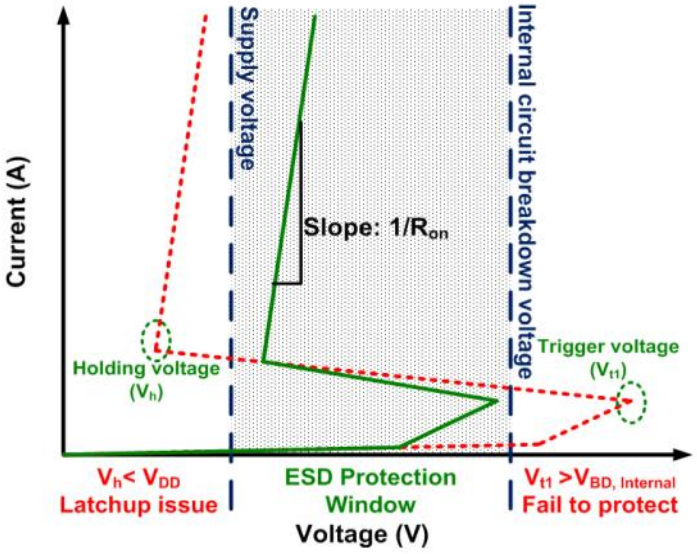


Fig. 1.8. The ESD protection design window [10].

1.4 Thesis Organization

The first chapter, chapter 1, includes the motivation of this work and research measurement methods.

Chapter 2 illustrates low-Leakage and low-Trigger-voltage SCR devices for I/O ESD Protection in 28-nm HKMG CMOS Process. Our proposed devices are realized under TSMC 28-nm HPM 0.9V / 2.5V process.

In chapter 3, our modified devices can be applied on power-rail ESD clamp circuit. Moreover, modified devices with additional Silicide Blocking (SAB) area acquire better ESD robustness, smaller trigger voltage and faster turn-on speed.

The last chapter, chapter 4, predicts that our proposed devices can be realized on Fin-FET structures for future investigation.

Chapter 2

Low-Leakage and Low-Trigger-Voltage SCR Device for I/O ESD Protection in 28-nm HKMG CMOS Process

2.1 introduction and Prior Art

The silicon-controlled rectifier (SCR) device has been reported to be useful for electrostatic discharge (ESD) protection in advanced CMOS process with low supply voltage and can be used without latch up concern [11],[12].However, the trigger voltage is one of the most essential design consideration for ESD protection in low-voltage CMOS process [13], [14]. Reducing the trigger voltage of SCR device is needed by efficient design.

The conventional SCR device in low-voltage CMOS process consists of P+, N-well, P-well, and N+. The cross-section view of conventional SCR is shown in Fig. 2.1. The equivalent circuit of the SCR compromise a p-n-p BJT (QPNP) and an n-p-n BJT (QNPN). As ESD zapping from anode to cathode, the positive-feedback regenerative mechanism of QPNP and QNPN results in the SCR device highly conductive to make SCR very robust against ESD stresses.

To reduce the trigger voltage of SCR device, several designs have been presented in advanced CMOS processes [15]-[21].

The inductor-assisted SCR device for high-frequency applications is designed to trigger at 5V, but its needs additional area of the inductor [15]. The direct-connected SCR device is designed with the same trigger voltage and holding voltage of 1.3V, but it needs additional deep N-well layer to isolate the P-well from the common P-substrate

[16]. The gate-bounded SCR devices are used dummy gate to shorten the distance between anode and cathode, but they need additional process steps to block the silicide to decrease the leakage current, or to form the scotty junction to increase the holding voltage [17]-[19]. The low-capacitance SCR device in silicon-on-insulator (SOI) CMOS process was designed to trigger at 8.1V [20].The SCR device in CMOS 32nm node was investigated [21], but it did not consider the parasitic capacitance.

The SCR device with low trigger voltage, low leakage current, low parasitic capacitance, and without additional process step for ESD protection is still requested. Therefore, a novel SCR device is proposed to meet the requirement and verified in a 28-nm high-k metal gate (HKMG) CMOS process.

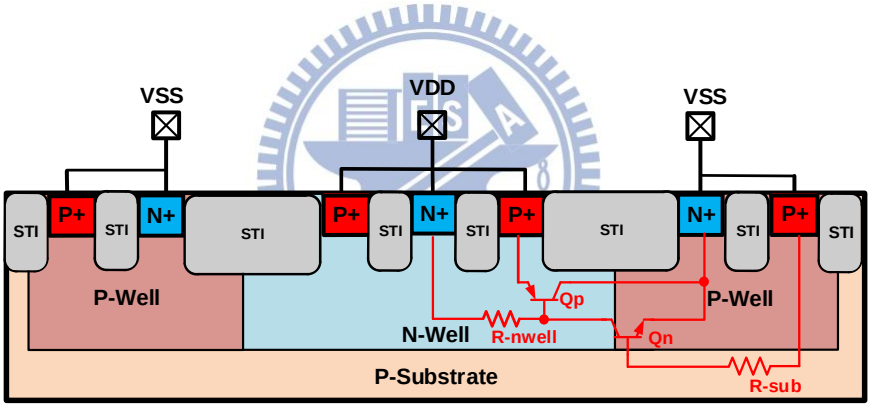


Fig. 2.1. The cross-section view of conventional SCR.

2.2 Motivation

In order to enhance ESD robustness in advanced CMOS process, we put small area and well-performance SCR devices into I/O ESD application. According to traditional whole chip scheme, ESD circuits use ESD diode to realize whole chip ESD protection. PD and NS Mode use diode as I/O ESD devices. Fig. 2.2 shows PD Mode and NS Mode. Positive to VDD mode (PD Mode) is that input pad/output pad ESD current flow to VDD by diode Dp1/Dp2, while NS Mode is that input pad/output pad ESD current flow to VSS by diode Dn1/Dn2.

Both of mode have the shortest ESD discharge path. Therefore, they have a decent performance on ESD Robustness test. Fig. 2.3 shows PS Mode and ND Mode. Compared to PD and NS mode, PS and ND Mode are not same as previous Modes. First of all, the discharge path of PS Mode can be found that ESD current release charges to VSS must go through Dp1 and power-rail ESD clamp circuit. By contrary, ND Mode is that ESD current flow to VSS by diode Dn1/Dn2 and power-rail ESD clamp circuit.

From both discharge modes, ESD power clamp and diode devices are needed. Under the typical whole-chip ESD protection scheme, we should guarantee our breakdown voltage of internal circuit is higher than power clamp voltage (Vt1) and forward bias voltage of ESD diode so that whole chip circuits are protected well by ESD protection circuit.

With the advanced CMOS process, the gate oxide thickness of devices in the integrated circuits (ICs) is ultra-thin. At the same time, ESD sensitivity becomes a critical issue to be concerned. The lower operating voltage is, the lower internal breakdown voltage is. Therefore, the conventional ESD device cannot usefully protect internal circuits. Companies and research groups hope to improve the problem of the weakness of ESD robustness by new SCR devices. Now, there are many similar design

concepts are provided under advanced process.

In this thesis, the purpose of design is to propose a novel SCR devices equipped with low-leakage and low-trigger-voltage and apply I/O ESD protection.

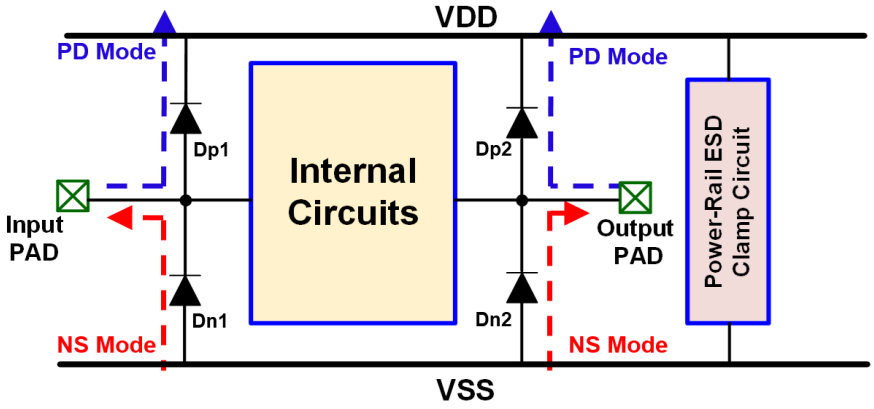


Fig. 2.2. PD Mode and NS Mode.

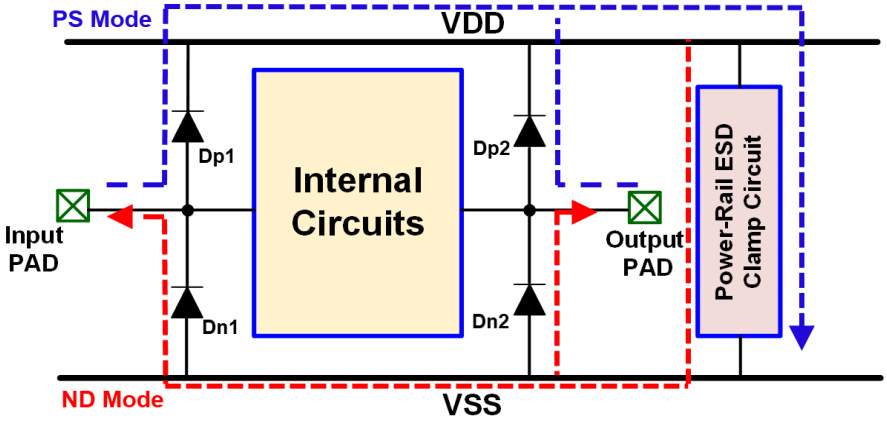


Fig. 2.3. PS Mode and ND Mode.

2.3 The propose Device Structure

The conventional SCR structure remain Shallow trench isolation (STI) which make the turn-on speed slower. To improve this disadvantage, a novel dummy-gate structure is used to block the shallow trench isolation (STI) structure and silicide in the SCR device. Futhermore, using dummy-gate structure can decrease trigger voltage and enhance its turn-on speed. Lower clamp voltage and smaller turn-on resistance, and faster turn-on speed are advantages as well.

The proposed SCR devices use two metal gates between the anode and cathode. One metal gate lies on the N-well/P-well junction, and the other metal gate forms a PMOS in P-SCR device or an NMOS in N-SCR device. These two device structures will be discussed in the following section.

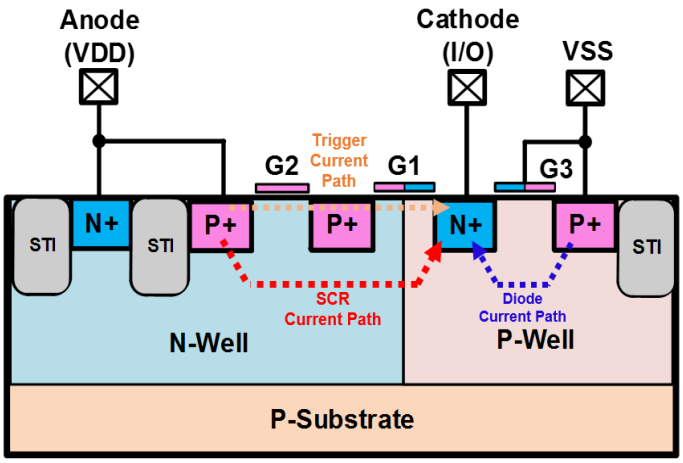
A. PSCR

The proposed SCR device with a PMOS (P-SCR) is shown in Fig. 2.4(a). The P-SCR can provide the ESD current paths from VDD to I/O through SCR current path, and from VSS to I/O through diode current path. To reduce the trigger voltage of PSCR device under ESD stress condition, the gate of PMOS (G2) and the gate across N-well and P-well (G1) should be well controlled, since the channels provide the trigger current path. The control circuit of G1 and G2 is shown in Fig. 2.5. The basic RC timer is used to distinguish the ESD transient and normal power-on, and then the control signals of G1 and G2 are generated. As ESD zapping from anode (VDD) to cathode (I/O) of PSCR, the G2 is firstly at low voltage to induce the P-type channel between P+ and P+, and the G1 is firstly at high voltage to induce the N-type channel between N-well and N+. These two induced channels form the trigger current path, and then the SCR current path can be trigger on. As ESD zapping from VSS to I/O, the ESD current can be discharged through the diode current path. Under normal circuit operating condition,

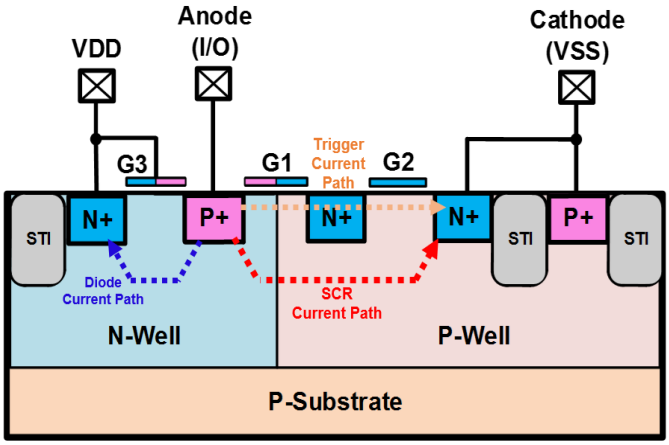
the G1 and G2 keep at the voltage levels of VSS and VDD, respectively, and then the leakage current from anode (VDD) to cathode (I/O) keeps very small.

B. NSCR

The proposed SCR device with an NMOS (NSCR) is shown in Fig. 2.4(b). The NSCR includes the gate across N-well and P-well (G1) and the gate of NMOS (G2). The NSCR can provide the ESD current paths from I/O to VSS through SCR current path, and from I/O to VDD through diode current path. The basic RC timer in Fig. 2.5 is also used to control the G1 and G2 of NSCR. As ESD zapping from anode (I/O) to cathode (VSS) of NSCR, the G1 is firstly at low voltage to induce the P-type channel between P+ and P-well, and the G2 is firstly at high voltage to induce the N-type channel between N+ and N+. These two induced channels form the trigger current path, and then the SCR current path can be trigger on. As ESD zapping from I/O to VDD, the ESD current can be discharged through the diode current path. Under normal circuit operating condition, the G1 and G2 keep at the voltage levels of VSS and VDD88, respectively, and then the leakage current from anode (I/O) to cathode (VSS) keeps very small.

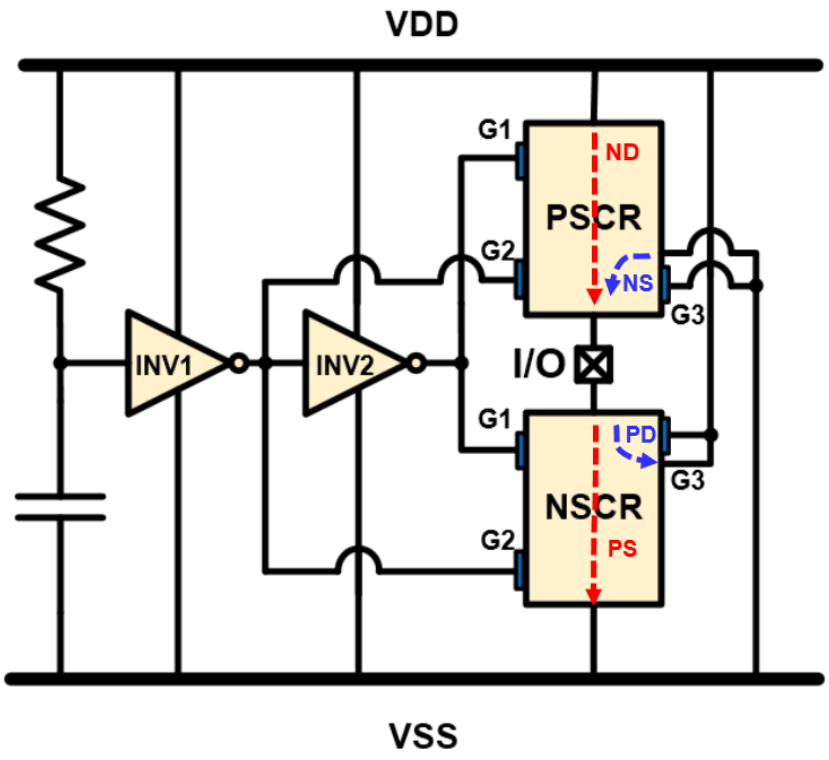


(a)

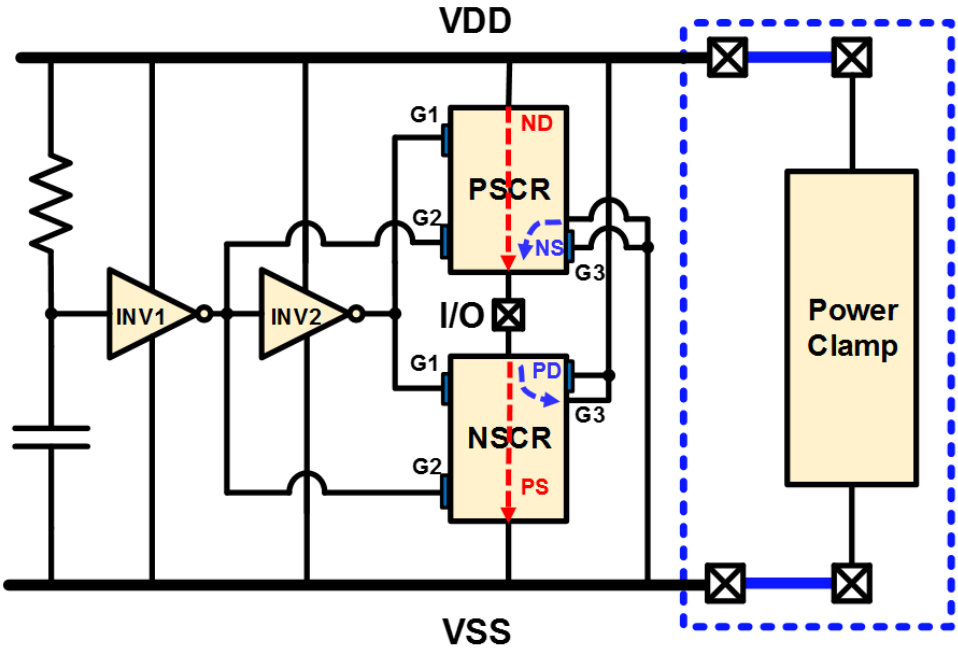


(b)

Fig. 2.4. (a) PSCR and (b) NSCR.



(a)



(b)

Fig. 2.5. PSCR and NSCR with trigger design for whole-chip ESD protection.
(a) Without power-rail ESD clamp circuit and (b) With power-rail ESD clamp circuit.

2.4 Measurement results

The test devices of PSCR and NSCR have been fabricated in 28-nm HKMG CMOS process. The dimension of each SCR is selected to be 20μm. In the trigger circuit, the RC time constant is 100ns, and the dimensions of PMOS and NMOS are 14μm and 6μm, respectively.

2.4.1. Normal Circuit Operating Condition

In normal circuit operating condition, the leakage current of the test devices are measured. The environment of leakage measurement is shown in Fig. 2.6. We use Power supply to measure all possible leakage path in proposed device. The voltages of VDD and VSS are 0.9V and 0V, respectively. The voltage drop of 0.9V between anode and cathode, the leakage currents of PSCR and NSCR are 3.2nA and 4.5nA, respectively.

In normal circuit operating condition, I/O of PSCR and NSCR are given different bias voltage. In the worst case, when I/O pin of PSCR reach to 0.0V, there is a maximum leakage current measured from VDD to I/O and its value is 10nA. However, when I/O pin of NSCR reach to 0.9V, there is a maximum leakage current measured from I/O to VSS and its value is 12nA.

All experiment data of the test devices in a 28-nm high-k/metal gate CMOS process are listed in Table 2.1. From above measurement results, PSCR and NSCR I/O device can efficiently reduce leakage current and guarantee the internal circuits would not be affected.

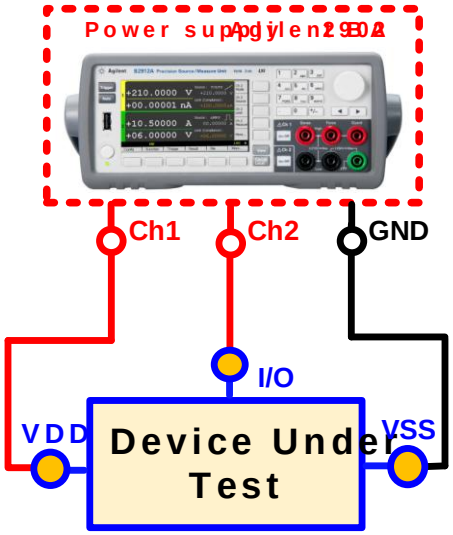


Fig. 2.6. The environmental setting of DC measurement.

Table 2.1 The standby leakage current of test devices with 20μm width in a 28-nm HKMG CMOS process.

Device	Leakage Path	Standby Leakage Current
PSCR	VDD to I/O	10nA
	VDD to VSS	4.5nA
NSCR	I/O to VSS	12nA
	VDD to VSS	3.2nA

2.4.2. ESD stress Condition

The human-body-model (HBM) ESD robustness of each device is tested. The PSCR and NSCR can pass 1.4kV and 1.8kV HBM ESD tests, respectively. The HBM robustness of both devices are high enough with regard to the recommended 1kV HBM robustness [22].

To investigate the I-V characteristics of the test devices, the transmission-line-pulsing (TLP) system with a 10ns rise time and a 100ns pulse width is used. The TLP-measured I-V curves of test devices are shown in Fig. 2.7. The diode current paths of PSCR (PSCR_Diode) and NSCR (NSCR_Diode) can turn on to discharge the NS and

PD currents, respectively. The SCR current paths of PSCR (PSCR_SCR) and NSCR (NSCR_SCR) can trigger on at 2.3V and 2.6V, respectively, and snap back to 2.0V and 2.4V, respectively. The proposed devices have high enough holding voltage to prevent from latch-up issue. To handle the ~0.6A ESD current during 1kV HBM stress [22], the clamping voltages of PSCR and NSCR are 4.3V and 4.8V, respectively. Of course, increasing the device size can reduce the turn-on resistance and decrease the clamping voltage.

In the real cases, the power-rail ESD clamp circuit should be equipped between V_{DD} and V_{SS}. In this work, two series diodes are used as the power-rail ESD clamp circuit [23]. The TLP-measured I-V curves of test devices with additional power-rail ESD clamp circuit are shown in Fig. 2.8. The clamping voltage, turn-on resistance, and current handling ability can be further improved.

To evaluate the effectiveness of proposed devices in faster ESD-transient events, another very-fast TLP (VF-TLP) system with a 0.2ns rise time and a 5ns pulse width is used. The VF-TLP-measured I-V curves of test devices are shown in Fig. 2.8. The transient voltage waveforms of proposed devices at holding region are also shown in Fig. 2.9. According to the measurement results, the overshoot voltage and clamping voltage of proposed devices are low enough, which can effectively protect the internal circuits from ESD damages.

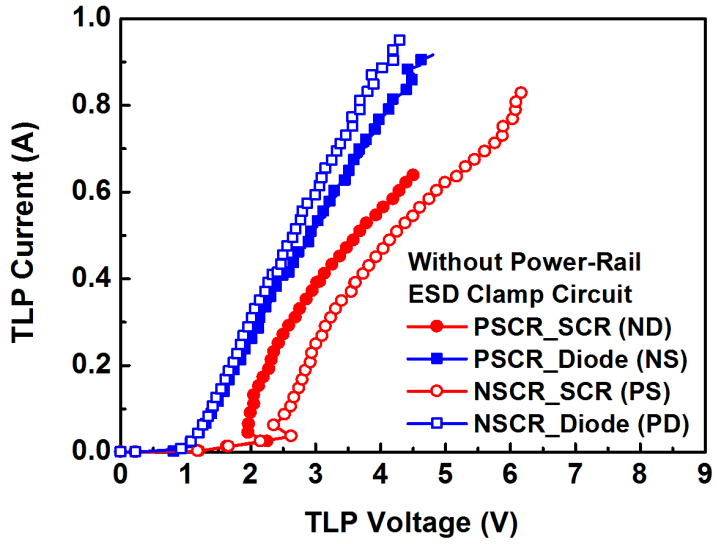


Fig. 2.7. TLP-measured I-V curves of test devices without power-rail ESD clamp circuit.

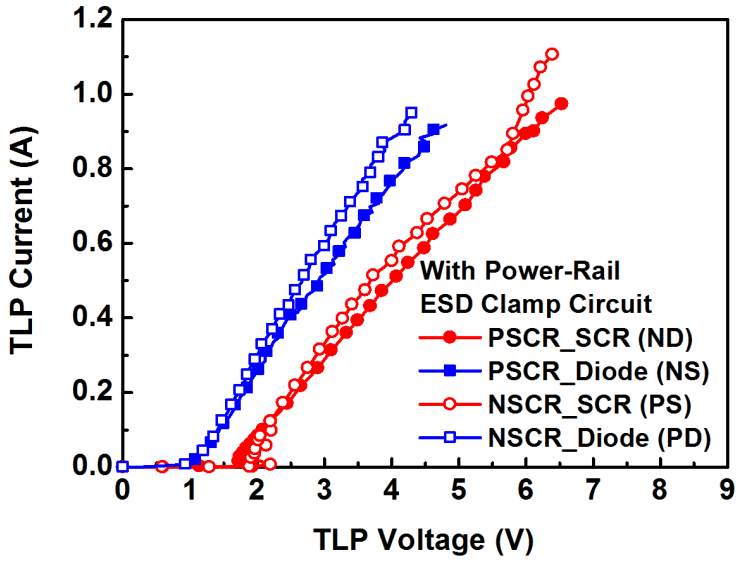


Fig. 2.8. TLP-measured I-V curves of test devices with power-rail ESD clamp circuit.

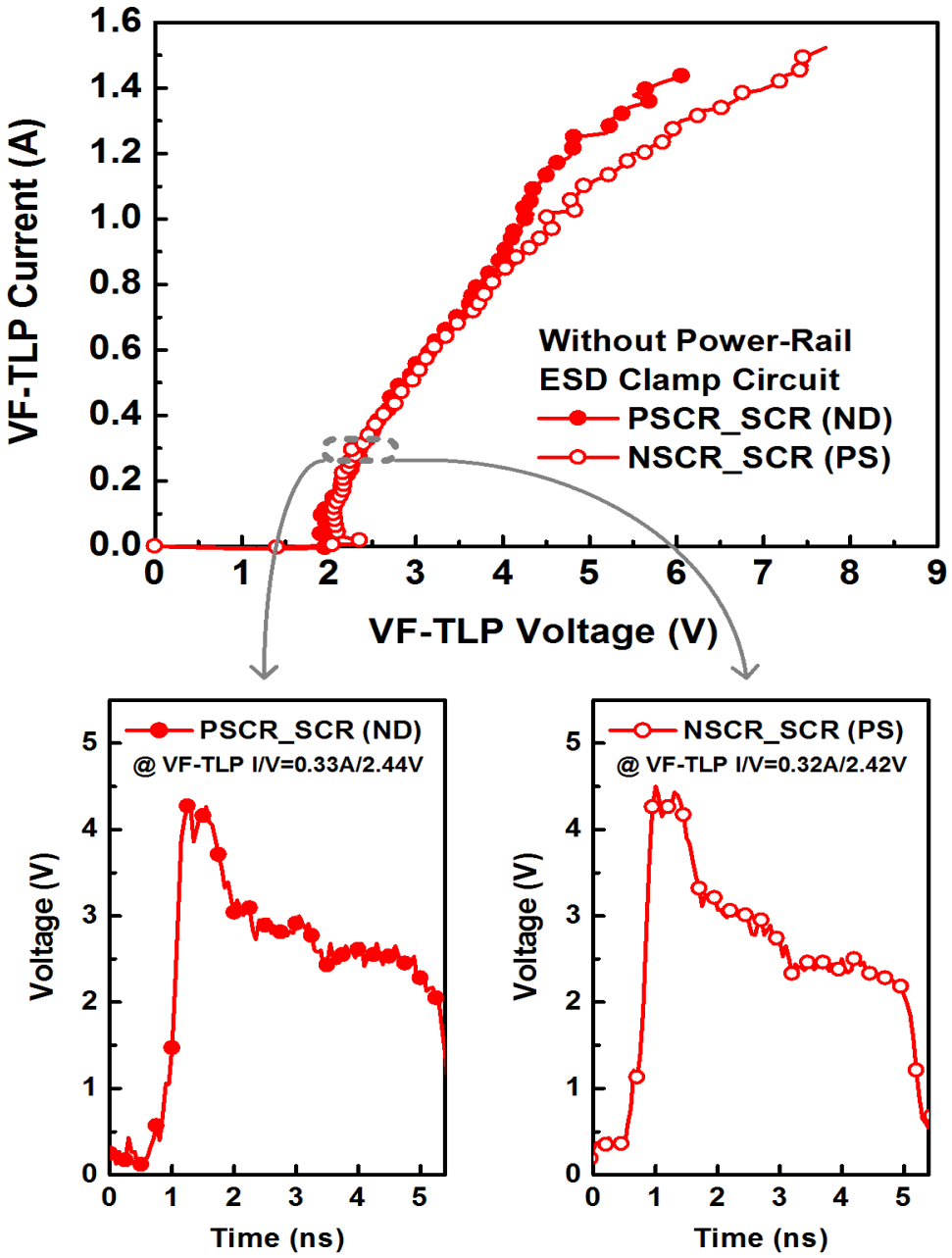


Fig. 2.9. VF-TLP-measured I-V curves and transient voltage waveforms of test devices without power-rail ESD clamp circuit.

2.4.3 Parasitic Capacitance

The parasitic capacitance seen at I/O port of each test device is measured by using the vector network analyzer. The parasitic effects of the pads have been removed by using the de-embedding technique [24]. Fig. 2.10 shows the extracted parasitic capacitances of the test devices. Both PSCR and NSCR appear low enough capacitance at gigahertz frequency. With the low capacitance, the PSCR and NSCR can be used for high-speed or high-frequency applications.

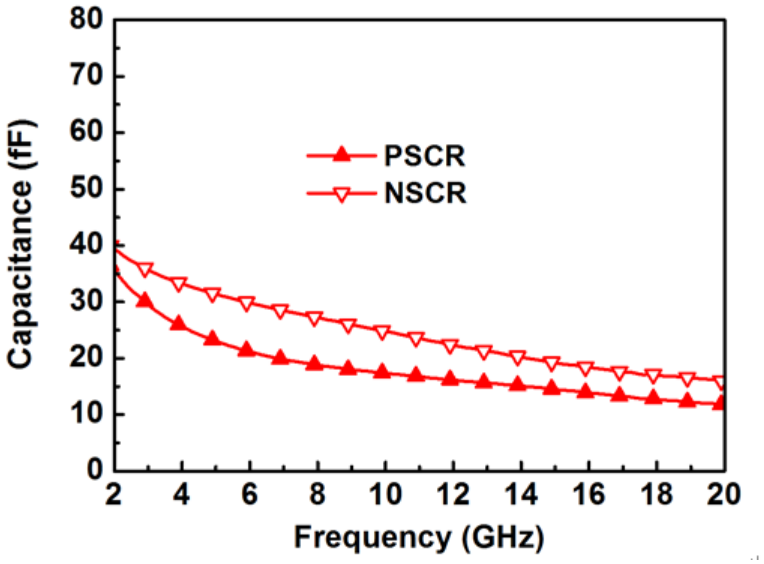


Fig. 2.10. Parasitic capacitance of PSCR and NSCR.

2.5 Summary

The proposed SCR devices have been developed for ESD protection in 28-nm CMOS process without using the silicide blocking, schottky junction, deep N-well, or other additional masks. The PSCR in 28nm HKMG CMOS process can be triggered at 2.3V and its holding voltage is 2.0V. Under HBM ESD tests, the PSCR device with width 20μm can pass 1.4kV. Moreover, the NSCR in 28nm HKMG CMOS process can be triggered at 2.6V, and NSCR can snap back to 2.4V. Under HBM ESD tests, the NSCR device with width 20μm can pass 1.8kV. Besides, they have low leakage current and low parasitic capacitance. Therefore, with the good performances during ESD stress and normal circuit operating conditions, the proposed SCR device is very suitable for ESD protection in 28nm HKMG CMOS process. All experiment data of the PSCR and NSCR are listed in Table 2.2 and Table 2.3.

Table 2.2 The measurement data of test devices without power-rail ESD clamp circuit.

	PSCR_SCR (Anode-to-Cathode)	NSCR_SCR (Anode-to-Cathode)
Width (W)	20μm	20μm
Leakage Current at 0.9V	3.2nA	4.5nA
TLP Vt1	2.3V	2.6V
TLP Vhold	2.0V	2.4V
TLP It2	0.65A	0.81A
VF-TLP Vt1	2.1V	2.4V
VF-TLP Vhold	2.0V	2.1V
VF-TLP It2	1.44A	1.53A
HBM ESD Robustness	1.4KV	1.8KV
Capacitance at 1GHz / 10GHz	36fF/18fF	39fF/25fF

Table 2.3 The measurement data of test devices with power-rail ESD clamp circuit.

	ND-Mode	NS-Mode	PS-Mode	PD-Mode
TLP Vt1	1.93V	1.07V	2.2V	1.12V
TLP Vhold	1.73V	N/A	1.9V	N/A
TLP It2	0.97A	0.92A	1.1A	0.95A

Chapter 3

Power-Rail ESD Clamp Circuit with Low trigger voltage Silicon Controlled Rectifier Device in 28-nm CMOS Process

3.1 Introduction and Motivation

A whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits is proposed to provide a real whole-chip ESD protection. The efficient VDD-to-VSS ESD clamp circuit has been designed to provide a low-impedance path between the VDD and VSS power lines of the IC during the ESD-stress condition, but this ESD clamp circuit is kept off when the IC is under its normal operating condition. To avoid ESD high energy destruction for integrated circuits, parasitic bipolar junction transistors (BJTs) in gate-VDD PMOS (GDPMOS) and gate-grounded NMOS (GGNMOS) devices are used to ESD protection device, especially ESD power clamp device. The devices cross-sectional view of the gate-grounded NMOS (GGNMOS) and gate-VDD PMOS (GDPMOS) are shown in Fig. 3.1 and Fig. 3.2, respectively. When the GGNMOS or the GDPMOS is under ESD stress, the parasitic NPN (N+, P-well, and N+) or PNP (P+, N-well, and P+) BJT will be triggered to discharge ESD current.

However, the thinner gate oxide problem exists due to CMOS process development and that cause ESD robustness decreasing. Conventional GGNMOS and GDPMOS are not enough to solve the problem of decreasing ESD robustness in advanced CMOS process, and their ESD reliability decrease as well. One of method is scaling size of ESD devices to solve the problem of low ESD robustness, but this method cost amount of

layout area to reach high-end ESD robustness. Moreover, companies also cost huge price and decrease revenue from productions.

The SCR device has been reported to be useful for ESD protection due to its decent ESD robustness, small device size, and excellent clamping capabilities (low holding voltage and small turn-on resistance) [25]-[29].

Due to high ESD robustness of SCR devices, we hope this structure can be applied on power clamp circuit in 28nm process. Fig. 3.1 shows the GGNMOS device cross-section view. We have to overcome the disadvantage of traditional SCR devices, which trigger voltage is too high. Our research motivation is to resolve this disadvantage and propose two novel SCR devices. At last, we will compare this two proposed devices with conventional SCR and substrate trigger SCR.

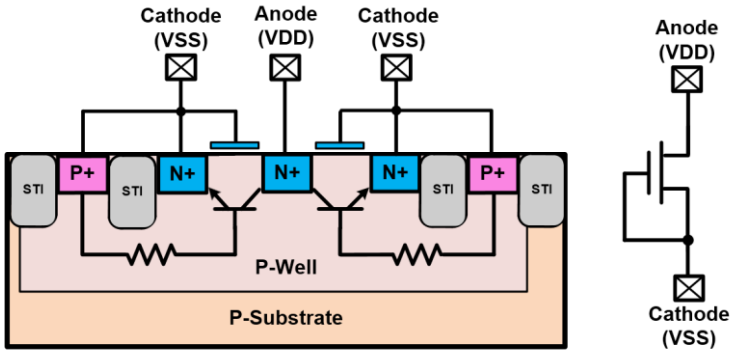


Fig. 3.1. The cross-section view of GGNMOS.

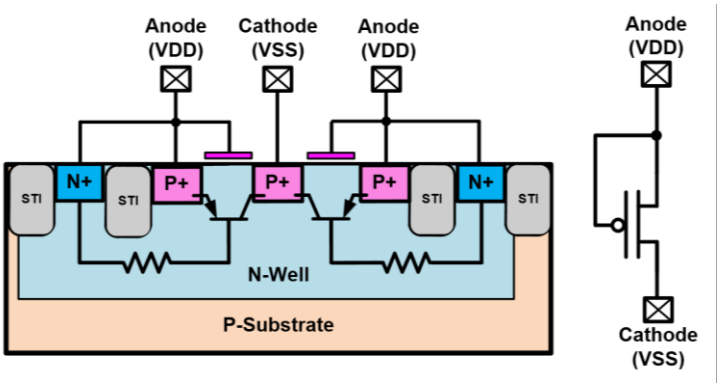


Fig. 3.2. The cross-section view of GDPMOS.

3.2 The Proposed design devices in 28-nm HKMG CMOS Process

3.2.1 Device Structure

The device cross-sectional view of the proposed device are P-SCR_PC and N-SCR_PC. The proposed design cross-section view of P-SCR_PC is shown in Fig. 3.3, we add a PMOS structure and dummy gate to conventional SCR structure. PMOS source is defined as VDD (Anode). When ESD Zapping, ESD current discharge from the VDD (anode) to VSS (cathode) by parasitic SCR path (P+, N-Well, P-Well/P-sub, N+). Due to the Latch-up positive feedback mechanism, it make ESD current efficiently discharge to VSS (cathode). Fig. 3.4 shows the proposed design cross-section view of N-SCR_PC The main structure of N-SCR_PC add a NMOS structure and dummy gate to traditional SCR devices. The proposed devices structure have a characteristic of low-leakage under normal circuits operating condition.

Dummy gate is inserted in our two proposed design devices. The advantaged of our design is that shallow trench isolation (STI) can be eliminated without another masks [30]. Therefore, parasitic SCR path can be shorter than conventional SCR parasitic path. Parasitic SCR turn-on speed and low voltage Vt1 are also improved. In last session, we would combine ESD transient detection circuit and the proposed devices to enhance ESD robustness.

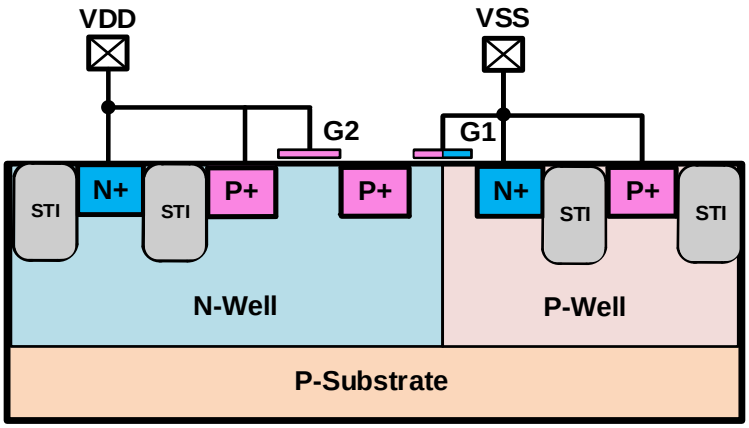


Fig. 3.3. The cross-section view of P-SCR_PC without ESD Transient Detection Circuit in 28-nm HKMG CMOS process.

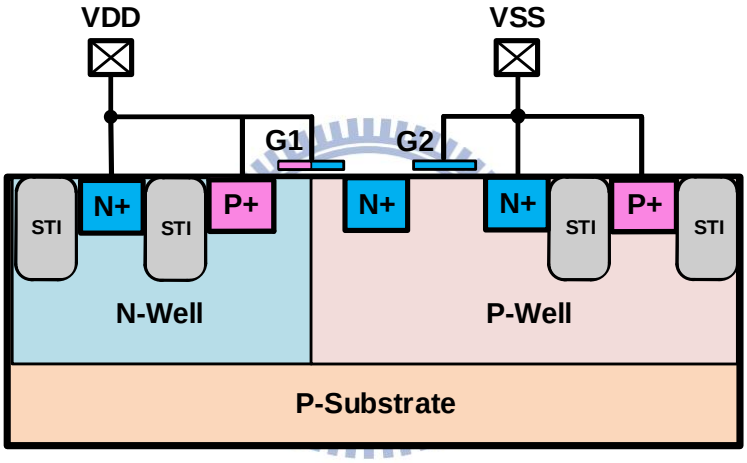


Fig. 3.4. The cross-section view of N-SCR_PC without ESD Transient Detection Circuit in 28-nm HKMG CMOS process.

3.2.2 DC Characteristics and Leakage Current

A. P-SCR_PC

The power-rail ESD clamp circuit plays an important role in the ESD protection scheme. Under normal circuit operating condition, VDD turns P-SCR_PC device off while SCR devices usefully turns on parasitic SCR path when ESD zapping. ESD current can efficiently discharges from VDD to VSS. The power-rail ESD clamp cell of P-SCR_PC combine ESD transient detection circuit is shown in Fig. 3.5.

Resistor is set to 50KΩ and MOS capacitor is equal to 2pF. Two stage inverter are also included. The output of first stage inverter is connected to the Gate-1, while the output of second stage inverter is connected to the Gate-2. Both of them are used to control P-SCR_PC device.

In normal circuit operating condition, the output of first stage inverter would pull the voltage of Gate-1 to 0V. The Gate-1 is located at the place between N-Well and P-Well. Gate-1 attracts holes and form inversion in N-well, generating P-type channel. To avoid problem of leakage current, we embedded a PMOS structure as a switch to resolve problem. PMOS turns off under normal operating condition. Gate-1 still has P-type channel, but Gate-2 turns off. The voltage between P-channel Source and gate is lower thanV_{tp}, $V_{gs}<V_{tp}$. This method can resolve the leakage current problem of P-SCR_PC and efficiently turn off P-SCR_PC device. Fig. 3.6 shows the result of standby leakage while P-SCR_PC work in normal operating condition. As VDD=0.9V, Width=100μm and Width=300μm standby leakage are 2.6nA and 4.5nA, respectively.

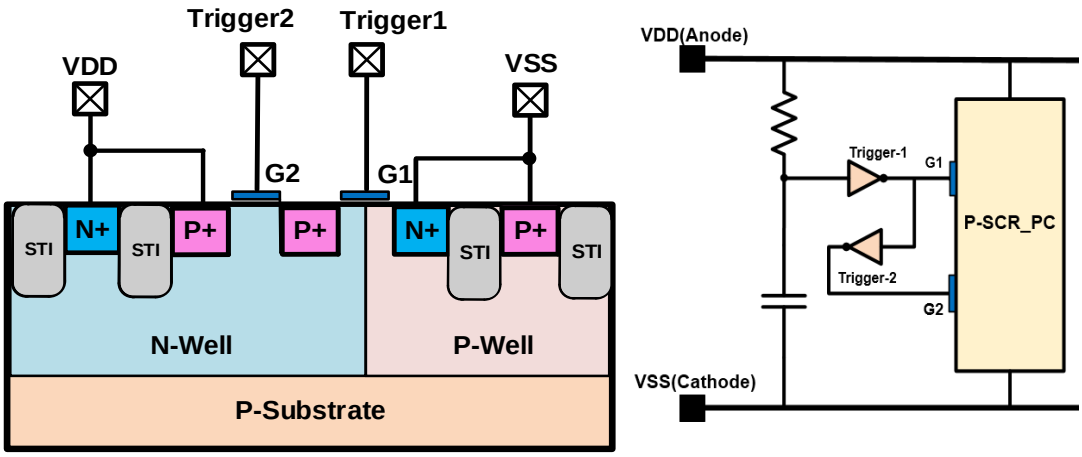


Fig. 3.5. The power-rail ESD clamp cell of P-SCR_PC combine ESD Transient Detection Circuit.

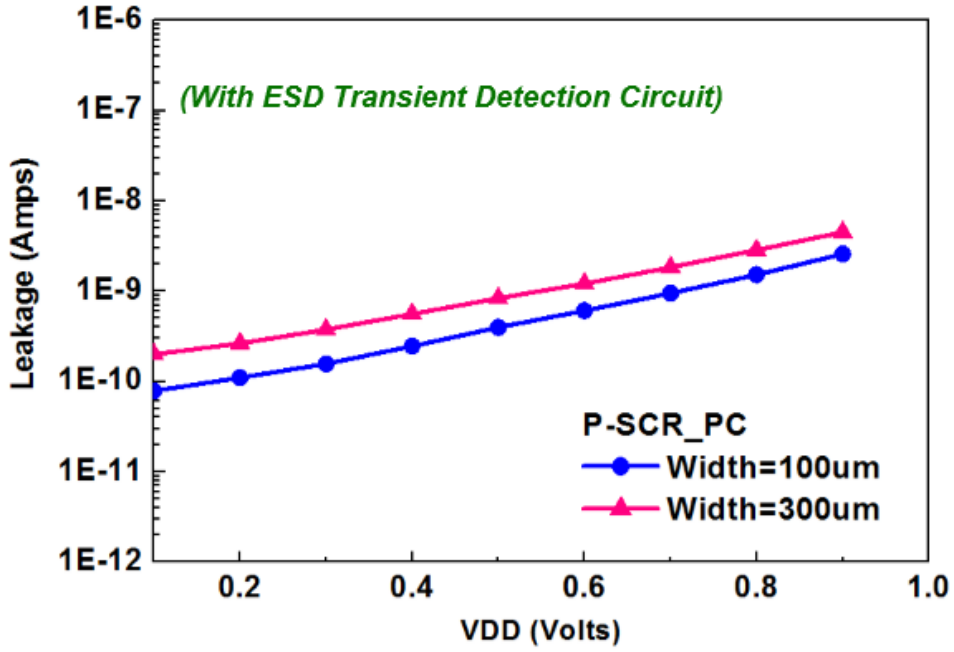


Fig. 3.6. The leakage measurement of the P-SCR_PC in a 28-nm HKMG CMOS process.

B. N-SCR_PC

The power-rail ESD clamp circuit plays an important role in the ESD protection scheme. VDD turns N-SCR_PC device off under normal circuit operating condition while SCR devices usefully turns on parasitic SCR path when ESD zapping. ESD current can efficiently discharges from VDD to VSS. The power-rail ESD clamp cell

of N-SCR_PC combine ESD Transient Detection Circuit is shown in Fig. 3.7.

Resistor is set to 50KΩ and MOS capacitor is equal to 2pF. Two stage inverter are also included. The output of first stage inverter is connected to the Gate2, while the output of second stage inverter is connected to the Gate1. Both of them are used to control N-SCR device.

In normal circuit operating condition, the output of first stage inverter would pull the voltage of Gate-1 to 1V. The Gate-1 is located at the place between N-Well and P-Well. Gate-1 attracts electrons and form inversion in P-well, generating N-type channel. To avoid problem of leakage current, we embedded a NMOS structure as a switch to resolve problem. NMOS turns off under normal operating condition. Gate-1 still has n-type channel, but Gate-2 turns off. The voltage between N-channel gate and source lower thanV_{tn}, V_{gs}<V_{tn}. This method can resolve the leakage current problem of N-SCR_PC and efficiently turn off N-SCR_PC device. Fig. 3.8 shows the result of standby leakage while N-SCR_PC work under normal operating condition. When VDD=0.9, Width=100μm and Width=300μm standby leakage are 16nA and 60nA, respectively.

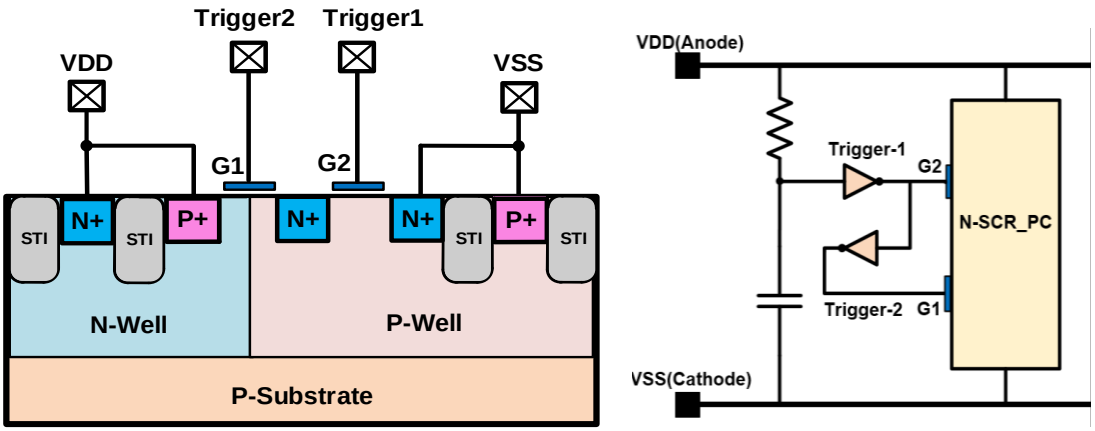


Fig. 3.7. The power-rail ESD clamp cell of N-SCR_PC combine ESD Transient Detection Circuit.

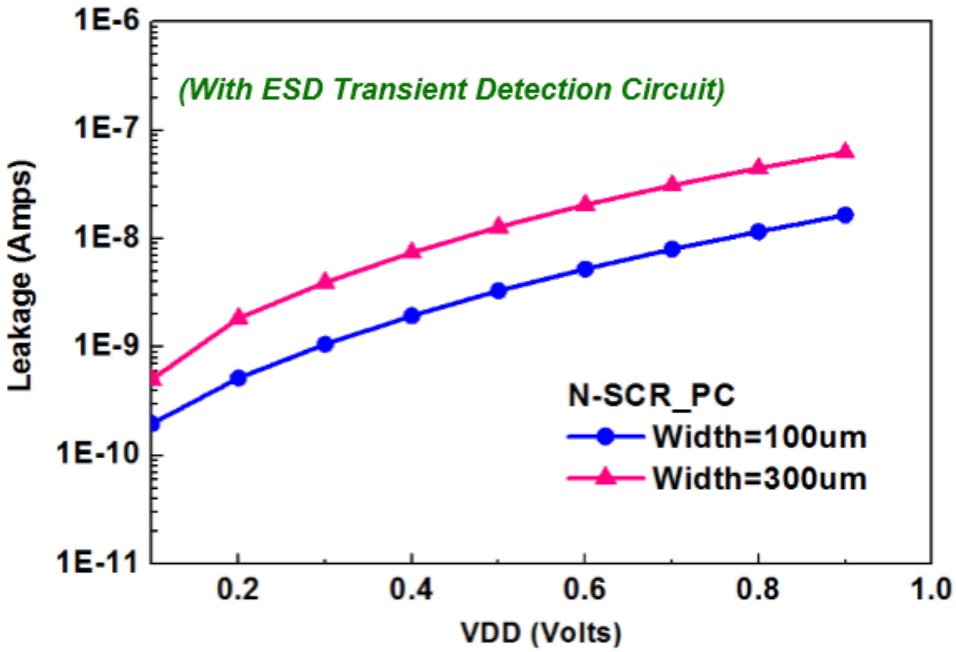


Fig. 3.8. The leakage measurement of the N-SCR_PC in 28-nm HKMG CMOS process.

3.2.3 TLP Characteristics

The TLP-measured I-V curves of P-SCR_PC devices are shown in Fig. 3.9 and Fig. 3.10. In Fig. 3.9, the measurement results of P-SCR_PC devices do not combine with the ESD transient detection circuit. The TLP measurement of It2 of P-SCR_PC with 100μm and 300μm are 0.4A and 0.66A. Fig. 3.10 shows that It2 of P-SCR_PC devices combined with ESD Transient Detection Circuit are only 0.67A and 1.58A, respectively. This results demonstrate that ESD robustness is not as well as we predict. However, the TLP measurement of Vt1 of proposed device P-SCR_PC with 100μm and 300μm are 1.6V and 1.5V, respectively. Vt1 successfully decrease voltage from 7.4V/ 7.8V to 1.6V/1.5V.

On the other hand, In Fig. 3.11, the measurement results of N-SCR_PC devices are not combined with the ESD transient detection circuit. The TLP measurement of It2 of N-SCR_PC with 100μm and 300μm are 0.56A and 0.58A. In Fig. 3.12, the TLP measurement of It2 of N-SCR_PC combing ESD transient detection circuit with 100μm and 300μm are 0.84A and 2.43A. The trigger voltage successfully drop from 6.5V/5.9V to 1.7V/1.5V with Width=100μm and Width= 300μm, respectively.

From the TLP measurement results, we found that the proposed device efficiently decreases trigger voltage and greatly improves SCR overpass turn-on speed. However, the performance of It2 are not well and proposed devices including N-SCR_PC and P-SCR_PC are necessary to improved.

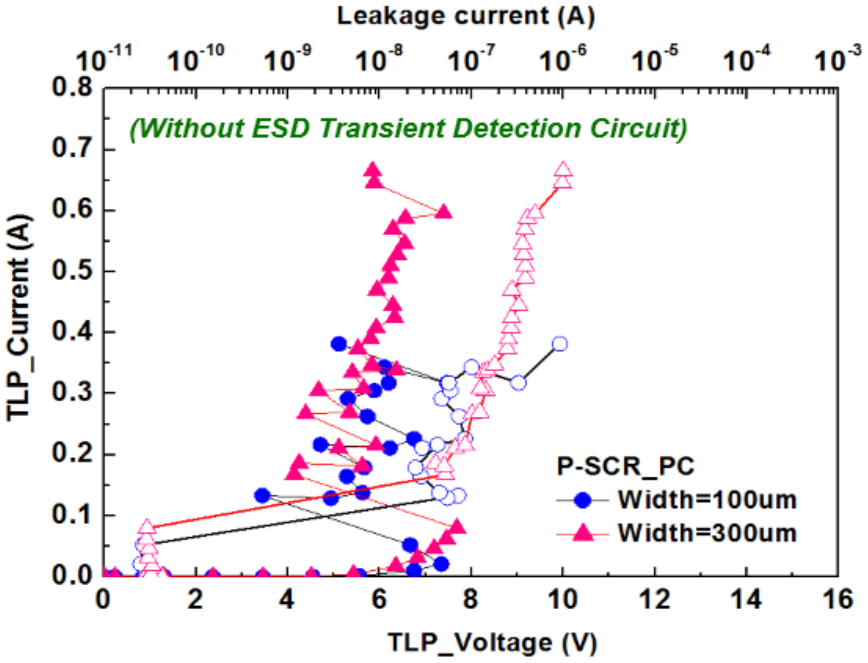


Fig. 3.9. TLP-measured I-V curves of P-SCR_PC without ESD Transient Detection Circuit in 28-nm HKMG CMOS process.

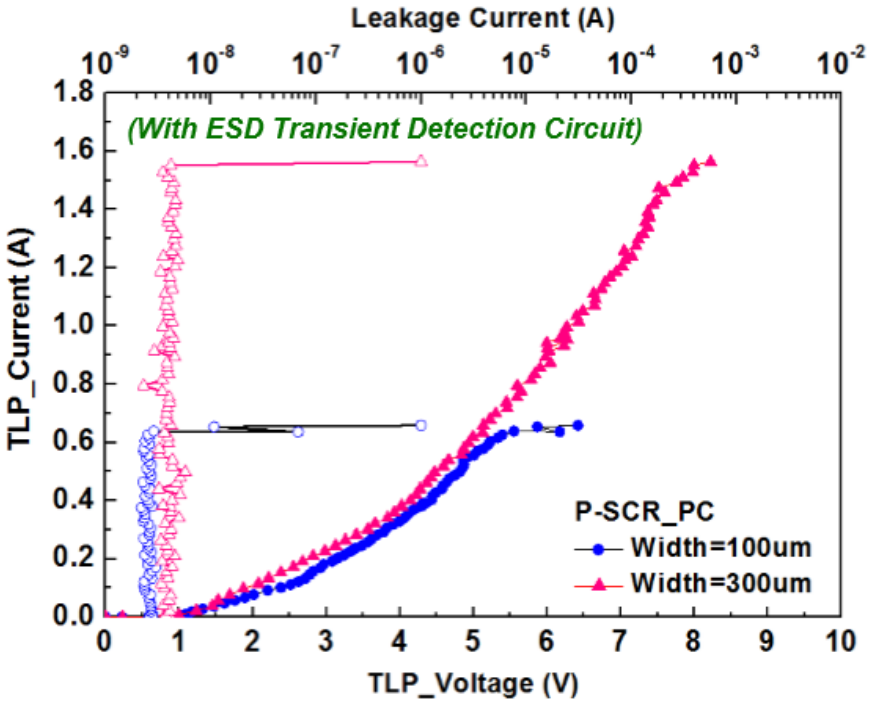


Fig. 3.10. TLP-measured I-V curves of P-SCR_PC with ESD Transient Detection Circuit in 28-nm HKMG CMOS process.

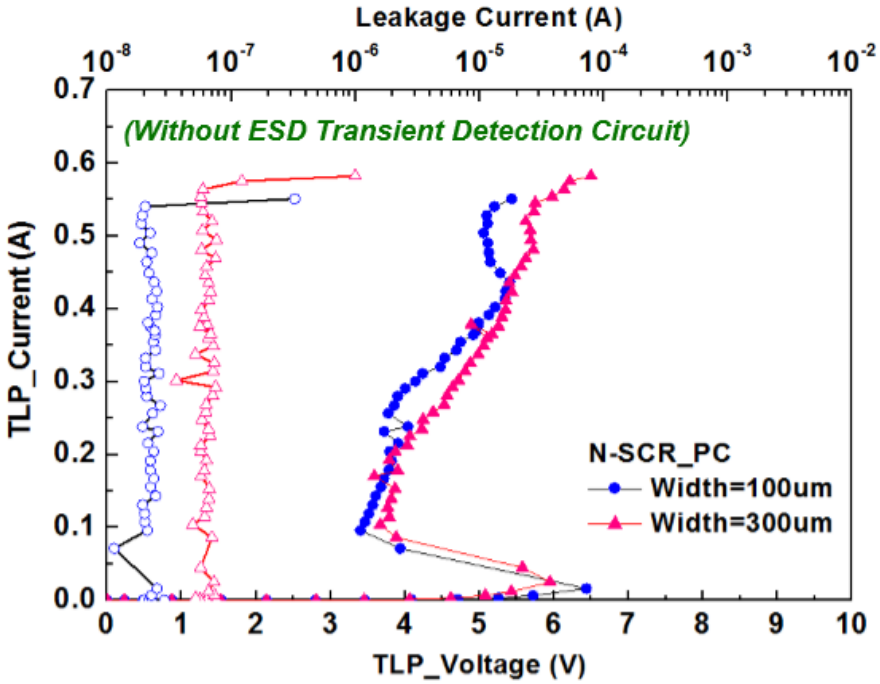


Fig. 3.11. TLP-measured I-V curves of N-SCR_PC without ESD Transient Detection Circuit in 28-nm HKMG CMOS process.

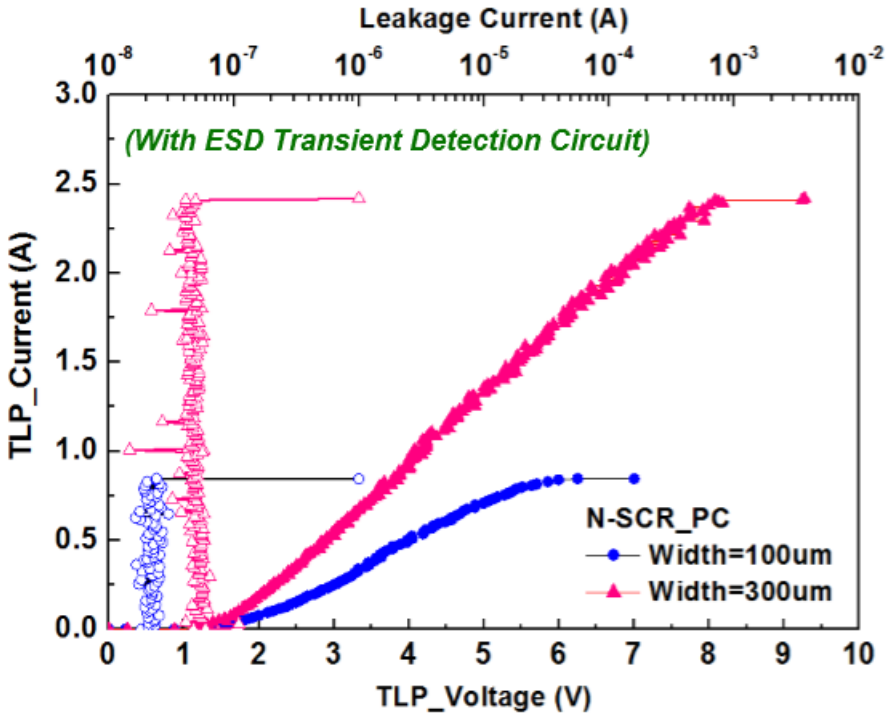


Fig. 3.12. TLP-measured I-V curves of NSCR_PC with ESD Transient Detection Circuit in 28-nm HKMG CMOS process.

3.2.4 Failure Analysis

After ESD test，we used the scanning electron microscope(SEM) to find out the failure locations in the device. Fig. 3.13 is manifested as SEM photo of 300um P-SCR_PC. We can found that failure locations are located at Gate oxide, especially on the top and bottom place. The medium place of device has few failure locations. This results shows that when ESD zapping, ESD Transient Detection Circuit can provide different voltage to the Gates. SCR parasitic path can be easier turned on but huge ESD current harms Gates. In 28-nm HKMG CMOS process, this phenomenon is obvious to observe. The distance between Anode (P+ Diffusion Area)/Cathode (N+ Diffusion Area) and gates should be more serious to be concerned. Fig. 3.14 shows that although devices width is equal to 300μm, N-SCR_PC devices without uniformly turn on lead to weak ESD robustness. Moreover, the metal width of power-clamp circuit layout should be wider to sustain large current.

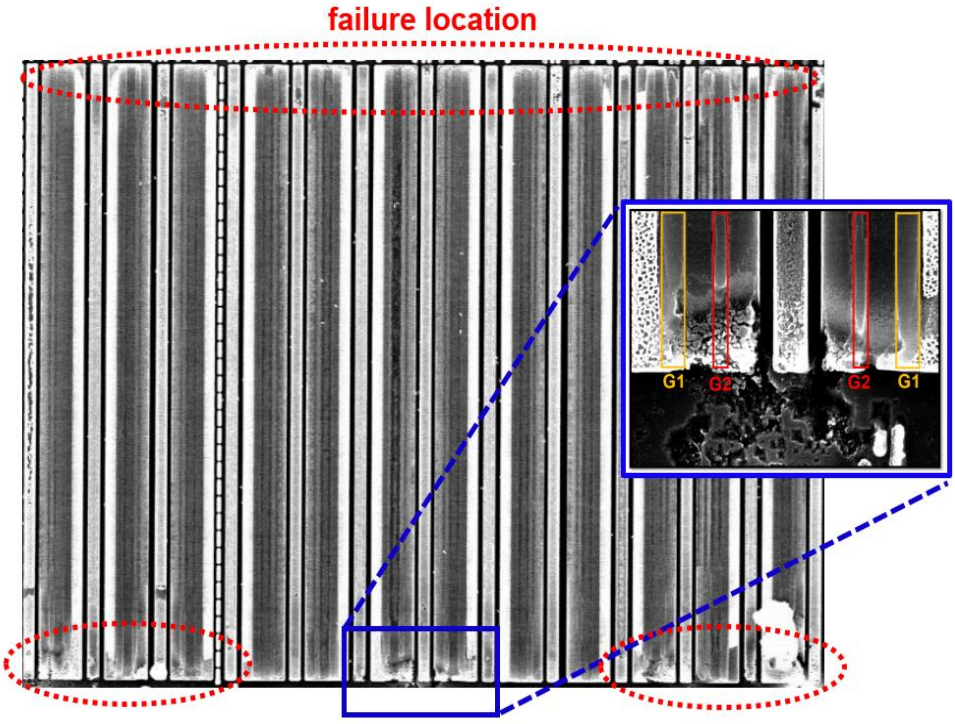


Fig. 3.13. SEM photo of P-SCR_PC device (W=300μm) after 1.6A TLP ESD test.

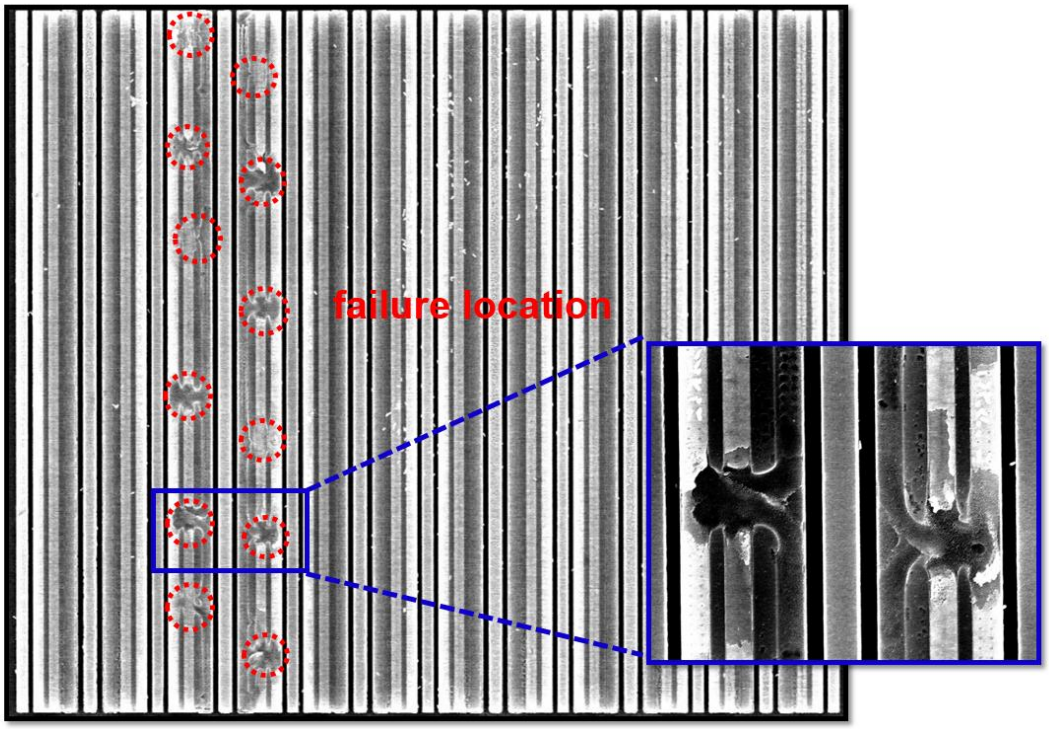


Fig. 3.14. SEM photo of N-SCR_PC device (W=300μm) after 2.4A TLP after ESD test.

3.2.5 Summary

In 28-nm HKMG CMOS Process, The measurement data of P-SCR_PC and N-SCR_PC are listed in the Table 3.1. Adding ESD transient detection circuit can usefully decrease trigger voltage which is generated from parasitic SCR path in P-SCR_PC and N-SCR_PC. The drop voltage of Vt1 proof that trigger-path mechanism of new devices helpfully decrease parasitic SCR path trigger voltage.

On the other hand, It2 performance is not as predictable as we predict. One possible reason is that when ESD is zapping, embedded gates are destroyed due to thinner Gate oxide, high ESD sensitivity. When ESD current flows to devices, anode (P+ diffusion) and cathode (N+ diffusion) have an extreme current passing, leading to burn out gates on SCR path. In order to improve this disadvantage, we need to optimize the proposed design of SCR devices layout.

P-SCR_PC and N-SCR_PC are used to compare with GGNMOS [31] in the 28nm HKMG CMOS process. We found that conventional GGNMOS of ESD robustness is too weak to sustain huge ESD current.

Table 3.1 The measurement data of test devices in 28-nm HKMG CMOS process.

	GGNMOS [31]		P-SCR_PC				N-SCR_PC			
CMOS Process	28-nm (High-k Metal Gate CMOS Process)									
Width	120μm	300μm	100μm	300μm	100μm	300μm	100μm	300μm	100μm	300μm
ESD Transient Detection Circuit	w/o	w/o	w/o	w/o	w/i	w/i	w/o	w/o	w/i	w/i
Leakage Current at 0.9V	82.2nA	270.9nA	1.54nA	3.68nA	2.6nA	4.5nA	14nA	50nA	16nA	60nA
TLP Vt1	4.30V	4.04V	7.4V	7.8V	1.6V	1.5V	6.5V	5.9V	1.7V	1.5V
TLP Vhold	3.98V	3.95	3.4V	4.1V	N/A	N/A	3.4V	3.6V	N/A	N/A
TLP It2	0.6A	1.25A	0.4A	0.66A	0.67A	1.58A	0.56A	0.58A	0.85A	2.43A
HBM ESD Robustness	0.5kV	1.5kV	0.5kV	0.6kV	0.6kV	2.4kV	0.6kV	0.8kV	1.2kV	4.8kV

3.3 Modified the Proposed device Structure in-28nm without HKMG CMOS Process

3.3.1 Introduction

In this chapter 3.3.1, this work is to optimize two proposed design devices in the 28-nm without HKMG CMOS process. Moreover, we add conventional Substrate trigger SCR (ST-SCR) and traditional SCR device to compare the optimized proposed design device. Fig. 3.15 shows the conventional SCR cross-section view, while Fig. 3.16 demonstrates the Substrate trigger SCR cross-section view. The conventional substrate trigger SCR structure remain shallow trench isolation (STI) structure. The deeper STI structure in the ST-SCR device creates a longer parasitic current path from the anode to the cathode, which also leads to a slow turn-on speed and the extra P+ diffusions are inserted into the ST-SCR device structure. The inserted P+ diffusions are connected out as the trigger node of the ST-SCR device. When a trigger current is applied into this trigger node, the ST-SCR can be triggered easily. The additional N-well regions under the cathode (N+ diffusion) of the ST-SCR device is used to further enhance the turn-on speed of the ST-SCR for more effective ESD protection because they increase the equivalent substrate resistance.

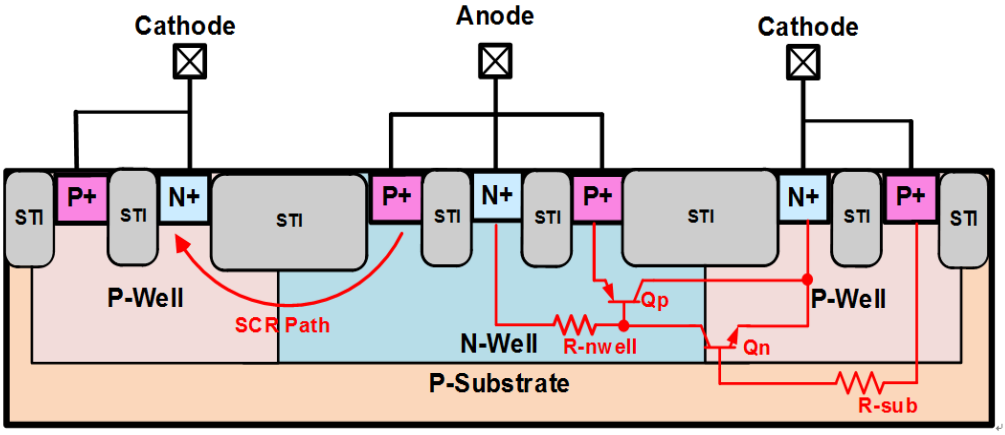


Fig. 3.15. Cross-sectional view of the Conventional SCR in-28nm CMOS process.

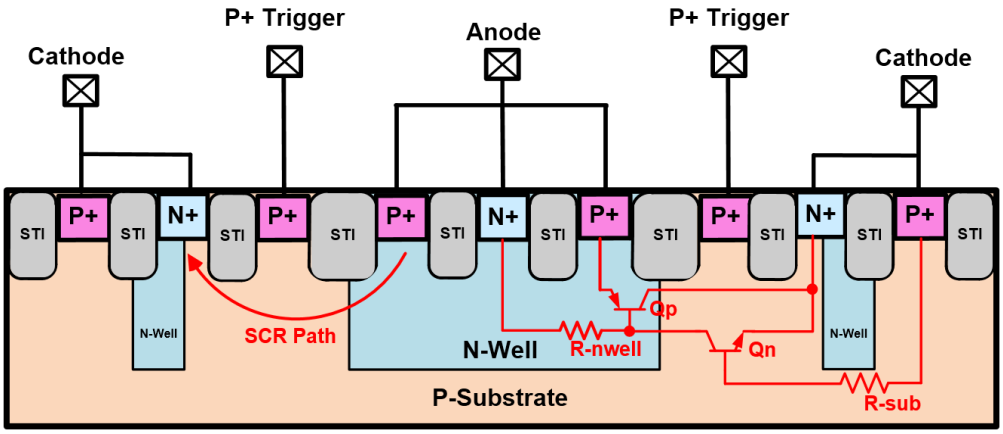


Fig. 3.16. Cross-sectional view of the Substrate trigger SCR in-28nm CMOS process.

3.3.2 Optimization of Device Structure

Fig. 3.17 shows the power-rail ESD clamp cell of fully-Silicide P-SCR_PC (Type A) combine ESD transient detection circuit. To decrease the holding voltage, one solution is to increase the R-sub/R-well in SCR device.

In addition, Fig. 3.18 is the power-rail ESD clamp cell of non-Silicide P-SCR_PC (Type B) combine ESD transient detection circuit. We increase silicide blocking (SAB) width surrounding Gate-1 and Gate-2 to enhance ballast resistance. The purpose of adding SAB width is to enhance ESD robustness. Fig. 3.19 shows the layout top view of P-SCR_PC devices.

From the explication of energy band diagrams, MOSFET with a discharging current path near to its channel and parasitic lateral BJT often cause a low ESD robustness. Therefore, the device with a wider channel width, a larger clearance from contact to the poly-gate edge leads to a higher ESD robustness [32].

On the research of adding silicide blocking (SAB) width, we proposed new design of P-SCR_PC (Type B) and N-SCR_PC (Type B). Both of them are optimized by adjusting SAB width. In the meanwhile, we use different ESD measurement to analyze their characteristics.

Fig. 3.20 and Fig. 3.21 are Fully Silicide N-SCR_PC (Type A) and non-Silicide N-SCR_PC (Type B) cross-section view, respectively. Fig. 3.22 shows the layout top view of N-SCR_PC devices.

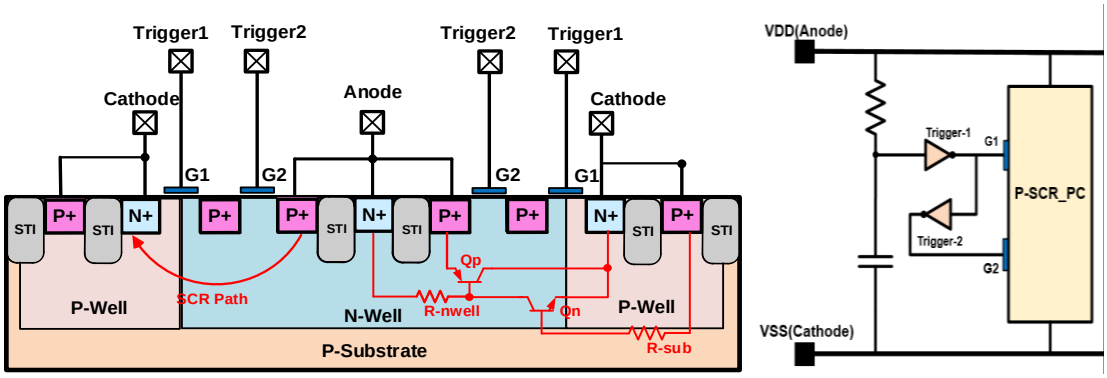


Fig. 3.17. The power-rail ESD clamp cell of fully-Silicide P-SCR_PC (Type A) combine ESD transient detection circuit in-28nm CMOS process.

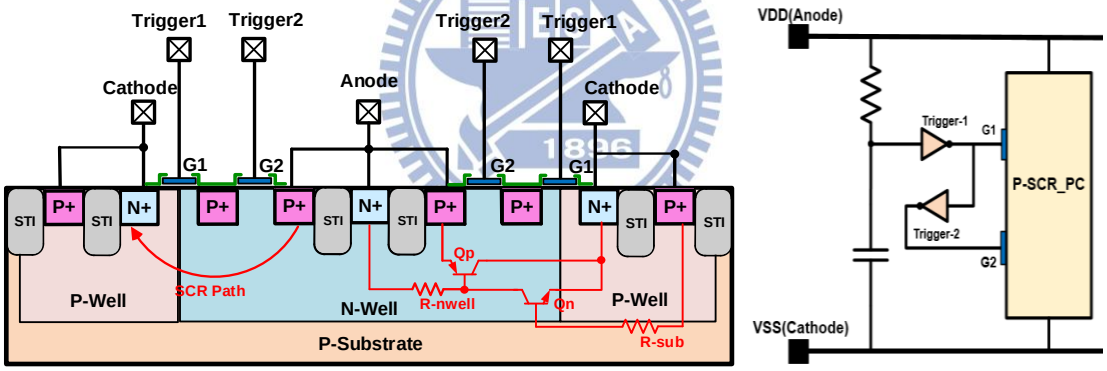
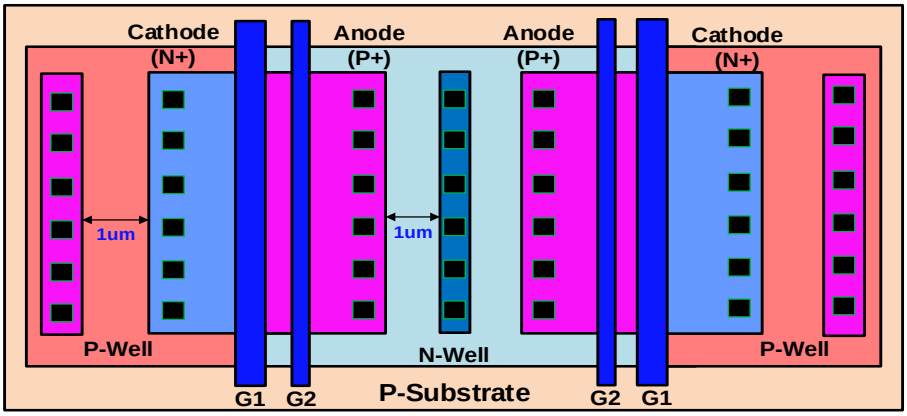
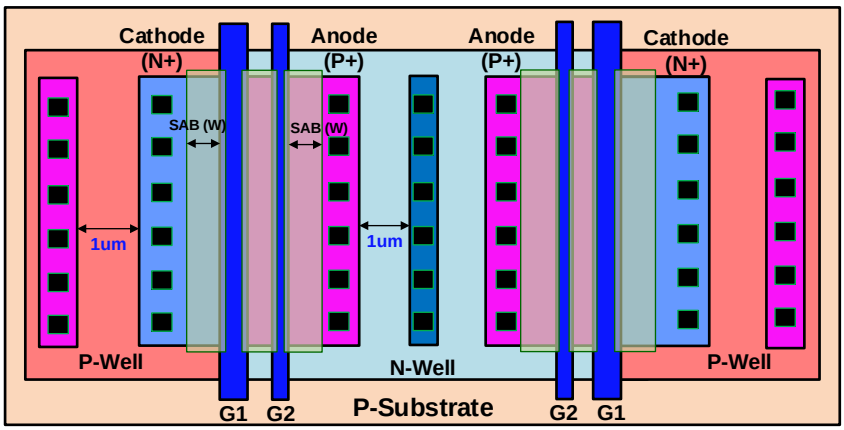


Fig. 3.18. The power-rail ESD clamp cell of non-Silicide P-SCR_PC (Type B) combine ESD transient detection circuit in-28nm CMOS process.



(a)



(b)

Fig. 3.19. The layout top view of P-SCR_PC device in-28nm CMOS process (a) Type A and (b) Type B.

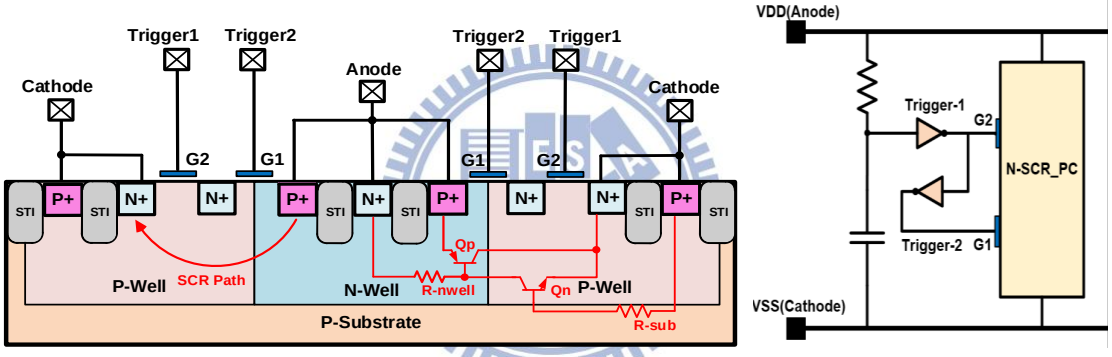


Fig. 3.20. The power-rail ESD clamp cell of fully-Silicide N-SCR_PC (Type A) combine ESD transient detection circuit in-28nm CMOS process.

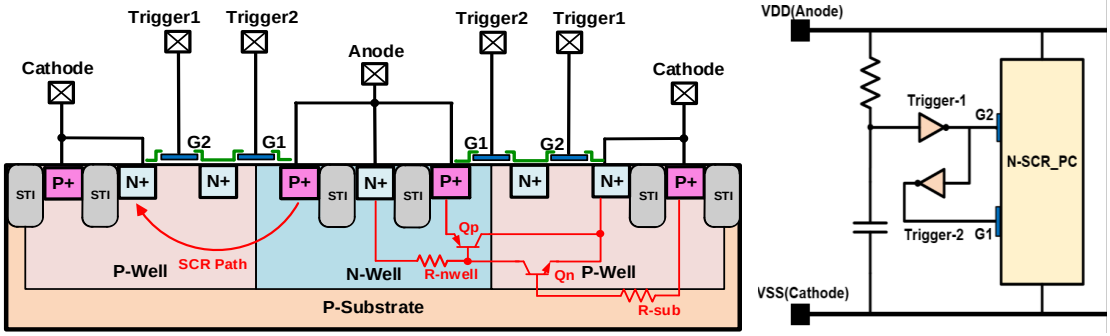
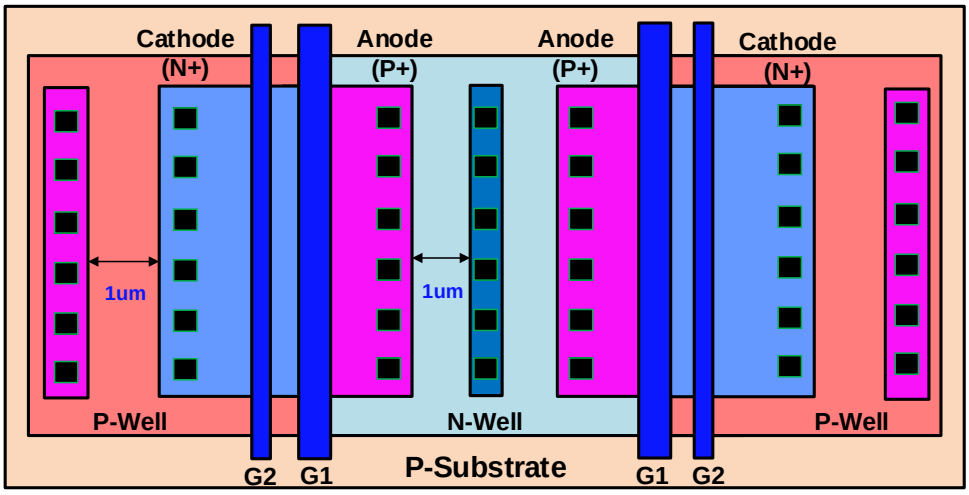
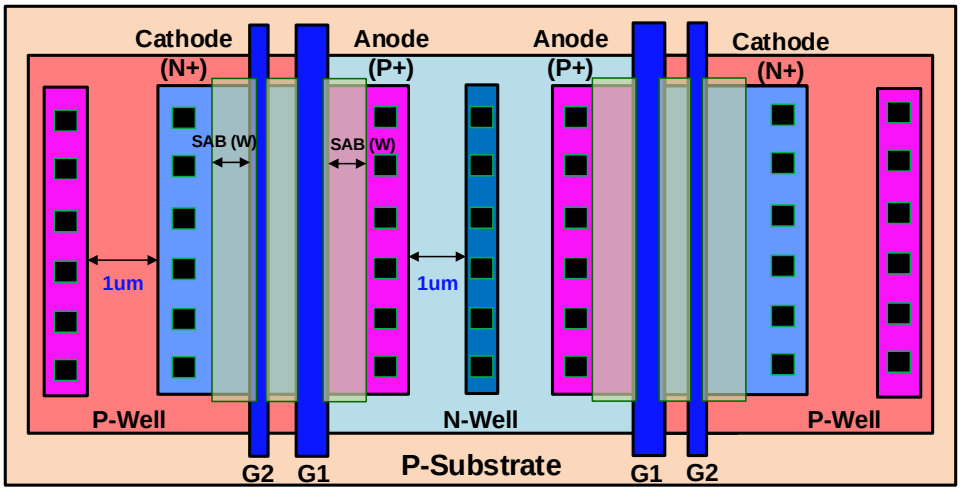


Fig. 3.21. The power-rail ESD clamp cell of non-Silicide N-SCR_PC (Type B) combine ESD transient detection circuit in-28nm CMOS process.



(a)



(b)

Fig. 3.22. The layout top view of N-SCR_PC in-28nm CMOS process.
(a) Type A and (b) Type B.

3.3.3 DC Characteristics and Leakage Current

After modifying the P-SCR_PC /N-SCR_PC devices, the large standby leakage current still exist in 28nm CMOS process without HKMG. According to the measurement result, leakage current may be induced by ESD transient detection circuit

Due to area efficiency, the MOS capacitor was often used in power-rail ESD clamp circuit. As following figure，with a leaky MOS capacitor, the PMOS (Mp) in the ESD detection circuit cannot be fully turned off, which causes another circuit

leakage path under normal circuit operating conditions. The thin gate oxide introduces large leakage currents through the gates, rendering previously used circuits almost useless because they used large transistors as capacitors.

Fig. 3.23 shows that gate leakage issue in ESD-detection circuit with NMOS capacitor. The gate leakage is the result of direct tunneling through the gate oxide. The tunneling effect is inherent to the MOSFET structure, and it has been studied in the early development of MOS transistors. Three kinds of tunneling mechanisms [33]-[35] were observed to explain the leakage in the CMOS. These mechanism are: ECB (electron tunneling from conduction band), EVB (electron tunneling from the valence band), and HVB (hole tunneling from valence band).

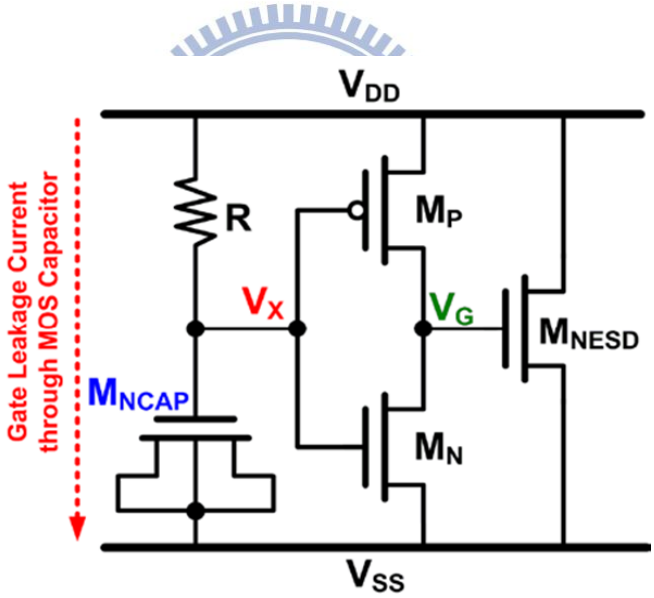


Fig. 3.23. Gate leakage issue in the traditional ESD-detection circuit with NMOS capacitor.

To determine whether proposed design have a correlation with leakage current, we design several methods to exemplify the results. Chapter 3.2 shows that proposed P-SCR_PC and N-SCR_PC devices have low standby leakage in 28nm HKMG CMOS process while proposed P-SCR_PC and N-SCR_PC devices have high standby leakage in 28nm CMOS process without HKMG. This result shows that the proposed design is

not main reason to cause leakage current. Under normal circuit operating condition, bias voltage are connected to P-SCR_PC (Type A) and N-SCR_PC (Type A). Fig. 3.24 is the result of leakage measurement of P-SCR_PC (Type A) and shows different standby leakage connecting with different gate-bias voltage. While VDD is 1.05 v, bias voltage of Gate-1 and Gate-2 are 0v and 1.05v, respectively. Leakage current still sustain on nano ampere even though VDD voltage increase from 0V to1.05V. When VDD is reach to worst case, 1.05 v, the highest leakage current is 3.07nA.

Fig. 3.25 is the result of leakage measurement of N-SCR_PC (Type A) and shows different standby leakage connecting different gate-bias voltage. While VDD is 1.05 v, bias voltage of Gate-1 and Gate-2 are 1.05v and 0v, respectively. Leakage current still sustain on nano ampere even though VDD voltage increase from 0V to1.05V. When VDD is reach to worst case, 1.05 v, the highest leakage current is 2.52nA.

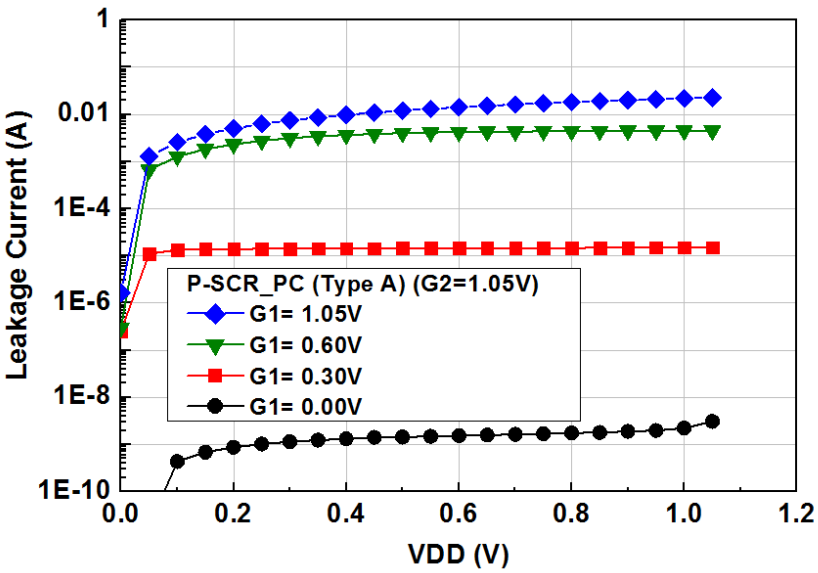


Fig. 3.24. The result of leakage measurement of P-SCR_PC (Type A) with different gate-bias voltage.

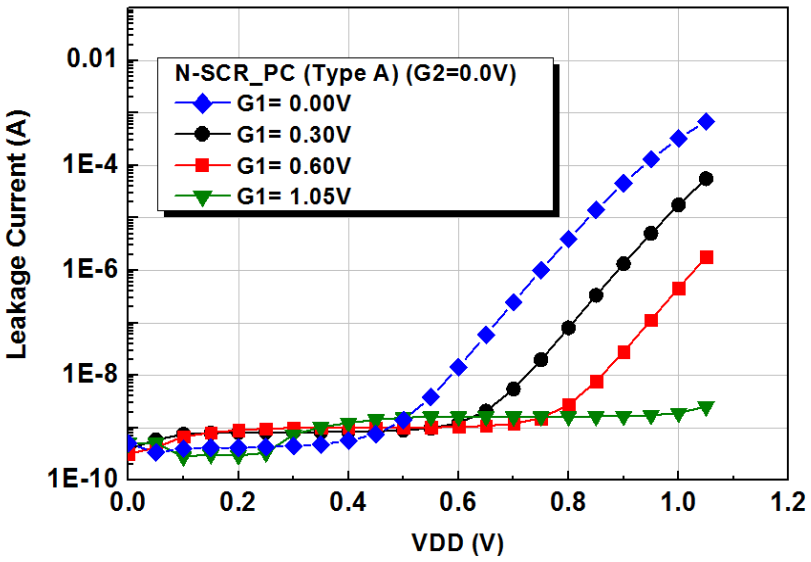


Fig. 3.25. The result of leakage measurement of N-SCR_PC (Type A) with different gate-bias voltage.

In traditional ESD transient detection circuit, the capacitors of NMOS cause the standby leakage having higher current in advanced process. From previous measurement, we can guarantee that the cause of leakage current do not come from mistake structure design. The following figure is focus on the packaged chips of P-SCR_PC (Type A) and N-SCR_PC (Type A) versus temperature to measure the change of leakage current. We heat the packaged chips of P-SCR_PC (Type A) and N-SCR_PC (Type A) in air isolation from 25℃ to 100℃ for half hour. In this condition, we implement this experiment and measure results.

Fig. 3.26 is the experimental result of the P-SCR_PC (Type A), and the device width is 120um. The leakage current are equal to 935nA and 1.3uA with 25 ℃ and 100℃, respectively; while 919nA and 1.27uA leakage current are separately equal to 25 degree and 100 degree for N-SCR_PC (Type A) structure. The experimental result of N-SCR_PC (Type A) device is shown in Fig. 3.27.

The leakage measurement of the test devices in a 28-nm CMOS process are listed in Table 3.2. We found that leakage current do not have any correlation with increasing

width but sustain constant leakage current. In other words, the cause of leakage current do not come from mistake structure design but MOS capacitors in advanced CMOS process influence the leakage current. The statistics exemplify the conclusion from following figures and tables.

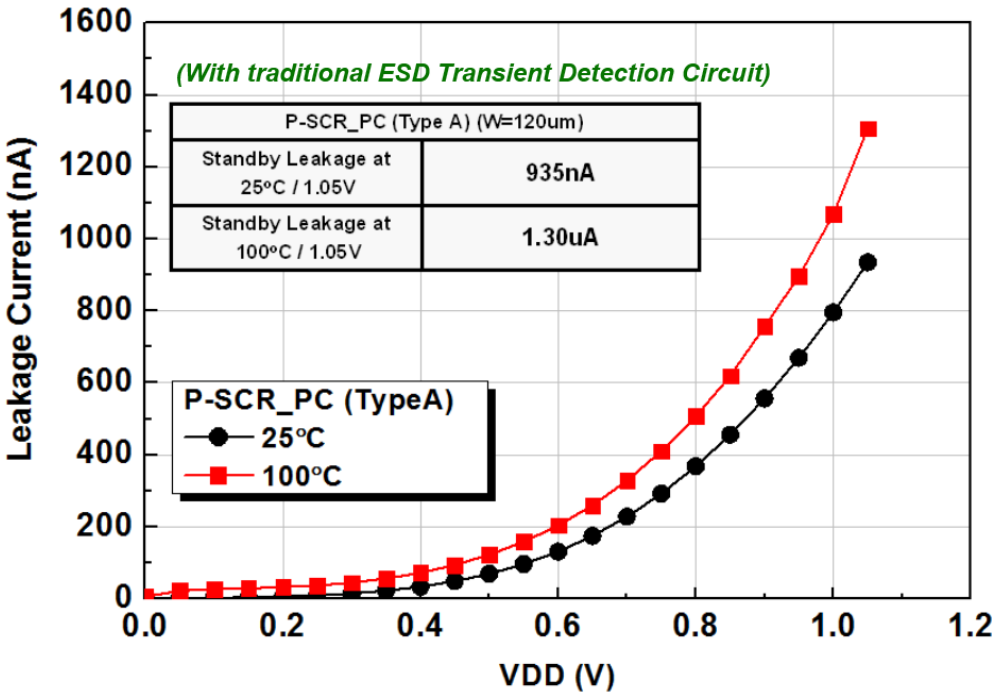


Fig. 3.26. The standby leakage of P-SCR_PC (Type A) with ESD transient detection circuit at different temperatures.

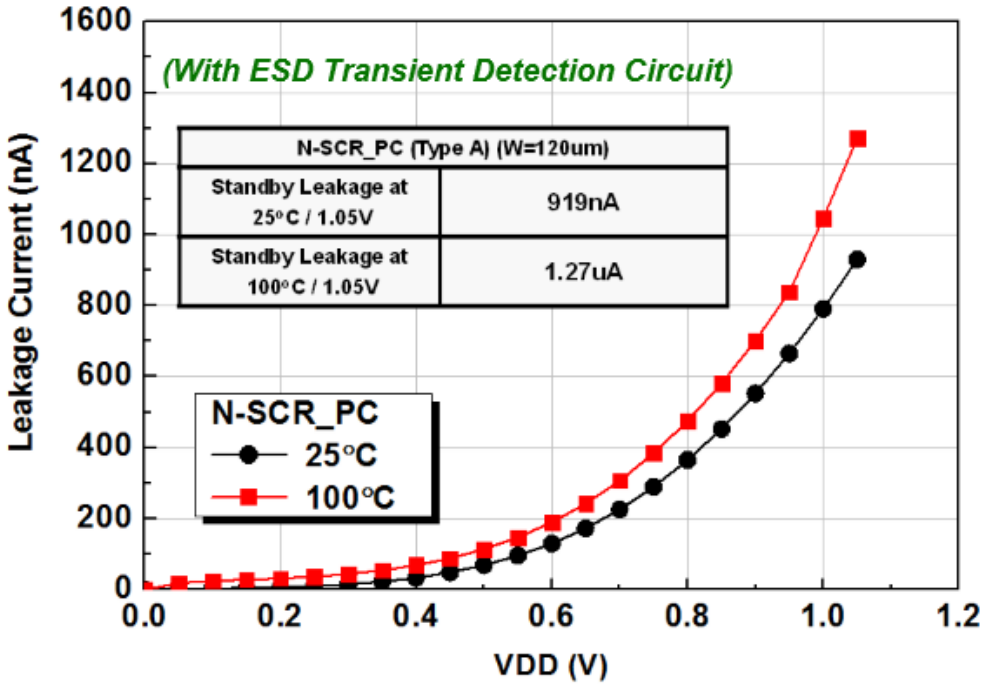


Fig. 3.27. The standby leakage of NSCR_PC (Type A) with ESD transient detection circuit at different temperatures.

Table 3.2 The leakage measurement data of the test devices with ESD transient detection circuit in 28-nm CMOS process.

	N-SCR_PC (Type A)	
CMOS Process	**28-nm CMOS Process**	
Temperature	**(25ºC / 1.05V)**	**(100ºC / 1.05V)**
Width=40um	902nA	1.17uA
Width=120um	919nA	1.27uA
Width=240um	921nA	1.31uA
Width=360um	937nA	1.34uA
	P-SCR_PC (Type A)	
CMOS Process	**28-nm CMOS Process**	
Temperature	**(25ºC / 1.05V)**	**(100ºC / 1.05V)**
Width=40um	912nA	1.21uA
Width=120um	935nA	1.30uA
Width=240um	944nA	1.34uA
Width=360um	965nA	1.41uA

3.3.4 TLP Characteristics

A. Prior Art

(a) Conventional SCR structure:

In conventional SCR structure, SCR path remains shallow trench isolation structure and turn-on mechanism which do not combine any trigger circuits. The TLP-measured I-V curves of conventional SCR devices are shown in Fig. 3.28. The devices width are 120μm, 240μm and 360μm, respectively. It2 are equal to 4A, 7.8A, 11.5A, respectively. Holding voltage are equal to 2.89V, 2.79V, and 3.02V, respectively. Trigger voltage are equal to 17.3V, 17.1V, 17.7V, respectively. We can see that It2 of conventional SCR is high enough to acquire a decent ESD robustness, but needs higher trigger voltage to turn on devices. Thus, conventional SCR device still needs to be modified.

The TLP-measurement data of the conventional SCR devices in a 28-nm CMOS process are listed in Table 3.3.

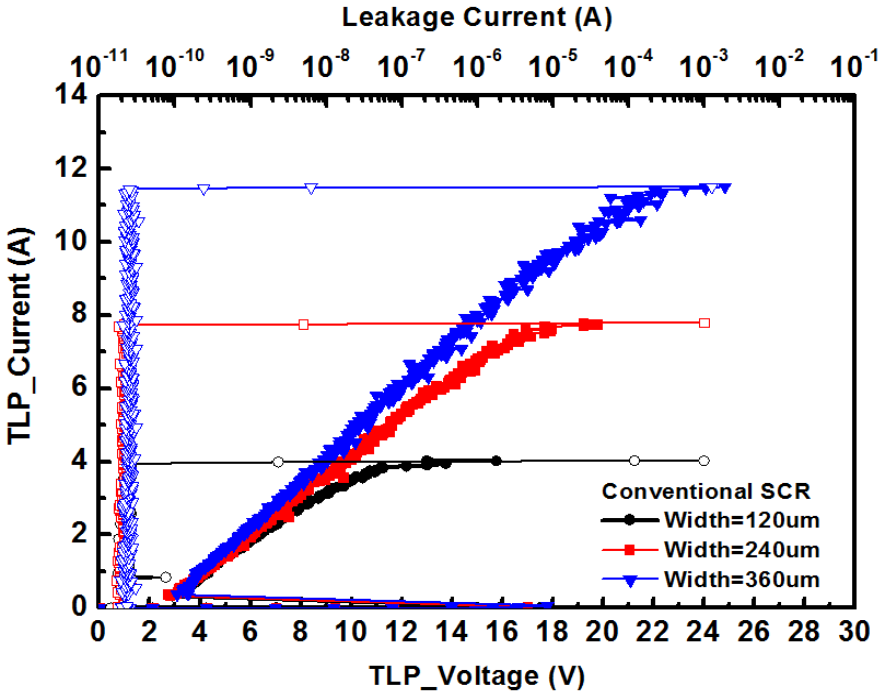


Fig. 3.28. TLP-measured I-V curves of Conventional SCR devices.

Table 3.3 The TLP-measurement data of the conventional SCR in 28-nm CMOS process.

Conventional SCR			
CMOS Process	**28-nm CMOS Process**		
Device Width	**W=120μm**	**W=240μm**	**W=360μm**
TLP Vt1	17.3V	17.1V	17.7V
TLP Vhold	2.89V	2.79V	3.02V
TLP It2	4.0A	7.8A	11.5A
Ron	2.4Ω	2.0Ω	1.8Ω
HBM ESD Robustness	6.2kV	>8kV	>8kV
MM ESD Robustness	250V	450V	500V

(b) Conventional Substrate Trigger SCR:

Conventional substrate trigger SCR add additional trigger node of P+ diffusion in the device structure. When ESD zapping, ESD transient detection circuit inserts current to node of P+ diffusion to enhance the voltage level of P-well and decrease breakdown voltage in parasitic SCR path. Trigger voltage can be easily turned on. In the trigger circuit, the RC time constant is 100ns, and the dimensions of PMOS and NMOS are 18μm and 9μm, respectively. The TLP-measured I-V curve of Conventional Substrate Trigger SCR devices are shown in Fig. 3.29. The devices width are 120um, 240um and 360um, respectively. It2 are equal to 4.3A, 8.1A, 12.3A, respectively. Holding voltage are equal to 2.48V, 2.42V, and 2.45V, respectively. Trigger voltage are equal to 4.0V, 4.4V, 4.7V, respectively. We can see that It2 of Conventional Substrate Trigger SCR devices with ESD transient detection circuit have a better performance than conventional SCR devices. The conventional substrate trigger SCR devices can sustain large ESD current because SCR parasitic path (P+/N-well/P-sub/N+) can be easily turn on. Trigger voltage is greatly lower compared to conventional SCR devices.

The TLP-measurement data of the conventional substrate trigger SCR in a 28-nm

CMOS process is listed in table 3.4.

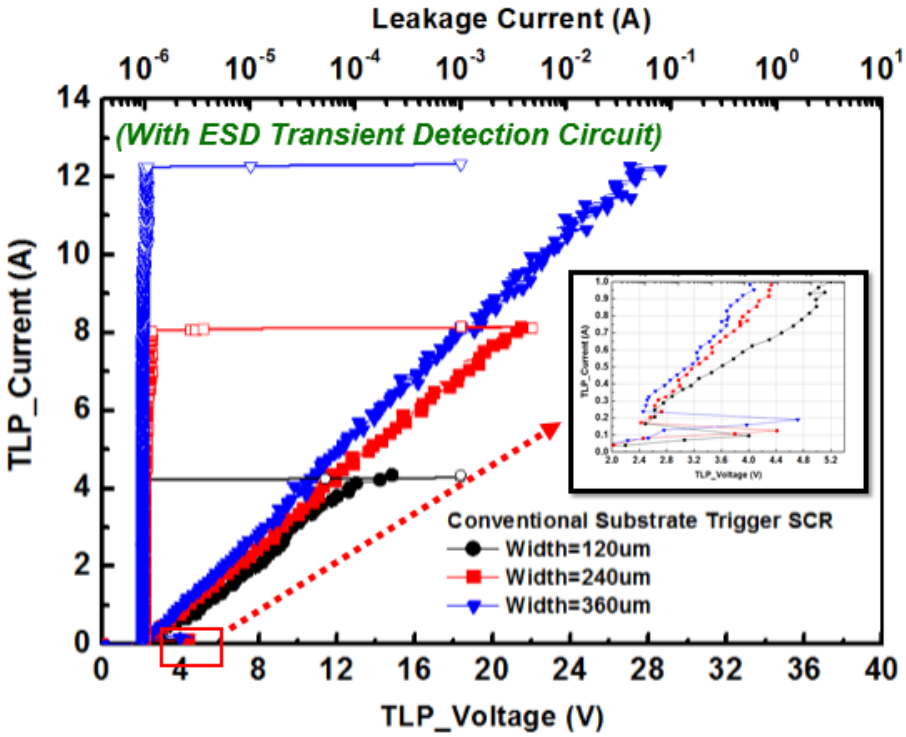


Fig. 3.29. TLP-measured I-V curves of Conventional Substrate trigger SCR devices.

Table 3.4 The TLP-measurement data of the conventional Substrate Trigger SCR in 28-nm CMOS process.

Conventional Substrate Trigger SCR			
CMOS Process	**28-nm CMOS Process**		
Device Width	**W=120μm**	**W=240μm**	**W=360μm**
TLP Vt1	4.0V	4.4V	4.7V
TLP Vhold	2.48V	2.42V	2.45V
TLP It2	4.3A	8.1A	12.3A
Ron	3.25Ω	2.3Ω	2.1Ω
HBM ESD Robustness	6.8kV	>8kV	>8kV
MM ESD Robustness	250V	400V	500V

B .Proposed design

(a) P-SCR_PC without ESD Transient Detection Circuit:

We separate two parts to compare. One is P-SCR_PC devices combine Trigger Circuit while the other one is P-SCR_PC without Trigger Circuit.

The TLP-measured I-V curves of P-SCR_PC (Type A) devices without trigger circuit are shown in Fig. 3.30. The device width is 120μm, 240μm and 360μm. It2 is equal to 4.8A, 9A, 13.1A, respectively. Holding voltage is equal to 3.13V, 3.23V and 3.15V, respectively. Trigger voltage is equal to 8.55V, 8.93V, 9.08V, respectively. Conventional SCR device turn-on voltage is roughly 17V. The trigger voltage of P-SCR_PC (Type A) is lower 10 V than the trigger voltage of Conventional SCR. Dummy gate can avoid to form the STI structure. Thus, parasitic length of SCR path is shorten and Trigger voltage can be improved.

The TLP-measured I-V curves of P-SCR_PC (Type B) devices are shown in Fig. 3.31. The device width is 120μm, 240μm and 360μm, respectively. It2 is equal to 5.3A, 10.3A, 13.9A, respectively. Holding voltage is equal to 1.95V, 2.06V and 1.97V, respectively. Trigger voltage is equal to 7.98V, 7.62V, 7.92V, respectively. From measurement results of Type-B, adding silicide blocking P-SCR_PC possesses low trigger voltage, holding voltage and turn-on resistance. The experience results conveys that when ESD zapping comes, additional silicide blocking can enhance Ballast resistance, easily turn on parasitic SCR (P+/N-well/P-sub/N+) path and enhance ESD robustness.

The TLP-measurement data of the P-SCR_PC without ESD transient detection circuit in a 28-nm CMOS process is listed in Table 3.5.

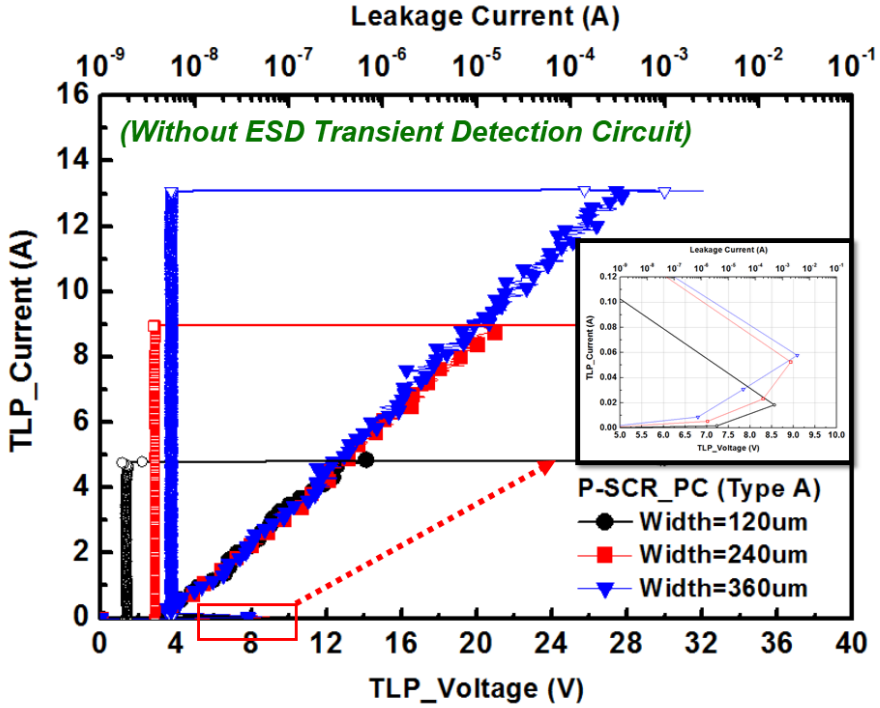


Fig. 3.30. TLP-measured I-V curves of P-SCR_PC (Type A) devices without ESD Transient Detection Circuit.

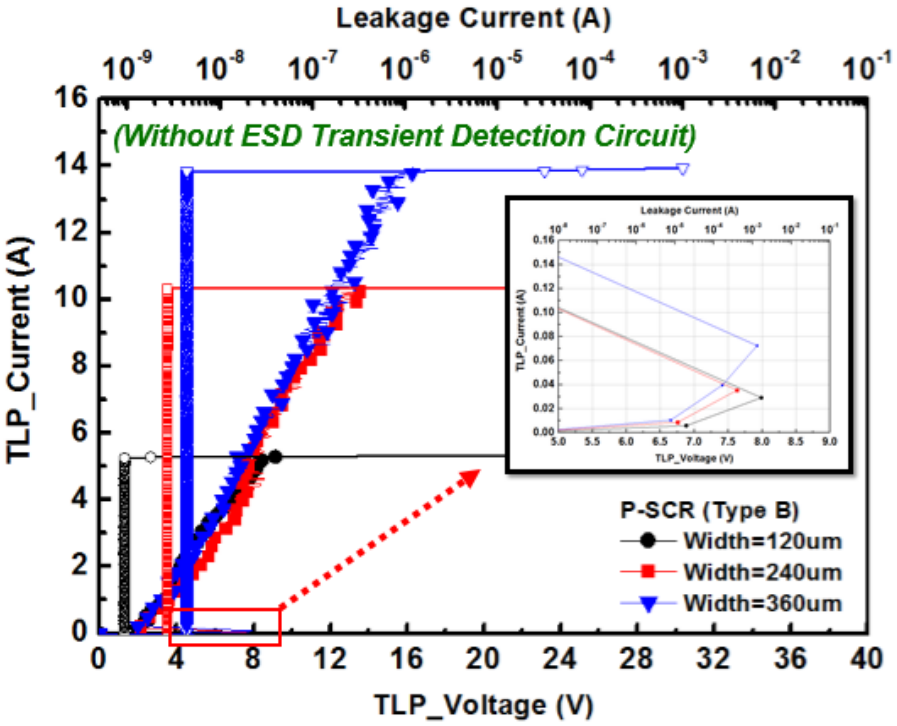


Fig. 3.31. TLP-measured I-V curves of P-SCR_PC (Type B) devices without ESD Transient Detection Circuit.

Table 3.5 The TLP-measurement data of the P-SCR_PC without ESD Transient Detection Circuit in a 28-nm CMOS process.

P-SCR_PC (Without ESD Transient Detection Circuit)						
	Type-A			Type-B		
CMOS Process	28-nm CMOS Process					
Device Width	W=120μm	W=240μm	W=360μm	W=120μm	W=240μm	W=360μm
TLP Vt1	8.55V	8.93V	9.08V	7.98V	7.62V	7.92V
TLP Vhold	3.13V	3.23V	3.15V	1.95V	2.06V	1.97V
TLP It2	4.8A	9.0A	13.1A	5.3A	10.3A	13.9A
Ron	2.4Ω	2.1Ω	2.5Ω	1.7Ω	1.7Ω	1.6Ω
HBM ESD Robustness	7.4kV	>8kV	>8kV	>8kV	>8kV	>8kV
MM ESD Robustness	300V	450V	550V	300V	500V	600V

(b) P-SCR_PC with ESD Transient Detection Circuit:

In order to acquire low trigger voltage in the proposed design of P-SCR_PC device, Type-A and Type-B combine the ESD transient detection circuit. In the trigger circuit, the RC time constant is 100ns, and the dimensions of PMOS and NMOS are 18μm and 9μm, respectively. The TLP-measured I-V curves of P–SCR_PC (Type A) devices are shown in Fig. 3.32. When TLP current is larger than 50mA, we define the measured voltage is trigger voltage. The devices width are 120μm, 240μm and 360μm, respectively. It2 are equal to 5.7A, 10.9A, 16.2A, respectively. Trigger voltage are equal to 1.64V, 1.56V and 1.46V, respectively. From above results, P-SCR_PC (Type A) combined with trigger circuit has a better ESD robustness. P-SCR_PC with trigger circuit has lower trigger voltage. Using gate control method usefully makes parasitic PNP and NPN turned on, forming Latch-up Positive feedback mechanism. Bypass ESD current can be released from latch-up positive feedback mechanism.

The TLP-measured I-V curves of P-SCR_PC (Type B) devices are shown in Fig. 3.33. The devices width are 120µm, 240µm and 360µm. It2 are equal to 5.7A, 10.9A, 16.4A, respectively. Trigger voltage are equal to 1.32V, 1.29V and 1.13V. We can found that the statistic of P-SCR_PC (Type-B) It2 is higher than type A, but trigger voltage is lower than type A. Adding silicide blocking can make parasitic SCR path turn on easily and enhance turn-on speed. Moreover, ESD level are improved.

The TLP-measurement data of the P-SCR_PC with ESD transient detection circuit in a 28-nm CMOS process is listed in Table 3.6.

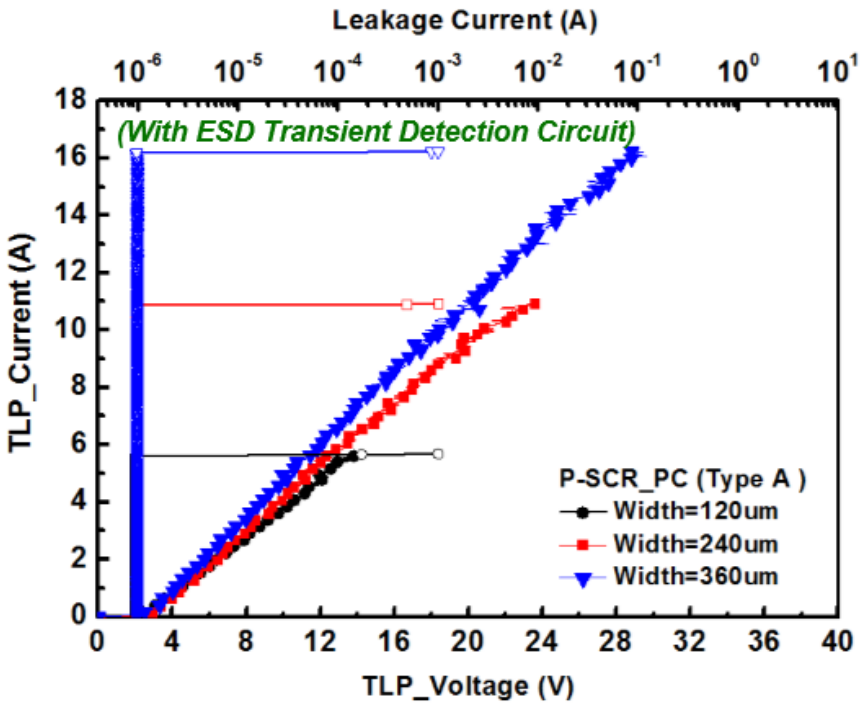


Fig. 3.32. TLP-measured I-V curves of P-SCR_PC (Type A) devices with ESD Transient Detection Circuit.

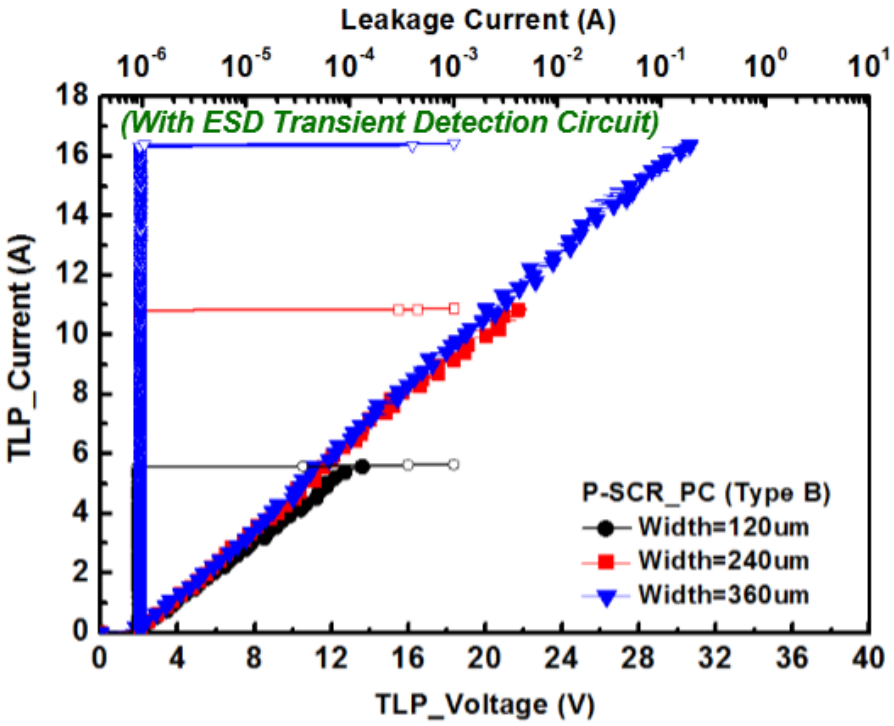


Fig. 3.33. TLP-measured I-V curves of P-SCR_PC (Type B) devices with ESD Transient Detection Circuit.

Table 3.6 The TLP-measurement data of the P-SCR_PC with ESD Transient Detection Circuit in a 28-nm CMOS process.

P-SCR_PC (With ESD Transient Detection Circuit)						
	Type-A			**Type-B**		
CMOS Process	**28-nm CMOS Process**					
Device Width	**W=120μm**	**W=240μm**	**W=360μm**	**W=120μm**	**W=240μm**	**W=360μm**
TLP Vt1	1.64V	1.56V	1.46V	1.32V	1.29V	1.13V
TLP Vhold	N/A	N/A	N/A	N/A	N/A	N/A
TLP It2	5.7A	10.9A	16.2A	5.7A	10.9A	16.4A
Ron	2.9Ω	2.7Ω	2.7Ω	2.4Ω	2.3Ω	2.4 Ω
HBM ESD Robustness	>8kV	>8kV	>8kV	>8kV	>8kV	>8kV
MM ESD Robustness	300V	450V	600V	300V	500V	650V

(c) N-SCR_PC without ESD Transient Detection Circuit:

We separate two parts to compare. One is N-SCR_PC devices combine Trigger Circuit while the other one is N-SCR_PC without Trigger Circuit.

The TLP-measured I-V curves of N-SCR_PC (Type A) devices without trigger circuit are shown in Fig. 3.34. The devices width are 120um, 240um and 360um, respectively. It2 are equal to 5.3A, 7.5A, 9.7A, respectively. Holding voltage are equal to 2.61V, 2.62V and 2.58V, respectively. Trigger voltage are equal to 6.70V, 7.23V, 7.32V, respectively. Conventional SCR device turn-on voltage is roughly 17V. The trigger voltage of N-SCR (Type-A) device is lower 10V than Conventional SCR device.

The TLP-measured I-V curves of N-SCR_PC (Type B) devices are shown in Fig. 3.35. The devices width are 120um, 240um and 360um, respectively. It2 are equal to 5.1A, 9.8A, 14.9A, respectively. Holding voltage are equal to 2.02V, 2.35V and 2.41V, respectively. Trigger voltage are equal to 6.52V, 7.33V, 7.42V, respectively. From measurement results of N-SCR_PC (Type B), adding silicide blocking N-SCR possesses can clamp lower holding voltage compared to N-SCR_PC (Type A). Moreover, N-SCR_PC (Type B) device also possesses lower trigger voltage and turn-on resistance. The experience results conveys that when ESD zapping, additional silicide blocking can enhance ballast resistance, easily turn on parasitic SCR (P+/N-well/P-sub/N+) path and enhance ESD Robustness. Meanwhile, devices turn on uniformly and It2 obviously enhances.

The TLP-measurement data of the N-SCR_PC without ESD transient detection circuit in a 28-nm CMOS process is listed in Table 3.7.

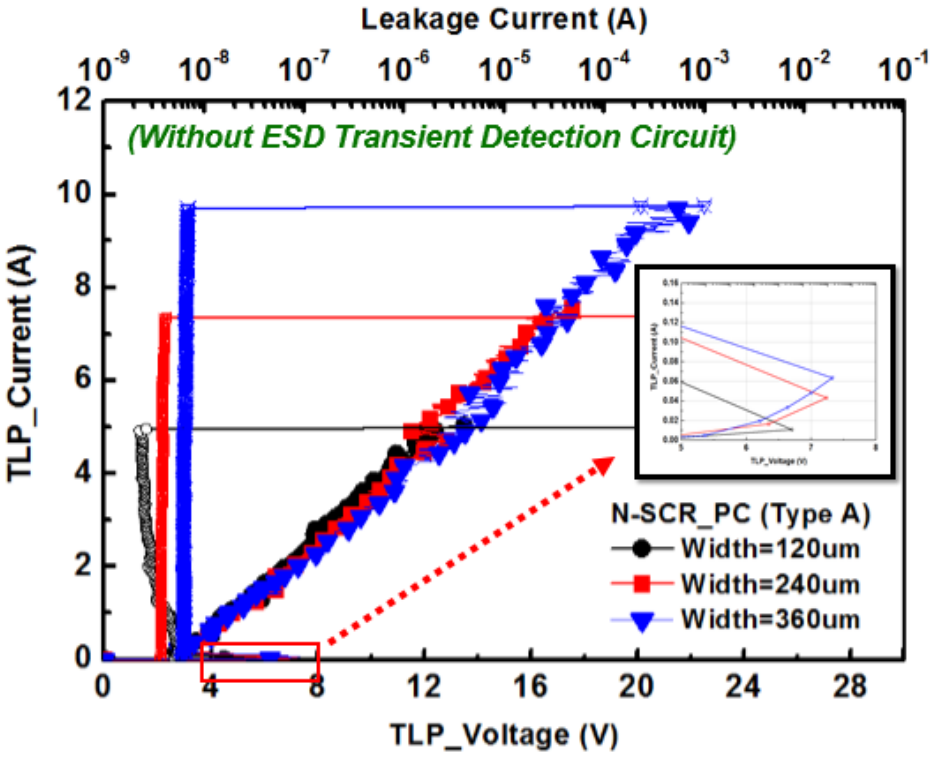


Fig. 3.34. TLP-measured I-V curves of N-SCR_PC (Type A) devices without ESD Transient Detection Circuit.

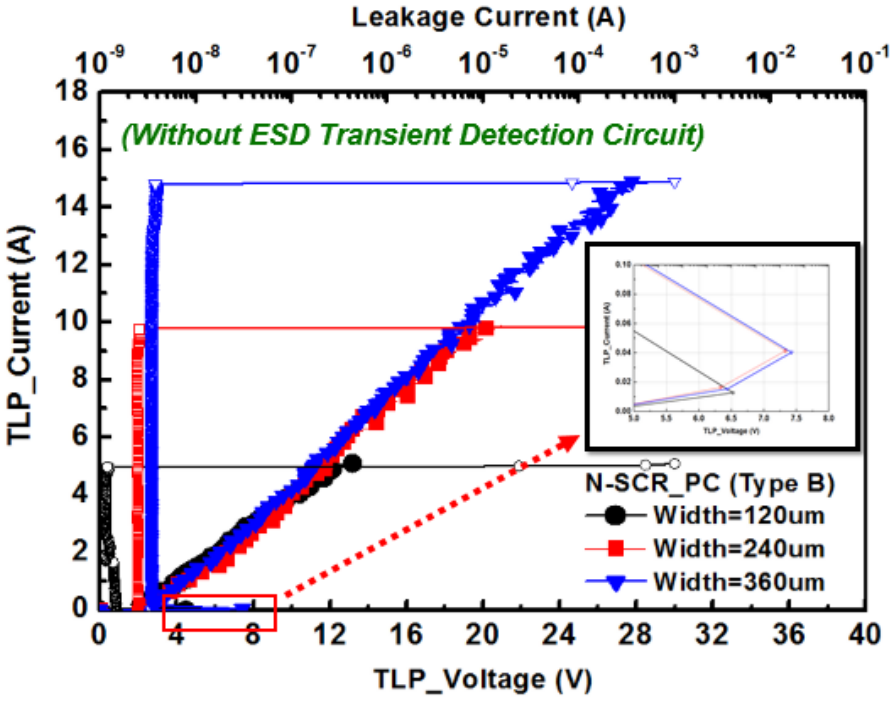


Fig. 3.35. TLP-measured I-V curves of N-SCR_PC (Type B) devices without ESD Transient Detection Circuit.

Table 3.7 The TLP-measurement data of the N-SCR_PC without ESD Transient Detection Circuit in a 28-nm CMOS process.

N-SCR_PC (Without ESD Transient Detection Circuit)						
	Type-A			Type-B		
CMOS Process	28-nm CMOS Process					
Device Width	W=120μm	W=240μm	W=360μm	W=120μm	W=240μm	W=360μm
TLP Vt1	6.70V	7.23V	7.32V	6.52V	7.33V	7.42V
TLP Vhold	2.61V	2.62V	2.58V	2.02V	2.35V	2.41V
TLP It2	5.3A	7.5A	9.7A	5.1A	9.8A	14.9A
Ron	2.4Ω	2.7Ω	2.3Ω	2.3Ω	1.9Ω	2.0Ω
HBM ESD Robustness	>8kV	>8kV	>8kV	>8kV	>8kV	>8kV
MM ESD Robustness	300V	450V	550V	300V	500V	600V

(d) N-SCR_PC with ESD Transient Detection Circuit:

In order to acquire low trigger voltage in the proposed design of N-SCR_PC device, Type-A and Type-B combine the ESD transient detection circuit. In the trigger circuit, the RC time constant is 100ns, and the dimensions of PMOS and NMOS are 18μm and 9μm, respectively. The TLP-measured I-V curves of N-SCR_PC (Type A) devices are shown in Fig. 3.36. When TLP current is larger than 50mA, we define the measured voltage is trigger voltage. The devices width are 120um, 240um and 360um, respectively. It2 are equal to 5.2A, 9.9A, 14.8A, respectively. Trigger voltage are equal to 2.12V, 1.85V and 2.13V, respectively. From above results, N-SCR_PC (Type A) combined with trigger circuit has a better ESD robustness. N-SCR_PC (Type A) with trigger circuit has lower trigger voltage. Using gate control method usefully makes parasitic SCR path turned on, forming latch-up positive feedback mechanism. Bypass ESD current can be released from Latch-up positive feedback mechanism.

The TLP-measured I-V curves of N-SCR_PC (Type B) devices are shown in Fig.

3.37. The devices width are 120µm, 240µm and 360µm, respectively. It2 are equal to 5.3A, 10.1A, 15.6A, respectively. Trigger voltage are equal to 1.97V, 1.85V and 2.15V, respectively. We can found that the statistic of N-SCR_PC (Type B) It2 and MM ESD level have better performance compared to N-SCR_PC (Type A).

The TLP-measurement data of the N-SCR_PC devices with ESD transient detection circuit in a 28-nm CMOS process are listed in Table 3.8.

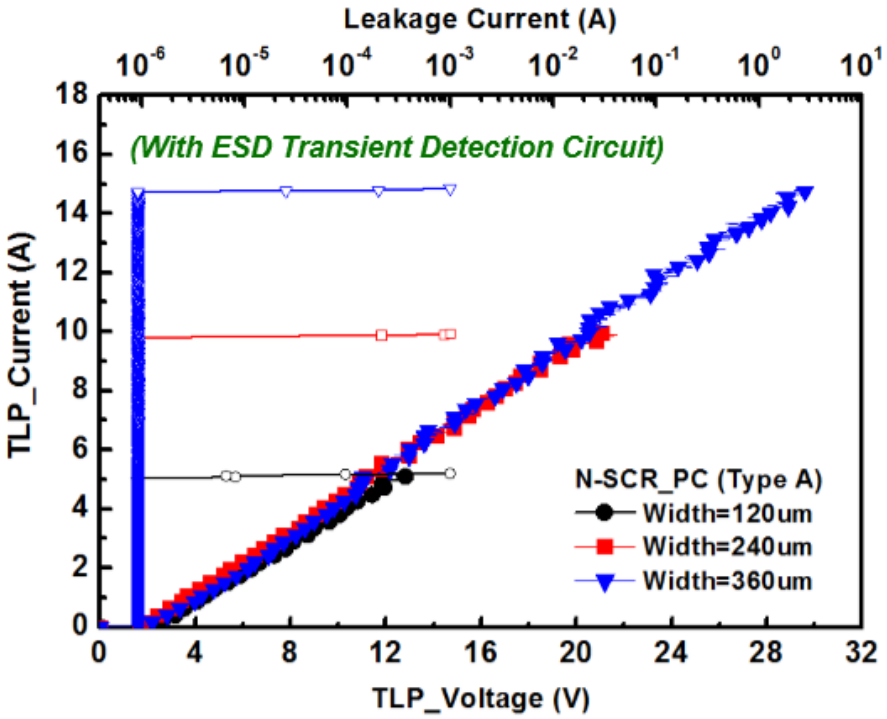


Fig. 3.36. TLP-measured I-V curves of N-SCR_PC (Type A) devices with ESD Transient Detection Circuit.

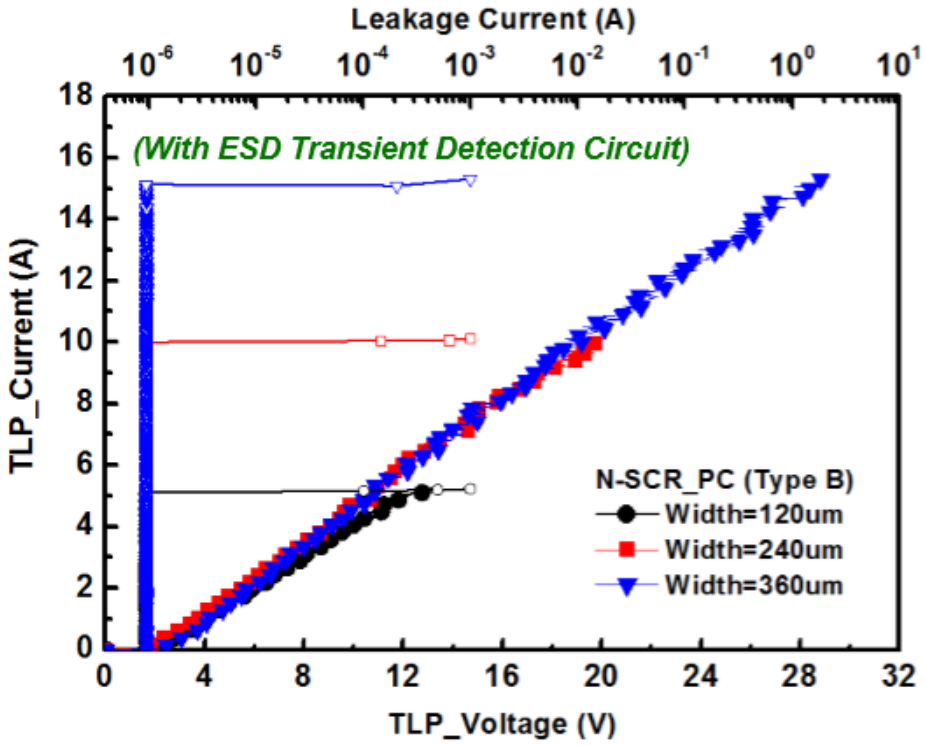


Fig. 3.37. TLP-measured I-V curves of N-SCR_PC (Type B) devices with ESD Transient Detection Circuit.

Table 3.8 The TLP-measurement data of the N-SCR_PC with ESD Transient Detection Circuit in 28-nm CMOS process.

N-SCR_PC (With ESD Transient Detection Circuit)						
	Type-A			**Type-B**		
CMOS Process	**28-nm CMOS Process**					
Device Width	**W=120μm**	**W=240μm**	**W=360μm**	**W=120μm**	**W=240μm**	**W=360μm**
TLP Vt1	2.12V	1.85V	2.13V	1.97V	1.85V	2.15V
TLP Vhold	N/A	N/A	N/A	N/A	N/A	N/A
TLP It2	5.2A	9.9A	14.8A	5.3A	10.1A	15.6A
Ron	2.2Ω	1.8Ω	2.4Ω	2.1Ω	1.8Ω	1.9Ω
HBM ESD Robustness	>8kV	>8kV	>8kV	>8kV	>8kV	>8kV
MM ESD Robustness	300V	500V	650V	300V	550V	700V

3.3.5 VF-TLP Characteristics

In traditional ESD measurement, we usually use TLP system to test. TLP system generate pulse which rise time is 10ns, Pulse width is 100ns and simulate the parameters of discharge waveform of Human body model.

As advanced process is scaling down, ESD sensitivity is increasing. To adapt faster ESD discharge current such as charge device model (CDM), we should use Very-Fast TLP System generate pulse which Rise time is 0.2ns, Pulse width is 5ns to implement discharging test.

In this chapter, we compare P-SCR_PC, N-SCR_PC, conventional substrate trigger SCR (ST-SCR) and conventional SCR by using VF-TLP to measure each device of ESD Robustness. Those devices are combined with the same trigger circuit to compare one another. The devices width are equal to 40um and 120um, respectively. Our proposed design is focus on the influence of ESD robustness and turn-on speed by adjusting SAB width parameters.

The VF-TLP measured I-V curves of the conventional SCR device are shown in Fig. 3.38. The conventional SCR device with 40-μm and 120-μm widths can achieve the VF-TLP -measured It2 of 2.98A and 9.66A, respectively. However, the trigger voltage of conventional SCR needs at least 16V to turn on device. The VF-TLP-measured I-V curves of the ST-SCR devices are shown in Fig 3.39. The VF-TLP-measured It2 of the ST-SCR devices with 40-μm and 120-μm width are only 1.10A and 1.72A, respectively. The measurement of It2 results show that the ST-SCR devices are not enough to be turned on under fast CDM-like ESD-transient events.

P-SCR_PC device VF-TLP versus IV curve measurement is shown in Fig 3.40. Without Silicide blocking, P-SCR device width is 40um. VF-TLP system shows that It2 is 3.2A. Compared to conventional ST-SCR device (It2 = 1.1A), It2 is higher. The proposed device structure (P-SCR_PC) possesses a better turn-on speed.

The proposed devices (P-SCR_PC) in the same area and width are also looking for different silicide blocking (SAB) width. In Fig. 3.41, we can found that width of SAB spacing in P-SCR_PC device is 0um, 0.2um and 0.4um, respectively. From VF-TLP measurement results, Vt1 is separate to 2.00V, 1.84V and 1.81V. The voltage of Vt1 would decrease as SAB width increase. On the other hand, we also find the uniform turn-on characteristic and turn-on speed on ESD robustness. The It2 of proposed P-SCR_PC device is equal to 3.22A, 3.43A and 4.07A, respectively. Under the same size of devices, changing SAB width can make VF-TLP It2 improve roughly 1A. Holding voltage also decreases from 1.83V to 1.72V. While device width is 120um, the power clamp cell of It2 can increase from 9.3A to 11.5A and its result can be observed clearly in Fig. 3.42.

The proposed design N-SCR_PC Device VF-TLP versus IV curve measurement is shown in Fig. 3.43. The proposed devices (N-SCR_PC) in the same area and width are also looking for different silicide blocking (SAB) width. In Fig.3.43 and Fig. 3.44, we can found that width of SAB spacing in N-SCR_PC device is 0um, 0.2um and 0.4um, respectively. From VF-TLP measurement results, Vt1 is separate to 1.69 V, 1.63V and 1.60V. The voltage of Vt1 would decrease as SAB width increase. On the other hand, we also find the uniform turn-on characteristic and turn-on speed on ESD robustness. The It2 of proposed N-SCR_PC device is equal to 3.25, 3.49 and 3.72, respectively. While device width is 120um, the power clamp cell of It2 can increase from 8.9A to 10.8A and its result can be observed clearly in Fig. 3.45. Adding silicide blocking method to optimize devices can enhance ESD level.

The VF-TLP-measurement data of test devices in a 28-nm CMOS process are listed in Table 3.9.

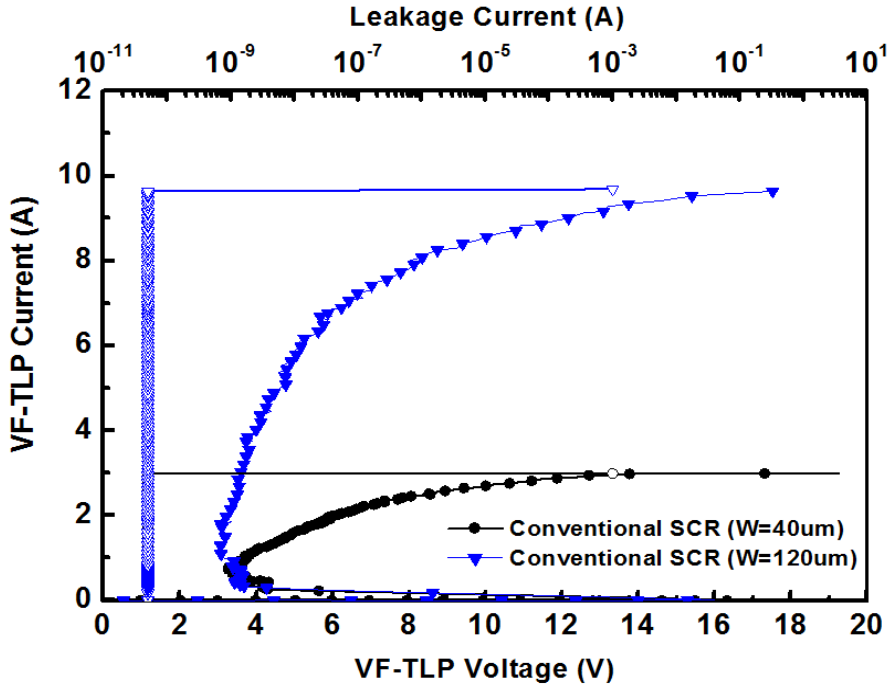


Fig. 3.38 VF-TLP-measured I-V curves of conventional SCRs.

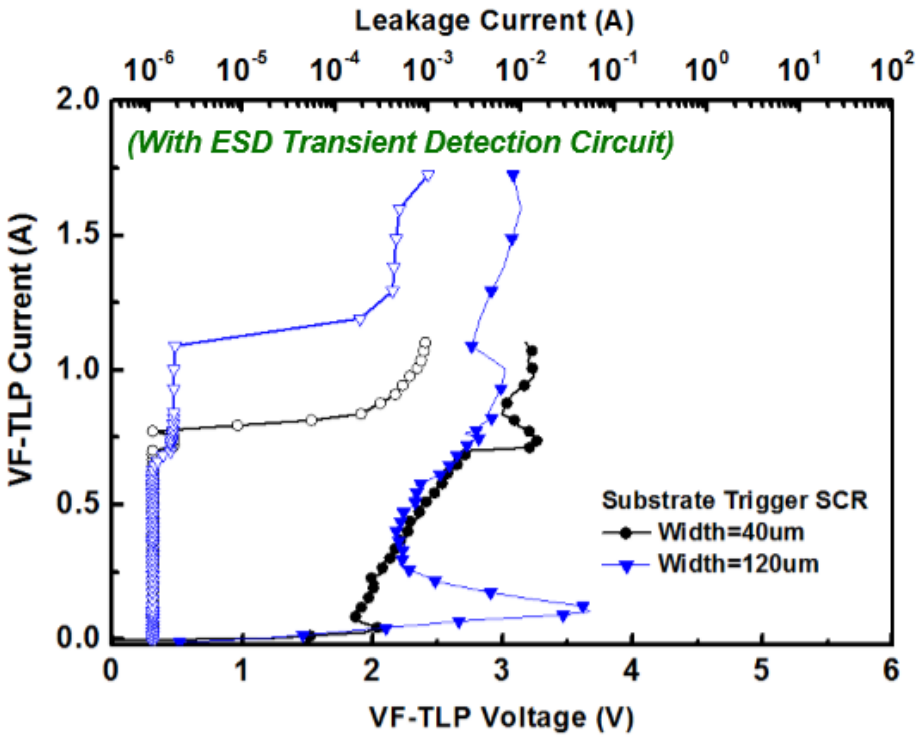


Fig. 3.39. VF-TLP-measured I-V curves of Substrate trigger SCRs.

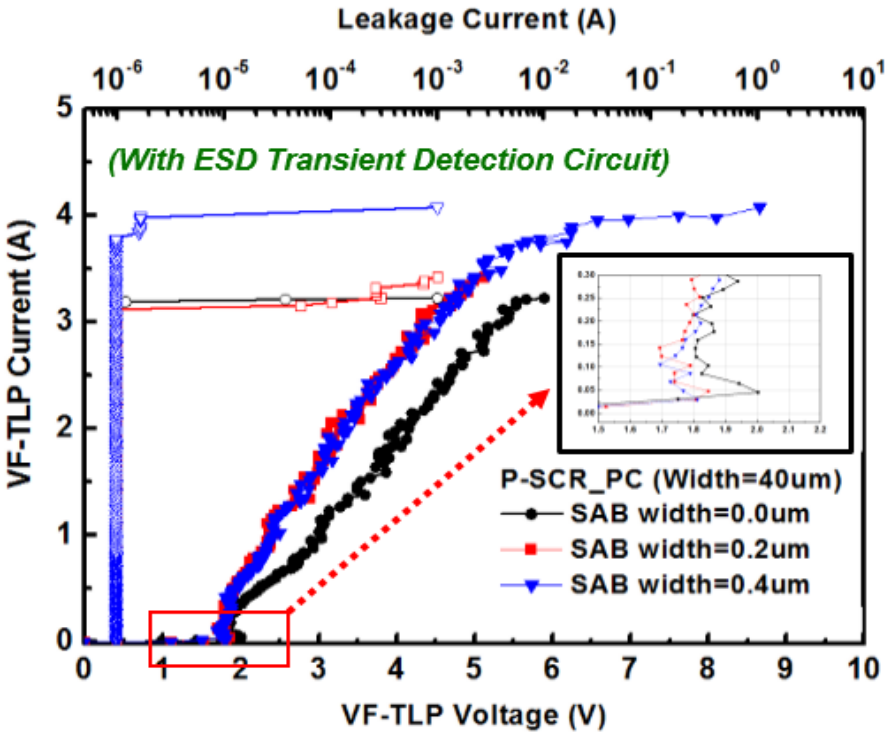


Fig 3.40. VF-TLP-measured I-V curves of P-SCR_PC (W=40μm) devices with ESD Transient Detection Circuit.

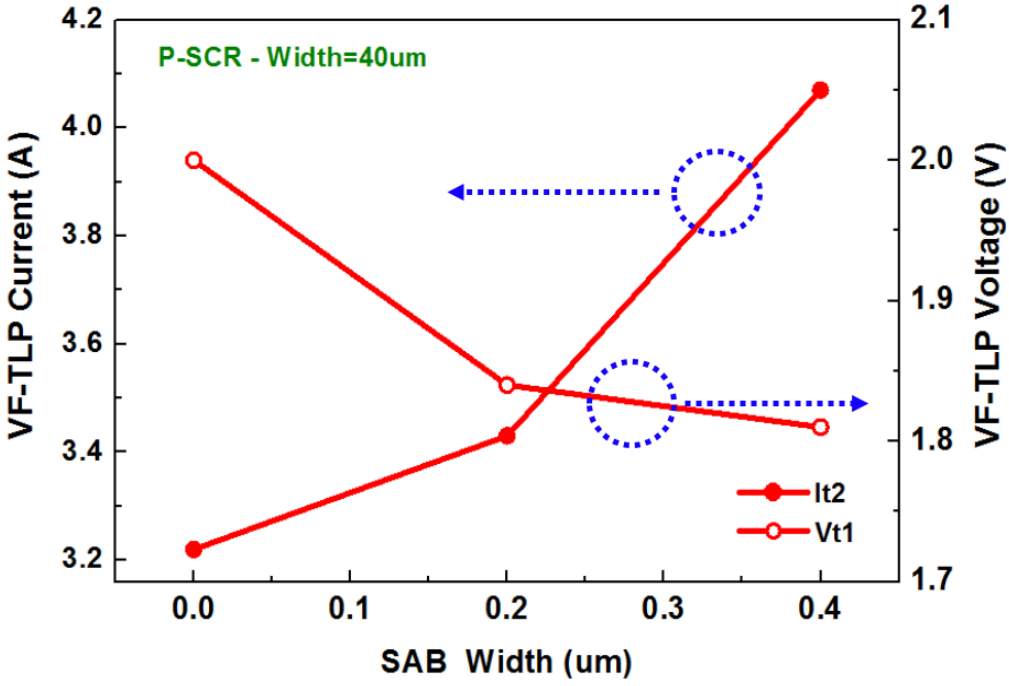


Fig. 3.41. The relationship between VF_TLP Current and VF_TLP Voltage with various SAB Width.

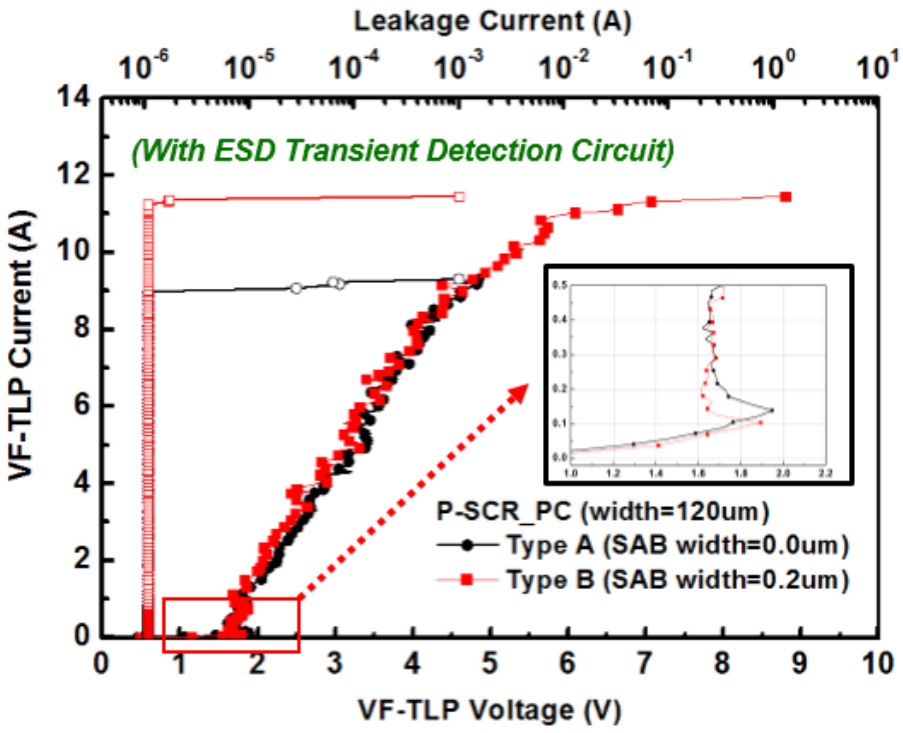


Fig. 3.42. VF-TLP-measured I-V curves of P-SCR_PC devices (w=120μm) with ESD Transient Detection Circuit.

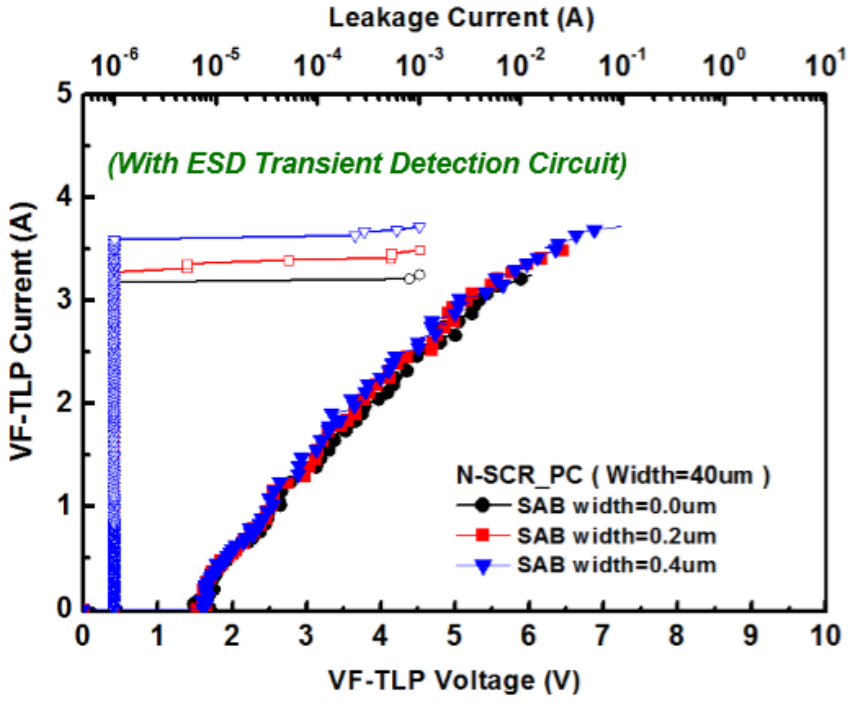


Fig. 3.43. VF-TLP-measured I-V curves of N-SCR_PC (w=40μm) devices with ESD Transient Detection Circuit.

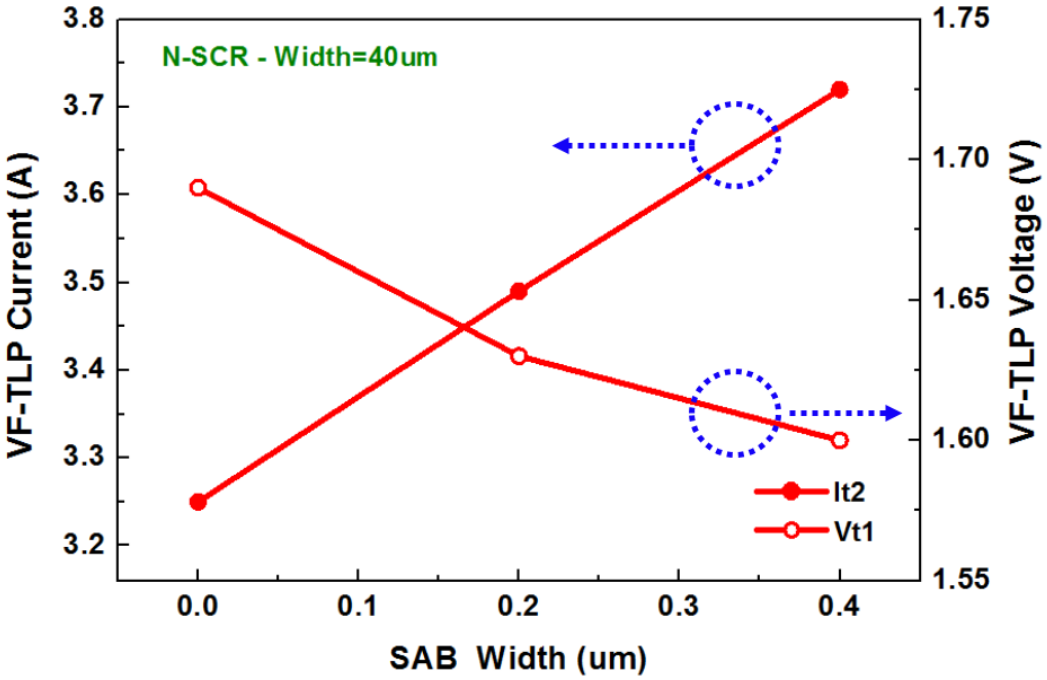


Fig. 3.44 The relationship between VF_TLP Current and VF_TLP Voltage with various SAB Width.

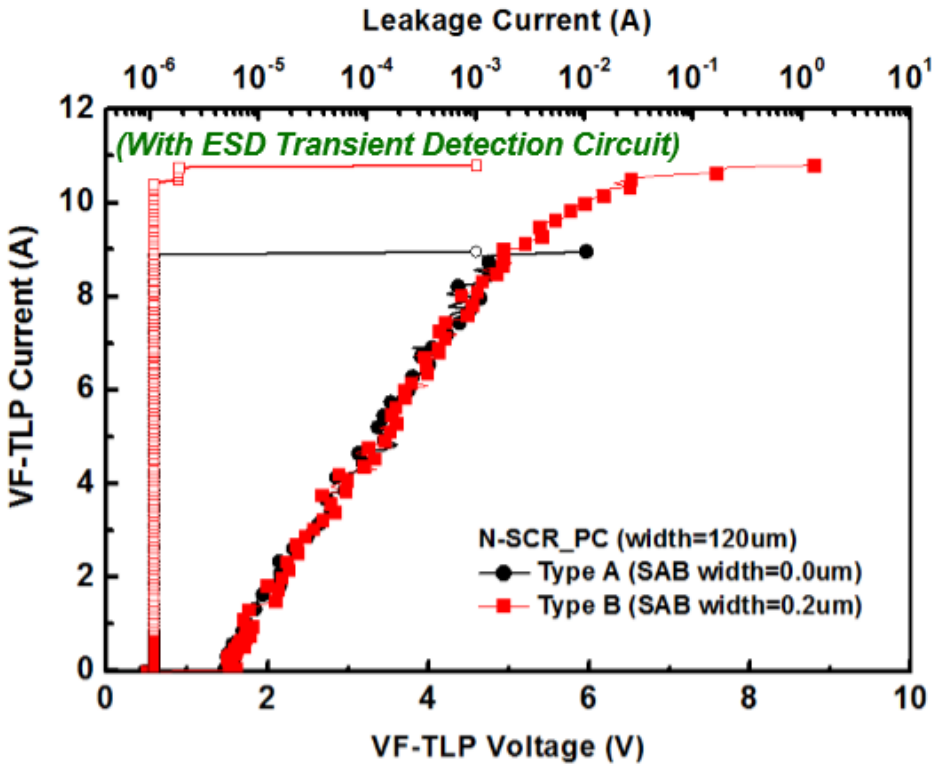


Fig. 3.45. VF-TLP-measured I-V curves of N-SCR_PC (W=120um) devices with ESD Transient Detection Circuit.

Table 3.9 The VF-TLP-measurement data of test devices in a 28-nm CMOS process.

VF-TLP					
	Device width	**SAB Width**	**VF-TLP Vt1**	**VF-TLP Vhold**	**VF-TLP It2**
Conventional SCR	40μm	0μm	16.7V	5.64V	2.98A
	120μm	0μm	15.9V	5.66V	9.66A
ST-SCR	40μm	0μm	2.06V	1.86V	1.10A
	120μm	0μm	3.61V	2.27V	1.72A
P-SCR_PC	40μm	0μm	2.00V	1.83V	3.22A
	40μm	0.2μm	1.84V	1.73V	3.43A
	40μm	0.4μm	1.81V	1.72V	4.07A
	120μm	0μm	1.94V	1.74V	9.3A
	120μm	0.2μm	1.89V	1.64V	11.5A
N-SCR_PC	40μm	0μm	1.69V	N/A	3.25A
	40μm	0.2μm	1.63V	N/A	3.49A
	40μm	0.4μm	1.60V	N/A	3.72A
	120μm	0μm	1.62V	N/A	8.9A
	120μm	0.2μm	1.60V	N/A	10.8A

3.3.6 ESD Robustness and System-Level ESD test

In this chapter 3.3.6, we use different ESD test model including HBM test, MM test and System-Level ESD test to measure ESD robustness. According to the measurement results, the proposed device of fully silicide P-SCR_PC (Type A) with 120um width can pass 7.4-kV HBM ESD test. P-SCR_PC (Type B) with 120um width can make HBM robustness higher than 8-kV HBM

For other measurement results, the width of N-SCR_PC device is equal to 120um. N-SCR (Type A) and non-silicide N-SCR_PC (Type B) can pass 8kV HBM ESD tests. Conventional SCR and substrate trigger SCR can pass HBM ESD tests with 6.2kV and 6.8kV, respectively.

From previous published reference [32] in 28nm HKMG CMOS Process, GGNMOS can pass 1.5-kV and 3.5-kV HBM ESD tests, respectively, but GDPMOS

cannot pass 0.5-kV HBM ESD tests.

In MM ESD test, the width of P-SCR_PC devices and N-SCR_PC devices are equal to 360 um. P-SCR_PC (Type A) can pass 550V MM ESD test; P-SCR_PC (Type B) can pass 600V MM ESD tests. N-SCR_PC (Type A) can pass 500V MM ESD test; N-SCR_PC can pass 600V MM ESD test. From above results, Non-Silicide SCR (type B) devices have better ESD robustness on MM mode ESD test compared to fully silicide SCR (Type A) devices.

According to IEC 61000-4-2, two test modes have been specified, which are the air-discharge and contact-discharge test mode.

The proposed non-Silicide P-SCR (type B) and non-Silicide N-SCR (Type B) with 360-μm width can pass 8-kV in contact-discharge test mode. And 15-kV in air-discharge test mode

3.3.7 Trigger Mechanism

Additional trigger pads are connected to Gate-1 and Gate-2, as shown in Fig. 3.46 and Fig. 3.47. The purpose of these two structures is to investigate the influence between the bias voltage and the trigger voltage. The DC bias voltage is connected to Gate as bias voltage. Fig.3.48 exhibits the measurement setup. Power supply Agilent B2902A provide voltage for the gates of proposed device. TLP System tests proposed device. Fig. 3.49 and Fig. 3.50 demonstrate the TLP-measured I-V curve of the P-SCR_PC (Type B) and N-SCR_PC (Type B).

TLP I-V curves of P-SCR_PC (Type B) trigger voltage are shown in Fig. 3.49. As bias voltage of Gate-1 increases, the region of Gate-1 in P-well gradually forms an electron inversion and n-channel. Trigger voltage of P-SCR_PC (Type B) device becomes small.

TLP I-V curve of N-SCR_PC (Type B) trigger voltage is shown in Fig. 3.50. As bias voltage of Gate-1 reduces, the region of Gate-1 in N-well gradually formulas a hole inversion and p-channel. Trigger voltage of N-SCR_PC (Type B) turns into small. The relation of devices between gate voltage and trigger voltage are listed in Table 3.10.

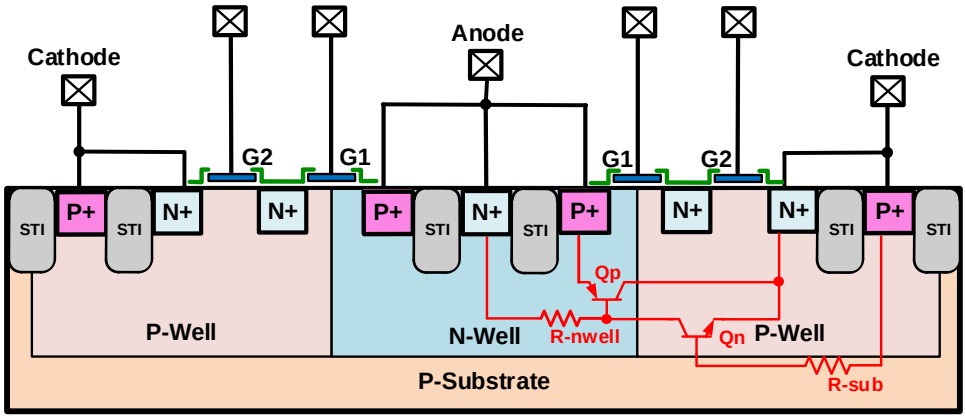


Fig. 3.46. The power-rail ESD clamp cell of P-SCR_PC (Type B).

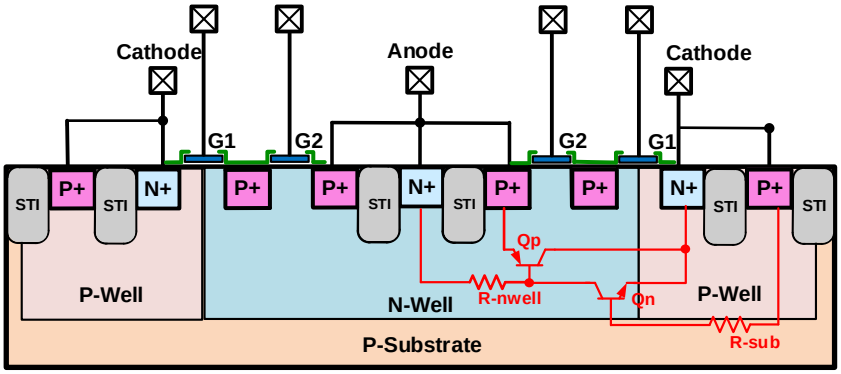


Fig. 3.47. The power-rail ESD clamp cell of N-SCR_PC (Type B).

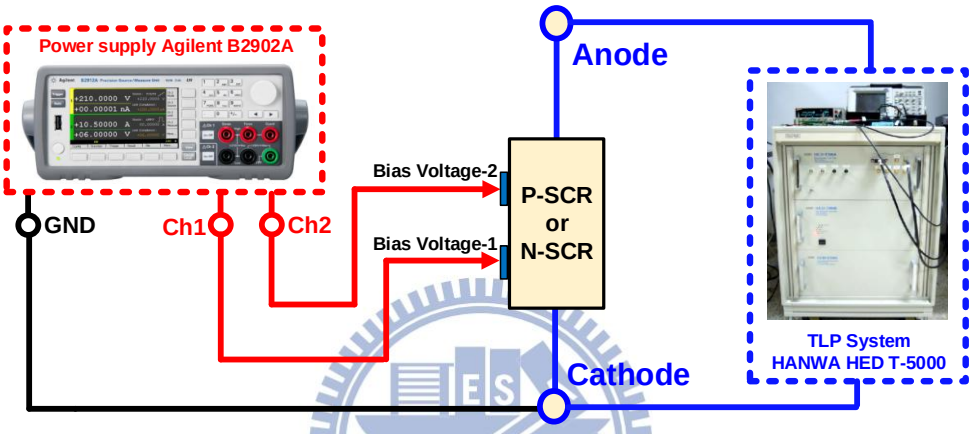


Fig. 3.48. Measurement setup of trigger mechanism test.

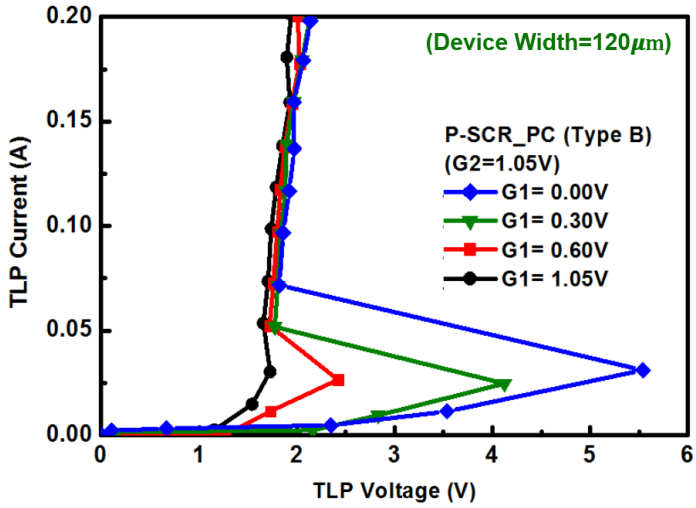


Fig. 3.49. TLP-measured I-V curves of P-SCR_PC (Type B) with different gate-bias voltage.

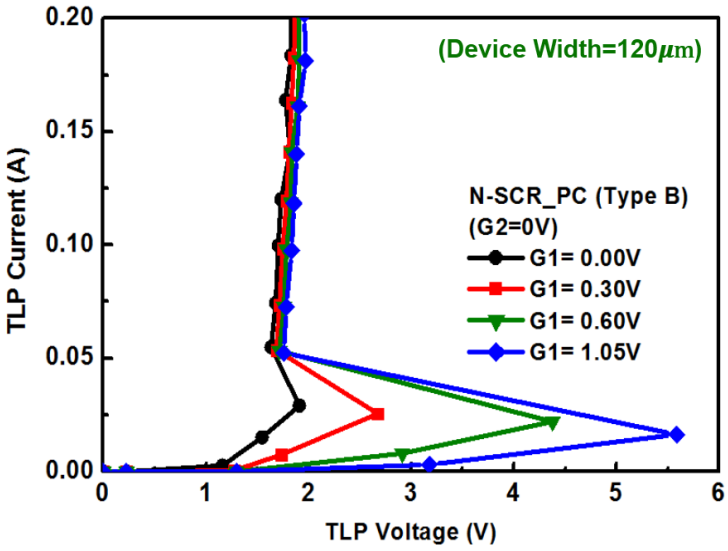


Fig. 3.50. TLP-measured I-V curves of N-SCR_PC (Type B) with different gate-bias voltage.

Table 3.10 The relation of test devices between gate voltage and trigger voltage.

	G1=0.00V	G1=0.30V	G1=0.60V	G1=1.05V
P-SCR_PC (Type B) Vt1	5.6V	4.1V	2.4V	1.6V
N-SCR_PC (Type B)Vt1	1.9V	2.7V	4.4V	5.7V

3.3.8 Definition of turn-on time

The exhibition of measurement setup is shown in Fig. 3.51. Agilent B1110A Pulse generator can provide an ESD pulse with zap voltage 30V, Rise time 2ns, and pulse width 30ns to DUT. Meanwhile, we use oscilloscope to observe and record the transient waveform.

In this section, the width of N-SCR_PC (Type B), P-SCR_PC (Type B), Substrate Trigger SCR (ST-SCR) and conventional SCR are 120 um. The measured results of turn-on time are shown in Fig. 3.52.

The definition of turn-on time is a period between start time 2ns and the time where clamping voltage enters steady state. The turn-on time of test devices in 28-nm CMOS process are listed in Table 3.11. The turn-on time of P-SCR_PC (Type B) and N-SCR_PC (Type B) device are 2.8ns and 3.3ns, respectively. The results proof that our

proposed design devices are shorten roughly 3~4 ns compared to the conventional SCR and ST-SCR device.

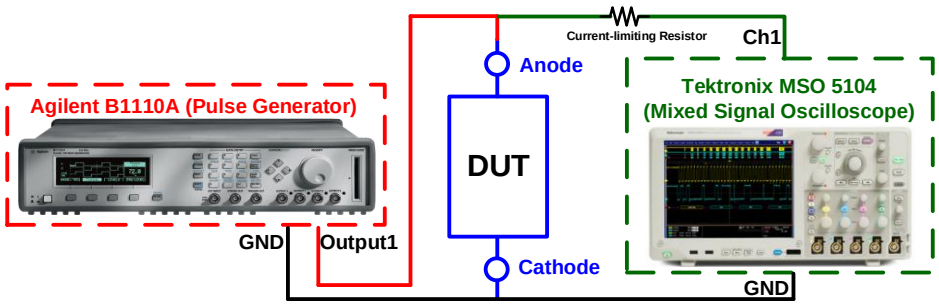


Fig. 3.51. Measurement setup of turn-on time test.

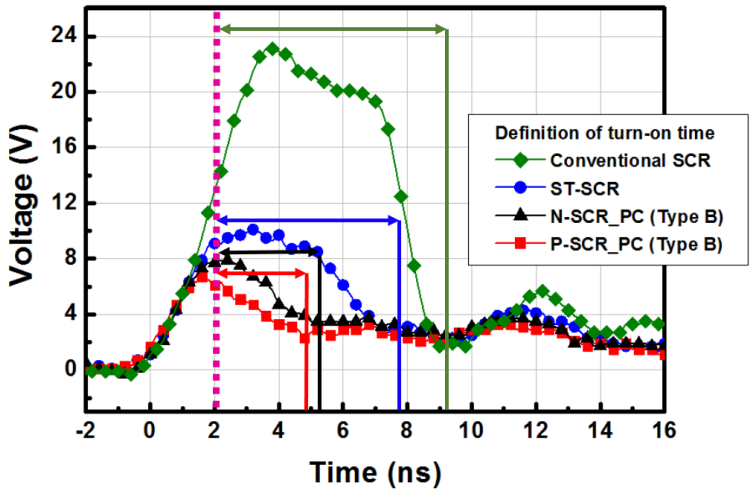


Fig. 3.52. The turn-on time of test devices in 28-nm CMOS process.

Table 3.11 The turn-on time of test devices in 28-nm CMOS process.

	Conventional SCR	ST-SCR	P-SCR_PC (Type B)	N-SCR_PC (Type B)
Turn-on time	7.1ns	5.9ns	2.8ns	3.3ns

3.3.9 Transient-Induced Latch up (TLU) test

Latch-up immunity should be considered while the ESD protection device is used as the power –rail ESD clamp device. In order to estimate the latch-up immunity of the proposed device, the transient-induced latch-up (TLU) is tested [36],[37] and the measure setup is manifested as itself in Fig. 3.53. The TLU-triggering source is constructed by a 200-pF charging capacitor, which function is storing charges and discharging stored charges to the test device. Fig. 3.54 shows that when TLU comes, the measured transient voltage waveforms of the proposed device with charging voltage of +10V.

Before the TLU tests, the voltage across the proposed device is 1.05V, which is the VDD voltage in the given CMOS process. During the TLU tests, the measured voltage waveforms are influenced simultaneously by the underdamped sinusoidal voltage. After the TLU tests, the voltage across the proposed device returns to 1.05V. From the TLU test results, the proposed device can immune to the latch-up issue.

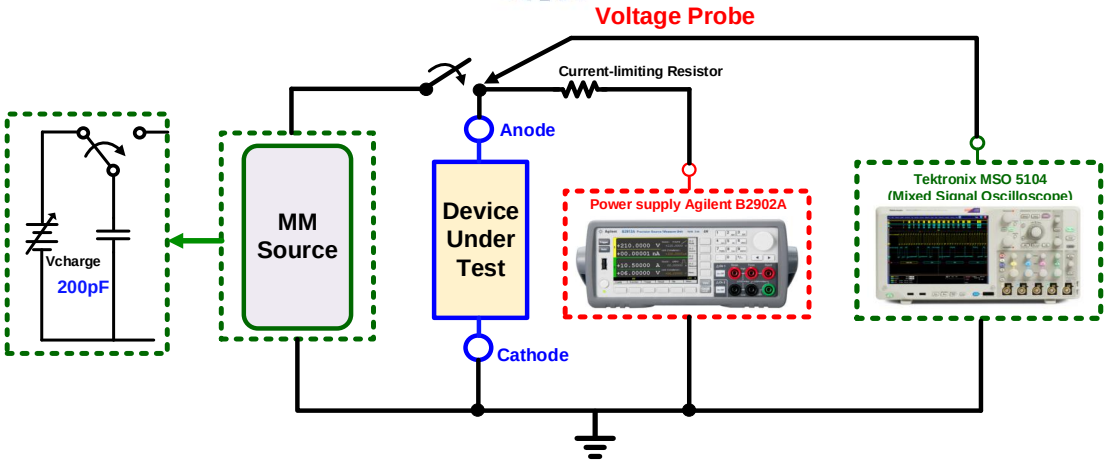
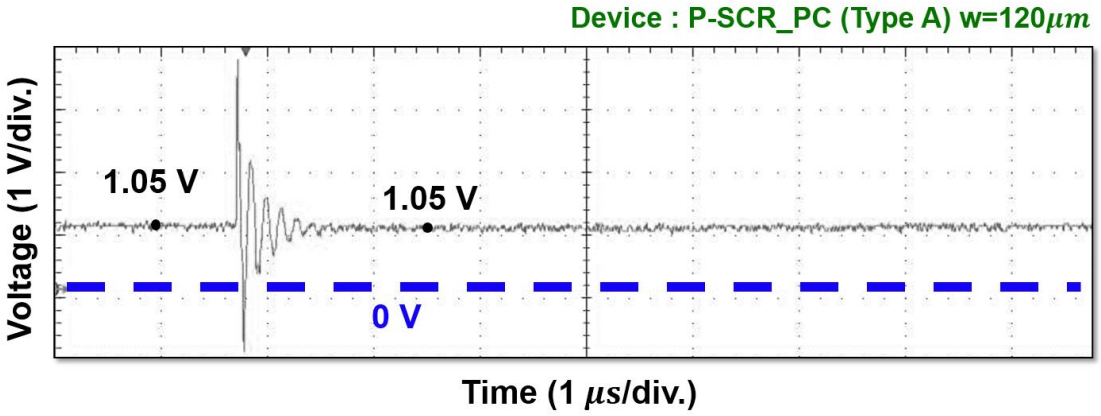
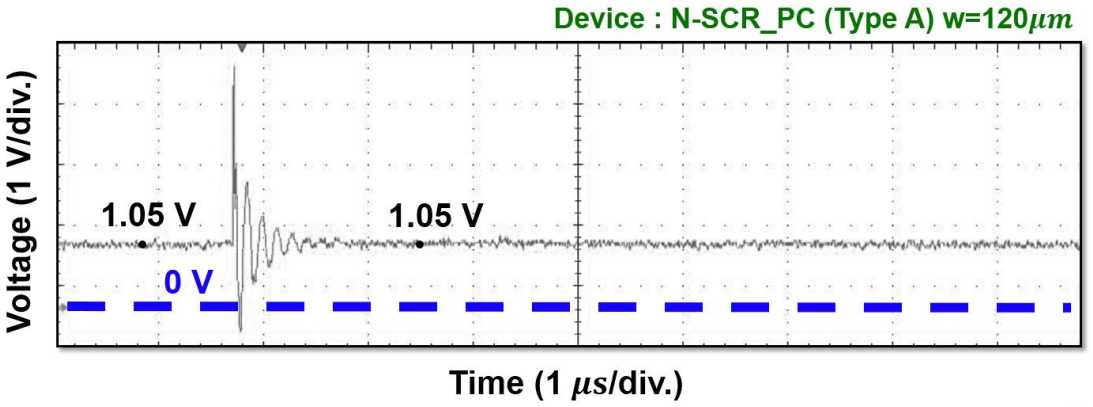


Fig. 3.53. Measurement setup of a transient-induced latch-up test.



(a)



(b)

Fig. 3.54. Measured voltage waveforms on test device (W=240μm) under TLU tests with charging voltage of +10V (a) P-SCR_PC (Type A) (b) N-SCR_PC (Type A).

3.3.10 Failure Analysis

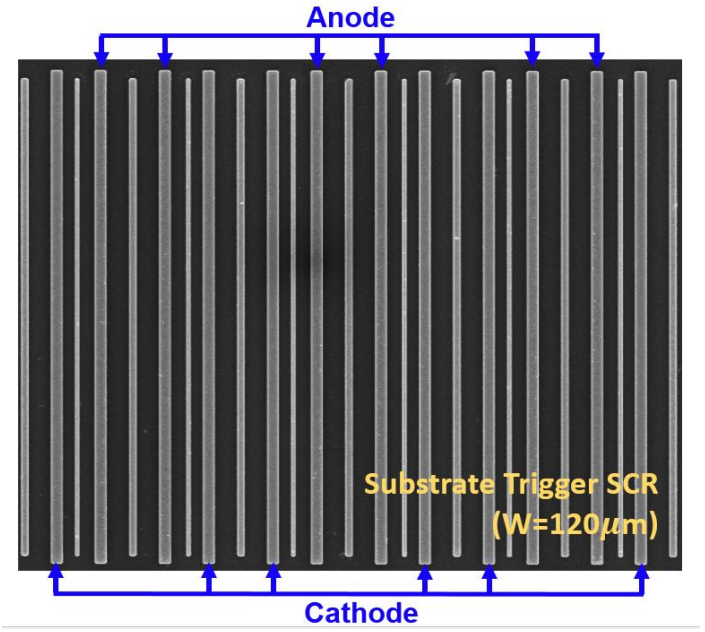
From the measurement result of ST-SCR devices, It2 can achieve to 4.3A in TLP system while It2 current only 1.7A in VF-TLP system. This result conveys that conventional ST-SCR device cannot apply on very fast ESD event. One reason to explain the result is that when very fast ESD zapping comes, ST-SCR device cannot be turned on immediately but ESD large current has already destroyed the inverter device of ESD transient detection circuit.

After VF-TLP ESD test, the scanning electron microscope (SEM) is used to find the failure locations. Fig. 3.55 shows the photo scanned from scanning electron microscope (SEM). From SEM photos, we can found that ST-SCR device do not have obvious destroyed points while inverter PMOS of ESD transient detection circuit have serious damage.

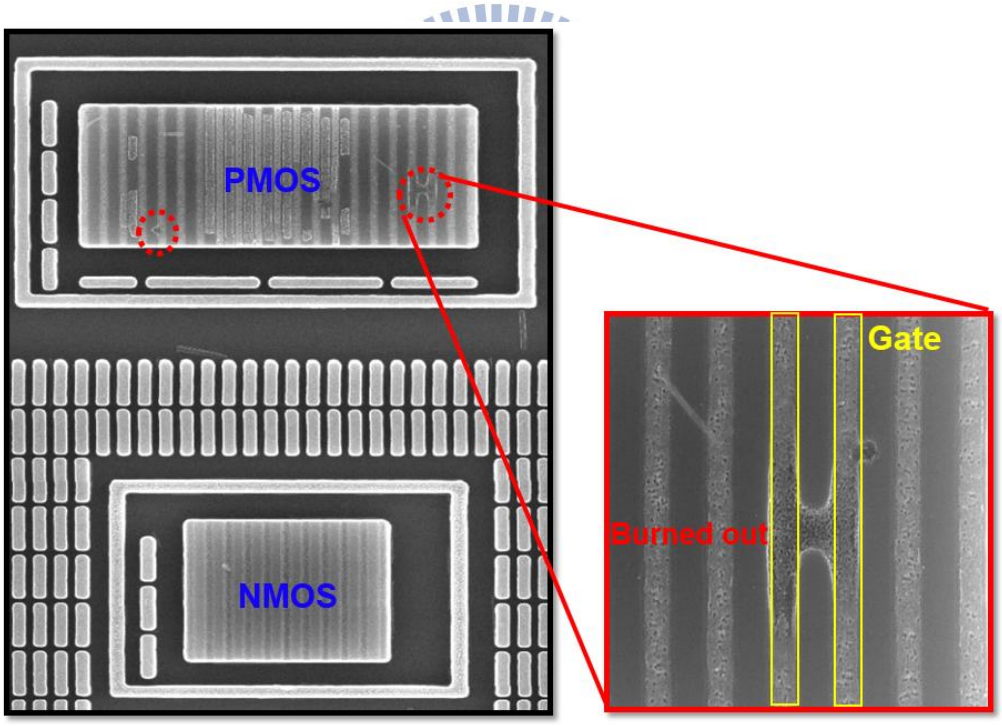
ST-SCR device uses ESD transient detection circuit to inject current to the node of embedded P+ diffusion. Substrate voltage level can be enhanced. However, ESD pulse with the characteristic of shorter rise time and pulse width causes ESD transient detection circuit cannot apply sufficient current to ST-SCR.

To solve this problem, the size of inverter in ESD detection circuit should be enlarged. Therefore, ESD detection circuit provides sufficient current to make ST-SCR turned on effectively in very fast ESD test.

Fig. 3.56 and Fig. 3.57 show the SEM photograph of the proposed device P-SCR_PC and N-SCR_PC with 360-μm width after TLP ESD test. The failure points are located at the SCR paths and the gate oxide. The SEM photograph indicates that the embedded SCR can be uniformly turned on under ESD zapping.



(a)



(b)

Fig. 3.55. SEM photo of ST-SCR device (W=120μm) after VF-TLP ESD tests. (a)ST-SCR (b) ESD Transient Detection Circuit.

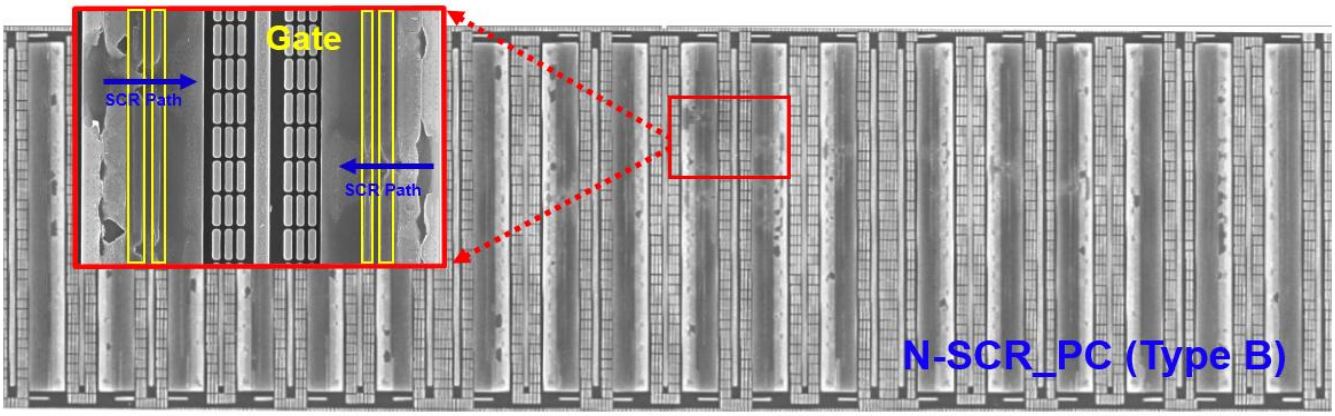


Fig. 3.56. SEM photo of N-SCR_PC (Type B) device (W=360μm) after TLP 15.4A ESD tests.

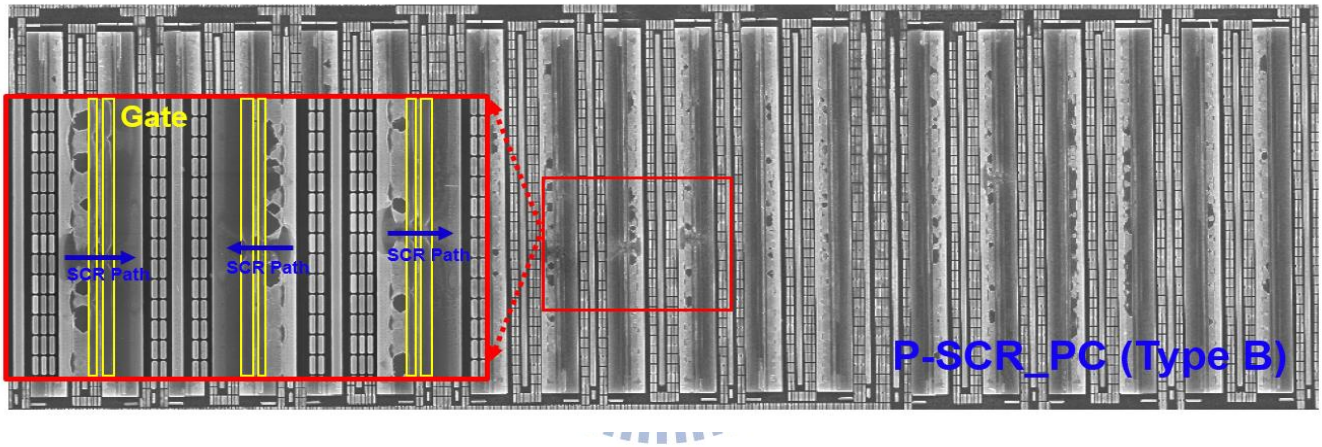


Fig. 3.57. SEM photo of P-SCR_PC (Type B) device (W=360μm) after TLP 16.4A ESD tests.

3.4 Summary

The new ESD protection devices of P-SCR_PC and N-SCR_PC have been designed, fabricated, and characterized in a 28-nm CMOS process.

The new devices is modified by the conventional SCR device with additional dummy gate. These proposed devices combine P+/, N-well, P-well, and N+ to form the parasitic SCR path. Verified in 28-nm CMOS process, the proposed devices of P-SCR_PC and N-SCR_PC with 120μm, 240μm and 360μm width are higher than 8-kV HBM ESD robustness. The results are better than the Conventional SCR, ST-SCR and GGNMOS.

In addition, modifying silicide blocking (SAB) width can enhance ESD robustness of the proposed device P-SCR_PC /N-SCR_PC ESD robustness. The measurement results proves that silicide blocking (SAB) can effectively enhance turn-on speed of device and decrease its trigger voltage. Therefore, the proposed design of Type B has better ESD reliability than the proposed device of Type A and ST-SCR.

Besides, all of the proposed devices have been tested to be free from transient-induced latch-up event. Therefore, the proposed devices can be a better solution for ESD protection in 28-nm CMOS process. All experimental data of the test devices in a 28-nm CMOS process are listed in Table 3.12, Table 3.13 and Table 3.14.

Table 3.12 The experimental data of Conventional SCR and ST-SCR in a 28-nm CMOS process.

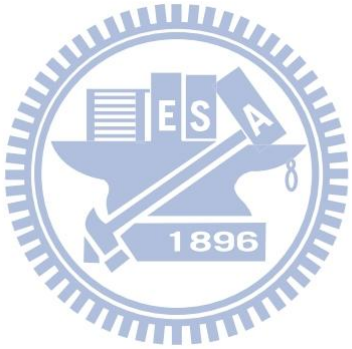
	Conventional SCR				ST-SCR			
Width	**40μm**	**120μm**	**240μm**	**360μm**	**40μm**	**120μm**	**240μm**	**360μm**
CMOS Process	**28-nm**	**28-nm**	**28-nm**	**28-nm**	**28-nm**	**28-nm**	**28-nm**	**28-nm**
TLP Vt1	N/A	17.3V	17.1V	17.7V	N/A	4.0V	4.4V	4.7V
TLP Vhold	N/A	2.89V	2.79V	3.02V	N/A	2.48V	2.42V	2.45V
TLP Ron	N/A	2.4Ω	2.0Ω	1.8Ω	N/A	3.25Ω	2.3Ω	2.1Ω
TLP It2	N/A	4.0A	7.8A	11.5A	N/A	4.3A	8.1A	12.3A
VF-TLP Vt1	16.7V	15.9V	N/A	N/A	2.06V	3.61V	N/A	N/A
VF-TLP Vhold	5.64V	5.66V	N/A	N/A	1.86V	2.27V	N/A	N/A
VF-TLP It2	2.98A	9.66A	N/A	N/A	1.10A	1.72A	N/A	N/A
HBM ESD Robustness	2.8KV	6.2KV	>8KV	>8KV	3.0KV	6.8KV	>8KV	>8KV
MM ESD Robustness	140V	250V	450V	500V	100V	250V	400V	500V

Table 3.13 The experimental data of P-SCR_PC in a 28-nm CMOS process.

	P-SCR_PC (Type-A)				P-SCR_PC (Type-B)				
Width	**40μm**	**120μm**	**240μm**	**360μm**	**40μm**	**40μm**	**120μm**	**240μm**	**360μm**
SAB width	**0μm**	**0μm**	**0μm**	**0μm**	**0.2μm**	**0.4μm**	**0.2μm**	**0.2μm**	**0.2μm**
TLP Vt1	N/A	1.64V	1.56V	1.46V	N/A	N/A	1.32V	1.29V	1.13V
TLP Vhold	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
TLP Ron	N/A	2.9Ω	2.7Ω	2.7Ω	N/A	N/A	2.4Ω	2.3Ω	2.4Ω
TLP It2	N/A	5.7A	10.9A	16.2A	N/A	N/A	5.7A	10.9A	16.4A
VF-TLP Vt1	2.00V	1.94V	N/A	N/A	1.84V	1.81V	1.89V	N/A	N/A
VF-TLP Vhold	1.83V	1.74V	N/A	N/A	1.73V	1.72V	1.64V	N/A	N/A
VF-TLP It2	3.22A	9.3A	N/A	N/A	3.43A	4.07A	11.5A	N/A	N/A
HBM ESD Robustness	3.6KV	>8KV	>8KV	>8KV	4KV	4KV	>8KV	>8KV	>8KV
MM ESD Robustness	120V	300V	450V	600V	140V	160V	350V	500V	650V

Table 3.13 The experimental data of N-SCR_PC in a 28-nm CMOS process.

	N-SCR_PC (Type-A)				N-SCR_PC (Type-B)				
Width	**40μm**	**120μm**	**240μm**	**360μm**	**40μm**	**40μm**	**120μm**	**240μm**	**360μm**
SAB width	**0μm**	**0μm**	**0μm**	**0μm**	**0.2μm**	**0.4μm**	**0.2μm**	**0.2μm**	**0.2μm**
TLP Vt1	N/A	2.12V	1.85V	2.13V	N/A	N/A	1.97V	1.85V	2.15V
TLP Vhold	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
TLP Ron	N/A	2.2Ω	1.8Ω	2.4Ω	N/A	N/A	2.1Ω	1.8Ω	1.9Ω
TLP It2	N/A	5.2A	9.9A	14.8A	N/A	N/A	5.3A	10.1A	15.6A
VF-TLP Vt1	1.69V	1.62V	N/A	N/A	1.63V	1.60V	1.60V	N/A	N/A
VF-TLP Vhold	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
VF-TLP It2	3.25A	8.9A	N/A	N/A	3.49A	3.72A	10.8A	N/A	N/A
HBM ESD Robustness	3.6KV	>8KV	>8KV	>8KV	3.8KV	3.8KV	>8KV	>8KV	>8KV
MM ESD Robustness	120V	300V	500V	650V	140V	140V	300V	550V	700V



Chapter 4

Conclusions and Future works

4.1 Conclusions

The proposed SCR devices have been developed for ESD protection in 28-nm CMOS process without using the ESD Implant, schottky junction, deep N-well, or other additional layers. The PSCR in 28nm HKMG CMOS process can be triggered at 2.3V and its holding voltage is 2.0V. Under HBM ESD tests, the PSCR device with width 20um can pass 1.4kV. Moreover, the NSCR in 28nm HKMG CMOS process can be triggered at 2.6V, and NSCR can snap back to 2.4V. Under HBM ESD tests, the NSCR device with width 20um can pass 1.8kV. Besides, they have low leakage current and low parasitic capacitance. Therefore, with the good performances during ESD stress and normal circuit operating conditions, the proposed SCR devices are very suitable for ESD protection in 28-nm high-k metal gate CMOS process.

The new ESD protection devices of P-SCR_PC and N-SCR_PC have been designed, fabricated, and characterized in 28-nm CMOS process.

The new devices is modified by the conventional SCR device with additional dummy gate. These proposed devices combine P+/, N-well, P-well, and N+ to form the parasitic SCR path. Verified in 28-nm CMOS process, the proposed devices of P-SCR_PC and N-SCR_PC with 120μm, 240μm and 360μm width are higher than 8-kV HBM ESD robustness. The results are better than the Conventional SCR, ST-SCR and GGNMOS in 28-nm CMOS process.

In addition, modifying silicide blocking (SAB) width can enhance the proposed device P-SCR_PC /N-SCR_PC ESD robustness in VF-TLP measurement results. The measurement results are proofed that silicide blocking (SAB) can effectively enhance

turn-on speed of device and decrease its trigger voltage. Therefore, the proposed devices of Type B have better ESD reliability than the proposed devices of Type A and ST-SCR.

Besides, the power-rail ESD clamp cell of proposed devices have been tested to be free from latch-up event. Therefore, the proposed devices can be a better solution for ESD protection in 28-nm CMOS process.

4.2 Future works

In chapter 3.3, the power-rail ESD clamp cell of proposed devices combing traditional ESD transient detection circuit in-28nm CMOS process cause large leakage current. The issue of gate leakage influences drastically in the traditional ESD detection circuit when a large MOSFET is used as a capacitor for ESD transient detection. Fig. 4.1 shows the power-rail ESD clamp cell of proposed devices combing traditional ESD transient detection circuit. The gate leakage through this MOS capacitor becomes unacceptable. Therefore, we can use another ESD detection circuits to resolve the leakage problem. Fig. 4.2 shows the power-rail ESD clamp circuit using the diode-string based ESD detection circuit [38] . The following steps introduce the operation of diode-string based ESD detection circuit. Under normal circuit operation, the operation voltage is lower than the diode string threshold voltage (Vth). Current cannot flow to R and Mp is turned off. Under ESD stress condition, VDD voltage can overpass Vth of diode string and diode string is turned on. Mp can be turned on as well, triggering the proposed devices.

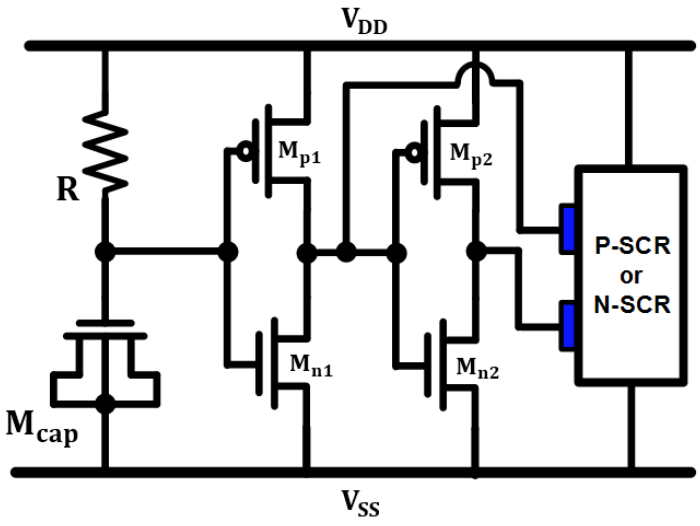


Fig. 4.1. The power-rail ESD clamp cell of proposed devices combing traditional ESD transient detection circuit.

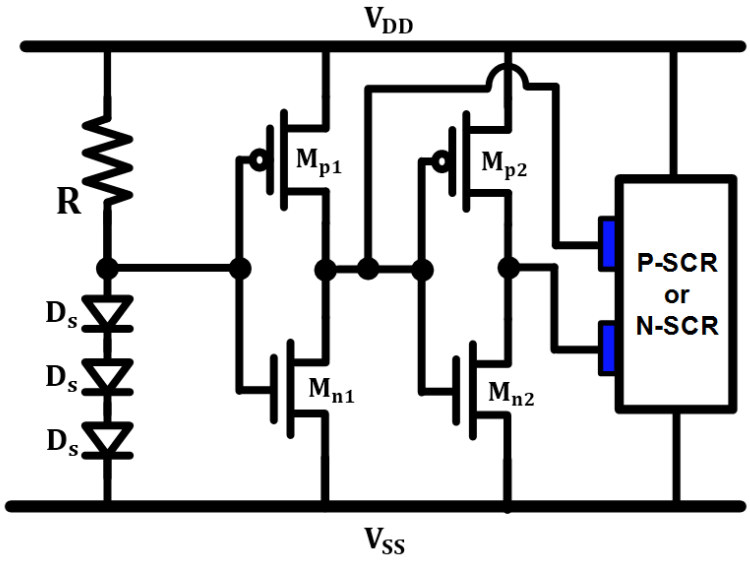


Fig. 4.2. The power-rail ESD clamp circuit using the diode-string based ESD detection circuit.

ESD robustness of traditional ESD devices becomes weak in FinFET CMOS process. The ESD robustness of FinFET devices is obviously not enough to protect integrated circuits. Therefore, many companies and international research groups focus on ESD protection of FinFET structure in FinFET CMOS process [39]-[40].

In order to enhance ESD robustness of devices, we can apply our novel design of SCR devices on ESD protection in advanced FinFET CMOS process. Moreover, we predict that low leakage, low trigger voltage and decent ESD robustness of SCR devices are the advantages of our novel design of SCR devices in future work. The illustrated layout top views of the P-SCR_PC device and N-SCR_PC device with narrow fin in FinFET CMOS process are shown in Fig. 4.2 and Fig. 4.3, respectively.

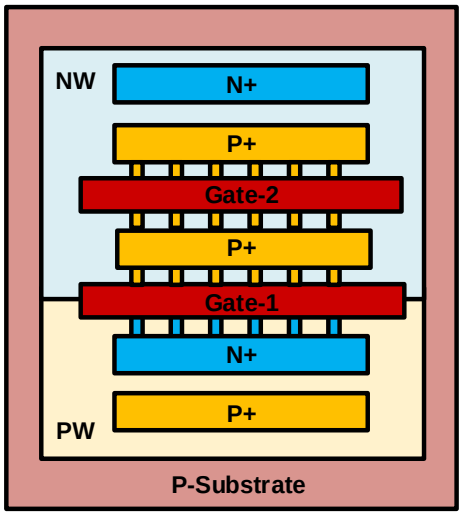


Fig. 4.3. The illustrated layout top view of the P-SCR_PC device with narrow fins in FinFET CMOS process.

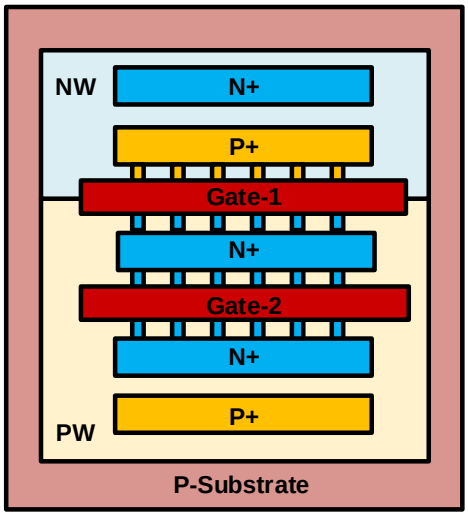


Fig. 4.4. The illustrated layout top view of the N-SCR_PC device with narrow fins in FinFET CMOS process.

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Publication List

Journal Papers:

[1] C.-Y. Lin, Yi-Han Wu, and M.-D. Ker, "Low-leakage and low-trigger-voltage SCR device for ESD protection in 28-nm high-k metal gate CMOS process," IEEE Electron Device Letters, vol. 37, no. 11, in press, Nov. 2016.

International Conference Papers:

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Patents:

[1] Yi-Han Wu, C.-Y. Lin, M.-D. Ker, and W.-T. Wang, "Low-leakage SCR structure in FinFET CMOS technology," Patent Pending.