國立交通大學

電子研究所

碩士論文

具自我重置功能之
系統層級靜電放電暫態偵測電路

On-Chip Self-Reset Transient Detection Circuit for System-Level ESD Protection

研究生：康宵瑞　　(Xiao-Rui Kang)

指導教授：柯明道教授(Prof. Ming-Dou Ker)

中華民國一〇六年五月

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摘要

隨着互補式金屬半導體積體電路製程的進步，功能日益複雜的積體電路(Integrated Circuits, ICs)得以廣泛應用於微電子產品中。在多樣的使用環境下，基於可控環境的元件層級靜電放電 (Component-Level ESD) 保護，已經無法確保積體電路在實際應用中的可靠度。因此針對終端用戶的系統層級靜電放電(System-Level ESD)以及電性快速脈衝(Electrical Fast Transient)防護在半導體積體電路的可靠度設計中越來越受到重視。在相應的靜電放電規範(IEC 61000-4-2 and IEC 61000-4-4)定義的測試條件下，由靜電放電電壓引起的快速暫態雜訊會隨機耦合到微電子產品的電源、接地、輸入/輸出腳位上，從而引發產品不正常工作，甚至損毀。針對系統層級靜電放電的防護，傳統的解決方法是在微電子產品的印刷電路板上增加抑制暫態雜訊的離散元件，如暫態突波抑制器(Transient Voltage Suppressor)及板上雜訊濾波網絡(Board-level Noise Filter Network)等。然

而板級的解決方案會大幅增加微電子產品的製造成本。因此，整合於積體電路內部的晶片上解決方案，更加符合業界實際需求。

整合於積體電路內部的暫態偵測電路結合韌體或軟體設定的晶片上解決方案，已經被證明能夠有效提升微電子產品在系統層級靜電放電以及電性快速脈衝測試下的防護能力。本论文首先提出一個新的晶片上暫態偵測電路設計方案。此暫態偵測电路採用無電容設計，經由 0.18-μm CMOS 製程技術實現。通過相關模擬及實際量測，新提出的晶片上暫態偵測電路能夠成功偵測系統層級靜電放電以及電性快速脈衝所引起的電源擾動，並送出轉態之邏輯訊號供系統執行回復。當系統回復執行完畢，配合重置訊號，此偵測電路可被重置爲初始態，以實現下一次的暫態雜訊干擾的偵測。

其次，提出一個在 0.18-μm CMOS 製程技術下，所實現的具自我重置功能的暫態偵測電路。此電路結合電容電阻延遲效應，利用反饋迴路的設計，以實現暫態偵測電路的偵測及自我重置功能。此暫態偵測電路在系統層級靜電放電或電性快速脈衝發生時，可成功偵測並記錄由靜電放電引起的發生在電源線上的暫態干擾，並送出系統所需的回復指針。在系統回復執行完畢後，此暫態偵測電路無需重置訊號即可實現自我重置至初始狀態，以偵測下一次暫態雜訊干擾，從而避免因重置訊號被暫態雜訊干擾而造成的系統故障。

On-Chip Self-Reset Transient Detection Circuit for System-Level ESD Protection

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Abstract

With the progress of CMOS semiconductor process, the increasingly complex integrated circuits (ICs) can be widely used in microelectronic products. In the variety of end users' environments, the ICs are unable to guarantee its reliability, even that has passed Component-Level ESD test. Therefore, the protection of system-level ESD and EFT tests, which simulate ESD events in an end user's environment, becomes a significant issue in the reliability design of CMOS ICs. Under the system-level electrical-transient disturbance tests, which specified in IEC 61000-4-2 and IEC 61000-4-4, the ESD-induced fast electrical transient can be randomly coupled to the power, ground and I/O pins to result in a hardware damage or system malfunction. In traditional solutions, extra discrete components are added on PCB to suppress the transient disturbance, such as TVS or board-level noise filter network. However, the board-level

solution is not cost efficient to microelectronic products. Therefore, an on-chip solution is highly desired by industry.

It has been proven that an on-chip transient detection circuit with hardware/firmware co-design can effectively enhance the immunity of CMOS ICs against the system-level ESD and EFT tests. In the thesis, firstly, a new on-chip transient detection circuit has been proposed and fabricated in a 0.18-μm CMOS process. It has been confirmed that with this capacitor-less on-chip transient detection circuit, the occurrence of electrical transient coupled to power lines due to system-level ESD or EFT event can be successfully detected and memorized. The memorized state can be further used as firmware index to execute the system recovery procedure. When system recovery ends, the proposed transient detection circuit can be reset to initial state with reset signal for next electrical transient detection.

Secondly, a novel on-chip self-reset transient detection circuit has been proposed. This circuit has been designed and fabricated in a 0.18-μm CMOS process. With different feedback, this CR-based transient detection circuit can realize the detection and self-reset function. The system-level ESD and EFT test results have confirmed that the proposed on-chip self-reset detection circuit can successfully store the occurrence of electrical transient disturbance on power lines and release the stored state after a time constant automatically. In system application, the hardware/firmware co-designed with this self-reset transient detection circuit can avoid the system upset caused by the mistriggering of reset signal.

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不知不覺中，我在臺灣的碩士生涯接近了尾聲。這兩年半的時間里有許多對我而言至關重要的事情發生，也有許多感恩要在這里表達。

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Chapter 1

Introduction

In this chapter, the motivation and the organization of this thesis are discussed. The first part of this chapter is an introduction to the motivation of transient detection circuit design, and the second part is a description of the thesis' organization.

1.1 Motivation

Electrostatic Discharge (ESD) is one of the most serious reliability issues of CMOS integrated circuits (ICs). With the improvement of semiconductor process and technology, the device size of CMOS ICs has been scaled down and more CMOS ICs have been integrated into a single chip. The thinner oxide and shallower junction depth in advanced technology increase the susceptibility to ESD stress of CMOS ICs. The ESD events of CMOS ICs can occur in a variety of ways during fabricating or operating. ESD-induced failure of CMOS ICs can be seen in the form of junction leakage, metal burn out, short circuits, etc. To solve the ESD-induced reliability issues, on-chip protection circuits have been added into CMOS ICs [1]-[3]. Those on-chip protection circuits are designed to meet the strict requirements of the ESD related international standards (component-level and system-level) [4]-[8]. Component-level ESD tests are used to simulate the ESD events in well-controlled environments, such as factory environment. Besides the component-level ESD tests, the system-level ESD tests are used to simulate the ESD events in the end-users' environments, which means the CMOS ICs under system-level ESD tests are powered on.

It has been reported that some CMOS ICs are still susceptible under system-level ESD tests even they have passed the specifications of component-level ESD, such as human-body-model (HBM), machine-model (MM) and charged-device-model (CDM) [9]-[13]. Therefore, electrical transient disturbance due to the system-level ESD events is an increasingly significant reliability issue in CMOS IC systems. These disturbances can influence the voltage level of power line (V_{DD}), ground line (V_{SS}), input/output (I/O) pins and even the inside signals, which cause the failure of CMOS ICs. The failures induced by the electrical transient disturbance include hardware damage and system malfunction, such as chip burning out, logic data losing or system upset [14]-[20]. Traditional solutions against the system-level ESD tests are adding discrete components or board-level noise filter to decouple, absorb or bypass the electrical transients and adding external hardware timer to check the system abnormal condition [21]-[23]. Those additional solutions substantially increase the total cost of a microelectronic product with CMOS ICs. Therefore, an on-chip solution integrated into CMOS ICs is strongly requested by the IC industry.

It has been proven that an on-chip transient detection circuit integrated into CMOS ICs co-design with hardware/firmware can enhance the robustness against system-level ESD tests of microelectronic products [9], [24]-[33]. The on-chip transient detection circuit can detect and memorize the occurrence of electrical transient disturbance during system-level ESD tests. The detected and stored state from the on-chip transient detection circuit can be set to the firmware as the recovery index to execute the system recovery procedure. Therefore, the system can pass “Class B” evaluation of system-level ESD test results. The prior on-chip transient detection circuits are composed with detection circuit, memory circuit and reset circuit. The reset circuit is designed to provide the initial state and the reset function of the on-chip transient detection circuits. Combined with firmware, additional data path is required

for the reset circuit too. The reset circuit and the additional data path also take risks during the system-level ESD tests [10]. With this consideration, an on-chip self-reset transient detection circuit is proposed to avoid these risks.

1.2 Thesis Organization

This thesis is composed of five chapters, including three major topics: (1) System-level ESD standard and EFT standard introduction, (2) New proposed on-chip transient detection circuit design, (3) On-chip self-reset transient detection circuit design. The outlines of each chapter is summarized below.

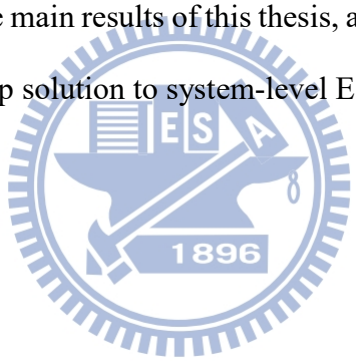
Chapter 1 introduces the motivation of on-chip transient detection circuit design and the main organization of this thesis.

Chapter 2 shows the standards and traditional solutions of system-level ESD and EFT. In this chapter, the test method, test level and test set-up are generally guided. Also, several solutions to overcome system-level ESD and EFT events are collected and introduced.

Chapter 3 propose a novel on-chip transient detection circuit. This circuit is designed to detect the positive and negative transient voltage coupled on V_{DD} and V_{SS} while system-level ESD and EFT event occurring. The circuit function is investigated by HSPICE simulation and verified in silicon chip. The experimental measurement results have confirmed that the proposed on-chip transient detection circuit can successfully change its output voltage level during the system-level ESD test and EFT test. Based on this on-chip transient detection circuit, the system recovery procedure is introduced to provide a hardware/firmware co-design to improve the immunity of CMOS ICs against the system level ESD tests.

Chapter 4 proposes an on-chip self-reset transient detection circuit. This circuit is designed to detect the system-level ESD-induced and EFT-induced electrical transient disturbance. The proposed on-chip self-reset transient detection circuit can operate without the reset part of circuit. With HSPICE simulation results and measurement results showed in this chapter, the detection and self-reset function have been confirmed. Combined with this self-reset transient detection circuit, the system recovery flowchart does not need additional reset data path added in. Thus, the on-chip self-reset transient detection circuit with hardware/firmware co-design can provide a more effective solution to solve the system-level ESD and EFT protection issue in microelectronic products equipped with CMOS ICs.

Chapter 5 concludes the main results of this thesis, and addresses some suggestion of future work for the on-chip solution to system-level ESD and EFT protection.



Chapter 2

Introduction of International Standards and Solutions

The component-level ESD standards are well defined by many international associations such as ESDA (Electrostatic Discharge Association), JEDEC (Joint Electron Device Engineering Council), and MIL-STD (US Military Standard), etc. To meet the component-level ESD standards, the protection circuits are added in the CMOS ICs. However, component-level ESD tests only simulate the ESD events in a well-controlled environment, such as factory environment. To simulate the ESD events in the end-users' environments, other standards such as IEC 61000-4-2 (system-level ESD) [7] and IEC 61000-4-4 (EFT) [8] are established. IEC 61000 is the series of EMC (Electromagnetic Compatibility) standards defined by IEC (International Electrotechnical Commission), and part 4 is about testing and measurement techniques. These two international standards and solutions are introduced below.

2.1 Introduction of International Standard

2.1.1 Introduction of System-level ESD standard

System-level ESD tests are intended to simulate end-user ESD events in the real world. IEC 61000-4-2 which defined by IEC is the most common test standard used in industry for system-level ESD tests. This standard specifies the test levels, the test methodologies and the evaluation levels of the test results against system-level ESD.

There are two test methods specified in this standard: contact-discharge test method and air-discharge test method. Under contact-discharge test method, the

discharge head of ESD gun used in system-level ESD test is held in contact with the equipment under test (EUT). Under air-discharge test method, the discharge head of ESD gun used in system-level ESD test approaches the EUT, then actuates the discharge by the spark.

Table 2.1 gives the test level specified in the standard for each test method. The test voltage for each test method are different. An "X" level is specified in the dedicated equipment specification. It is important to note that the test severity is not related between contact discharge and air discharge test methods. In addition, contact-discharge is preferred test method due to the unrepeatability of air-discharge test method.

Table 2.1
Test Levels of system-level ESD

Contact Discharge		**Air Discharge**	
Level	**Test Voltage (kV)**	**Level**	**Test Voltage (kV)**
1	**± 2**	**1**	**± 2**
2	**± 4**	**2**	**± 4**
3	**± 6**	**3**	**± 8**
4	**± 8**	**4**	**± 15**
X	**Specified by Customer**	**X**	**Specified by Customer**

Contact-discharge and Air-discharge test methods use same ESD generator to execute the system-level ESD test. Fig. 2.1 shows the equivalent circuit of ESD generator used in system-level ESD test. Table 2.2 shows the definition of each device of the ESD generator. The typical value of charging capacitor (C_d+C_s) is 150 pF. The typical value of discharge resistor (R_d) is 330 Ω. The ESD gun is commonly used as the system-level ESD generator. The head of ESD gun used in contact discharge method is much sharper than which used in air-discharge as Fig. 2.2 shows. In order to compare

the test results obtained from different ESD generator, the standard of IEC 61000-4-2 specify the characteristics of discharge waveform in Table 2.3. In additional, an ideal discharge current waveform at 4 kV test voltage is shown as Fig. 2.3.

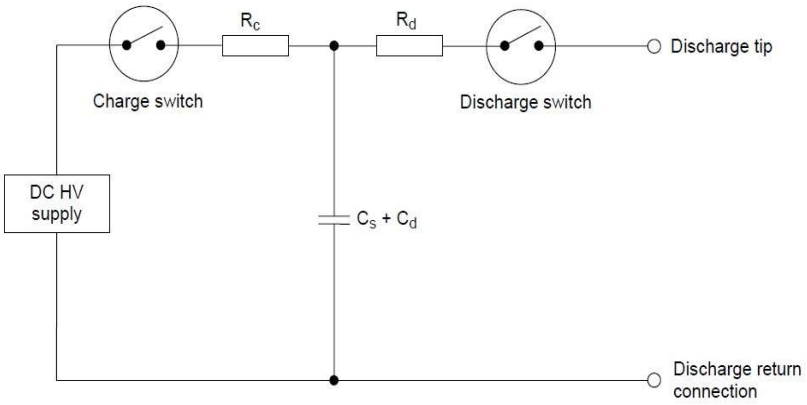


Fig. 2.1 The equivalent circuit of ESD generator used in system-level ESD test.

Table 2.2
Characteristics of the equivalent circuit of system-level ESD generator

Parameter	Definition
R_c	Charging Resistor
R_d	Discharge Resistor
C_s	Energy-store Capacitor
C_d	Distributed Capacitor

Fig. 2.2 Discharge heads of ESD gun that used under system-level ESD test with contact-discharge mode and air-discharge mode.

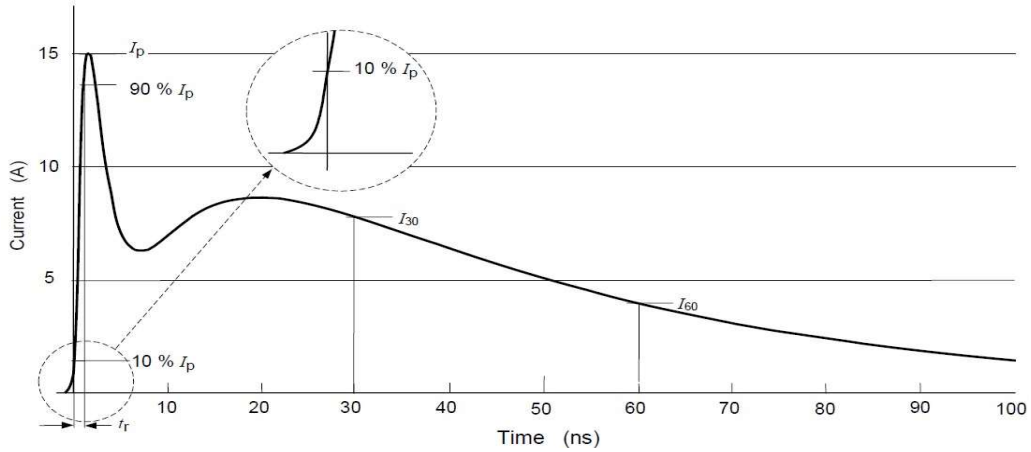


Fig. 2.3 Ideal current waveform under system-level ESD with 4 kV zapping voltage.

Table 2.3

Waveform parameters of discharge current under system-level ESD test

Level	Indicated Voltage (kV)	First Peak Current ±10% (A)	Rise Time (ns)	Current (±30%) at 30ns (A)	Current (±30%) at 60ns (A)
1	2	7.5	0.7 to 1	4	2
2	4	15	0.7 to 1	8	4
3	6	22.5	0.7 to 1	12	6
4	8	30	0.7 to 1	16	8

The contact-discharge test mode is divided into direct discharge to EUT and indirect discharge to horizontal coupling planes (HCP) or vertical coupling planes (VCP). Fig. 2.4 shows the standard measurement setup of system-level ESD test in contact-discharge test mode. All the instruments are placed on the ground reference plane (GRP). The EUT shall be separated from the HCP by an insulation plane. The HCP and VCP are connected to the GRP with two 470 kΩ resistors in series. Under system-level ESD test, the electromagnetic interference coming from ESD gun will be coupled into CMOS ICs inside EUT through HCP or VCP.

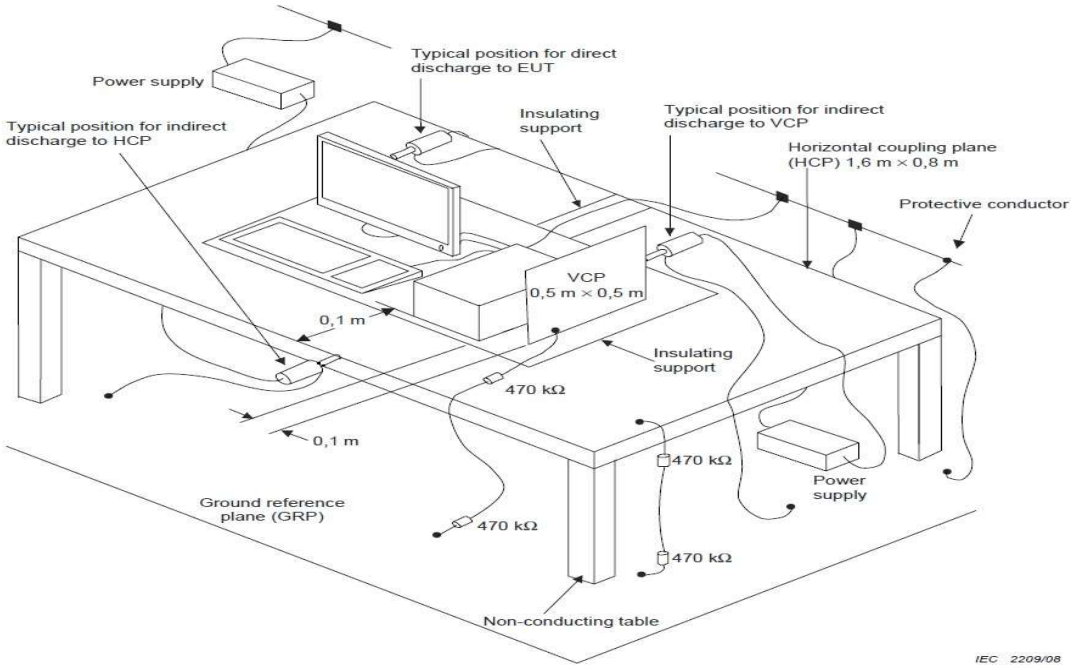


Fig. 2.4 The measurement setup system-level ESD test.

Four levels of evaluation of system-level ESD test results are specified in IEC 61000-4-2 standard. From the evaluation shown in Table 2.4, the system have to pass "Class B" at least which means system shall be recover automatically after the system-level ESD tests.

Table 2.4

Recommended classifications of system-level ESD results

Criterion	Classification
Class A	Normal performance within limits specified by defined
Class B	Temporary loss of function or degradation of performances, self-recovery
Class C	Temporary loss of function or degradation of performances, recovery with operator intervention
Class D	Loss of function or degradation of performances which is not recoverable

2.1.2 Introduction of EFT standard

EFT (Electrical Fast Transient) test is meant to simulate the switching transients caused by the interruption of inductive loads such as relays, switch contactors, etc. A common cause of EFT is sparking that occurs whenever a power cord is plugged in, equipment is switched off, or when circuit breakers are opened or closed. The EFT test is a burst of pulses that have predetermined amplitude and limited duration. IEC defines the EFT test standard in IEC 61000-4-4. The object of this standard is to establish and reproducible reference for evaluating the immunity of electrical and electronic equipment when subjected to electrical fast transient/bursts on supply, signal, control and earth port. This standard include the test levels, test methodologies and the evaluation levels of test result of EFT test.

Table 2.5 list the EFT test levels for power port testing and I/O ports testing of equipment under test (EUT). The voltage peak for testing these two types port of EUT is different. Half of voltage peak, which set to power port test, is set to I/O ports test in each level. The repetition rate of both tests is 5 kHz or 100 kHz. Generally, the repetition rate of 5 kHz is traditional, but 100 kHz is much closer to reality. Consider to the different output load, the measured peak voltage under test is smaller than the set voltage as Table 2.6 listed. For example, with output load of 50 Ω, the measured peak voltage is half of the value of open-circuit load due to 50 Ω impedance matching resistor in equivalent circuit of EFT generator.

Table 2.5

Test levels of EFT

Level	On Power and PE (Protective Earth) Ports		On I/O (Input/Output) Signal, Data, and Control Ports	
	Voltage Peak (kV)	Repetition Rate (kHz)	Voltage Peak (kV)	Repetition Rate (kHz)
1	0.5	5 or 100	0.25	5 or 100
2	1	5 or 100	0.5	5 or 100
3	2	5 or 100	1	5 or 100
4	4	5 or 100	2	5 or 100
X	Specified by Customer	Specified by Customer	Specified by Customer	Specified by Customer

Table 2.6

Output voltage peak values under EFT test

Set Voltage (kV)	V_P (Open) (kV)	V_P (1000 Ω) (kV)	V_P (50 Ω) (kV)	Repetition Rate (kHz)
0.25	0.25	0.24	0.125	5 or 100
0.5	0.5	0.48	0.25	5 or 100
1	1	0.95	0.5	5 or 100
2	2	1.9	1	5 or 100
4	4	3.8	2	5 or 100

Fig. 2.5 shows the simplified circuit diagram of EFT generator. The dc blocking capacitor (C_d) is 10 nF and the impedance matching resistor (R_m) is 50 Ω. The detail parameter of this circuit diagram is collected in Table 2.7.

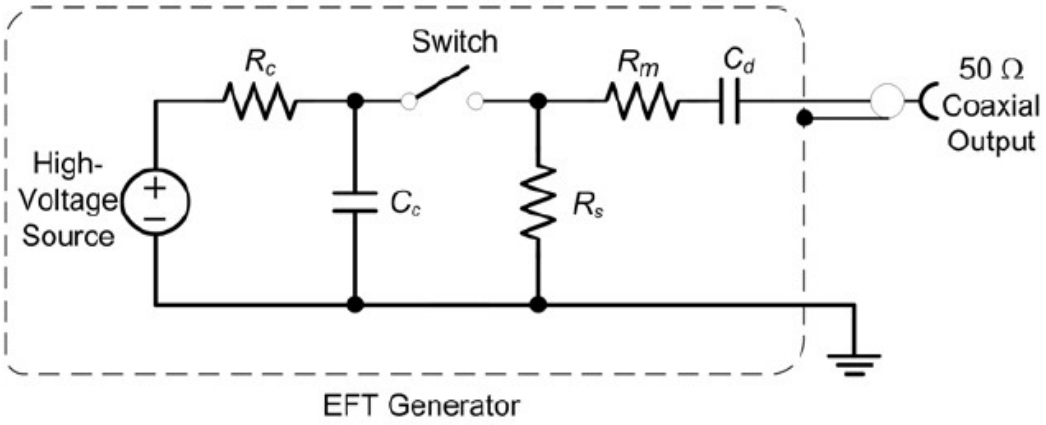


Fig. 2.5 The equivalent circuit of EFT generator.

Table 2.7

Characteristics of equivalent circuit of the EFT generator

Parameter	Definition
R_c	Charge Resistor
C_c	Energy Storage Capacitor
R_s	Duration Shaping Resistor
R_m	Impedance Matching Resistor
C_d	DC Blocking Capacitor

The EFT test is a test with repetitive burst string consisting a number of fast pulses. These pulses shall be couple in to power or any signal ports of microelectronic products. The standard defines the typical EFT waveforms in Fig. 2.6. The burst consist 75 pulses with every 300 ms period. Each burst duration should be 15 ms at repetition rate 5 kHz or 0.75 ms at repetition rate 100 kHz. That means the period of these pulses should be 200 μs at 5 kHz or 10 μs at 100 kHz. Fig. 2.7 shows the wave shape of a single pulse into 50 Ω load. The rise time of the pulse is about 5 ns and the pulse duration (time interval at half of peak EFT voltage) is about 50 ns. The peak voltage shall follow the value listed in Table 2.5.

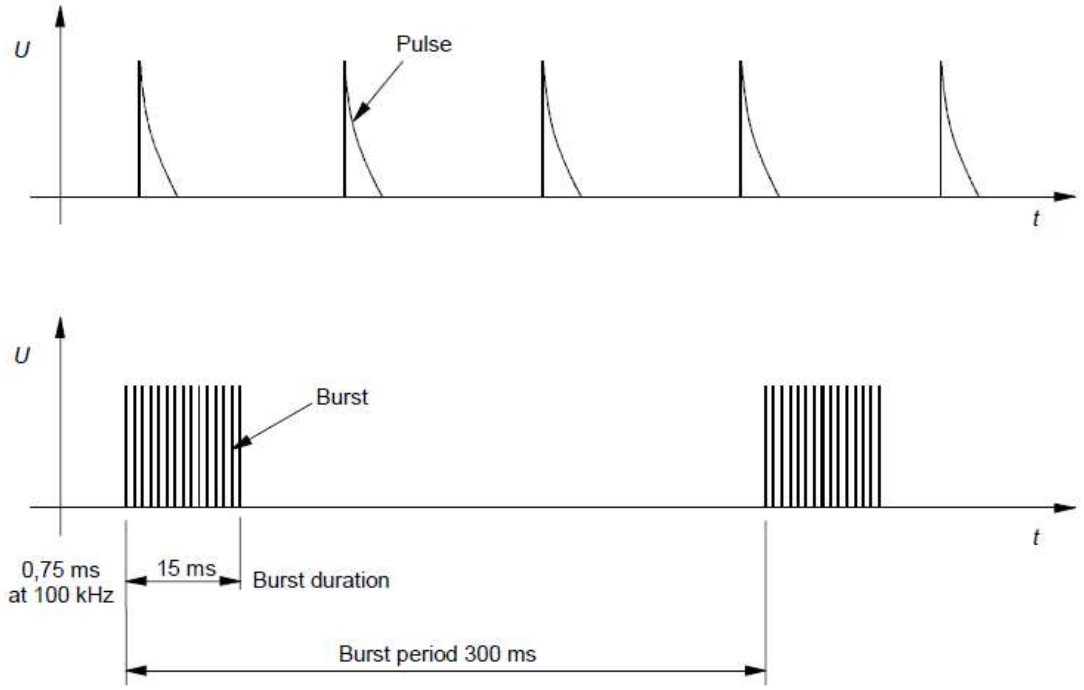


Fig. 2.6 General graph of a fast transient/burst.

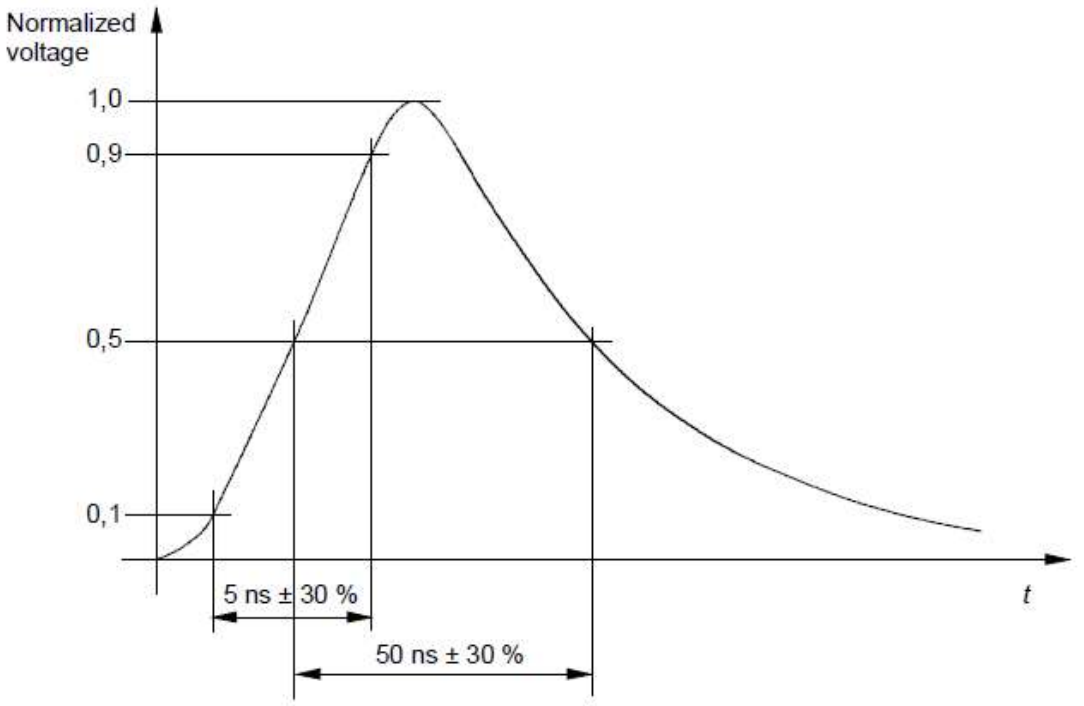


Fig. 2.7 Wave shape of a single pulse into a 50 Ω load.

The method of coupling the test voltage to the EUT is dependent on the type of EUT port. Fig. 2.8 shows an example of the test set-up for direct coupling test method.

The EFT disturbance voltage couple the transients via a coupling/decoupling network. This is the preferred method of coupling transients to power supply ports. If there is no suitable coupling/decoupling network, the capacitive coupling clamp shall be used to test power supply ports too. The test set-up of capacitive coupling clamp test method is showed in Fig. 2.9. This method is used for I/O and communication ports test usually. The EFT disturbance voltage couple the transients via the capacitive coupling clamp.

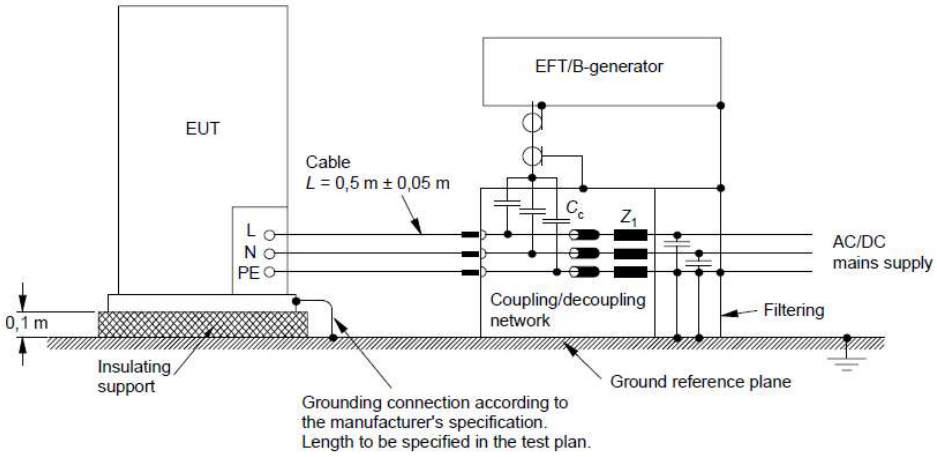


Fig. 2.8 Test setup for direct coupling of the test voltage to power supply ports under EFT test.

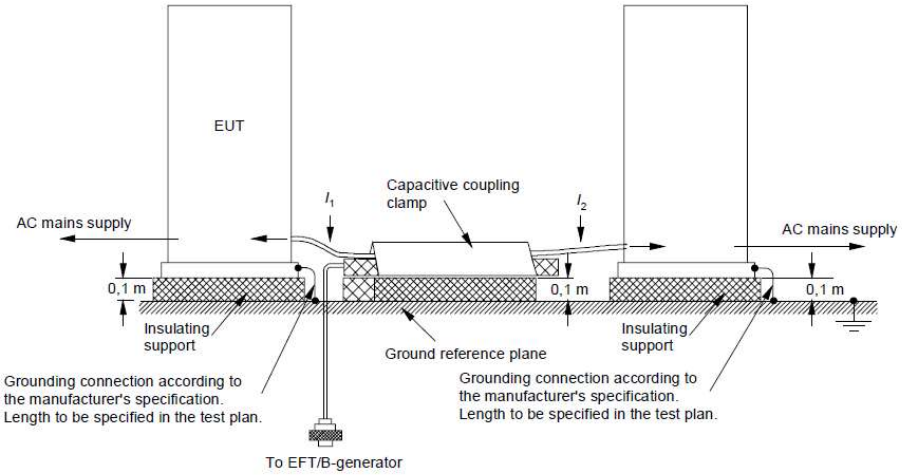


Fig. 2.9 Test setup for application of the test voltage by the capacitive coupling clamp under EFT test.

The evaluation of EFT test results is listed in Table 2.7. The test results shall be classified in terms of the loss of function or degradation of performance of the equipment under test. The microelectronic product should recover automatically itself after the EFT test that means to pass “Class B” at least.

Table 2.8
Recommended classifications of EFT results

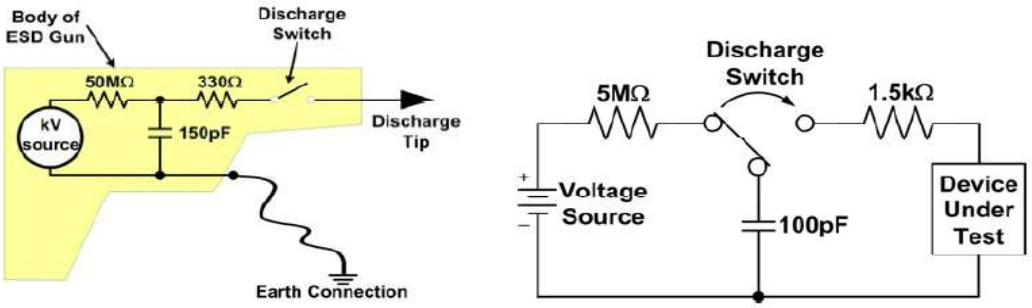
Criterion	Classification
Class A	Normal performance within limits specified by defined
Class B	Temporary loss of function or degradation of performances, self-recovery
Class C	Temporary loss of function or degradation of performances, recovery with operator intervention
Class D	Loss of function or degradation of performances which is not recoverable

2.2 System Solutions to Overcome Electrical Transient Disturbance

2.2.1 Background

According to the specifications defined by system-level ESD standard, system-level ESD is more significant to influence the reliability of microelectronic products. Fig. 2.10 (a) is the equivalent circuit of ESD gun used for system-level ESD test, and Fig. 2.10 (b) is the equivalent circuit of human body model (HBM) in component-level ESD test. Compare to the component-level ESD test, the charging capacitor of system-level ESD gun is larger and the discharge resistor is smaller. Thus, the system-level ESD-induced energy is much larger. Fig. 2.11 shows the typical discharge current waveform under system-level ESD (IEC 61000-4-2) and component-level ESD test (MIL-STD 883). From the waveform, the peak current in system-level ESD test is about

five times than that in component-level ESD test under 8 kV zapping. Unfortunately, there is no clear correlation of system-level performance to the HBM robustness [14]. It has been proven that improving the component-level ESD level of the CMOS ICs cannot solve the system-level ESD issues [9].



(a) (b)

Fig. 2.10 The equivalent circuit of (a) ESD gun used in system-level ESD test and of (b) human body model under component-level ESD test.

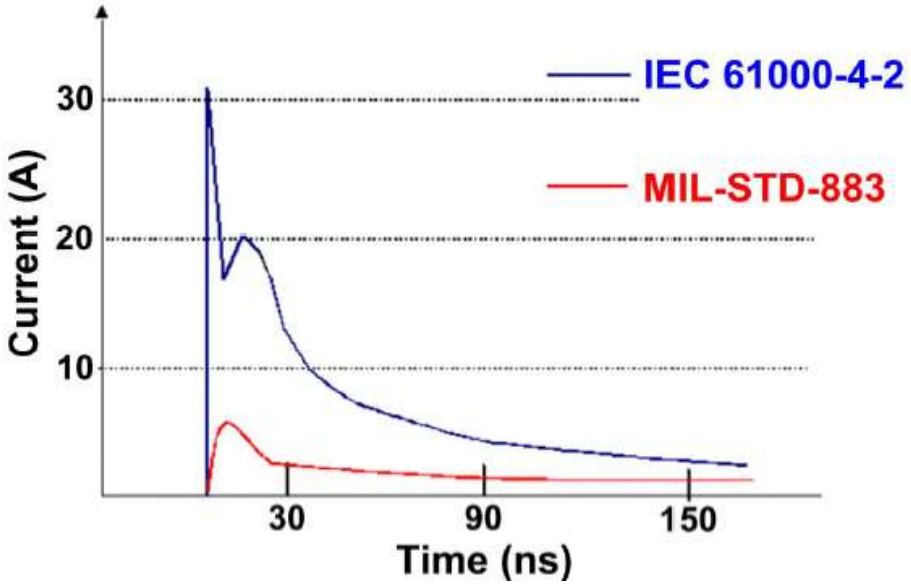


Fig. 2.11 The peak current waveform of system-level ESD test and component-level ESD test under 8 kV zapping voltage.

2.2.2 Traditional Board-level System Solutions

In order to improve the immunity of microelectronic products to achieve the strict system-level ESD specifications, two useful methods has been reported and

investigated. One of the system design solution against system-level ESD events is to add some discrete noise-decoupling components (TVS diode) or board–level noise filters on the printed circuit board (PCB), as shown in Fig. 2.12. For example, Fig. 2.12 (a) shows the system solution to overcome the system-level ESD issue in keyboard, and Fig. 2.12 (b) is used for universal series bus (USB) input/output (I/O) port protection. The transient noise generated from system-level ESD events can be decoupled, bypassed, or absorbed by these discrete components and board-level noise filters [20]. Therefore, choosing proper components and noise filter can significantly enhance the system-level ESD immunity of CMOS ICs. Another solution against system-level ESD events is to add an external hardware timer, such as watchdog timer [19]. The external hardware timer help resetting the system from an abnormal condition due to system-level ESD tests.

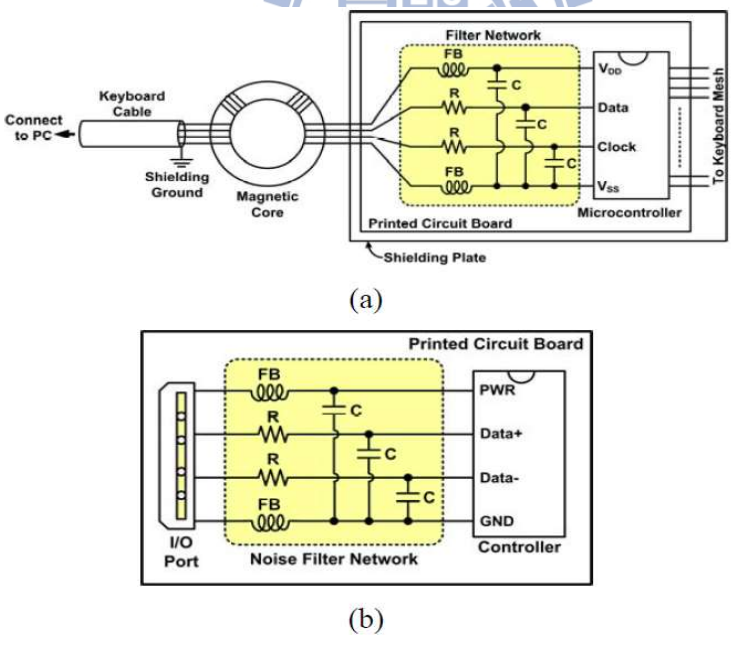


Fig. 2.12 The system solution to protect overcome the system-level ESD issue (a) in keyboard and (b) in USB I/O port.

However, the additional discrete noise-bypassing components and the external hardware timer increase the total cost of the microelectronic products. Moreover, if the

register in the hardware timer is changed during the system-level ESD test, the main operation program of system may be malfunction. Therefore, the chip-level solutions to meet the transient disturbance immunity specifications for microelectronic products are desired for IC industry.

2.2.3 Hardware/Firmware Co-design Solution

The previous researches show the system-level ESD susceptibility of CMOS IC products can be effectively enhanced by the hardware/firmware co-design concept [9]. An on-chip transient detection circuit is designed to detect the occurrence of electrical transient disturbance events due to system-level ESD tests. During the system-level ESD tests, the output voltage level of the on-chip transient detection circuit is changed. This output state can be sent to the firmware as the system recovery index.

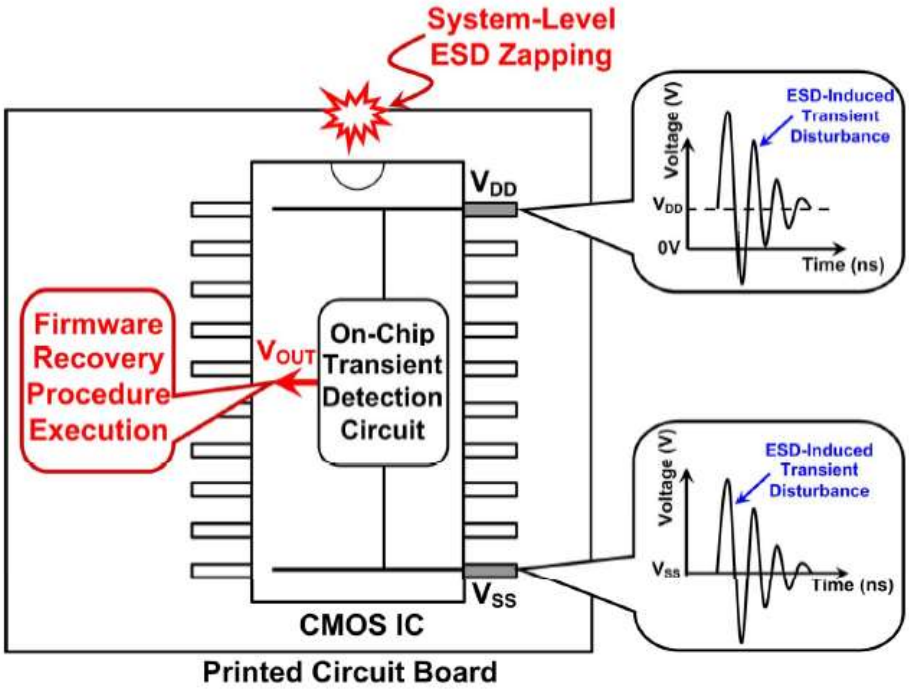


Fig. 2.13 The on-chip transient detection circuit with hardware/firmware co-design.

Fig. 2.13 is an example of proper designed on-chip transient detection circuit with hardware/firmware co-design. From the example, the output of transient detection

circuit and the firmware is cleared to logic “0” at initial state. When the fast electrical transient disturbance happens, the on-chip detection circuit can detect the occurrence of transient disturbance coupled to power and ground lines, then change its output state to memorize this event. The output of transient detection circuit set the firmware index to logic “1”. System will execute the recovery procedure to reset the abnormal state. When the recovery procedure ended, the firmware and the transient detection circuit are reset to logic “0” again for detecting the next system-level ESD events.

2.3 Summary

The IEC defines the standards of system-level ESD test and EFT test. These two standards are introduced in this chapter. Microelectronic products shall pass “Class B” of these tests, which means they must be able to recover automatically. Traditional solutions to enhance the system-level immunity under the system-level ESD tests and EFT tests are not a cost-effective choice. It has been proved the system will execute automatic recovery procedure by the on-chip transient detection circuit with hardware/firmware co-design concept. Thus, an on-chip solution can help microelectronic products quipped with CMOS ICs to pass “Class B” classification under system-level ESD tests and EFT tests. This on-chip solution can save cost and enhance the robustness of microelectronic products against system-level ESD and EFT tests.

Chapter 3

Design of New On-Chip Transient Detection Circuit

3.1 Background

High-energy ESD-induced transient noise will be coupled to power (V_{DD}) and ground (V_{SS}) lines of CMOS ICs inside EUT during the system-level ESD tests and EFT tests. These high-energy noises are the main reasons of system errors, such as data loss or system frozen, even hardware damage. It has been proven that a hardware/firmware co-design solution will help system avoid these unexpected situations during system-level ESD test and EFT test. According to this co-design concept, an on-chip transient detection circuit is designed to help system executes the recovery procedure and restores to a known and stable state.

3.1.1 Prior Arts

Two on-chip transient detection circuits have been proposed in prior arts. They are both verified in silicon chips.

The circuit diagram of first design of on-chip transient detection circuit is show in Fig. 3.1 [25]. The proposed detection circuit comprises of one latch, two coupling capacitor and one reset device. The coupling capacitors (C_{p1} and C_{p2}) placed between the input/output node of latch and V_{DD}/V_{SS} lines can sense the fast electrical transient disturbance coupled to the V_{DD}/V_{SS} lines. The latch circuit is designed as a memory unit to store the detected occurrence of ESD events. It has been analyzed that the well-designed device W/L ratios of latch can increase the sensitivity of the detection circuit. In order to effectively detecting the positive and negative voltage coupled on the

V_{DD}/V_{SS} line, the NMOS (M_{n1}) is designed with a larger W/L than PMOS (M_{p1}), the PMOS (M_{p2}) is designed with a larger W/L than NMOS (M_{n2}). The reset device provides the initial state of the detection circuit so that the metastable operation of this latch can be avoided. Furthermore, this reset device is realized as NMOS or PMOS. In normal circuit operations, the output nodes of this proposed circuit will keep at logic 0 by the reset device. When the system-level event comes, circuit can detect the transient disturbance coupled on V_{DD}/V_{SS} lines and memorize this state for firmware check. As a result, this circuit which be fabricated in 0.13μm 1.2/3.3V 1P8M CMOS process, has successfully detected +1500V and -1500V system-level ESD zapping voltage under indirect contact-discharge test mode.

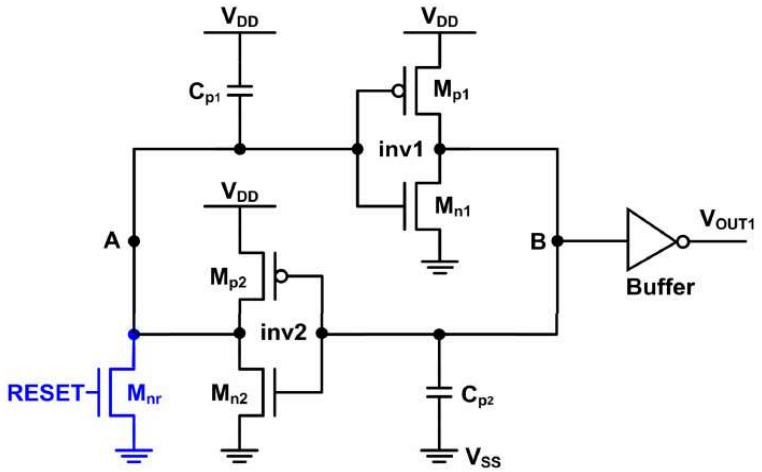


Fig. 3.1 Previous on-chip transient detection circuit (1).

Fig. 3.2 shows another on-chip transient detection circuit [27]. The NMOS (M_{nr}) is designed as reset device to provide the initial state of the proposed circuit. C_p is the parasitic capacitance on node V_1 of this circuit. Under normal operation, node V_x is biased at V_{DD}. When the system-level ESD event comes, the voltage of V_x has much slower voltage response then the Voltage of V_{DD} due to the RC delay circuit. Then M_{p1}, which is turned on due to the voltage delay, will charge node V_1 to logic "1". Therefore, the on-chip transient detection circuit can successfully detect and memorize the

occurrence of electronic transient disturbance. However, after the ESD events, node V_1 will be leaked down though the parasitic capacitor C_{p1} because M_{p1} and M_{n1} will be both switch to "OFF" state at this moment. The discharge time of V_1 can be estimated by the parasitic capacitor and the leakage current parameter. With a 0.3 pF parasitic capacitor in this design and process-depended parameter leakage current, the leaking down time is about 10ms. Of course, this time is enough for the firmware check and system recovery.

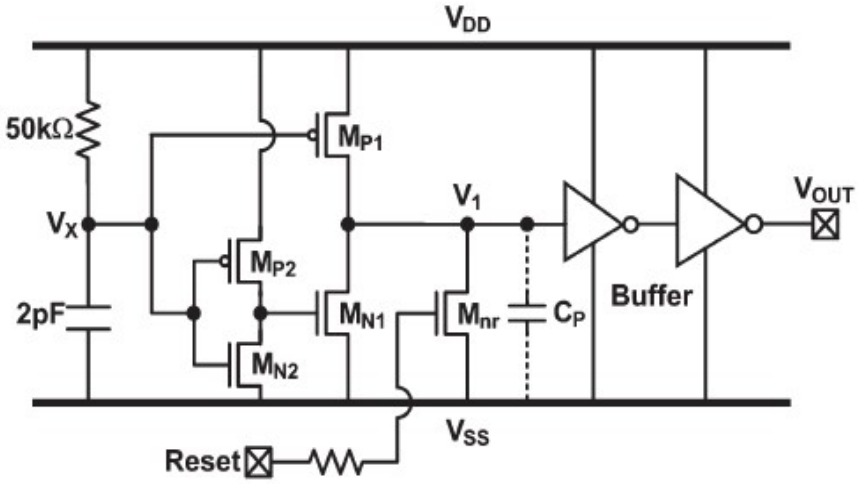


Fig. 3.2 Previous on-chip transient detection circuit (2).

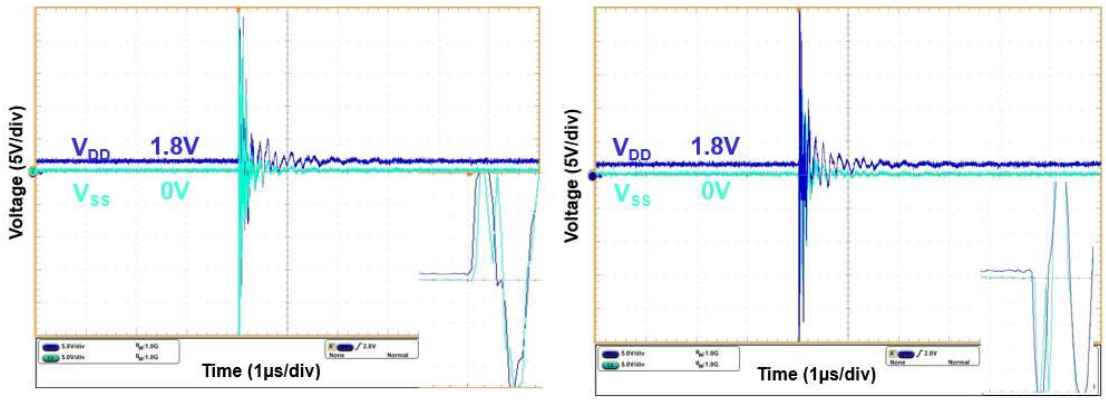
Generally, the detection sensitivity of previous on-chip transient detection circuit (1) against the system-level ESD is only +/- 1500V. By using the RC circuit structure with a larger time constant, the previous on-chip transient detection circuit (2) could detect +/- 200V system-level ESD zapping voltage and +/- 200V EFT zapping voltage, but there is leakage issue in this design. Thus, a new transient detection circuit, which has better detection sensitivity and no leakage issue, is required.

3.1.2 Simulation Parameter of System-Level ESD Test

The transient voltage coupled on power (V_{DD}) and ground (V_{SS}) lines of CMOS ICs has been investigated under system-level ESD test. Fig. 3.3 shows the measured

voltage waveforms of V_{DD} and V_{SS} under system-level ESD test with indirect-contact discharge test mode. The voltage level of V_{DD} and V_{SS} line cannot keep its normal level and performs as a positive-going (negative-going) under-damped waveform during the positive (negative) system-level ESD test. According to the measured results, a sinusoidal time-dependent voltage source with a damping factor parameter is used to simulate the circuit performance under system-level ESD tests. This source as Fig.3.4 shows can be described as below equation:

$$V(t) = V_0 + V_A \times \sin\left(2\pi D_{Freq}(t - t_d)\right) \times exp(-(t - t_d)D_{Facto}\ ) \quad (1)$$



(a) (b)

Fig. 3.3 Measured voltage waveforms with system-level ESD test voltage of (a) +2 kV, and (b) -2 kV.

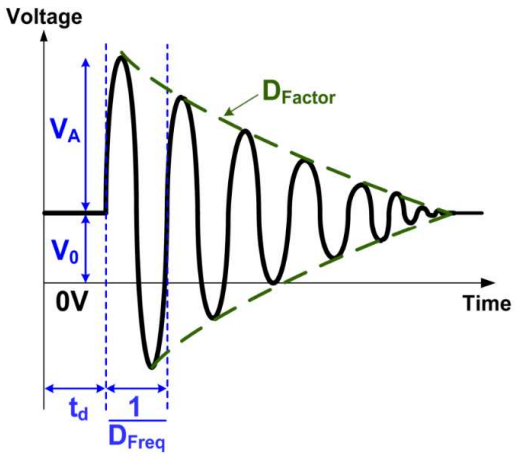


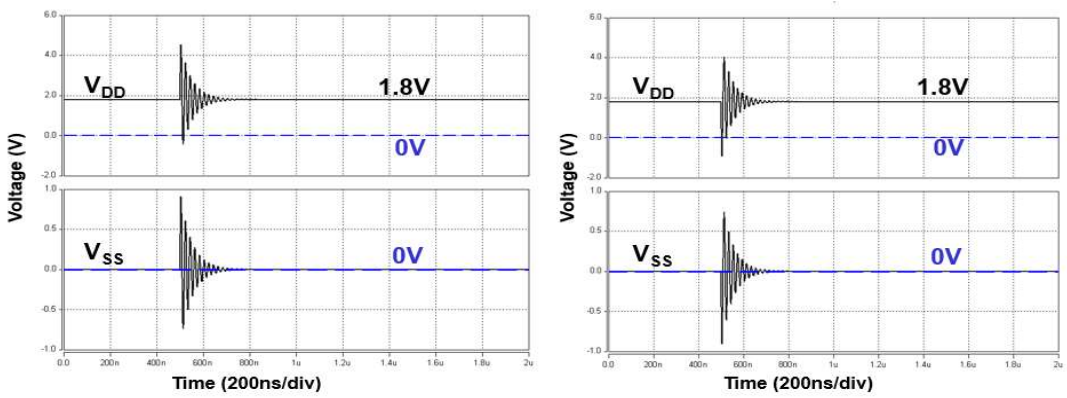
Fig. 3.4 The specific time-dependent underdamped sinusoidal waveform applied on the power and ground lines to simulate the disturbance under system-level ESD zapping.

Table 3.1 gives the parameter definitions and values of this underdamped sinusoidal voltage source. With the proper parameter values, this voltage source can be used in HSPICE simulation to simulate the electrical transient waveforms under system-level ESD tests. Positive (negative) polarity of parameter V_A simulates the positive-going (negative-going) system-level ESD test. Same value of time delay (t_d), damping factor (D_{Factor}) and damping frequency (D_{Freq}) are choose corresponding to the measured transient voltage waveforms in Fig. 3.3 (a) and (b). Therefore, Fig. 3.5 shows the voltage waveforms of positive zapping and negative zapping condition used in HSPICE simulation.

Table 3.1

Parameter definition and value of underdamped sinusoidal voltage waveform

Parameter	Definition	Value
V_0	Initial DC Voltage	1.8V for V_{DD}, 0V for V_{SS} line
V_A	Voltage Amplitude	Depends on the test level(+/-)
t_d	Time Delay	500 ns
D_{Factor}	Damping Factor	$2x10^{-7}$ s^{-1}
D_{Freq}	Damping Frequency	50 MHz

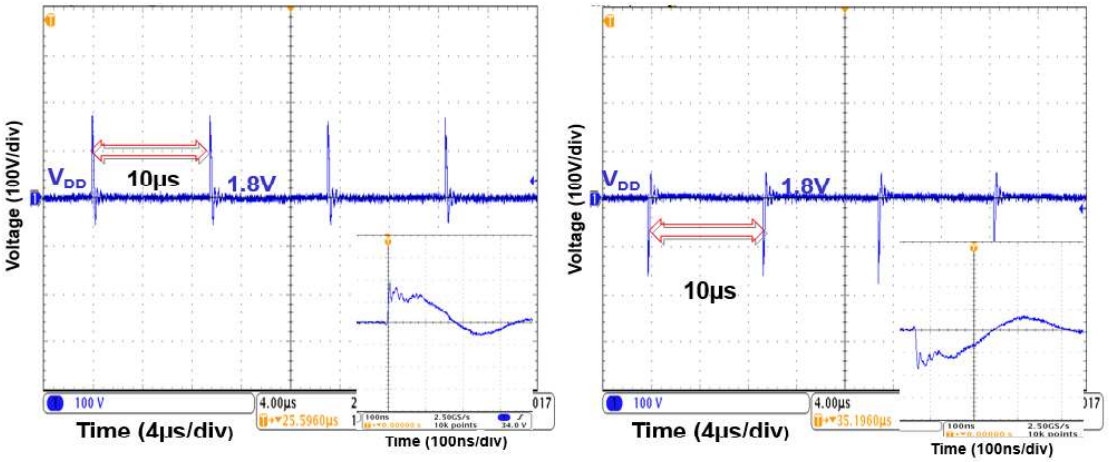


➢ **Positive zapping** ➢ **Negative zapping**

Fig. 3.5 Positive and negative system-level ESD zapping condition in HSPICE simulation.

3.1.3 Simulation Parameter of EFT Test

The measured voltage waveforms of power line under EFT tests with direct coupling test mode are shown in Fig. 3.6. The repetition rate of EFT voltage pulses is 100 kHz which closer to reality. Therefore, the period of pulses is 10μs. Generally, the single pulse has a rise time about 5ns and the pulse duration (time interval at half of the peak EFT voltage) about 50ns. To simulate the response of on-chip transient detection circuit under EFT tests, an exponential time-dependent voltage pulse coupled to power line is used as Fig. 3.7 shown.



(a) (b)

Fig. 3.6 Measured voltage waveform with EFT test voltage of (a) +200V, and (b) -200V.

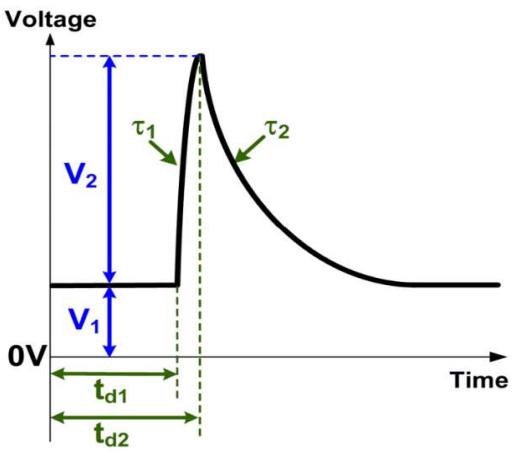


Fig. 3.7 The specific time-dependent exponential pulse waveform applied on the power lines to simulate the disturbance under EFT zapping.

Table 3.2

Parameter definition and value of the exponential time-dependent voltage waveform

Parameter	Definition	Value
τ_1	Rise time constant	3ns
τ_2	Fall time constant	25ns
t_{d1}/t_{d2}	Rise/Fall time Delay	td1-td2=10ns
V_1	Initial DC voltage	Same as V_{DD}
V_2	Exponential pulse voltage	Depends on the test level(+/-)

Table 3.2 is the parameter explanations and values of the exponential time-dependent voltage source. This voltage source can be expressed as two equations.

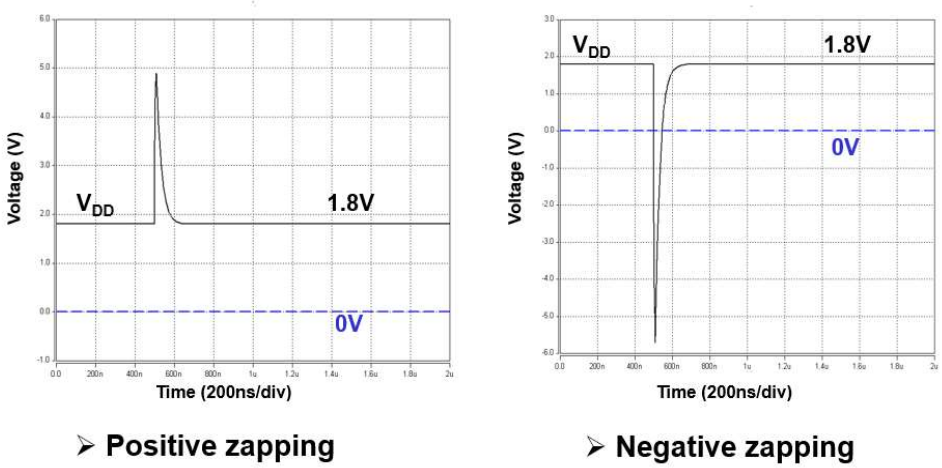
For the rising edge of the exponential time-dependent voltage pulse:

$$V_{Pr}(t) = V_1 + (V_2 - V_1) \times \left[1 - exp\left(-\frac{t-t_{d1}}{\tau_1}\right)\right], \text{ when } t_{d1} \le t \le t_{d2}. \quad (2)$$

For the falling edge of the exponential time-dependent voltage pulse：

$$V_{Pf}(t) = V_1 + (V_2 - V_1) \times \left[1 - exp\left(-\frac{t - t_{d1}}{\tau_1}\right)\right] + (V_1 - V_2) \times \left[1 - exp\left(-\frac{t-t_{d2}}{\tau_2}\right)\right], \text{ when } t \ge t_{d2}. \quad (3)$$

Same parameters of rise-time constant, fall-time constant, rise-time delay and fall-time delay are used in HSPICE simulations. Different polarity and value of V_2 (exponential pulse voltage value) are used to simulate the positive and negative EFT zapping conditions. Due to the shielding plate designed in reality microelectronic products, the EFT-induced electrical-transient disturbance in the inside CMOS ICs can be degraded compare with the original test. Fig. 3.8 shows the waveform used in HSPICE for EFT tests simulation.



➢ **Positive zapping** ➢ **Negative zapping**

Fig. 3. 8 Positive zapping and negative EFT zapping condition in HSPICE simulation.

3.2 Proposed New On-Chip Transient Detection Circuit

It has been proven that a RC structure with larger delay time constant can detect the transient voltage coupled on power lines more effectively. In addition, a well-designed latch structure circuit can successfully memorize the state of detected occurrence of electronic transient disturbance. According to the previous researches, a new on-chip transient detection circuit has been proposed. The sensitivity to transient noises coupled on power lines of this new circuit should be enhanced and the voltage leaking down issue should be avoided.

3.2.1 Circuit Implementation

The circuit diagram of newly proposed on-chip transient detection circuit is as Fig. 3.9 shown. The main part of circuit comprise with a resistor (R), an inverter structure (M_{p2} and M_{n2}), a feedback MOSFET (M_{n1}) and a reset device (M_{nr}). M_{nr} is designed as the reset device to provide the initial state of proposed circuit, so the metastable state of V_o can be avoided. The resistor R, M_{n1}, and the inverter (M_{p2} and M_{n2}) compose a latch circuit as the memory cell of the transient detection circuit. R and the parasitic

capacitors of node V_X (C_P) constitute the RC delay structure. Under the normal operation, V_O is set to logic "0" by the reset device M_{nr}, M_{n1} is turned off so that node V_x is biased to V_{DD} though the resistor. M_{p2} is turned off and M_{n2} is turned on. Thus, the output voltage level of V_{OUT} is locked to logic "0" though the buffers. When electrical disturbance coupled to power lines under system-level ESD event or EFT tests, due to the RC delay time constant, the voltage of node V_x will response much slower than the voltage coupled to V_{DD}. Therefore, the device M_{p2} is turned on to pull up the voltage level of node V_O. With the positive feedback device M_{n1}, the voltage level of node V_X will be pulled low to logic "0" finally. M_{p2} will be turned on and M_{n2} will be turned off. Thus, when the system-level ESD and EFT events ended, the node V_O will be latched to logic "1". Therefore, the occurrence of electrical transient disturbance can be detected and stored. The changed output state can be sent to firmware as the recovery index of system. When the recovery procedure of system is totally executed, the reset signal V_{RESET} is then used to release output state of the transient detection circuit from logic "1" to logic "0" again for the next system-level ESD and EFT events detecting. It is obviously that there are no leaking down occurs whether normal or detecting operation of the proposed circuit.

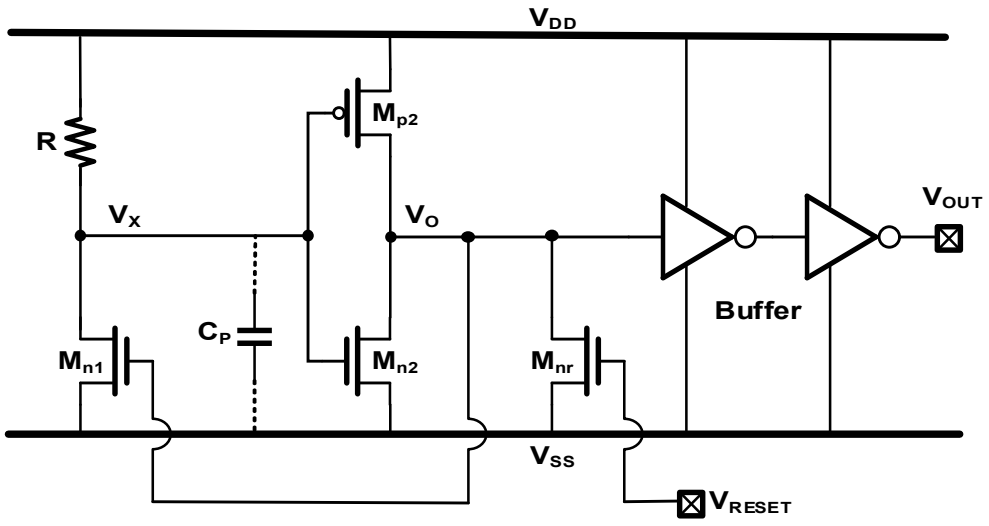


Fig. 3.9 Schematic diagram of the proposed new transient detection circuit.

According to the operation of the proposed transient detection circuit, the time constant of R and C_P shall be a larger value to enhance the sensitivity of detecting the electrical transients. To latch the changed state quickly, a larger size ratio of M_{n1} and M_{p2} are designed. Table 3.3 list the device dimensions (W/L) used in the proposed transient detection circuit. The time constant of the RC delay structure is about 86ns. To adjust this time constant, resistor (R) value or size of M_{n2} should be modified.

Table 3.3
Device dimensions used in the proposed transient detection circuit

Device	Parameter
R	50K
M_{n1}	5/0.18μm
M_{p2}	5/0.18μm
M_{n2}	10/10μm

3.2.2 HSPICE Simulation Results under System-Level ESD Zapping

The underdamped sinusoidal time-dependence voltage source is used for HSPICE simulation to investigate the performance of proposed transient detection circuit. Same parameter of D_{Factor}=2x10^7s-1, D_{Freq}=50 MHz, t_d=500 ns of voltage source coupled on V_{DD}/V_{SS} lines are used for both positive and negative system-level ESD tests simulation. In these simulations, different voltage amplitudes and polarity of V_{DD}/V_{SS} are used to simulate the condition of V_{DD} and V_{SS} overshooting under system-level ESD tests.

Fig. 3.10 shows the simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the proposed transient detection circuit with a positive-going underdamped sinusoidal voltage source. To simulate the overshooting voltage coupled on power lines under positive system-level ESD test, the positive-going underdamped sinusoidal voltage with V_A of +3V on V_{DD} and V_A of +1V on V_{SS} are used. From the waveform, the voltage of V_{DD} level is kept at 1.8V with a relatively V_{SS} of 0V in initial state. Under system-

level ESD stress, V_{DD} (V_{SS}) begins to increase rapidly from 1.8V (0V). At same time, due to the disturbance on V_{DD} (V_{SS}) lines, V_{OUT} also acts as a positive underdamped sinusoidal voltage waveform during the simulated system-level ESD events. After the system-level ESD event ends, V_{DD} (V_{SS}) returns to 1.8V (0V), V_{OUT} can keep to 1.8V until the next V_{RESET} comes. As a result, the proposed transient detection circuit successfully detect and store the occurrence of electrical transient disturbance coupled on V_{DD} and V_{SS}.

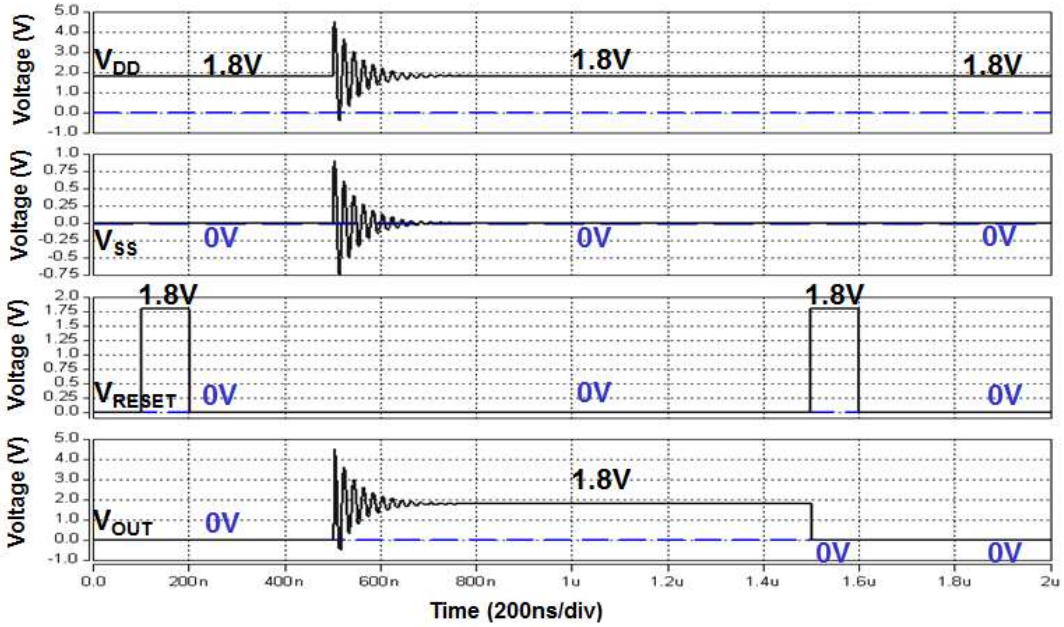


Fig. 3. 10 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the proposed transient detection circuit under positive system-level ESD test simulation.

To simulate the negative system-level ESD zapping condition, the waveform of V_{DD}, V_{SS}, V_{RESET} and V_{OUT} of proposed transient detection circuit is shown in Fig. 3.11. The negative-going underdamped sinusoidal voltage with V_A of -3V on V_{DD} and V_A of -1V on V_{SS} are used to simulate this test. From the waveform, under the negative system-level ESD zapping condition, V_{OUT} is disturbed simultaneously during the disturbance of V_{DD} and V_{SS}, and finally changed the voltage level from 0V to 1.8V until the next V_{RESET} signal comes.

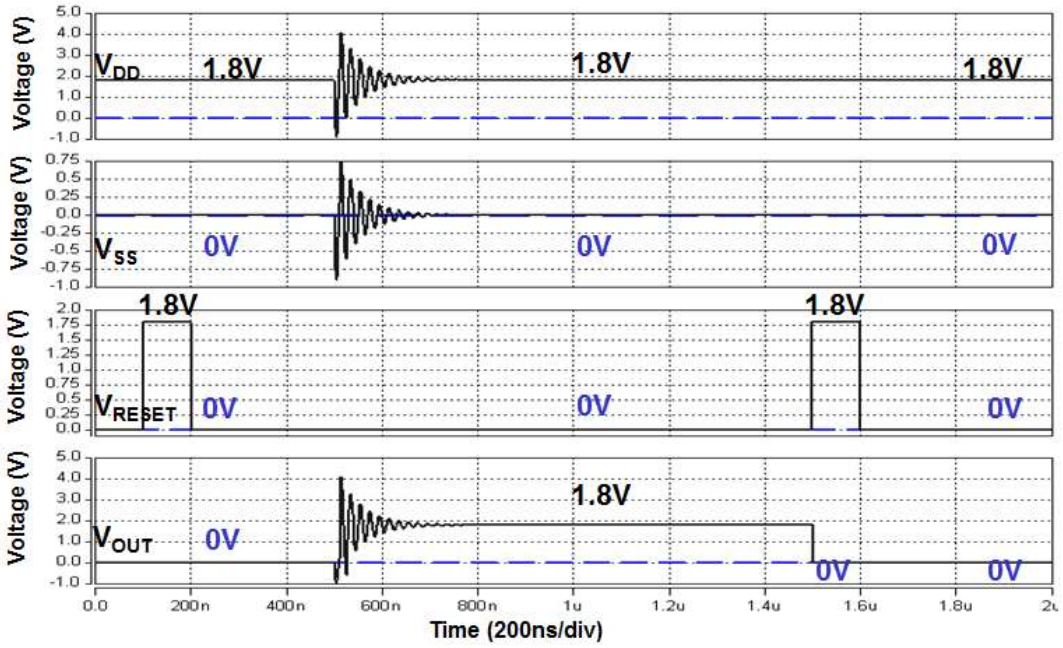


Fig. 3. 11 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the proposed transient detection circuit under negative system-level ESD test simulation.

3.2.3 HSPICE Simulation Results under EFT ESD Zapping

The simulated V_{DD}, V_{RESET} and V_{OUT} waveforms of the new proposed on-chip transient detection circuit with a positive exponential pulse transient disturbance coupled on V_{DD} line are show in Fig. 3.12. To simulate the positive zapping EFT test, the exponential voltage with an amplitude of +5V is used. From the simulated waveform, the output voltage of V_{OUT} is initially set to 0V by the V_{RESET} signal. When the positive EFT pulse coupled to V_{DD} lines, V_{OUT} also acts as a positive exponential voltage pulse waveform and finally keep to 1.8V. When V_{DD} voltage returns to its normal voltage level of 1.8V, V_{OUT} can latch on 1.8V level. When another V_{RESET} signal comes, V_{OUT} will be pulled low to 0V to detect next electronic transient disturbance. As a result, the new proposed on-chip transient detection circuit can successfully detect and memorize the occurrence of simulated positive EFT-induced exponential pulse transient disturbance.

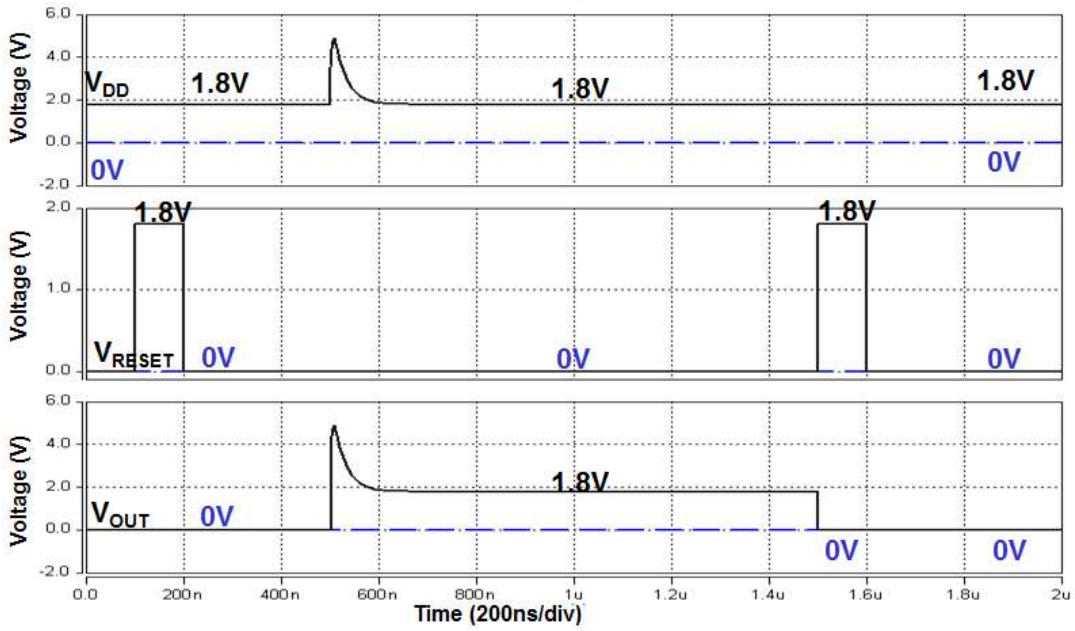


Fig. 3. 12 Simulated V_{DD}, V_{RESET} and V_{OUT} waveforms of the proposed transient detection circuit under positive EFT test simulation.

The simulated V_{DD}, V_{RESET} and V_{OUT} waveforms of the newly proposed on-chip transient detection circuit with a negative exponential pulse transient disturbance coupled on V_{DD} line are show in Fig. 3.13. To simulate the negative zapping EFT test, the exponential voltage with an amplitude of -6V is used. From the simulated waveform, the output voltage of V_{OUT} is initially set to 0V by the V_{RESET} signal. When the negative EFT pulse coupled to V_{DD} lines, V_{OUT} also acts as a negative exponential voltage pulse waveform and finally keep to 1.8V. When V_{DD} voltage returns to its normal voltage level of 1.8V, V_{OUT} can latch on 1.8V level. When another V_{RESET} signal comes, V_{OUT} will be pulled low to 0V to detect next electronic transient disturbance. As a result, the new proposed on-chip transient detection circuit can successfully detect and memorize the occurrence of simulated negative EFT-induced exponential pulse transient disturbance.

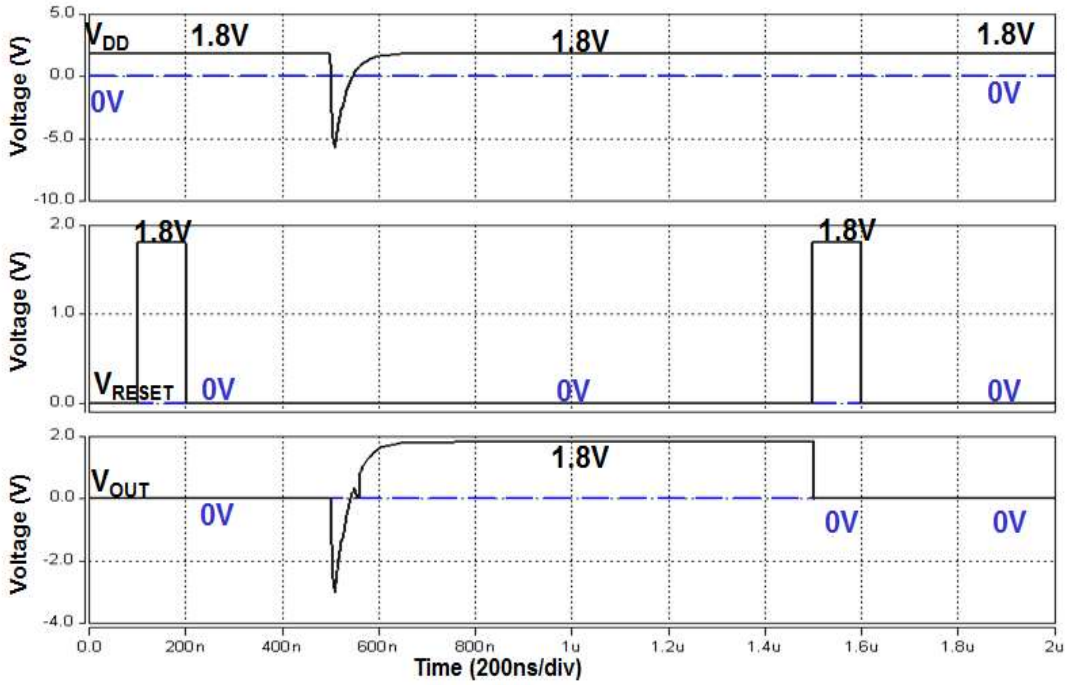


Fig. 3. 13 Simulated V_{DD}, V_{RESET} and V_{OUT} waveforms of the proposed transient detection circuit under negative EFT test simulation.

3.3 Measurement Results

The newly proposed on-chip transient detection circuit has been designed and fabricated in a 0.18um CMOS process with 1.8-V devices. Fig. 3.14 is the photo of fabricated chip. The silicon area of this transient detection circuit without PAD is 40μm* 50μm. To evaluate the function of newly proposed on-chip transient detection circuit, system-level ESD gun and the EFT generator are used in system-level ESD test and EFT test respectively.

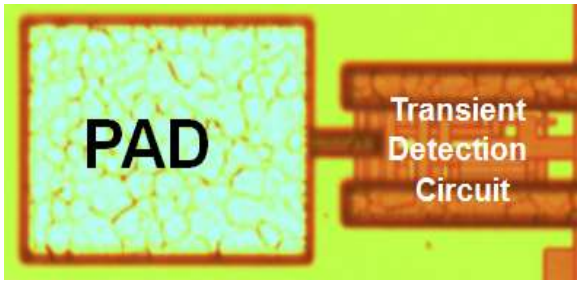
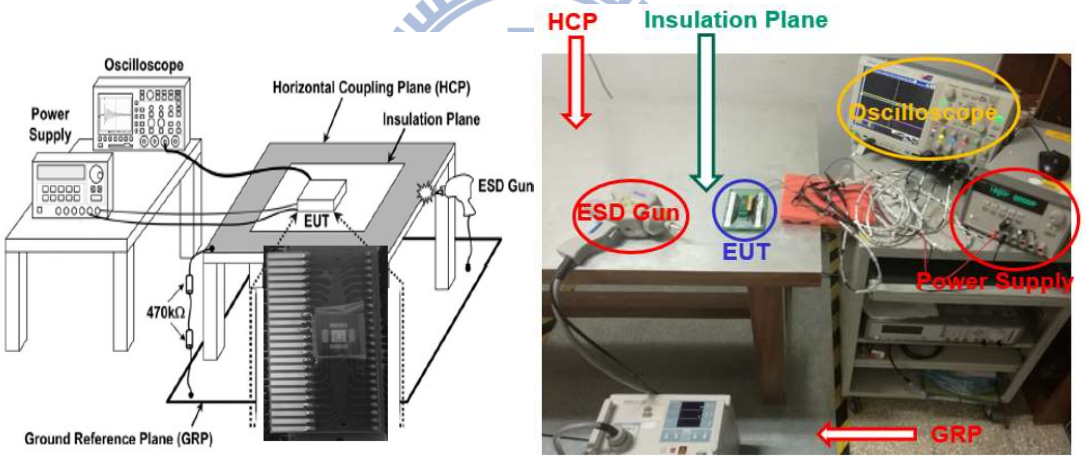


Fig. 3. 14 Die photo of the proposed on-chip transient detection circuit.

3.3.1 System-Level ESD Test

According to the test setup clarified in IEC 61000-4-2 standard, the block diagram of system-level ESD indirect contact-discharge test setup is shown as Fig. 3.15 (a), while the actual setup is shown as Fig. 3.15 (b). The EUT is placed on a wooden table which standing on the ground reference plane (GRP). Insulation plane is used to insulate the EUT and the horizontal coupling plane (HCP) placed on the table. ESD gun is used as the system-level ESD generator. In additional, the discharge return cable of the ESD gun should be connected to the GRP directly and the HCP shall be connected to the GRP with two 470kohm resistors in series. Under the indirect contact coupling test mode, the head of ESD gun zapped on the edge of HCP. The electrical transient disturbance will couple to EUT though the HCP.



(a) Block Diagram (b) Test setup

Fig. 3. 15 Measurement setup for a system-level ESD test with indirect contact-discharge test mode: (a) Block diagram, and (b) Test setup.

Fig. 3.16 shows the mearsured V_{DD}, V_{SS} and V_{OUT} waveforms of the new propoesd on-chip transient detection circuit under the +0.2 kV system-level ESD test voltgae. The ESD stress under system-level ESD test couppled to the power (V_{DD}) and ground (V_{SS}) line of the proposed transient detection circuit disturb the normal voltgae level of them. The voltage level of V_{DD} (V_{SS}) rapidly increases from 1.8V (0V), and the voltage

level of V_{OUT} also increase simultaneously. Finally, the output voltgae of the new propesd transient detection circuit (V_{OUT}) transist from 0V to 1.8V. Therefore, the detection function of propoesd transient detection circuit is succesfully verified by the positive system-level ESD test.

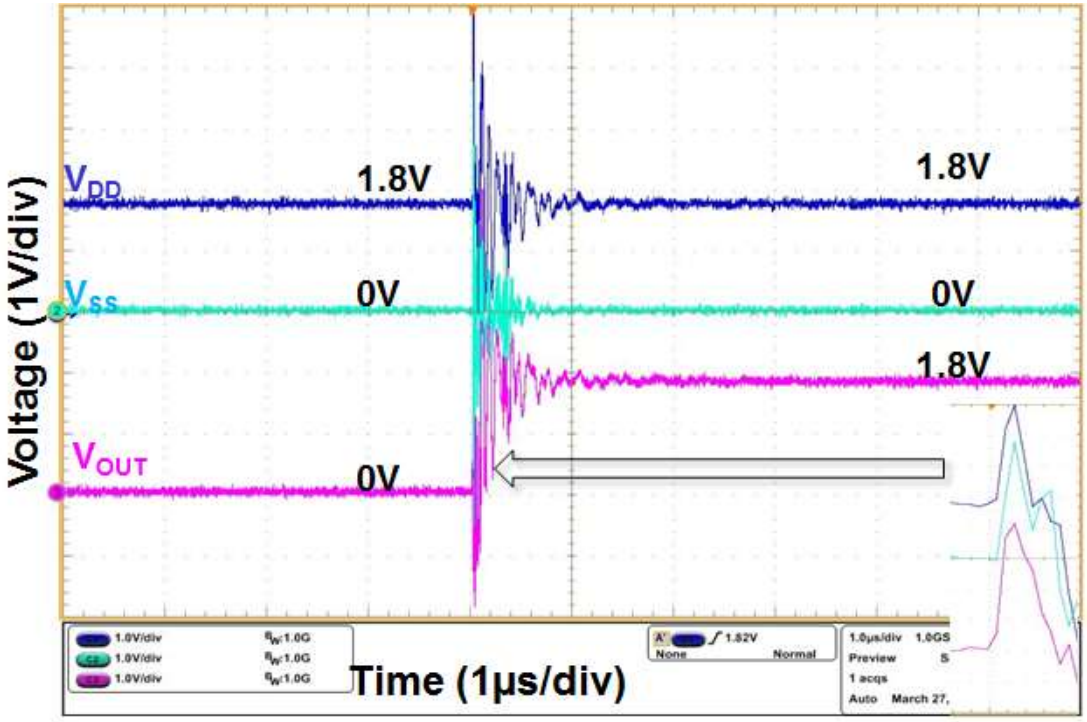


Fig. 3. 16 Measured V_{DD}, V_{SS} and V_{OUT} waveforms of the propoesd transient detection circuit under system-level ESD test with zapping voltage of +0.2 kV.

Fig. 3.17 shows the mearsured V_{DD}, V_{SS} and V_{OUT} waveforms of the new propoesd on-chip transient detection circuit under the -0.2 kV system-level ESD test voltgae. The ESD stress under system-level ESD test couppled to the power (V_{DD}) and ground (V_{SS}) line of the proposed transient detection circuit disturb the normal voltgae level of them. The voltage level of V_{DD} (V_{SS}) rapidly decreases from 1.8V (0V), and the voltage level of V_{OUT} also increase simultaneously. Finally, the output voltgae of the new propesd transient detection circuit (V_{OUT}) transist from 0V to 1.8V. Therefore, the detection function of propoesd transient detection circuit is succesfully verified by the negative system-level ESD test.

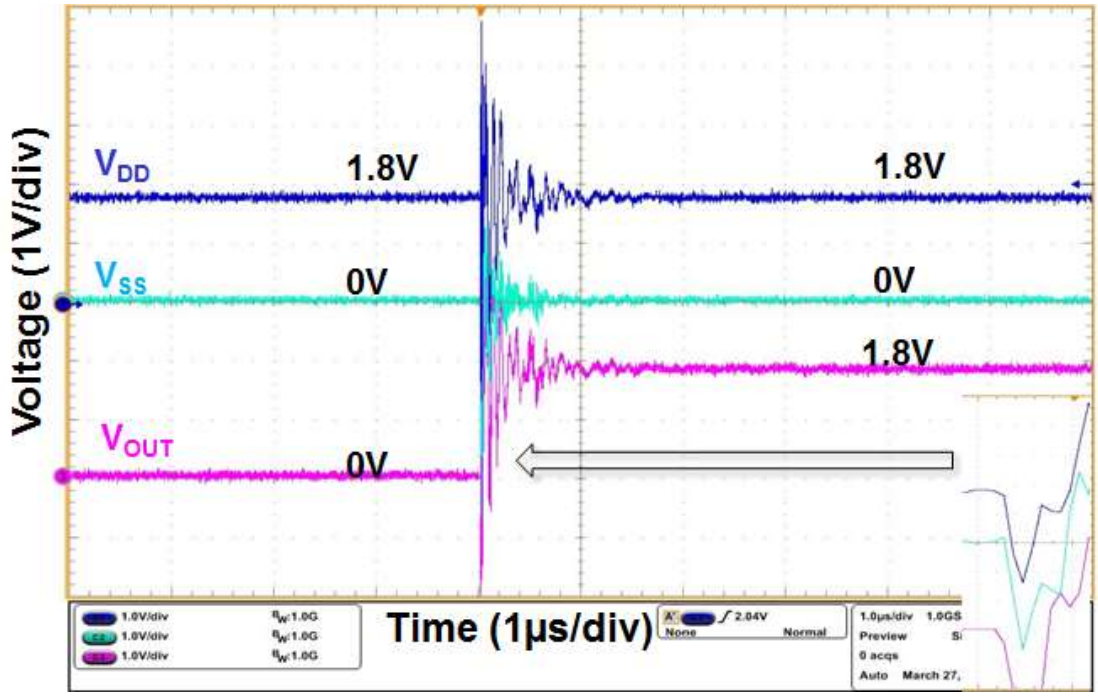
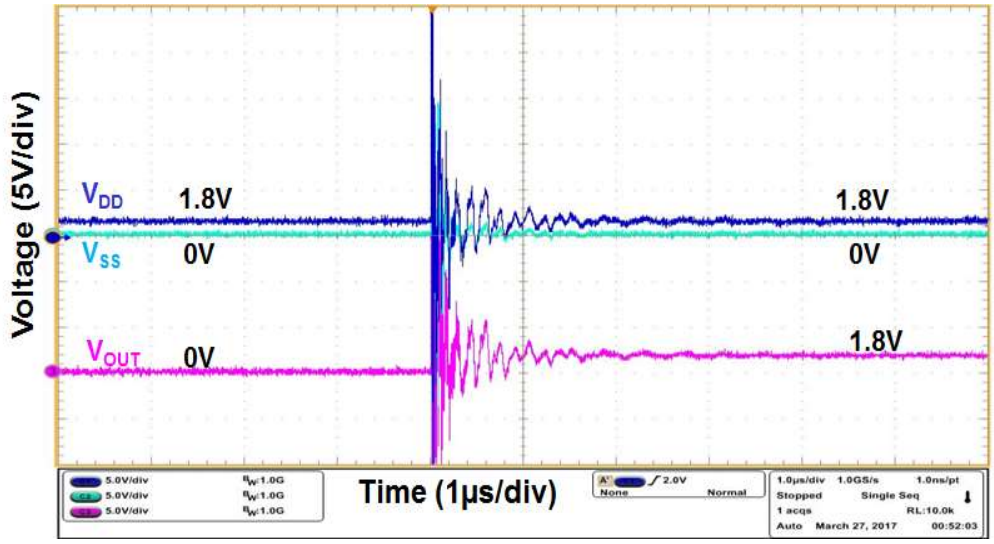
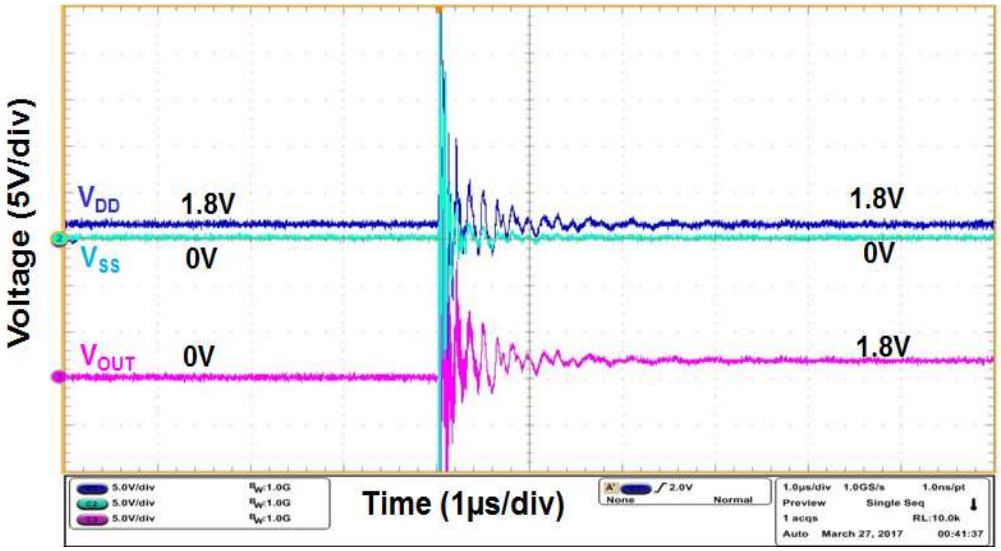


Fig. 3. 17 Measured V_{DD}, V_{SS} and V_{OUT} waveforms of the propoesd transient detection circuit under system-level ESD test with zapping voltage of -0.2 kV.

To verify the perfomance of the propoesd transient detection circuit with test level specified by IEC 61000-4-2, the measured V_{DD}, V_{SS} and V_{OUT} transient responses are shown in Fig. 3.18 (a) and (b) , respectively. The system-level ESD voltgae of Fig. 3.18 (a) is +2 kV and the ESD voltgage of Fig. 3.18 (b) is -2 kV. From the waveforms, the transisent detection circuit can sense the positive or negetive-going electrical transient disturbance on the V_{DD} and V_{SS} lines and memorize the occurrence of these system-level ESD events. Therefore, the function of the proposed transient dection circuit under +2 kV and –2 kV system-level ESD zapping voltage has been confirmed.



(a)



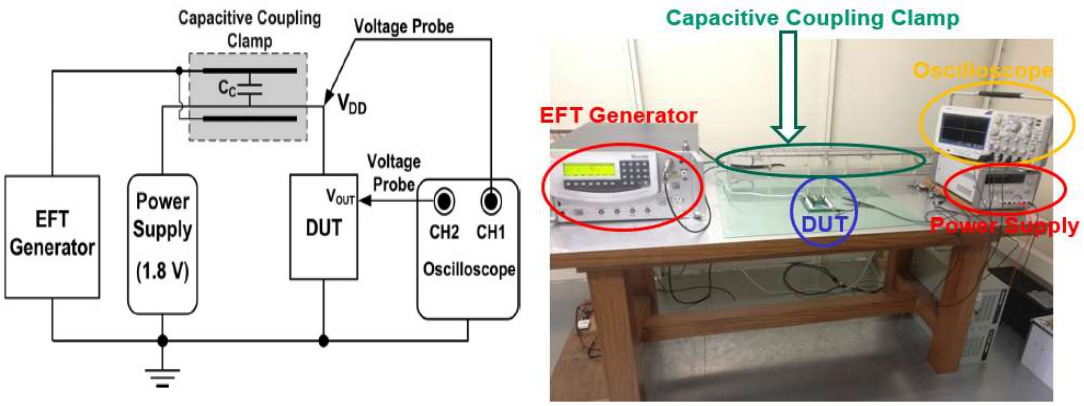
(b)

Fig. 3. 18 Measured V_{DD}, V_{SS} and V_{OUT} waveforms of the propoesd transient detection circuit under system-level ESD test with zapping voltage of: (a) +2 kV and (b) -2 kV.

3.3.2 EFT Test

The IEC 61000-4-4 defines the test methodology of EFT tests. In order to simulate the EFT-induced transient disturbance coupled to CMOS ICs inside the microelectronics products, the capacitive coupling clamp is used in this work. Fig. 3.19 shows the measurement diagram (a) and setup (b) for EFT test combined with capacitive coupling clamp, respectively. The output of EFT generator connect to the

end of capacitive coupling clamp directly. The power cables from the power supply equipment are placed inside the capacitive coupling clamp, and the capacitive coupling clamp itself should be closed as much as possible to provide maximum coupling capacitance between the clamp and the cable. The typical capacitance between the cable and clamp is from 50 pF to 200 pF. Thus, the EFT testing voltage will be coupled to the power cable via the capacitor of capacitive coupling clamp. The digital oscilloscope can monitored the voltage response of V_{DD} and V_{OUT} during the EFT tests. With this setup, the circuit performance of proposed on-chip transient detection circuit under EFT tests can be evaluated.

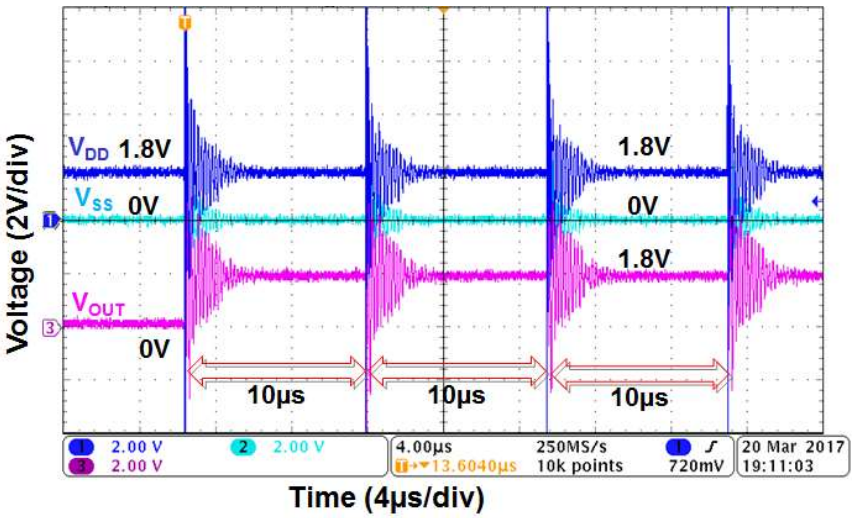


(a) (b)

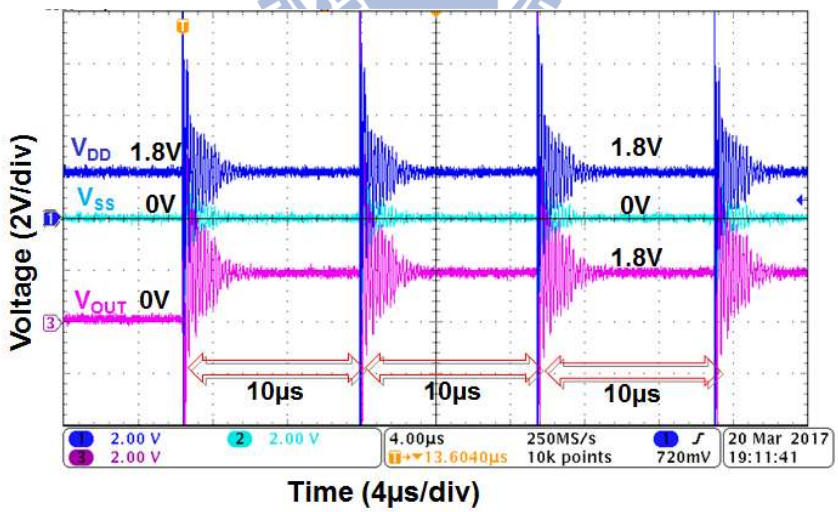
Fig. 3. 19 Measurement setup for an EFT test combined with capacitive coupling clamp: (a) Block diagram, and (b) Test setup.

Fig. 3.20 (a) shows the V_{DD}, V_{SS} and V_{OUT} waveform under the EFT test voltage of +200V with a repetition rate 100 kHz. The period of the pulses is 10 μs. From the waveform, V_{DD} and V_{SS} acts like a positive-going underdamped sinusoidal voltage waveform when the EFT pulse coupled on. In addition, V_{OUT} is influenced simultaneously with these transients. After the EFT pulse, the voltage level of V_{OUT} transits from 0V to 1.8V, and keep at 1.8V until the total EFT test ended.

Fig. 3.20 (b) shows the V_{DD}, V_{SS} and V_{OUT} waveform under the EFT test voltage of -200V with a repetition rate 100 kHz. The period of the pulses is 10 μs. From the waveform, V_{DD} and V_{SS} acts like a negative-going underdamped sinusoidal voltage waveform when the EFT pulse coupled on. In addition, V_{OUT} is influenced simultaneously with these transients. After the EFT pulse, the voltage level of V_{OUT} transits from 0V to 1.8V, and keep at 1.8V until the total EFT test ended.



(a)



(b)

Fig. 3. 20 Measured V_{DD}, V_{SS} and V_{OUT} waveforms of the propoesd transient detection circuit under EFT tests with zapping voltage of: (a) +200 V, and (b) -200V by combing with capacitive coupling clamp.

As a result, the output voltage level of V_{OUT} can change its normal level from 0V to 1.8V under the positive or negative EFT zapping test with the capacitive coupling clamp. Therefore, the proposed transient detection circuit can successfully detect and memorize the occurrence of positive or negative EFT induced transient disturbance.

3.4 System Application

The hardware/firmware co-design solution has been proven as an effective method to solve the system-level ESD and EFT issues in microelectronic products equipped with CMOS ICs. The proposed on-chip transient detection circuit can be co-designed with firmware to execute the system recovery procedure. Therefore, the automatically recovery of system after system-level ESD test and EFT test can be realized.

Fig. 3.21 gives an example flowchart of system recovery combined with transient detection circuit. The index of firmware and output of transient detection circuit (V_{OUT}) are set to "0" by power-on reset (POR) circuit. The system executes the normal reset procedure. When the electrical transients happens, the voltage level of V_{OUT} should be changed to logic "1". Then an index "1" will be sent to firmware to execute the recovery procedure. Consider to the mistrigger condition of power-on reset circuit during the fast electrical transient events, an OR gate is also added in the flowchart. The V_{OUT} signal of transient detection circuit and the output signal of POR are connected as the input signals of this OR gate. Whether the POR circuit be mistriggered or not by the electrical transients, the system can still execute the recovery procedure. After the recovery procedures, the output state of transient detection circuit and firmware should be reset to "0" as soon as possible for the next system-level ESD or EFT event. From this flowchart, the proposed transient detection circuit can help system recovering from the

abnormal condition due to system-level ESD or EFT test. Therefore, a “Class B” evaluation of micro products under system-level ESD and EFT tests can be passed.

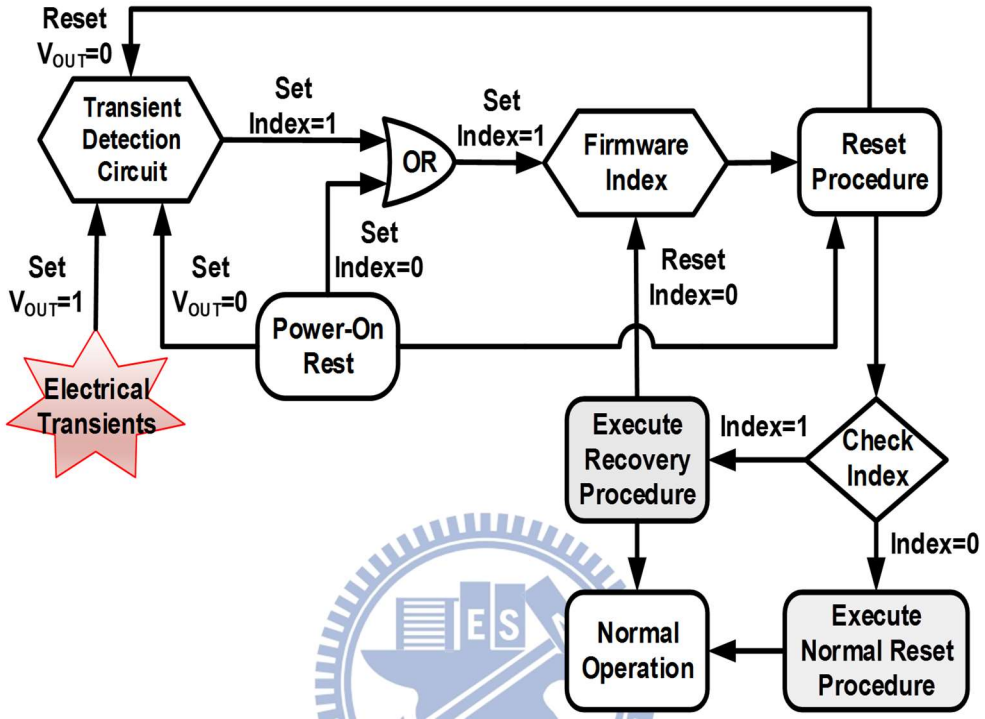


Fig. 3. 21 Firmware flowchart to recover system when electrical transients happen.

3.5 Summary

A novel on-chip transient detection circuit has been proposed in this section. The transient detection circuit has been designed and fabricated in a 0.18-μm CMOS process with 1.8-V devices. The performance of the detection circuit has been investigated by HSPICE simulation and verified by the measurement results. The test methods include system-level ESD test with indirect contact-discharge and EFT test combined with capacitive coupling clamp. It has been proven that positive or negative-going ESD-induced fast electrical transients can be detected and memorized by the proposed transient detection circuit. Table 3.4 list the comparison of previous designs and newly

proposed design, the detection sensitivity of this work against the fast electrical transient disturbance is enhanced with the larger time constant of RC delay circuit and the voltage leaking down issue is avoided. In system application, system recovery procedure co-designed with the proposed transient detection circuit and POR circuit can provide an effective solution against the system malfunction due to a system-level ESD or EFT event.

Table 3.4

Comparison between previous designs and newly proposed design

	Previous Design 1 [25]	Previous Design 2 [27]	Newly Proposed Design
Technology	0.13-μm CMOS process	0.18-μm CMOS process	0.18-μm CMOS process
Detection Sensitivity (System-level ESD)	+/- 1500V	+/- 200V	+/- 200V
Detection Sensitivity (EFT)	n/A	+/- 200V	+/- 200V
Leakage Issue	No	Yes	No
Reset Function	Required	Required	Required

Chapter 4

Design of New On-Chip Self-Reset Transient Detection Circuit

The prior and newly proposed on-chip transient detection circuits both operate with reset devices. The reset device provides the initial state and the reset function of the on-chip transient detection circuit. In system recovery flow, an additional reset data path is required in the hardware/firmware co-design with these detecting circuits. In addition, some logic gates are also added in to avoid mistriggering of power-on reset circuit during the system-level ESD or EFT events. However, all the on-chip signal or circuits are likely to be disturbed by the fast electrical transients due to system-level ESD or EFT events. Therefore, the prior and new proposed on-chip transient detection circuits co-designed with firmware will be risky due to these mistriggering condition. Considering that, an on-chip self-reset transient detection circuit has been proposed.

4.1 Background

4.1.1 Prior Arts

Fig. 4.1 shows a CR based on-chip transient detection circuit [29]. The capacitor C, the resistor R and MOSFET M_{n1} compose the detection part to detect the fast electrical transients. Two inverter (INV_1 and INV_2) designed as a static latch structure to store the changed state under system-level ESD and EFT tests. M_{nr} is the reset device to provide the initial state and reset function. In normal operation, the voltage of node V_B is pulled down by device M_{nr} and latch to static logic “0” by the

static latch. Therefor, node V_A is kept at logic "1", node V_G is biased to V_{SS} by the resistor R, M_{n1} is turned off. During the system-level ESD or EFT events, the voltage level of node V_G will be coupled with positive voltage by MOSFET capacitor coupling. Then M_{n1} will be turned on to pull down the voltage level of node V_A by the overshooting ESD voltages. Therefore, the logic level stored at node V_A can be changed from logic "1" to logic "0". With the buffer inverters, the voltage of output (V_{OUT}) is finally changed from 1.8V to 0V. This on-chip transient detection circuit can successfully detect and store the occurrence of electrical transients due to system-level ESD or EFT test.

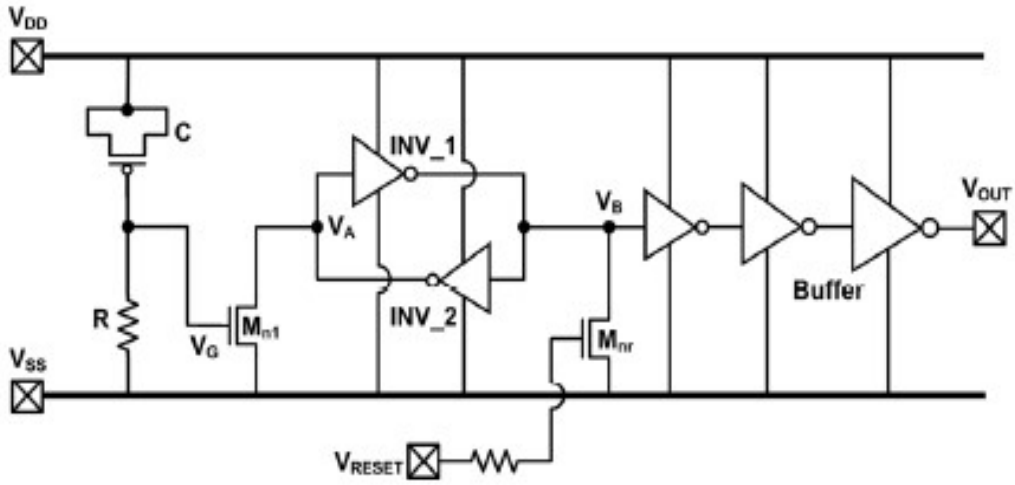


Fig. 4. 1 The on-chip CR-based transient detection circuit.

4.1.2 Simulation Parameter of System-Level ESD Test

From the measured voltage waveform of V_{DD} and V_{SS} under system-level ESD test with indirect-contact discharge test mode shown in Fig. 3.3, the sinusoidal time-dependent voltage source with a damping factor parameter is used to simulate the circuit performance under system-level ESD tests. This voltage source is given by:

$$\mathrm{V(t)} = V_0 + V_A \times \sin\left(2\pi D_{Freq}(t - t_d)\right) \times exp(-(t - t_d)D_{Facto}\ ) \qquad (1)$$

In HSPICE simulation, the same parameters of D_{Factor}=2x10^7s-1, D_{Freq}=50 MHz and t_d=500 ns are used, which is corresponding to the measured waveform shown in Fig. 3.3. The different polarity and amplitude of parameter V_A simulate the positive and negative system-level ESD test condition. In additional, the initial voltage parameter V_0 is 1.8V (0V) as the initial DC voltage of V_{DD} (V_{SS}) line of the proposed transient detection circuit.

4.1.3 Simulation Parameter of EFT Test

The measured voltage waveforms of power line under EFT tests with direct coupling test mode are shown in Fig. 3.6. To simulate the response of on-chip transient detection circuit under EFT tests, an approximated exponential time-dependent voltage pulse coupled to power line is used. This voltage source can be expressed as two equations:

For the rising edge of the exponential time-dependent voltage pulse:

$$V_{Pr}(t) = V_1 + (V_2 - V_1) \times \left[1 - exp\left(-\frac{t-t_{d1}}{\tau_1}\right)\right], \text{ when } t_{d1} \le t \le t_{d2}. \quad (2)$$

For the falling edge of the exponential time-dependent voltage pulse：

$$V_{Pf}(t) = V_1 + (V_2 - V_1) \times \left[1 - exp\left(-\frac{t-t_{d1}}{\tau_1}\right)\right]$$
$$+(V_1 - V_2) \times \left[1 - exp\left(-\frac{t-t_{d2}}{\tau_2}\right)\right], \quad \text{when } t \ge t_{d2}. \quad (3)$$

Same parameters of $\tau_1 = 3\ ns$, $\tau_2 = 25\ ns$, and $t_{d1} - t_{d2} = 10\ ns$ are used in HSPICE simulations, which is corresponding to the measured waveform shown in Fig. 3.6. Different polarity and amplitude of V_2 is used to simulate the positive and negative EFT zapping conditions. In additional, the initial voltage parameter V_1 is 1.8V as the initial DC voltage of V_{DD} line of the proposed transient detection circuit.

4.2 New On-Chip Self-Reset Transient Detection Circuit

It has been proven that a CR structure with large delay time constant can detect the transient voltage coupled on power lines. To realize the memorizing and self-resetting function of the transient detection circuit, a novel on-chip self-reset transient detection circuit has been proposed. This circuit is designed without reset devices.

4.2.1 Circuit Implementation

The proposed on-chip self-reset transient detection circuit is shown as Fig. 4.2. The CR-based transient detection circuit is designed to detect the system-level ESD-induced and EFT-induced transient disturbances without reset devices. C and R devices are composed as detection part of the circuit. The memory unit of circuit comprise two NMOS devices (M_{n1} and M_{n2}), two cross-coupled PMOS devices (M_{p1} and M_{p2}) and an inverter (INV). Two inverters are designed as buffer cells. During the normal operation, the voltage level of node V_X is biased to 0V by the resistor R, the voltage level of node V_{XB} is biased to 1.8V as the output of the inverter (INV). Therefore, M_{n1} is turned off and M_{n2} is turned on to pull down the voltage of node V_2. When the voltage level of node V_2 is lower enough, M_{p1} will be turned on to pull up the voltage level of V_1, and then M_{p2} will be turned off. Finally, the voltage level of node V_1 will be pulled high to logic "1" and voltage level of V_2 will be pulled low to logic "0". Through the buffer inverters, the initial output voltage of this self-reset transient detection circuit (V_{OUT}) will be kept to 0V. Under the system-level ESD or EFT event with an overshooting transient voltage, the node V_X will be coupled with positive voltage by capacitor coupling, the node V_{XB} will be coupled with negative voltage by INV. Then the NMOS device M_{n2} will be turned off, and M_{n1} will be turned on to pull low the voltage level of node V_1 to logic "0". The PMOS device M_{p2} acts as the positive feedback to pull up the

voltage level of V_2 to logic "1", M_{p1} will be turned off finally. The voltage of V_{OUT} will be changed from logic "0" to logic "1" with two buffers. When the system-level or EFT ESD events ends, it is obviously that the voltage of node V_X will be biased to 0V and V_{XB} will be biased to 1.8V. Therefore, M_{n1} is turned off and M_{n2} is turned on again. The voltage level of node V_2 will be pulled low by M_{n2} and the voltage level of node V_1 will be pulled high though the positive feedback. After a time constant, which is related to the positive feedback device M_{p1}, the output voltage of proposed transient detection circuit will be changed from 1.8V to 0V. Therefore, the proposed on-chip self-reset transient detection circuit successfully detects the occurrence of fast electrical transient events, and reset its voltage level to initial state itself.

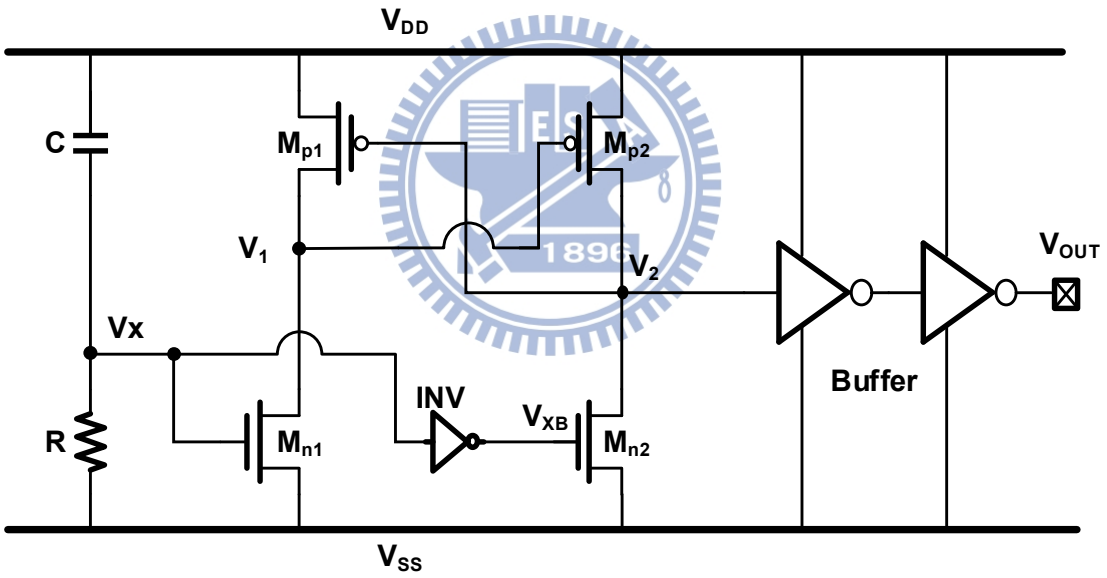


Fig. 4. 2 The proposed on-chip self-reset transient detection circuit.

As the operation of proposed on-chip self-reset transient detection circuit be analyzed, in order to detect the fast electrical transients more effectively, a larger size (W/L ratio) of M_{n1} and M_{p2} is designed. In order to help latching the state stored on node V_2, a smaller size of M_{n2} and M_{p1} is designed. Table 4.1 gives the parameter of the proposed on-chip self-reset transient detection circuit.

Table 4.1
Device dimensions used in the proposed on-chip self-reset transient detection circuit

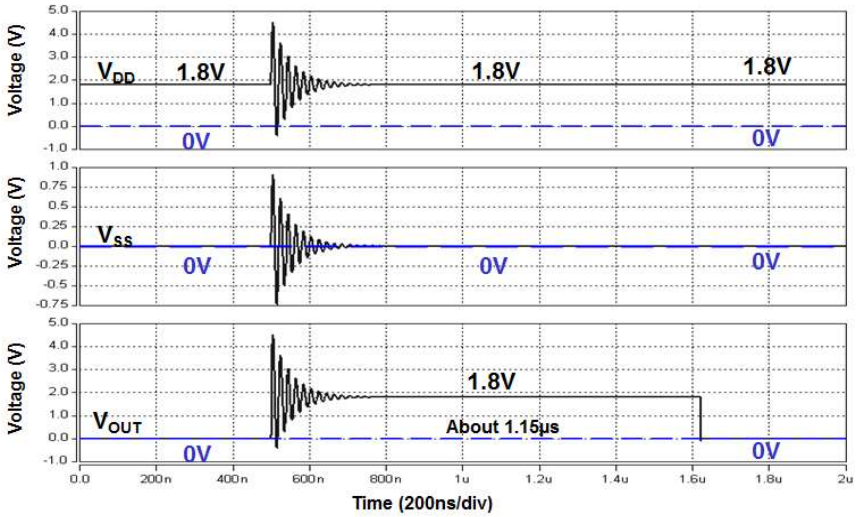
Device	Parameter
M_{p1}	1/0.18μm
M_{n1}	6/0.18μm
M_{p2}	6/0.18μm
M_{n2}	1/0.18μm

4.2.2 HSPICE Simulation Results under System-Level ESD Zapping

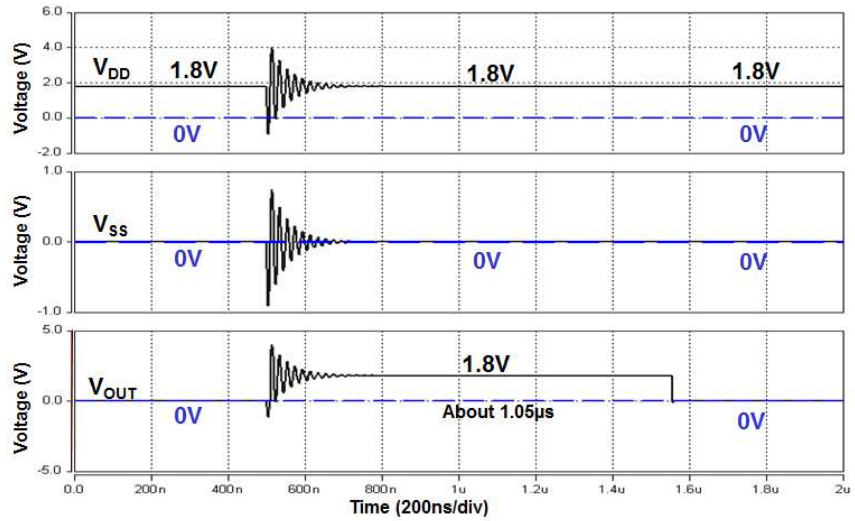
The simulated V_{DD}, V_{SS} and V_{OUT} waveforms of the on-chip self-reset transient detection circuit are shown in Fig. 4.3 (a). The positive-going underdamped sinusoidal voltage on V_{DD} and V_{SS} of this circuit are used to simulate the positive system-level ESD zapping condition. From the waveforms, the voltage of V_{DD} and V_{SS} is 1.8V and 0V in beginning. Meanwhile, the output of the proposed transient detection circuit (V_{OUT}) is kept at 0V. With an amplitude +3V of the voltage source on V_{DD} and amplitude +1V of the voltage source on V_{SS} to simulate the occurrence of system-level ESD events, V_{OUT} responses like a positive-going underdamped sinusoidal voltage simultaneously. When the disturbance ends, the voltage level of V_{DD} and V_{SS} return to its initial value, and the voltage level of V_{OUT} is changed from 0V to 1.8V. After a latch time constant (about 1.15 μs), V_{OUT} is reset to 0V again. Therefore, the occurrence of simulated positive-going underdamped sinusoidal transient disturbance is detected and stored. In addition, the detection result can be cleared by the proposed on-chip self-reset transient detection circuit itself.

The simulated V_{DD}, V_{SS} and V_{OUT} waveforms of the on-chip self-reset transient detection circuit with a negative-going underdamped sinusoidal voltage on V_{DD} and V_{SS} line are shown in Fig. 4.3 (b). With an amplitude -3V of the voltage source on V_{DD} and amplitude -1V of the voltage source on V_{SS} to simulate the negative system-level ESD

events, V_{OUT} acts like a negative-going underdamped sinusoidal voltage simultaneously. When the disturbance ends, the voltage level of V_{DD} and V_{SS} return to its initial value, and the voltage level of V_{OUT} is changed from 0V to 1.8V. After a latch time constant (about 1.05 μs), V_{OUT} is reset to 0V itself. Therefore, the occurrence of simulated negative-going underdamped sinusoidal transient disturbance is detected and stored. In additional, the state stored can be cleared automatically by the proposed on-chip self-reset transient detection circuit.



(a)



(b)

Fig. 4. 3 Simulated V_{DD}, V_{SS}, and V_{OUT} waveforms of the proposed on-chip self-reset transient detection circuit under: (a) positive and (b) negative system-level ESD test simulation.

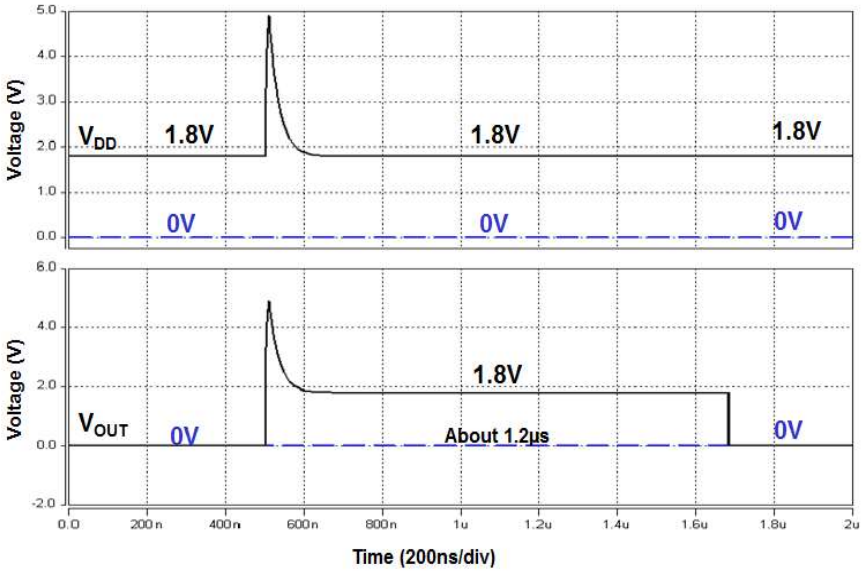
4.2.3 HSPICE Simulation Results under EFT Zapping

To simulate the EFT-induced electrical transient under EFT zapping test, an exponential pulse is used in HSPICE simulation. The polarity of pulse is positive or negative to simulate the positive or negative EFT test.

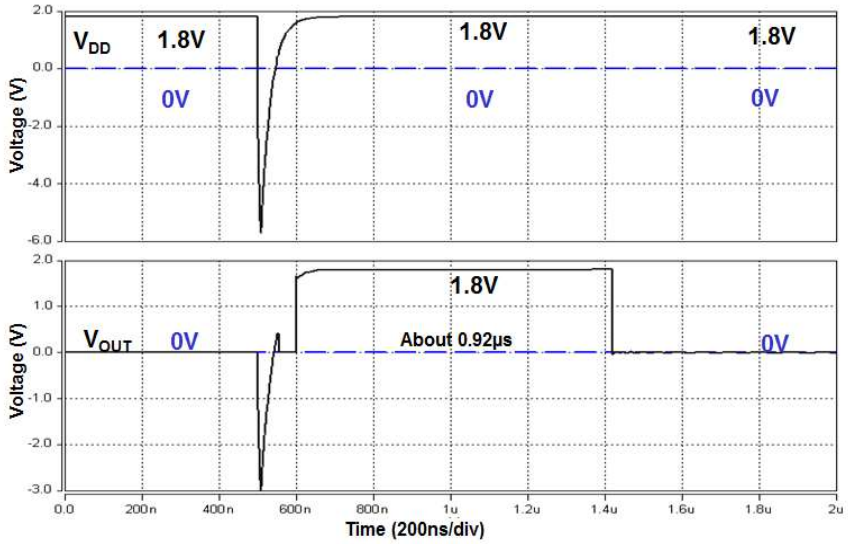
Fig. 4.4 (a) shows the simulated V_{DD} and V_{OUT} waveforms of the proposed on-chip self-reset transient detection circuit with a positive exponential pulse disturbance on V_{DD} line. When an exponential pulse with +5V amplitude coupled to V_{DD} line, V_{OUT} responses as a positive-going exponential pulse simultaneously and keep to 1.8V finally from initial voltage level of 0V. After a time constant (about 1.2 μs), the voltage level of V_{OUT} reset to 0V automatically.

Fig. 4.4 (b) shows the simulated V_{DD} and V_{OUT} waveforms of the proposed on-chip self-reset transient detection circuit with a negative exponential pulse disturbance on V_{DD} line. When an exponential pulse with -6V amplitude coupled to V_{DD} line, V_{OUT} responses as a negative-going exponential pulse simultaneously and keep to 1.8V finally from initial voltage level of 0V. After a latch time constant (about 0.92 μs), the voltage level of V_{OUT} reset to 0V automatically.

From the simulated waveforms, the detection and the self-reset function is investigated by HSPICE. As a result, the output voltage level of self-reset transient detection circuit can successfully transit from 0V to 1.8V to response the occurrence of simulated positive or negative EFT event and reset to 0V itself after a latch time constant that depended to the parameter of circuit device. Therefore, the electrical transient disturbance due to EFT events can be detected and stored.



(a)



(b)

Fig. 4. 4 Simulated V_{DD} and V_{OUT} waveforms of the proposed on-chip self-reset transient detection circuit under: (a) positive and (b) negative EFT test simulation.

4.2.4 Consideration with Latch time

During the fast electrical transient duration, the PMOS device M_{p2} is turned on to pull high the voltage level at node V_2 of the proposed self-reset transient detection circuit as aforementioned description of circuit operation and simulation results shown to get the output (V_{OUT}) voltage changing from 0V to 1.8V. When the electrical transient

ends, due to the bias voltage of node V_X and V_{XB} setting back to 0V and 1.8V respectively, M_{n1} will be turned off and M_{n2} will be turned on. Thus, the voltage level of node V_2 will be biased to

$$V_2 = V_{DD} \times \frac{R_{ON_{n_2}}}{R_{ON_{p_2}} + R_{ON_{n_2}}} \tag{4}$$

R_{ON} is the turn on resistance of MOSFET device. With the proper designed size (W/L) ratio of M_{p2} and M_{n2}, the voltage level of node V_2 will bias M_{p1} to a known region. Thus, the drain current of M_{p1} (I_{dp1}) will charge high the voltage level of node V_1. Meanwhile, the voltage level of node V_2 will be pulled low continuously by device M_{n2}. Finally, node V_1 will be charged to logic "1" and node V_2 will be discharged to logic "0". The latch time, which means the time of node V_2 kept at logic "1", is related to the parameter I_{dp1} and pull-down ability of M_{n2} as analyzed. Therefore, in order to increase the latch time, M_{p1} should be biased to a subthreshold region. The drain current in subthreshold region has the relationship as:

$$I_{d_{p_1}} \propto \frac{W_{p_1}}{L_{p_1}}, \quad I_{d_{p_1}} \propto exp\left(\frac{V_{gs_{p_1}}}{n * V_T}\right), \quad where \quad V_{gs_{p_1}} = V_2 - V_{DD} \tag{5}$$

Thus, the latch time should be controlled by the size ratio (W/L) of M_{n2} and M_{p1}.

To investigate the latch time, the transistor size of the proposed self-reset transient detection circuit has been scaled up as Table 4.2 listed.

Table 4.2

Device dimensions of proposed on-chip self-reset transient detection circuit used for latch time simulation

Device	Parameter
M_{n1}	30/0.18μm
M_{p1}	3/0.18μm
M_{n2}	5/0.18μm
M_{p2}	30/0.18μm

Fig. 4.5 shows the simulated waveforms with different size of M_{n2}. The turn on resistance is inversely proportional to the width of M_{n2}. Therefore, when the fast electrical transient end, the voltage level of node V_2 is also decreased with the width of M_{n2} increased, which means the discharge time of voltage level of node V_2 return to 0V is decreased too. As a result, due to the different voltage level of node V_2 biased by different size of M_{n2}, different latch time of V_{OUT} kept to 1.8V is designed.

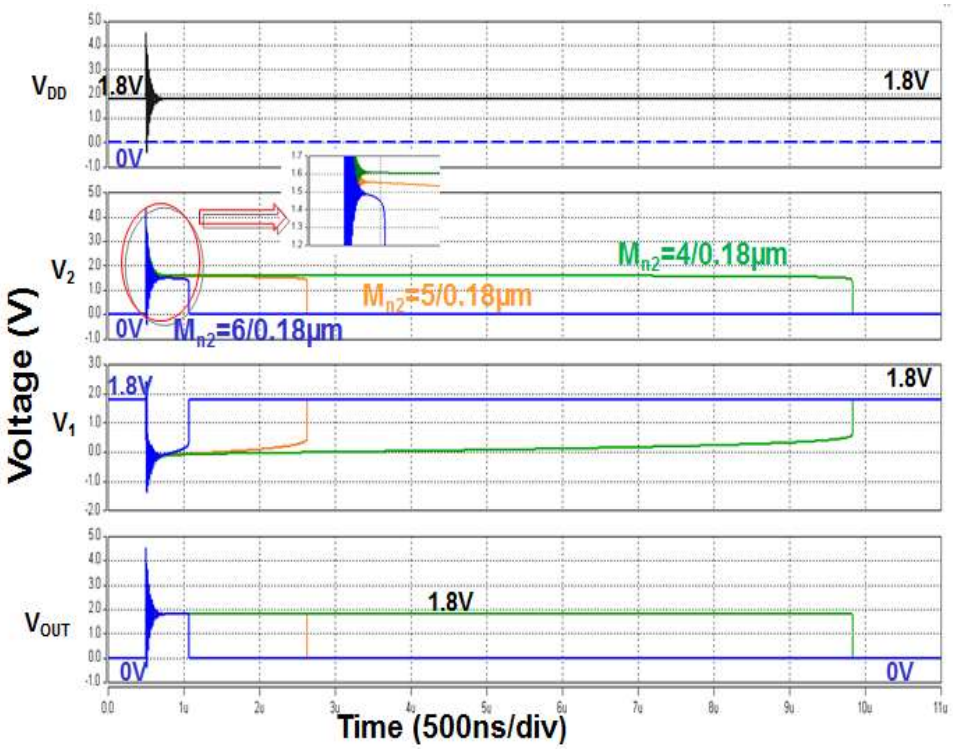


Fig. 4. 5 Simulated V_{DD}, V_1, V_2 and V_{OUT} waveforms of the proposed on-chip self-reset transient detection circuit with different size of M_{n2}.

Fig. 4.6 shows the simulated waveforms with different size of M_{p1}. At the moment of fast electrical transient ending, the voltage level of node V_2 is biased to same value, the charge current of node V_1 is proportional to the width of M_{p1}. Therefore, the charge time of voltage level of node V_1 return to 1.8V is different too. As a result, due to the different size of M_{p1}, different latch time of V_{OUT} kept to 1.8V is designed.

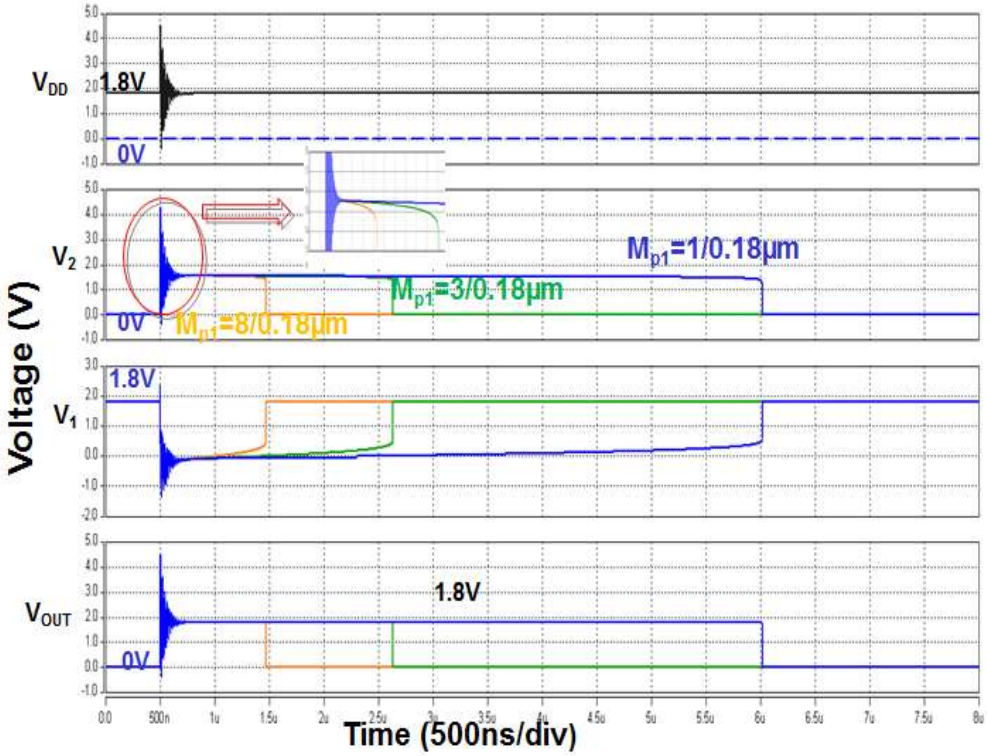
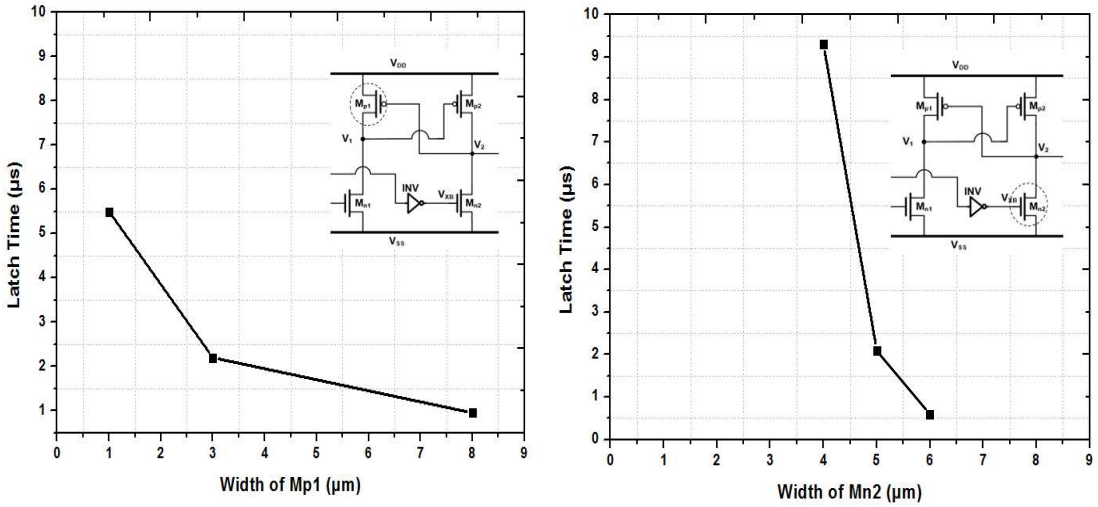


Fig. 4. 6 Simulated V_{DD}, V_1, V_2 and V_{OUT} waveforms of the proposed on-chip self-reset transient detection circuit with different size of M_{p1}.

The aforementioned waveforms (Fig. 4.5 and Fig. 4.6) prove that the latch time can be controlled by adjusting the charge current of node V_1 when the electrical transient disturance ends. A larger charge current of node V1 will cause a smaller latch time. In addition, the charge current is related to the width of M_{p1} and the width of M_{n2}. The relationship between latch time and size ratio of M_{p1} is given in Fig. 4.7 (a). Compare to the relationship between latch time and size ratio of M_{n2} shown in Fig. 4.7 (b), the curve of Fig. 4.7 (a) is more linear. Therefore, to adjust the size ratio of M_{p1} can perform a better latch time control.



(a) (b)

Fig. 4. 7 Latch time of the on-chip self-reset transient detection circuit with (a) different size of $M_{p1,}$ and (b) different size of M_{n2}.

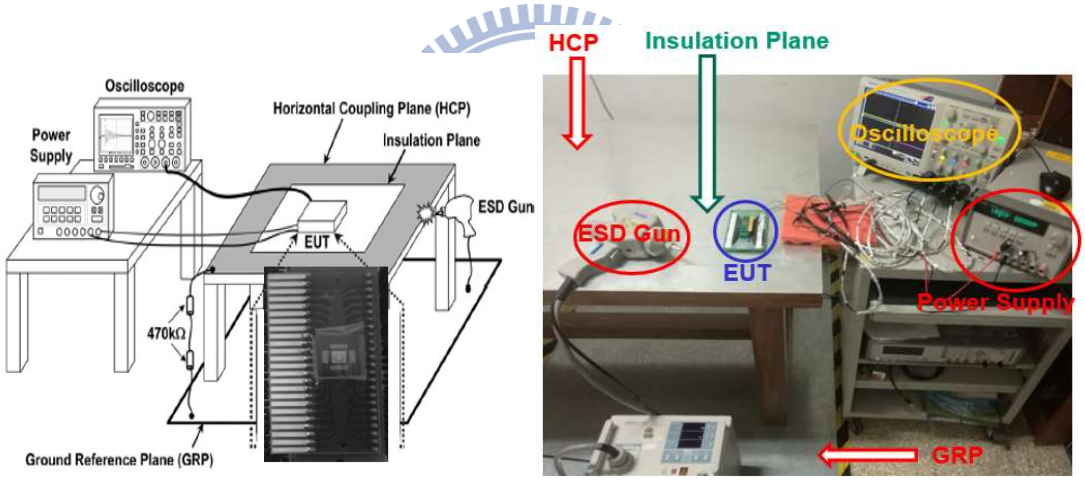
4.3 Measurement Results

The new proposed on-chip self-reset transient detection circuit has been designed and fabricated in a 0.18um CMOS process with 1.8-V devices. Fig. 4.8 is the photo of fabricated chip. The silicon area of this on-chip self-reset transient detection circuit without PAD is 106μm* 96μm. To evaluate the performance of new proposed on-chip self-reset transient detection circuit, system-level ESD gun and the EFT generator are used in system-level ESD test and EFT test.

Fig. 4. 8 Die photo of the proposed on-chip self-reset transient detection circuit.

4.3.1 System-Level ESD Test

Fig. 4.9 (a) and (b) shows the block diagram and setup of an indirect contact-discharge system-level ESD test mode, respectively. The EUT is placed on a wooden table which standing on the ground reference plane (GRP). Insulation plane is used to insulate the EUT and the horizontal coupling plane (HCP) placed on the table. ESD gun is used as the system-level ESD generator. In additional, the discharge return cable of the ESD gun should be connected to the GRP directly and the HCP shall be connected to the GRP with two 470kohm resistors in series. Under the indirect contact-discharge test mode, the head of ESD gun zaps the edge of HCP. The ESD-coupled electrical transients will disturb the power lines of CMOS IC inside the EUT.



(a) (b)

Fig. 4. 9 Measurement setup for a system-level ESD test with indirect contact-discharge test mode: (a) Block diagram, and (b) Test setup.

Fig. 4.10 shows the mearsured V_{DD}, V_{SS} and V_{OUT} waveforms of the new propoesd on-chip self-reset transient detection circuit under the +0.2 kV system-level ESD test voltgae. The ESD stress under system-level ESD test disturb the normal voltgae level of the power (V_{DD}) and ground (V_{SS}) lines of the self-reset transient detection circuit. The voltage level of V_{DD} (V_{SS}) rapidly increases from 1.8V (0V), and the voltage level of V_{OUT} also increase as an positive-going underdamped sinuosoidal waveform

simultaneously. Finally, the output voltgae of the new propesd transient detection circuit (V_{OUT}) transist from 0V to 1.8V and keep at 1.8V with a latch time 2.9 μs. Therefore, the detection and self-reset function of propoesd self-reset transient detection circuit is succesfully verified by the positive system-level ESD test.

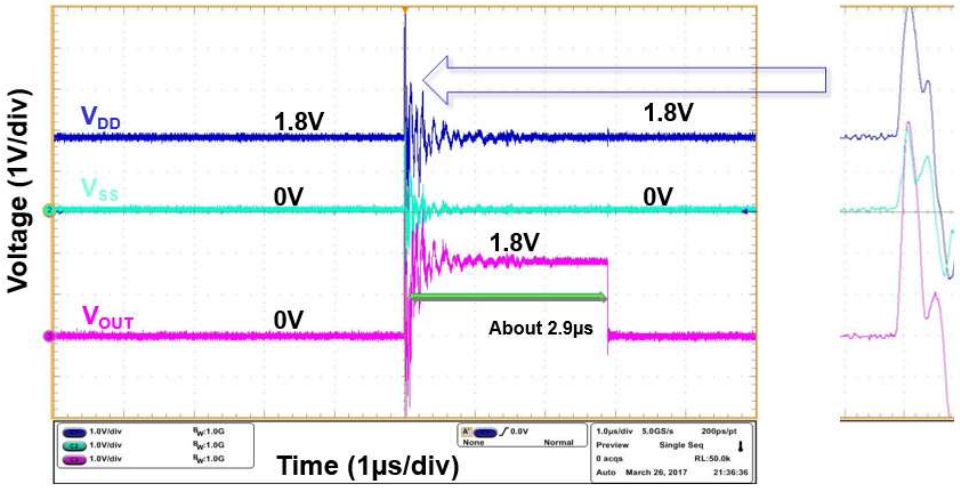


Fig. 4. 10 Measured V_{DD}, V_{SS} and V_{OUT} waveforms of the propoesd self-reset transient detection circuit under system-level ESD test with zapping voltage of +0.2 kV.

Fig. 4.11 shows the mearsured V_{DD}, V_{SS} and V_{OUT} waveforms of the new propoesd on-chip self-reset transient detection circuit under the -0.2 kV system-level ESD test voltgae. The system-level ESD-induced electrical transients disturb the normal voltgae level of the power (V_{DD}) and ground (V_{SS}) lines of the self-reset transient detection circuit. The voltage level of V_{DD} (V_{SS}) rapidly decrease from 1.8V (0V), and the voltage level of V_{OUT} also acts as a negative-going underdamped sinuosoidal waveform simultaneously. Finally, the output voltgae of the new propesd transient detection circuit (V_{OUT}) transist from 0V to 1.8V and keep at 1.8V with a latch time 2.9 μs. Therefore, the detection and self-reset function of propoesd self-reset transient detection circuit is succesfully verified by the negative system-level ESD test.

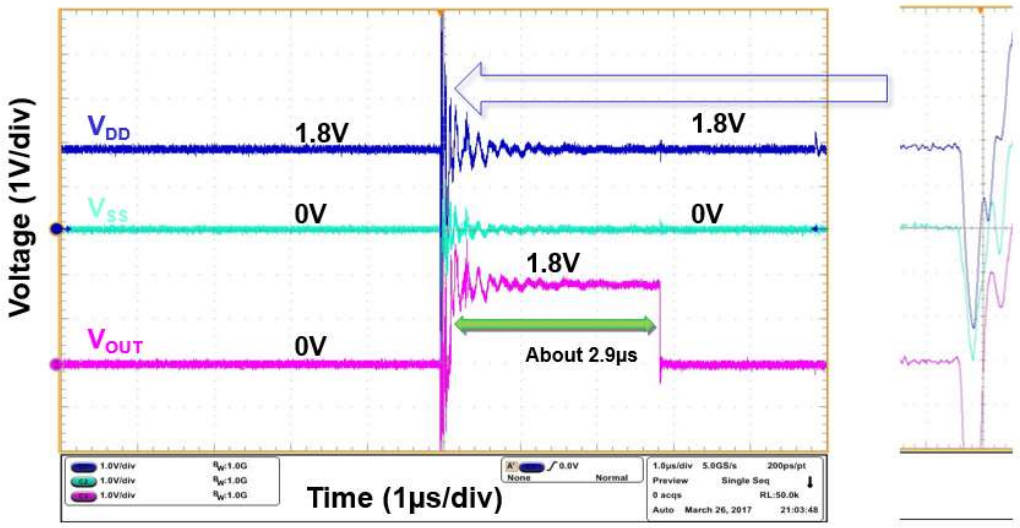
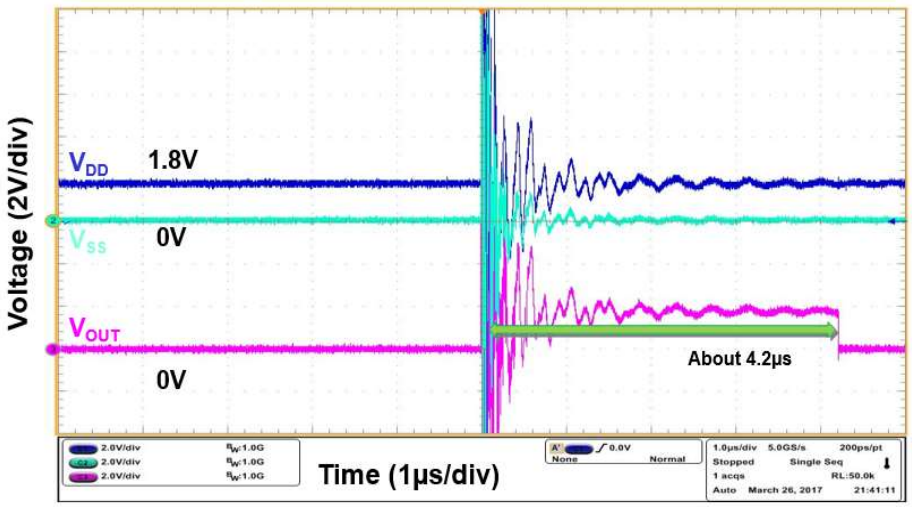
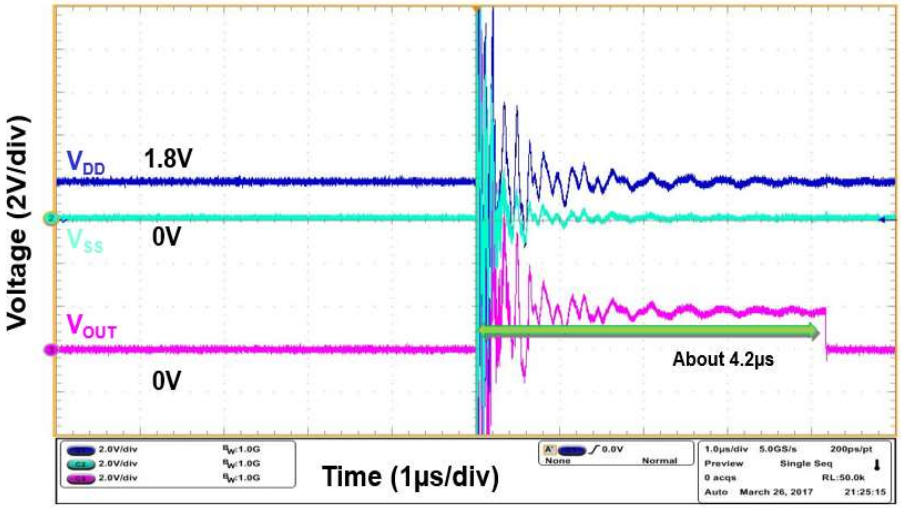


Fig. 4. 11 Measured V_{DD}, V_{SS} and V_{OUT} waveforms of the propoesd self-reset transient detection circuit under system-level ESD test with zapping voltage of -0.2 kV.

To verify the perfomance of the propoesd self-reset transient detection circuit under test level specified by IEC 61000-4-2, the measured V_{DD}, V_{SS} and V_{OUT} transient response under +2 kV and -2 kV system-level ESD zapping voltage are shown in Fig. 4.12 (a) and (b), respectively. From the waveforms, the transisent detection circuit can detect the positive or negetive-going electrical transient disturbance on the V_{DD} and V_{SS} lines and reset the output (V_{OUT}) voltage automatically after a time constant. Therefore, the function of the proposed self-reset transient dection circuit under +2 kV and –2 kV system-level ESD zapping voltage teset has been verified. Furthermore, the eletctrical transients duration as the wavefroms shown is much longer. Due to the difference of electrical transients duration under ±2 kV system-level ESD test and ±0.2 kV system-level ESD test, the latch time of the proposed self-reset transient detection circuit is increased.



(a)



(b)

Fig. 4. 12 Measured V_{DD}, V_{SS} and V_{OUT} waveforms of the propoesd self-reset transient detection circuit under system-level ESD test with zapping voltage of (a) +2 kV, and (b) -2 kV.

Fig. 4.13 shows the latch time control waveforms under +300 V system-level ESD zapping voltage. The width of M_{p1} is designed as 1 μm, 3 μm and 8 μm. Other devices of self-reset transient detection circuit are as Table 4.2 listed. From the waveforms, the latch time is inversely proportional to the width of M_{p1}. The time of V_{OUT} voltage reset to 0V is 17.5 μs, 6 μs, and 2.5 μs with the size ratio of M_{p1} designed to 1/0.18 μm, 3/0.18 μm and 8/0.18 μm, respectively.

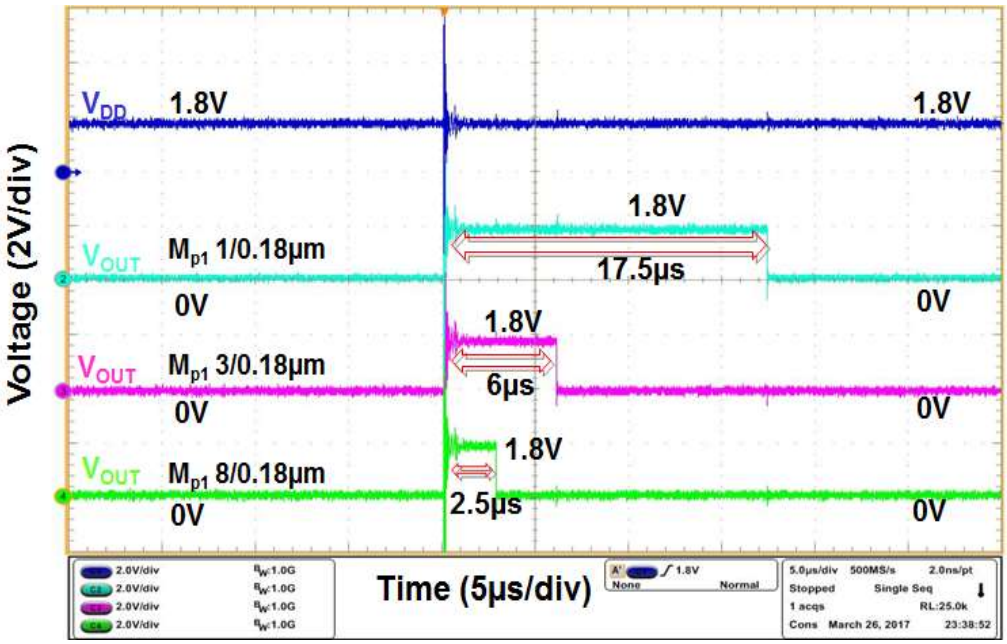
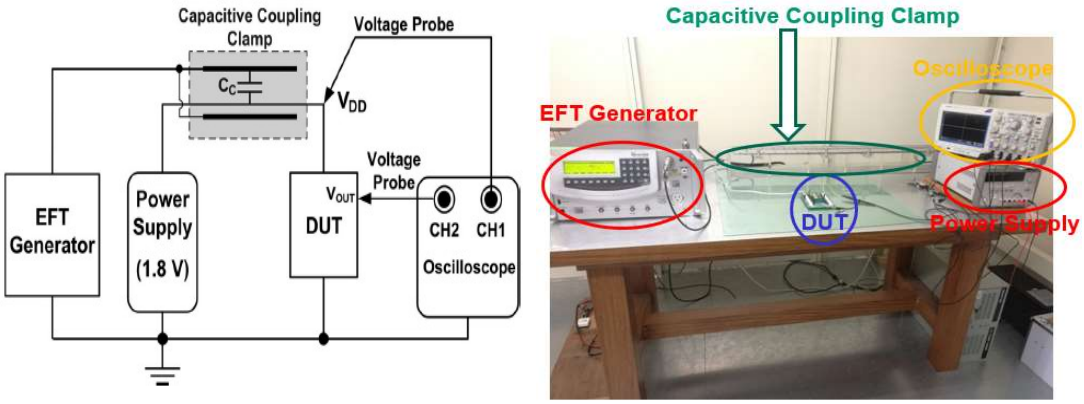


Fig. 4. 13 Measured latch time control waveforms of the self-reset transient detection circuit under system-level ESD test with zapping voltage of +300V.

4.3.2 EFT Test

Fig. 4.14 shows the measurement diagram (a) and setup (b) for EFT test combined with capacitive coupling clamp, respectively. The output of EFT generator connect to the end of capacitive coupling clamp directly. The power cables from the power supply equipment are placed inside the capacitive coupling clamp, and the capacitive coupling clamp itself should be closed as much as possible to provide maximum coupling capacitance between the clamp and the cable. The typical capacitance between the cable and clamp is from 50 pF to 200 pF. Thus, the EFT testing voltage will be coupled to the power cable via the capacitor of capacitive coupling clamp. The digital oscilloscope can monitored the voltage response of V_{DD}, V_{SS} and V_{OUT} of proposed self-reset transient detection circuit during the EFT tests. With this setup, the circuit performance of proposed on-chip transient detection circuit under EFT tests can be evaluated.



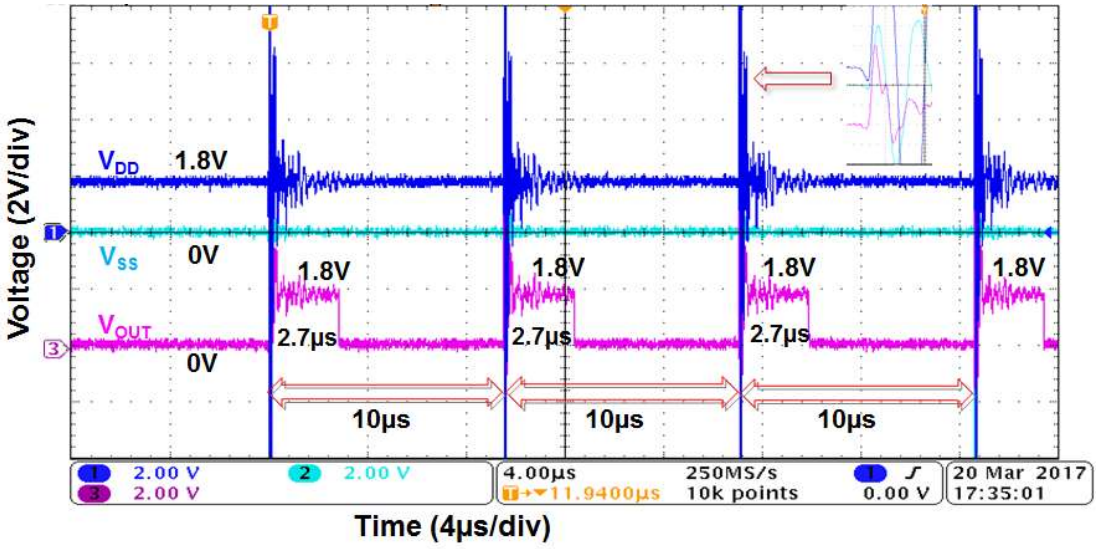
(a) (b)

Fig. 4. 14 Measurement setup for an EFT test combined with capacitive coupling clamp: (a) Block diagram, and (b) Test setup.

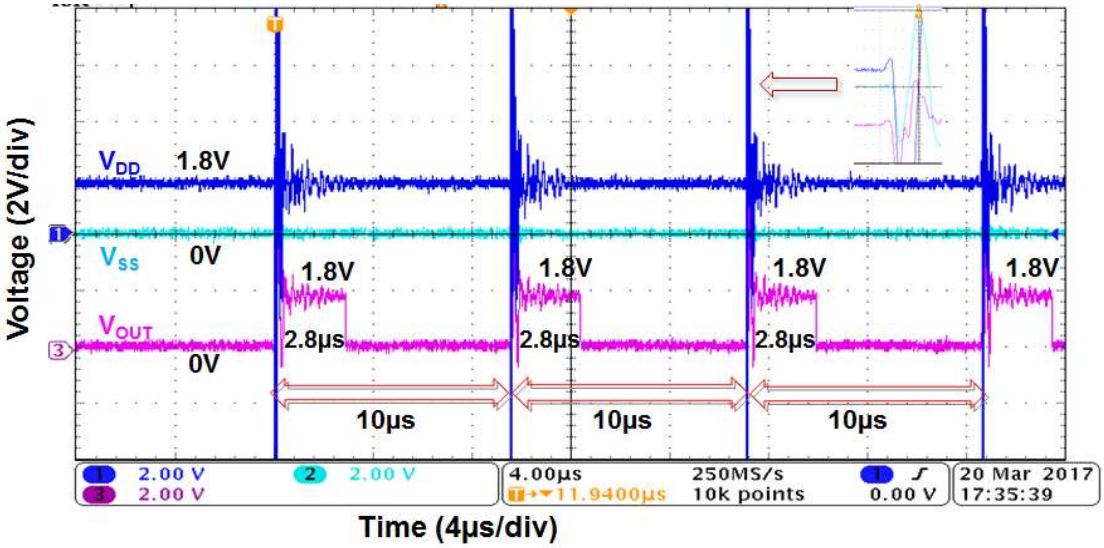
Fig. 4.15 (a) shows the V_{DD}, V_{SS} and V_{OUT} waveforms under the EFT test voltage of +200V with a repetition rate 100 kHz. The period of the pulses is 10 μs. From the waveform, V_{DD} and V_{SS} acts like a positive-going underdamped sinusoidal voltage waveform when the EFT pulse coupled on. Meanwhile, V_{OUT} is influenced simultaneously with these electrical transients. After an EFT pulse ends, the voltage level of V_{OUT} transits from 0V to 1.8V, and keep at 1.8V. With a 2.7μs latch time, the voltage level of V_{OUT} is return to 0V for next EFT pulse detection.

Fig. 4.15 (b) shows the V_{DD}, V_{SS} and V_{OUT} waveform under the EFT test voltage of -200V with a repetition rate 100 kHz. The period of the pulses is 10 μs. From the waveform, V_{DD} and V_{SS} acts like a negative-going underdamped sinusoidal voltage waveform when the EFT pulse coupled on. Meanwhile, V_{OUT} is influenced simultaneously with these transients. After an EFT pulse ends, the voltage level of V_{OUT} transits from 0V to 1.8V, and keep at 1.8V. With a 2.8μs latch time, the voltage level of V_{OUT} is return to 0V for next EFT pulse detection.

From the waveforms shown in Fig. 4.15, the electrical transient disturbance is a little different between +0.2 kV EFT zapping voltage and -0.2 kV EFT zapping voltage. Consider to that, the different latch time as shown in these waveforms can be explained.



(a)



(b)

Fig. 4. 15 Measured V_{DD}, V_{SS} and V_{OUT} waveforms of the propoesd self-reset transient detection circuit under EFT tests with zapping voltage of: (a) +200 V, and (b) -200V by combing with capacitive coupling clamp.

Fig. 4.16 shows the latch time control waveforms under +300 V EFT zapping voltage with a single pulse. The width of M_{p1} is designed as 1 μm, 3 μm and 8 μm. Other devices of self-reset transient detection circuit are as Table 4.2 listed. From the waveforms, the latch time is inversely proportional to the width of M_{p1}. The time of

V_{OUT} voltage reset to 0V is 17.5 μs, 6.5 μs, and 3 μs with the size ratio of M_{p1} designed to 1/0.18 μm, 3/0.18 μm and 8/0.18 μm, respectively.

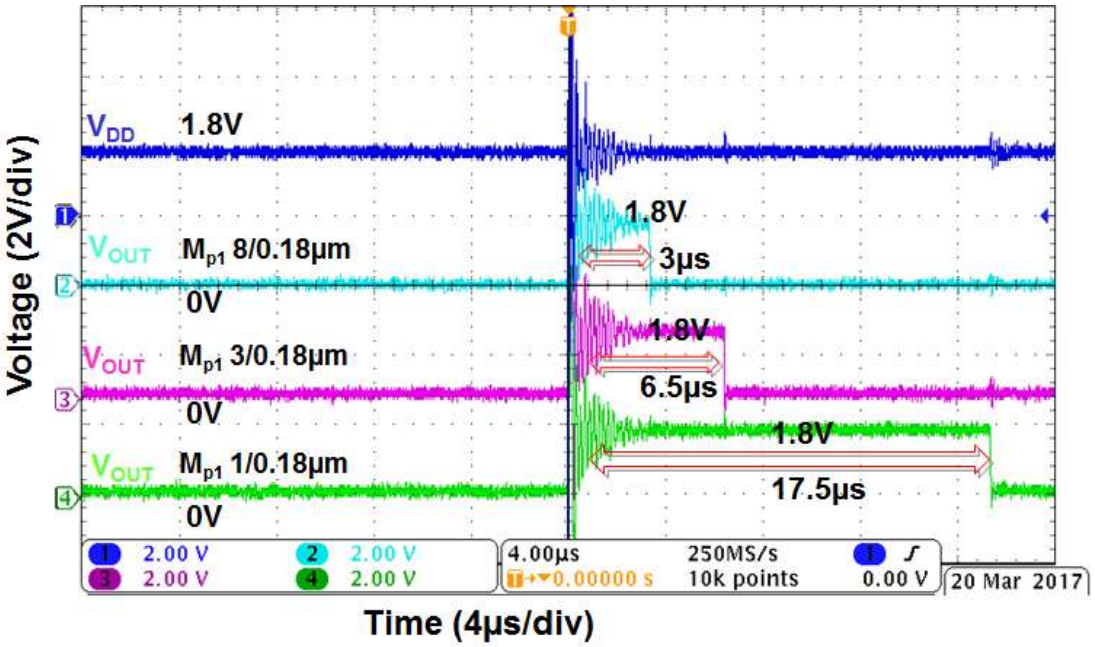


Fig. 4. 16 Measured latch time control waveforms of the self-reset transient detection circuit under EFT test with zapping voltage of +300V.

Compare to the latch time under system-level ESD, EFT tests and the HSPICE simulation, as shown in the aforementioned waveforms, the system-level ESD measurement results is nearly same as the EFT results. However, these latch time constant are much larger than that under HSPICE simulations. Fig. 4.17 shows the curve of relations between the width of M_{p1} and the latch time under the system-level ESD test， EFT test and HSPICE simulation conditions. The root cause of the latch time difference is the ideal voltage sources using in HSPICE to simulate the electrical transient disturbances due to system-level ESD or EFT test. The real electrical transients coupled on power lines of CMOS IC under ESD tests are much complex.

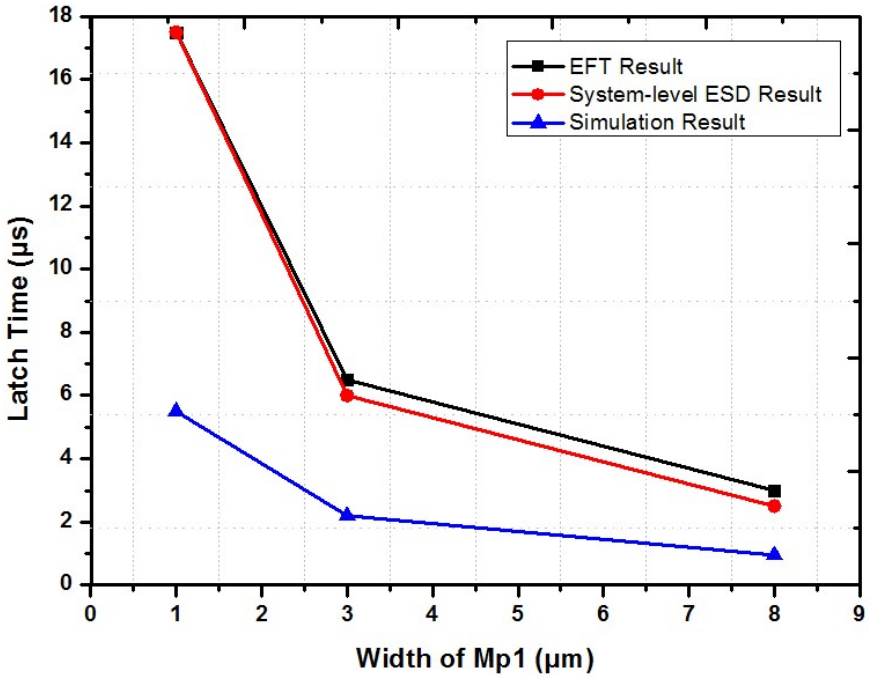


Fig. 4. 17 Relations between the width of M_{p1} and the latch time under simulation under HSPICE simulation, system-level ESD and EFT tests.

4.4 System Application

To solve the system malfunction issues of microelectronic products under system-level or EFT test, a hardware/firmware co-design has been proposed in previous researches. However, traditional hardware/firmware co-designed with the on-chip transient detection circuit and power-on reset circuit will be risky due to the mistriggering situations. The proposed on-chip self-reset transient detection circuit is designed to perform a more effective hardware/firmware co-design.

Fig. 4.18 shows the new firmware recover flowchart combined with the on-chip self-reset transient detection circuit. In beginning, the output (V_{OUT}) state of proposed on-chip self-reset transient detection circuit is initially set to logic “0” when power on. The index of system is set to logic “0” by the V_{OUT} state. The power-on reset (POR)

circuit reset the system operation after power-on transition. When electrical transients happen, the self-reset transient detection circuit can detect the occurrence of transient disturbance and transit the V_{OUT} state from logic “0” to logic “1”. The index stored in firmware is also changed to logic “1” by V_{OUT} state and then initiate the firmware recover procedure to restore the system to a known stable state. After the system recover procedure, the proper designed self-reset transient detection circuit will reset V_{OUT} state to logic “0” itself and the firmware index is also reset to logic “0” again by the output state of V_{OUT}. Therefore, the next electrical transient event can be detected.

From the flowchart, the index of firmware is set by the output state of self-reset transient detection circuit only. Compare to the system recovery flowchart shown in Fig. 3.21, there are no reset data path to the detection circuit and additional logic gate in the new system flowchart. Whether the reset data path be disturbed and POR circuit be mistriggered or not, the system recovery procedure can be still initiated to restore the system from the abnormal condition. Therefore, due to the optimized data path, the solution of firmware co-designed with the on-chip self-reset transient detection circuit provides a more efficient protection for the microelectronic products against the electrical transitions from system-level ESD and EFT events.

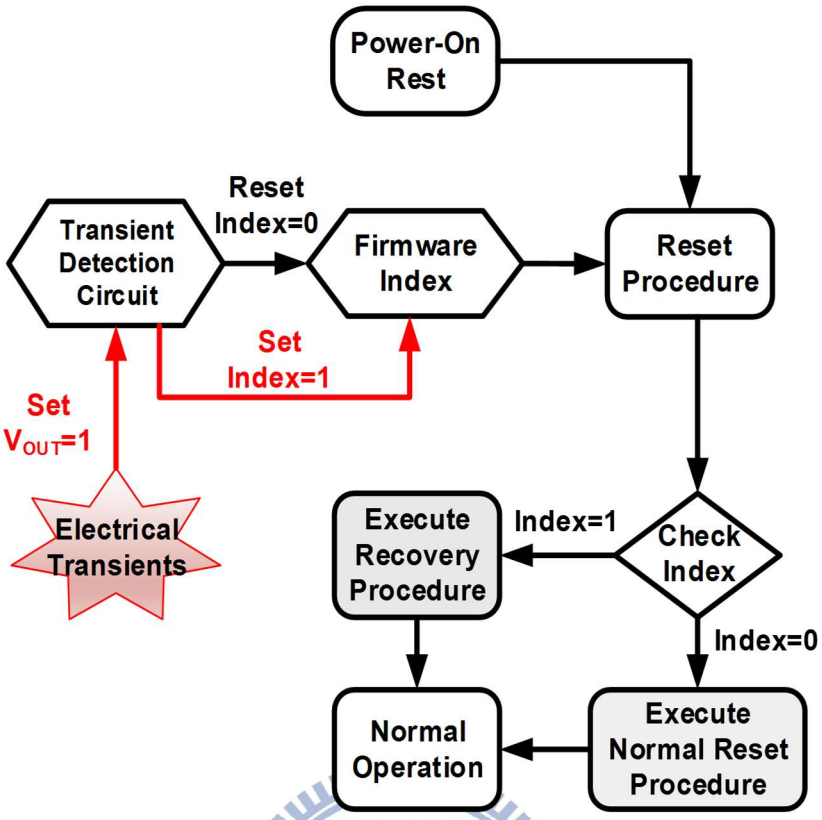


Fig. 4. 18 Firmware flowchart to recover system when electrical transients happen.

4.5 Summary

A novel on-chip self-reset transient detection circuit has been proposed. This circuit is designed to detect the system-level ESD-induced or EFT-induced electrical transient disturbance, and to be reset automatically without reset signal. The performance of the proposed self-reset transient detection circuit has been investigated by HSPICE simulation, and verified by the measurement results under system-level ESD tests and EFT tests. Compare to the previous designs and newly proposed transient detection circuit (Chapter 3.), the new on-chip self-reset transient detection circuit realize the reset function without reset devices. The output state of this circuit can be rested itself after a well-designed latch time constant. In addition, the detection sensitivities of this design against system-level ESD test and EFT test are +/- 200V, respectively.

With hardware/firmware co-design, the output state of the new proposed on-chip self-reset transient detection circuit can set the recovery and reset index of firmware to execute the system recovery procedure and firmware reset. In addition, the latch time of the output state can be adjusted to meet different requirement of system recovery procedure. Compare to the previous work shown in Fig. 3.21, the new system recovery flow chart do not need an additional reset data path, as Fig. 4.18 shows. Therefore, a more efficient solution against the protection of microelectronic products under system-level ESD and EFT test is achieved by the hardware/firmware co-designed with the proposed on-chip self-reset transient detection circuit.

Chapter 5
Conclusions and Future Works

5.1 Conclusions

This thesis proposes two novel on-chip transient detection circuits. These transient detection circuits are designed to detect the fast electrical transient disturbance coupled on the power lines of CMOS ICs in a 0.18-μm CMOS process with 1.8-V devices. In chapter 3, a new on-chip transient detection circuit with simple circuit structure has been proposed. The resistor and parasitic capacitor compose the detection unit of this circuit. The occurrence of the electrical transients can be detected and stored by the proposed circuit. A reset signal connected to the reset device in this circuit helps reset the stored output state. In chapter 4, on-chip self-reset transient detection circuit has been proposed. This circuit operates without reset signal. The occurrence of the electrical transients can be detected and memorized by the proposed circuit. In addition, the stored output state of the self-reset transient detection circuit can be released automatically. The performance of the proposed circuits has been investigated by HSPICE simulation and verified under system-level ESD and EFT tests.

Two types of system recovery flowcharts have been proposed in this thesis. The detection results of the proposed transient detection circuits can be used as system recover index to provide a hardware/firmware solution against the system-level and EFT events. The microelectronic products can achieve the criterion of “Class B” level in the system-level ESD and EFT standards. Furthermore, compared to the aforementioned flowcharts, the on-chip self-reset transient detection circuit co-

designed with firmware provides a more efficient solution for the protection of system-level ESD and EFT tests due to the optimized data path.

5.2 Future Works

In order to suppress power supply noise, a large bypass/decoupling capacitor is placed between supply rails of CMOS ICs. The voltage level of system-level ESD-induced and EFT-induced transients will be degraded by these bypass/decoupling capacitors too. Thus, the detection sensitivity of on-chip transient detection circuit will be influenced. The relationship between bypass/decoupling capacitor and the detection range of transient detection circuit should be investigated in future.

It has been proven that the noise filter networks can affect the parameters of the underdamped sinusoidal voltage, such as damping frequency and transient peak voltage [24]. A proper designed noise filter network can strongly enhance the immunity of CMOS ICs to the ESD-induced electrical transient disturbance. The noise filter network can be realized as different types, such as capacitor filter and RC filter. Therefore, the transient detection circuit combined with on-chip filter networks has been proposed in previous research [26], [28]. Fig. 5.1 shows a 4-bit transient-to-digital converter composed of four transient detection circuits and RC filter networks. Fig. 5.2 shows another 4-bit transient-to-digital converter. The proposed converters are designed to detect different ESD voltage levels and transfer output voltages into 4-bit digital codes under system-level ESD tests. Considering energy saving and system recovery time, the 4-bit digital codes can be used as the firmware index to execute different recovery procedures of the microelectronic products which equipped CMOS ICs.

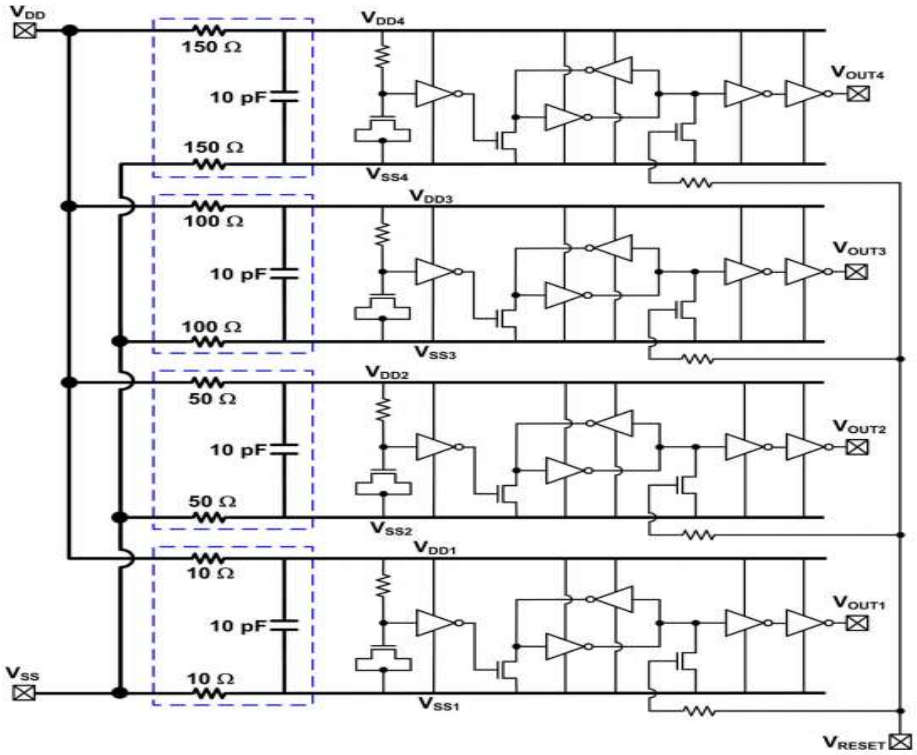


Fig. 5.1 4-bit transient-to-digital converter (1).

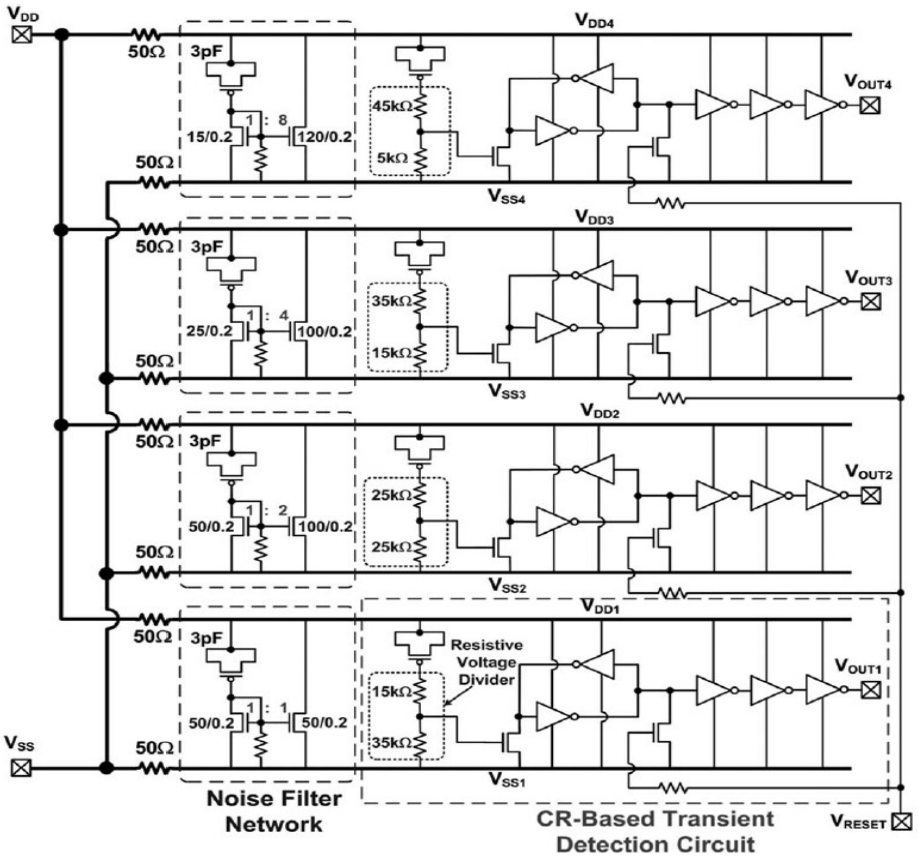


Fig. 5.2 4-bit transient-to-digital converter (2).

For further applications, the on-chip transient-to-digital converters composed of self-reset transient detection circuits and noise filter networks should be designed. Besides, the impedance of the EUT influences the detection range of system-level ESD voltage. In future, an on-chip self-reset transient-to-digital converter designed to detect ESD-induced current variations of power and ground lines under system-level ESD zapping condition should be investigated.

References

[1] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp.173–183, Jan. 1999.

[2] S. Voldman, ESD: *Circuits and Devices*, John Wiley & Sons, 2006.

[3] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, 2nd Edition, John Wiley & Sons, Ltd., England, 2002.

[4] *EOS/ESD Standard for ESD Sensitivity Testing – Human Body Model – Component Level*, STM 5.1, EOS/ESD Association, NY., 2011.

[5] *EOS/ESD Standard for ESD Sensitivity Testing – Machine Model – Component Level*, STM 5.2, EOS/ESD Association, NY., 2009.

[6] *EOS/ESD Standard for ESD Sensitivity Testing – Charge Device Model – Component Level*, STM 5.3.1, EOS/ESD Association, NY., 2009.

[7] IEC 61000-4-2 Standard, *"EMC – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test,"* IEC, 2008.

[8] IEC 61000-4-4 Standard, *"EMC – Part 4-4: Testing and Measurement Techniques –Electrical Fast Transient/Burst Immunity Test,"* IEC, 2004.

[9] M.-D. Ker and Y.-Y. Sung, "Hardware/firmware co-design in an 8-bits microcontroller to solve the system-level ESD issue on keyboard," in *Proc. EOS/ESD Symp.*, 1999, pp.352–360.

[10] T.-H. Wang, W.-H. Ho, and L.-C. Chen, "On-chip system ESD protection design for STN LCD drivers," in *Proc. EOS/ESD Symp.*, 2005, pp. 316–322.

[11] A. Ristow, M. Begovic, A. Pregelj, and A. Rohatgi, "Development of a methodology for improving photovoltaic inverter reliability," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2581-2592, Jul. 2008.

[12] W. Stadler, S. Bargstadt-Franke, T. Brodbeck, R. Gaertner, M. Goroll, H. Goβner, N. Jensen, and C. Muller, "From the ESD robustness of products to the system-level ESD robustness," in *Proc. EOS/ESD Symp.*, 2004, pp. 67–74.

[13] M.-D. Ker and S.-F. Hsu, "Physical mechanism and device simulation on transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1821-1831, Aug. 2005.

[14] White Paper 3—*System Level ESD, Part I*, Industry Council on ESD Target Levels, 2011.

[15] M.-D. Ker and S.-F. Hsu, "Component-level measurement for transient-induced latch-up in CMOS ICs under system-level ESD considerations," *IEEE Trans. Device Mater. Reliabil.*, vol. 6, no. 3, pp. 461–472, Sep. 2006.

[16] M. Kelly, L. Henry, J. Barth, G. Weiss, M. Chaine, H. Gieser, D. Bonfert, T. Meuse, V. Gross, C. Hatchard, and I. Morgan, "Developing a transient induced latch-up standard for testing integrated circuits," in *Proc. EOS/ESD Symp.*, 1999, pp. 178-189.

[17] Y. Xiu, N. Thomson, R. Mertens, and E. Rosenbaum, "A mechanism for logic upset induced by power-on ESD," in *Proc. EOS/ESD Symp.*, 2014, pp. 1-10.

[18] M.-D. Ker and C.-C. Yen, "Investigation and design of on-chip power-rail ESD clamp circuits without suffering latchup-like failure during system-level ESD test," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2533–2545, Nov. 2008.

[19] M.-D. Ker and S.-F. Hsu, *Transient-Induced Latchup in CMOS Integrated Circuits.* New York, NY, USA: Wiley, 2009.

[20] C.-C. Yen, M.-D. Ker, and T.-Y. Chen, "Transient-induced latchup in complementary-metal-oxide-semiconductor integrated circuits under electrical fast transient test," *IEEE Trans. Device Mater. Reliab.*, vol. 9, no. 2, pp. 255–264, Jun. 2009.

[21] C.-C. Yen and M.-D. Ker, "The effect of IEC-like fast transients on RC-triggered ESD power clamps," *IEEE Trans. Electron Devices,* vol. 56, no. 6, pp. 1204–1210, Jun. 2009.

[22] H. Ott, *Noise Reduction Techniques in Electronic Systems*, 2nd ed. Hoboken, NJ: Wiley, 1988.

[23] M. Montrose, *Printed Circuit Board Design Techniques for EMC Compliance.* Piscataway, NJ: IEEE Press, 2000.

[24] M.-D. Ker and S.-F. Hsu, "Evaluation on board-level noise filter networks to suppress transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 1, pp. 161–171, Feb. 2006.

[25] M.-D. Ker, C.-C. Yen, and P.-C. Shin, "On-chip transient detection circuit for system-level ESD protection to meet electromagnetic compatibility regulation," *IEEE Trans. Electromagn. Compat.,* vol. 50, no. 1, pp. 13–21, Feb. 2008.

[26] M.-D. Ker and C.-C. Yen, "Transient-to-digital converter for system-level ESD protection in CMOS integrated circuits," *IEEE Trans. Electromagn. Compat.*, vol. 51, no. 3, pp. 620–630, Aug. 2009.

[27] M.-D. Ker and C.-C. Yen, "New transient detection circuit for on-chip protection design against system-level electrical transient disturbance," *IEEE Trans. Ind. Electron.*, vol. 57, no. 10, pp. 3533–3543, Oct. 2010.

[28] M.-D. Ker and C.-C. Yen, "New 4-bit transient-to-digital converter for system-level ESD protection in display panels," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 1278–1287, Feb. 2012.

[29] C.-C. Yen, W.-Y. Lin, and M.-D. Ker, “Transient-to-digital converter to detect electrical fast transient (EFT) disturbance for system protection design,” in *Proc. IEEE ICICDT*, 2011, pp. 1-4.

[30] M.-D. Ker, W.-Y. Lin, C.-C. Yen, C.-M. Yang, T.-Y. Chen, and S.-F. Chen, “On-chip ESD detection circuit for system-level ESD protection design,” in *Proc. IEEE ICSICT,* 2010, pp. 1584–1587.

[31] M.-D. Ker, W.-Y. Lin, C.-C. Yen, C.-M. Yang, T.-Y. Chen, and S.-F. Chen, “New transient detection circuit for electrical fast transient (EFT) protection design in display panels,” in *Proc. IEEE ICIDT*, 2010, pp. 51-54

[32] M.-D. Ker, C.-S. Liao, and C.-C. Yen, “Transient detection circuit for system-level ESD protection and its on-board behavior with EMI/EMC filters,” in *Proc. IEEE Int. Symp. Electromagn. Compat. (EMC)*, 2008. pp. 1-4

[33] M.-D. Ker, C.-C. Yen, and P.-C. Shin, “On-chip transient detection circuit for system-level ESD protection in CMOS ICs,” in *Proc. IEEE Custom Integrated Circuits Conf.*, 2006, pp. 361–364.

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