國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

佈局最佳化的低壓元件堆疊來達成
高壓積體電路之靜電放電防護設計

Optimization of Stacked Low-Voltage PMOS for High-Voltage ESD Protection with Layout Consideration

研 究 生：廖顯峰　　(Seian-Feng Liao)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國一〇四年九月

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碩士論文

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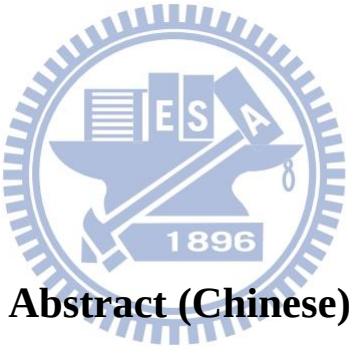
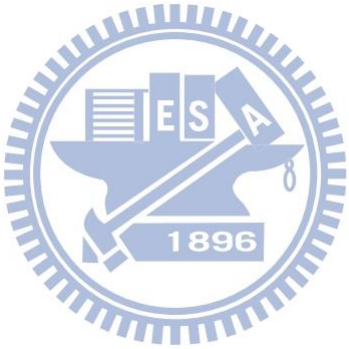


Abstract (Chinese)

靜電放電防護和閂鎖效應 (latchup) 預防是在積體電路中兩個重要的可靠度議題，尤其是在高壓應用方面。靜電放電可能發生在積體電路產品製造、封裝、組裝的過程中，通常會造成在積體電路中嚴重的損害，而在電路正常操作情況下，雜訊可能會觸發積體電路內部的寄生電晶體，所以在高壓靜電放電防護設計中，必須使持有電壓 (holding voltage) 高於電路操作電壓，否則在應用上可能會發生閂鎖效應 (latchup)。

高壓的靜電防護設計中，通常使用橫向擴散電晶體 (lateral diffused MOS, LDMOS)，但通常橫向擴散電晶體的持有電壓小於電路的操作電壓，會有閂鎖效應的風險，因此提出使用低壓電晶體來做堆疊結構來達到在高壓中靜電防護有著高持有電壓的一種方法，藉由調整元件的不同堆疊個數，使得在不同高壓應用來提供有效的靜電防護。

在此篇論文中，實驗並驗證堆疊結構，藉由多種不同的佈局方式來增加元件的靜電耐受度，並且使用不同的防護環 (guard-ring) 的佈局方式，探討對持有電壓的影響。此外，使用不同傳輸線脈衝產生器 (transmission line pulsing, TLP) 脈衝寬度對持有電壓的影響，以及試著減少其佈局面積達到相同的靜電耐受度。



Optimization of Stacked Low-Voltage PMOS for High-Voltage ESD Protection with Layout Consideration

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Abstract

Electrostatic discharge (ESD) protection and latchup prevention are two important reliability issues to the CMOS integrated circuits, especially in high-voltage (HV) applications. ESD may occur accidentally during the fabrication, package, and assembling processes of IC products, which often caused serious damages on ICs. During normal circuit operation, the noise might unpredictably trigger the parasitic BJT of the ESD devices. Furthermore, to avoid latchup issue, the holding voltage (V_h) should be larger than the supply voltage of the internal circuits in ESD protection design for HV applications.

Lateral DMOS (LDMOS) was often used as ESD protection device in HV process, but the holding voltage (V_h) of LDMOS after snapback was smaller than the circuit operating voltage (V_{CC}). Thus, the LDMOS was sensitive to latchup issue. Therefore, the stacked configuration of LV devices is a way to achieve a high holding voltage for ESD protection in

HV circuits. By adjusting the stacking numbers of stacked PMOSs, it can provide effective ESD protection for various HV applications.

In this thesis, stacks for ESD protection are implemented and verified, and it is discussed about different layout parameters to effectively improve ESD robustness of ESD devices. The guard-ring layout on the stacked LV devices was further investigated holding voltage in silicon chip. In addition, the pulse width of the transmission line pulsing (TLP) system was also investigated holding voltage in silicon chip. Decreasing the layout area to get high ESD robustness and latchup-free immunity for HV applications.

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首先要感謝柯明道老師，在碩士班這兩年的指導，在上台報告時，老師總能很快地指出問題所在，讓我能透過問題，仔細思考後，得到新的知識，也非常謝謝老師可以推薦我去公司工讀實習，能夠提早一步進入業界探索。

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廖顯峰

104 年 9 月於竹塹交大

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Chapter 1
Introduction

In this chapter, the motivation of this thesis is depicted first. The chapter shows the advantage of stacking in high-voltage (HV) applications, and different guard-ring layout types can achieve both of good ESD robustness and high latchup-free immunity with reasonable total layout area. Electrostatic discharge (ESD) protection scheme reveals the typical arrangement for integrated circuits (ICs). It also introduces the concerns of ESD protection design and testing methods. Finally, thesis organization is included in the end of this chapter.

1.1 Motivation

Electrostatic discharge (ESD) may occur accidentally to cause damages on IC products during the fabrication, package, and assembling processes, which often caused serious damages on ICs. High-voltage (HV) ICs were found with bad ESD robustness [1]-[2].

Lateral DMOS (LDMOS) was often used as ESD protection device in HV process, but the holding voltage (V_h) of LDMOS after snapback was smaller than the circuit operating voltage (V_{CC}) [3]-[4]. Thus, the LDMOS was sensitive to latchup issue. Therefore, the stacked configuration of LV devices is a way to achieve a high holding voltage for ESD protection in HV circuits [5]-[7].It is suggested that ICs should require 2kV in human body model (HBM) and 200V in machine model (MM) [8], [9].

Stacking low-voltage devices is an excellent solution for latchup immunity and ESD robustness. The total holding voltage of stacked PMOSs is the multiple of the holding voltage of single PMOS. The total trigger voltage (V_{t1}) of stacked PMOSs is also the multiple of the trigger voltage of single PMOS. The secondary breakdown current (I_{t2}) of stacked PMOSs are almost the same in spite of different stacking numbers [10]. The main layout parameters to

affect ESD robustness of CMOS devices are the channel width, the channel length, the clearance from contact to poly-gate edge at drain and source regions, the spacing from the drain diffusion to the guard-ring diffusion, and the finger width of each unit finger. The optimized layout parameters have been verified to effectively improve ESD robustness of CMOS devices [11]. Try to use different layout methods to improve ESD robustness on stacking low-voltage devices effectively. In addition, the ESD devices should be surrounded by the guard ring in real circuit application. The ESD device without the guard ring can reduce the layout area, but it might cause the latchup issue under the normal circuit operation.

1.2 ESD Protection Scheme in High-Voltage Integrated Circuits

A typical whole-chip ESD protection scheme is shown in Fig. 1.1. The ESD stresses on each I/O pin have four stress modes of pin combination with the relatively grounded GND pin or VDD/VCC pin [12]. The ESD stresses could also happen from the VCC pin to the GND pin with positive or negative voltage pulses [12]. Stacked devices can be the ESD protection cells at the input or output pads or the power-rail ESD clamp between the VCC/GND power lines.

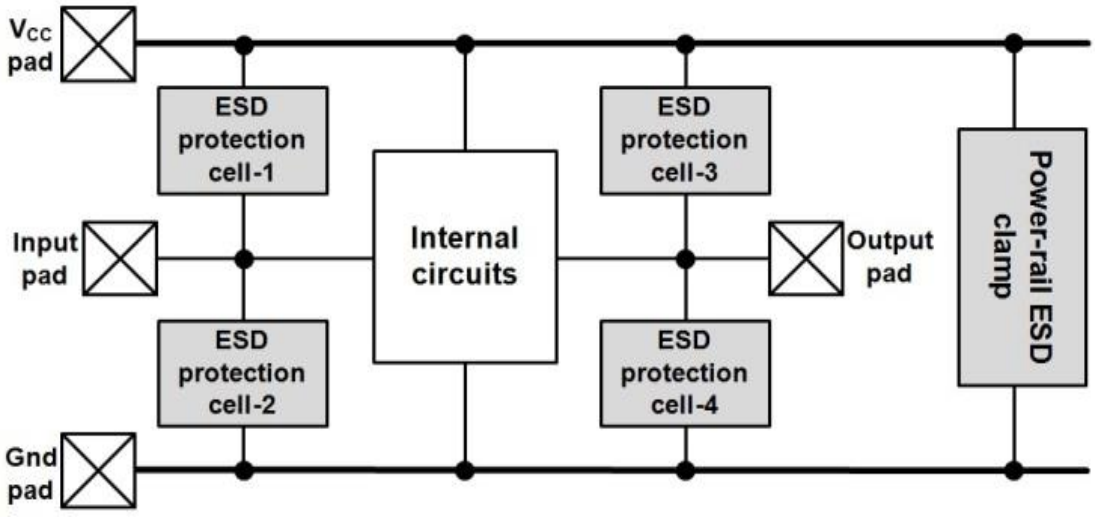


Fig. 1.1 A typical whole-chip ESD protection scheme

The typical I-V characteristics of ESD protection devices are illustrated in Fig. 1.2.

Breakdown voltage (V_{BD}) and supply voltage (V_{DD} or V_{CC}) of the internal circuits divide the plot into three parts. The middle part is the desired ESD protection window. The green curve is an example of the desired ESD device's I-V characteristics. To get an effective ESD protection, the trigger voltage (V_{t1}) should be smaller than breakdown voltage of the internal circuits. Furthermore, to avoid latchup issue, the holding voltage (V_h) should be larger than the supply voltage of the internal circuits. The on-resistance of an ESD protection device should be as small as possible to get a high ESD robustness. The I-V characteristics of ESD devices should fit into this window for both effective ESD protection and latchup-free design.

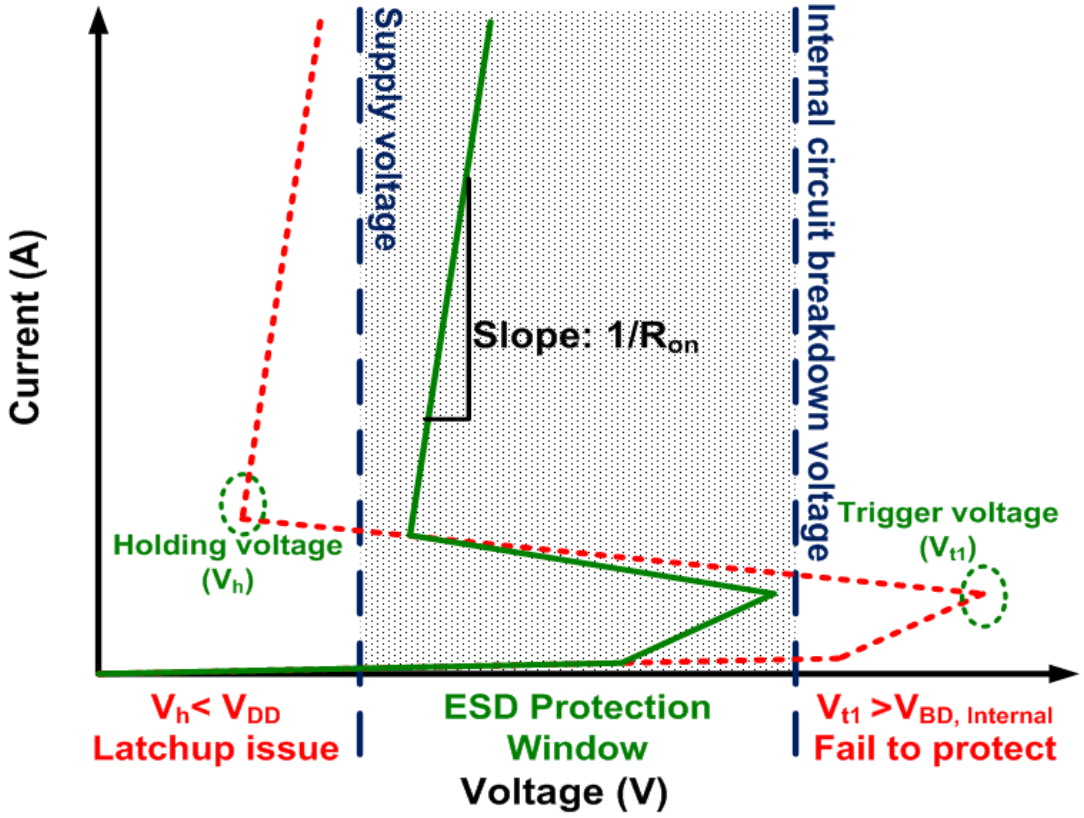
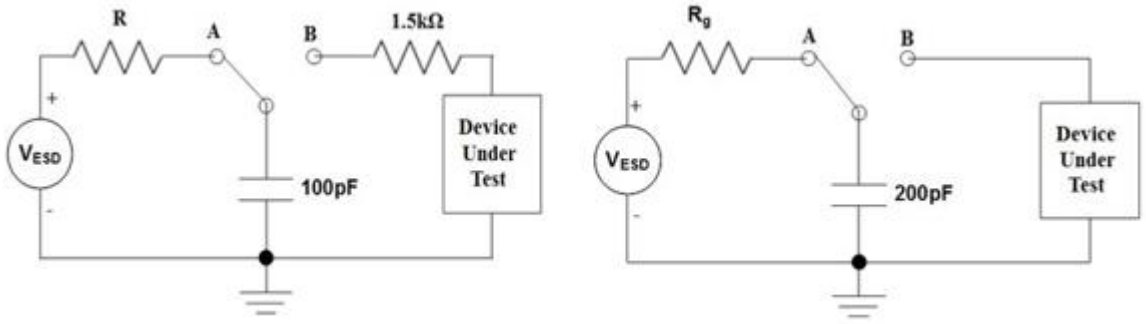


Fig. 1.2 The ESD protection design window [10]

1.3 Measurement Methods

ESD could induce serious yield > loss in ICs. Change may accumulate in human bodies and machines. When one pin connected to ground, the ESD current may damage ICs. It is suggested that ICs should require 2kV in human body model (HBM) and 200V in machine

model (MM). There are several ways to test ESD robustness. The equivalent models of HBM and MM are illustrated in Fig. 1.3.



(a) (b)

Fig. 1.3 Equivalent circuits of (a) HBM and (b) MM

Transmission line pulse (TLP) system can measure the ESD-related device parameters for ESD protection design. The Barth pulse curve tracer 4002 TLP is used to measure the TLP I-V curve. It is common to use 100-ns pulse width. It can be obtained device parameters such as trigger voltage (V_{t1}), holding voltage (V_h), secondary breakdown current (I_{t2}) and on-resistance (R_{on}) from TLP I-V curve. Higher secondary breakdown current usually means a higher ESD level.

The holding voltage of n-channel LDMOS in an HV BCD process has been investigated by TLP measurements with different pulse widths and dc curve tracer. It is found that the holding voltages of an n-channel LDMOS measured by 100-ns TLP system and curve tracer are substantially different [13]. The I-V curve of the long pulse width TLP measured by TLP celestron-1 in this thesis. The TLP I-V curve can be measured by 100-ns, 200-ns, 500-ns and 800-ns pulse width. The I-V curve can be measured by curve tracer Tek370 in a dc condition. During latchup test, the positive or negative current of up to 200mA will be directly applied to the I/O pin [14]. Such latchup-test current will be injected into the substrate through the on-chip ESD device that is often drawn with the I/O pad together to provide ESD protection.

1.4 Thesis Organization

This thesis focuses on optimization of stacked low-voltage devices for good ESD robustness and latchup immunity. In chapter 1, it introduces research motivation, measurement methods and an ESD protection scheme.

It describes the dependence of layout parameters on ESD robustness of stacked LV PMOSs in chapter 2. Chapter 3 shows stacked PMOSs with different guard ring layouts for HV ESD protection. In this thesis, the stacked LV PMOS devices have been successfully verified in a VIS 0.5-μm HV process and 0.25-μm 80V BCD process. In chapter 4, conclusions and future work.

Chapter 2

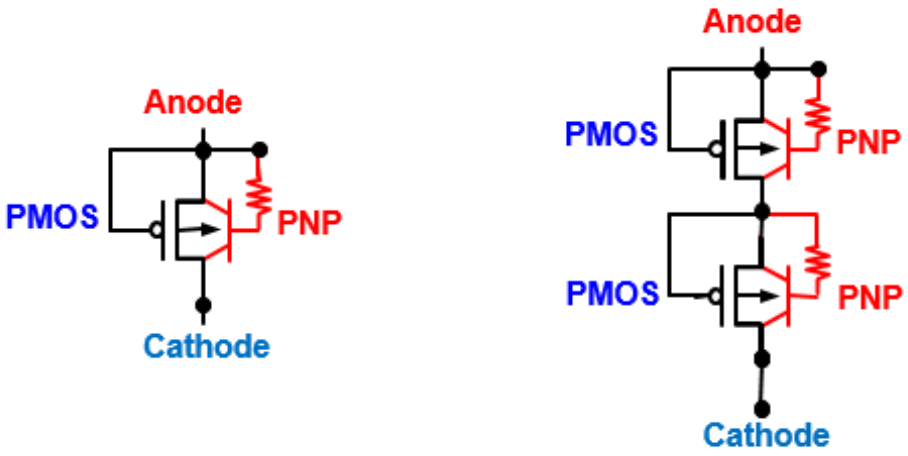
Layout Optimization on the Stacked Low-Voltage PMOS for High-Voltage ESD Protection

Stacking is a good way to reach high holding voltage for high-voltage ESD protection. The trigger voltage and the holding voltage of stacked configuration can be adjusted to meet different HV applications. In this chapter, the dependence of layout parameters on ESD robustness of stacked LV PMOSs. In this work, the stacked LV PMOS devices have been successfully verified in a VIS 0.5-μm HV process and 0.25-μm 80V BCD process.

2.1 Stacked Low-Voltage PMOS in a 0.5-μm HV Process

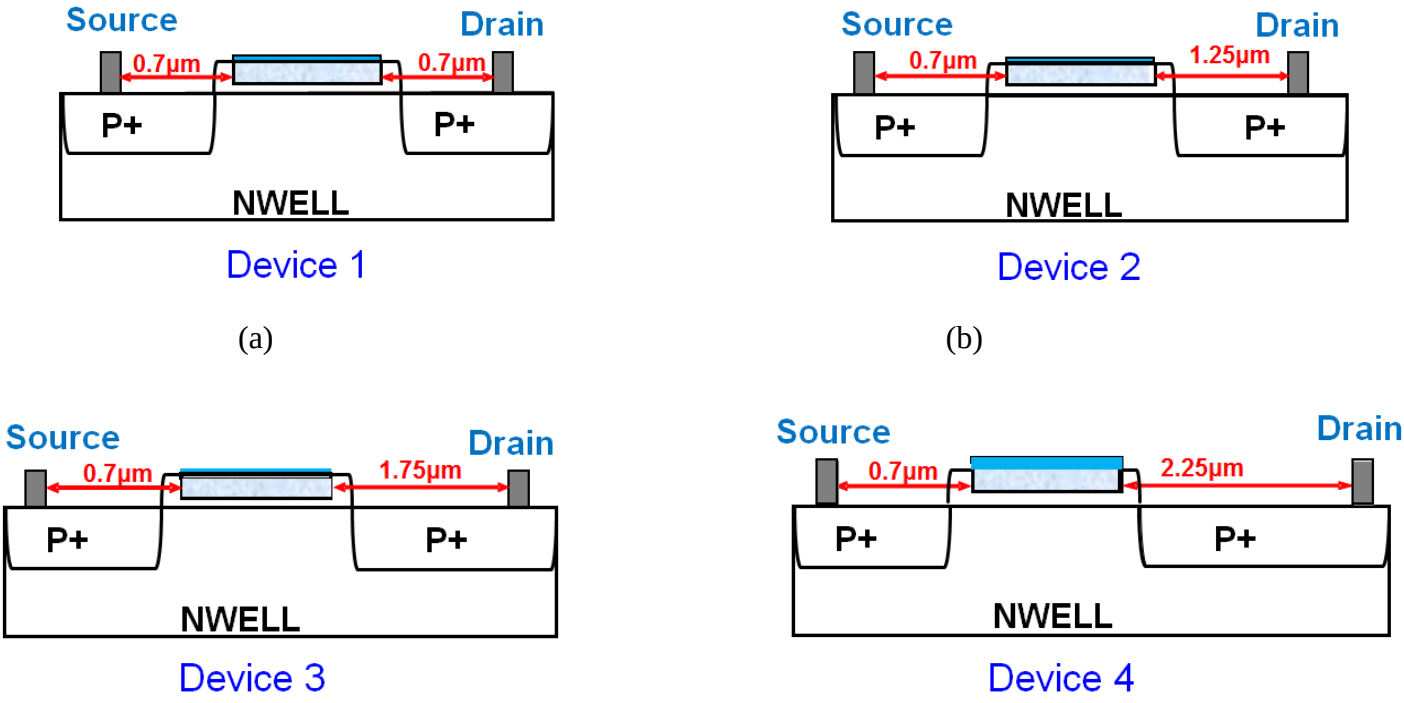
2.1.1 Stacking Units

A PMOS was fabricated in a 0.5-μm HV process, which has a device dimension of W/L = 800μm/0.5μm. The equivalent circuits are showed in Fig. 2.1. The stacked LV PMOSs with two and three stacking numbers are investigated in this work, which are designed to meet 20-V and 30-V HV applications. There are four different stacking units, the spacing from drain contact to poly-gate edge (d1) of PMOS devices are investigated through the fabricated test chips. The cross-section view of PMOS stacking units are showed in Fig. 2.2. The d1 spacing of stacking units are drawn with 0.7μm, 1.25μm, 1.75μm, and 2.25μm in Fig. 2(a), Fig. 2(b), Fig. 2(c) and Fig. 2(d).



(a) (b)

Fig. 2.1 Equivalent circuits of (a) a single LV PMOS and (b) stacked LV PMOSs structure



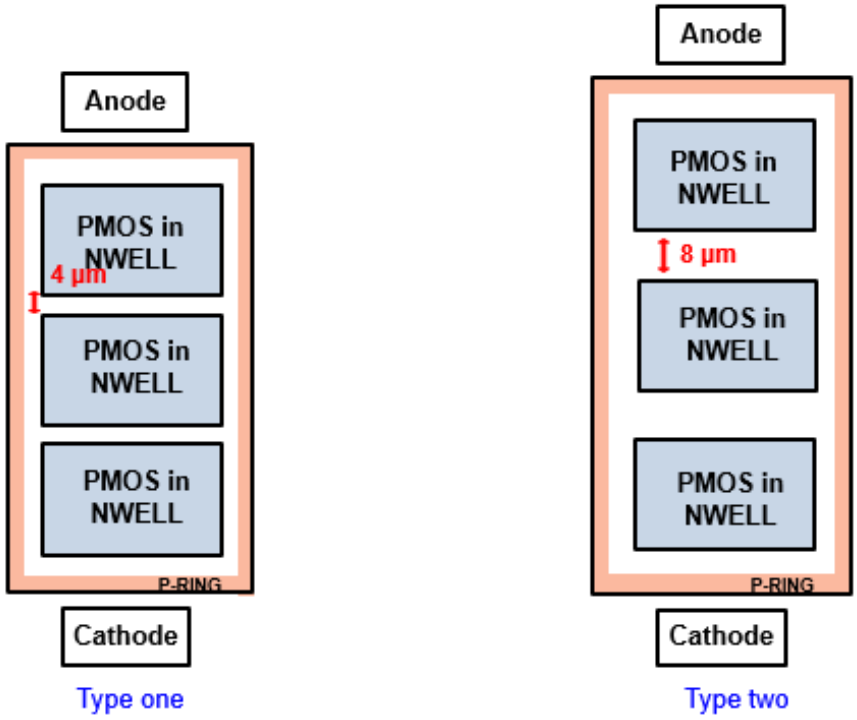
(a) (b)

(c) (d)

Fig. 2.2 The cross-section views of PMOS stacking unit drawn with (a) the drain contact to poly-gate edge (d1) spacing of 0.7μm, (b) the d1 spacing of 1.25μm, (c) the d1 spacing of 1.75μm, and (d) the d1 spacing of 1.25μm

2.1.2 *Device Types*

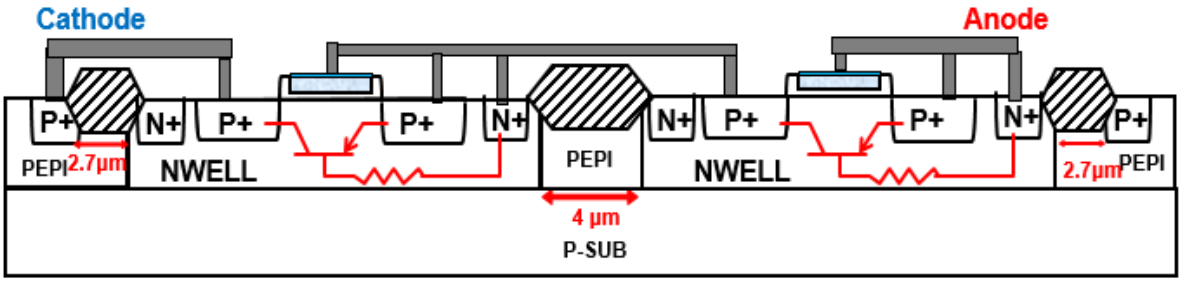
The ESD devices should be surrounded by the guard ring in real circuit application. These four kinds of devices have different types of the guard ring layouts. There are two types (type one and type two) of the guard ring layouts to surround the stacked PMOSs, as shown in Fig. 2.3, where 3-PMOSs stacked structure is demonstrated. In type one and type two, the stacked PMOSs were surrounded by one P-ring that is typically connected to cathode. The NWELL spacing between each N-well in the type one (type two) is 4μm (8μm). The clearance of P-ring to the N-well edge is kept at 2.7μm, which is a layout rule specified by the foundry in the given 0.5-μm process.



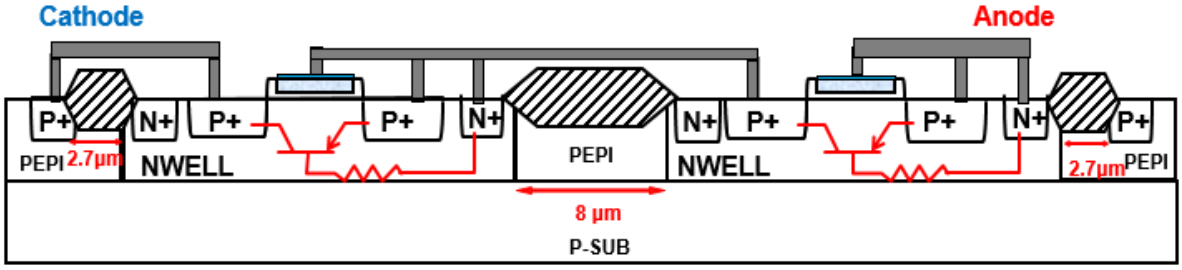
(a) (b)

Fig. 2.3 The two types of guard-ring layout for 3-PMOSs stacked structure, (a) with one whole p-ring and NWELL spacing of 4μm and (b) with one whole p-ring and NWELL spacing of 8μm

Each LV PMOS in the stacked configuration is drawn with the total channel width of 800μm and a channel length of 0.5μm. The cross-sectional view of stacked structure with two LV PMOSs is shown in Fig. 2.4. The NWELL spacings of the two LV PMOSs are drawn with 4μm and 8μm in Fig. 2.4(a) and Fig. 2.4(b), respectively. The gate of each PMOS is connected to its local high potential point, so each PMOS in the stacked structure is kept in the off state during the normal circuit operation. The P+ diffusion (drain) of the bottom PMOS in the stacked PMOSs is connected to the cathode. The P-ring is connected to the cathode, which is typically biased at ground with the common p-substrate.



(a)



(b)

Fig. 2.4 The cross-sectional views of stacked structure with two LV PMOSs drawn with (a) the NWELL spacing of 4μm (type one) and (b) the NWELL spacing of 8μm (type two). Each LV PMOS has its own separated N-well in the stacked structure

2.1.3 Experiment Results

All test devices of stacked PMOSs had been fabricated in a 0.5-μm HV process. Each PMOS in all stacked structure is drawn with a channel width of 800μm and a channel length

of 0.5μm. Every layout type has 2-PMOSs and 3-PMOSs stacked structures. The TLP-measured I-V characteristics of device 1 with the two types of guard ring layout are shown in Fig. 2.5. The detailed characteristics of device 1 stacked structure with different guard-ring types are listed in Table 2.1.

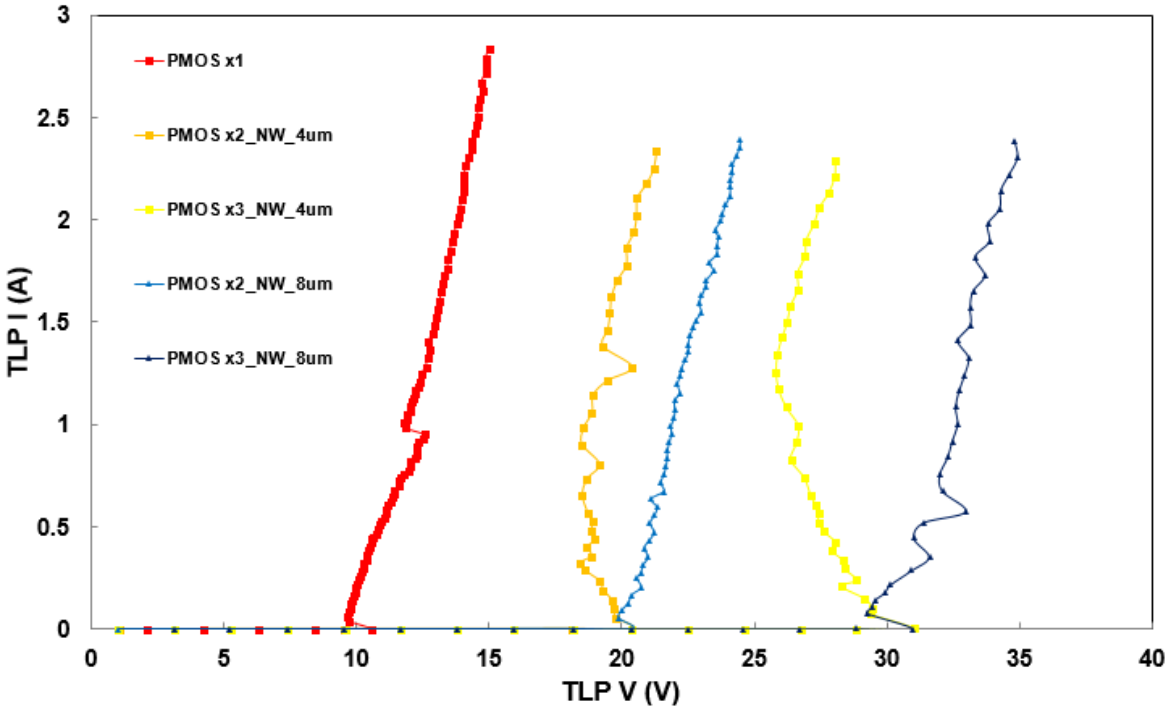


Fig. 2.5 The TLP-measured I-V characteristics of device 1 with different guard-ring layouts

Table 2.1

The measurement data of device 1

d1 is 0.7 μm	TLP				DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	R_{on} (Ω)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
PMOS x1	10.57	9.68	1.91	2.79	11.1	5.5	250
PMOS x2_NW_4μm	20.39	18.41	1.44	2.25	20.5	4.5	300
PMOS x3_NW_4μm	31.02	25.81	2.32	2.21	34	4.5	300
PMOS x2_NW_8μm	20.4	19.88	1.98	2.35	22.1	4.5	300
PMOS x3_NW_8μm	30.99	29.27	2.54	2.3	33.5	4.5	300

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

In Table 2.1, the trigger voltage of stacked PMOSs is the multiple of the trigger voltage of single PMOS, but the holding voltage of type one is smaller than type two. It will be discussed about guard-ring layout in the chapter 3. The breakdown voltage of stacked PMOSs

is the multiple of the breakdown voltage of single PMOS. The breakdown voltage is defined the off current equal 1μA in DC measurement. All of stacked structure with two guard-ring types can pass 4.5 kV in the human-body-model (HBM) ESD test and 300 V in the machine-model (MM) ESD test.

The TLP-measured I-V characteristics of device 2 with the two types of guard ring layout are shown in Fig. 2.6. The detailed characteristics of device 2 stacked structure with different guard-ring types are listed in Table 2.2.

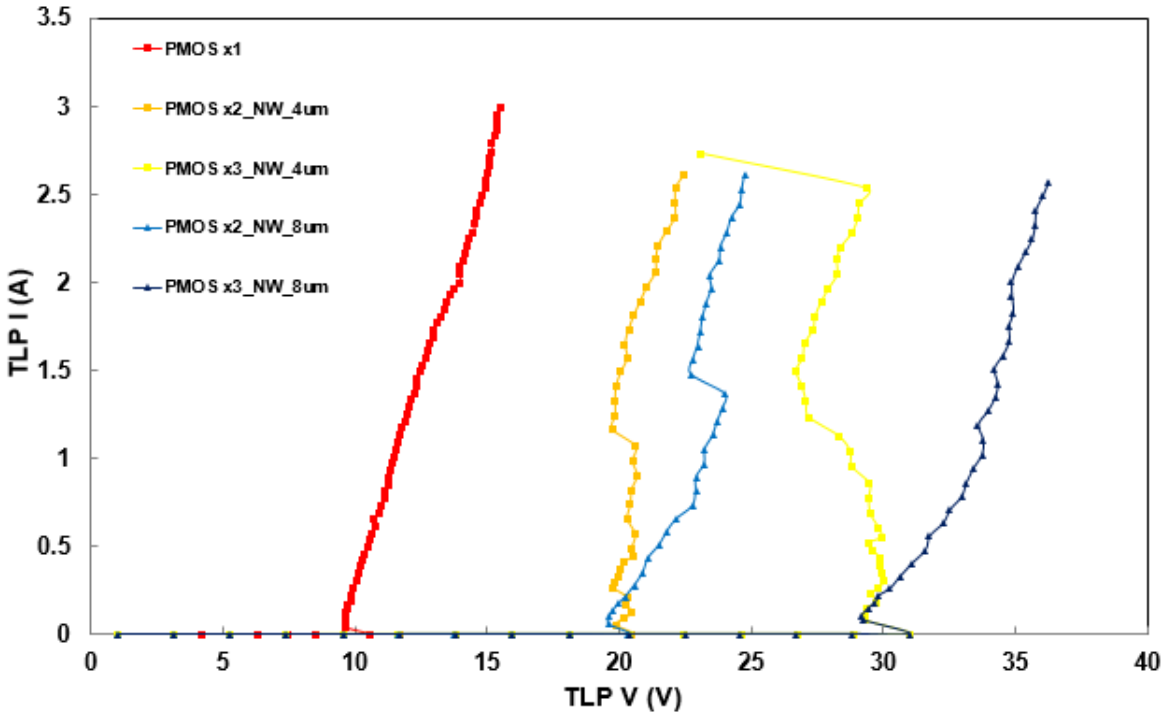


Fig. 2.6 The TLP-measured I-V characteristics of device 2 with different guard-ring layouts

Table 2.2

The measurement data of device 2

d1 is 1.25 μm	TLP				DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	R_{on} (Ω)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
PMOS x1	10.59	9.62	2.02	2.95	11.1	6	300
PMOS x2_NW_4μm	20.43	19.74	1.75	2.54	20.4	5	300
PMOS x3_NW_4μm	31.02	26.69	2.62	2.53	30.9	5	300
PMOS x2_NW_8μm	20.34	19.61	2.05	2.52	22.3	5	300
PMOS x3_NW_8μm	30.98	29.17	2.88	2.49	34	5	300

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The TLP-measured I-V characteristics of device 3 with the two types of guard ring layout are shown in Fig. 2.7. The detailed characteristics of device 3 stacked structure with different guard-ring types are listed in Table 2.3.

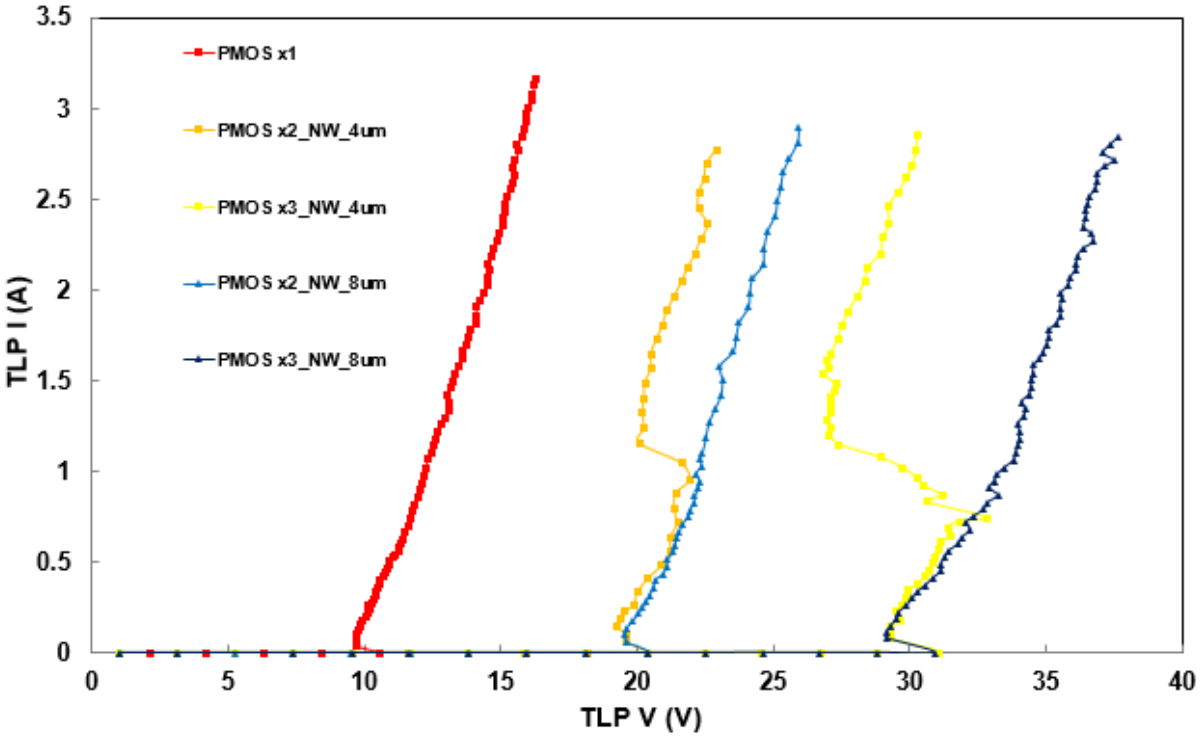


Fig. 2.7 The TLP-measured I-V characteristics of device 3 with different guard-ring layouts

Table 2.3

The measurement data of device 3

d1 is 1.75 μm	TLP				DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	R_{on} (Ω)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
PMOS x1	10.57	9.68	2.14	3.12	10.1	6	300
PMOS x2_NW_4μm	20.38	19.26	1.29	2.69	20.4	5	300
PMOS x3_NW_4μm	31.09	26.85	2.74	2.77	34	5.5	300
PMOS x2_NW_8μm	20.36	19.57	2.33	2.81	22.3	5.5	300
PMOS x3_NW_8μm	30.91	29.13	3.05	2.8	34	5.5	300

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The TLP-measured I-V characteristics of device 4 with the two types of guard ring layout are shown in Fig. 2.8. The detailed characteristics of device 4 stacked structure with different guard-ring types are listed in Table 2.4.

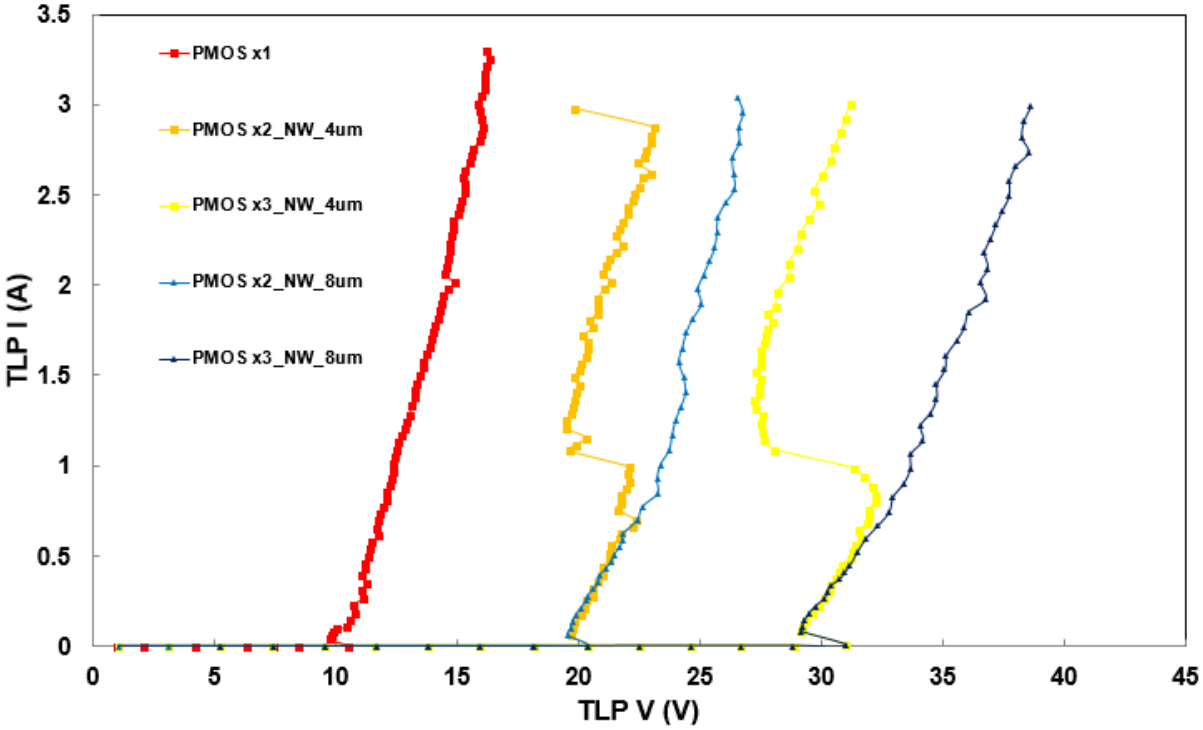


Fig. 2.8 The TLP-measured I-V characteristics of device 4 with different guard-ring layouts

Table 2.4

The measurement data of device 4

d1 is 2.25 μm	TLP				DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	R_{on} (Ω)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
PMOS x1	10.55	9.76	2.04	3.25	10.1	6	300
PMOS x2_NW_4μm	20.36	19.47	2.2	2.87	20.4	5.5	300
PMOS x3_NW_4μm	31.01	27.24	2.4	2.92	34.5	5.5	300
PMOS x2_NW_8μm	20.35	19.58	2.49	2.96	22.3	5.5	300
PMOS x3_NW_8μm	30.99	29.18	2.91	3.23	33.9	5.5	350

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The TLP-measured I-V characteristics of the stacked 2-PMOSs and 3-PMOSs with the guard-ring layout type one (type two) are compared in Fig. 2.9 (Fig. 2.10). The detailed

characteristics of different devices with same type guard ring layout are listed in Table 2.5 and Table 2.6.

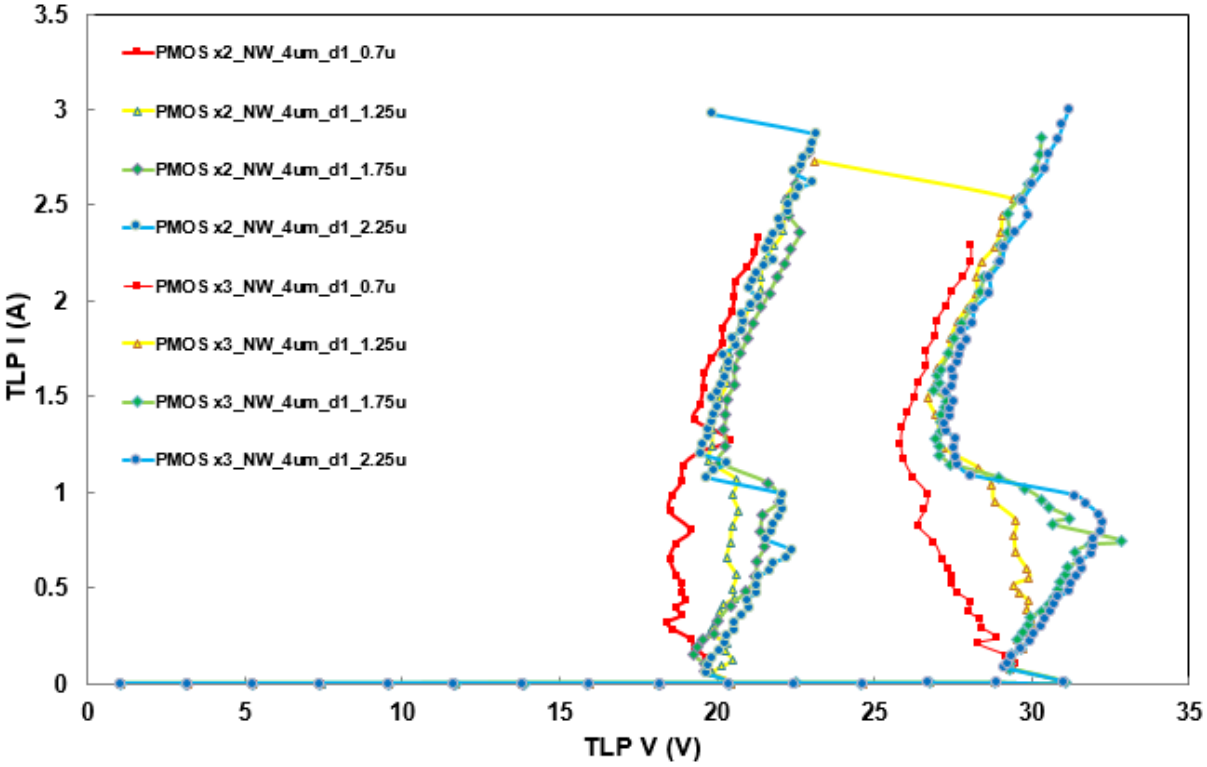


Fig. 2.9 The TLP-measured I-V characteristics of devices with guard-ring layout type one

Table 2.5

The measurement data of devices with guard-ring layout type one

type one	TLP				DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	R_{on} (Ω)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
PMOS x2_NW_4μm_d1_0.7 μm	20.39	18.41	1.44	2.25	20.5	4.5	300
PMOS x2_NW_4μm_d1_1.25 μm	20.43	19.74	1.75	2.54	20.4	5	300
PMOS x2_NW_4μm_d1_1.75 μm	20.38	19.26	1.29	2.69	20.4	5	300
PMOS x2_NW_4μm_d1_2.25 μm	20.36	19.47	2.2	2.87	20.4	5.5	300
PMOS x3_NW_4μm_d1_0.7 μm	31.02	25.81	2.32	2.21	34	4.5	300
PMOS x3_NW_4μm_d1_1.25 μm	31.02	26.69	2.62	2.53	30.9	5	300
PMOS x3_NW_4μm_d1_1.75 μm	31.09	26.85	2.74	2.77	34	5.5	300
PMOS x3_NW_4μm_d1_2.25 μm	31.01	27.24	2.4	2.92	34.5	5.5	300

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

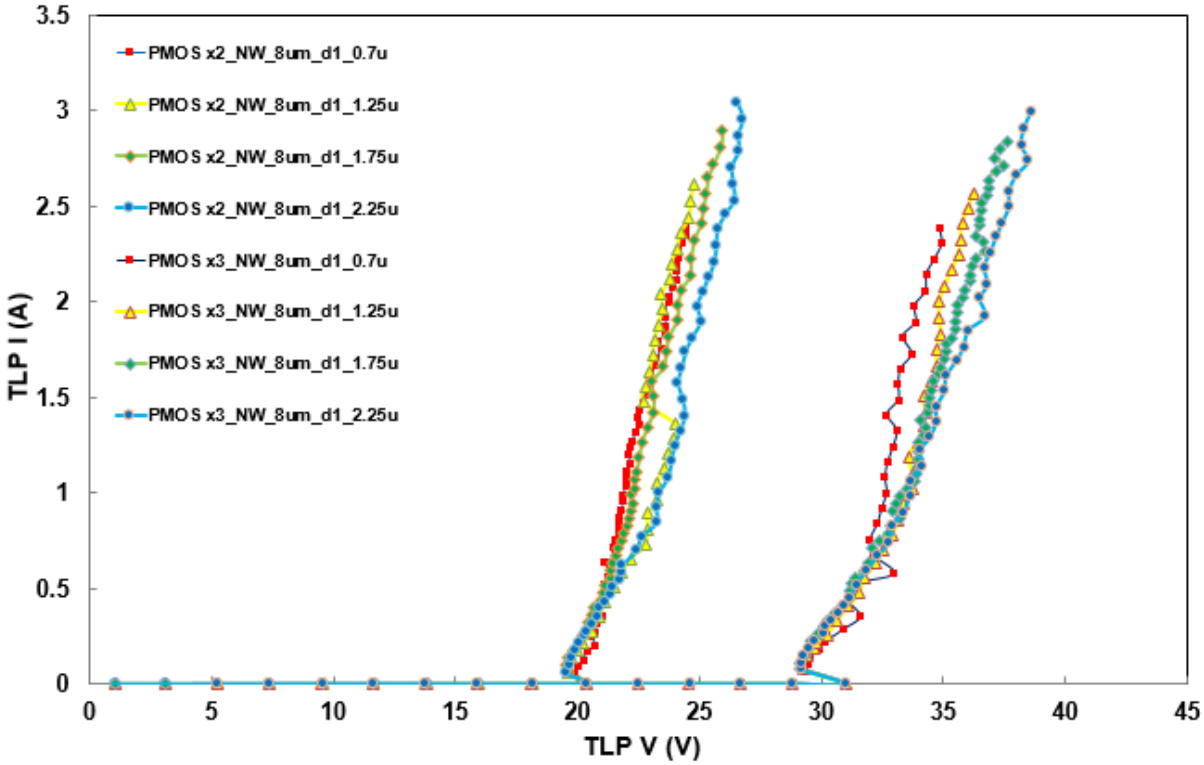


Fig. 2.10 The TLP-measured I-V characteristics of devices with guard-ring layout type two

Table 2.6

The measurement data of devices with guard-ring layout type two

type two	TLP				DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	R_{on} (Ω)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
PMOS x2_NW_8μm_d1_0.7 μm	20.4	19.88	1.98	2.35	22.1	4.5	300
PMOS x2_NW_8μm_d1_1.25 μm	20.34	19.61	2.05	2.52	22.3	5	300
PMOS x2_NW_8μm_d1_1.75 μm	20.36	19.57	2.33	2.81	22.3	5.5	300
PMOS x2_NW_8μm_d1_2.25 μm	20.35	19.58	2.49	2.96	22.3	5.5	300
PMOS x3_NW_8μm_d1_0.7 μm	30.99	29.27	2.54	2.3	33.5	4.5	300
PMOS x3_NW_8μm_d1_1.25 μm	30.98	29.17	2.88	2.49	34	5	300
PMOS x3_NW_8μm_d1_1.75 μm	30.91	29.13	3.05	2.8	34	5.5	300
PMOS x3_NW_8μm_d1_2.25 μm	30.99	29.18	2.91	3.23	33.9	5.5	350

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

From the experimental results, the larger d1 parameter can cause larger I_{t2} of stacked PMOS devices. From above results with TLP-measured I_{t2} and ESD test, the device 4 among is the best choice for the stacked PMOSs structure for HV ESD protection. All of device 4

with two guard-ring types can pass 5.5 kV in the human-body-model (HBM) ESD test and 300 V in the machine-model (MM) ESD test. The holding voltage of type one still suffers latchup risk for 20V and 30V application. During ESD zapping, the ESD current unpredictably trigger the other parasitic BJT of the ESD devices. It induces the holding voltage (V_h) of type one smaller than the holding voltage (V_h) of type two. Guard-ring layout will be discussed in the Chapter 3. The type two among is the best choice for the stacked PMOSs structure for HV ESD protection.

2.2 Stacked Low-Voltage PMOS in a 0.25-μm BCD Process

2.2.1 Typical Devices

The test devices were all fabricated in a VIS 0.25-μm Bipolar-CMOS-DMOS (BCD) process. The main layout parameters to affect ESD robustness of ESD devices are the silicide blocking, the spacing from drain contact to poly-gate edge (d1), contact number, the channel length, and total width. The optimized layout parameters have been verified to effectively improve ESD robustness of ESD devices. Try to achieve this concept in stacked LV PMOS structure. Stacking number was from 1 to 10 in this test. Typical PMOS devices in this investigation, the clearance from the resist-protection-oxide (RPO) to poly-gate edge, the clearance from the drain contact to poly-gate edge (d1), the drain contact number (co), the channel length (L), the single finger width, and the total width are kept at 0.3μm, 2μm, 2, 0.8μm, 30μm ,and 360μm, respectively. The cross-section view of typical PMOS stacking unit is showed in Fig. 2.11.

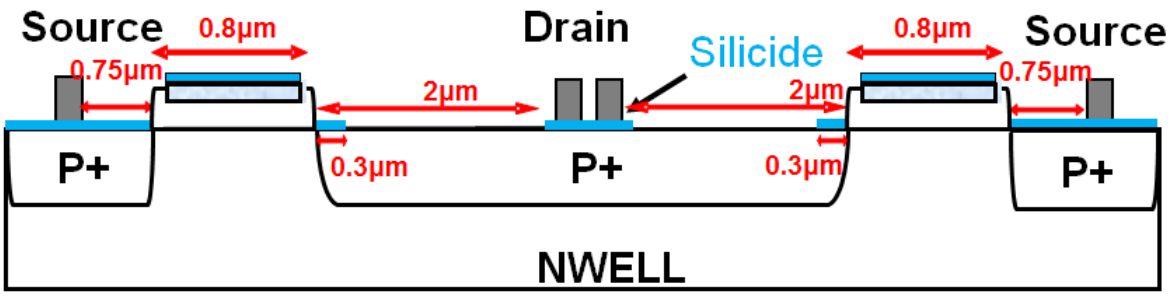
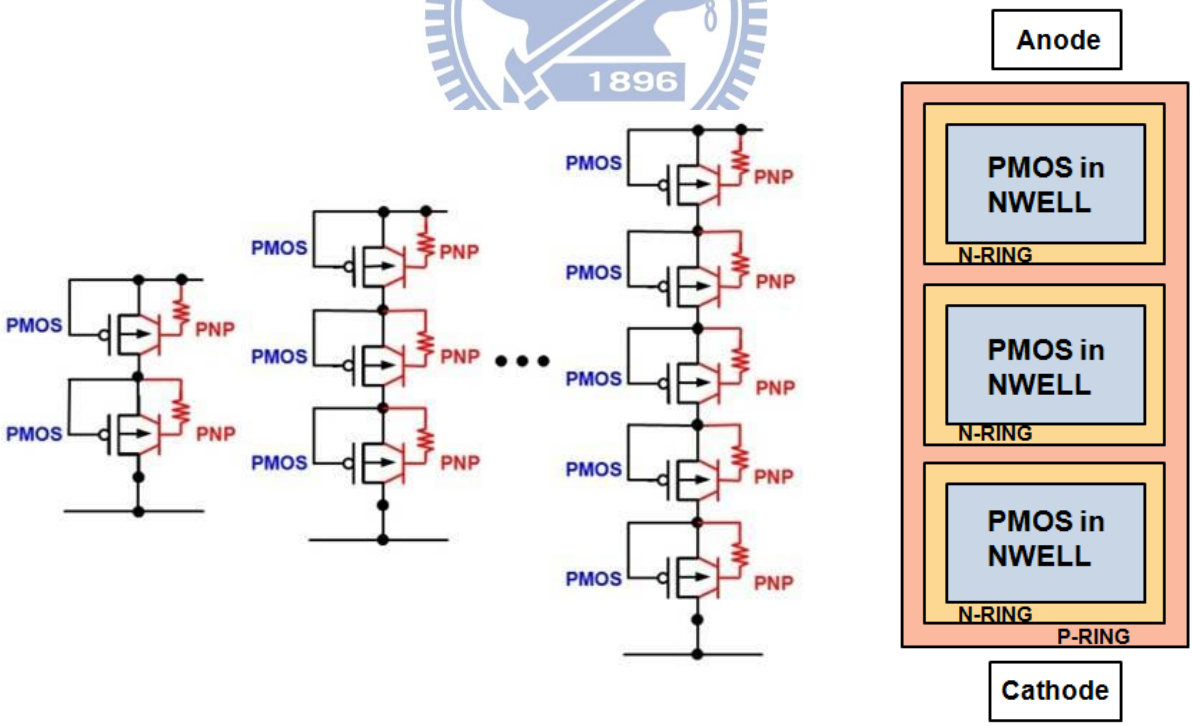


Fig. 2.11 The cross-section view of typical PMOS

Low-voltage devices should be surrounded by isolation ring for HV applications. Isolation rings are composed by a HV-NWELL ring and a HV-PWELL ring. The P+ diffusion (drain) of the bottom PMOS in the stacked PMOSs is connected to the cathode. The HV-PWELL ring is connected to the cathode, which is typically biased at ground with the common p-substrate. The HV-NWELL ring is tied to relative high potential point. Fig. 2.12(a) and Fig. 2.12(b) show the schematic of stacked LV PMOSs for HV ESD protection and the top view respectively.



(a) (b)

Fig. 2.12 The (a) schematic of stacked LV PMOSs with different stacking numbers and (b) top view for 3-PMOSs stacked structure

2.2.2 *Layout Parameters of Test Devices*

There are four splits about RPO effect of PMOS, which focus on full silicide (no RPO) and silicide blocking. The RPO spacing is decrease from 0.3μm (typical) to -0.06μm at the drain region. There are several splits about the drain contact to poly-gate edge (d1) effect and drain contact number (co). The spacings of the drain contact to poly-gate edge (d1) are 2μm (typical), 4μm, and 6μm, and the clearance variation on the drain contact number (co) splits from 2 (typical) to 4. There are two splits about channel length (L) effect of PMOS, the clearance variation are 0.8μm (typical) and 1μm. The clearance variation on total width splits from 360μm (typical) to 600μm. The single finger width of the PMOS devices with total width of 360μm (typical) and 600μm are 30μm and 50μm, respectively.

2.2.3 *Experiment Results*

The TLP measured I-V characteristics of typical stacked LV PMOSs are shown in Fig. 2.13. The holding voltages of stacked LV PMOSs with different stacking numbers can be found in Fig. 2.13. The total holding voltage of stacked PMOSs is the multiple of the holding voltage of single PMOS. The total trigger voltage of stacked PMOSs is also the multiple of the trigger voltage of single PMOS. The secondary breakdown current (I_{t2}) of stacked PMOSs are almost the same in spite of different stacking numbers. The detailed characteristics of typical stacked LV PMOSs are listed in Table 2.7.

The TLP measured I-V characteristics of full silicide (no RPO) stacked LV PMOSs are shown in Fig. 2.14. All of full silicide (no RPO) stacked LV PMOSs can pass 4 kV in the human-body-model (HBM) ESD test and 200 V in the machine-model (MM) ESD test. The detailed characteristics of full silicide (no RPO) stacked LV PMOSs are listed in Table 2.7. The TLP measured I-V characteristics of silicide blocking stacked LV PMOSs are shown in Fig. 2.14, Fig. 2.15, Fig. 2.16. The spacings of RPO are 0μm (overlap poly-gate), -0.03μm, and -0.06μm. The detailed characteristics of silicide blocking stacked LV PMOSs are listed in Table 2.8, Table 2.9, and Table 2.10.

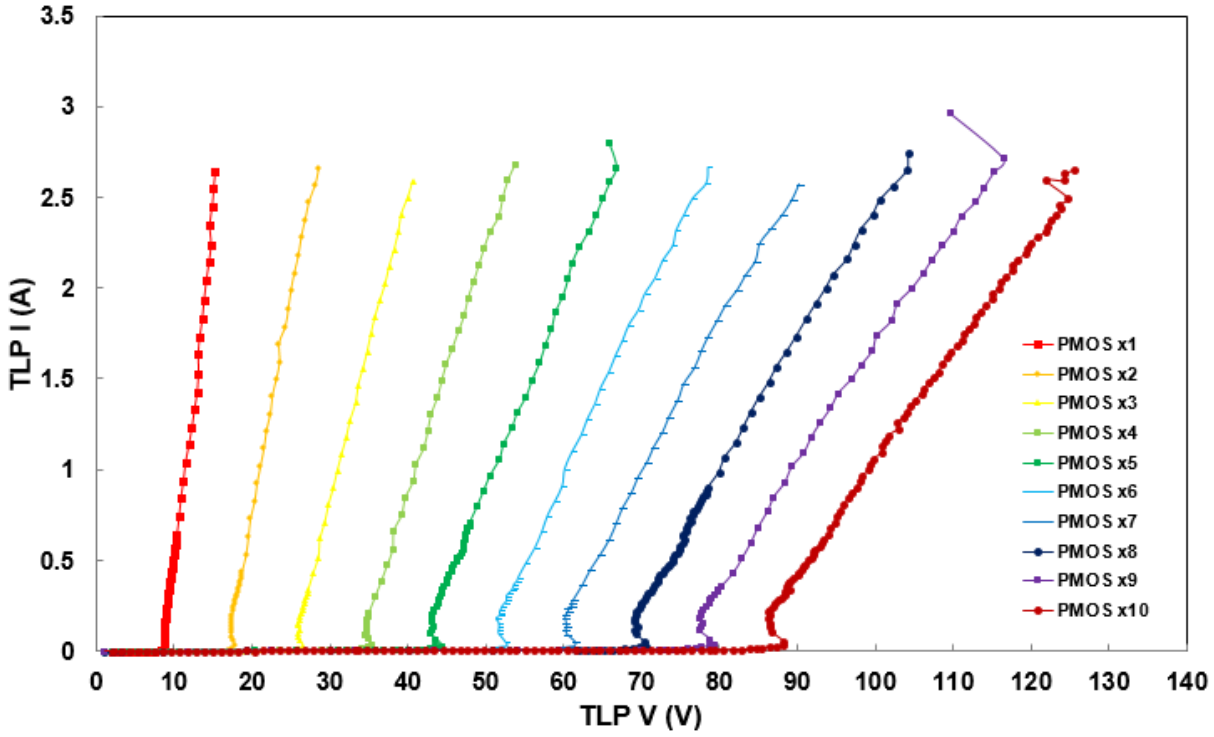


Fig. 2.13 The TLP-measured I-V characteristics of typical stacked LV PMOSs

Table 2.7

The measurement data of typical stacked LV PMOSs

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	8.81	8.67	2.55	8.2	4.5	300
2 units	17.74	17.25	2.57	16.3	4.5	300
3 units	26.54	25.82	2.49	24.4	4.5	300
4 units	35.41	34.54	2.6	32.6	5	350
5 units	44.34	42.92	2.66	40.7	5	350
6 units	52.79	51.36	2.58	48.8	5	400
7 units	61.49	60.21	2.49	57	5	400
8 units	70.56	69.15	2.65	65.2	5	400
9 units	79.37	77.43	2.72	73.2	5	450
10 units	88.23	86.26	2.63	81.6	5	450

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

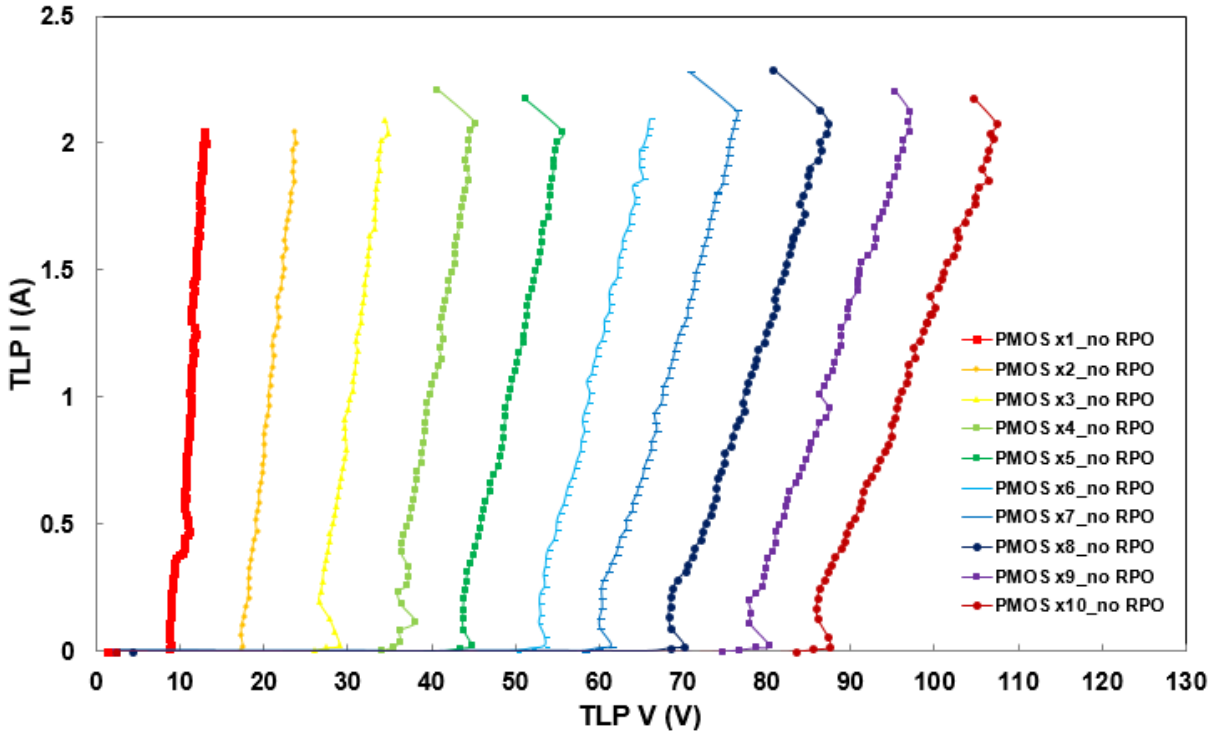


Fig. 2.14 The TLP-measured I-V characteristics of full silicide (no RPO) stacked LV PMOSs

Table 2.8

The measurement data of full silicide (no RPO) stacked LV PMOSs

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	8.99	8.66	2.02	8.2	4	200
2 units	17.49	17.36	2	16.4	4	250
3 units	29.01	26.58	2.04	24.6	4	250
4 units	36.3	35.96	2.08	32.8	4	250
5 units	44.76	43.84	2.05	41	4	300
6 units	53.53	52.86	2.06	49	4	300
7 units	61.49	60.17	2.13	57.2	4	300
8 units	70.11	68.24	2.13	65.4	4	300
9 units	80.27	77.83	2.12	74	4	350
10 units	87.46	85.95	2.08	81.8	4	350

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

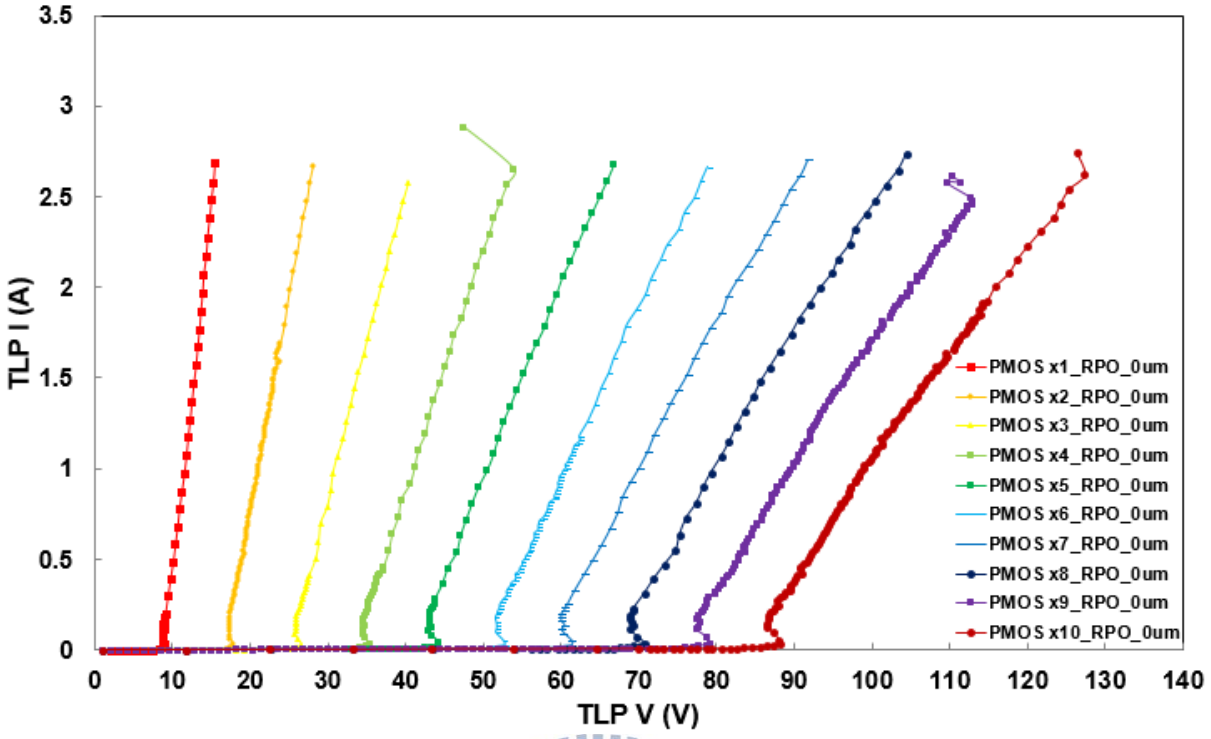


Fig. 2.15 The TLP-measured I-V characteristics of silicide blocking (RPO_0μm) stacked LV PMOSs

Table 2.9

The measurement data of silicide blocking (RPO_0μm) stacked LV PMOSs

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	8.85	8.73	2.58	8.2	4.5	300
2 units	17.69	17.23	2.58	16.3	5	300
3 units	26.63	25.77	2.48	24.4	4.5	350
4 units	35.29	34.46	2.66	32.6	4.5	350
5 units	44.08	42.93	2.59	40.7	5	350
6 units	52.77	51.52	2.58	48.8	5	400
7 units	61.41	60.01	2.62	57	5	400
8 units	70.75	68.8	2.64	65	5	400
9 units	79.23	77.36	2.46	73.2	5	450
10 units	88.21	86.43	2.46	81.4	5	450

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

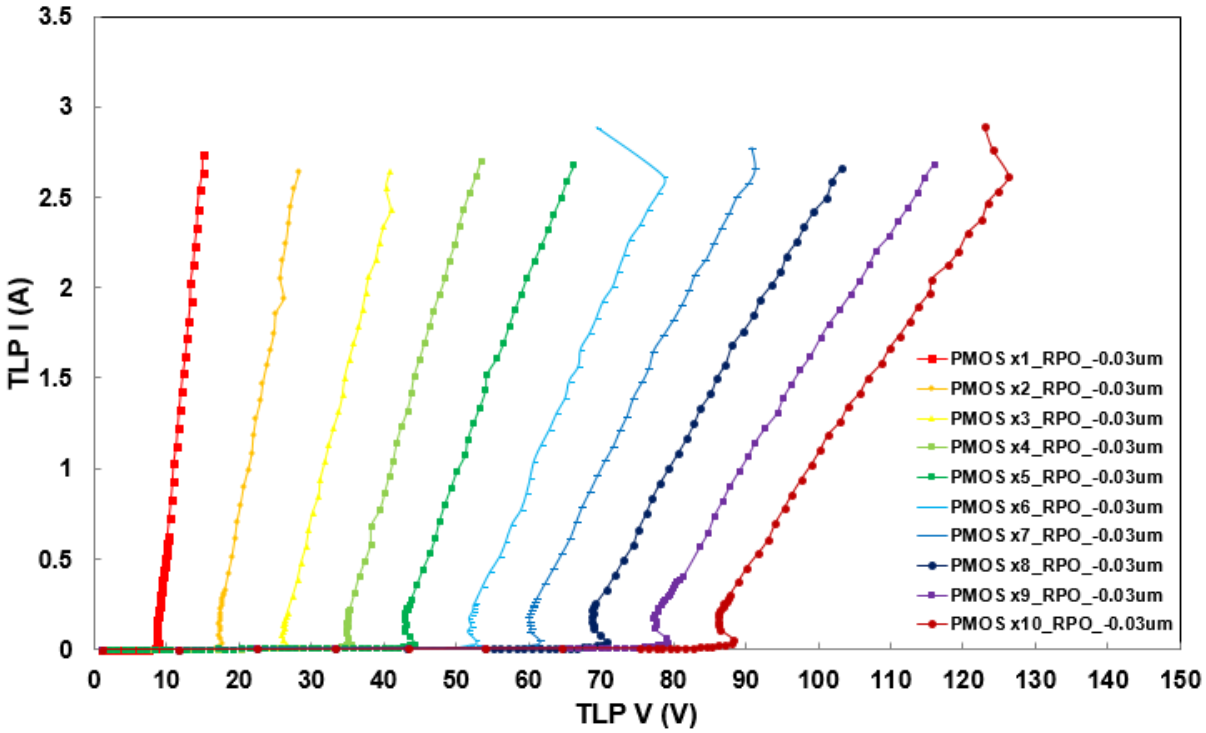


Fig. 2.16 The TLP-measured I-V characteristics of silicide blocking (RPO_-0.03μm) stacked LV PMOSs

Table 2.10

The measurement data of silicide blocking (RPO_-0.03μm) stacked LV PMOSs

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	8.81	8.62	2.63	8.2	4.5	300
2 units	17.68	17.2	2.55	16.3	4.5	300
3 units	26.55	26	2.55	24.4	5	350
4 units	35.6	34.82	2.61	32.6	4.5	350
5 units	44.42	42.92	2.58	40.7	4.5	350
6 units	52.81	51.64	2.62	48.8	5	400
7 units	61.54	60.07	2.66	57	5	400
8 units	70.68	68.61	2.59	65.2	5	400
9 units	79.4	77.25	2.61	73.2	5	450
10 units	88.25	86.12	2.76	81.4	5	450

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

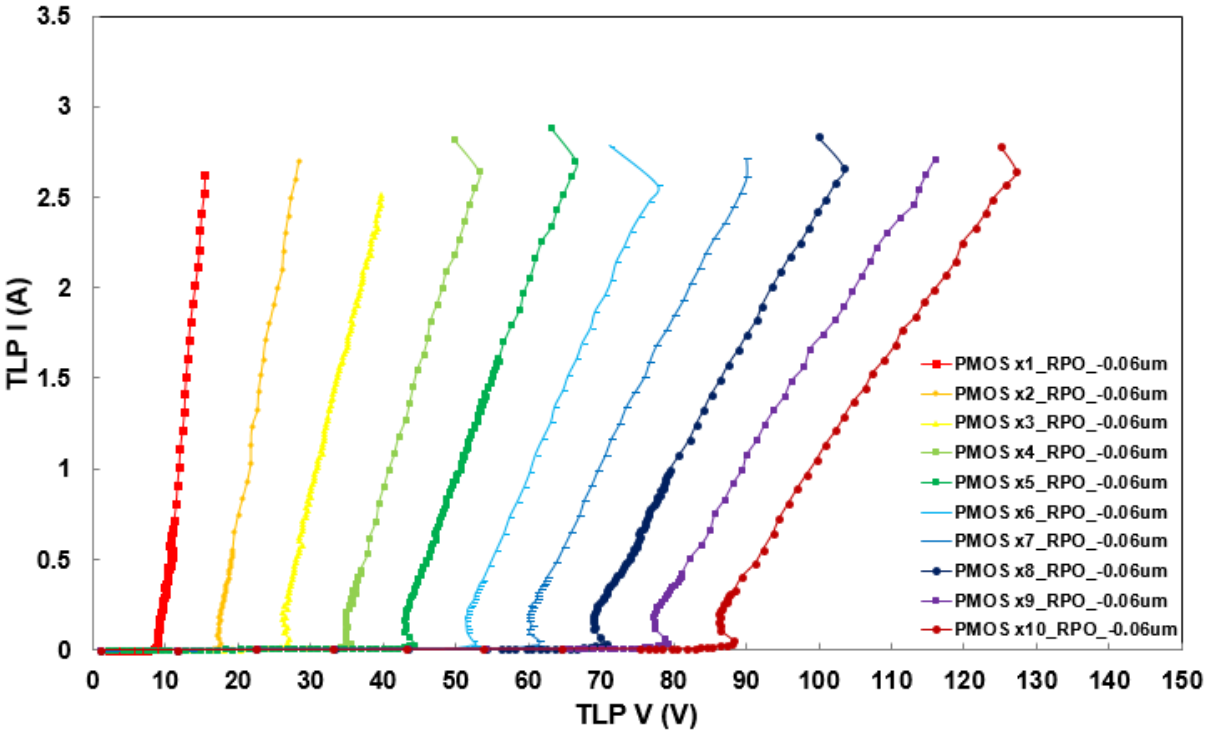


Fig. 2.17 The TLP-measured I-V characteristics of silicide blocking (RPO_-0.06μm) stacked LV PMOSs

Table 2.11

The measurement data of silicide blocking (RPO_-0.06μm) stacked LV PMOSs

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	8.89	8.81	2.52	8.2	4.5	300
2 units	17.74	17.27	2.59	16.3	4.5	300
3 units	27.17	26.07	2.49	24.4	4.5	350
4 units	35.48	34.83	2.64	32.5	4.5	350
5 units	44.35	42.97	2.7	40.7	5	350
6 units	52.9	51.42	2.57	48.8	5	400
7 units	61.58	60.17	2.62	57	5	400
8 units	70.67	68.91	2.67	65	5	450
9 units	79.26	77.3	2.62	73.2	5	450
10 units	88.21	86.08	2.64	81.4	5	450

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

All of silicide blocking stacked LV PMOSs can pass 4.5 kV in the human-body-model (HBM) ESD test and 300 V in the machine-model (MM) ESD test. Three silicide blocking devices have almost similar I_{t2} and ESD robustness. The ESD robustness of stacked PMOS devices with silicide blocking on drain side are better than stacked PMOS devices with full silicide in the TLP test.

The TLP measured I-V characteristics of stacked LV PMOSs with different drain contact to poly-gate edge (d1) are shown in Fig. 2.18, Fig. 2.19. The spacings of d1 are 4μm and 6μm. The detailed characteristics of stacked LV PMOSs with different drain contact to poly-gate edge (d1) are listed in Table 2.12 and Table 2.13.

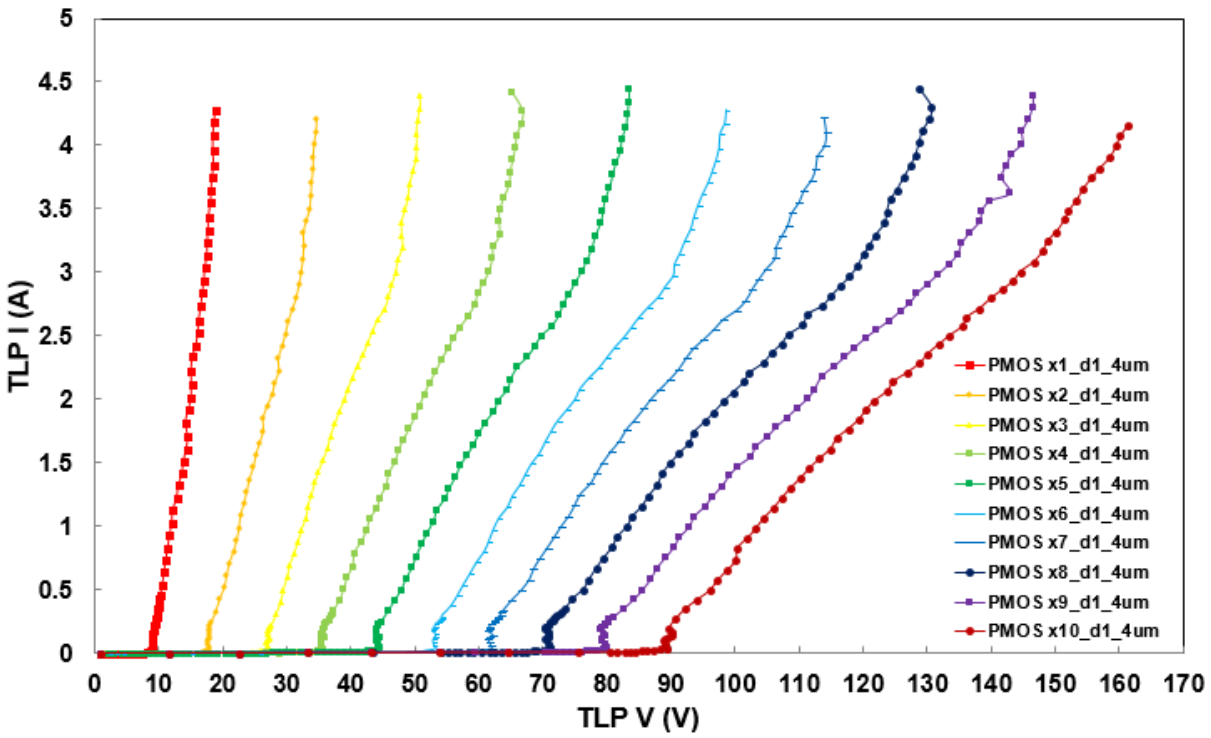


Fig. 2.18 The TLP-measured I-V characteristics of stacked LV PMOSs with d1 4μm

All of stacked LV PMOSs with d1 4μm can pass 7 kV in the human-body-model (HBM) ESD test and 450 V in the machine-model (MM) ESD test. The ESD robustness of stacked LV PMOSs with d1 4μm are better than typical stacked PMOS devices in the TLP test.

Table 2.12

The measurement data of stacked LV PMOSs with d1 4μm

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	8.95	8.9	4.18	8.2	7	450
2 units	17.88	17.61	4.11	16.3	7.5	450
3 units	26.95	26.7	4.29	24.4	7.5	500
4 units	35.55	35.26	4.28	32.5	7	550
5 units	44.53	43.84	4.35	40.7	7.5	550
6 units	53.29	52.67	4.18	48.8	7.5	550
7 units	62.07	61.36	4.1	56.8	7.5	600
8 units	71.12	70.19	4.31	65	7.5	600
9 units	79.98	78.93	4.3	73.2	7.5	550
10 units	89.26	88.85	4.16	81.4	7.5	500

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

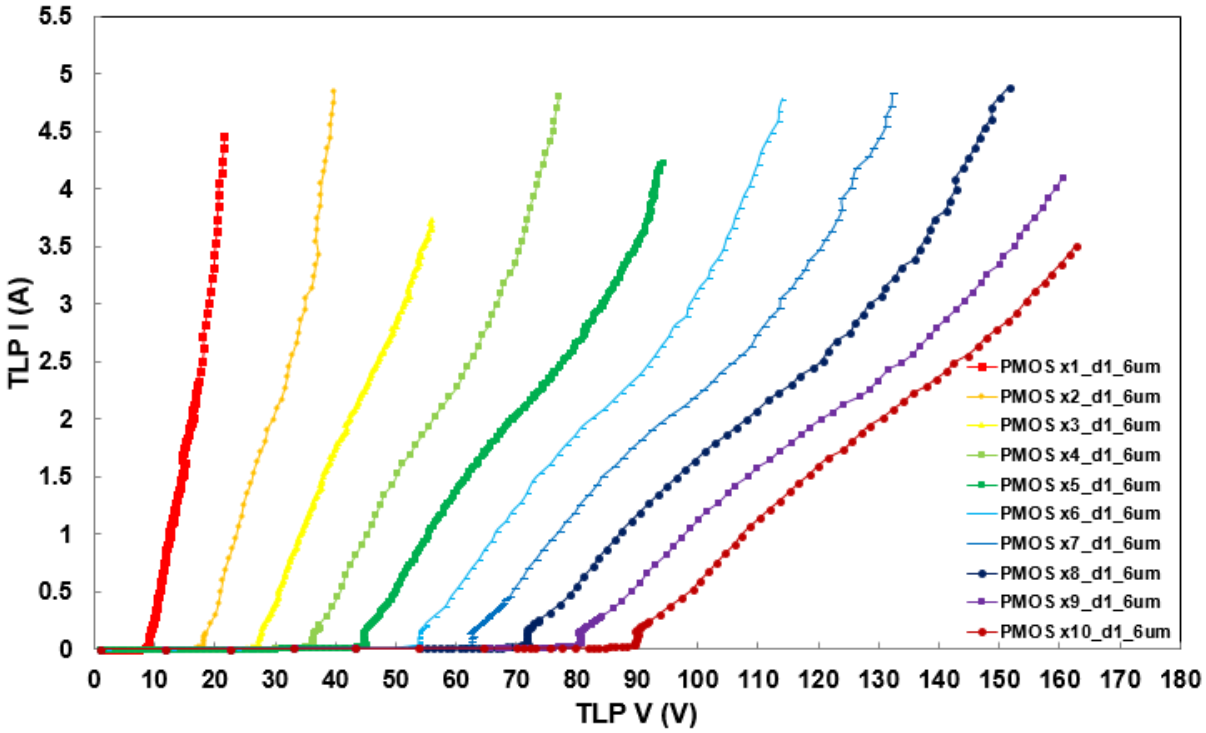


Fig. 2.19 The TLP-measured I-V characteristics of stacked LV PMOSs with d1 6μm

Table 2.13

The measurement data of stacked LV PMOSs with d1 6μm

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	9.05	9.04	4.35	8.2	>8	450
2 units	18.12	18.09	4.75	16.3	>8	500
3 units	27.35	27.29	3.71	24.4	>8	500
4 units	36.25	36.04	4.7	32.5	>8	550
5 units	45.06	44.67	4.2	40.7	>8	550
6 units	53.69	53.62	4.68	48.8	>8	600
7 units	62.94	62.38	4.72	57	>8	550
8 units	71.89	71.61	4.79	65	>8	550
9 units	80.81	80.38	4.1	73.2	7	450
10 units	90.11	89.68	3.5	81.4	6	400

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

All of stacked LV PMOSs with d1 6μm can pass 6 kV in the human-body-model (HBM) ESD test and 400 V in the machine-model (MM) ESD test.

The TLP measured I-V characteristics of stacked LV PMOSs with different drain contact number (co) effect are shown in Fig. 2.20. The number of drain contact number (co) is 4. The detailed characteristics of stacked LV PMOSs with different drain contact number effect are listed in Table 2.14. All of stacked LV PMOSs with drain contact number 4 can pass 5 kV in the human-body-model (HBM) ESD test and 350 V in the machine-model (MM) ESD test.

Furthermore, to get good ESD robustness, d1 effect and drain contact number effect are considered simultaneously. The TLP measured I-V characteristics of stacked LV PMOSs with different d1 and drain contact number are shown in Fig. 2.21 and Fig. 2.22. The detailed characteristics of stacked LV PMOSs with different d1 and drain contact number are listed in Table 2.15 and Table 2.16.

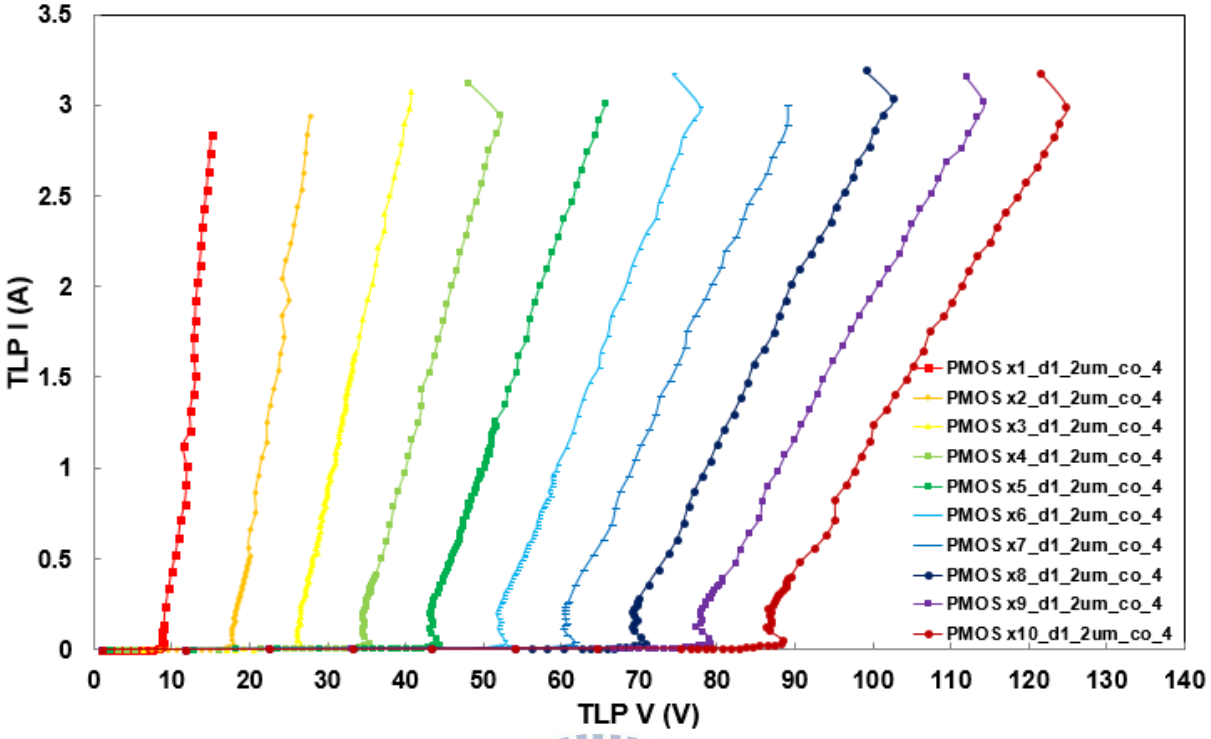


Fig. 2.20 The TLP-measured I-V characteristics of stacked LV PMOSs with drain contact number 4

Table 2.14

The measurement data of stacked LV PMOSs with drain contact number 4

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	8.83	8.71	2.74	8.2	5	350
2 units	17.9	17.65	2.84	16.3	5.5	350
3 units	26.57	26.09	2.98	24.4	5.5	350
4 units	35.39	34.4	2.94	32.5	5.5	400
5 units	44.33	43.09	2.92	40.6	5.5	400
6 units	52.86	51.58	3	48.8	5.5	450
7 units	61.66	60.21	2.89	57	5.5	450
8 units	70.79	69.1	3.04	65	5.5	450
9 units	79.23	77.25	3.02	73.2	5.5	500
10 units	88.32	86.32	3	81.4	5.5	500

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

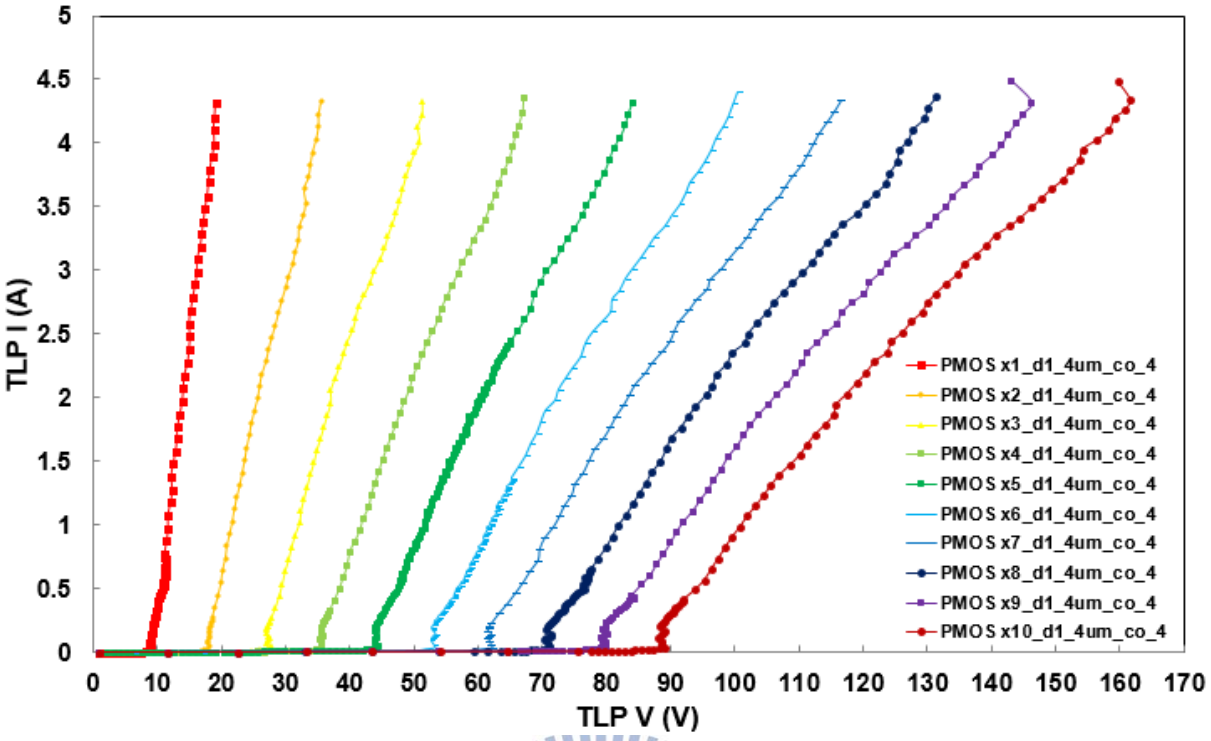


Fig. 2.21 The TLP-measured I-V characteristics of stacked LV PMOSs with d1 4μm and drain contact number 4

Table 2.15

The measurement data of stacked LV PMOSs with d1 4μm and drain contact number 4

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	9	8.89	4.2	8.2	7.5	500
2 units	18.14	17.97	4.22	16.3	7.5	500
3 units	27.67	26.97	4.22	24.4	7.5	550
4 units	35.69	35.3	4.24	32.5	7.5	550
5 units	44.56	43.86	4.23	40.6	7.5	600
6 units	53.35	52.68	4.31	48.8	7.5	600
7 units	62.18	61.41	4.25	57	>8	600
8 units	71.06	70.36	4.28	65	>8	650
9 units	79.97	79.21	4.32	73.2	>8	600
10 units	89.04	87.96	4.35	81.4	>8	550

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

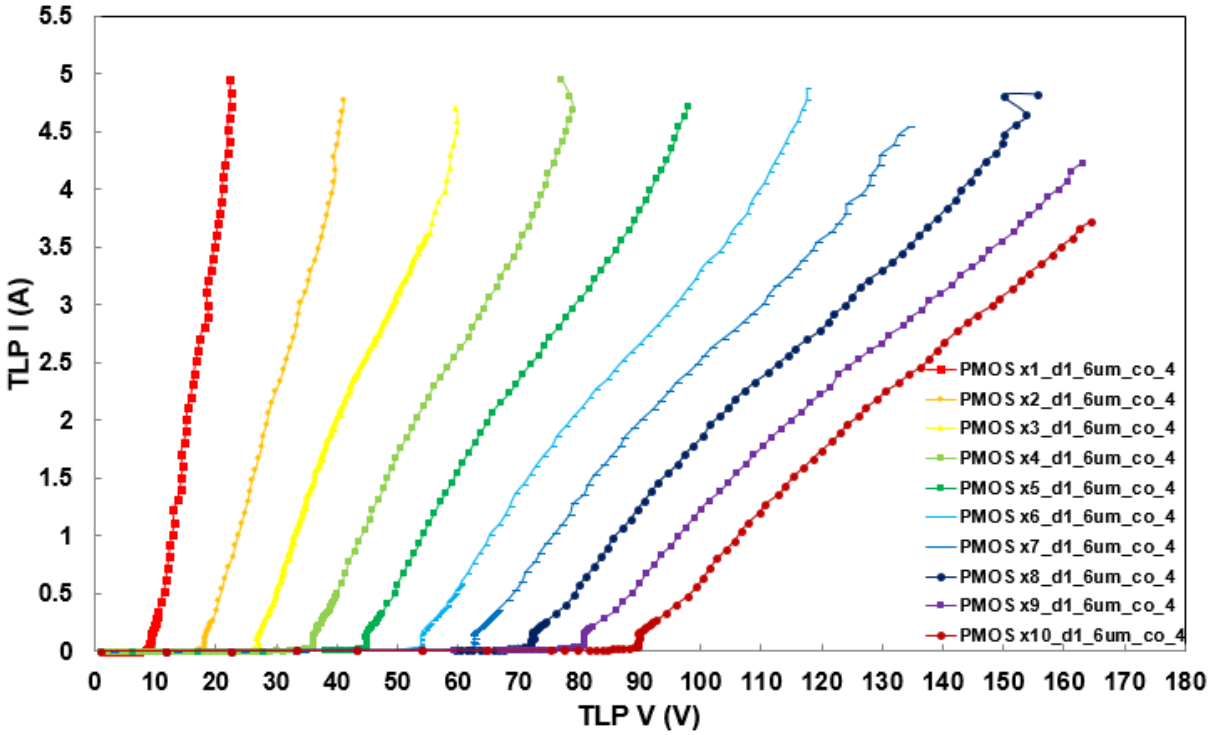


Fig. 2.22 The TLP-measured I-V characteristics of stacked LV PMOSs with d1 6μm and drain contact number 4

Table 2.16

The measurement data of stacked LV PMOSs with d1 6μm and drain contact number 4

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	9.09	8.94	4.83	8.2	>8	450
2 units	18.16	18.1	4.68	16.3	>8	500
3 units	27.27	26.74	4.59	24.4	>8	500
4 units	36.15	36.07	4.81	32.5	>8	550
5 units	44.97	44.68	4.62	40.7	>8	550
6 units	53.84	53.73	4.77	48.8	>8	600
7 units	62.9	62.52	4.47	57	>8	650
8 units	72.57	72.12	4.81	65	>8	550
9 units	80.85	80.68	4.23	73.2	7.5	500
10 units	89.74	89.56	3.66	81.4	6.5	450

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

All of stacked LV PMOSs with d1 4μm and drain contact number 4 can pass 7.5 kV in the human-body-model (HBM) ESD test and 500 V in the machine-model (MM) ESD test. All of stacked LV PMOSs with d1 6μm and drain contact number 4 can pass 6.5 kV in the human-body-model (HBM) ESD test and 450 V in the machine-model (MM) ESD test. From the above experiments, d1 effect and drain contact number effect of stacked LV PMOSs can get good ESD robustness.

The TLP measured I-V characteristics of stacked LV PMOSs with channel length effect are shown in Fig. 2.23. The channel length of stacked LV PMOSs is 1μm. The detailed characteristics of stacked LV PMOSs with channel length effect are listed in Table 2.17. All of stacked LV PMOSs with channel length 1μm can pass 5 kV in the human-body-model (HBM) ESD test and 350 V in the machine-model (MM) ESD test.

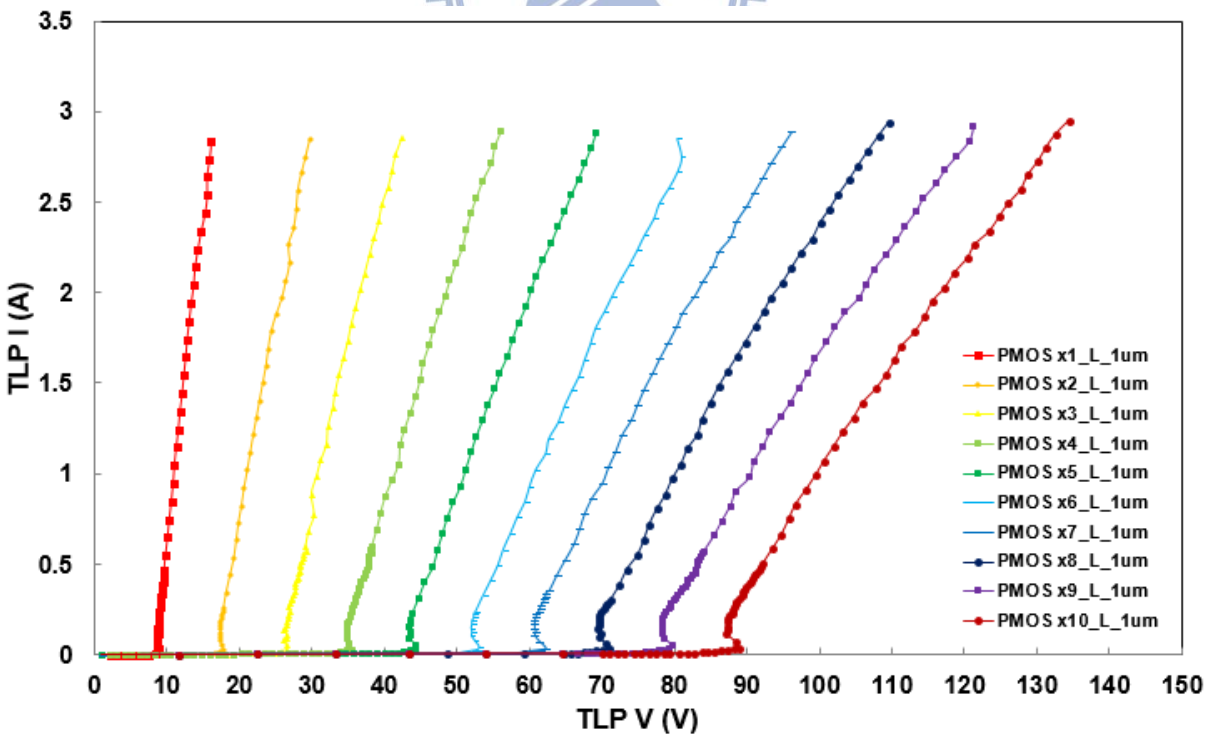


Fig. 2.23 The TLP-measured I-V characteristics of stacked LV PMOSs with channel length 1μm

Table 2.17

The measurement data of stacked LV PMOSs with channel length 1μm

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	8.86	8.72	2.74	8.2	5	350
2 units	17.84	17.4	2.75	16.3	5	350
3 units	26.6	26.23	2.76	24.4	5	350
4 units	35.49	34.8	2.8	32.5	5	400
5 units	44.42	43.47	2.8	40.7	5	400
6 units	53.09	52	2.75	48.8	5.5	450
7 units	62.28	60.72	2.81	57	5	450
8 units	70.91	69.51	2.87	65	5.5	450
9 units	79.71	78.28	2.92	73.2	5.5	500
10 units	88.89	87.19	2.95	81.4	5.5	500

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The TLP measured I-V characteristics of stacked LV PMOSs with total width effect are shown in Fig. 2.24. The total width of stacked LV PMOSs is 600μm, and the single finger width of stacked LV PMOSs is 50μm. The total width of typical stacked LV PMOSs is 360μm, and the single finger width of typical stacked LV PMOSs is 30μm. The detailed characteristics of stacked LV PMOSs with total width 600μm are listed in Table 2.18. All of stacked LV PMOSs with total width 600μm can pass 8 kV in the human-body-model (HBM) ESD test and 500 V in the machine-model (MM) ESD test.

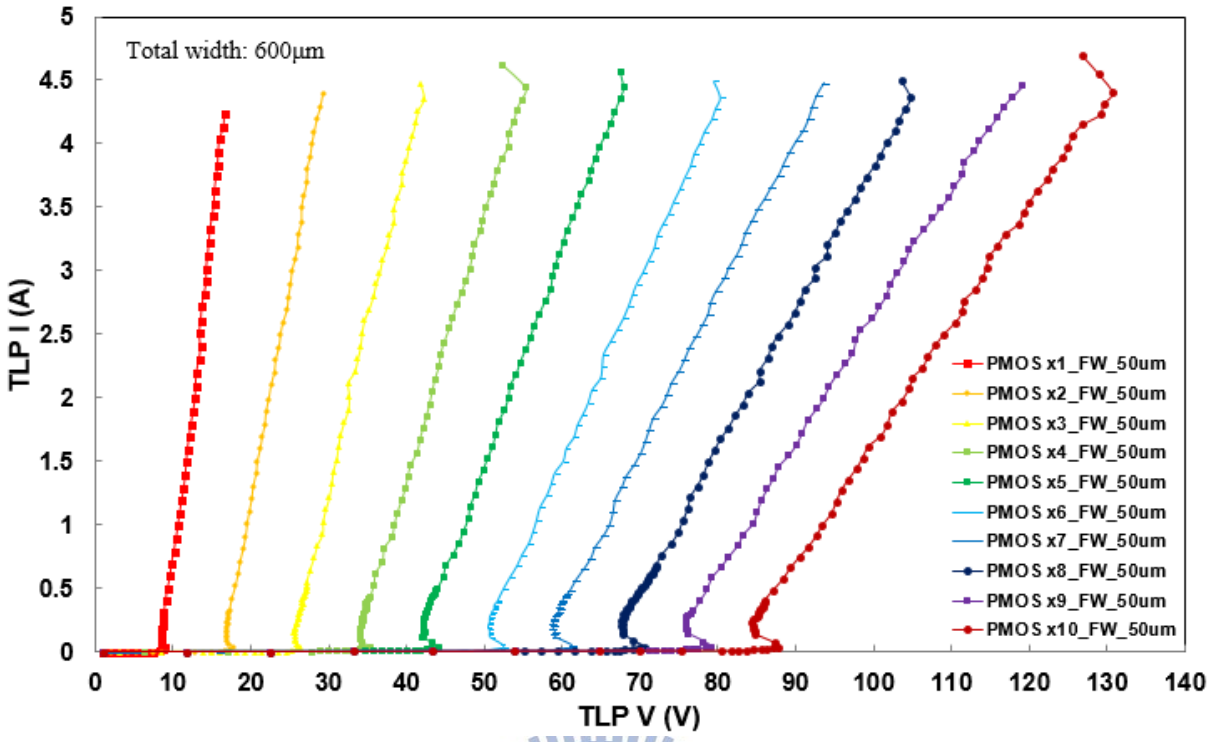


Fig. 2.24 The TLP-measured I-V characteristics of stacked LV PMOSs with total width 600μm and the single finger width 50μm

Table 2.18

The measurement data of stacked LV PMOSs with total width 600μm and the single finger width 50μm

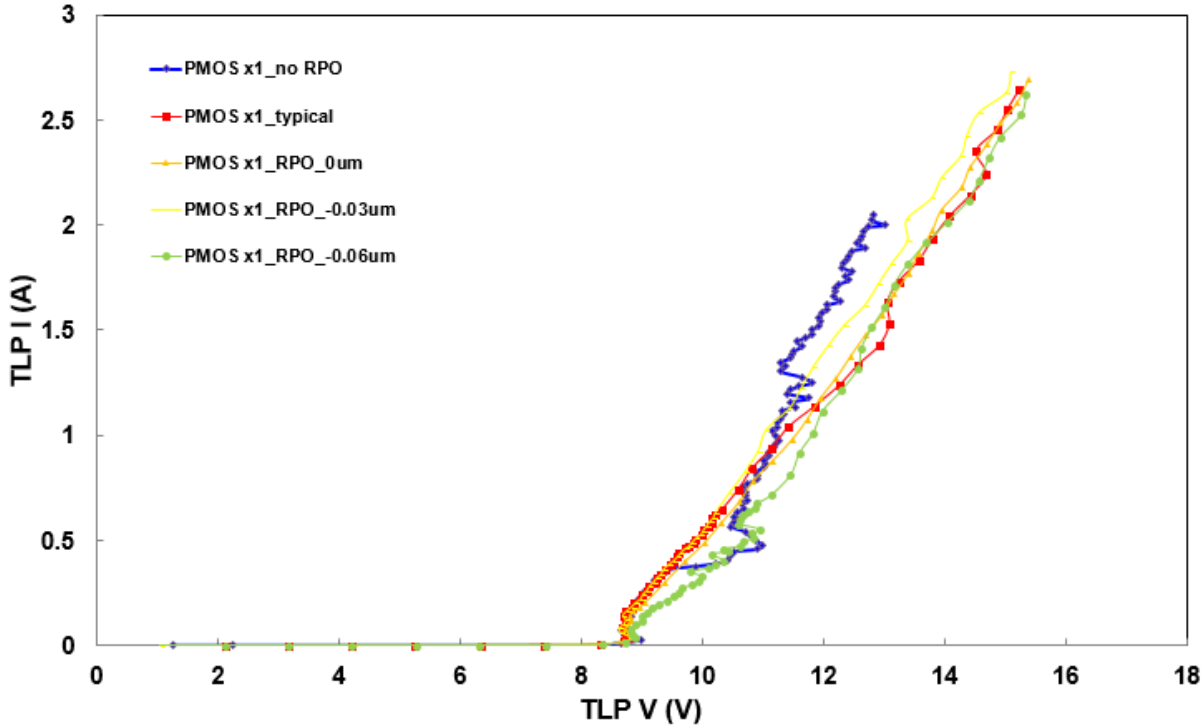
	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	8.89	8.46	4.13	8.2	>8	500
2 units	17.73	16.9	4.28	16.3	>8	500
3 units	26.44	25.56	4.36	24.4	>8	500
4 units	35.31	34.02	4.44	32.5	>8	550
5 units	44.17	42.08	4.44	40.6	>8	550
6 units	52.54	50.48	4.37	48.8	>8	600
7 units	61.28	58.85	4.38	57	>8	600
8 units	70.57	67.54	4.37	65	>8	650
9 units	79.16	75.89	4.37	73.2	>8	650
10 units	87.86	84.32	4.55	81.4	>8	700

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

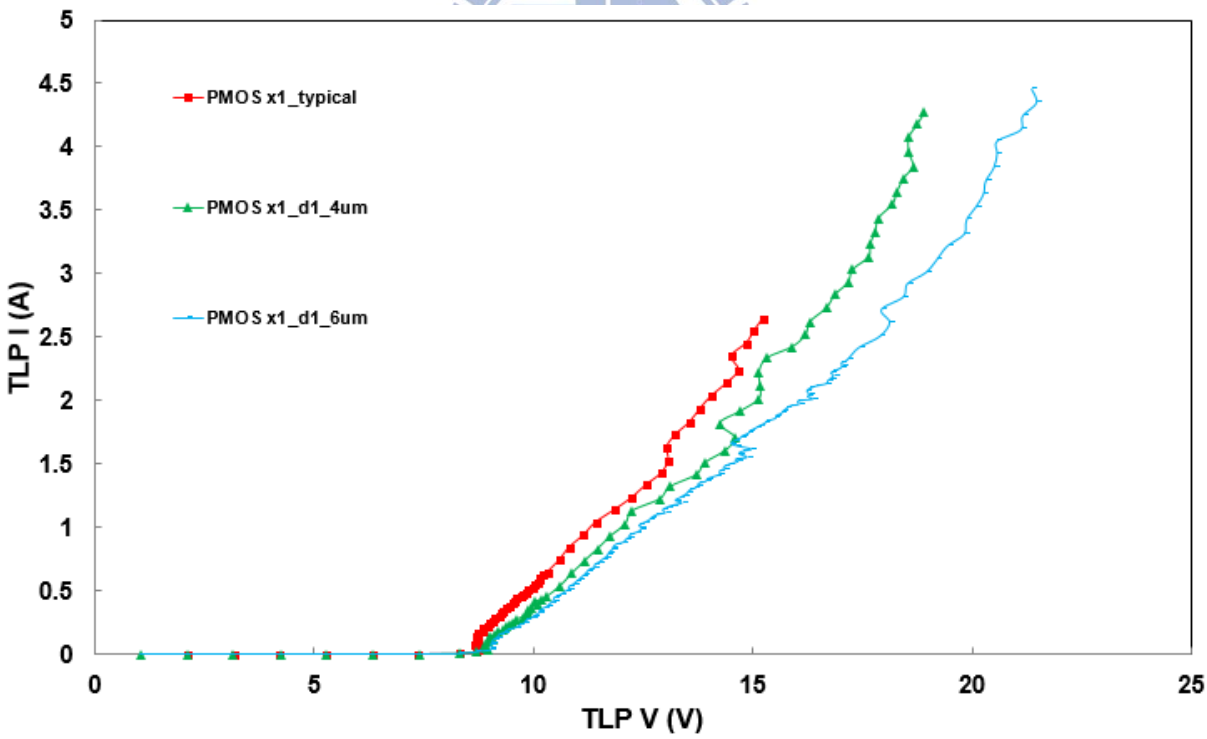
2.2.4 Discussion

From the above experiments, ESD robustness of stacked LV PMOSs with different layout parameters are better than those of typical ones. Therefore, the trigger voltage and the holding voltage of stacked configuration can be adjusted to meet different HV applications. Stacking numbers of the stacked LV PMOSs were fabricated and verified from one to ten for different HV applications. Layout parameters were investigated to study its impact on ESD protection performance from stacking number one to ten, respectively. There are RPO, drain contact to poly-gate edge (d1), drain contact number (co), channel length (L), and total width effect.

The TLP measured I-V curves of LV PMOS with different RPO splits (typical_0.3μm, 0μm, -0.03μm, -0.06μm, and no RPO) are compared in Fig. 2.25(a). The TLP measured I-V curves of LV PMOS with different d1 splits (typical_2μm, 4μm, and 6μm) are compared in Fig. 2.25(b). The TLP measured I-V curves of LV PMOS with different d1 and drain contact number splits (typical_d1_2μm_co_2, d1_2μm_co_4, d1_4μm_co_4, and d1_6μm_co_4) are compared in Fig. 2.25(c). The TLP measured I-V curves of LV PMOS with different L splits (typical_0.8μm and 1μm) are compared in Fig. 2.25(d). The TLP measured I-V curves of LV PMOS with different total width (TW) splits (typical_360μm and 600μm) are compared in Fig. 2.25(e). The total width of LV PMOS is 600μm, and the single finger width of LV PMOS is 50μm. The total width of LV PMOS is 360μm, and the single finger width of typical LV PMOS is 30μm. The detailed characteristics of LV PMOS with different layout parameters are listed in Table 2.19.

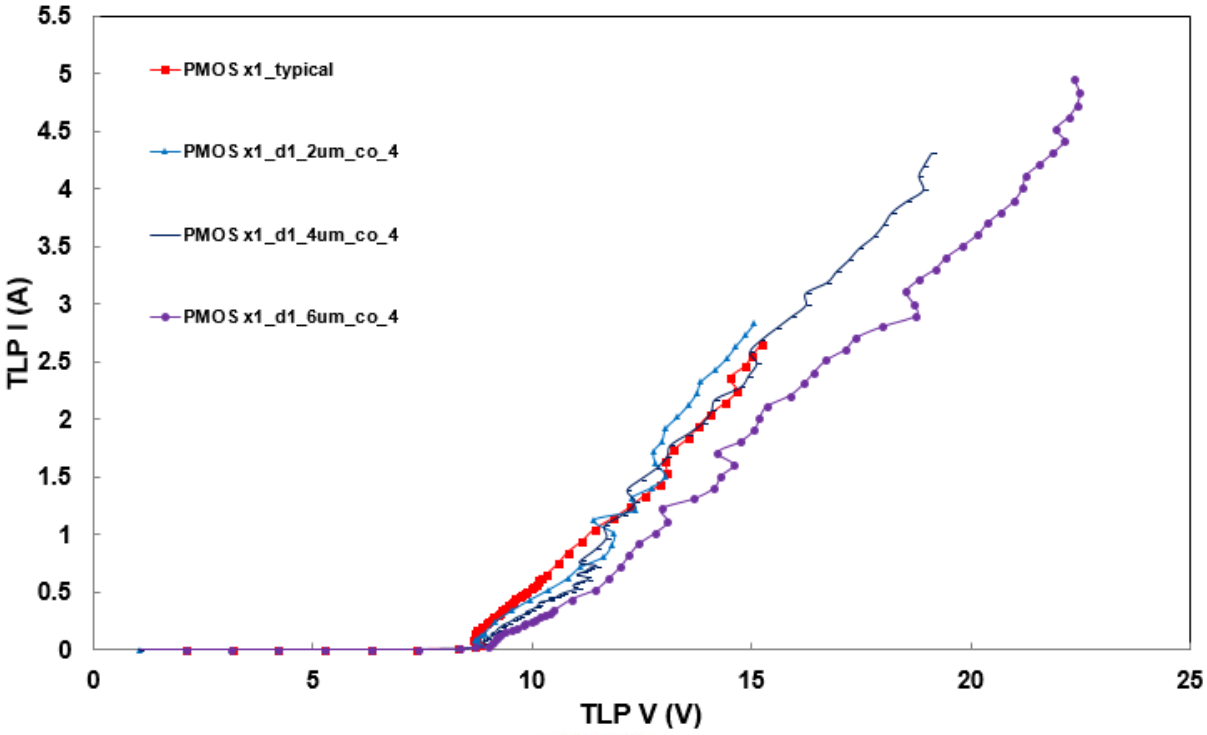


(a)

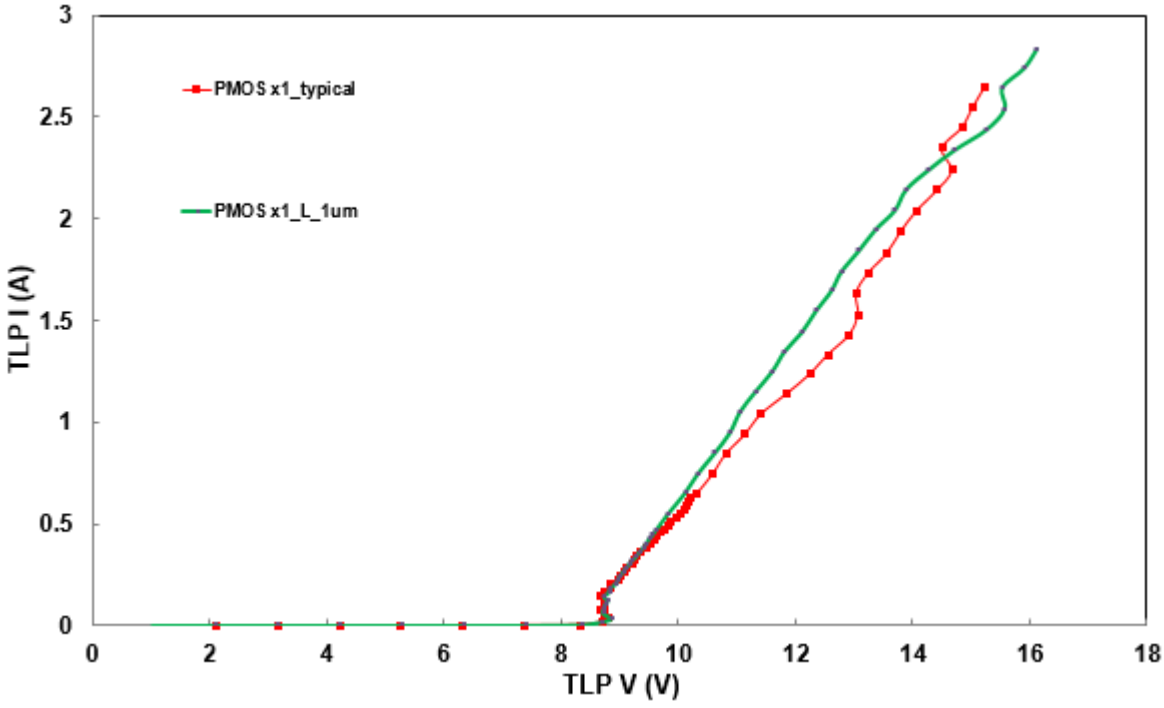


(b)

Fig. 2.25 The TLP measured I-V curves of LV PMOS with different (a) RPO splits and (b) d1 splits

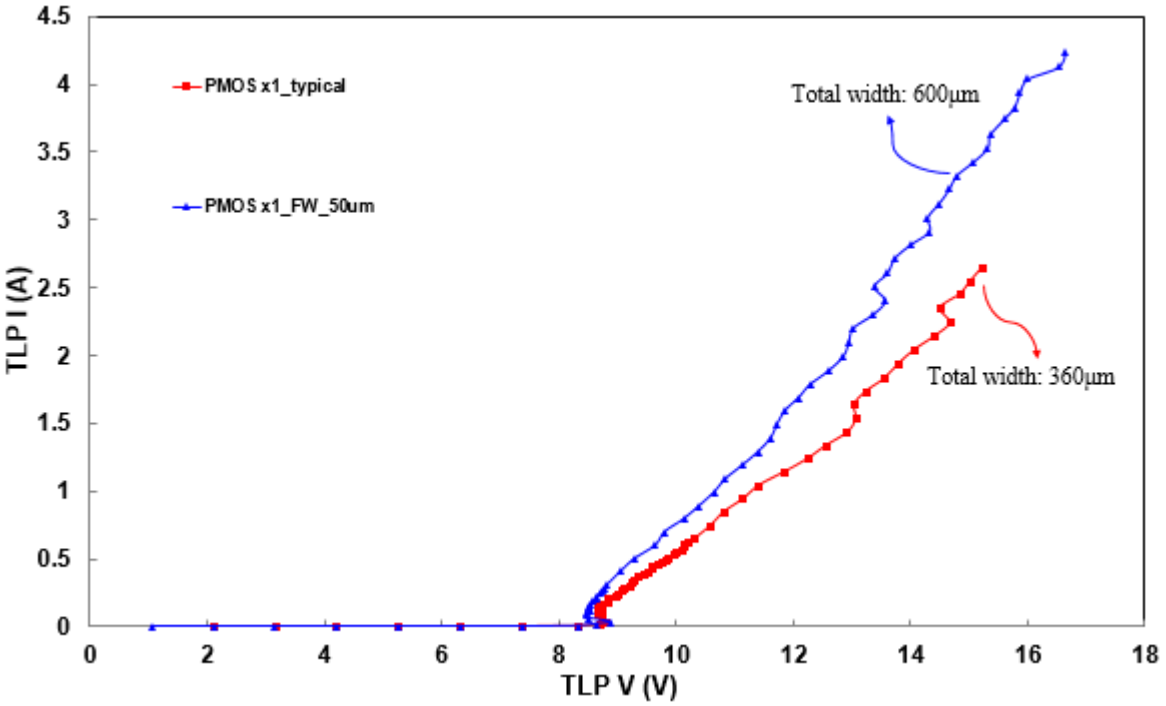


(c)



(d)

Fig. 2.25 The TLP measured I-V curves of LV PMOS with different (c) d1 and drain contact number (co) splits and (d) L splits



(e)

Fig. 2.25 The TLP measured I-V curves of LV PMOS with different (e) total width splits

Table 2.19

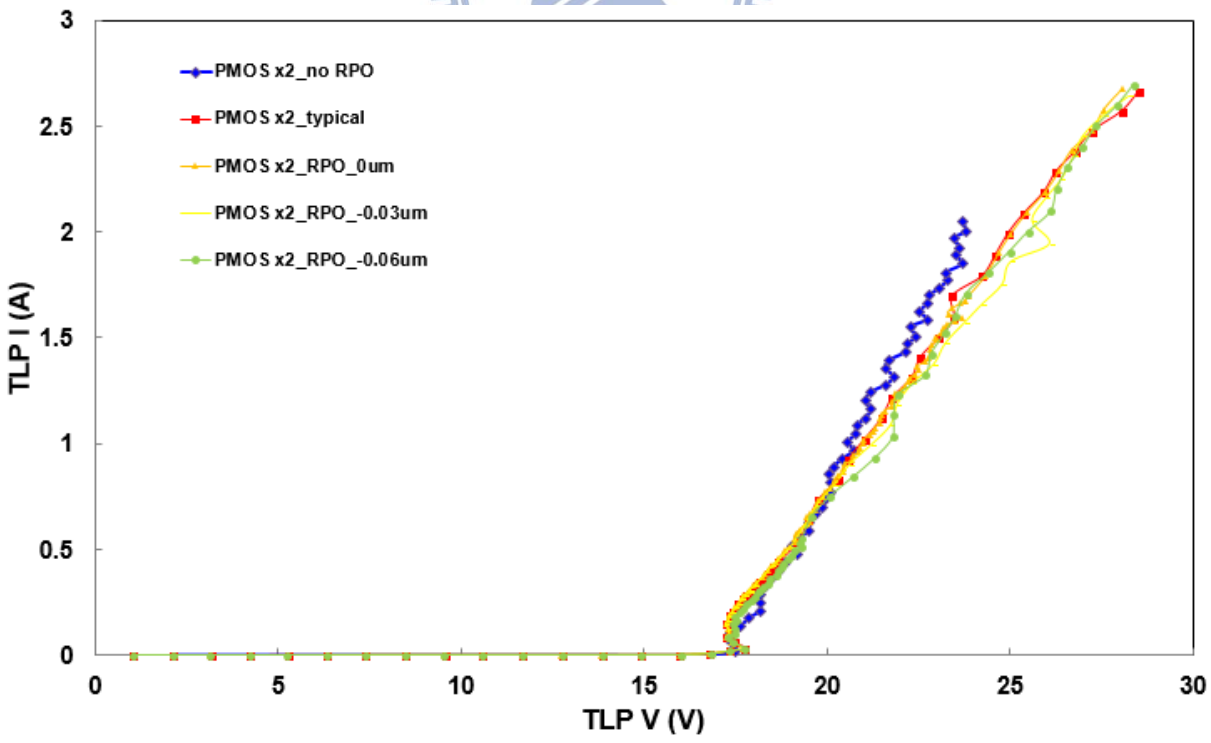
The measurement data of LV PMOS with different layout parameters

PMOS x1	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
typical	8.81	8.67	2.55	8.2	4.5	300
no_RPO	8.99	8.66	2.02	8.2	4	200
RPO_0μm	8.85	8.73	2.58	8.2	4.5	300
RPO_-0.03 μm	8.81	8.62	2.63	8.2	4.5	300
RPO_-0.06 μm	8.89	8.81	2.52	8.2	4.5	300
d1_4 μm	8.95	8.9	4.18	8.2	7	450
d1_6 μm	9.05	9.04	4.35	8.2	>8	450
d1_2 μm_co_4	8.83	8.71	2.74	8.2	5	350
d1_4 μm_co_4	9	8.89	4.2	8.2	7.5	500
d1_6 μm_co_4	9.09	8.94	4.83	8.2	>8	450
L_1 μm	8.86	8.72	2.74	8.2	5	350
TW_600 μm	8.89	8.46	4.13	8.2	>8	500

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

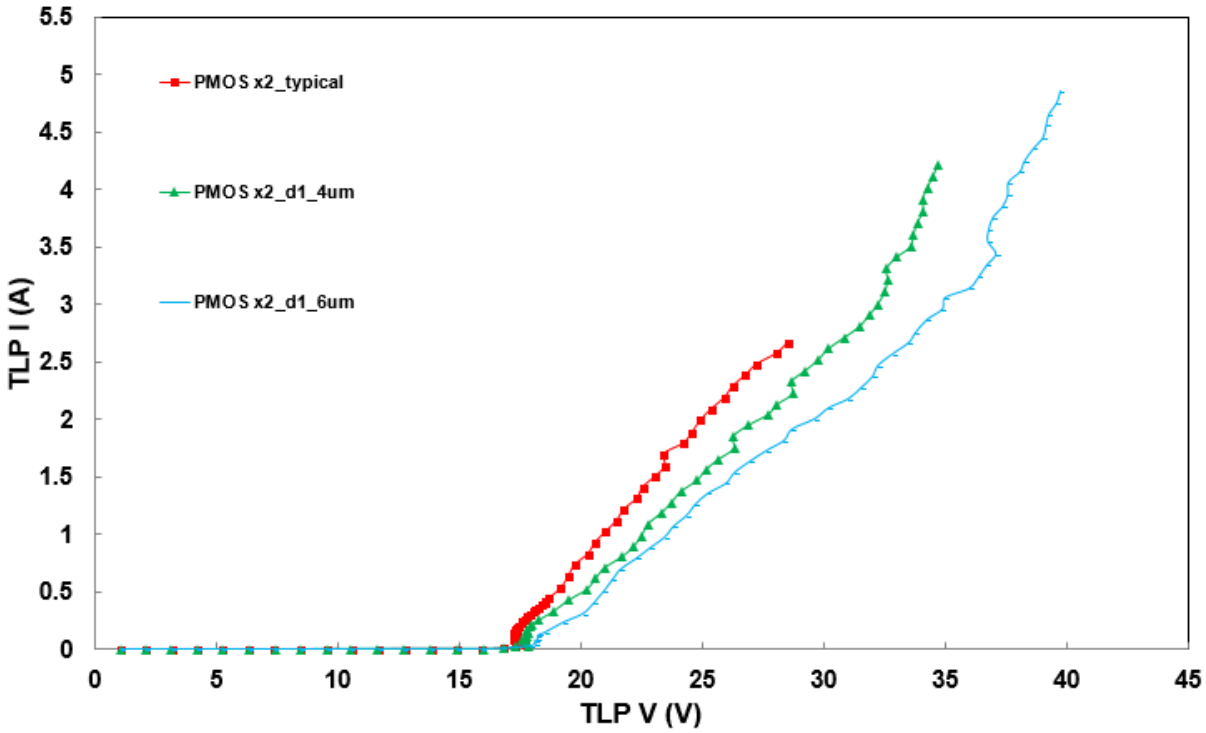
From the above experiments, the breakdown voltages of LV PMOS are almost the same in DC measurement. The holding voltages and the trigger voltages of LV PMOS are almost the same in TLP measurement. From above results with TLP-measured I_{t2} and ESD test, ESD robustness of LV PMOS with full silicide (no RPO) is bad. The LV PMOS with silicide blocking leads to a higher ESD robustness. Generally, the LV PMOS with a larger clearance drain contact to poly-gate edge, the more drain contact number, a wider channel width, a bigger total width leads to higher ESD robustness. LV PMOS with d1_6μm, d1_6μm_co_4, and TW_600μm can pass 8 kV in the human-body-model (HBM) ESD test and 450 V in the machine-model (MM) ESD test.

The TLP measured I-V curves of 2-PMOSs with different layout parameters splits (RPO, d1, drain contact number, L, and TW) are compared in Fig. 2.26(a) ~ (e). The detailed characteristics of 2-PMOSs with different layout parameters are listed in Table 2.20.

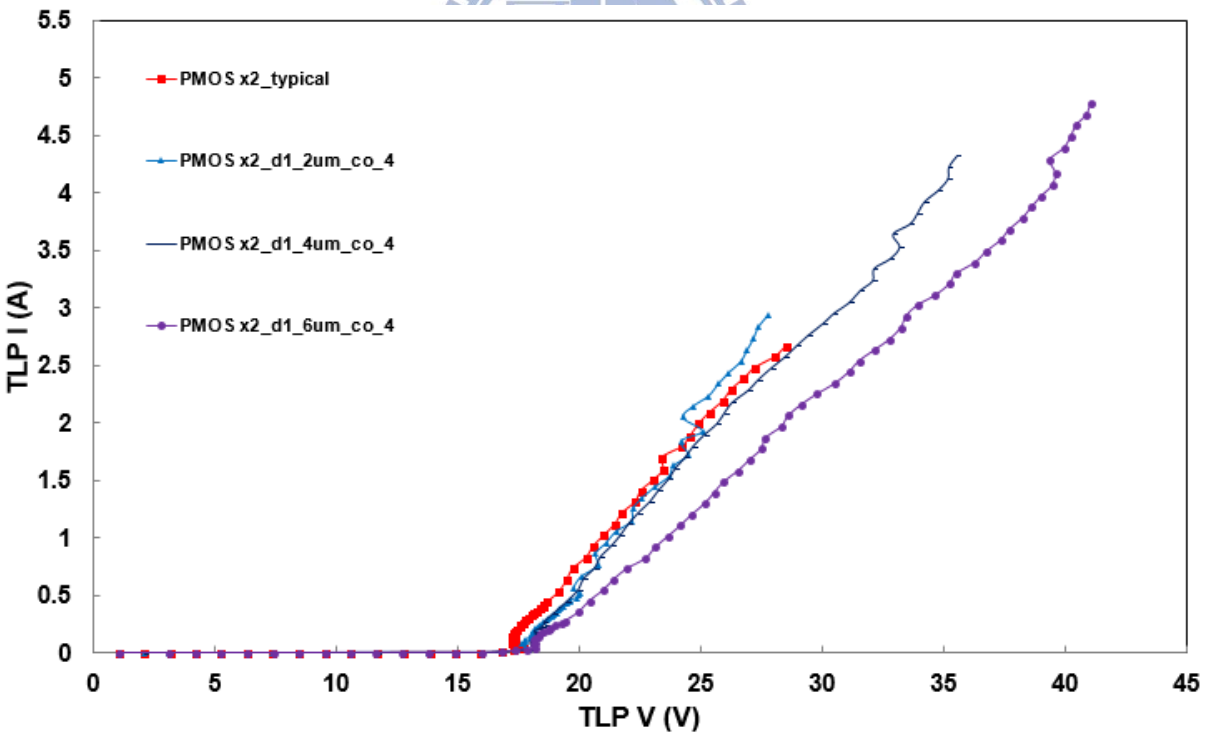


(a)

Fig. 2.26 The TLP measured I-V curves of 2-PMOSs with different (a) RPO splits

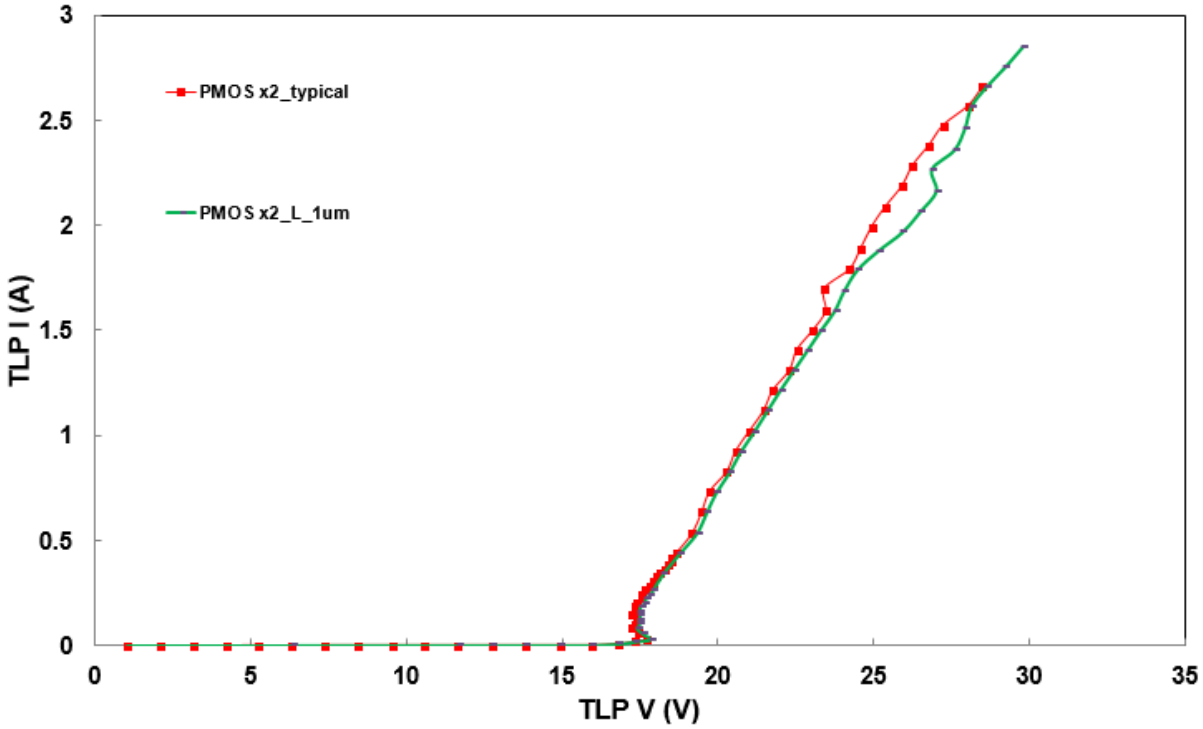


(b)

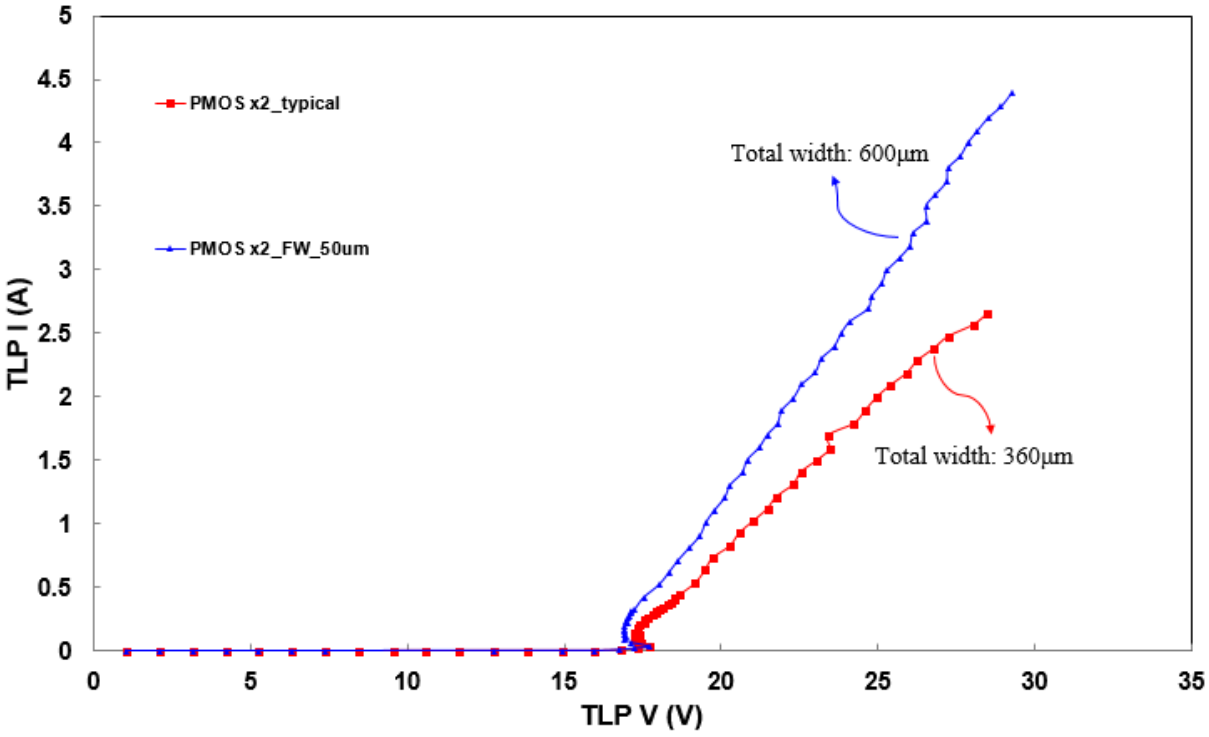


(c)

Fig. 2.26 The TLP measured I-V curves of 2-PMOSs with different (b) d1 splits and (c) d1 and drain contact number (co) splits



(d)



(e)

Fig. 2.26 The TLP measured I-V curves of 2-PMOSs with different (d) L splits and (e) total width splits

Table 2.20

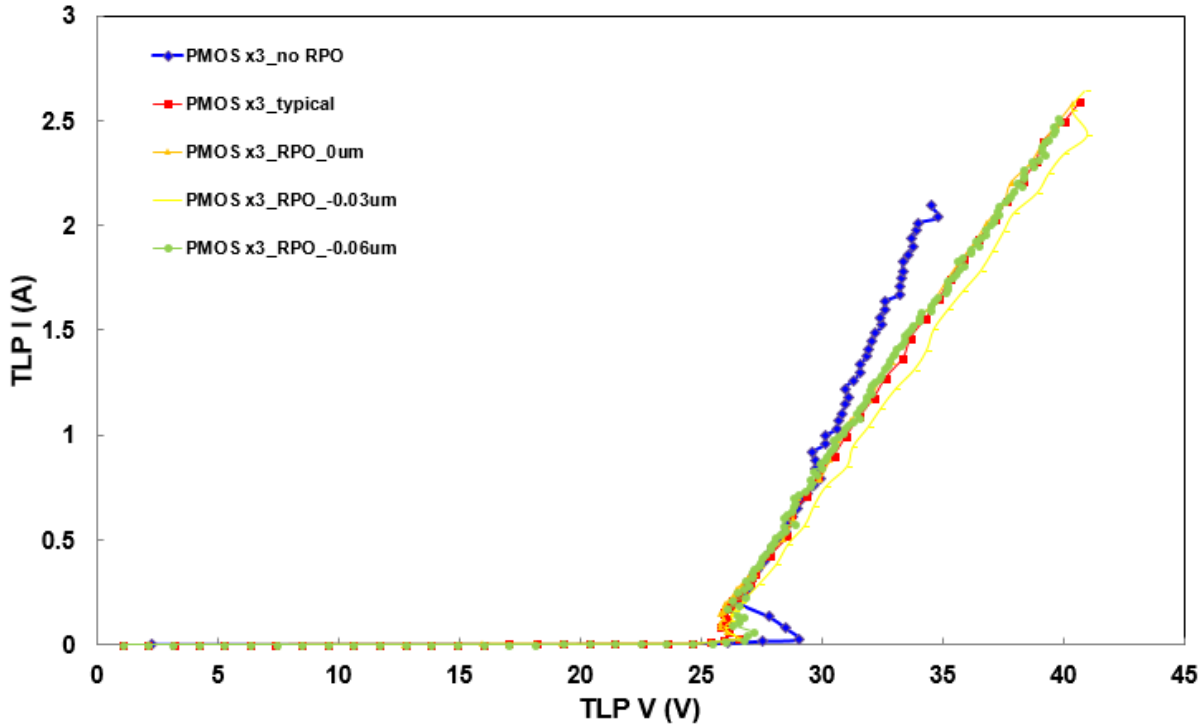
The measurement data of 2-PMOSs with different layout parameters

PMOS x2	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
typical	17.74	17.25	2.57	16.3	4.5	300
no_RPO	17.49	17.36	2	16.4	4	250
RPO_0μm	17.69	17.23	2.58	16.3	5	300
RPO_-0.03 μm	17.68	17.2	2.55	16.3	4.5	300
RPO_-0.06 μm	17.74	17.27	2.59	16.3	4.5	300
d1_4 μm	17.88	17.61	4.11	16.3	7.5	450
d1_6 μm	18.12	18.09	4.75	16.3	>8	500
d1_2 μm_co_4	17.9	17.65	2.84	16.3	5.5	350
d1_4 μm_co_4	18.14	17.97	4.22	16.3	7.5	500
d1_6 μm_co_4	18.16	18.1	4.68	16.3	>8	500
L_1 μm	17.84	17.4	2.75	16.3	5	350
TW_600 μm	17.73	16.9	4.28	16.3	>8	500

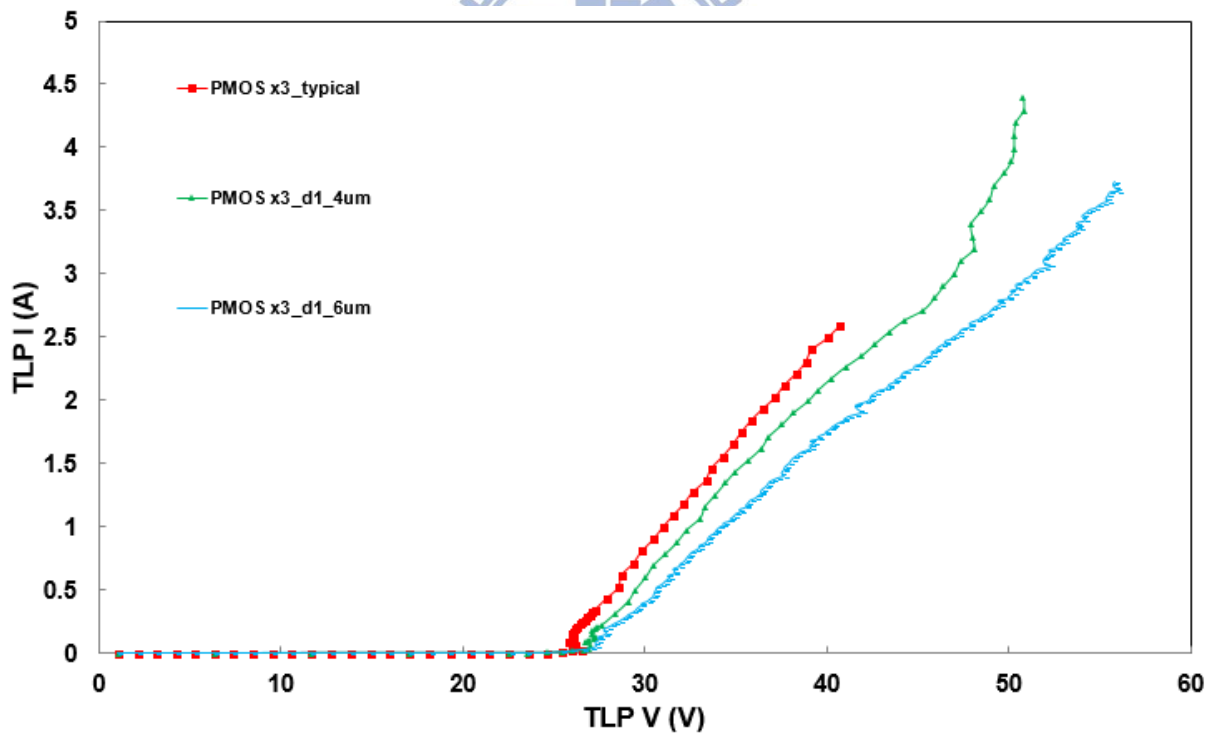
#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The breakdown voltages of 2-PMOSs stacked structure are also almost the same in DC measurement. The holding voltage of 2-PMOSs stacked structure is two times of the holding voltage of single PMOS. The trigger voltage of 2-PMOSs stacked structure is also double of the trigger voltage of single PMOS in TLP measurement. The 2-PMOSs with d1_6μm, d1_6μm_co_4, and TW_600μm can pass 8 kV in the human-body-model (HBM) ESD test and 500 V in the machine-model (MM) ESD test.

The TLP measured I-V curves of 3-PMOSs with different layout parameters splits (RPO, d1, drain contact number, L, and TW) are compared in Fig. 2.27(a) ~ (e). The detailed characteristics of 3-PMOSs with different layout parameters are listed in Table 2.21.

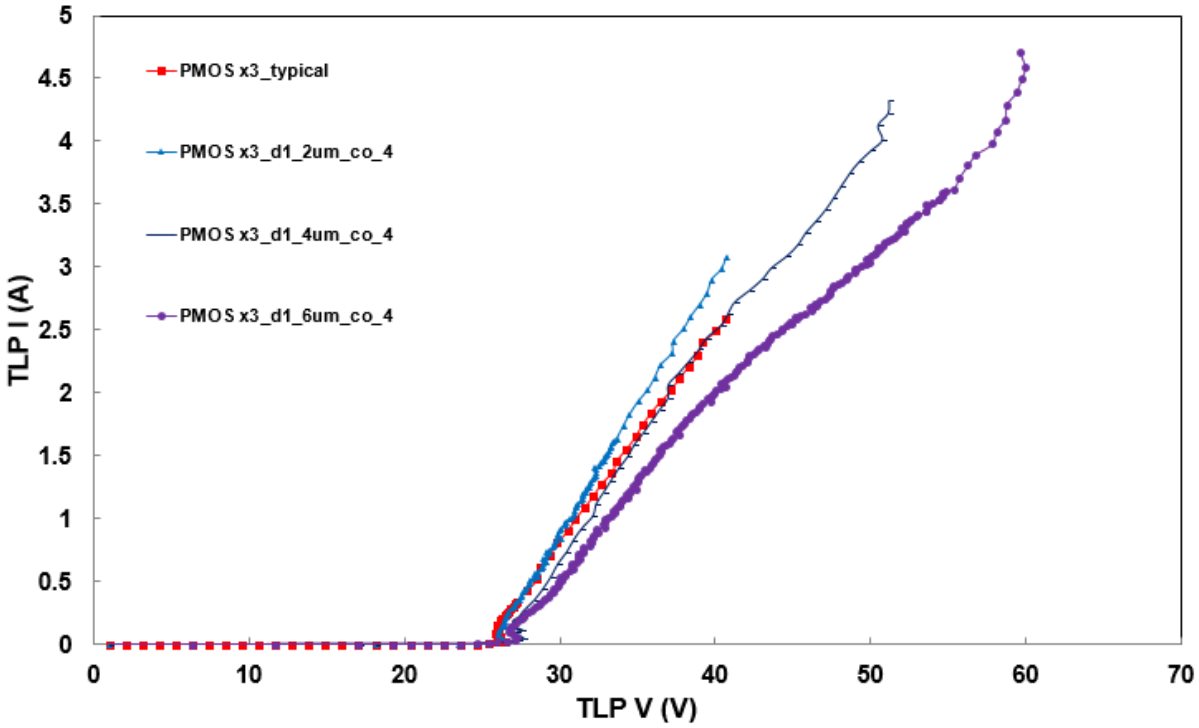


(a)

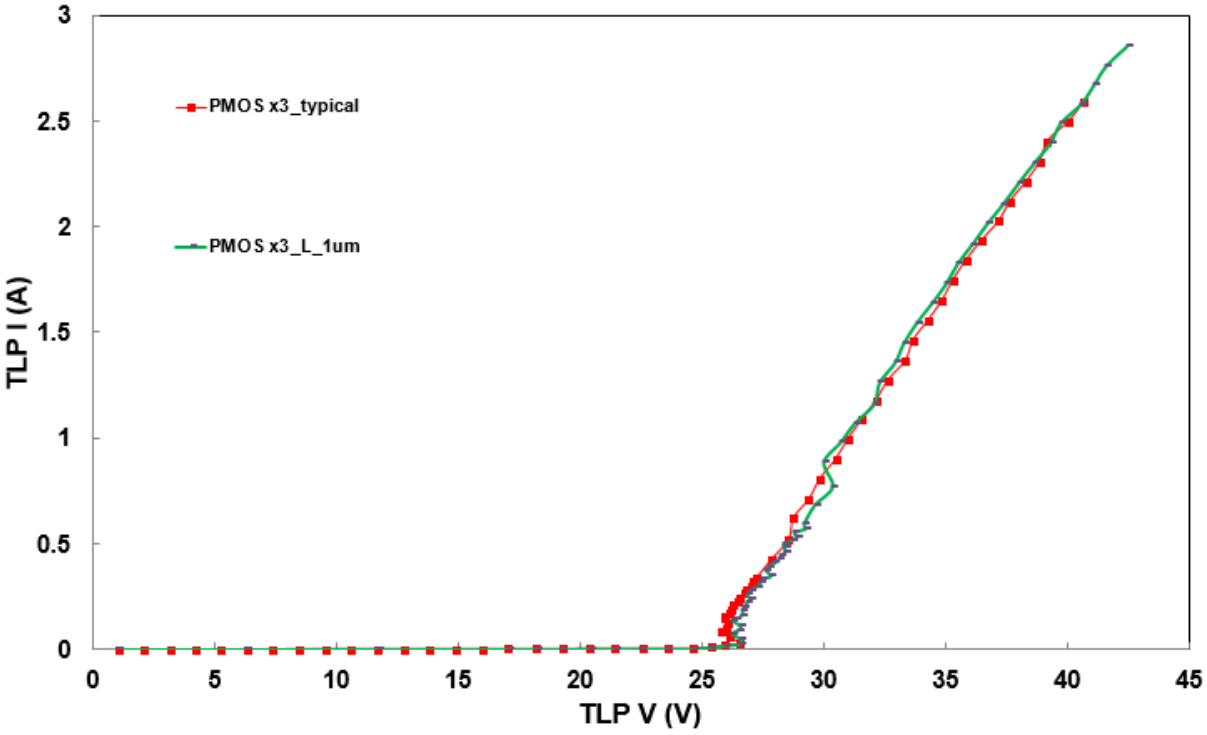


(b)

Fig. 2.27 The TLP measured I-V curves of 3-PMOSs with different (a) RPO splits and (b) d1 splits

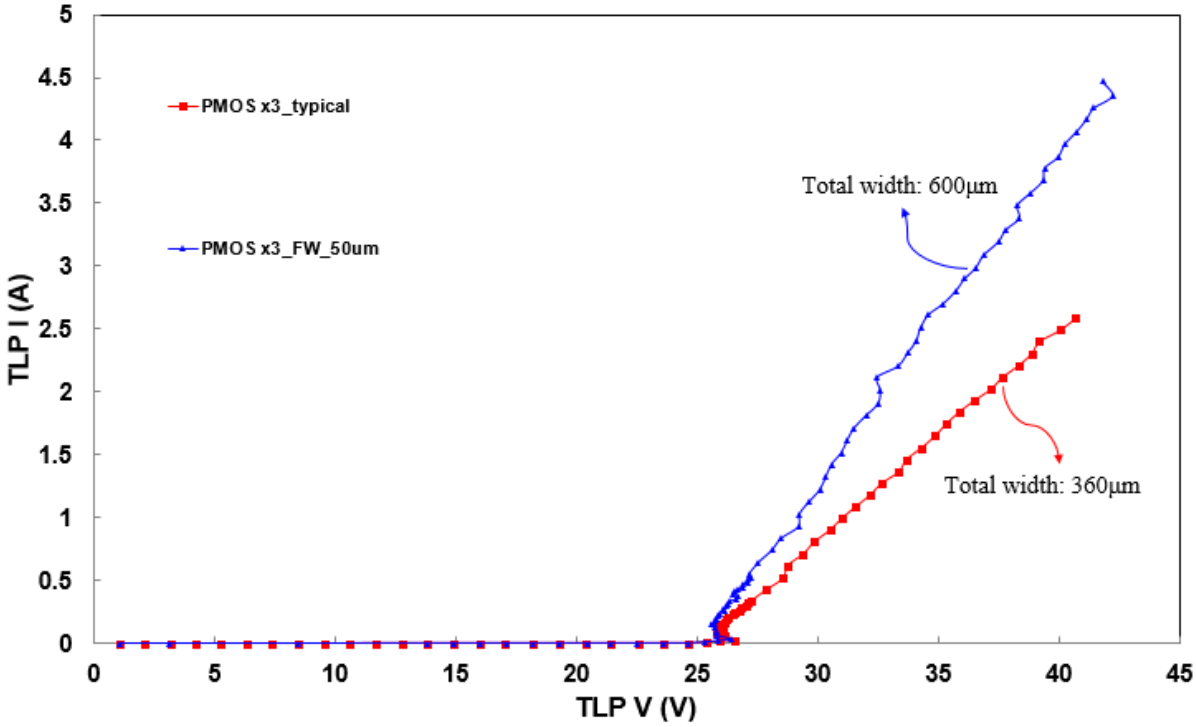


(c)



(d)

Fig. 2.27 The TLP measured I-V curves of 3-PMOSs with different (c) d1 and drain contact number (co) splits and (d) L splits



(e)

Fig. 2.27 The TLP measured I-V curves of 3-PMOSs with different (e) total width splits

Table 2.21

The measurement data of 3-PMOSs with different layout parameters

PMOS x3	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
typical	26.54	25.82	2.49	24.4	4.5	300
no_RPO	29.01	26.58	2.04	24.6	4	250
RPO_0μm	26.63	25.77	2.48	24.4	4.5	350
RPO_-0.03 μm	26.55	26	2.55	24.4	5	350
RPO_-0.06 μm	27.17	26.07	2.49	24.4	4.5	350
d1_4 μm	26.95	26.7	4.29	24.4	7.5	500
d1_6 μm	27.35	27.29	3.71	24.4	>8	500
d1_2 μm_co_4	26.57	26.09	2.98	24.4	5.5	350
d1_4 μm_co_4	27.67	26.97	4.22	24.4	7.5	550
d1_6 μm_co_4	27.27	26.74	4.59	24.4	>8	500
L_1 μm	26.6	26.23	2.76	24.4	5	350
TW_600 μm	26.44	25.56	4.36	24.4	>8	500

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

In Table 2.21, the breakdown voltages in different layout consideration are almost the same. As seen in Table 2.21, the trigger voltage of 3-PMOSs stacked structure is triple of the trigger voltage of single PMOS, and the holding voltage of 3-PMOSs stacked structure is also triple of the holding voltage of single PMOS. The trigger voltages and the holding voltages of 3-PMOSs stacked structure are also the same. ESD robustness of 3-PMOSs with d1_6μm, d1_6μm_co_4, and TW_600μm can pass 8 kV in the human-body-model (HBM) ESD test and 500 V in the machine-model (MM) ESD test.

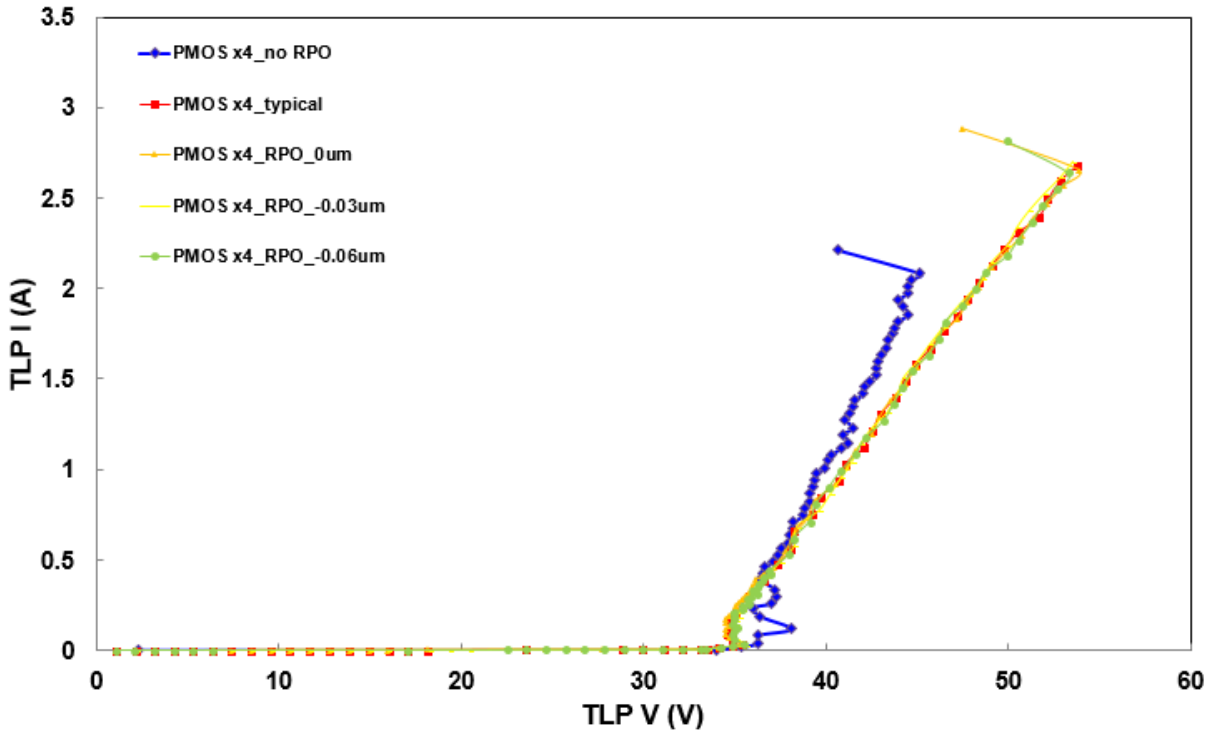
The TLP measured I-V curves of 4-PMOSs with different layout parameters splits (RPO, d1, drain contact number, L, and TW) are compared in Fig. 2.28(a) ~ (e). The detailed characteristics of 4-PMOSs with different layout parameters are listed in Table 2.22.

The TLP measured I-V curves of 5-PMOSs with different layout parameters splits (RPO, d1, drain contact number, L, and TW) are compared in Fig. 2.29(a) ~ (e). The detailed characteristics of 5-PMOSs with different layout parameters are listed in Table 2.23.

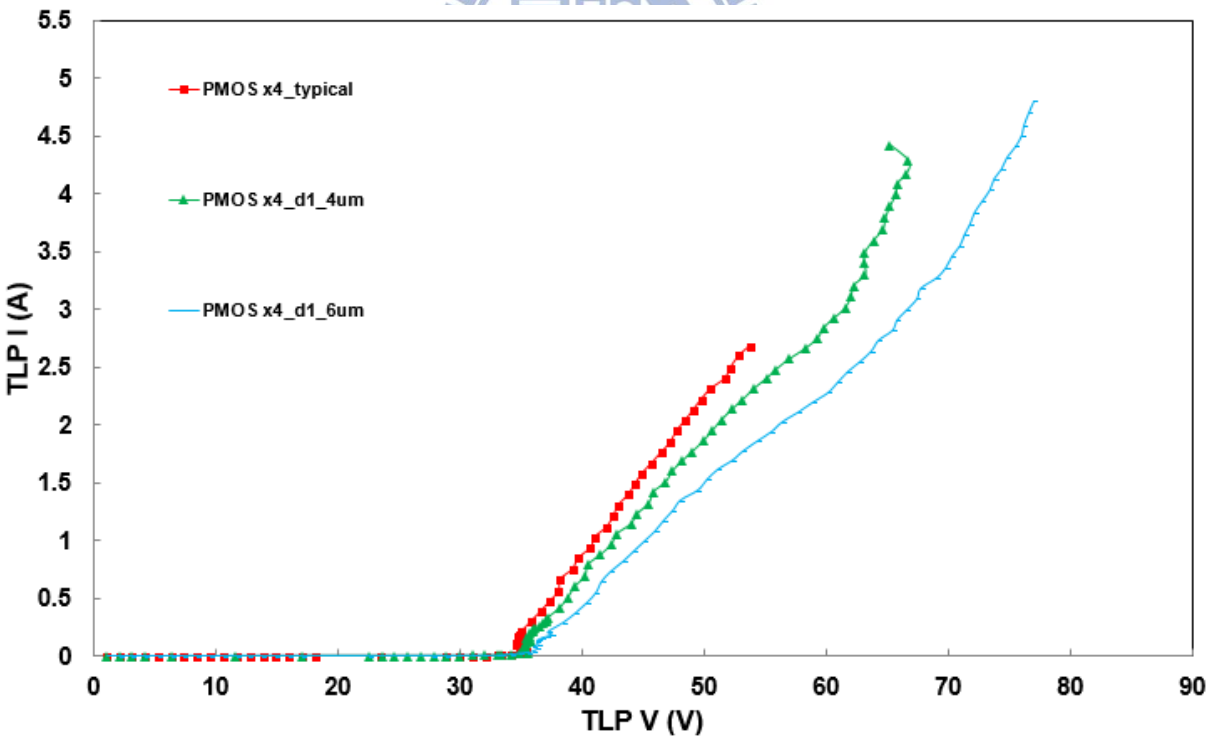
The TLP measured I-V curves of 6-PMOSs with different layout parameters splits (RPO, d1, drain contact number, L, and TW) are compared in Fig. 2.30(a) ~ (e). The detailed characteristics of 6-PMOSs with different layout parameters are listed in Table 2.24.

The TLP measured I-V curves of 7-PMOSs with different layout parameters splits (RPO, d1, drain contact number, L, and TW) are compared in Fig. 2.31(a) ~ (e). The detailed characteristics of 7-PMOSs with different layout parameters are listed in Table 2.25.

The TLP measured I-V curves of 8-PMOSs with different layout parameters splits (RPO, d1, drain contact number, L, and TW) are compared in Fig. 2.32(a) ~ (e). The detailed characteristics of 8-PMOSs with different layout parameters are listed in Table 2.26.

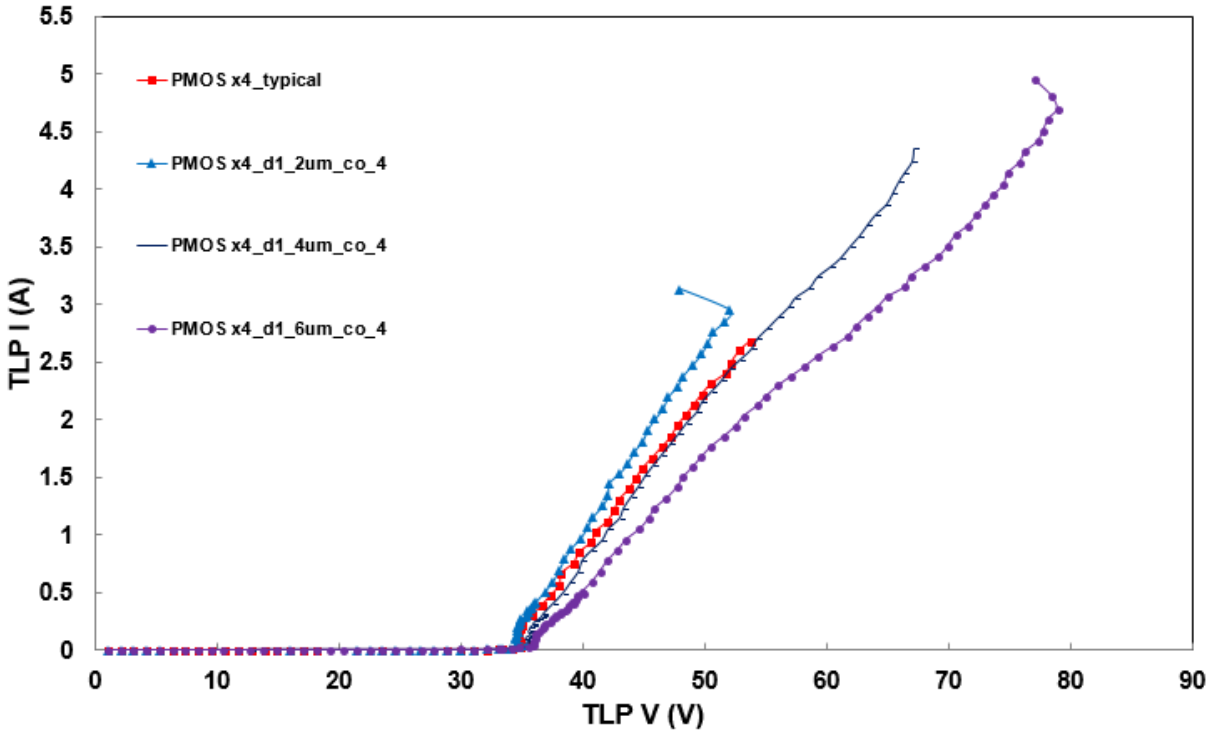


(a)

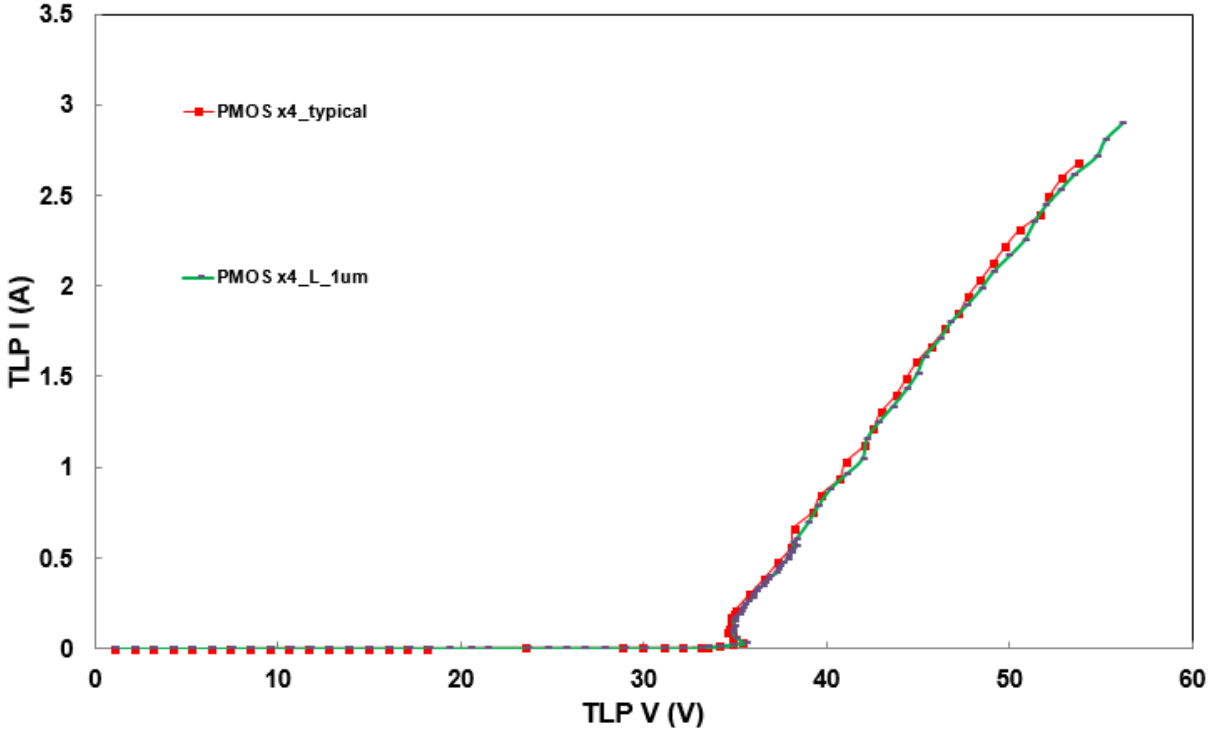


(b)

Fig. 2.28 The TLP measured I-V curves of 4-PMOSs with different (a) RPO splits and (b) d1 splits

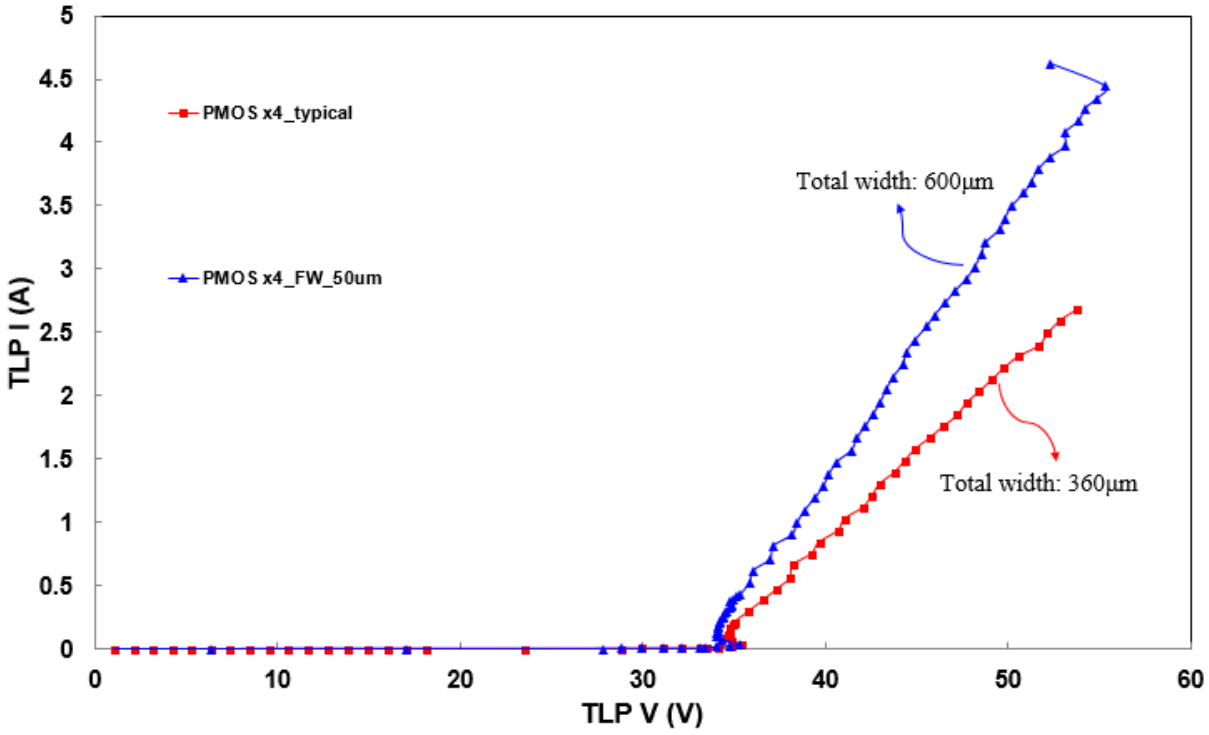


(c)



(d)

Fig. 2.28 The TLP measured I-V curves of 4-PMOSs with different (c) d1 and drain contact number (co) splits and (d) L splits



(e)

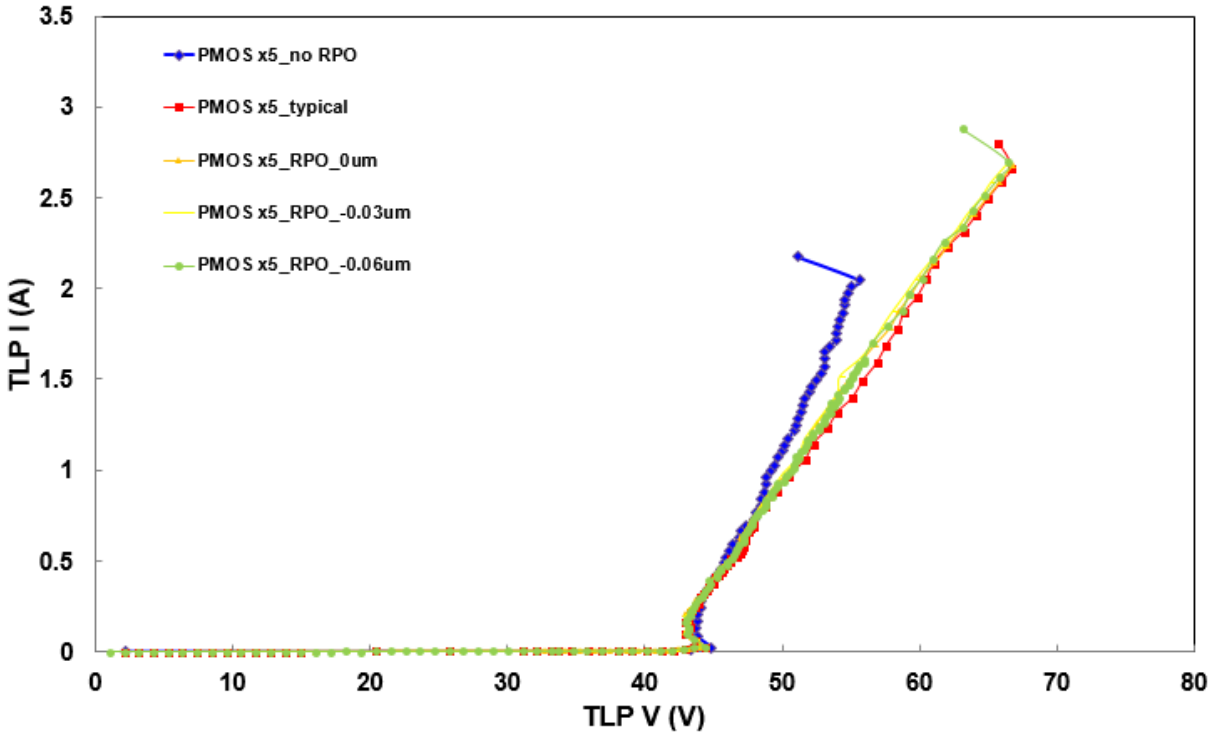
Fig. 2.28 The TLP measured I-V curves of 4-PMOSs with different (e) total width splits

Table 2.22

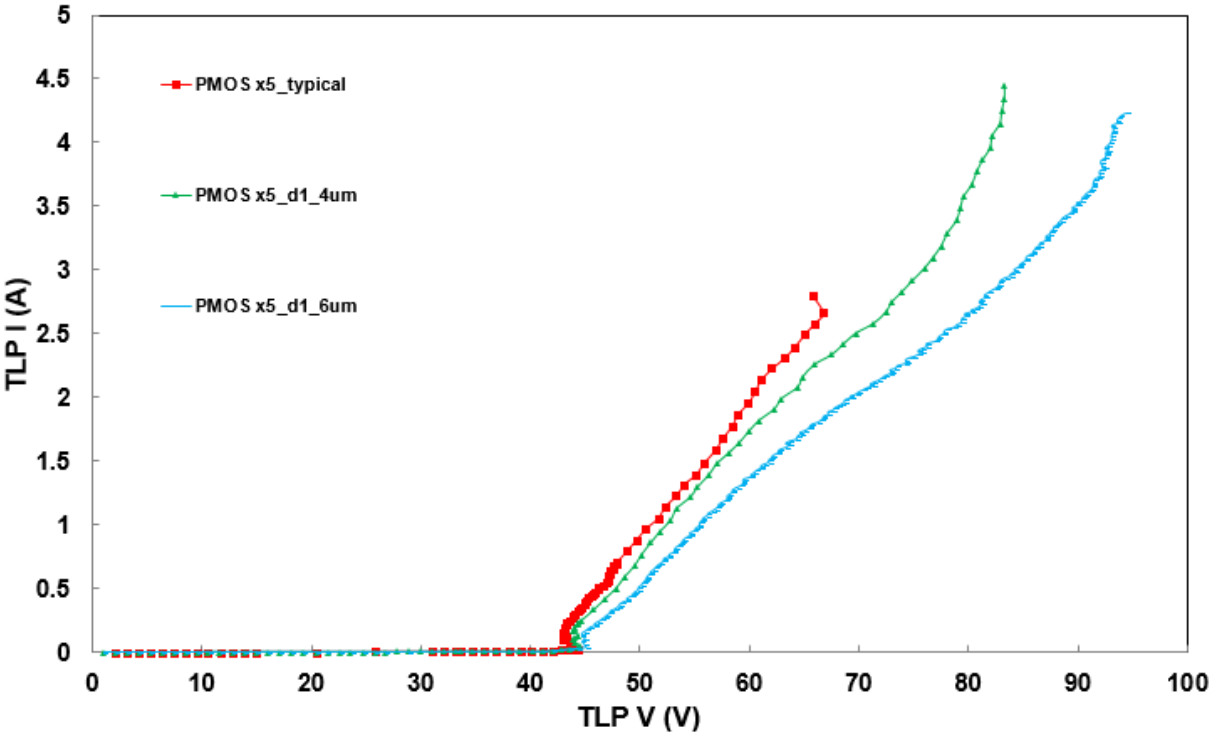
The measurement data of 4-PMOSs with different layout parameters

PMOS x4	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
typical	35.41	34.54	2.6	32.6	5	350
no_RPO	36.3	35.96	2.08	32.8	4	250
RPO_0μm	35.29	34.46	2.66	32.6	4.5	350
RPO_-0.03 μm	35.6	34.82	2.61	32.6	4.5	350
RPO_-0.06 μm	35.48	34.83	2.64	32.5	4.5	350
d1_4 μm	35.55	35.26	4.28	32.5	7	550
d1_6 μm	36.25	36.04	4.7	32.5	>8	550
d1_2 μm_co_4	35.39	34.4	2.94	32.5	5.5	400
d1_4 μm_co_4	35.69	35.3	4.24	32.5	7.5	550
d1_6 μm_co_4	36.15	36.07	4.81	32.5	>8	550
L_1 μm	35.49	34.8	2.8	32.5	5	400
TW_600 μm	35.31	34.02	4.44	32.5	>8	550

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

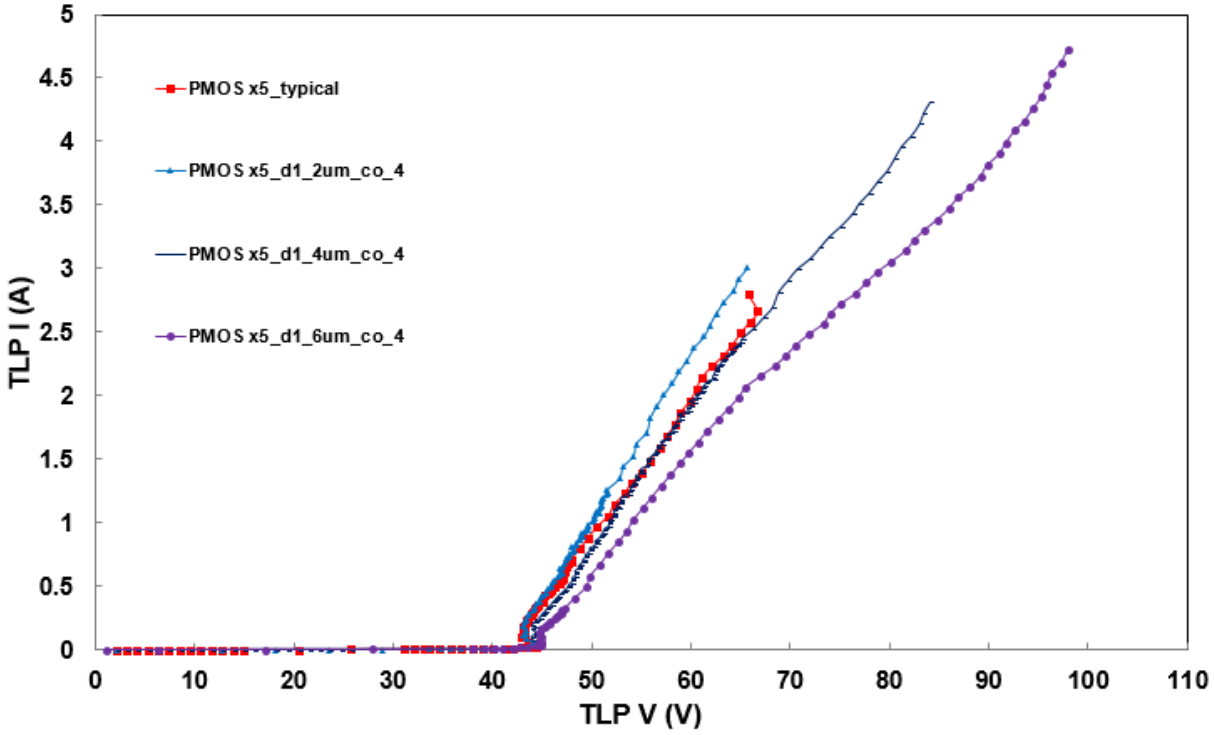


(a)

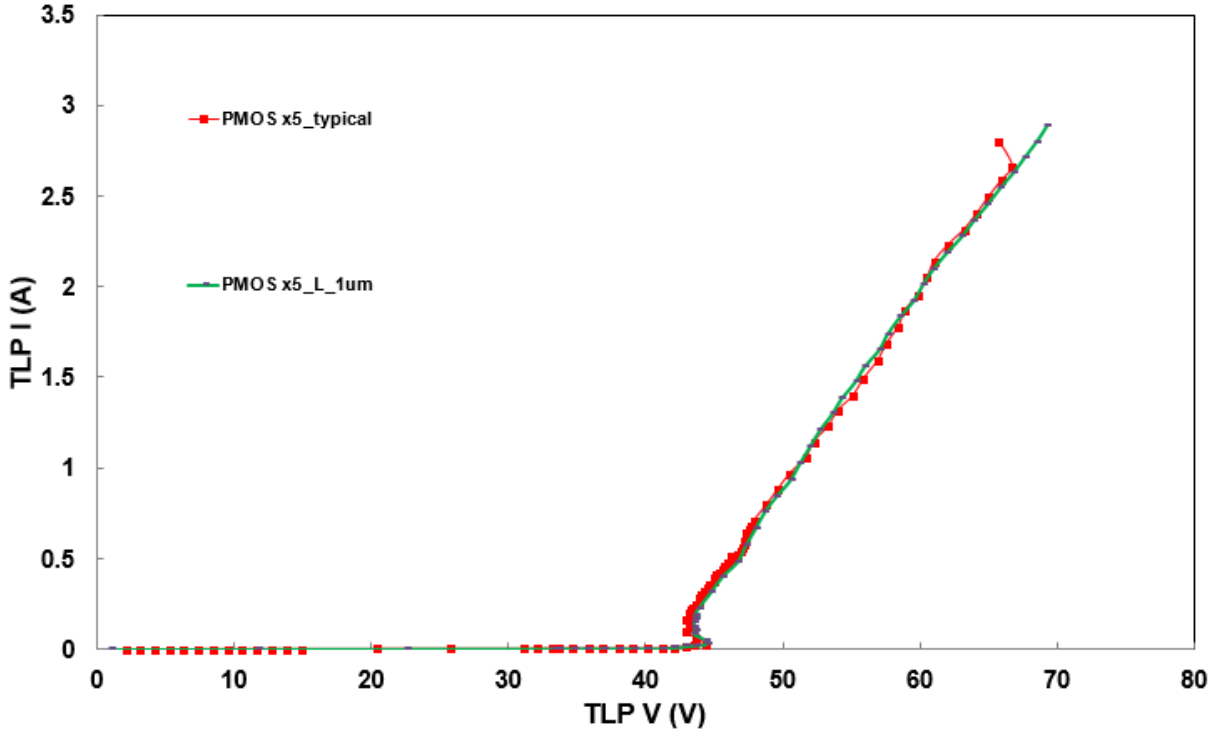


(b)

Fig. 2.29 The TLP measured I-V curves of 5-PMOSs with different (a) RPO splits and (b) d1 splits

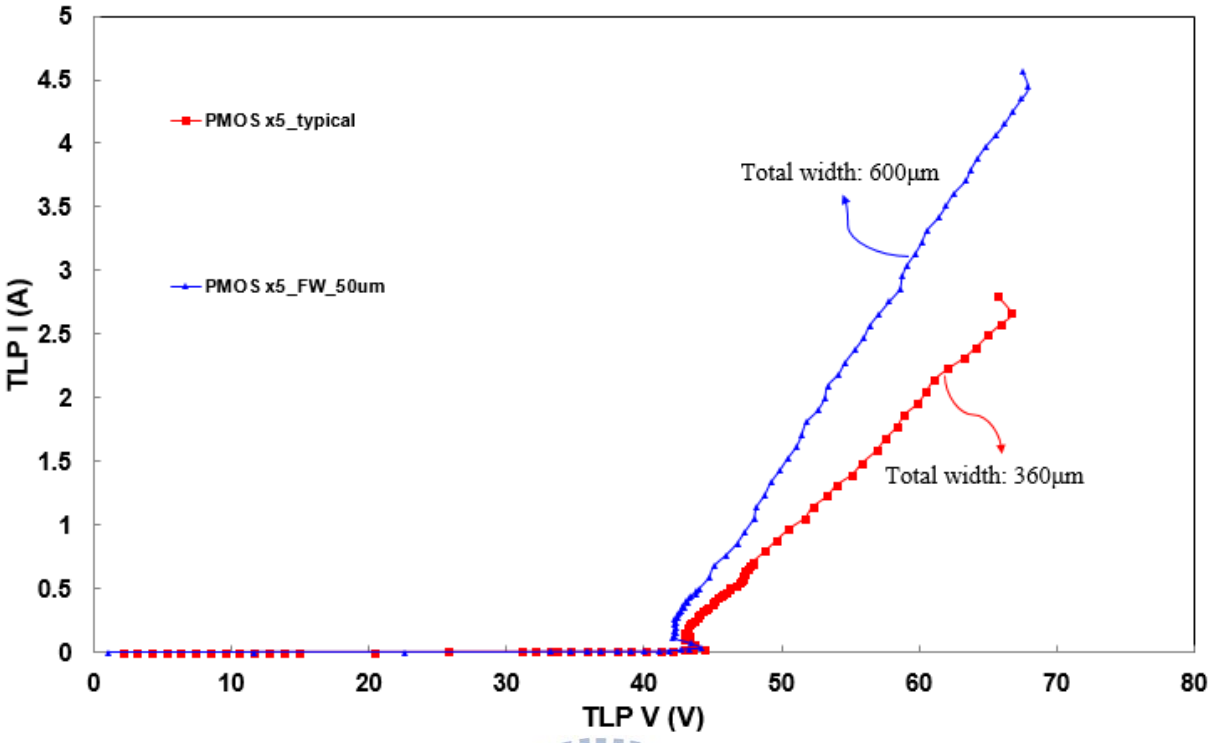


(c)



(d)

Fig. 2.29 The TLP measured I-V curves of 5-PMOSs with different (c) d1 and drain contact number (co) splits and (d) L splits



(e)

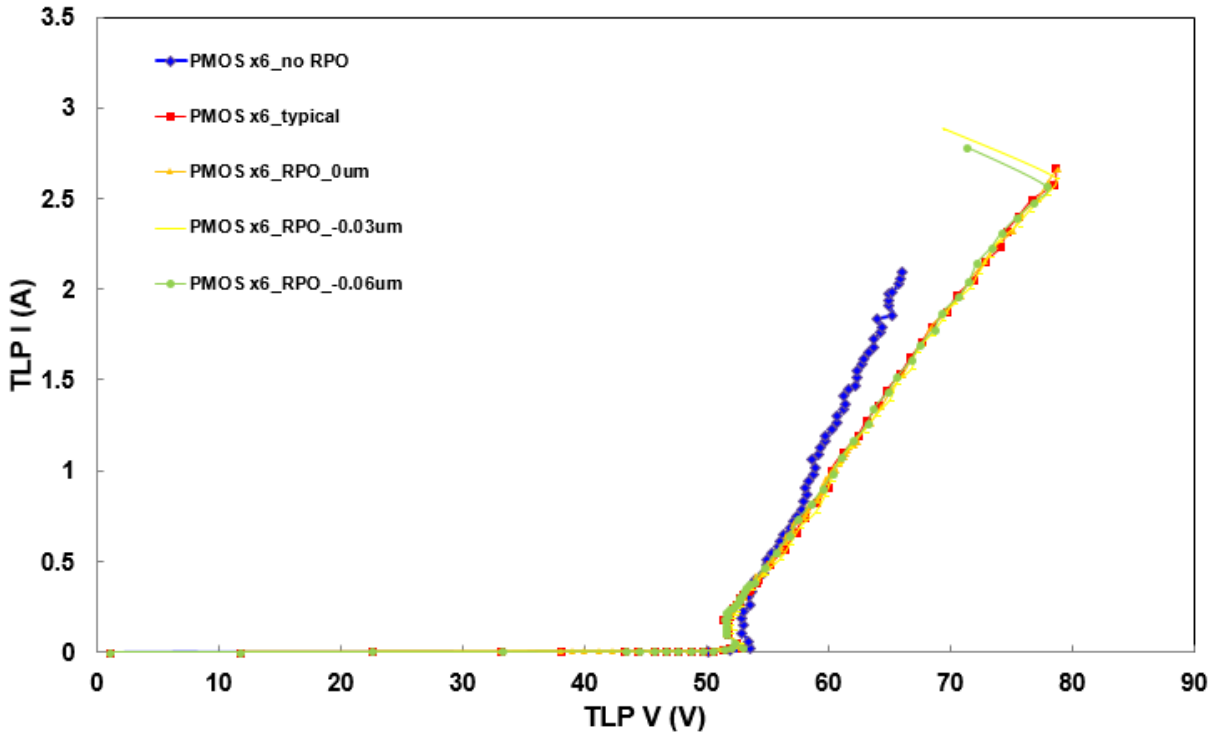
Fig. 2.29 The TLP measured I-V curves of 5-PMOSs with different (e) total width splits

Table 2.23

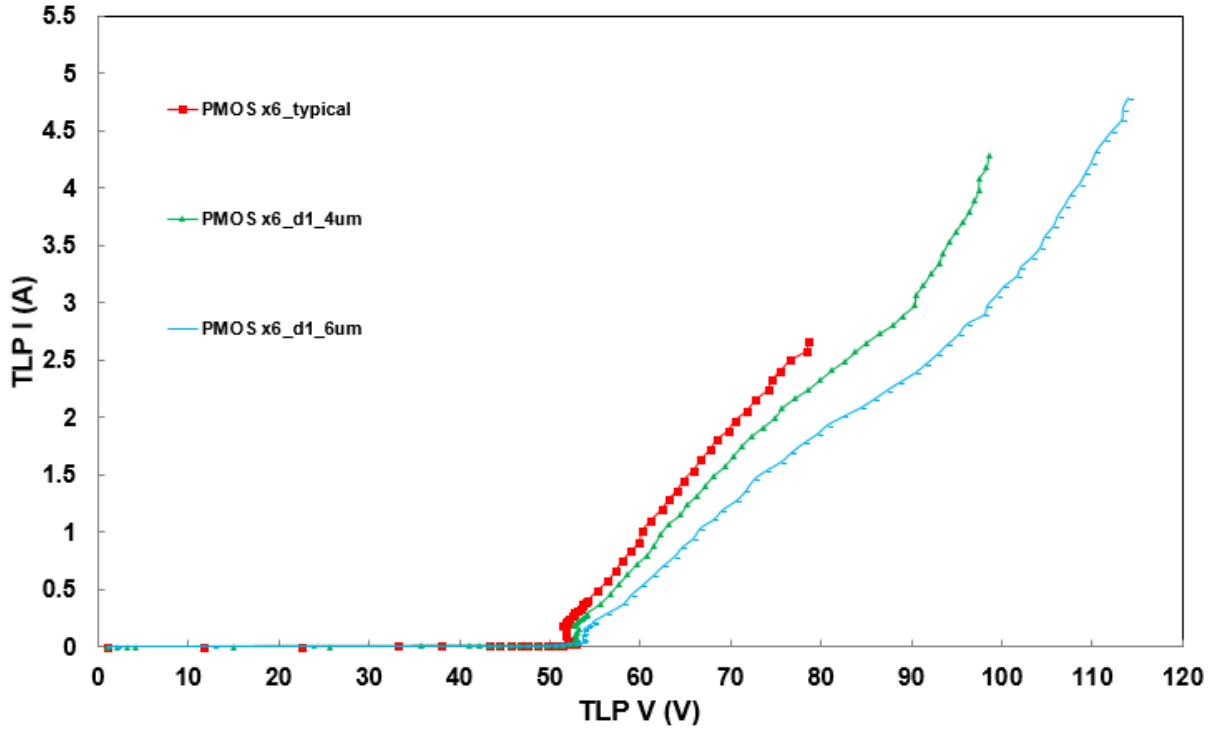
The measurement data of 5-PMOSs with different layout parameters

PMOS x5	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
typical	44.34	42.92	2.66	40.7	5	350
no_RPO	44.76	43.84	2.05	41	4	300
RPO_0µm	44.08	42.93	2.59	40.7	5	350
RPO_-0.03 µm	44.42	42.92	2.58	40.7	4.5	350
RPO_-0.06 µm	44.35	42.97	2.7	40.7	5	350
d1_4 µm	44.53	43.84	4.35	40.7	7.5	550
d1_6 µm	45.06	44.67	4.2	40.7	>8	550
d1_2 µm_co_4	44.33	43.09	2.92	40.6	5.5	400
d1_4 µm_co_4	44.56	43.86	4.23	40.6	7.5	600
d1_6 µm_co_4	44.97	44.68	4.62	40.7	>8	550
L_1 µm	44.42	43.47	2.8	40.7	5	400
TW_600 µm	44.17	42.08	4.44	40.6	>8	550

#DC BV: I = 1µA *ESD failure criteria: I-V curve shift > 10%

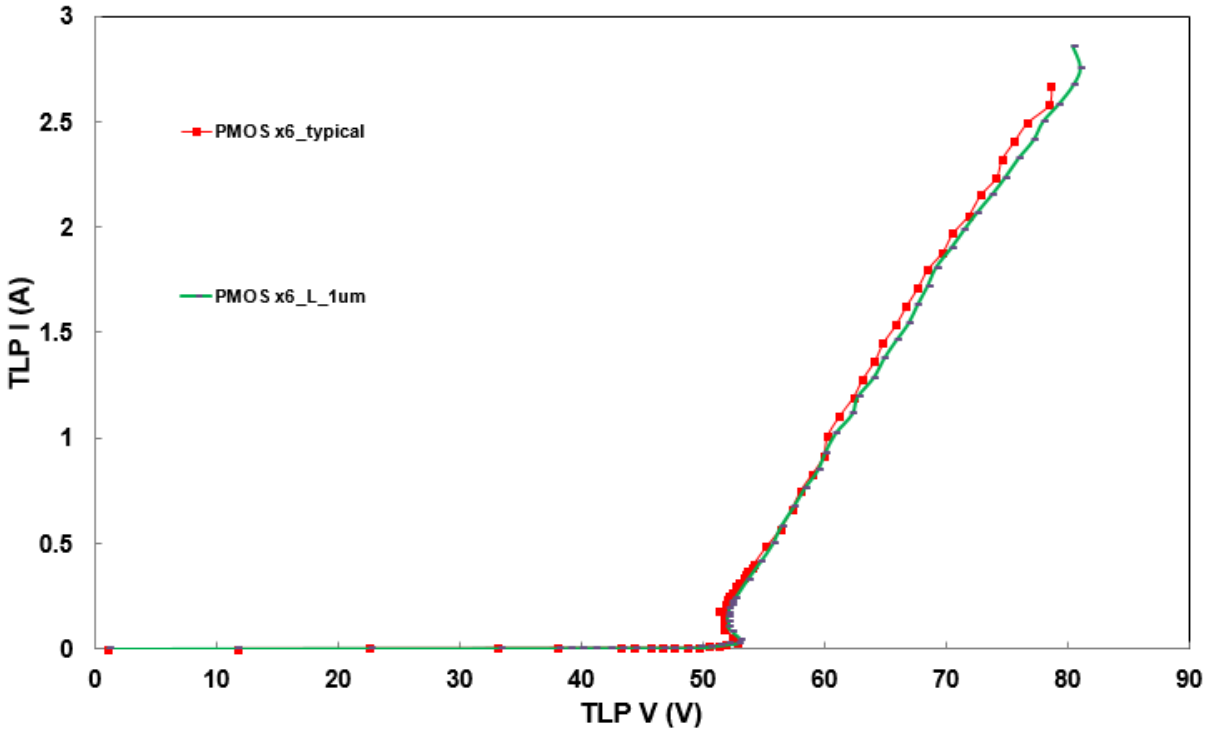


(a)

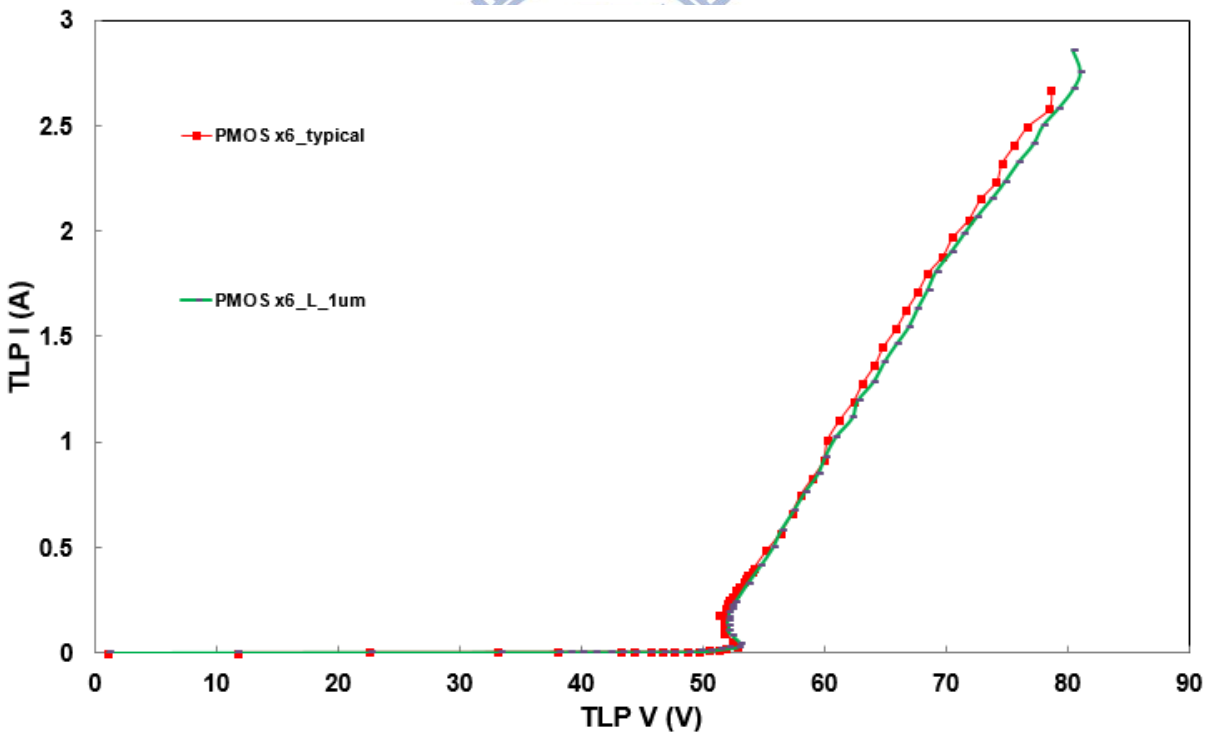


(b)

Fig. 2.30 The TLP measured I-V curves of 6-PMOSs with different (a) RPO splits and (b) d1 splits

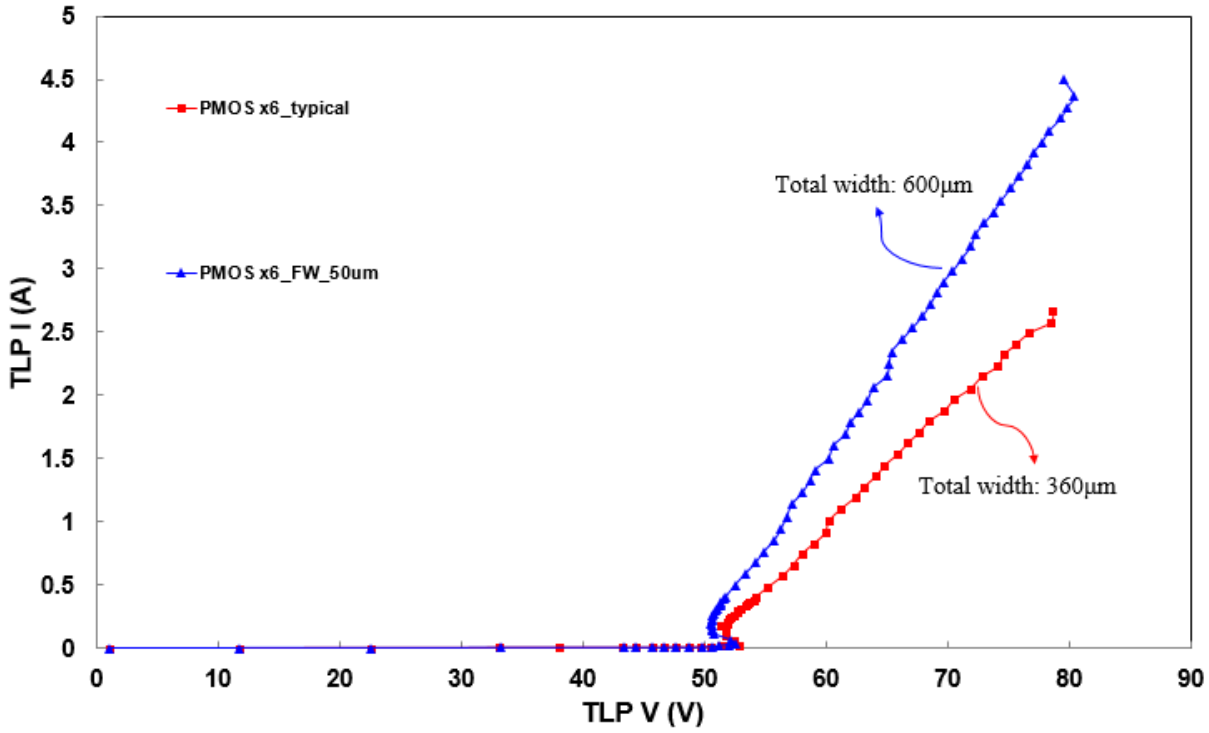


(c)



(d)

Fig. 2.30 The TLP measured I-V curves of 6-PMOSs with different (c) d1 and drain contact number (co) splits and (d) L splits



(e)

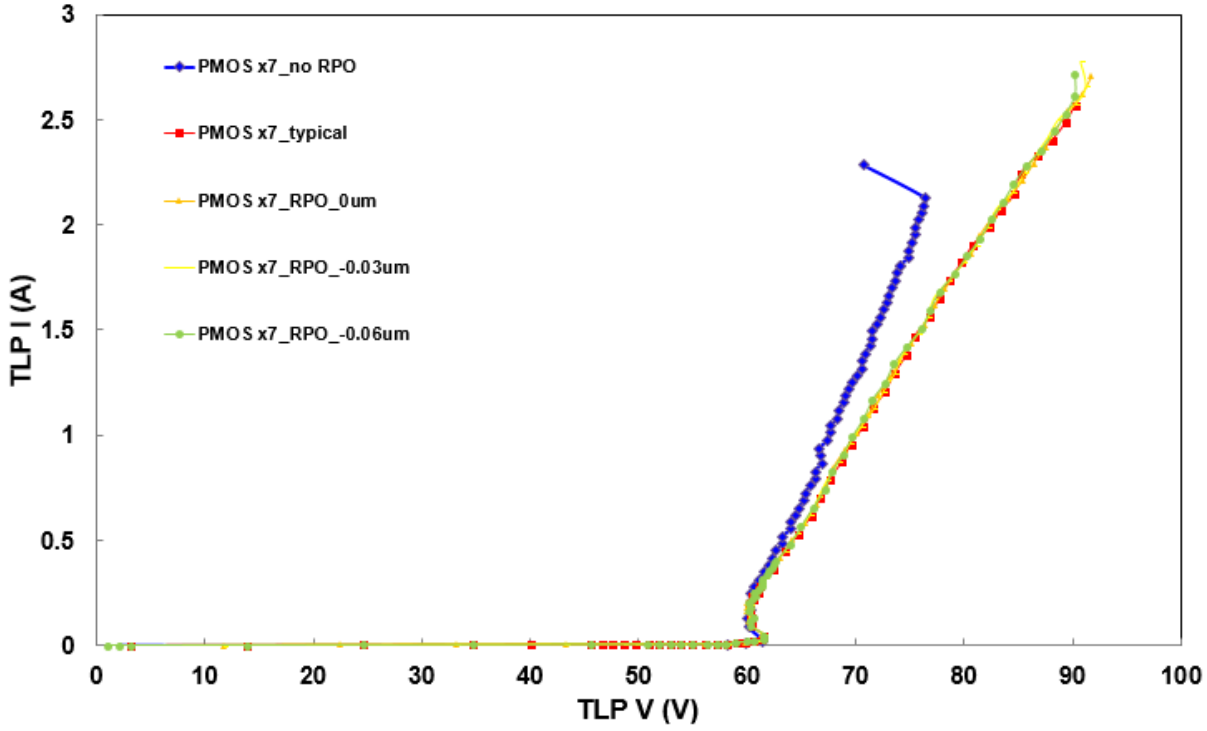
Fig. 2.30 The TLP measured I-V curves of 6-PMOSs with different (e) total width splits

Table 2.24

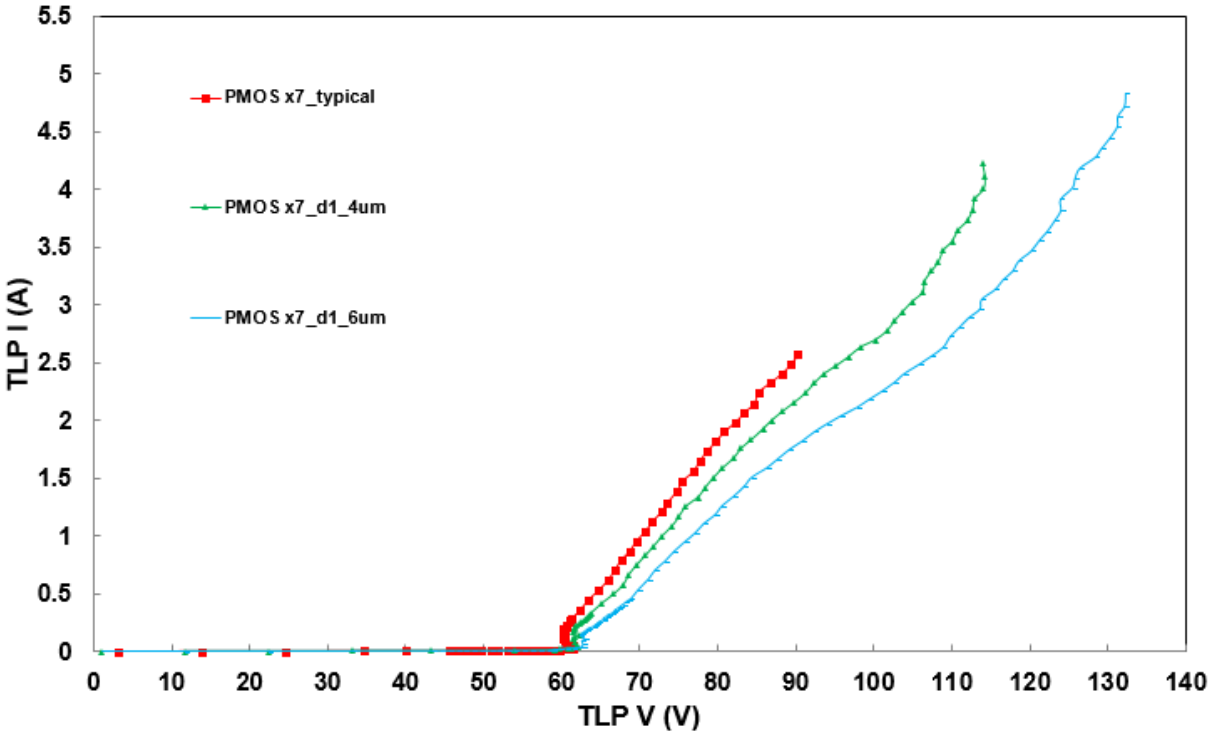
The measurement data of 6-PMOSs with different layout parameters

PMOS x6	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
typical	52.79	51.36	2.58	48.8	5	400
no_RPO	53.53	52.86	2.06	49	4	300
RPO_0μm	52.77	51.52	2.58	48.8	5	400
RPO_-0.03 μm	52.81	51.64	2.62	48.8	5	400
RPO_-0.06 μm	52.9	51.42	2.57	48.8	5	400
d1_4 μm	53.29	52.67	4.18	48.8	7.5	550
d1_6 μm	53.69	53.62	4.68	48.8	>8	600
d1_2 μm_co_4	52.86	51.58	3	48.8	5.5	450
d1_4 μm_co_4	53.35	52.68	4.31	48.8	7.5	600
d1_6 μm_co_4	53.84	53.73	4.77	48.8	>8	600
L_1 μm	53.09	52	2.75	48.8	5.5	450
TW_600 μm	52.54	50.48	4.37	48.8	>8	600

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

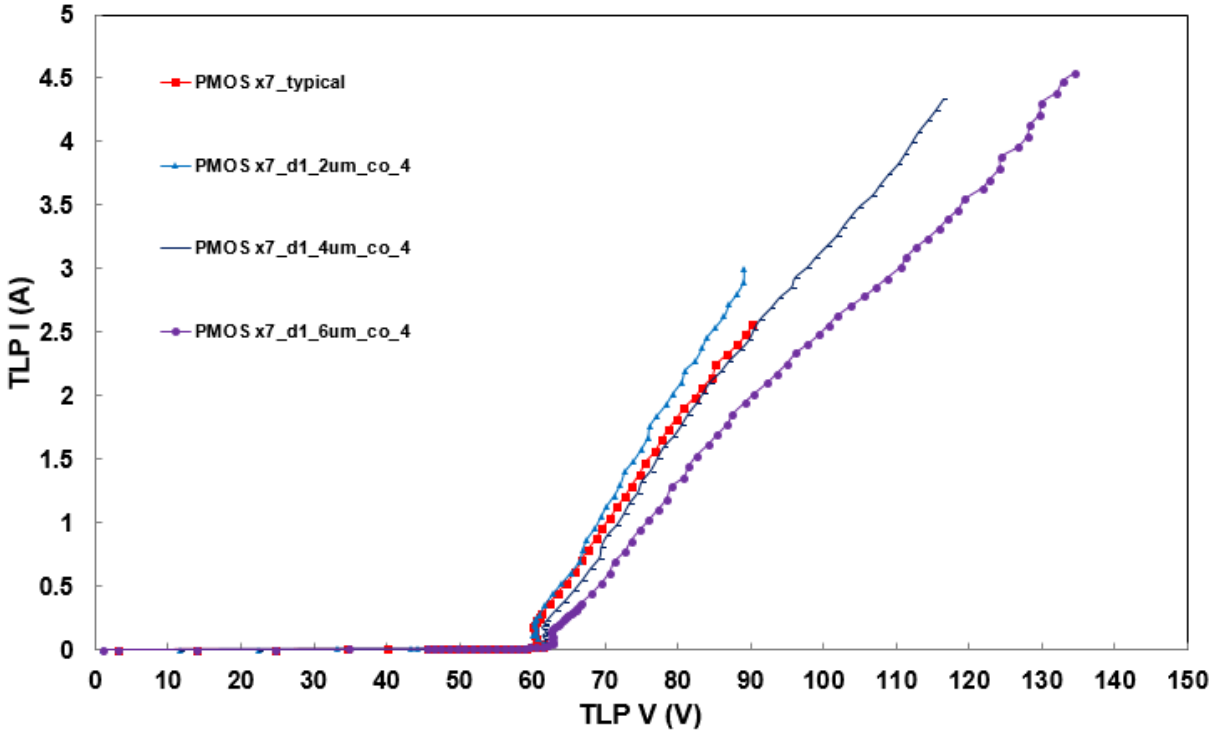


(a)

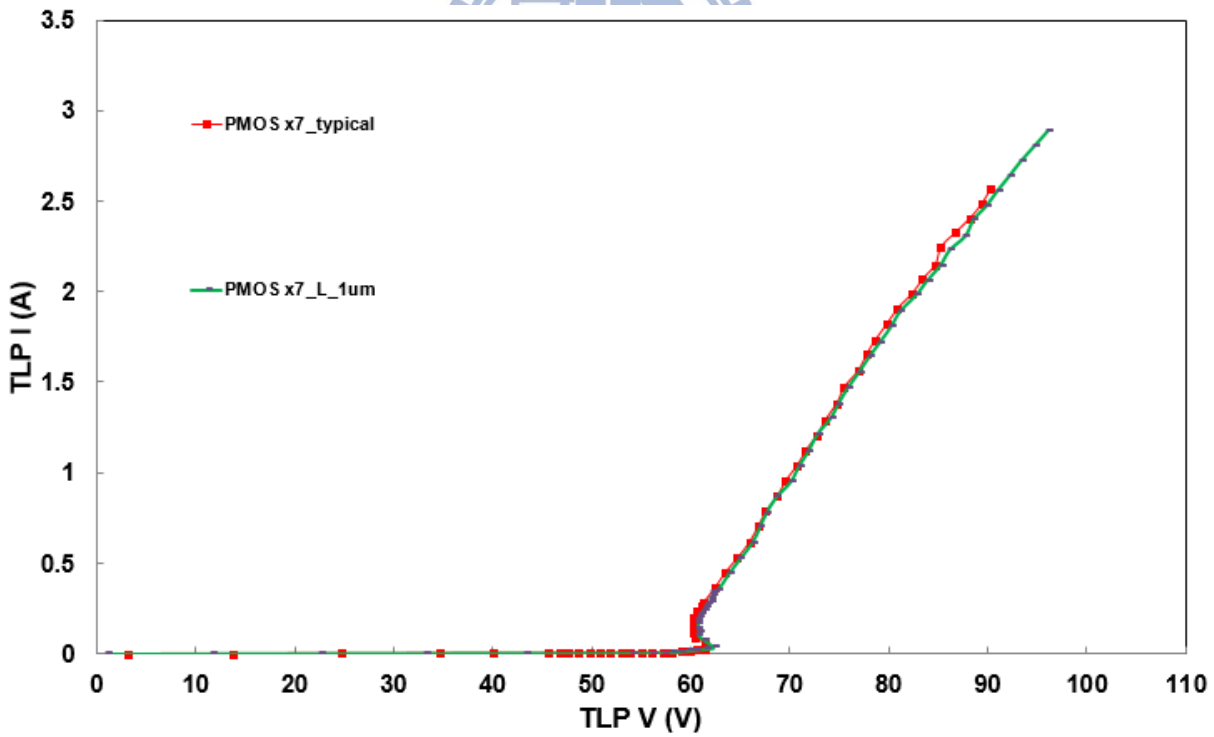


(b)

Fig. 2.31 The TLP measured I-V curves of 7-PMOSs with different (a) RPO splits and (b) d1 splits

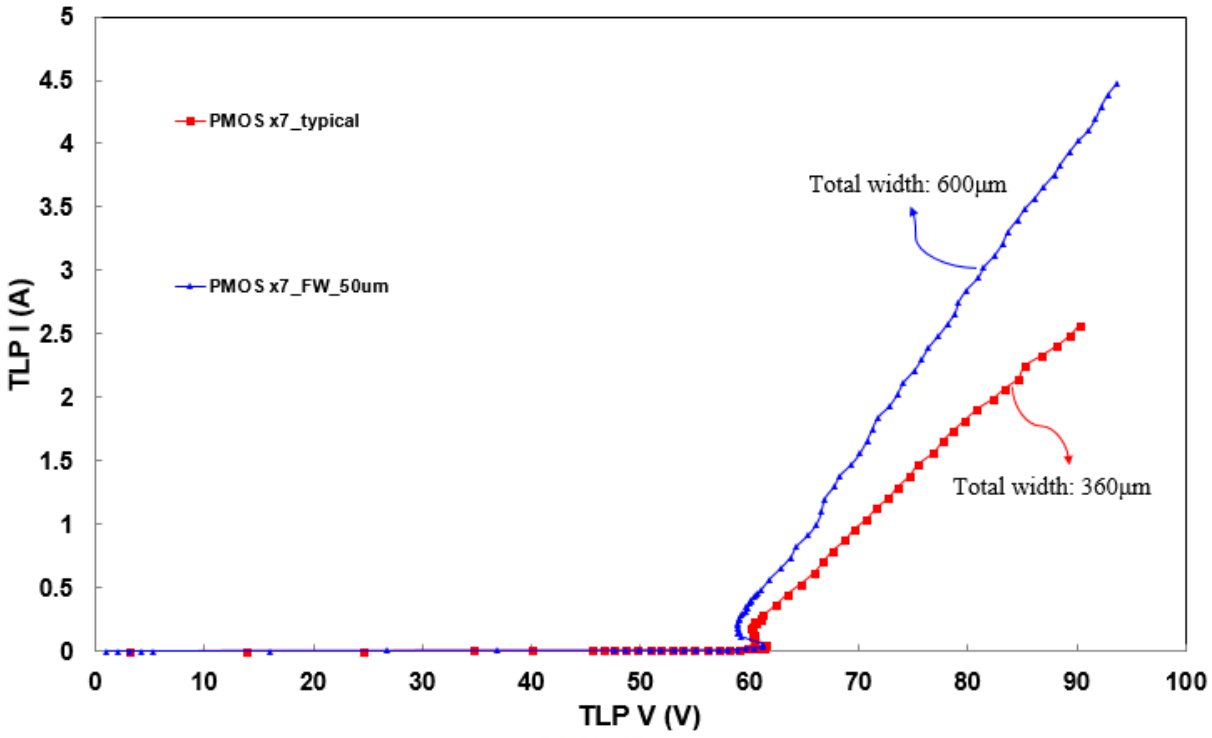


(c)



(d)

Fig. 2.31 The TLP measured I-V curves of 7-PMOSs with different (c) d1 and drain contact number (co) splits and (d) L splits



(e)

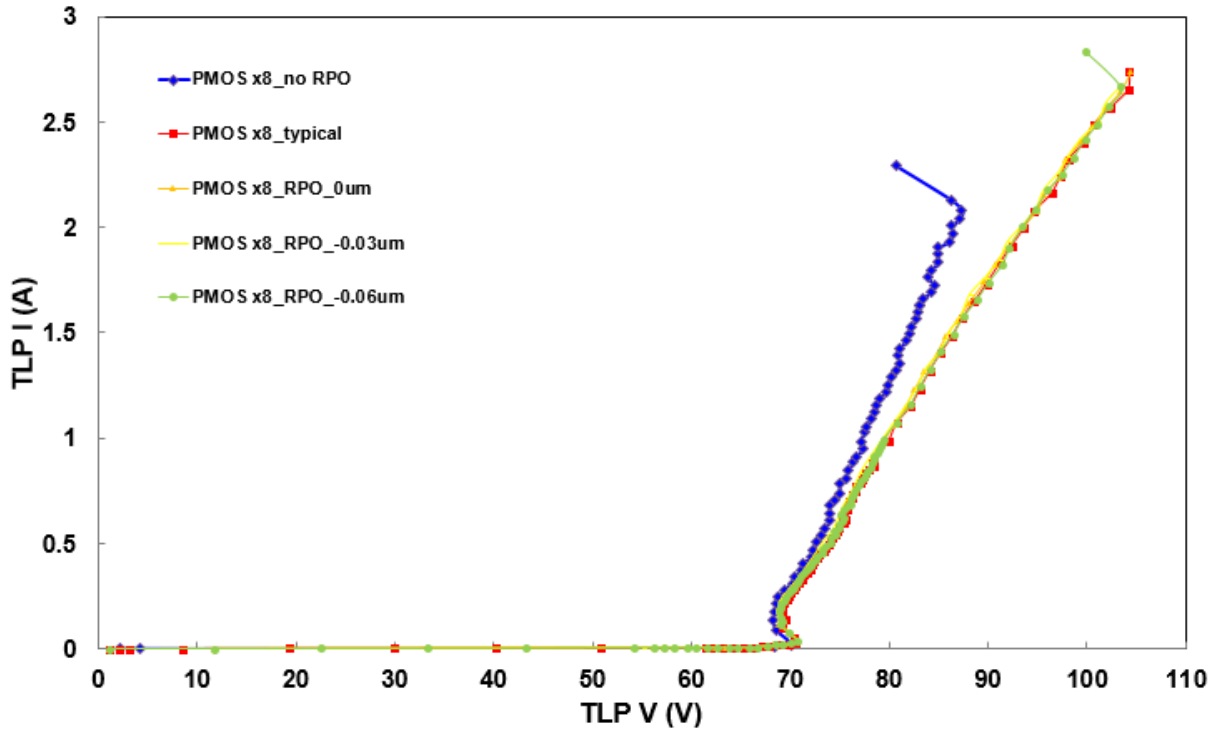
Fig. 2.31 The TLP measured I-V curves of 7-PMOSs with different (e) total width splits

Table 2.25

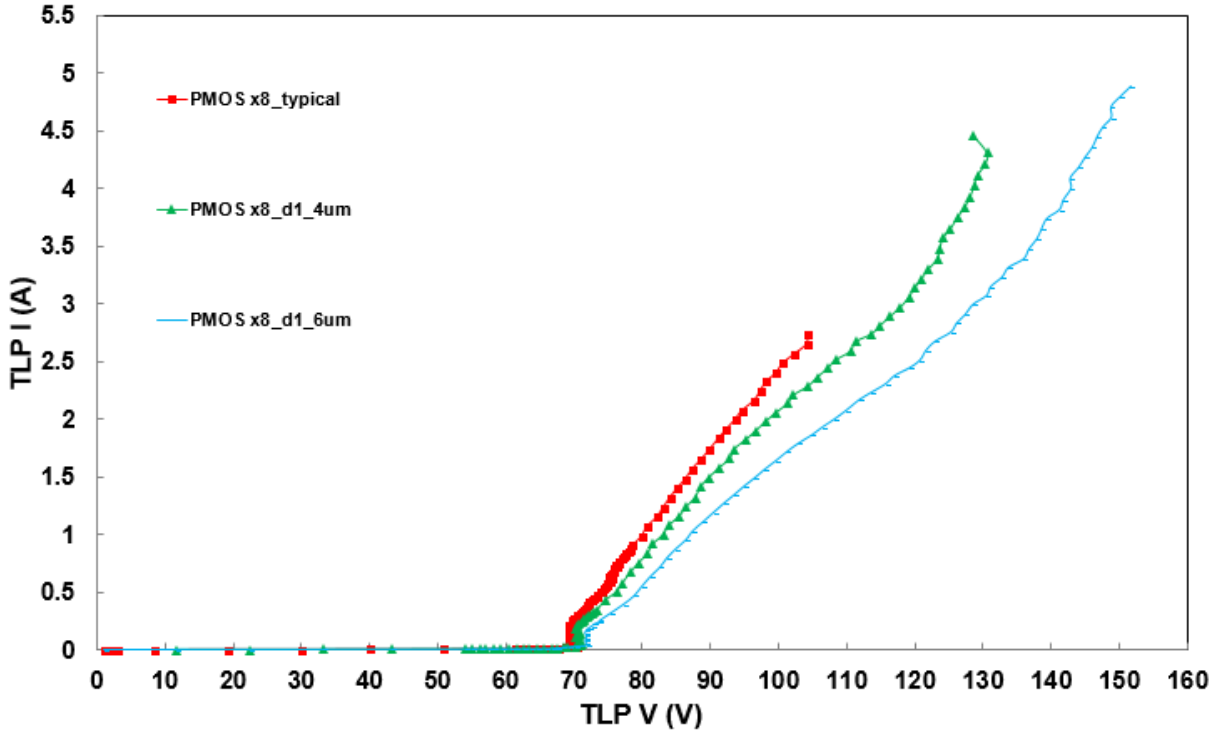
The measurement data of 7-PMOSs with different layout parameters

PMOS x7	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
typical	61.49	60.21	2.49	57	5	400
no_RPO	61.49	60.17	2.13	57.2	4	300
RPO_0μm	61.41	60.01	2.62	57	5	400
RPO_-0.03 μm	61.54	60.07	2.66	57	5	400
RPO_-0.06 μm	61.58	60.17	2.62	57	5	400
d1_4 μm	62.07	61.36	4.1	56.8	7.5	600
d1_6 μm	62.94	62.38	4.72	57	>8	550
d1_2 μm_co_4	61.66	60.21	2.89	57	5.5	450
d1_4 μm_co_4	62.18	61.41	4.25	57	>8	600
d1_6 μm_co_4	62.9	62.52	4.47	57	>8	650
L_1 μm	62.28	60.72	2.81	57	5	450
TW_600 μm	61.28	58.85	4.38	57	>8	600

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

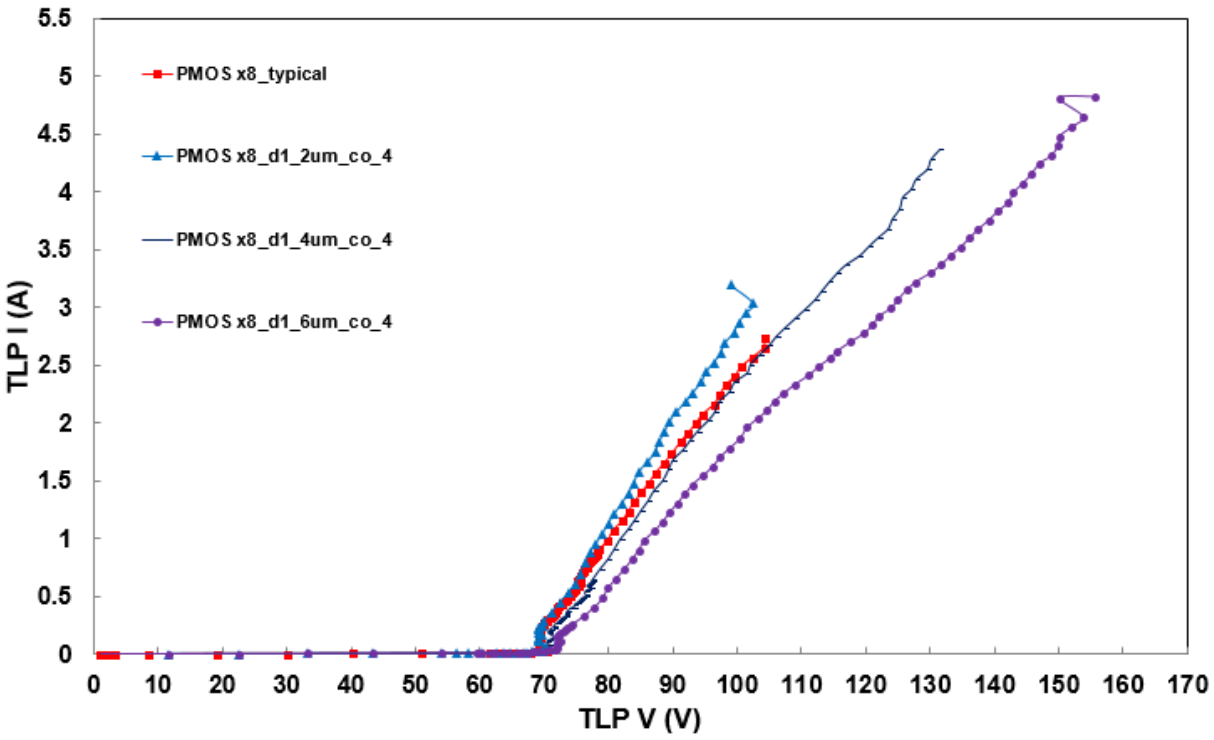


(a)

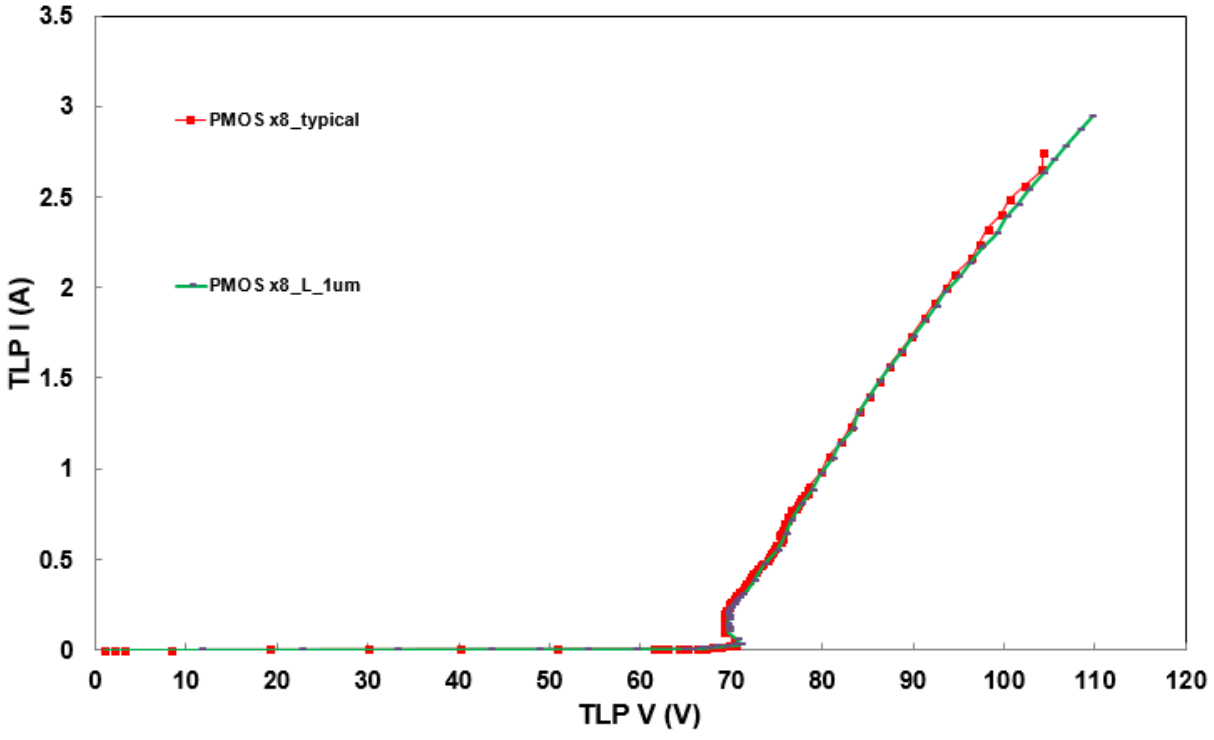


(b)

Fig. 2.32 The TLP measured I-V curves of 8-PMOSs with different (a) RPO splits and (b) d1 splits

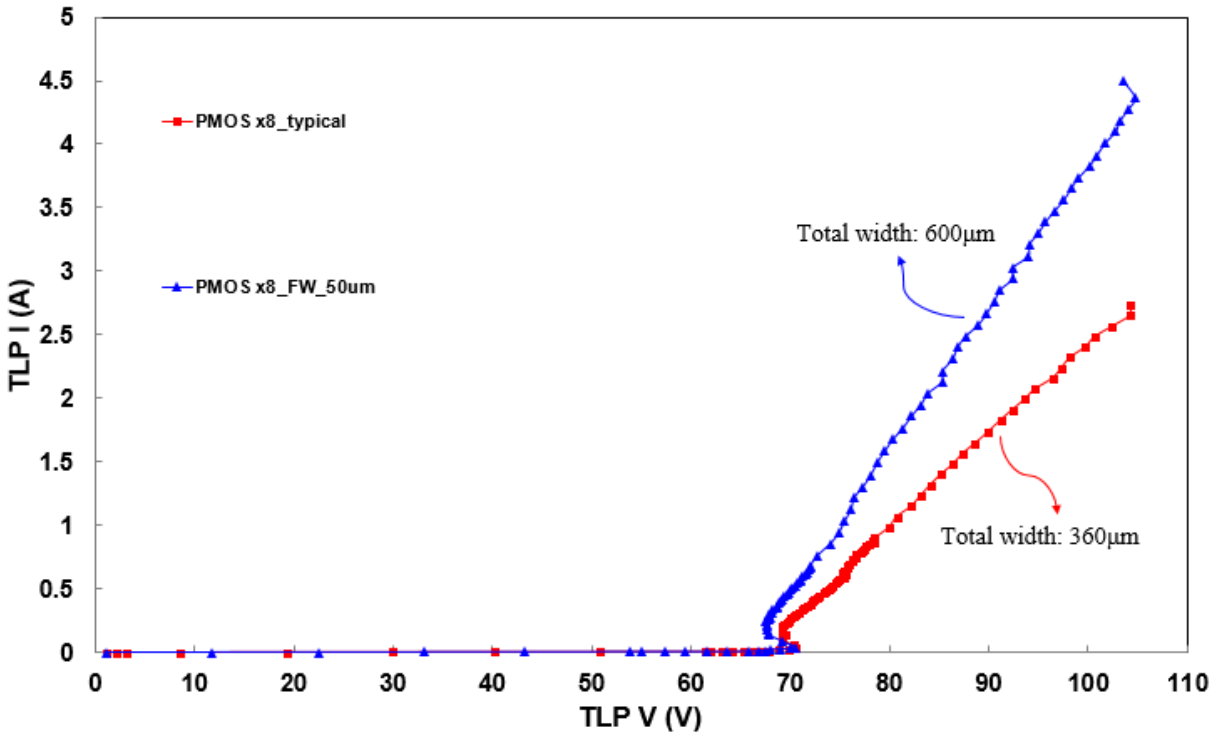


(c)



(d)

Fig. 2.32 The TLP measured I-V curves of 8-PMOSs with different (c) d1 and drain contact number (co) splits and (d) L splits



(e)

Fig. 2.32 The TLP measured I-V curves of 8-PMOSs with different (e) total width splits

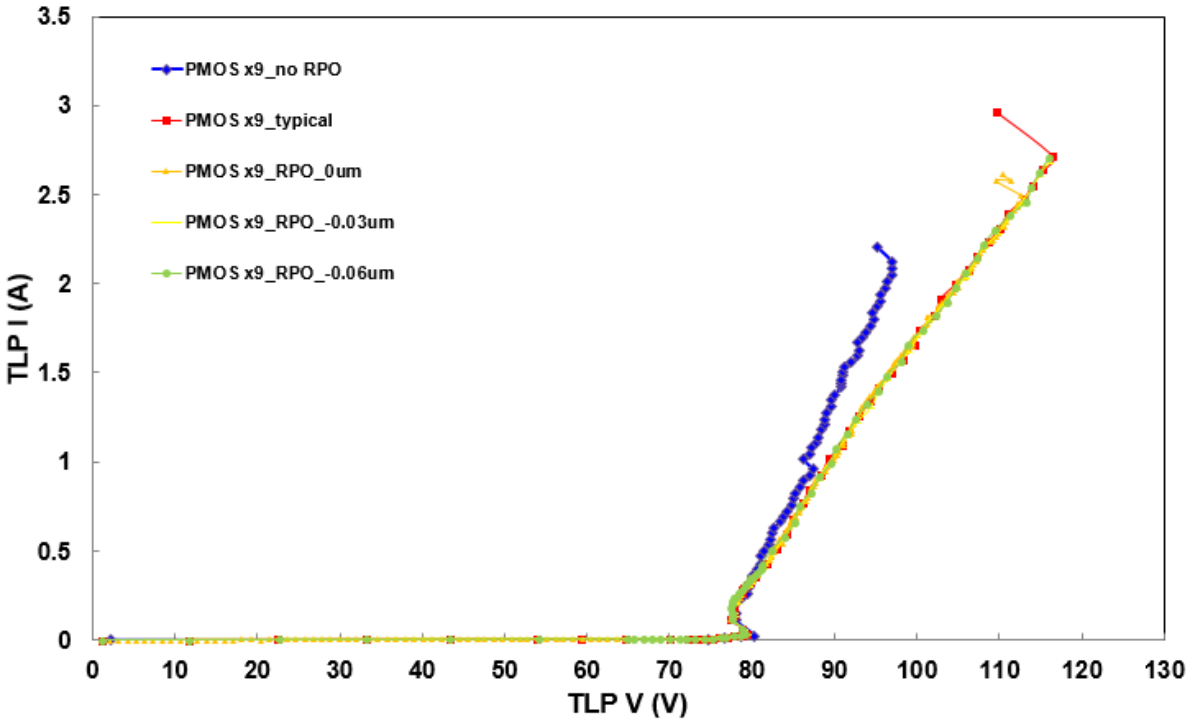
Table 2.26

The measurement data of 8-PMOSs with different layout parameters

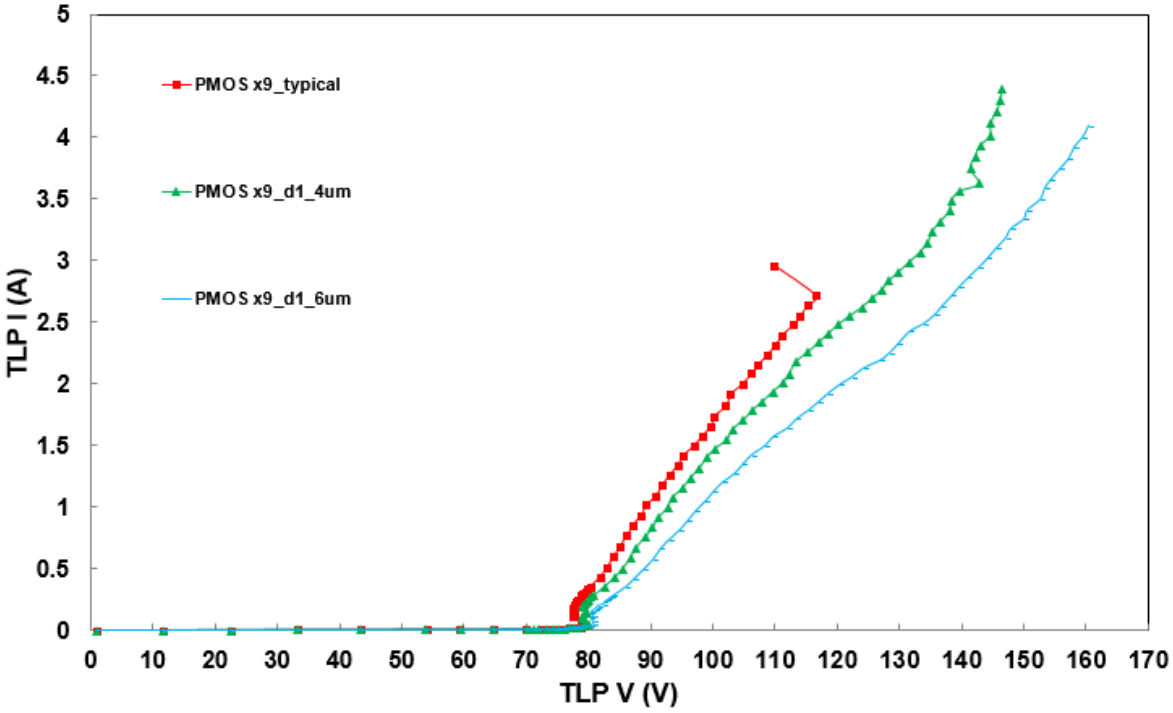
PMOS x8	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
typical	70.56	69.15	2.65	65.2	5	400
no_RPO	70.11	68.24	2.13	65.4	4	300
RPO_0μm	70.75	68.8	2.64	65	5	400
RPO_-0.03 μm	70.68	68.61	2.59	65.2	5	400
RPO_-0.06 μm	70.67	68.91	2.67	65	5	450
d1_4 μm	71.12	70.19	4.31	65	7.5	600
d1_6 μm	71.89	71.61	4.79	65	>8	550
d1_2 μm_co_4	70.79	69.1	3.04	65	5.5	450
d1_4 μm_co_4	71.06	70.36	4.28	65	>8	650
d1_6 μm_co_4	72.57	72.12	4.81	65	>8	550
L_1 μm	70.91	69.51	2.87	65	5.5	450
TW_600 μm	70.57	67.54	4.37	65	>8	650

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The TLP measured I-V curves of 9-PMOSs with different layout parameters splits (RPO, d1, drain contact number, L, and TW) are compared in Fig. 2.33(a) ~ (e).

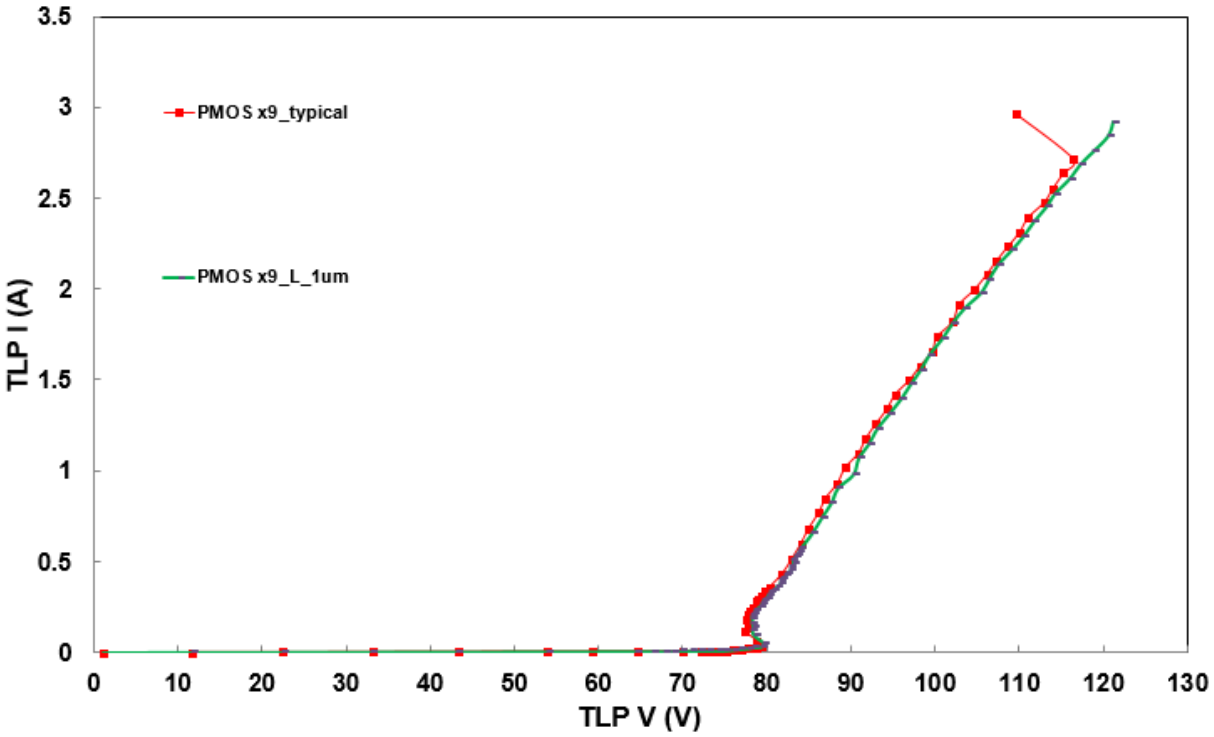


(a)

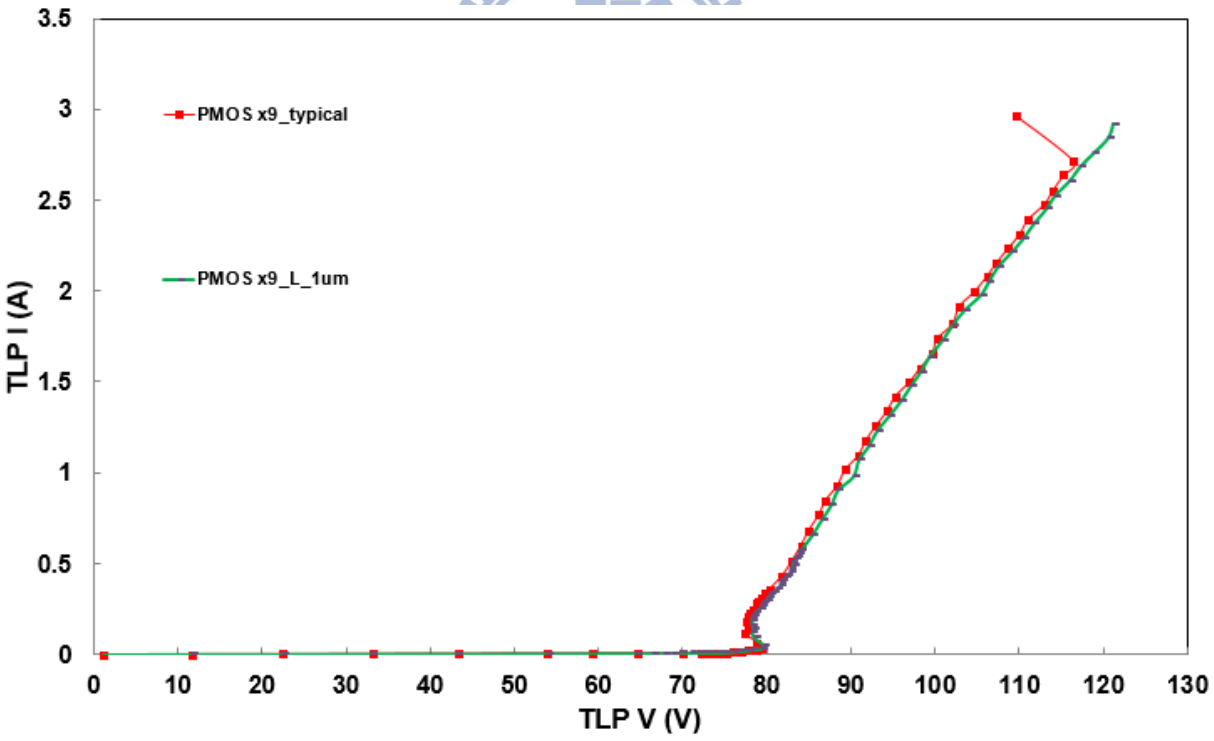


(b)

Fig. 2.33 The TLP measured I-V curves of 9-PMOSs with different (a) RPO splits and (b) d1 splits

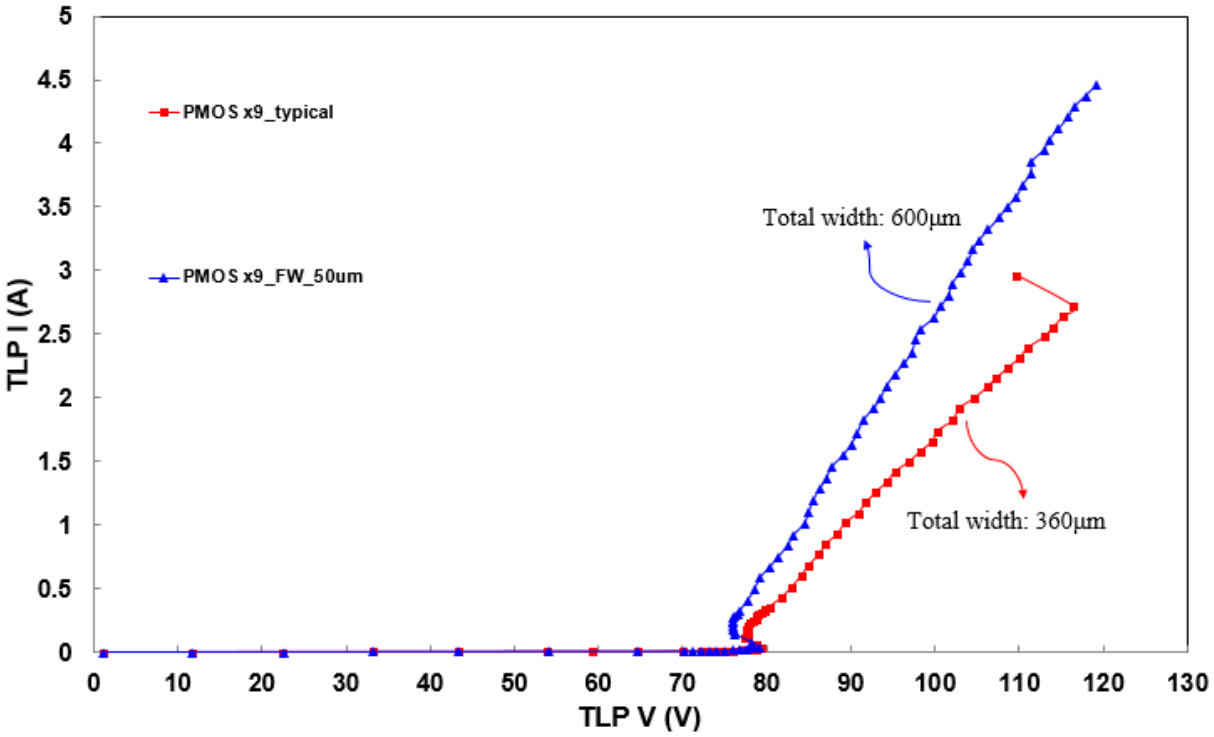


(c)



(d)

Fig. 2.33 The TLP measured I-V curves of 9-PMOSs with different (c) d1 and drain contact number (co) splits and (d) L splits



(e)

Fig. 2.33 The TLP measured I-V curves of 9-PMOSs with different (e) total width splits

The detailed characteristics of 9-PMOSs with different layout parameters are listed in Table 2.27.

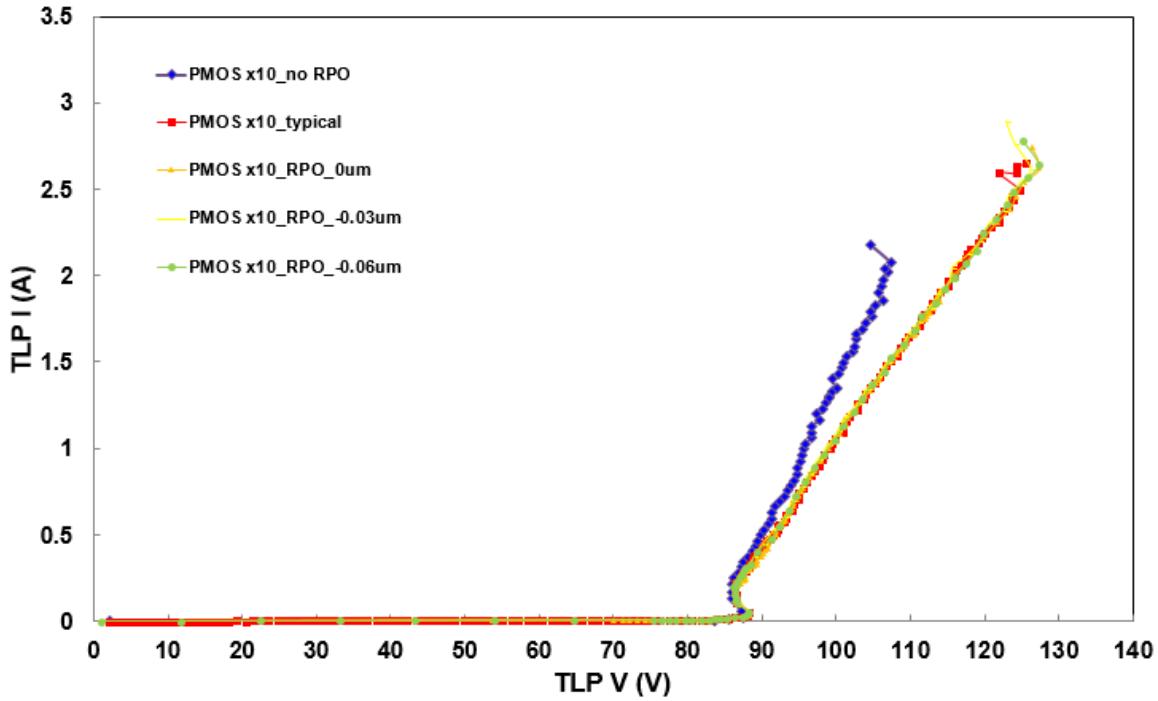
Table 2.27

The measurement data of 9-PMOSs with different layout parameters

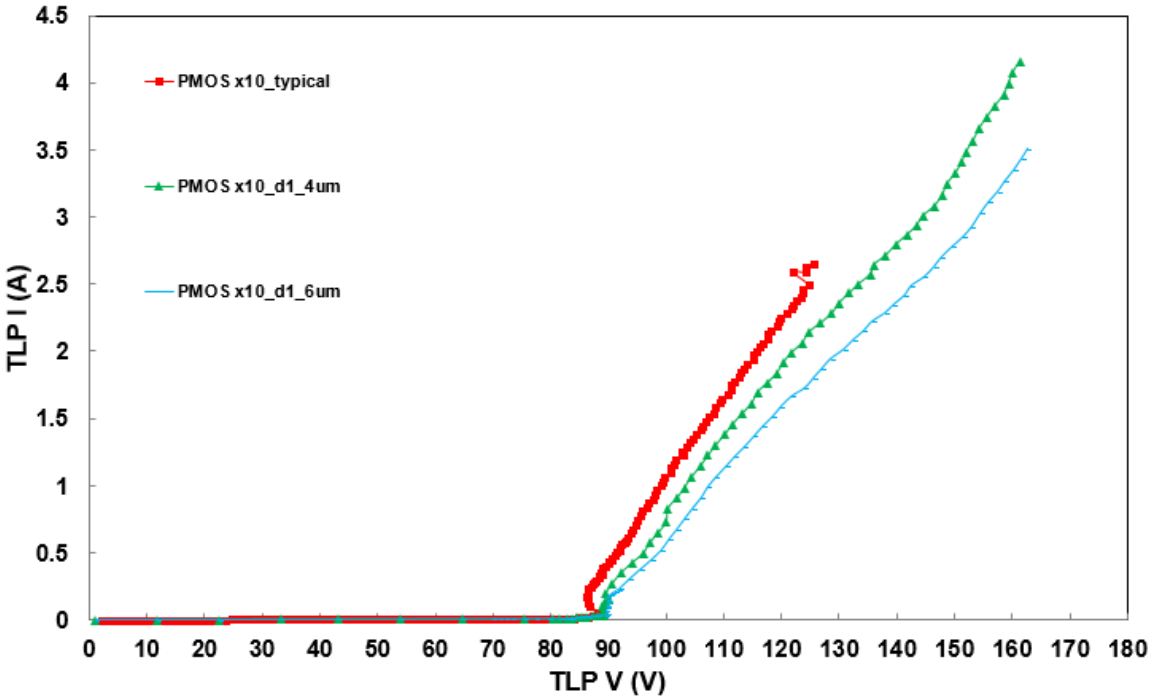
PMOS x9	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
typical	79.37	77.43	2.72	73.2	5	450
no_RPO	80.27	77.83	2.12	74	4	350
RPO_0μm	79.23	77.36	2.46	73.2	5	450
RPO_-0.03 μm	79.4	77.25	2.61	73.2	5	450
RPO_-0.06 μm	79.26	77.3	2.62	73.2	5	450
d1_4 μm	79.98	78.93	4.3	73.2	7.5	550
d1_6 μm	80.81	80.38	4.1	73.2	7	450
d1_2 μm_co_4	79.23	77.25	3.02	73.2	5.5	500
d1_4 μm_co_4	79.97	79.21	4.32	73.2	>8	600
d1_6 μm_co_4	80.85	80.68	4.23	73.2	7.5	500
L_1 μm	79.71	78.28	2.92	73.2	5.5	500
TW_600 μm	79.16	75.89	4.37	73.2	>8	650

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The TLP measured I-V curves of 10-PMOSs with different layout parameters splits (RPO, d1, drain contact number, L, and TW) are compared in Fig. 2.34(a) ~ (e).

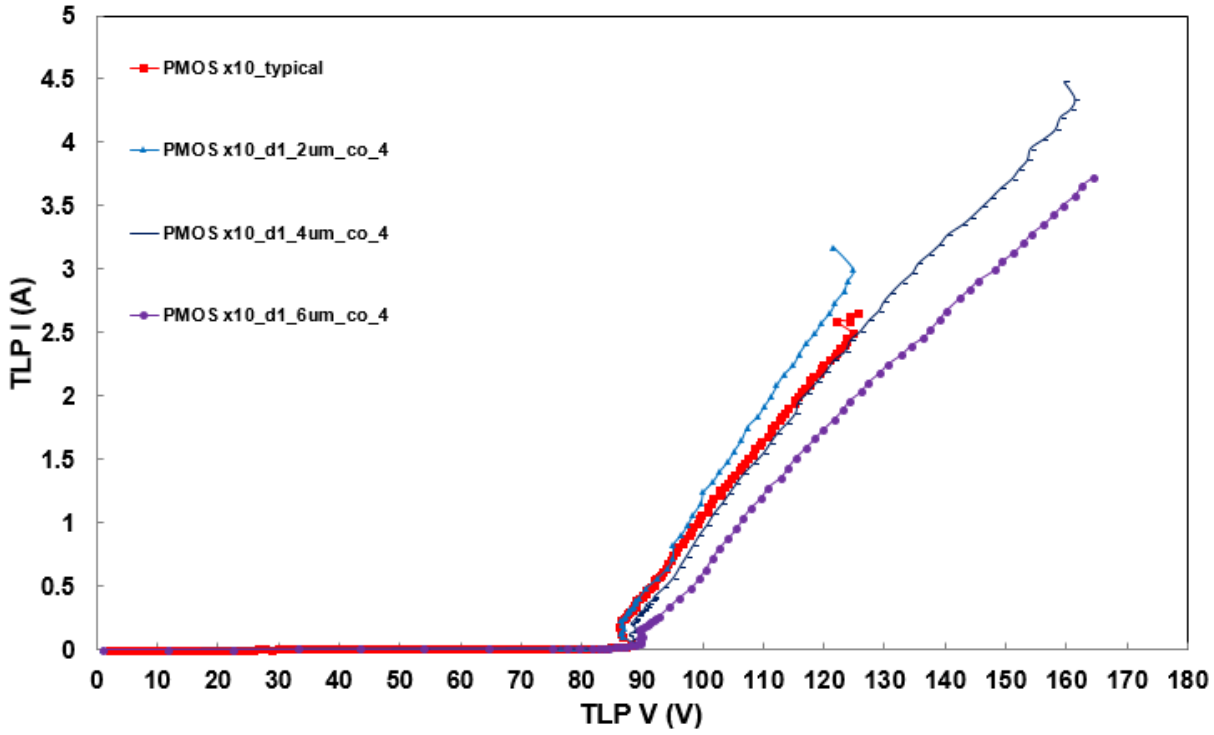


(a)

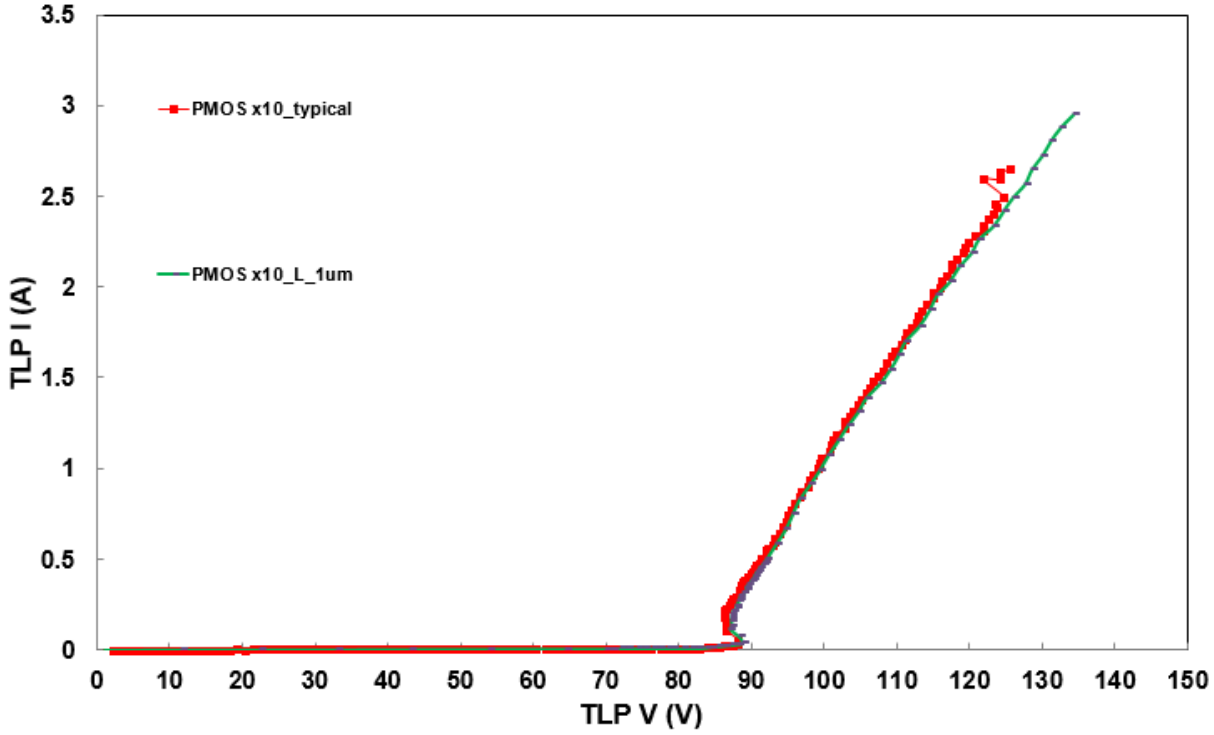


(b)

Fig. 2.34 The TLP measured I-V curves of 10-PMOSs with different (a) RPO splits and (b) d1 splits

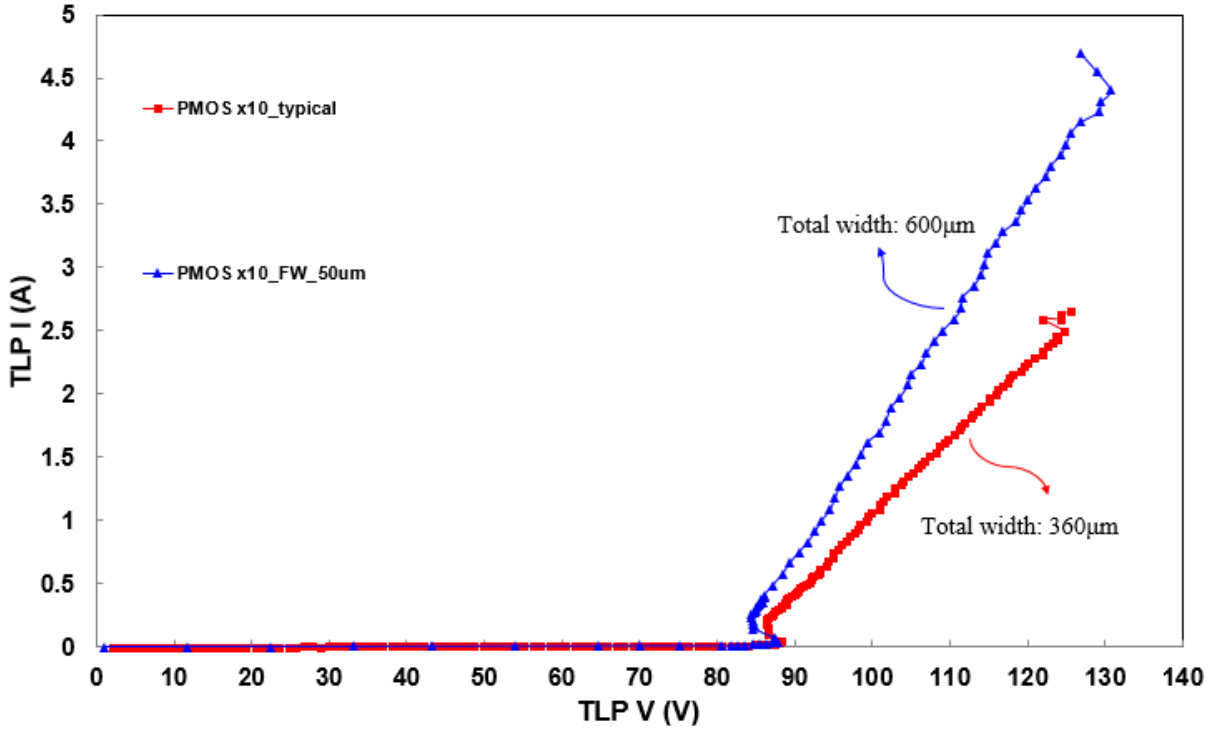


(c)



(d)

Fig. 2.34 The TLP measured I-V curves of 10-PMOSs with different (c) d1 and drain contact number (co) splits and (d) L splits



(e)

Fig. 2.34 The TLP measured I-V curves of 10-PMOSs with different (e) total width splits

The detailed characteristics of 10-PMOSs with different layout parameters are listed in Table 2.28.

Table 2.28

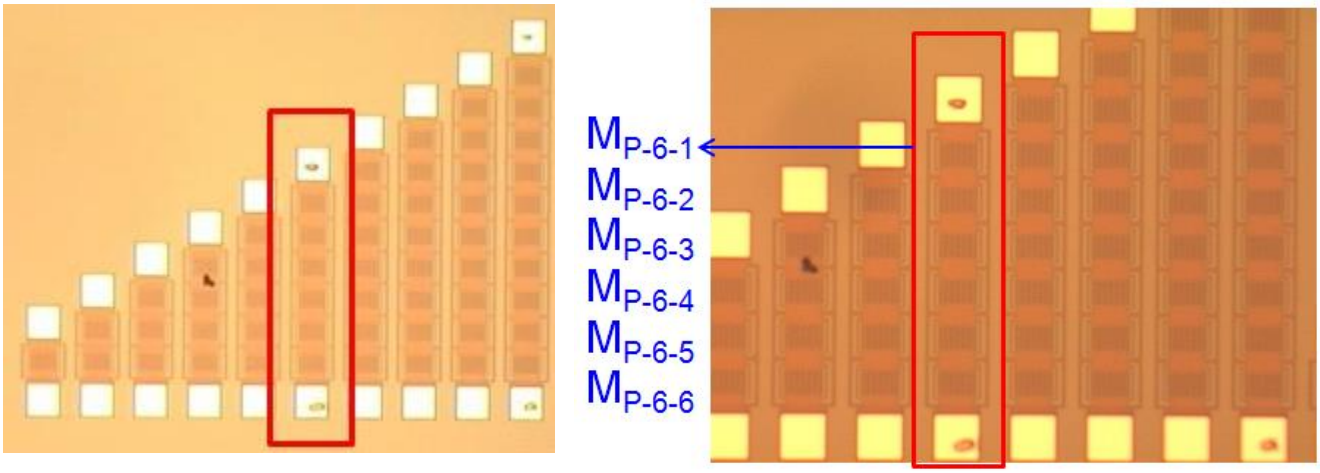
The measurement data of 10-PMOSs with different layout parameters

PMOS x10	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
typical	88.23	86.26	2.63	81.6	5	450
no_RPO	87.46	85.95	2.08	81.8	4	350
RPO_0μm	88.21	86.43	2.46	81.4	5	450
RPO_-0.03 μm	88.25	86.12	2.76	81.4	5	450
RPO_-0.06 μm	88.21	86.08	2.64	81.4	5	450
d1_4 μm	89.26	88.85	4.16	81.4	7.5	500
d1_6 μm	90.11	89.68	3.5	81.4	6	400
d1_2 μm_co_4	88.32	86.32	3	81.4	5.5	500
d1_4 μm_co_4	89.04	87.96	4.35	81.4	>8	550
d1_6 μm_co_4	89.74	89.56	3.66	81.4	6.5	450
L_1 μm	88.89	87.19	2.95	81.4	5.5	500
TW_600 μm	87.86	84.32	4.55	81.4	>8	700

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

From above results with TLP-measured I_{t2} and ESD test, ESD robustness of 9-PMOSs with d1 splits and drain contact number splits has different results. ESD robustness of 10-PMOSs with d1 splits and drain contact number splits also has different results. ESD robustness of stacking number 9 and 10 is lower than that of stacking number from 1 to 8.

The optical microscope (OM) pictures of 6-PMOSs with d1_2μm (typical) are shown in Fig. 2.35 after MM stress. ESD robustness of 6-PMOSs with d1_2μm (typical) can pass 400 V in the machine-model (MM) ESD test, and that failed 450 V in the machine-model (MM) ESD test. The optical microscope (OM) pictures of 6-PMOSs with d1_6μm are shown in Fig. 2.36 after MM stress. ESD robustness of 6-PMOSs with d1_6μm can pass 600 V in the machine-model (MM) ESD test, and that failed 650 V in the machine-model (MM) ESD test. The optical microscope (OM) pictures of 10-PMOSs with d1_2μm (typical) are shown in Fig. 2.37 after MM stress. ESD robustness of 10-PMOSs with d1_2μm (typical) can pass 450 V in the machine-model (MM) ESD test, and that failed 500 V in the machine-model (MM) ESD test. The optical microscope (OM) pictures of 10-PMOSs with d1_6μm are shown in Fig. 2.38 after MM stress. ESD robustness of 10-PMOSs with d1_6μm only pass 400 V in the machine-model (MM) ESD test, and that failed 450 V in the machine-model (MM) ESD test.



(a) (b)

Fig. 2.35 The optical microscope (OM) pictures of 6-PMOSs with d1_2μm after MM stress (a) top view and (b) partial enlarged drawing

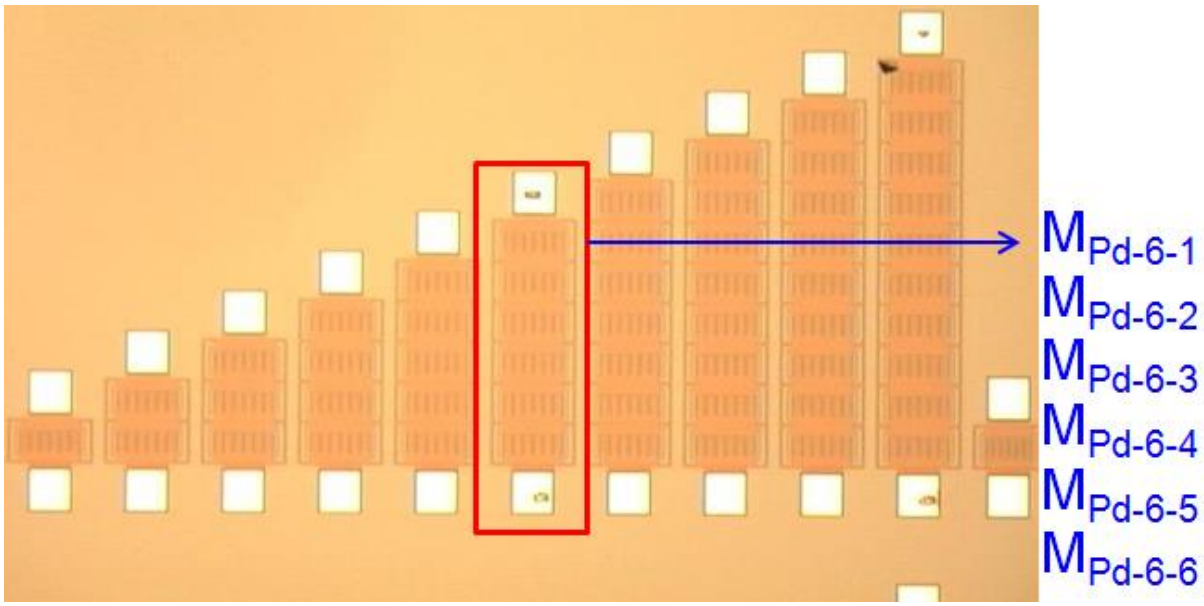


Fig. 2.36 The optical microscope (OM) pictures of 6-PMOSs with d1_6μm after MM stress

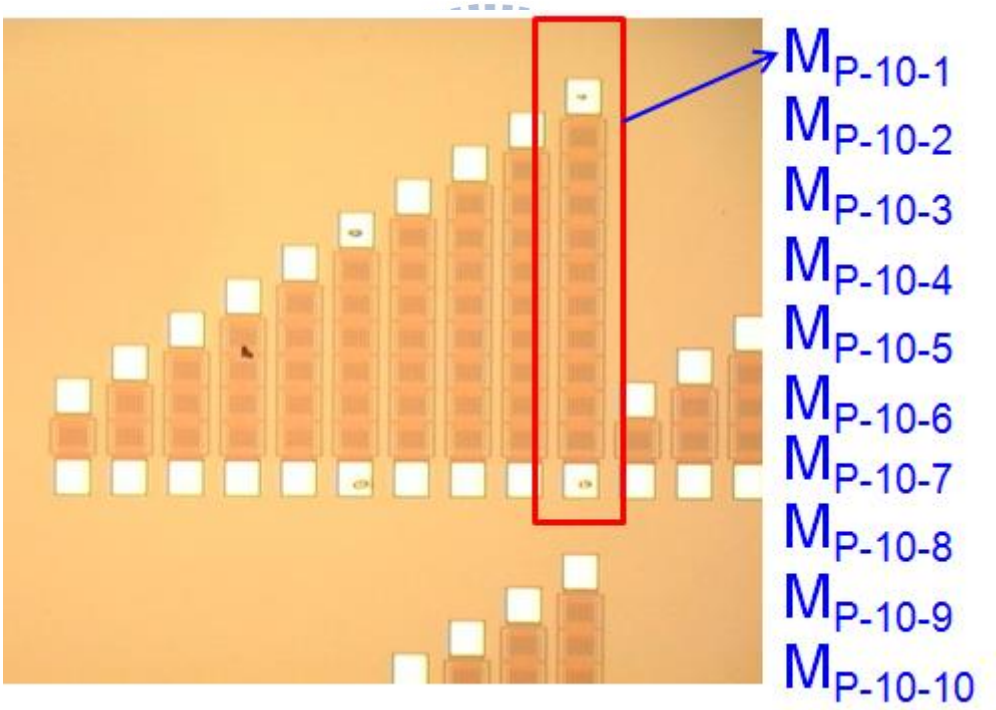


Fig. 2.37 The optical microscope (OM) pictures of 10-PMOSs with d1_2μm after MM stress

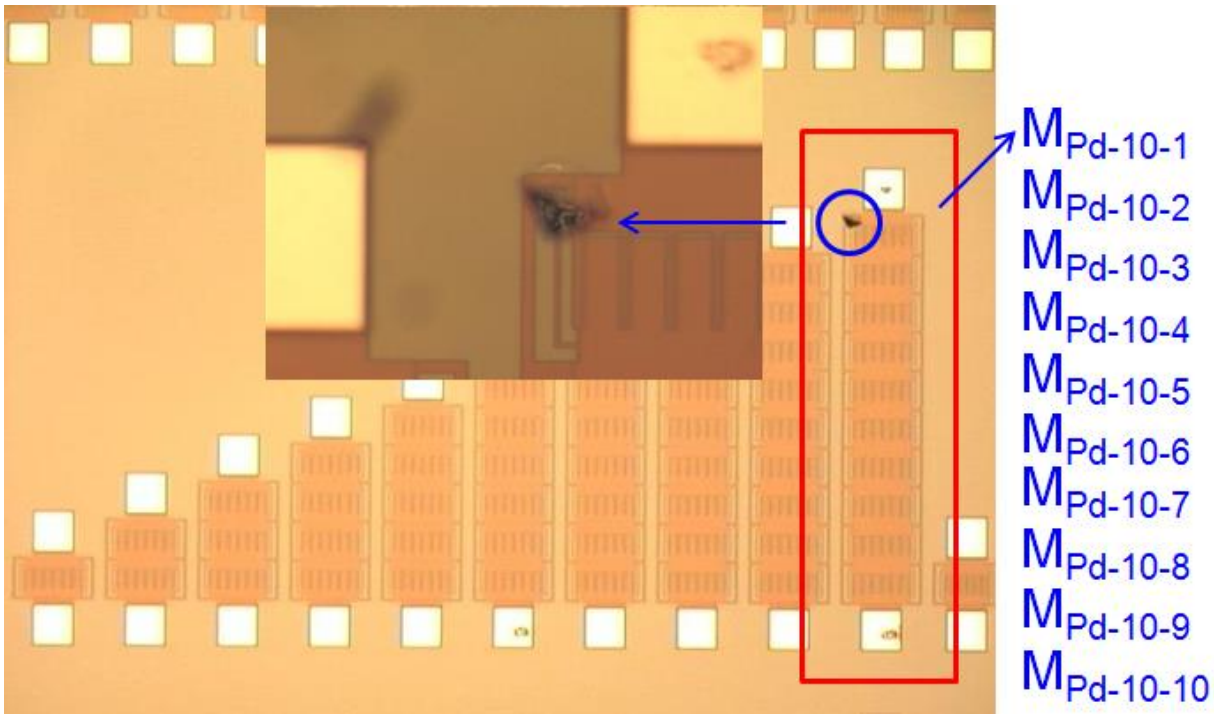


Fig. 2.38 The optical microscope (OM) pictures of 10-PMOSs with d1_6μm after MM stress

From above pictures, the OM pictures of 10-PMOSs with d1_6μm after MM stress can directly clear to see the failure position, but other OM pictures can't. After delayer to substrate, ESD failure positions of stacked PMOS structure can be seen directly.

The names of 6-PMOSs with d1_2μm are M_{P-6-1}, M_{P-6-2}, M_{P-6-3}, M_{P-6-4}, M_{P-6-5}, M_{P-6-6} from top to bottom, respectively. The names of 10-PMOSs with d1_2μm are M_{P-10-1}, M_{P-10-2}, M_{P-10-3}, M_{P-10-4}, M_{P-10-5}, M_{P-10-6}, M_{P-10-7}, M_{P-10-8}, M_{P-10-9}, $M_{P-10-10}$ from top to bottom, respectively.

The names of 6-PMOSs with d1_6μm are M_{Pd-6-1}, M_{Pd-6-2}, M_{Pd-6-3}, M_{Pd-6-4}, M_{Pd-6-5}, M_{Pd-6-6} from top to bottom, respectively. The names of 10-PMOSs with d1_6μm are M_{P-10-1}, M_{P-10-2}, $M_{Pd-10-3}$, $M_{Pd-10-4}$, $M_{Pd-10-5}$, $M_{Pd-10-6}$, $M_{Pd-10-7}$, $M_{Pd-10-8}$, $M_{Pd-10-9}$, $M_{Pd-10-10}$ from top to bottom, respectively.

The optical microscope (OM) pictures of 10-PMOSs with d1_2μm (typical) are shown in Fig. 2.39 after delayer to substrate.

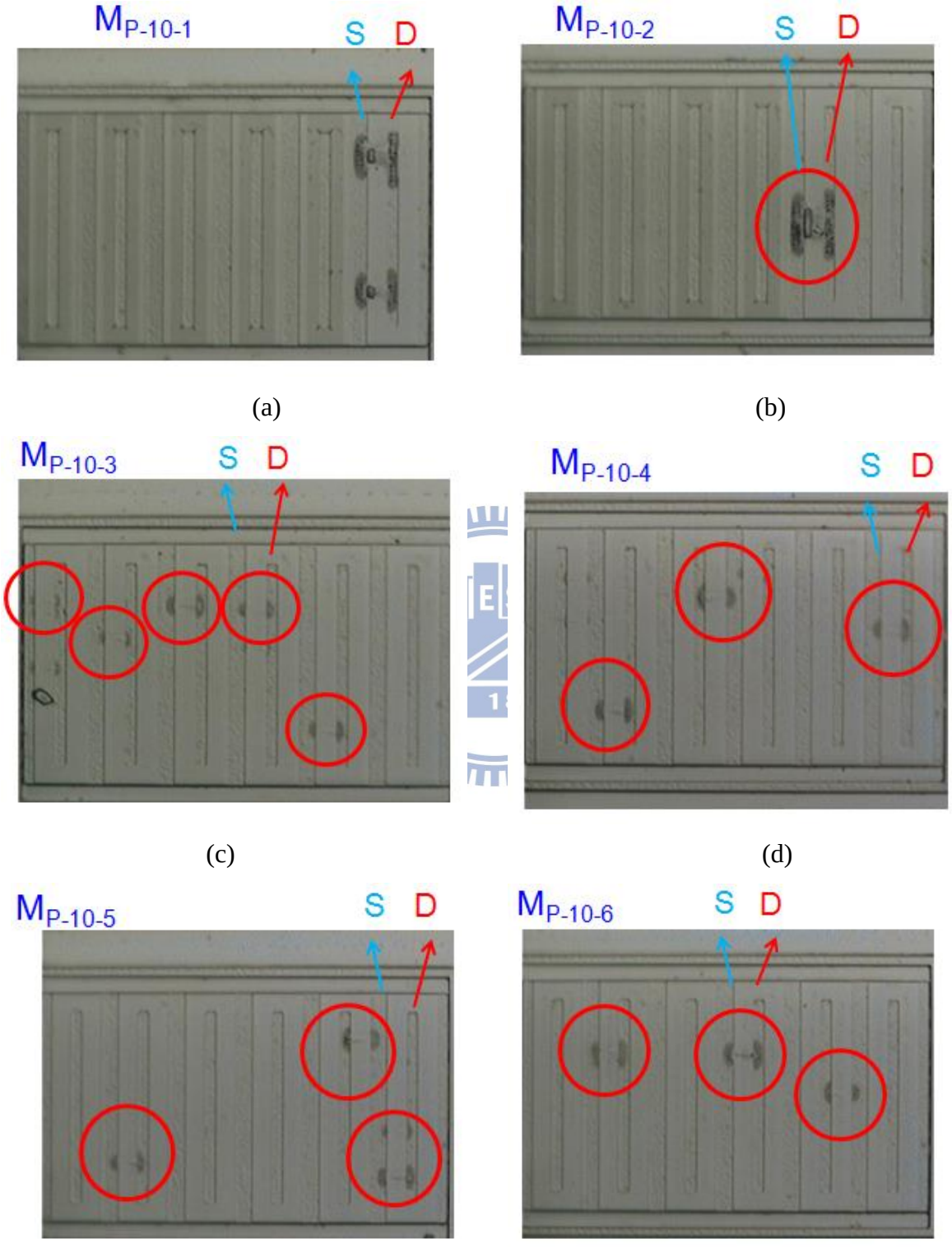
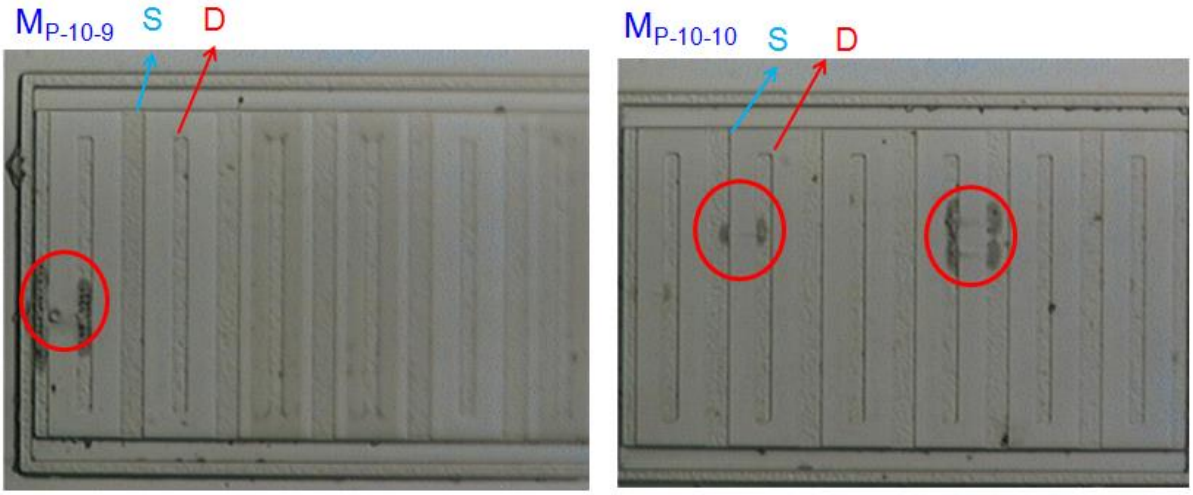


Fig. 2.39 The OM pictures of 10-PMOSs with d1_2μm (typical) after delayer to substrate (a) M_{P-10-1}, (b) M_{P-10-2}, (c) M_{P-10-3}, (d) M_{P-10-4} (e) M_{P-10-5}, and (f) M_{P-10-6}

(g) (h)



(i) (j)

Fig. 2.39 The OM pictures of 10-PMOSs with d1_2μm (typical) after delayer to substrate (g) $M_{P\text{-}10\text{-}7}$, (h) $M_{P\text{-}10\text{-}8}$, (i) $M_{P\text{-}10\text{-}9}$, and (j) $M_{P\text{-}10\text{-}10}$

From Fig. 2.39, every PMOS of 10-PMOSs with d1_2μm (typical) can clear to see failure positions after delayer to substrate. It proves the ESD current gets through every stacked parasitic PNP under ESD stress, and every PMOS can turns on uniformity.

The optical microscope (OM) pictures of 6-PMOSs with d1_6μm are shown in Fig. 2.40 after delayer to substrate. The optical microscope (OM) pictures of 10-PMOSs with d1_6μm

are shown in Fig. 2.41 after delayer to substrate. The scanning electron microscope (SEM) pictures of 10-PMOSs with d1_6μm are shown in Fig. 2.42 after delayer to substrate.

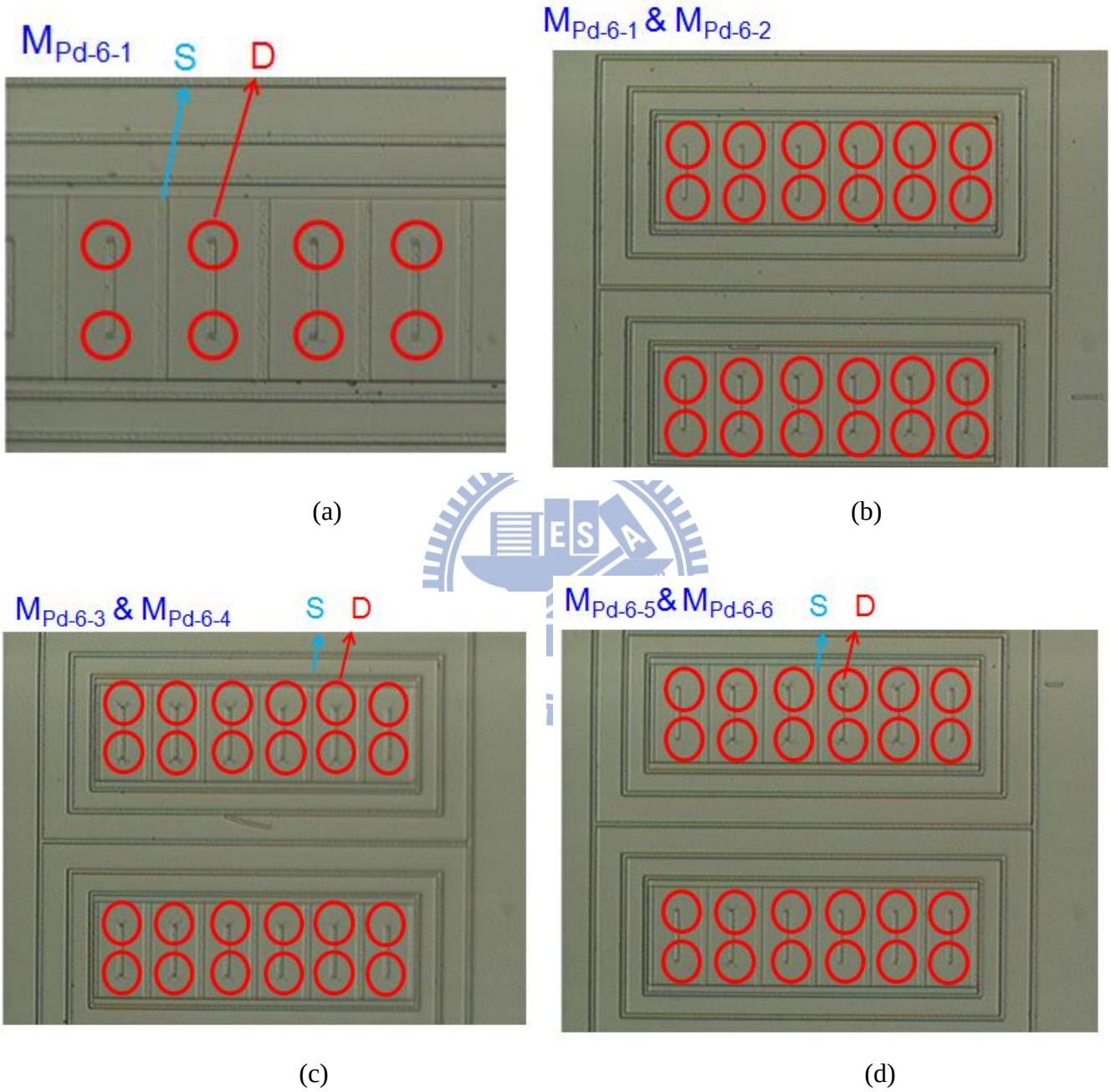


Fig. 2.40 The OM pictures of 6-PMOSs with d1_6μm after delayer to substrate (a) M_{Pd-6-1}, (b) M_{Pd-6-1} & M_{Pd-6-2}, (c) M_{Pd-6-3} & M_{Pd-6-4}, and (d) M_{Pd-6-5} & M_{Pd-6-6}

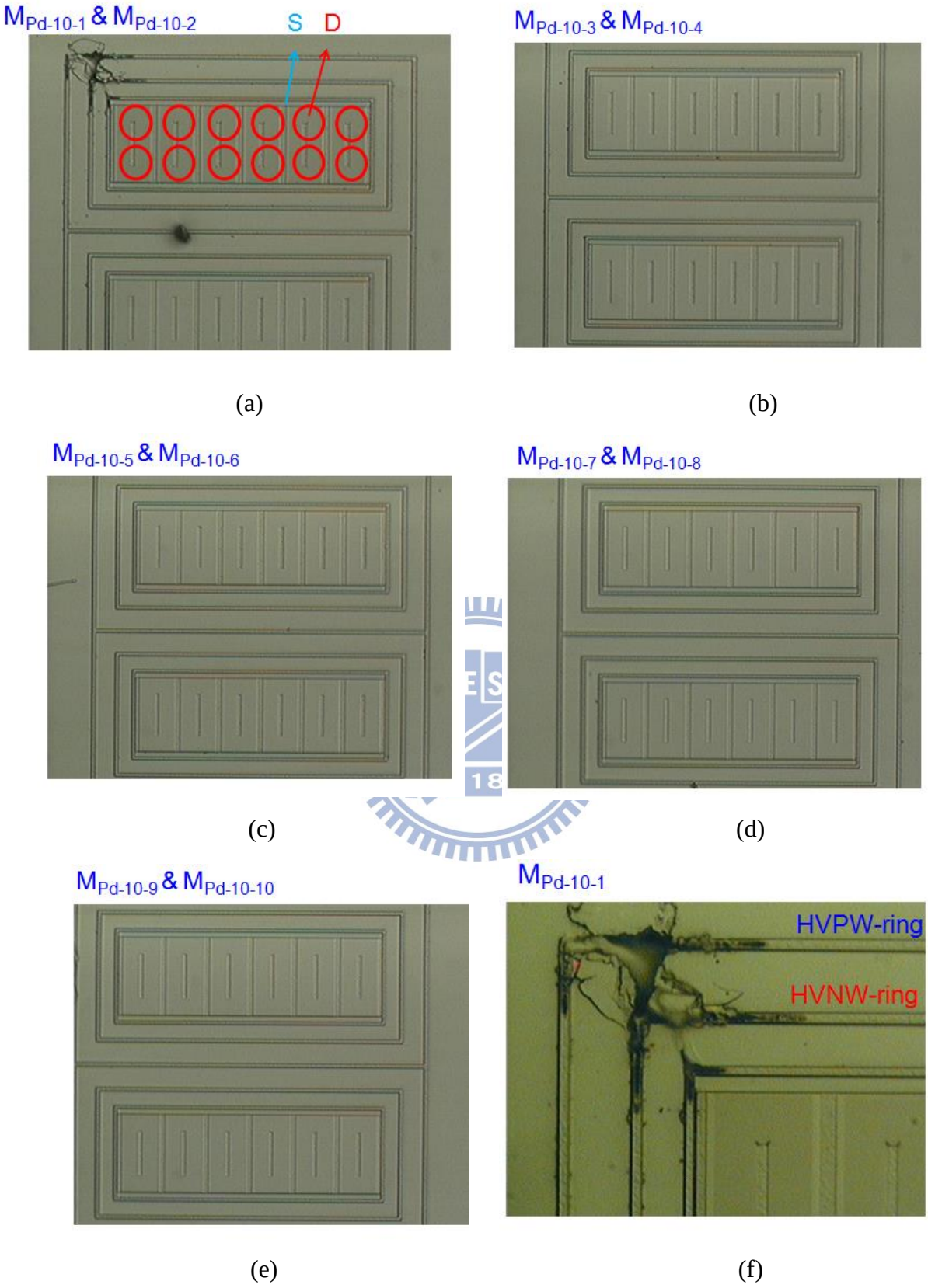
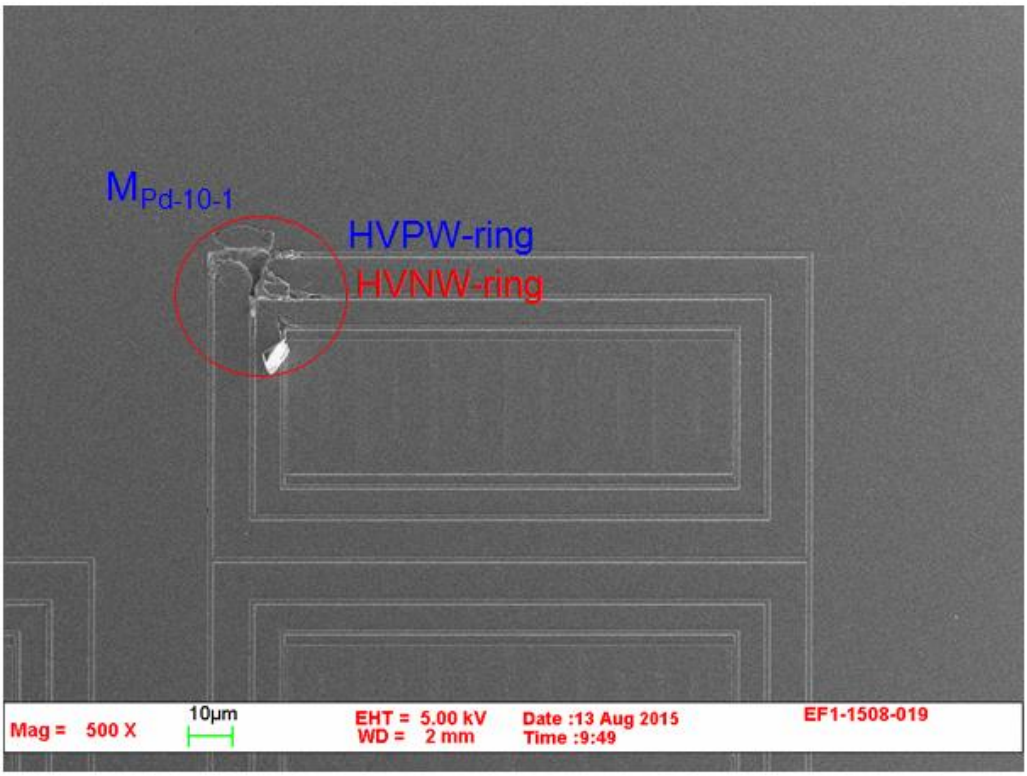
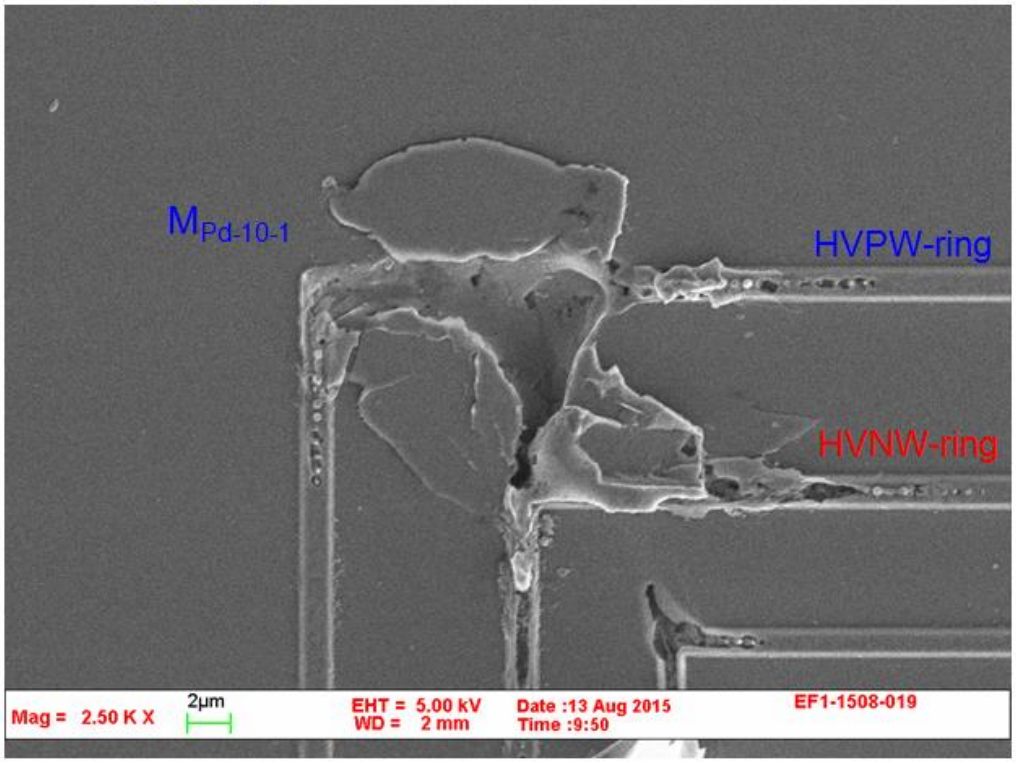


Fig. 2.41 The OM pictures of 10-PMOSs with d1_6μm after delayer to substrate (a) $M_{Pd-10-1}$ & $M_{Pd-10-2}$, (b) $M_{Pd-10-3}$ & $M_{Pd-10-4}$, (c) $M_{Pd-10-5}$ & $M_{Pd-10-6}$, (d) $M_{Pd-10-7}$ & $M_{Pd-10-8}$, (e) $M_{Pd-10-9}$ & $M_{Pd-10-10}$, and (f) the edge of $M_{Pd-10-1}$



(a)



(b)

Fig. 2.42 The SEM pictures of 10-PMOSs with d1_6μm after delayer to substrate (a) $M_{Pd-10-1}$, (b) the edge of $M_{Pd-10-1}$

From Fig. 2.40, every PMOS of 6-PMOSs with d1_6μm can see failure positions after delayer to substrate. It proves the ESD current also gets through every stacked parasitic PNP under ESD stress, and every PMOS can turns on uniformity. Due to the spacing of d1 become wider, and the parasitic PNPs path become longer. Instead of getting through stacked parasitic PNPs, the ESD current unpredictably gets through the parasitic path from P+ diffusion (drain) to HVNW-ring. From Fig. 2.41 and Fig. 2.42, the ESD failure positions located on the top of 10-PMOSs. For the experiment results, the 9-PMOSs and 10-PMOSs with d1_6μm are not good options.

2.3 Summary

Optimization of stacked LV PMOS for high-voltage ESD protection needs to notice layout consideration. From above results, stacked PMOSs with larger d1 have good ESD robustness in 0.5-μm and 0.25-μm. However, 9-PMOSs and 10-PMOSs with larger d1 got lower ESD robustness due to the parasitic path from P+ diffusion (drain) to HVNW-ring damage. From above results, layout optimization for stacked LV PMOSs (1-PMOS to 8-PMOSs) to get higher ESD robustness: d1_6 μm and TW_600 μm. From above results, layout optimization for stacked LV PMOSs (9-PMOS and 10-PMOSs) to get higher ESD robustness: d1_4 μm and TW_600 μm. The holding voltages of stacked LV PMOS with different guard-ring layout have some different. The guard-ring layout on the stacked LV PMOS devices was further investigated in next chapter.

Chapter 3

Impact of Guard Ring Layout on the Stacked Low-Voltage PMOS for High-Voltage ESD Protection

PMOS is a non-snapback device, and it is a good choice for latchup-free design. In this chapter, Stacked PMOSs with different guard ring layouts have been investigated in a 0.5-μm HV process for HV applications. The holding voltages of stacked PMOSs with different guard ring layouts have been investigated by TLP systems with different pulse widths and the curve tracer. In addition, stacked PMOSs with different guard ring layouts have been investigated to save layout area in a 0.25-μm BCD process for HV applications.

3.1 Stacked Low-Voltage PMOS with Different Guard Ring Layout in a 0.5-μm HV Process

3.1.1 Test Devices

The ESD devices should be surrounded by the guard ring in real circuit application. The ESD device without the guard ring can reduce the layout area, but it might cause the latchup issue under the normal circuit operation. Therefore, the on-chip ESD devices were often surrounded by the guard ring to prevent latchup issue in the IC products.

In this work, the stacked LV PMOSs with two or three stacking numbers for HV applications were fabricated and verified in the silicon chip. Especially, different guard ring layouts on the stacked PMOSs were investigated to study its impact to ESD protection performance. The transmission line pulse (TLP) and ESD tester are used to verify the stacked

PMOSs with different guard ring layouts for HV applications.

The test structures of stacked PMOSs with different stacking numbers and layout arrangements were fabricated in a 0.5-μm high-voltage process. The stacked LV PMOSs with two and three stacking numbers are investigated in this work, which are designed to meet 20-V and 30-V HV applications. Each LV PMOS in the stacked configuration is drawn with the total channel width of 800μm and a channel length of 0.5μm.

There are four types (type A, type B, type C, and type D) of the guard ring layouts to surround the stacked PMOSs, as shown in Fig. 3.1, where 3-PMOSs stacked structure is demonstrated. In type A, the stacked PMOSs were not surrounded by P-ring, which is used as the base line for reference. In type B and type C, the stacked PMOSs were surrounded by one P-ring that is typically connected to cathode. The NWELL spacing between each N-well in the type B (type C) is 4μm (8μm). In type D, each PMOS in the N-well of the 3-PMOSs stacked structure was fully surrounded by the P-ring. The clearance of P-ring to the N-well edge is kept at 2.7μm, which is a layout rule specified by the foundry in the given 0.5-μm process.

The cross-sectional view of stacked structure with two LV PMOSs is shown in Fig. 3.2. The cross-sectional view of the stacked PMOSs without surrounded by P-ring is shown in Fig. 3.2(a). The NWELL spacings of the two LV PMOSs are drawn with 4μm and 8μm in Fig. 3.2(b) and Fig. 3.2(c), respectively. The cross-sectional view of the stacked PMOSs with inserted p-ring to surround each LV PMOS is shown in Fig. 3.2(d). The gate of each PMOS is connected to its local high potential point, so each PMOS in the stacked structure is kept in the off state during the normal circuit operation. The P+ diffusion (drain) of the bottom PMOS in the stacked PMOSs is connected to the cathode. The P-ring is connected to the cathode, which is typically biased at ground with the common p-substrate. If the deep N-Well is provided in the process, the P-ring can be isolated to the common substrate.

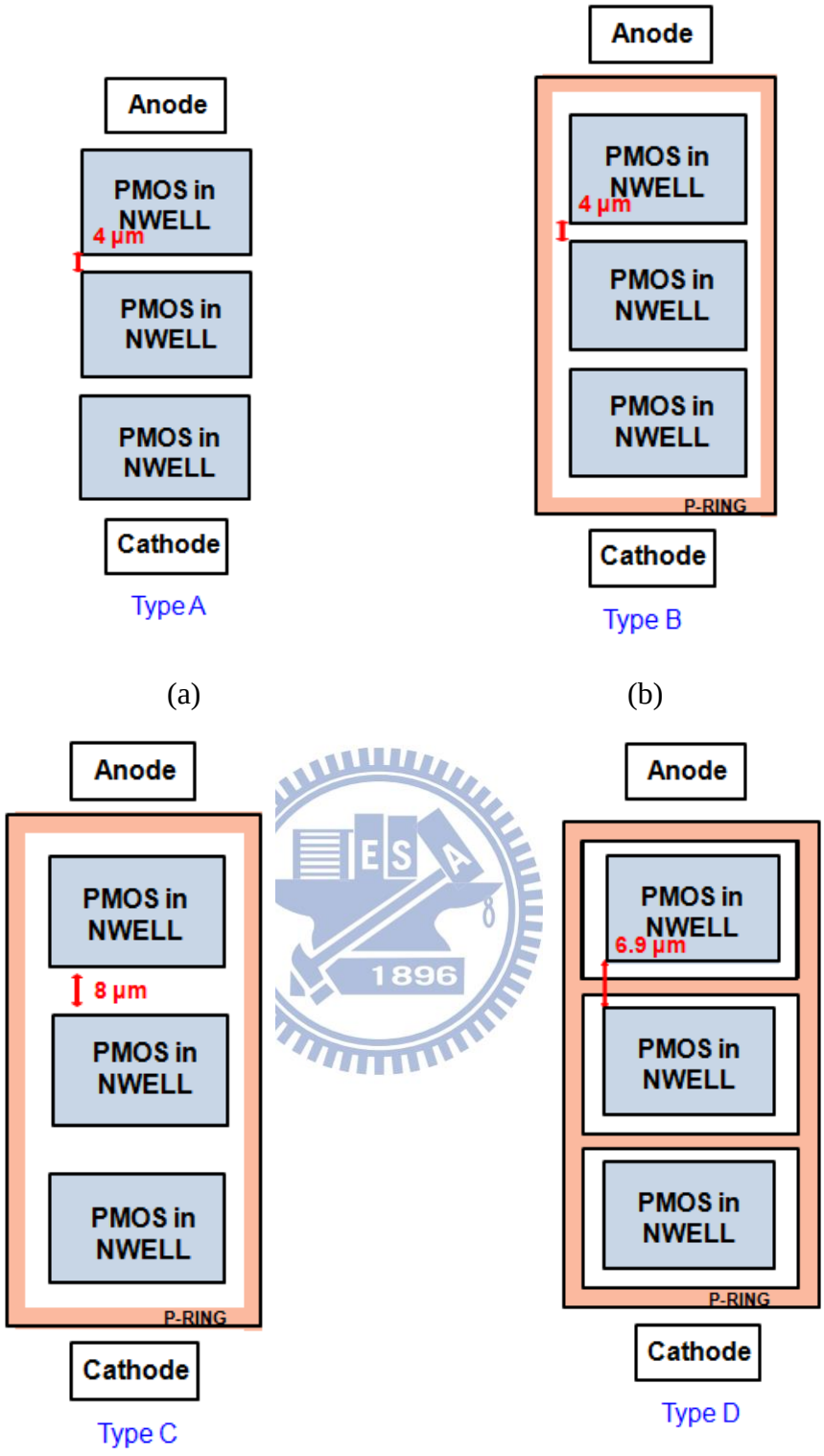
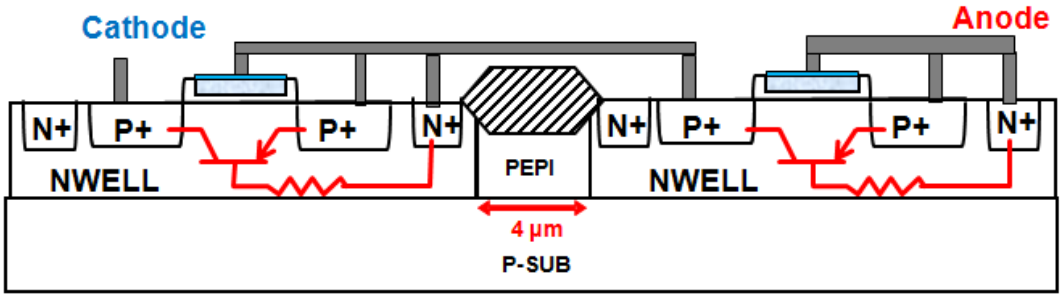
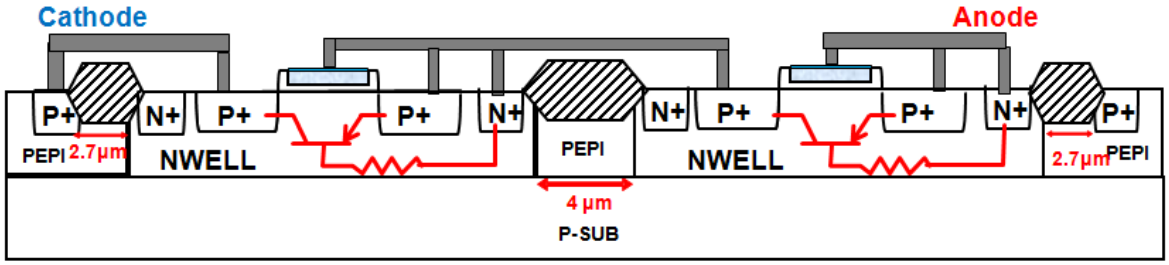


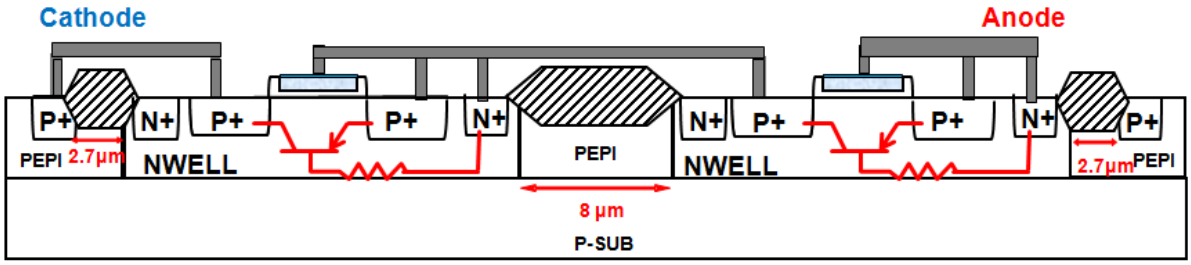
Fig. 3.1 The four types of guard-ring layout for 3-PMOSs stacked structure, (a) without p-ring, (b) with one whole p-ring and NWELL spacing of 4µm, (c) with one whole p-ring and NWELL spacing of 8µm, and (d) with inserted p-ring to surround each LV PMOS



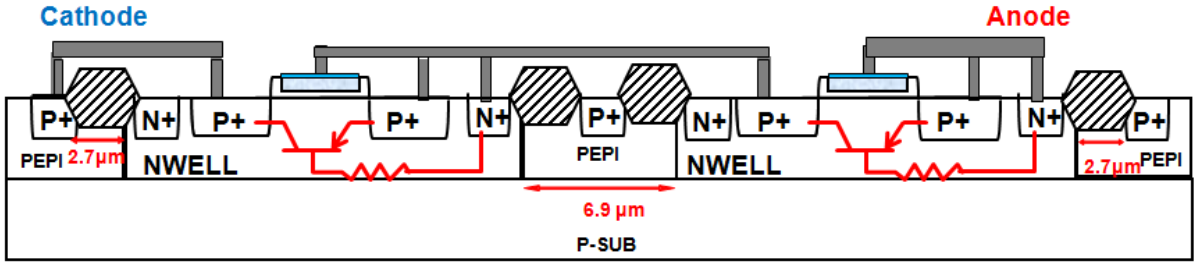
(a)



(b)



(c)



(d)

Fig. 3.2 The cross-sectional views of stacked structure with two LV PMOSs drawn with (a) without p-ring, (b) the NWELL spacing of 4μm, (c) the NWELL spacing of 8μm, and (d) with inserted p-ring to surround each LV PMOS. Each LV PMOS has its own separated N-well in the stacked structure

3.1.2 Experimental Results

All test devices of stacked PMOSs had been fabricated in a 0.5-μm HV process. Each PMOS in all stacked structure is drawn with a channel width of 800μm and a channel length of 0.5μm. Every layout type has 2-PMOSs and 3-PMOSs stacked structures. The 100-ns TLP-measured I-V characteristics of two stacked PMOSs with the four types of guard ring layout are shown in Fig. 3.3.

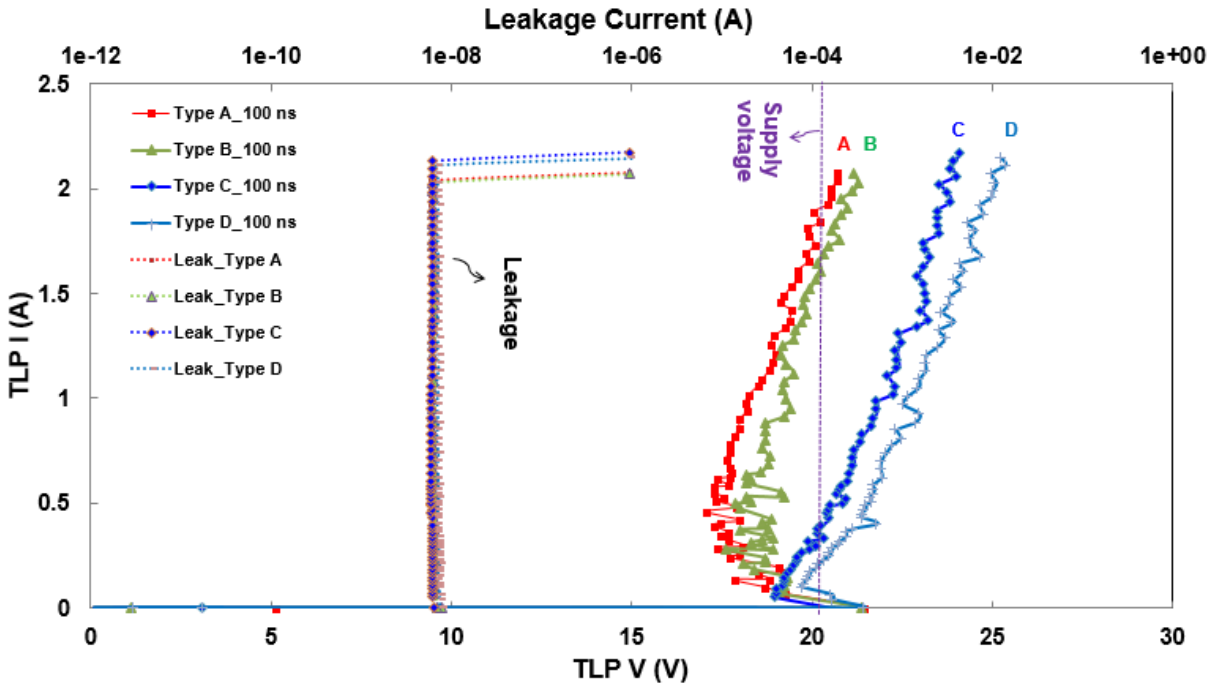


Fig. 3.3 The TLP-measured I-V characteristics of 2-PMOSs with different guard-ring layouts

In Fig. 3.3, the holding voltage of 2-PMOSs stacked structure is two times of the holding voltage of single PMOS. The trigger voltage of 2-PMOSs stacked structure is also double of the trigger voltage of single PMOS in TLP measurement. In Fig. 3.3, the trigger voltages of the 2-PMOSs stacked structure with different guard-ring layouts are almost the same, but the holding voltage of type A is smaller than those of other types. Type B is better than type A, because it adds one guard ring to surround itself. The holding voltage of type B still suffers

latchup risk for 20V application. The holding voltages of type C and type D are better (higher) than that of type A and type B, and they can achieve latchup-free design for 20V application. However, the layout area of type D is smaller than the layout area of type C, as well as the type D has the best I_{t2} among all guard-ring types.

The detailed characteristics of 2-PMOSs stacked structure with different guard-ring types are listed in Table 3.1. The breakdown voltages of type C and type D are almost the same as those of type A and type B in DC measurement. All of 2-PMOSs stacked structure with different guard-ring types can pass 3.5 kV in the human-body-model (HBM) ESD test and 250 V in the machine-model (MM) ESD test.

Table 3.1
Summary of 2-PMOSs stacked structure with different guard-ring types

2-PMOSs Stacked Structure	TLP (100-ns)			DC (#)	ESD Level (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
Type A	21.48	17.09	2.04	22.3	3.5	250
Type B	21.43	17.6	2.03	22.3	3.5	250
Type C	20.48	19.02	2.13	22.6	3.5	250
Type D	21.47	19.69	2.11	22.6	3.5	250

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The TLP-measured I-V characteristics of three stacked PMOSs with the four types of guard ring layout are shown in Fig. 3.4. As seen in Fig. 3.4, the trigger voltage of 3-PMOSs stacked structure is triple of the trigger voltage of single PMOS. In Fig. 3.4, the trigger

voltages in different guard-ring types are almost the same, but the holding voltage of type A is still the smallest among the four types of guard ring layout. Type A and type B would suffer latchup risk for 30V high voltage application. The holding voltages of type C and type D are better (higher) than those of type A and type B, which can achieve latchup-free design for 30V application. The total layout area of type D is also smaller than that of type C, as well as the type D has the best I_{t2} among the four guard-ring types.

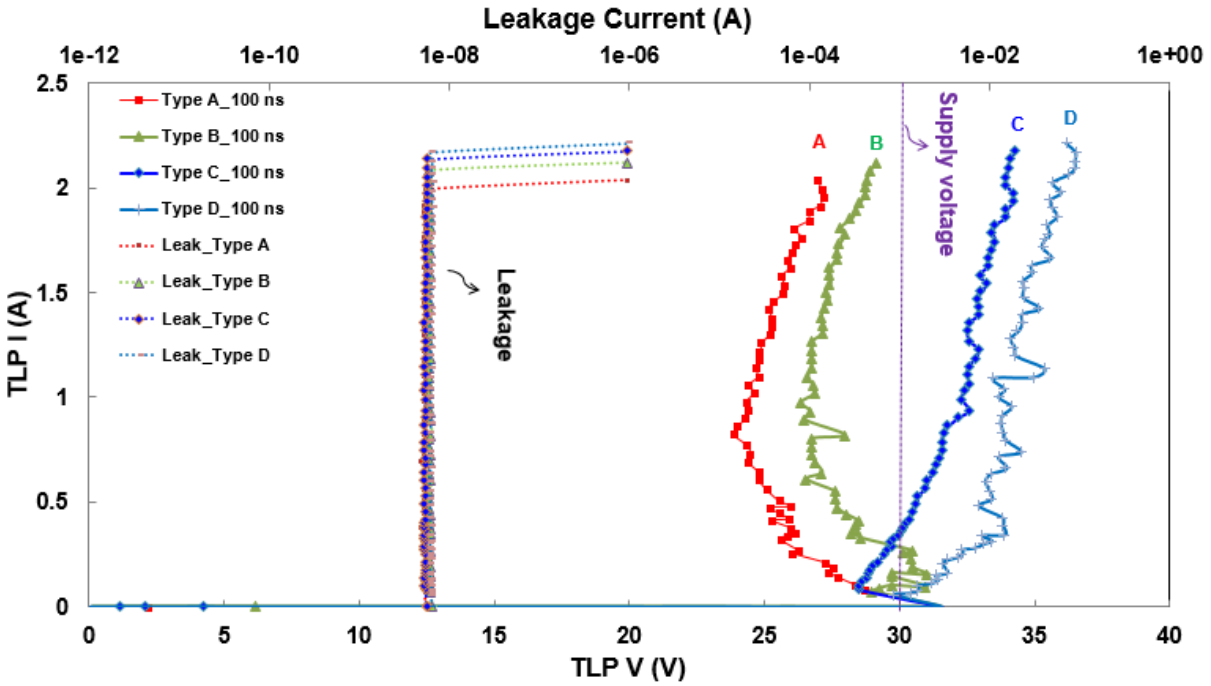


Fig. 3.4 The TLP-measured I-V characteristics of 3-PMOSs with different guard-ring layouts

The detailed characteristics of 3-PMOSs stacked structure with different guard-ring types are listed in Table 3.2. The breakdown voltages of all guard-ring types almost have the same value. The MM ESD level (300V) of type C and type D are better than that (250V) of type A and type B. Except type A, all layout types of 3-PMOSs stacked structure can pass 3.5 kV in the HBM ESD test.

Table 3.2

Summary of 3-PMOSs stacked structure with different guard-ring types

3-PMOSs Stacked Structure	TLP (100-ns)			DC (#)	ESD Level (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
Type A	31.58	23.87	1.99	30.7	3	250
Type B	31.53	26.34	2.08	30.5	3.5	250
Type C	31.56	28.47	2.14	30.7	3.5	300
Type D	31.58	29.84	2.17	30.7	3.5	300

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

From above results with 100-ns TLP-measured I_{t2} and ESD test, the type D among the four types of guard-ring layout is the best choice for the stacked PMOSs structure for HV ESD protection. The TLP-measured I-V characteristics of the stacked 2-PMOSs and 3-PMOSs with the guard-ring layout of type D are compared in Fig. 3.5. As seen in Fig. 3.5, the holding voltage can be linearly increased in the PMOSs stacked structure by adjusting the stacking number. The trigger voltage can also be linearly increased in the PMOSs stacked structure. Moreover, the I_{t2} of PMOSs stacked structure with different stacking numbers can be kept almost the same. Different stacking numbers on the stacked PMOSs can be adjusted for various HV applications to achieve latchup-free immunity on the ESD protection device.

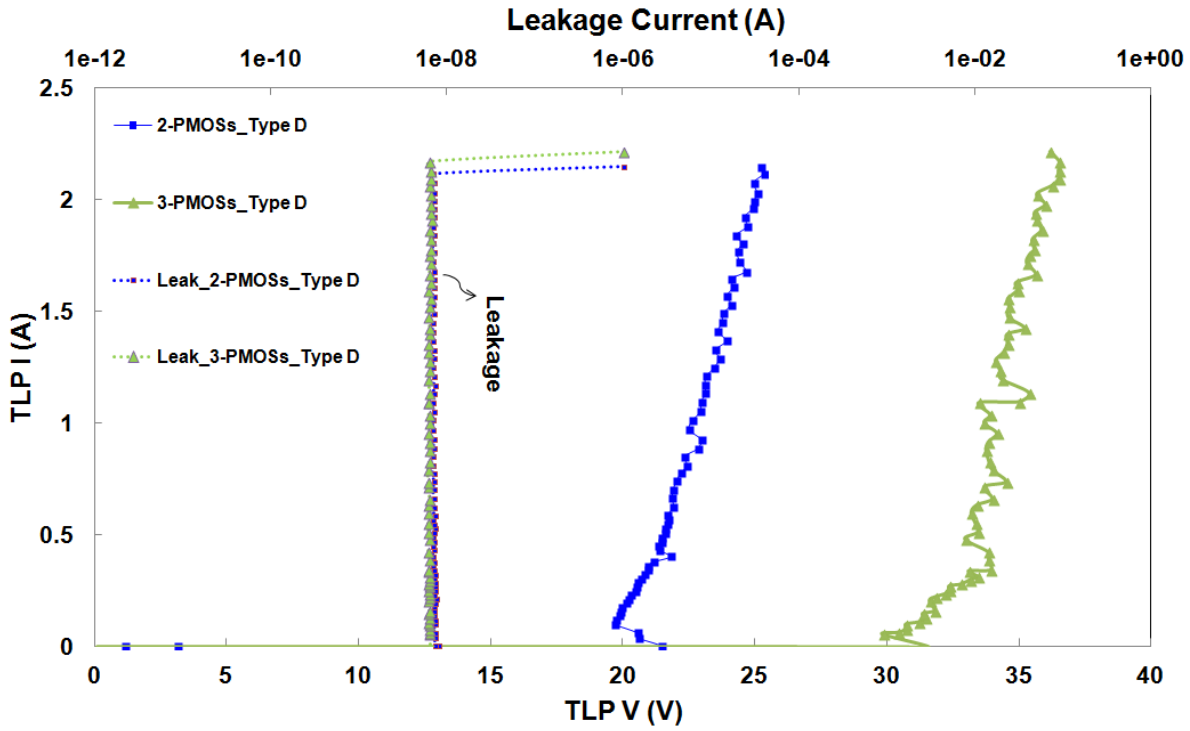


Fig. 3.5 The TLP-measured I-V characteristics of the stacked 2-PMOSs and 3-PMOSs with the guard-ring layout of type D

3.2 Different Guard Ring Layout of Stacked Low-Voltage PMOS measured by TLP with different pulse widths in a 0.5-μm HV Process

3.2.1 Different TLP Pulse Widths

The test devices were all the same in chap3.1. There are four types (type A, type B, type C, and type D) of the guard ring layouts to surround the stacked PMOSs. From above results, the stacked PMOSs with guard-ring layout of type D can achieve both of good ESD robustness and high latchup-free immunity with reasonable total layout area. Furthermore, the test devices measured by 100-ns, 200-ns, 500-ns, 800-ns TLP systems, and curve tracer. In this work, the stacked LV PMOSs with two or three stacking numbers for HV applications were fabricated and verified in the silicon chip. Especially, different TLP pulse widths on the stacked PMOSs were investigated to study its impact to the holding voltages of the stacked PMOSs with different guard ring layouts.

3.2.2 Experiment Results

The 100-ns TLP-measured I-V characteristics of 2-PMOSs with the four types of guard ring layout are shown in Fig. 3.6. The detailed characteristics of 2-PMOSs stacked structure with different guard-ring types are listed in Table 3.3.

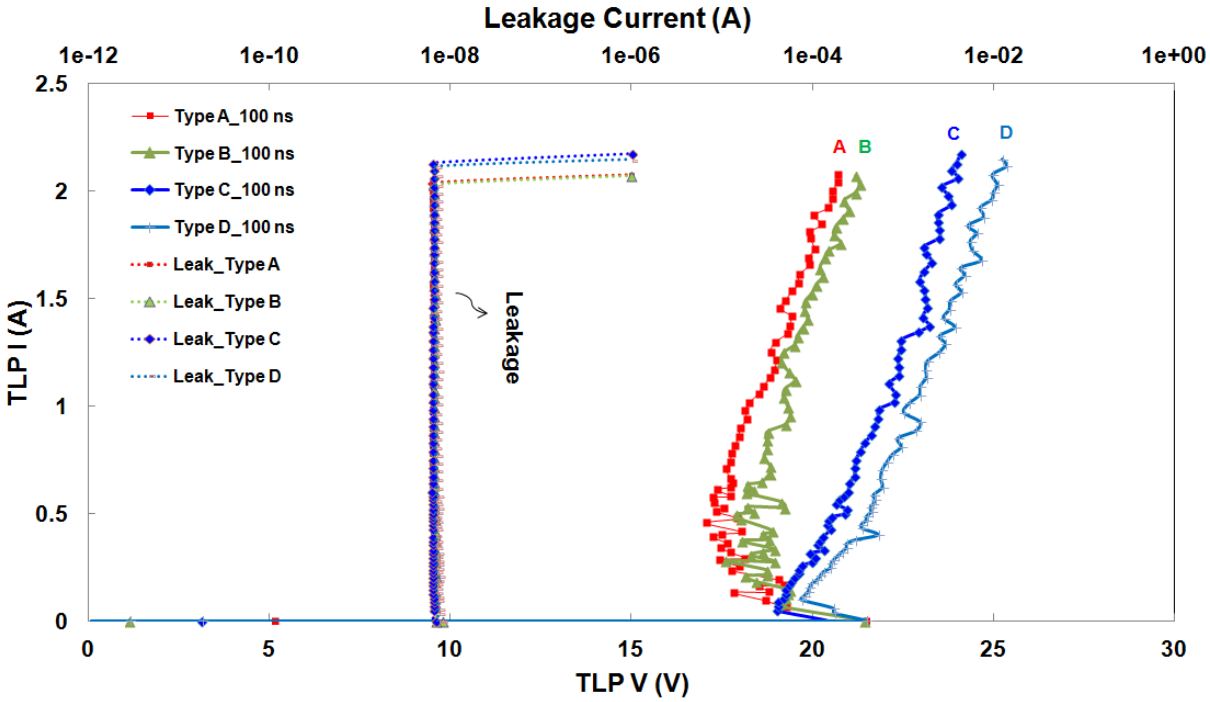


Fig. 3.6 The 100-ns TLP-measured I-V characteristics of 2-PMOSs with different guard-ring layouts

Table 3.3

Summary of 2-PMOSs with different guard-ring types measured by 100-ns TLP

2-PMOSs Stacked Structure	TLP (100-ns)			DC (#)	ESD Level (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
Type A	21.48	17.09	2.04	22.3	3.5	250
Type B	21.43	17.6	2.03	22.3	3.5	250
Type C	20.48	19.02	2.13	22.6	3.5	250
Type D	21.47	19.69	2.11	22.6	3.5	250

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The 200-ns TLP-measured I-V characteristics of 2-PMOSs with the four types of guard ring layout are shown in Fig. 3.7. The detailed characteristics of 2-PMOSs stacked structure with different guard-ring types are listed in Table 3.4.

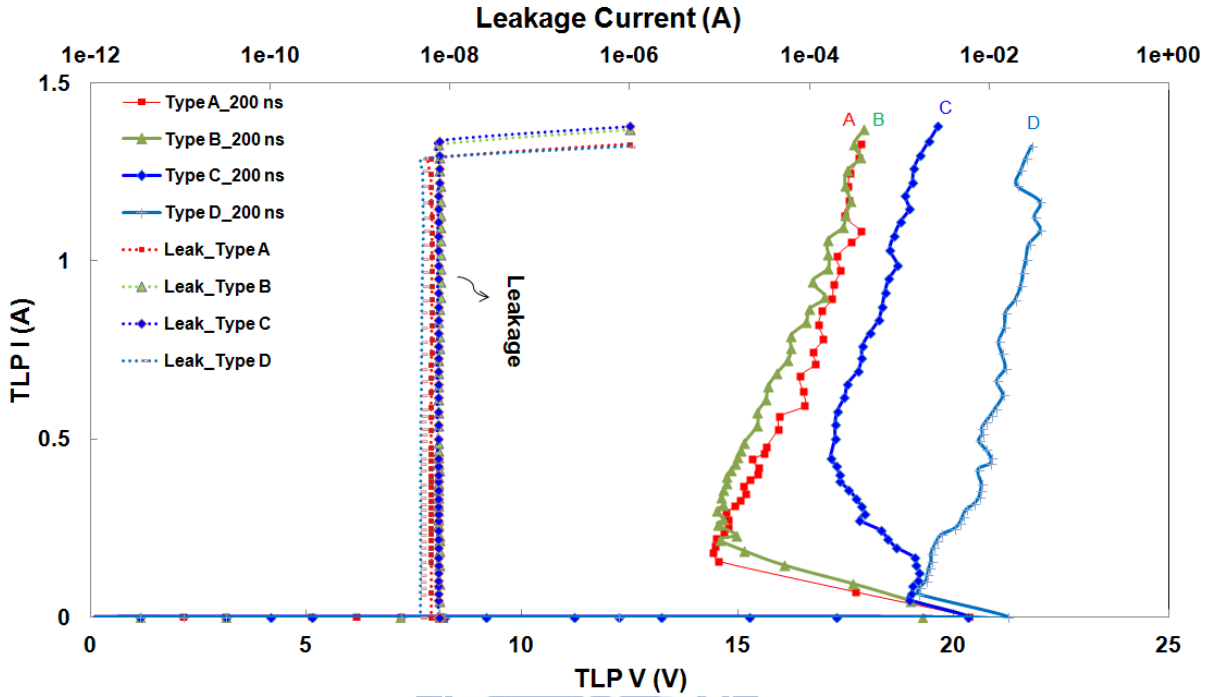


Fig. 3.7 The 200-ns TLP-measured I-V characteristics of 2-PMOSs with different guard-ring layouts

Table 3.4

Summary of 2-PMOSs with different guard-ring types measured by 200-ns TLP

2-PMOSs Stacked Structure	TLP (200-ns)			DC (#)	ESD Level (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
Type A	20.38	14.44	1.29	22.3	3.5	250
Type B	20.35	14.5	1.33	22.3	3.5	250
Type C	20.33	17.15	1.34	22.6	3.5	250
Type D	21.26	19.2	1.29	22.6	3.5	250

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The 500-ns TLP-measured I-V characteristics of 2-PMOSs with the four types of guard ring layout are shown in Fig. 3.8. The detailed characteristics of 2-PMOSs stacked structure with different guard-ring types are listed in Table 3.5.

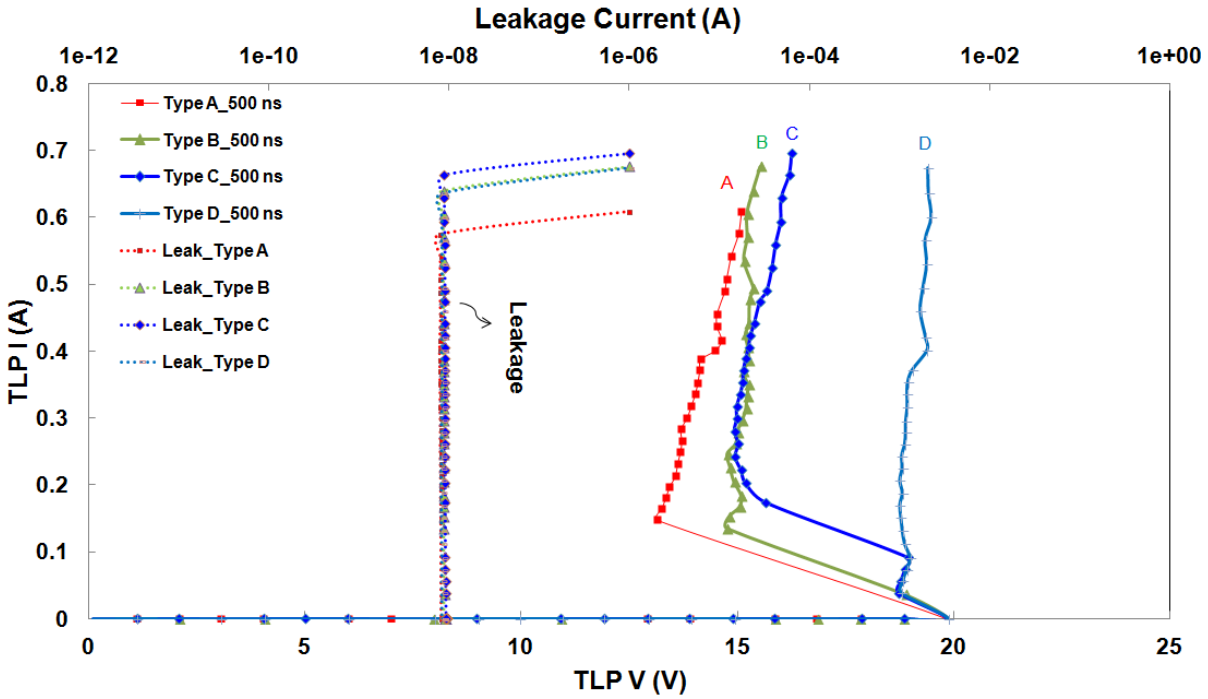


Fig. 3.8 The 500-ns TLP-measured I-V characteristics of 2-PMOSs with different guard-ring layouts

Table 3.5

Summary of 2-PMOSs with different guard-ring types measured by 500-ns TLP

2-PMOSs Stacked Structure	TLP (500-ns)			DC (#)	ESD Level (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
Type A	19.86	13.15	0.58	22.3	3.5	250
Type B	19.89	14.77	0.64	22.3	3.5	250
Type C	19.87	14.93	0.66	22.6	3.5	250
Type D	19.87	18.85	0.64	22.6	3.5	250

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The 800-ns TLP-measured I-V characteristics of 2-PMOSs with the four types of guard ring layout are shown in Fig. 3.9. The detailed characteristics of 2-PMOSs stacked structure with different guard-ring types are listed in Table 3.6.

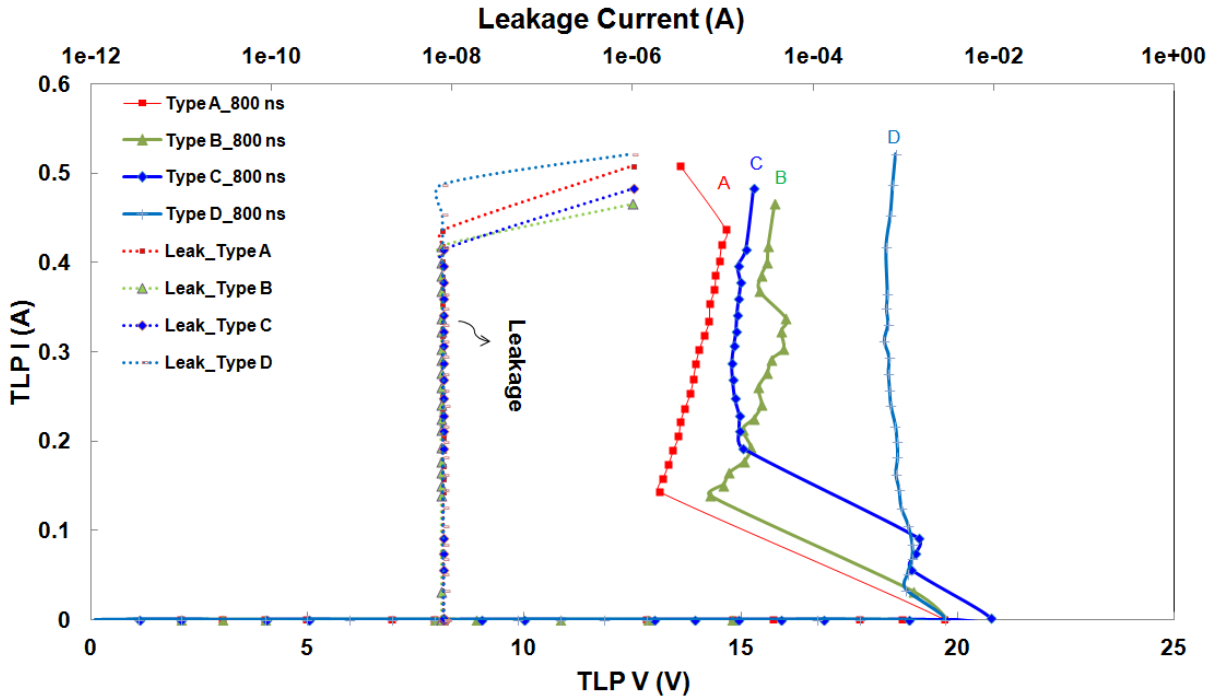


Fig. 3.9 The 800-ns TLP-measured I-V characteristics of 2-PMOSs with different guard-ring layouts

Table 3.6

Summary of 2-PMOSs with different guard-ring types measured by 800-ns TLP

2-PMOSs Stacked Structure	TLP (800-ns)			DC (#)	ESD Level (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
Type A	19.71	13.14	0.44	22.3	3.5	250
Type B	19.73	14.29	0.42	22.3	3.5	250
Type C	20.76	14.79	0.41	22.6	3.5	250
Type D	19.71	18.31	0.49	22.6	3.5	250

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The different pulse widths TLP-measured I-V characteristics of 2-PMOSs_type A are shown in Fig. 3.10. The holding voltages (V_h) and secondary breakdown current (I_{t2}) of 2-PMOSs_type A with different TLP pulse widths are shown in Fig. 3.11.

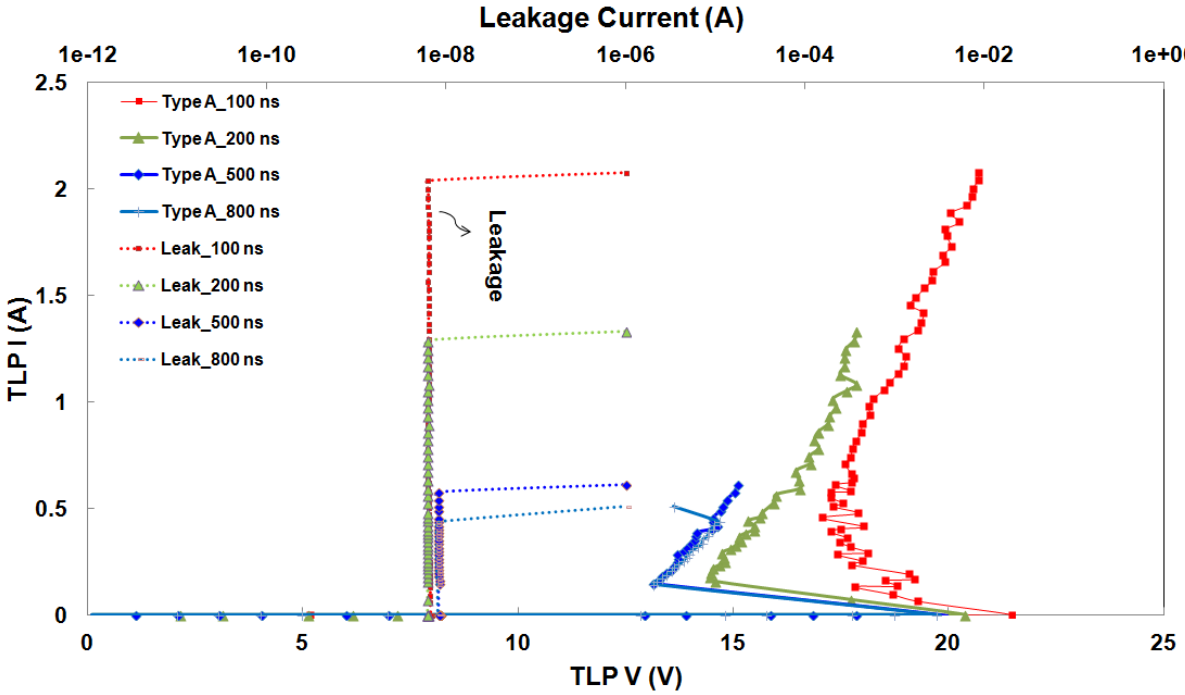


Fig. 3.10 The TLP-measured I-V characteristics of 2-PMOSs_type A with different TLP pulse widths

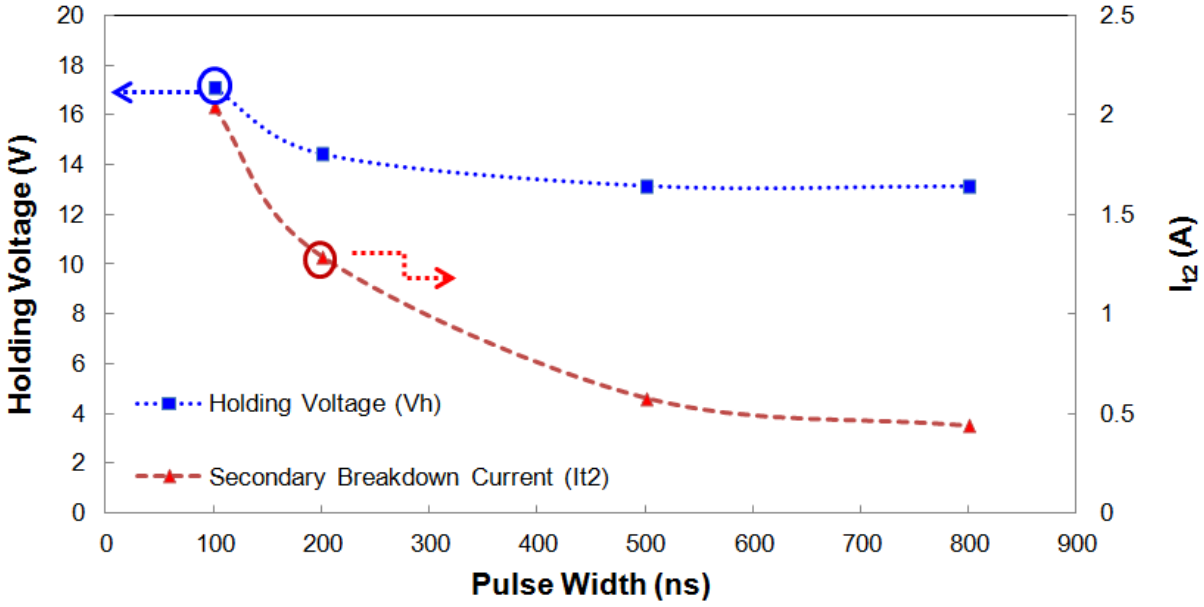


Fig. 3.11 The V_h and I_{t2} of 2-PMOSs_type A with different TLP pulse widths

The different pulse widths TLP-measured I-V characteristics of 2-PMOSs_type B are shown in Fig. 3.12. The holding voltages (V_h) and secondary breakdown current (I_{t2}) of 2-PMOSs_type B with different TLP pulse widths are shown in Fig. 3.13.

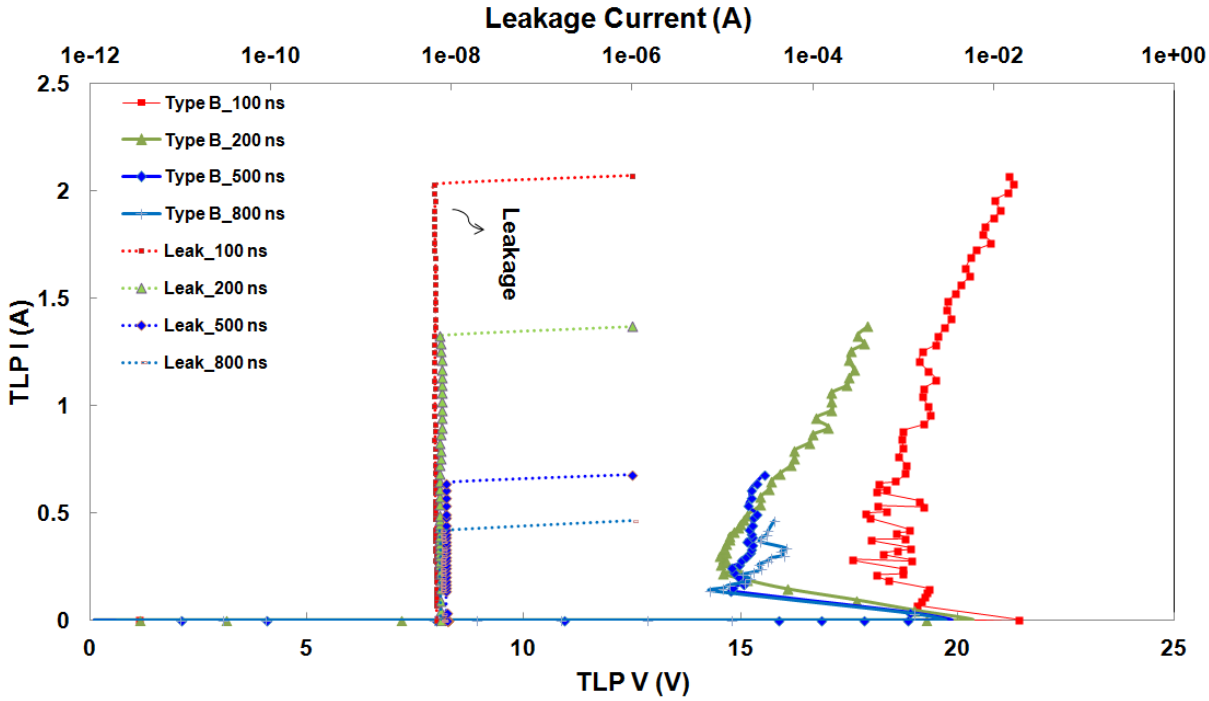


Fig. 3.12 The TLP-measured I-V characteristics of 2-PMOSs_type B with different TLP pulse widths

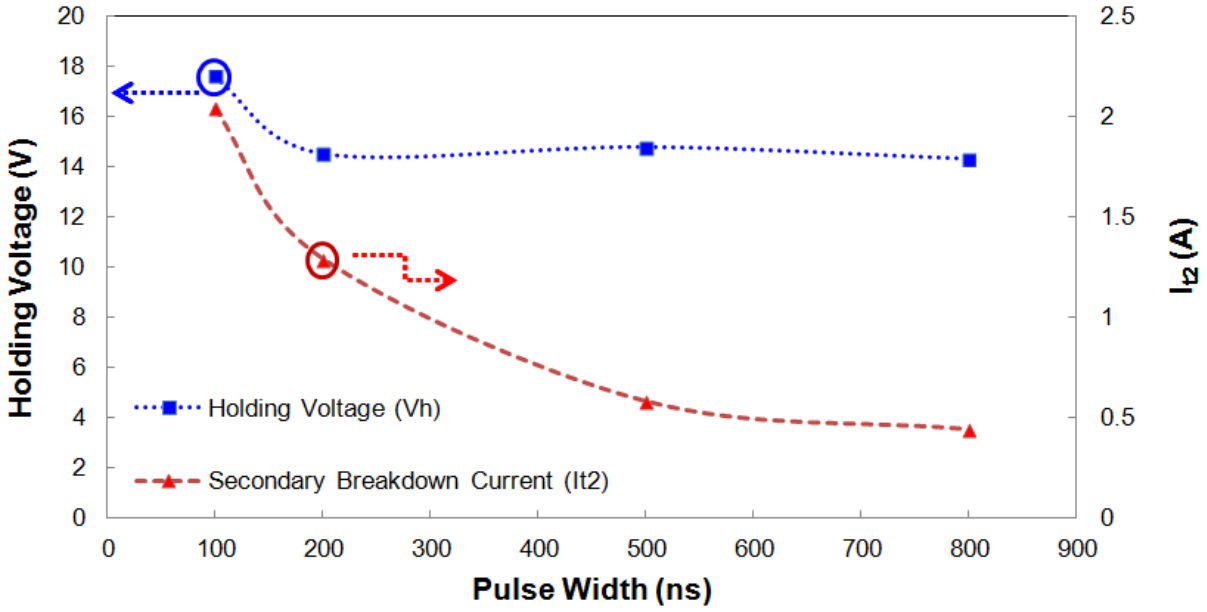


Fig. 3.13 The V_h and I_{t2} of 2-PMOSs_type B with different TLP pulse widths

The different pulse widths TLP-measured I-V characteristics of 2-PMOSs_type C are shown in Fig. 3.14. The holding voltages (V_h) and secondary breakdown current (I_{t2}) of 2-PMOSs_type C with different TLP pulse widths are shown in Fig. 3.15.

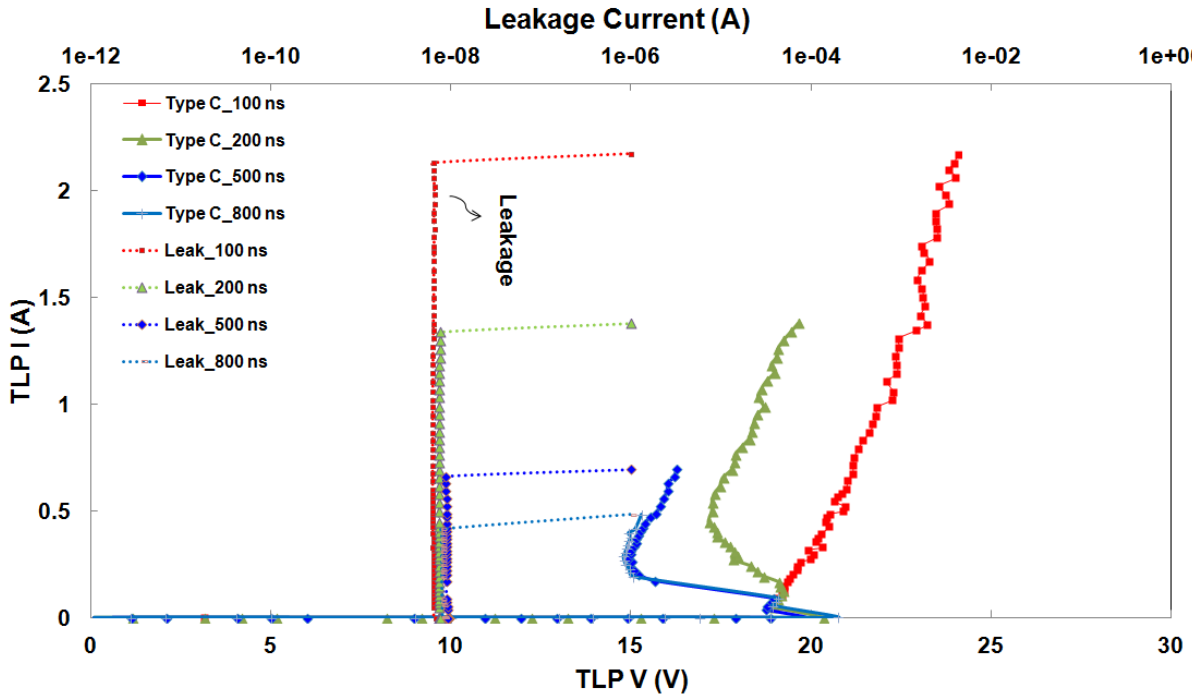


Fig. 3.14 The TLP-measured I-V characteristics of 2-PMOSs_type C with different TLP pulse widths

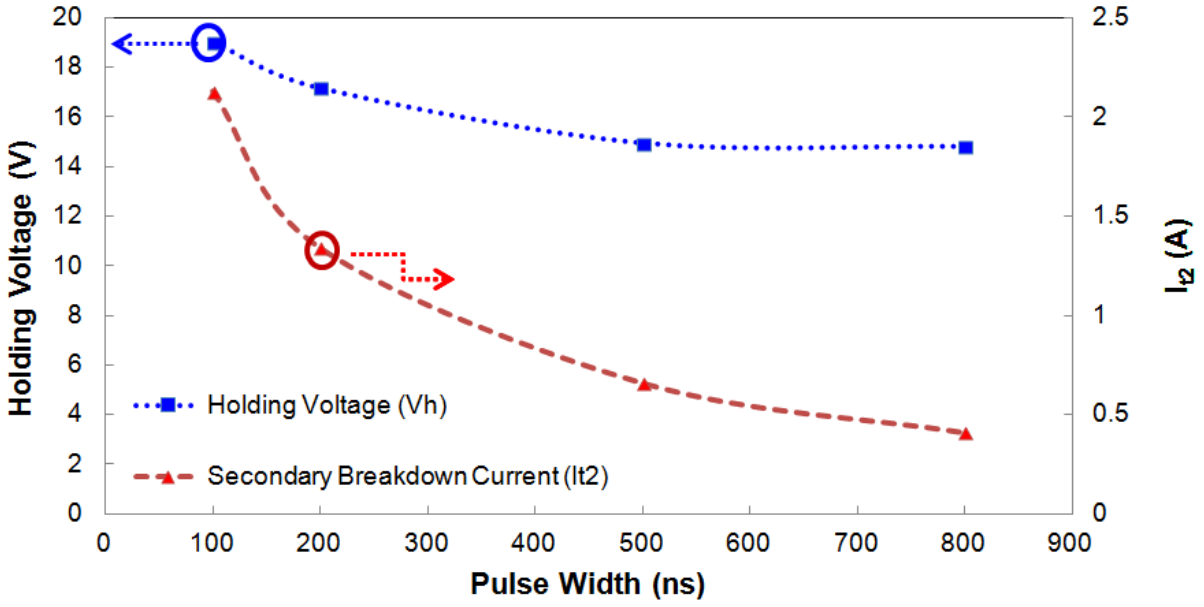


Fig. 3.15 The V_h and I_{t2} of 2-PMOSs_type C with different TLP pulse widths

The different pulse widths TLP-measured I-V characteristics of 2-PMOSs_type D are shown in Fig. 3.16. The holding voltages (V_h) and secondary breakdown current (I_{t2}) of 2-PMOSs_type D with different TLP pulse widths are shown in Fig. 3.17.

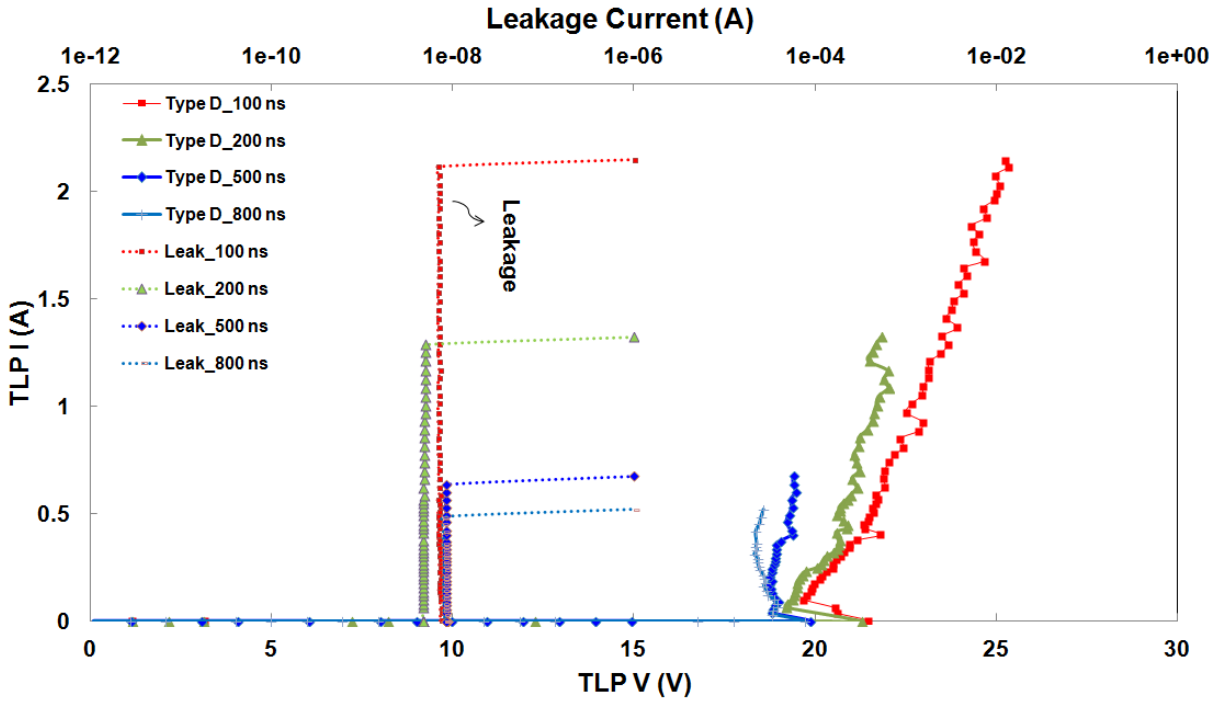


Fig. 3.16 The TLP-measured I-V characteristics of 2-PMOSs_type D with different TLP pulse widths

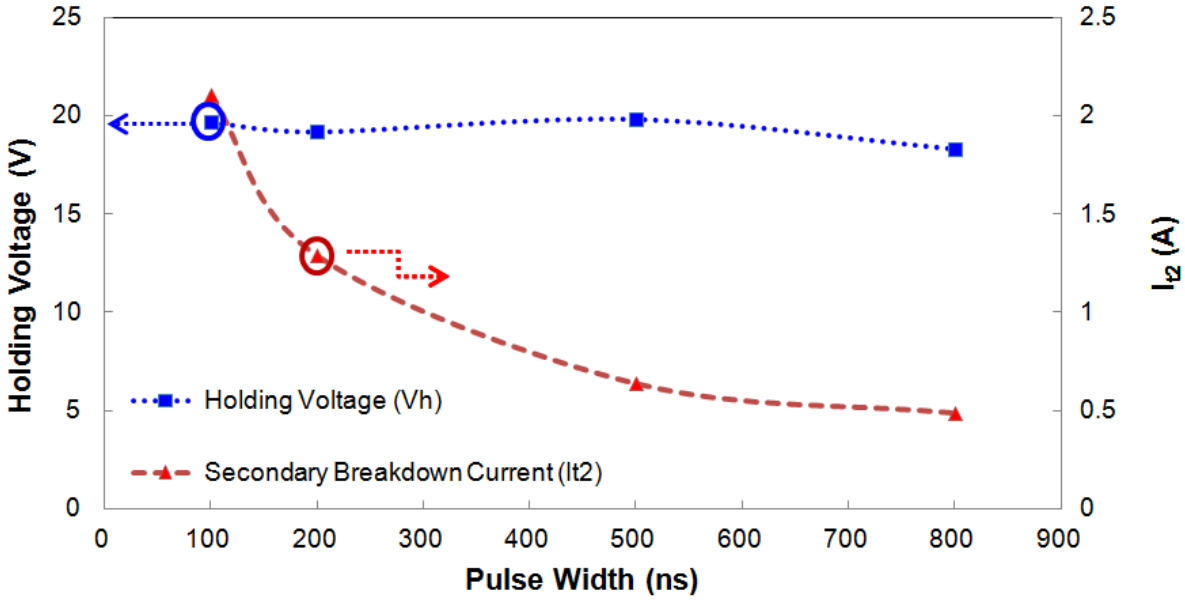


Fig. 3.17 The V_h and I_{t2} of 2-PMOSs_type D with different TLP pulse widths

The 100-ns TLP-measured I-V characteristics of 3-PMOSs with the four types of guard ring layout are shown in Fig. 3.18. The detailed characteristics of 3-PMOSs stacked structure with different guard-ring types are listed in Table 3.7.

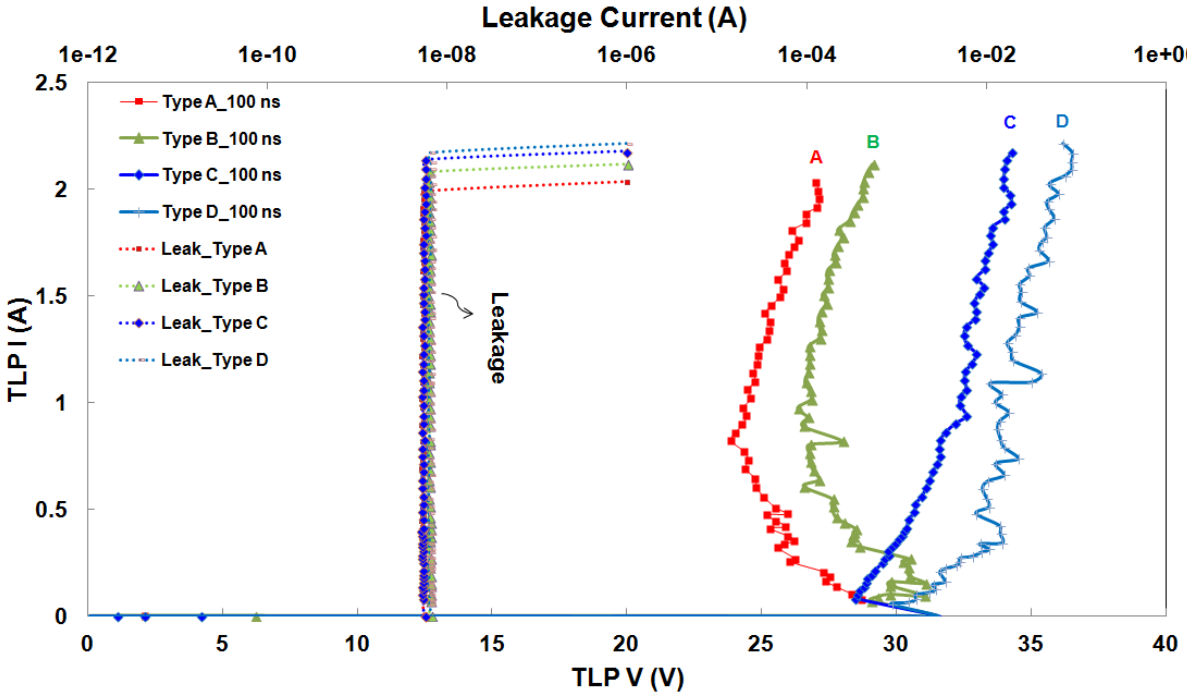


Fig. 3.18 The 100-ns TLP-measured I-V characteristics of 3-PMOSs with different guard-ring layouts

Table 3.7

Summary of 3-PMOSs with different guard-ring types measured by 100-ns TLP

3-PMOSs Stacked Structure	TLP (100-ns)			DC (#)	ESD Level (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
Type A	31.58	23.87	1.99	30.7	3	250
Type B	31.53	26.34	2.08	30.5	3.5	250
Type C	31.56	28.47	2.14	30.7	3.5	300
Type D	31.58	29.84	2.17	30.7	3.5	300

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The 200-ns TLP-measured I-V characteristics of 3-PMOSs with the four types of guard ring layout are shown in Fig. 3.19. The detailed characteristics of 3-PMOSs stacked structure with different guard-ring types are listed in Table 3.8.

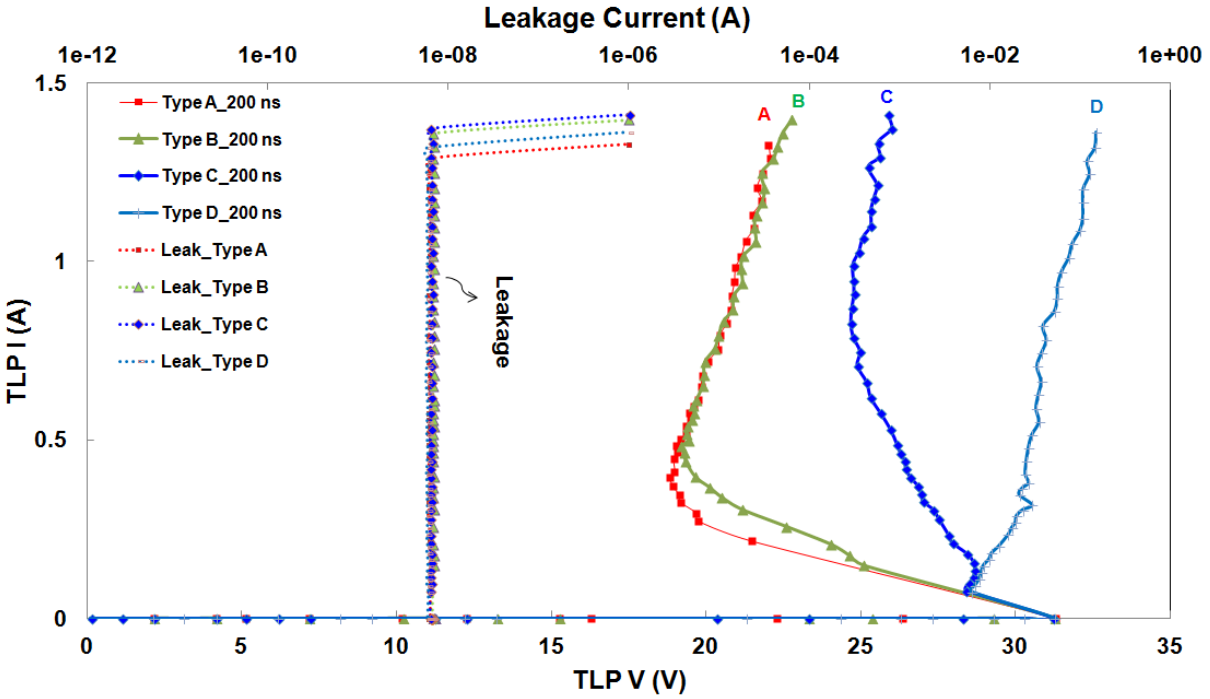


Fig. 3.19 The 200-ns TLP-measured I-V characteristics of 3-PMOSs with different guard-ring layouts

Table 3.8

Summary of 3-PMOSs with different guard-ring types measured by 200-ns TLP

3-PMOSs Stacked Structure	TLP (200-ns)			DC (#)	ESD Level (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
Type A	31.29	18.83	1.29	30.7	3	250
Type B	31.25	19.19	1.36	30.5	3.5	250
Type C	31.22	24.67	1.37	30.7	3.5	300
Type D	31.28	28.58	1.32	30.7	3.5	300

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The 500-ns TLP-measured I-V characteristics of 3-PMOSs with the four types of guard ring layout are shown in Fig. 3.20. The detailed characteristics of 3-PMOSs stacked structure with different guard-ring types are listed in Table 3.9.

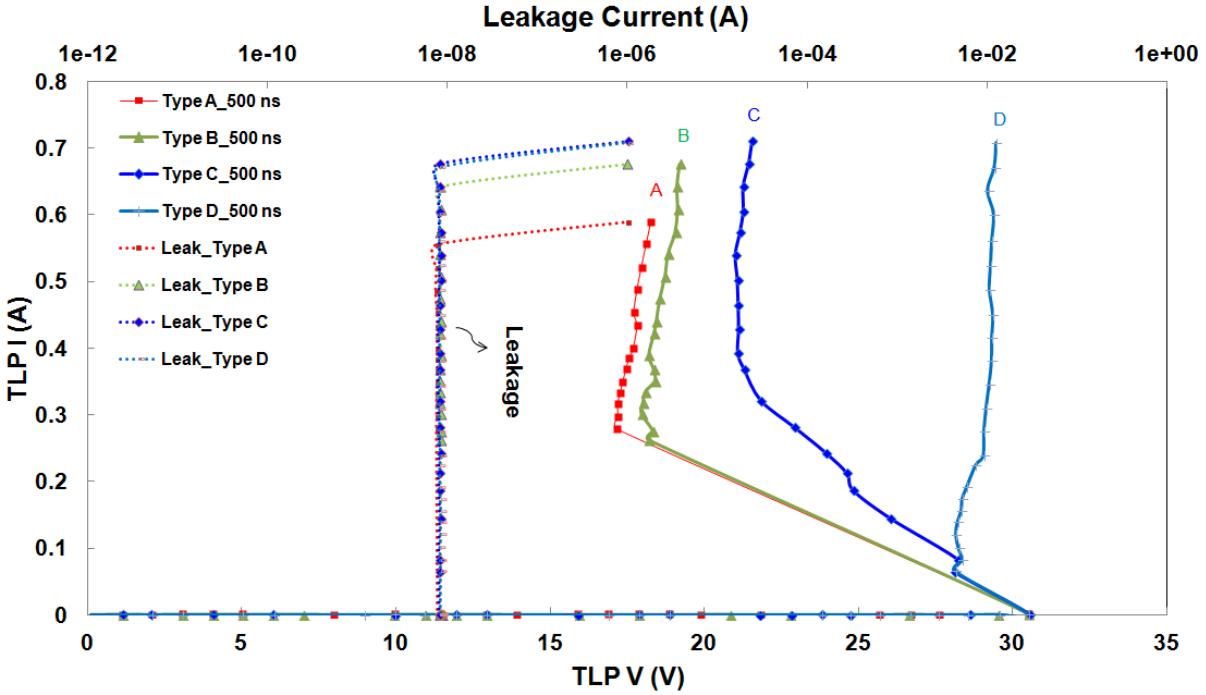


Fig. 3.20 The 500-ns TLP-measured I-V characteristics of 3-PMOSs with different guard-ring layouts

Table 3.9

Summary of 3-PMOSs with different guard-ring types measured by 500-ns TLP

3-PMOSs Stacked Structure	TLP (500-ns)			DC (#)	ESD Level (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
Type A	30.51	17.16	0.56	30.7	3	250
Type B	30.5	17.96	0.64	30.5	3.5	250
Type C	30.53	21	0.68	30.7	3.5	300
Type D	30.5	28.13	0.67	30.7	3.5	300

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The 800-ns TLP-measured I-V characteristics of 3-PMOSs with the four types of guard ring layout are shown in Fig. 3.21. The detailed characteristics of 3-PMOSs stacked structure with different guard-ring types are listed in Table 3.10.

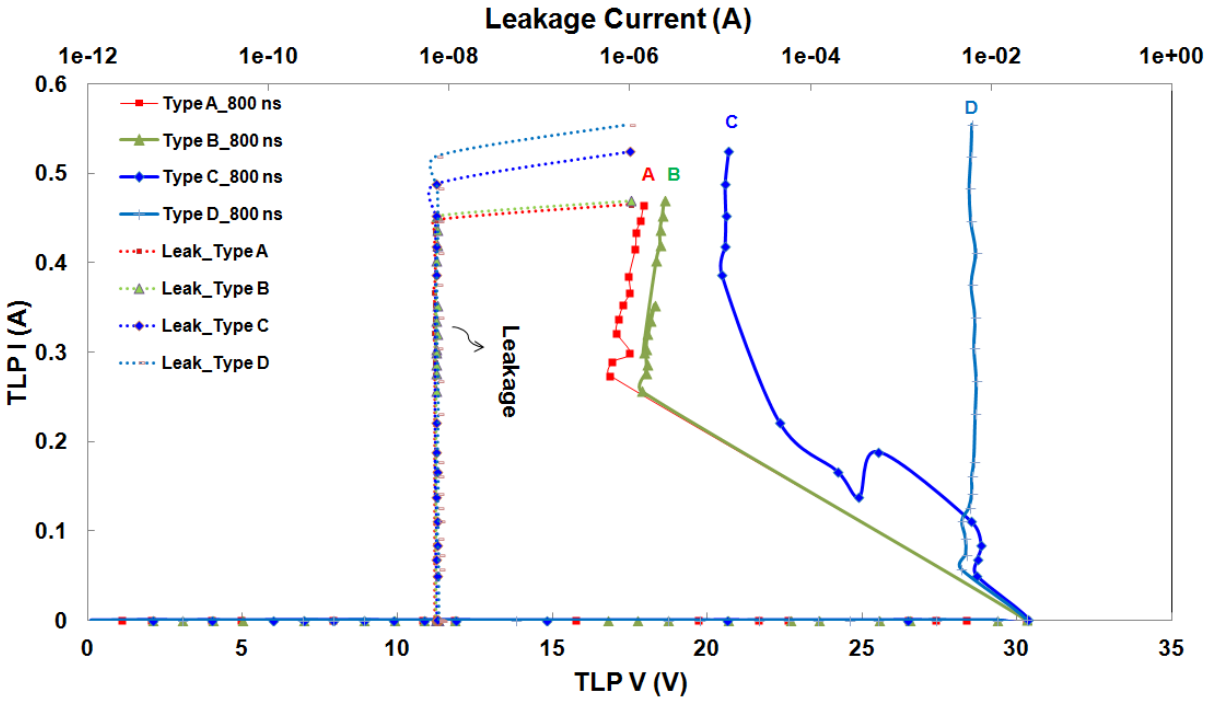


Fig. 3.21 The 800-ns TLP-measured I-V characteristics of 3-PMOSs with different guard-ring layouts

Table 3.10

Summary of 3-PMOSs with different guard-ring types measured by 800-ns TLP

3-PMOSs Stacked Structure	TLP (800-ns)			DC (#)	ESD Level (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
Type A	30.33	16.85	0.45	30.7	3	250
Type B	30.3	17.9	0.45	30.5	3.5	250
Type C	30.36	20.47	0.49	30.7	3.5	300
Type D	30.31	28.2	0.52	30.7	3.5	300

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The different pulse widths TLP-measured I-V characteristics of 3-PMOSs_type A are shown in Fig. 3.22. The holding voltages (V_h) and secondary breakdown current (I_{t2}) of 3-PMOSs_type A with different TLP pulse widths are shown in Fig. 3.23.

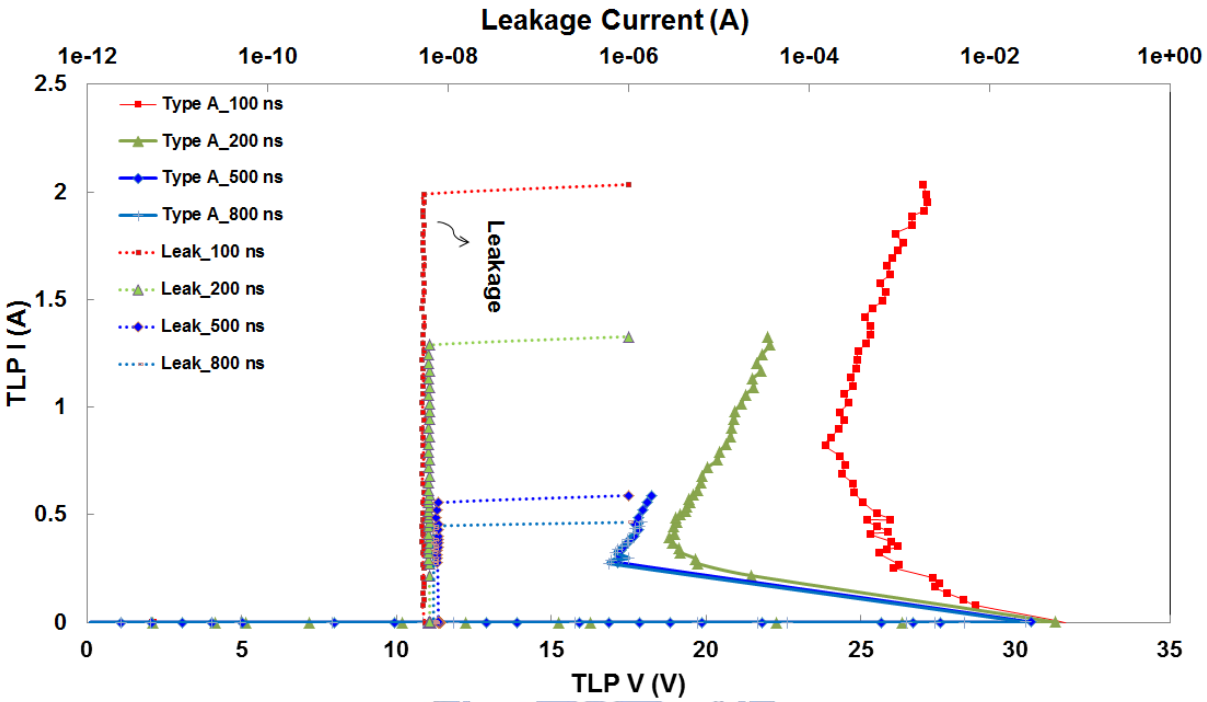


Fig. 3.22 The TLP-measured I-V characteristics of 3-PMOSs_type A with different TLP pulse widths

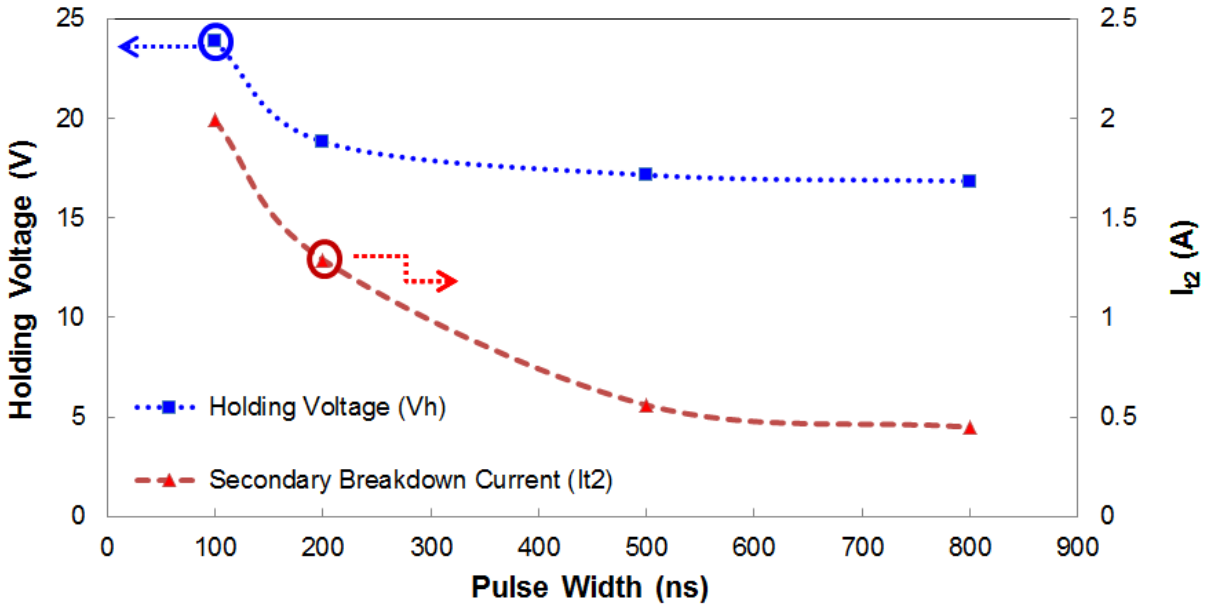


Fig. 3.23 The V_h and I_{t2} of 3-PMOSs_type A with different TLP pulse widths

The different pulse widths TLP-measured I-V characteristics of 3-PMOSs_type B are shown in Fig. 3.24. The holding voltages (V_h) and secondary breakdown current (I_{t2}) of 3-PMOSs_type B with different TLP pulse widths are shown in Fig. 3.25.

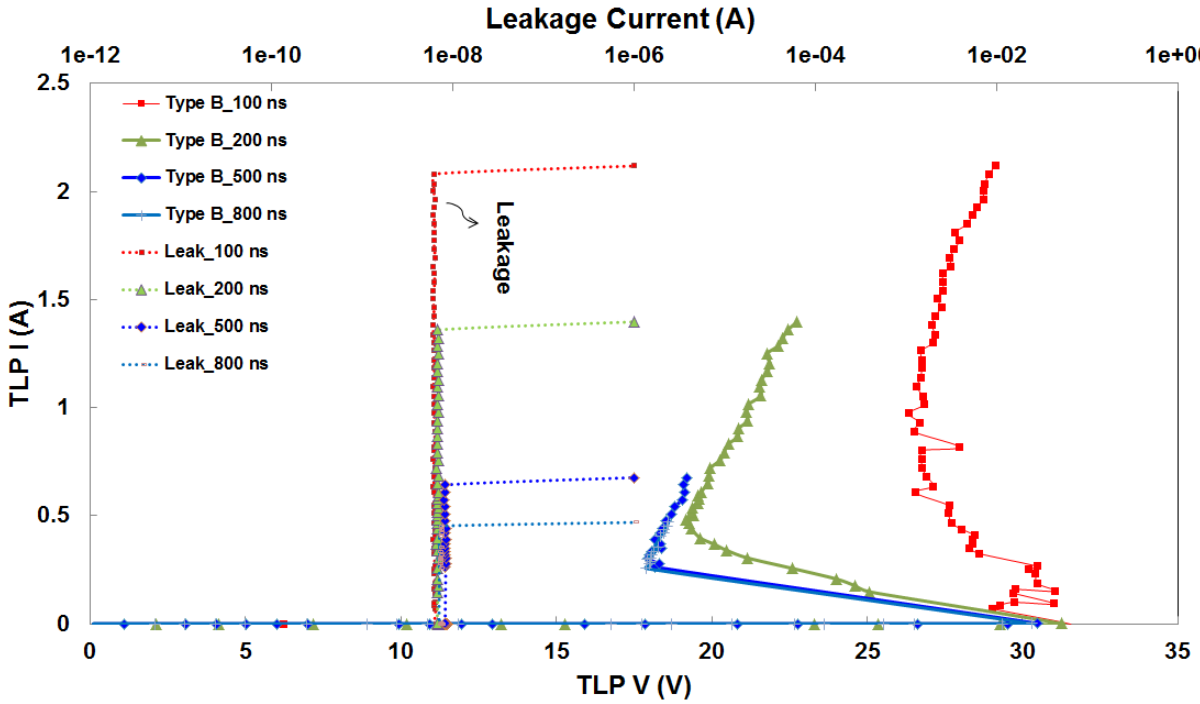


Fig. 3.24 The TLP-measured I-V characteristics of 3-PMOSs_type B with different TLP pulse widths

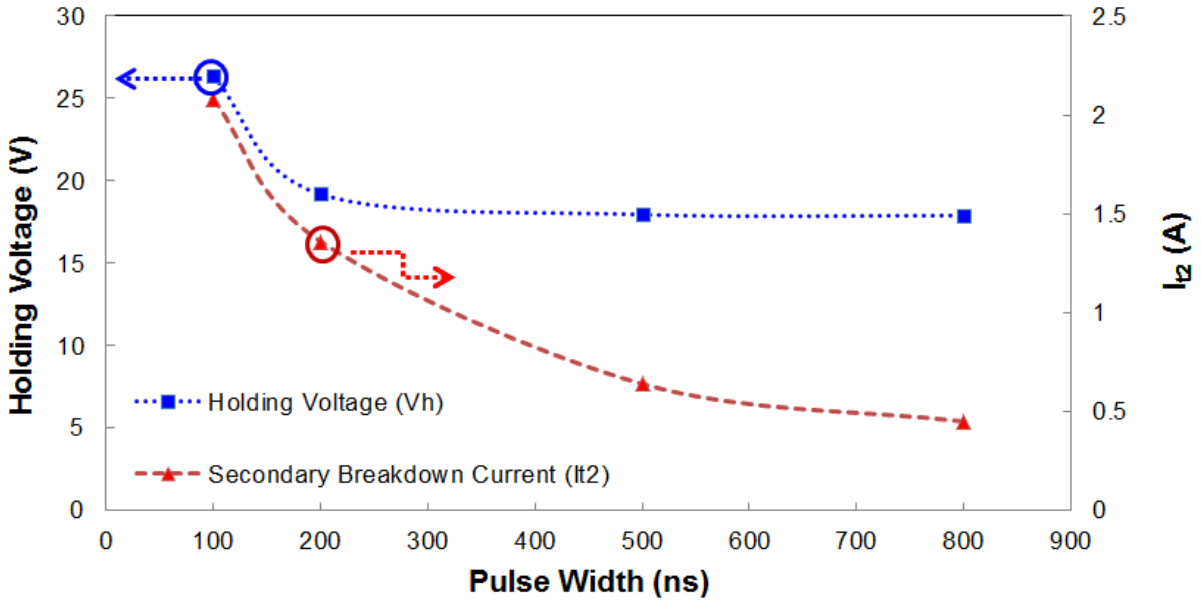


Fig. 3.25 The V_h and I_{t2} of 3-PMOSs_type B with different TLP pulse widths

The different pulse widths TLP-measured I-V characteristics of 3-PMOSs_type C are shown in Fig. 3.26. The holding voltages (V_h) and secondary breakdown current (I_{t2}) of 3-PMOSs_type C with different TLP pulse widths are shown in Fig. 3.27.

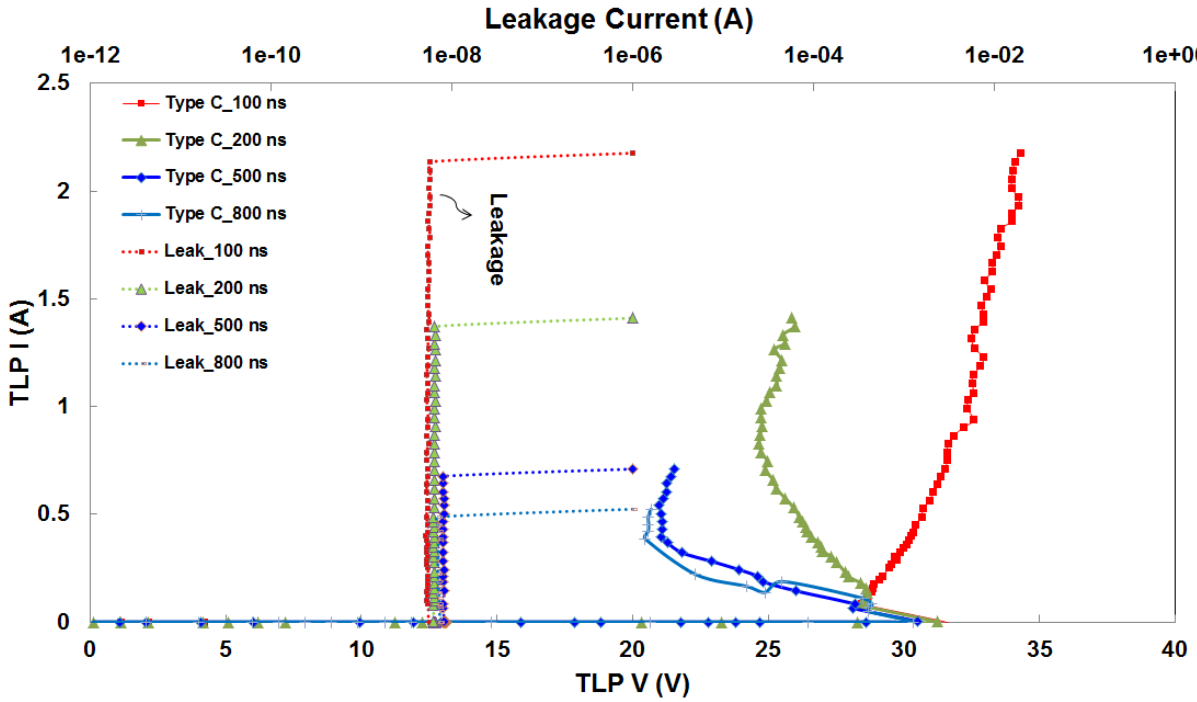


Fig. 3.26 The TLP-measured I-V characteristics of 3-PMOSs_type C with different TLP pulse widths

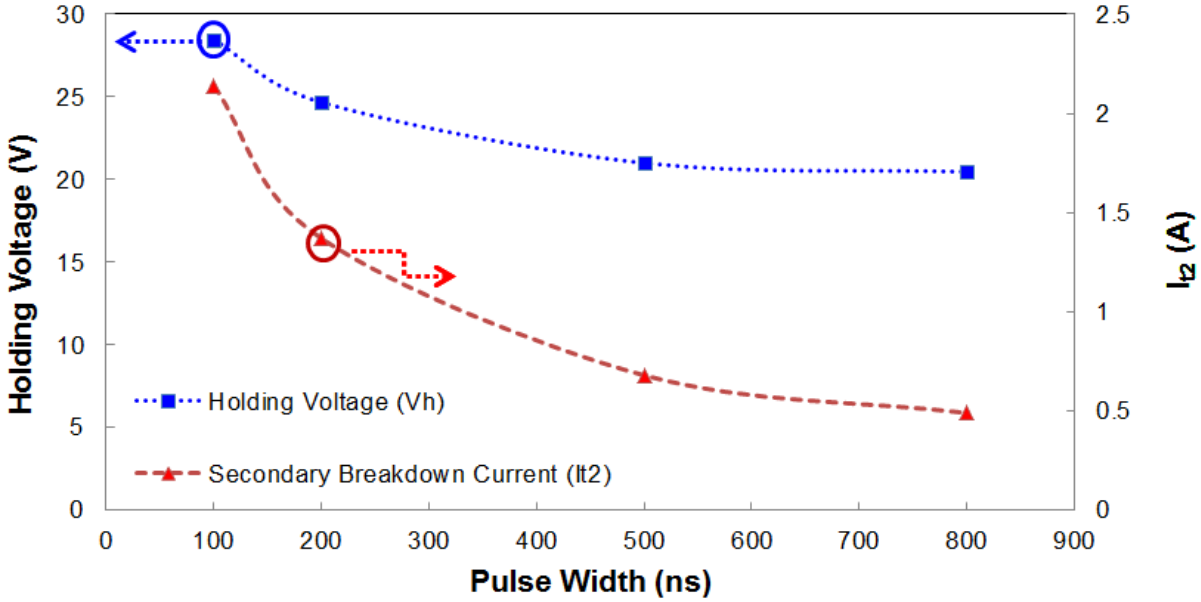


Fig. 3.27 The V_h and I_{t2} of 3-PMOSs_type C with different TLP pulse widths

The different pulse widths TLP-measured I-V characteristics of 3-PMOSs_type D are shown in Fig. 3.28. The holding voltages (V_h) and secondary breakdown current (I_{t2}) of 3-PMOSs_type D with different TLP pulse widths are shown in Fig. 3.29.

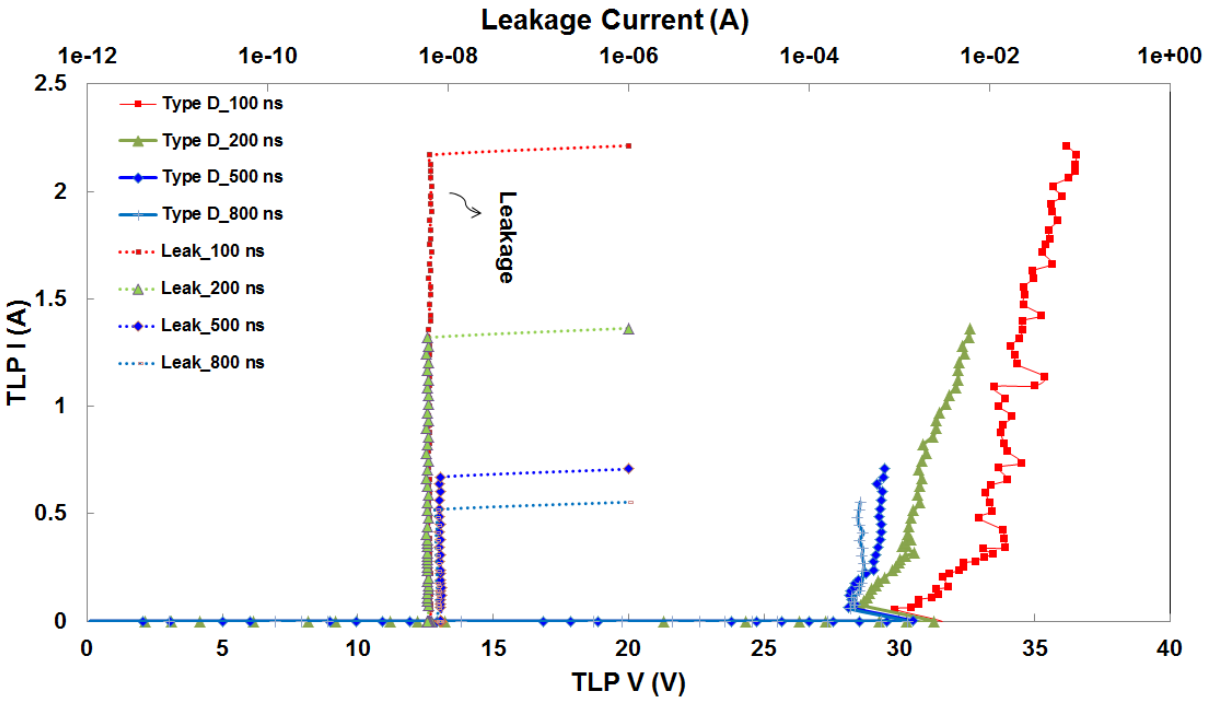


Fig. 3.28 The TLP-measured I-V characteristics of 3-PMOSs_type D with different TLP pulse widths

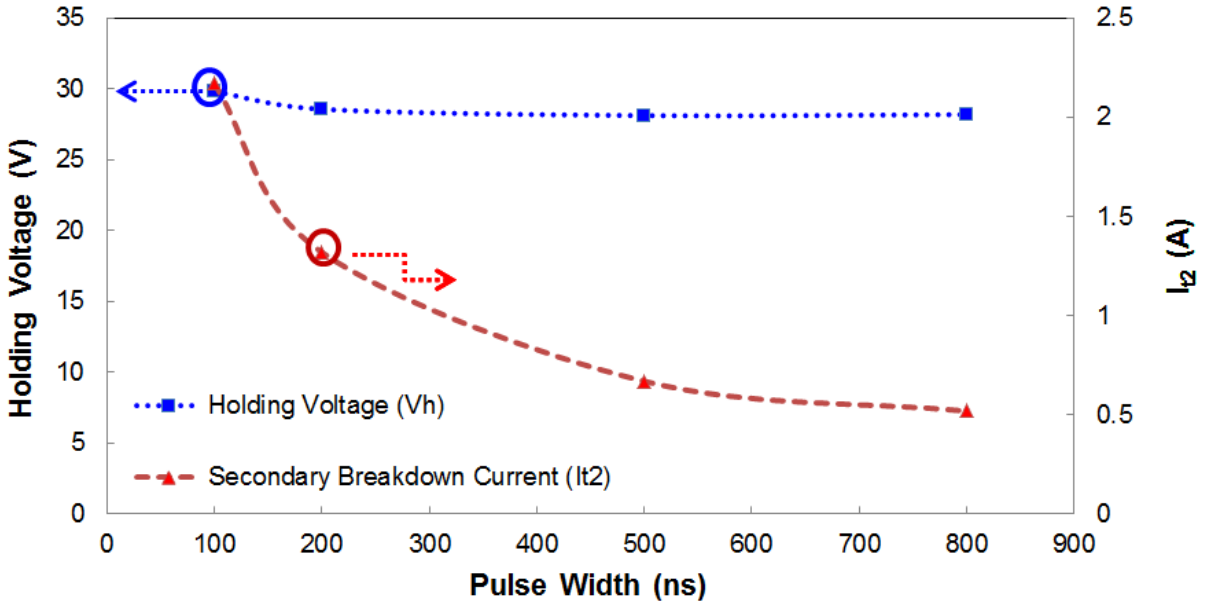


Fig. 3.29 The V_h and I_{t2} of 3-PMOSs_type D with different TLP pulse widths

The Tek370-measured I-V characteristics of 2-PMOSs with the four layout types are shown in Fig. 3.30. The Tek370-measured I-V characteristics of 3-PMOSs with the four layout types are shown in Fig. 3.31.

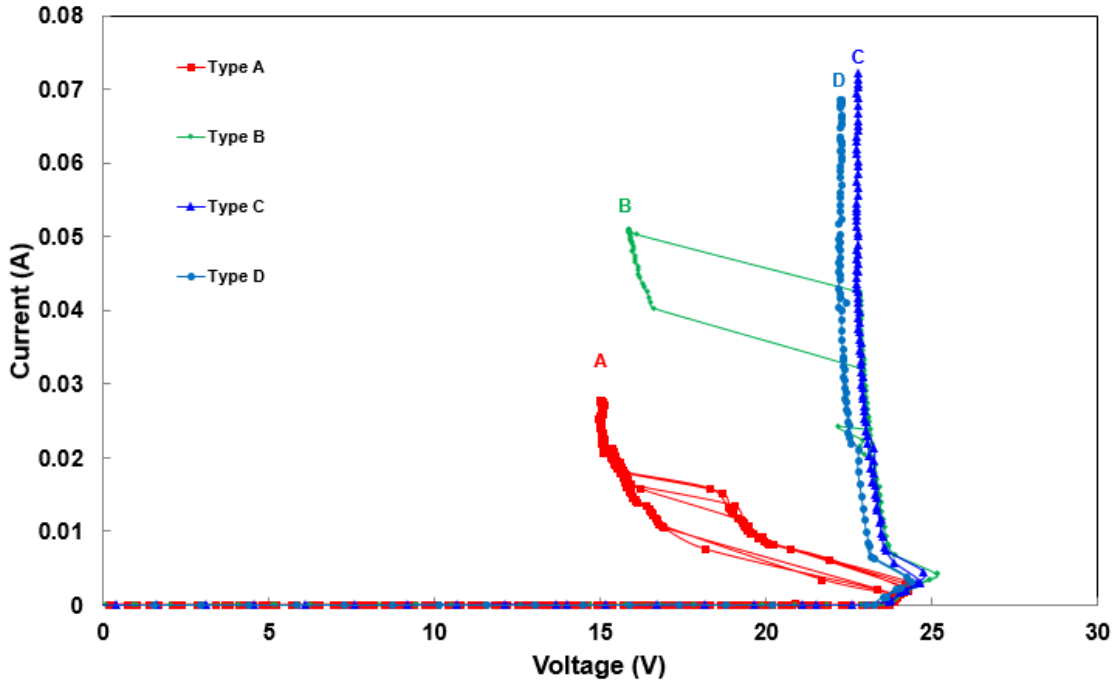


Fig. 3.30 The Tek370-measured I-V characteristics of 2-PMOSs with different guard-ring layouts

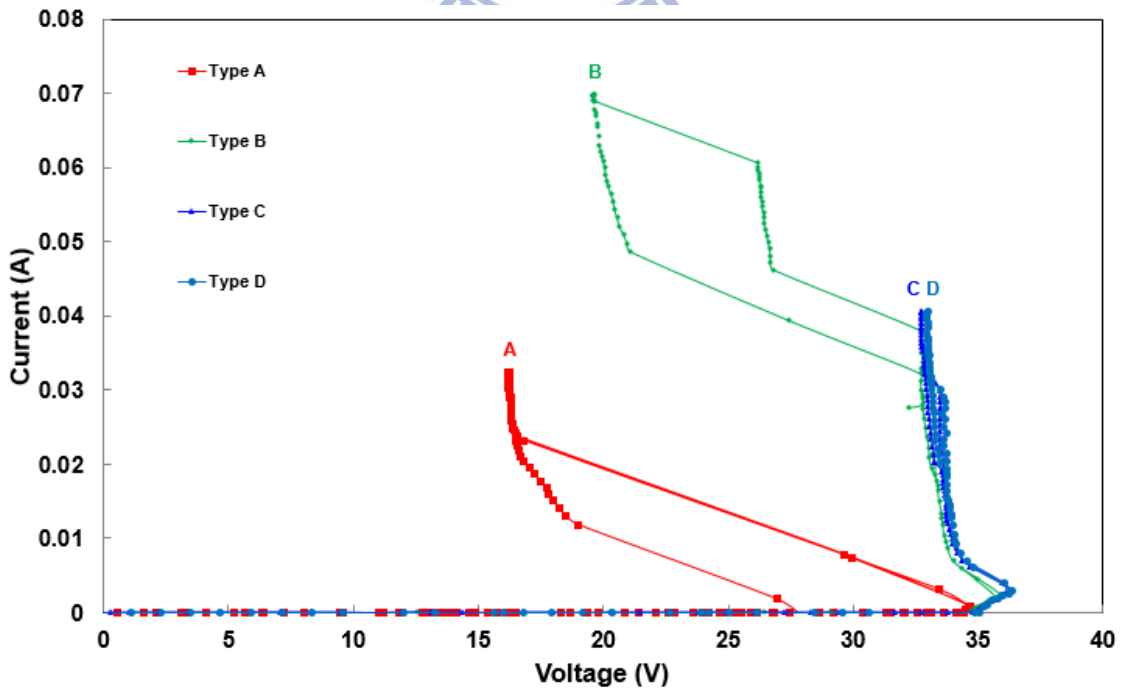


Fig. 3.31 The Tek370-measured I-V characteristics of 3-PMOSs with different guard-ring layouts

The Tek370 I-V curve can show snapback and the holding voltage of the device in a dc condition. Due to the self-heating effect, the values of holding voltage measured by Tek370 are not real. Before the real values of holding voltage measured by Tek370, the devices are failed. The detailed characteristics of 2-PMOSs stacked structure with different guard-ring types are listed in Table 3.11. The detailed characteristics of 3-PMOSs stacked structure with different guard-ring types are listed in Table 3.12.

Table 3.11

Summary of 2-PMOSs with different guard-ring types measured by different TLP pulse width

Pulse width	TLP (Type A)			TLP (Type B)			TLP (Type C)			TLP (Type D)		
	V_{t1} (V)	V_h (V)	I_{t2} (A)	V_{t1} (V)	V_h (V)	I_{t2} (A)	V_{t1} (V)	V_h (V)	I_{t2} (A)	V_{t1} (V)	V_h (V)	I_{t2} (A)
100-ns	21.48	17.09	2.04	21.43	17.6	2.03	20.48	19.02	2.13	21.47	19.69	2.11
200-ns	20.38	14.44	1.29	20.35	14.5	1.33	20.33	17.15	1.34	21.26	19.2	1.29
500-ns	19.86	13.15	0.58	19.89	14.77	0.64	19.87	14.93	0.66	19.87	18.85	0.64
800-ns	19.71	13.14	0.44	19.73	14.29	0.42	20.76	14.79	0.41	19.71	18.31	0.49

Table 3.12

Summary of 3-PMOSs with different guard-ring types measured by different TLP pulse width

Pulse width	TLP (Type A)			TLP (Type B)			TLP (Type C)			TLP (Type D)		
	V_{t1} (V)	V_h (V)	I_{t2} (A)	V_{t1} (V)	V_h (V)	I_{t2} (A)	V_{t1} (V)	V_h (V)	I_{t2} (A)	V_{t1} (V)	V_h (V)	I_{t2} (A)
100-ns	31.58	23.87	1.99	31.53	26.34	2.08	31.56	28.47	2.14	31.58	29.84	2.17
200-ns	31.29	18.83	1.29	31.25	19.19	1.36	31.22	24.67	1.37	31.28	28.58	1.32
500-ns	30.51	17.16	0.56	30.5	17.96	0.64	30.53	21	0.68	30.5	28.13	0.67
800-ns	30.33	16.85	0.45	30.3	17.9	0.45	30.36	20.47	0.49	30.31	28.2	0.52

In chapter 3.1, the holding voltages of the type A for 2-PMOSs and 3-PMOSs are lower than supply voltages (20V and 30V), and the holding voltages of the type B for 2-PMOSs and 3-PMOSs are also lower than supply voltages (20V and 30V). The holding voltages of the type C are almost same as the type D for 2-PMOSs and 3-PMOSs, but the layout areas of the type C are bigger than the type D for 2-PMOSs and 3-PMOSs.

Due to the pulse widths of TLP increase, the holding voltages of the type C for 2-PMOSs and 3-PMOSs are lower than that under 100-ns TLP stress. The holding voltages of the type D for 2-PMOSs and 3-PMOSs are almost same under different TLP pulse width stress. In addition, I_{t2} of all types of stacked PMOS are also lower since the pulse widths of TLP become longer. Stacked PMOSs under 100-ns TLP pulse width get the highest I_{t2}, and stacked PMOSs under 800-ns TLP pulse width are the lowest.

From above results with different pulse widths TLP-measured I_{t2} and ESD test, the type D among the four types of guard-ring layout is the best choice for the stacked PMOSs structure for HV ESD protection.

3.3 Different Guard Ring Layout of Stacked Low-Voltage PMOS measured by TLP in a 0.25-μm BCD Process

3.3.1 Test Devices

From chapter 3.1 and 3.2, the ESD devices should be surrounded by the guard ring. The test devices were all fabricated in a VIS 0.25-μm BCD process. PMOS devices in this investigation, the clearance from the resist-protection-oxide (RPO) to poly-gate edge, the clearance from the drain contact to poly-gate edge (d1), the drain contact number (co), the channel length (L), the single finger width, and the total width are kept at 0.3μm, 2μm, 2, 0.8μm, 30μm ,and 360μm, respectively. Stacking number was from 1 to 10 in this test.

There are three types (type A, type B, and type C) of the guard ring layouts to surround

the stacked PMOSs, as shown in Fig. 3.32, where 3-PMOSs stacked structure is demonstrated. Guard rings are composed by a HV-NWELL ring and a HV-PWELL ring. Fig. 3.33 show the schematic of 3-PMOSs.

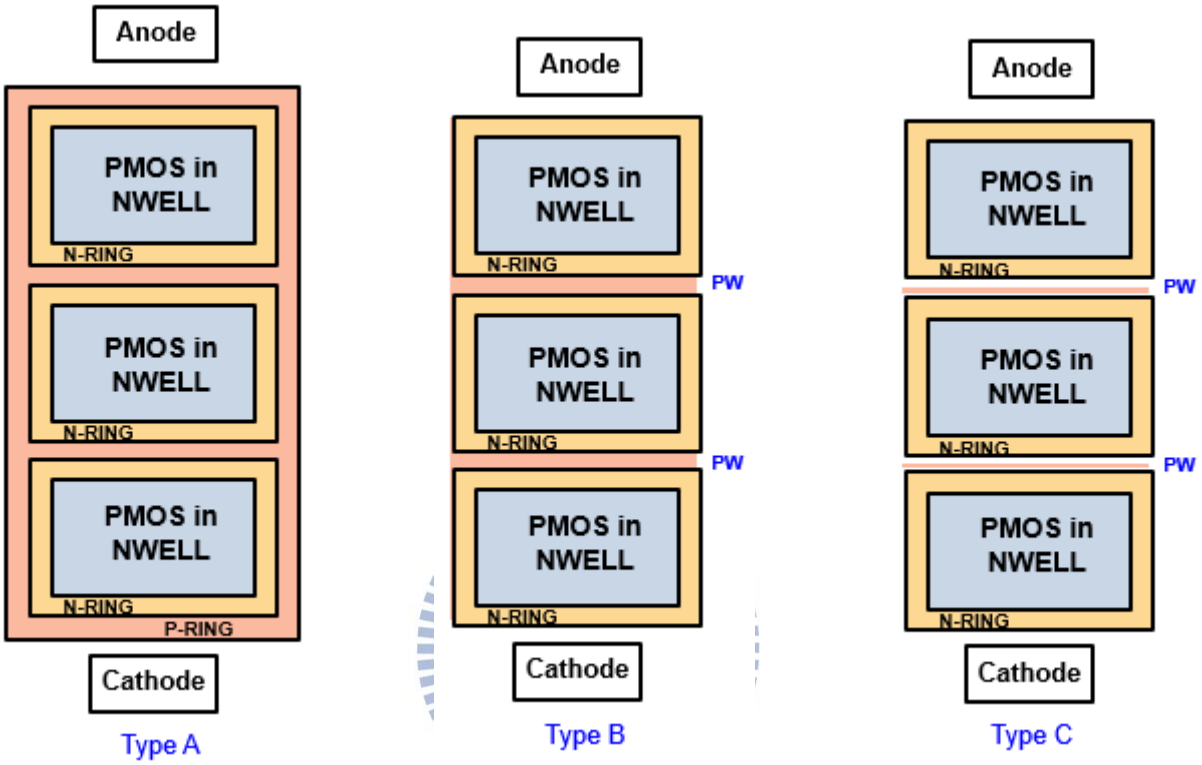


Fig. 3.32 The three types of guard-ring layout for 3-PMOSs stacked structure, (a) type A (typical), (b) type B, and (c) type C

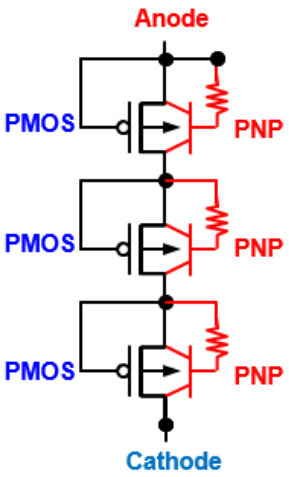
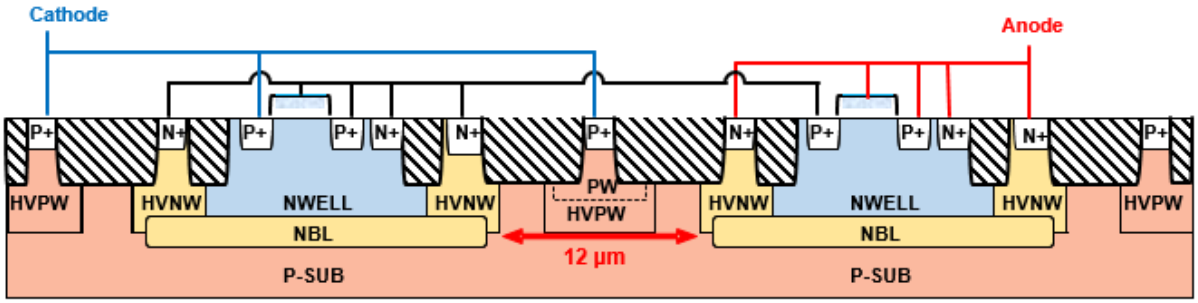
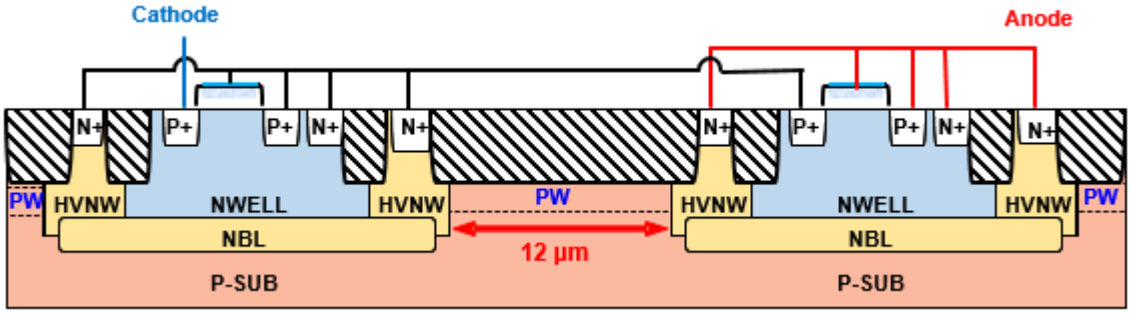


Fig. 3.33 The schematic of 3-PMOSs in BCD process

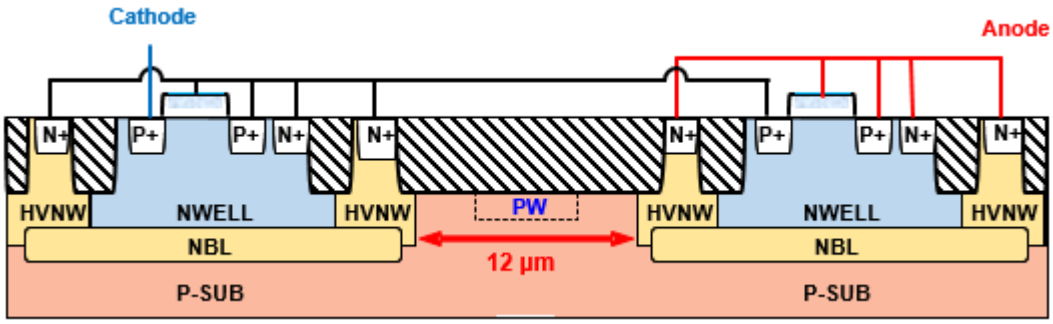
The cross-sectional view of stacked structure with two LV PMOSs is shown in Fig. 3.34. The cross-sectional view of type A (typical) is shown in Fig. 3.34(a). The cross-sectional view of type B is shown in Fig. 3.34(b). The cross-sectional view of type C is shown in Fig. 3.34(c).



(a)



(b)



(c)

Fig. 3.34 The cross-sectional views of stacked structure with two LV PMOSs drawn (a) type A (typical), (b) type B (12μm), and (c) type C (12μm)

In type A (typical), the HV-PWELL ring is usually tied to the lowest potential point, and the HV-NWELL ring is tied to relative high potential point. In type B and type C, the HV-NWELL ring is tied to relative high potential point. The spacing between each HV-NWELL ring in the type B is 12μm. The HVNW spacing spites from 12μm to 2μm, and the PWELL under the STI is connected between two HV-NWELL rings. The spacing between each HV-NWELL ring in the type C is 12μm. The HVNW spacing spites from 12μm to 9μm, and the length of the PWELL spites from 4μm to 1μm. The position of the PWELL is under middle of the STI between two HV-NWELL rings. The transmission line pulse (TLP) and ESD tester are used to verify the stacked PMOSs with different guard ring layouts for HV applications.

3.3.2 Experiment Results

The TLP measured I-V characteristics of type A (typical stacked LV PMOSs) are shown in Fig. 3.35. The total holding voltage of stacked PMOSs is the multiple of the holding voltage of single PMOS. The total trigger voltage of stacked PMOSs is also the multiple of the trigger voltage of single PMOS. The secondary breakdown current (I_{t2}) of stacked PMOSs are almost the same in spite of different stacking numbers. The detailed characteristics of type A (typical stacked LV PMOSs) are listed in Table 3.13.

The TLP measured I-V characteristics of type B are shown in Fig. 3.36. The spacing between each HV-NWELL ring is 12μm. The detailed characteristics of type B (12μm) are listed in Table 3.14. The TLP measured I-V characteristics of type B (10μm) are shown in Fig. 3.37. The detailed characteristics of type B (10μm) are listed in Table 3.15. The TLP measured I-V characteristics of type B (8μm) are shown in Fig. 3.38. The detailed characteristics of type B (8μm) are listed in Table 3.16. The TLP measured I-V characteristics of type B (6μm) are shown in Fig. 3.39. The detailed characteristics of type B (6μm) are listed in Table 3.17. The detailed characteristics of type B (4μm) are listed in Table 3.18. The

detailed characteristics of type B (2μm) are listed in Table 3.19.

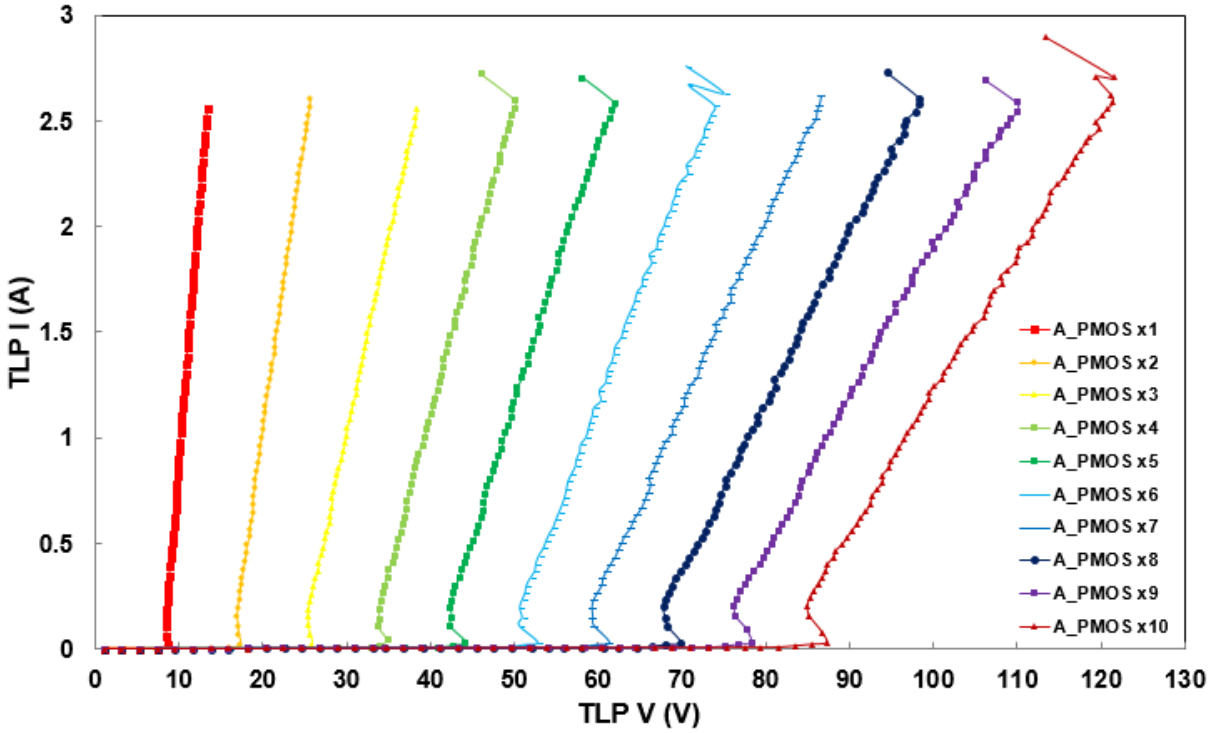


Fig. 3.35 The TLP-measured I-V characteristics of type A (typical stacked LV PMOSs)

Table 3.13

The measurement data of type A (typical stacked LV PMOSs)

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	8.67	8.47	2.51	8.2	4.5	300
2 units	17.3	16.94	2.56	16.5	5	300
3 units	25.85	25.39	2.52	24.9	5	350
4 units	34.88	33.83	2.56	32.4	5.5	350
5 units	44.12	42.27	2.51	40.5	5	350
6 units	52.87	50.62	2.5	48.6	5	400
7 units	61.33	59.24	2.57	56.6	5	400
8 units	69.88	67.77	2.54	64.8	5	400
9 units	78.29	76.24	2.51	73	5	450
10 units	87.25	84.98	2.71	81	5	450

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

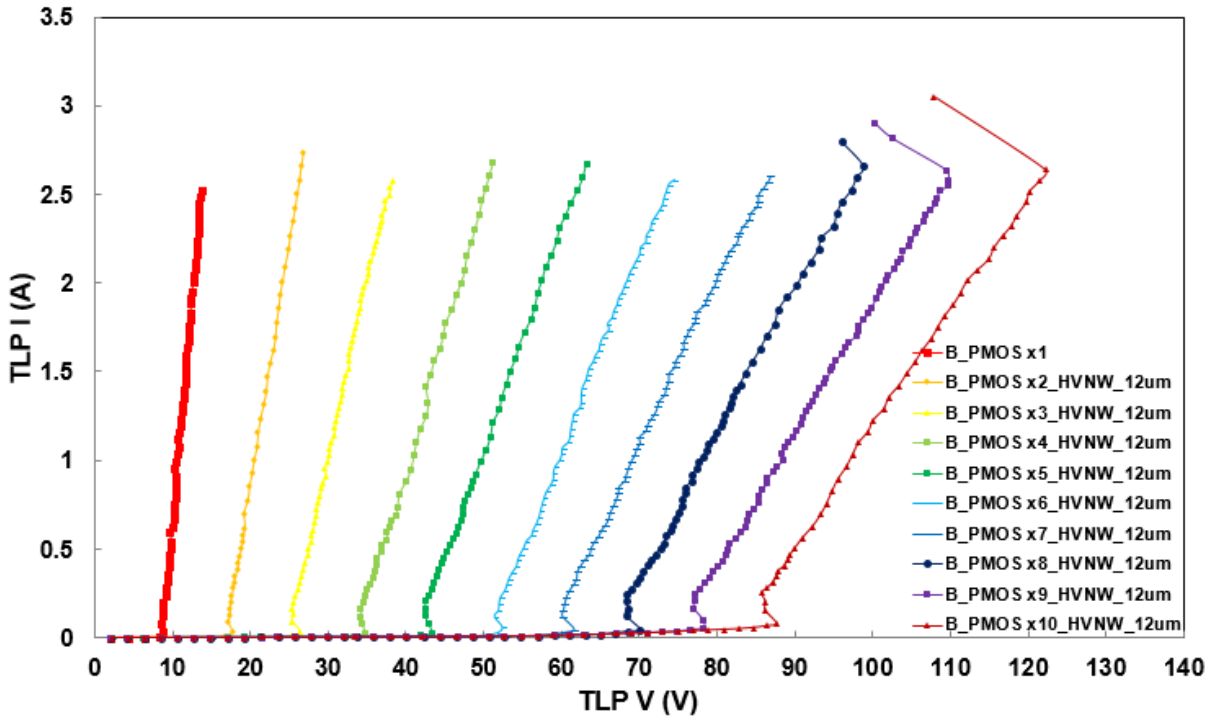


Fig. 3.36 The TLP-measured I-V characteristics of type B (12μm)

Table 3.14

The measurement data of type B (12μm)

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	8.75	8.54	2.49	8	5	300
2 units	17.66	17.18	2.66	16.1	5.5	300
3 units	26.42	25.37	2.54	24.2	5.5	300
4 units	34.76	34.16	2.53	32.3	5	350
5 units	43.42	42.52	2.45	40.4	5	350
6 units	52.36	51.33	2.55	48.4	5	350
7 units	61.59	60.09	2.5	52	-	-
8 units	70.12	68.26	2.6	52	-	-
9 units	78.25	77	2.58	52	-	-
10 units	87.68	85.78	2.64	52	-	-

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

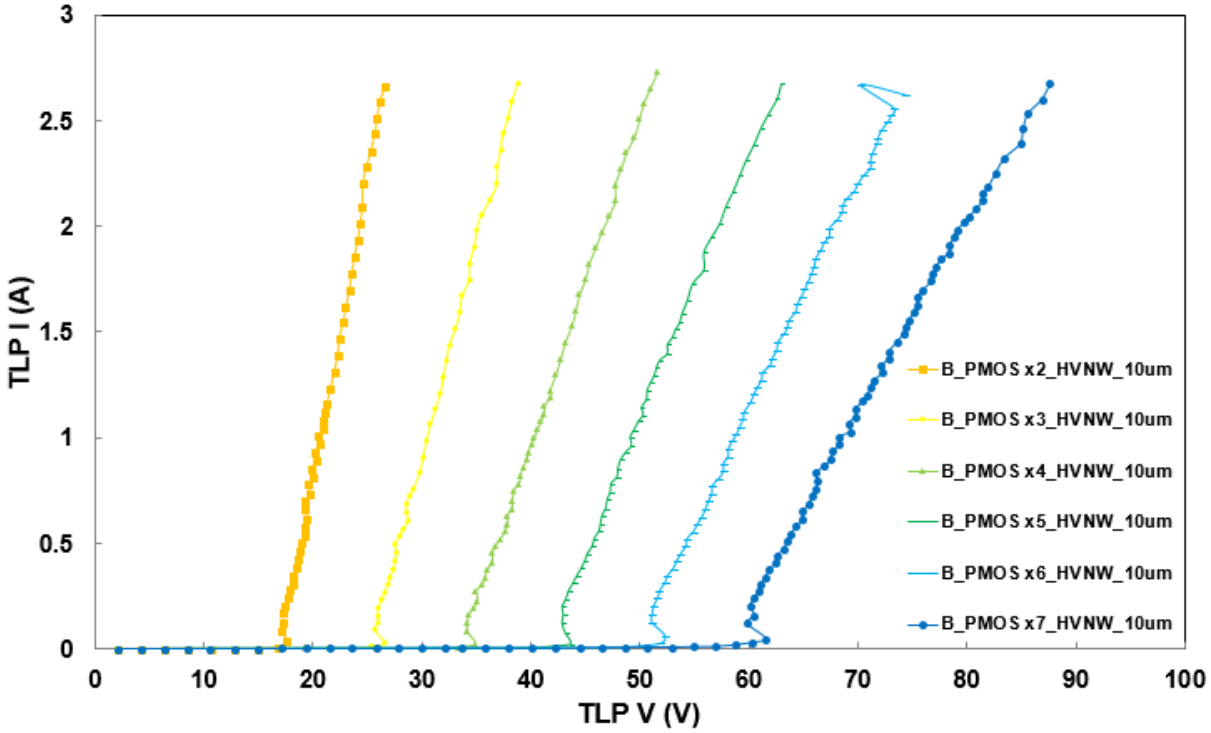


Fig. 3.37 The TLP-measured I-V characteristics of type B (10μm)

Table 3.15
The measurement data of type B (10μm)

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
2 units	17.62	17.07	2.59	16.1	5.5	300
3 units	26.55	25.65	2.59	24.2	5	300
4 units	34.83	34.11	2.58	32.3	5	350
5 units	43.57	42.8	2.6	40.5	5.5	350
6 units	52.25	51.09	2.49	48.4	5	350
7 units	61.53	59.75	2.47	51.2	-	-
8 units	-	-	-	51.2	-	-
9 units	-	-	-	51.4	-	-
10 units	-	-	-	51.6	-	-

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

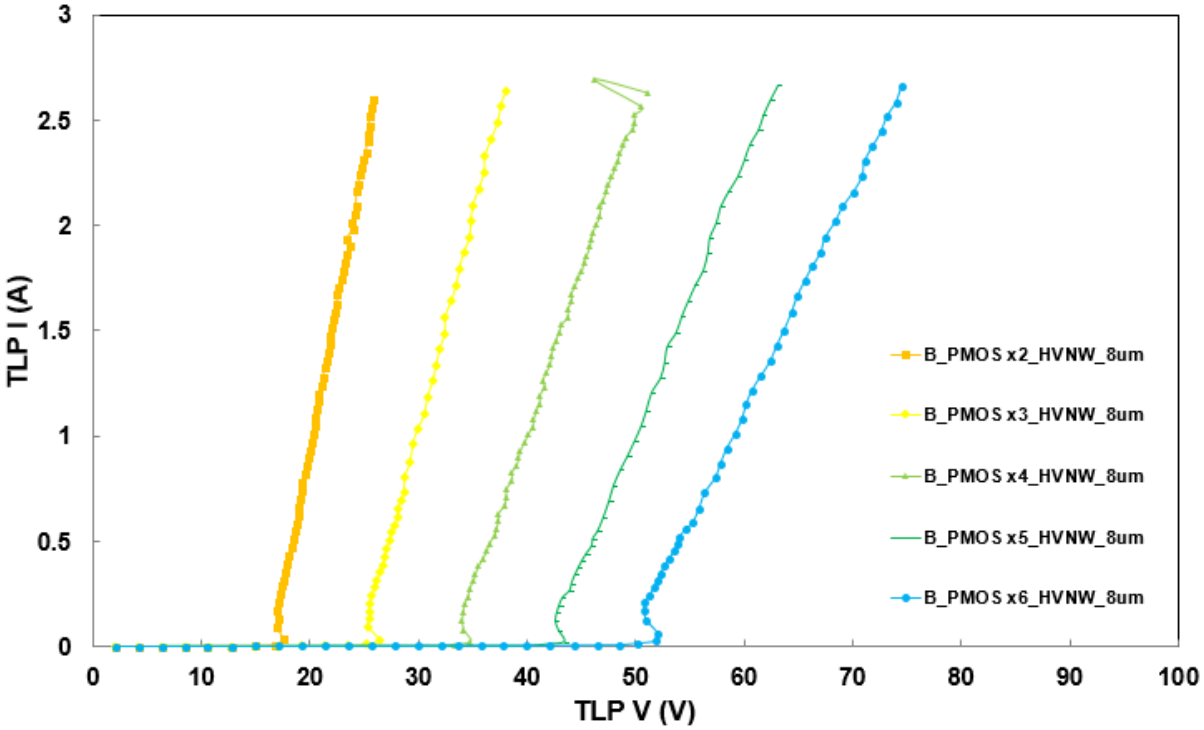


Fig. 3.38 The TLP-measured I-V characteristics of type B (8μm)

Table 3.16

The measurement data of type B (8μm)

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
2 units	17.51	16.97	2.47	16.2	5.5	300
3 units	26.36	25.34	2.56	24.3	5	300
4 units	34.78	34	2.69	32.4	5	350
5 units	43.38	42.53	2.6	40.5	5	350
6 units	52.03	50.85	2.59	48.6	5	350
7 units	-	-	-	51	-	-
8 units	-	-	-	51.2	-	-
9 units	-	-	-	51.4	-	-
10 units	-	-	-	51.4	-	-

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

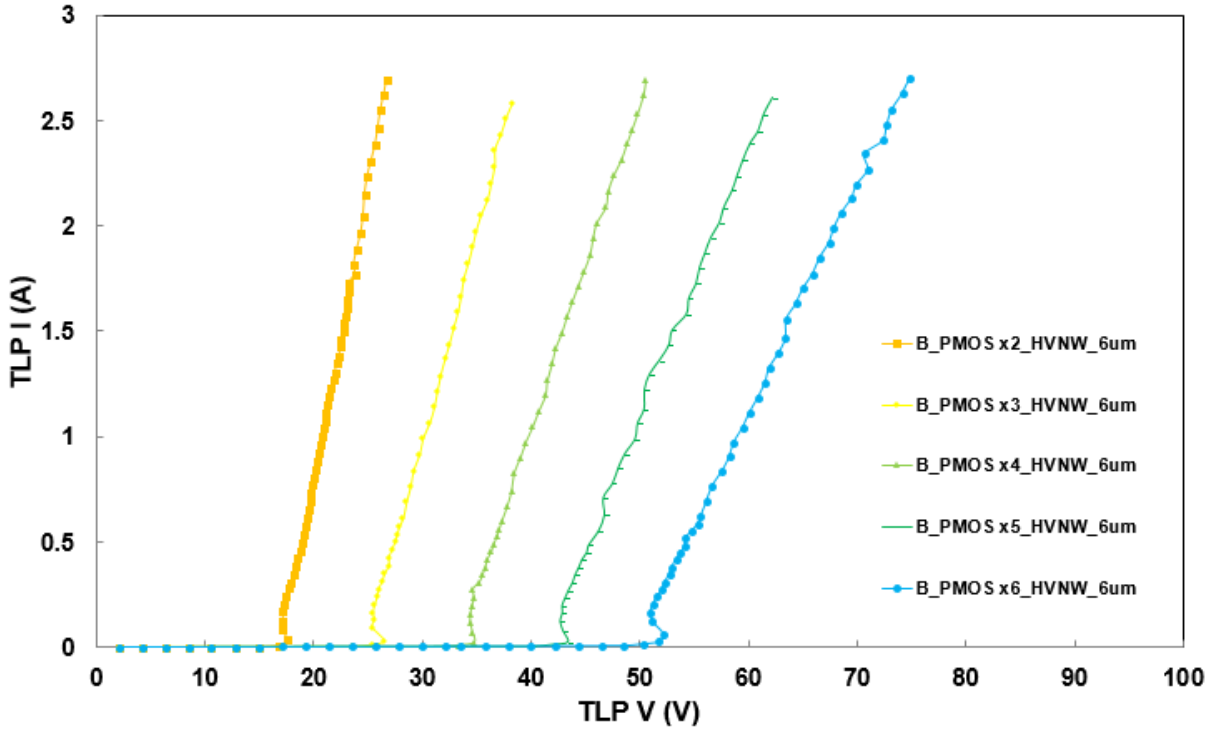


Fig. 3.39 The TLP-measured I-V characteristics of type B (6μm)

Table 3.17

The measurement data of type B (6μm)

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
2 units	17.54	17.05	2.62	16.1	5	300
3 units	26.38	25.31	2.51	24.3	5	350
4 units	34.74	34.35	2.62	32.4	5	350
5 units	43.38	42.67	2.53	40.5	5	350
6 units	52.17	50.97	2.48	48.2	5	350
7 units	-	-	-	49.4	-	-
8 units	-	-	-	48.8	-	-
9 units	-	-	-	50	-	-
10 units	-	-	-	50.2	-	-

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

Table 3.18

The measurement data of type B (4μm)

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
2 units	-	-	-	11.8	-	-
3 units	-	-	-	19.9	-	-
4 units	-	-	-	28.1	-	-
5 units	-	-	-	36.3	-	-
6 units	-	-	-	41.6	-	-
7 units	-	-	-	43	-	-
8 units	-	-	-	44	-	-
9 units	-	-	-	44.4	-	-
10 units	-	-	-	44.8	-	-

#DC BV: I = 1μA

Table 3.19

The measurement data of type B (2μm)

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
2 units	-	-	-	8	-	-
3 units	-	-	-	8	-	-
4 units	-	-	-	8.1	-	-
5 units	-	-	-	-	-	-
6 units	-	-	-	-	-	-
7 units	-	-	-	-	-	-
8 units	-	-	-	-	-	-
9 units	-	-	-	-	-	-
10 units	-	-	-	-	-	-

#DC BV: I = 1μA

The TLP measured I-V characteristics of type C (12μm) are shown in Fig. 3.40. The spacing between each HV-NWELL ring is 12μm. The length of the PWELL is 4μm, and the position of the PWELL is under the middle of the STI between two HV-NWELL rings. The detailed characteristics of type C (12μm) are listed in Table 3.20.

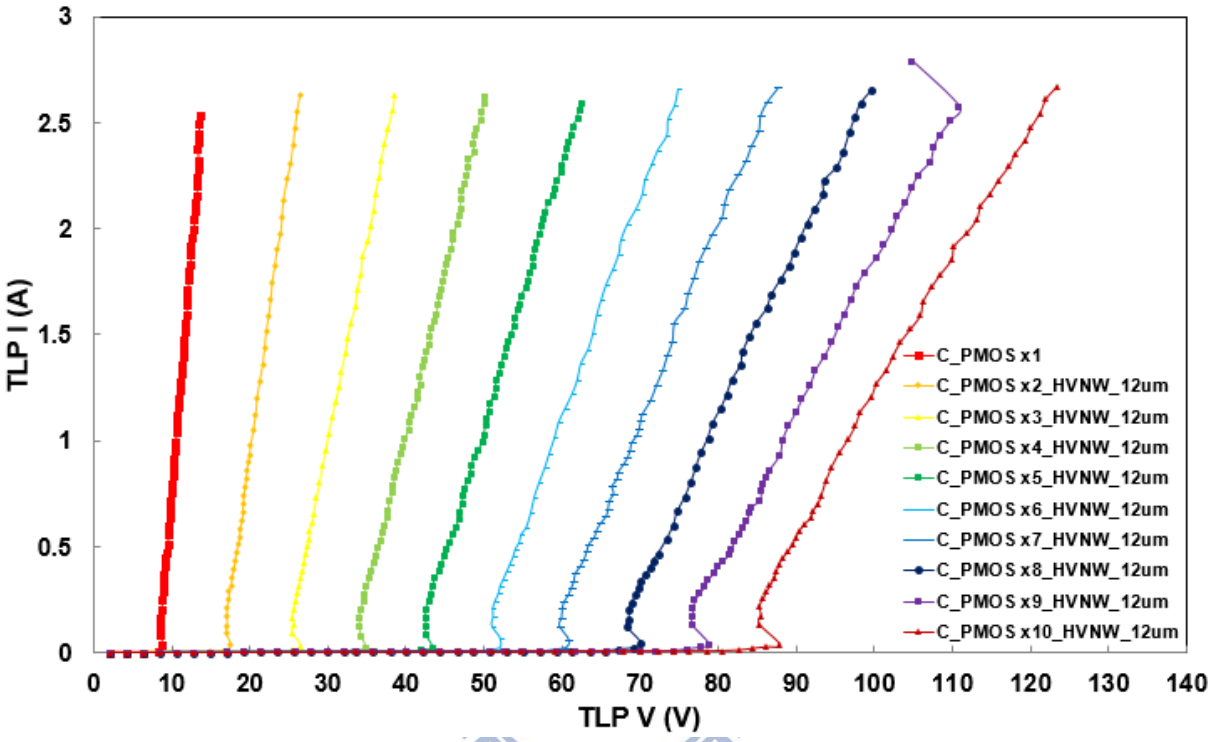


Fig. 3.40 The TLP-measured I-V characteristics of type C (12μm)

Table 3.20

The measurement data of type C (12μm)

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
1 unit	8.72	8.51	2.5	8	5	300
2 units	17.6	16.98	2.55	16.1	5	300
3 units	26.45	25.41	2.56	24.2	5.5	300
4 units	34.79	34.03	2.59	33.2	5	350
5 units	43.43	42.56	2.48	40.5	5	350
6 units	51.96	50.9	2.58	49.2	5	350
7 units	60.86	59.64	2.6	56.6	5	400
8 units	70.13	68.28	2.59	64.8	5	400
9 units	78.82	76.58	2.44	72.8	5	400
10 units	87.9	85.17	2.48	80.8	5	450

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The TLP measured I-V characteristics of type C (11μm) are shown in Fig. 3.41. The length of the PWELL is 3μm. The detailed characteristics of type C (11μm) are listed in Table 3.21.

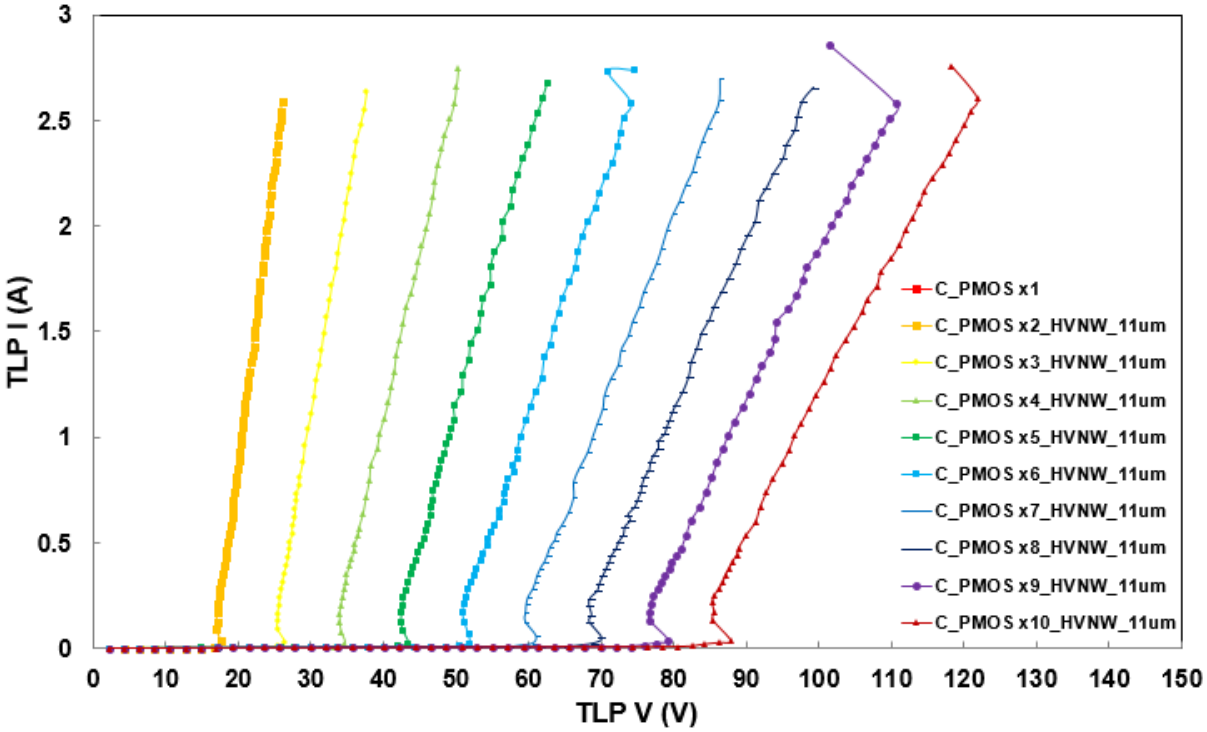


Fig. 3.41 The TLP-measured I-V characteristics of type C (11μm)

Table 3.21

The measurement data of type C (11μm)

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
2 units	17.56	16.99	2.54	16.2	5	300
3 units	26.33	25.32	2.55	24.2	5	300
4 units	34.69	33.93	2.58	32.4	5	350
5 units	43.41	42.43	2.46	40.5	5	350
6 units	51.89	50.97	2.44	48.6	5	350
7 units	60.94	59.48	2.6	56.6	5	400
8 units	70.08	68.32	2.59	64.8	5	400
9 units	79.18	76.66	2.58	72.8	5	400
10 units	87.92	85.32	2.48	81	5	450

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The TLP measured I-V characteristics of type C (10μm) are shown in Fig. 3.42. The length of the PWELL is 2μm. The detailed characteristics of type C (10μm) are listed in Table 3.22.

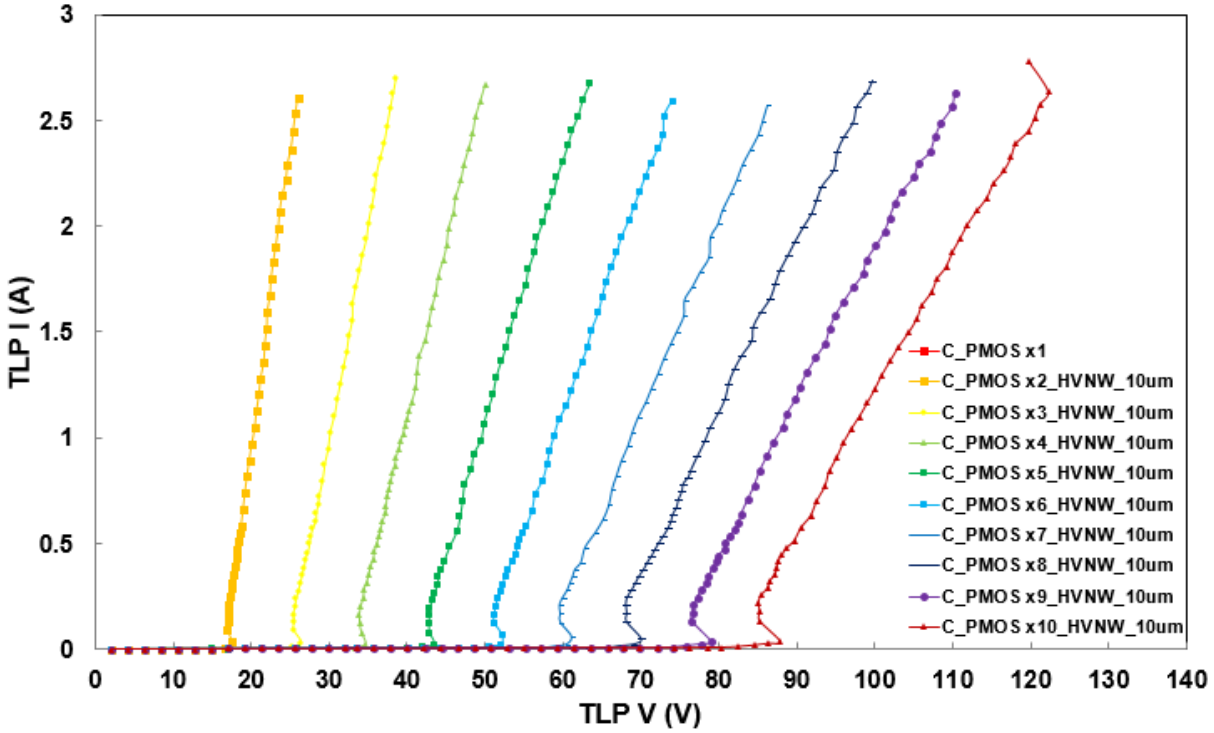


Fig. 3.42 The TLP-measured I-V characteristics of type C (10μm)

Table 3.22

The measurement data of type C (10μm)

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
2 units	17.53	16.96	2.53	16.1	5	300
3 units	26.39	25.33	2.63	24.3	5	300
4 units	34.71	33.9	2.59	32.3	5	300
5 units	43.42	42.73	2.6	40.5	5	350
6 units	52.21	51.17	2.52	48.4	5	350
7 units	61	59.48	2.49	56.6	5.5	400
8 units	69.98	68.02	2.63	64.8	5	400
9 units	78.95	76.56	2.56	72.8	5	400
10 units	87.91	85.1	2.45	81	5	450

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

The TLP measured I-V characteristics of type C (9μm) are shown in Fig. 3.43. The length of the PWELL is 1μm. The detailed characteristics of type C (9μm) are listed in Table 3.23.

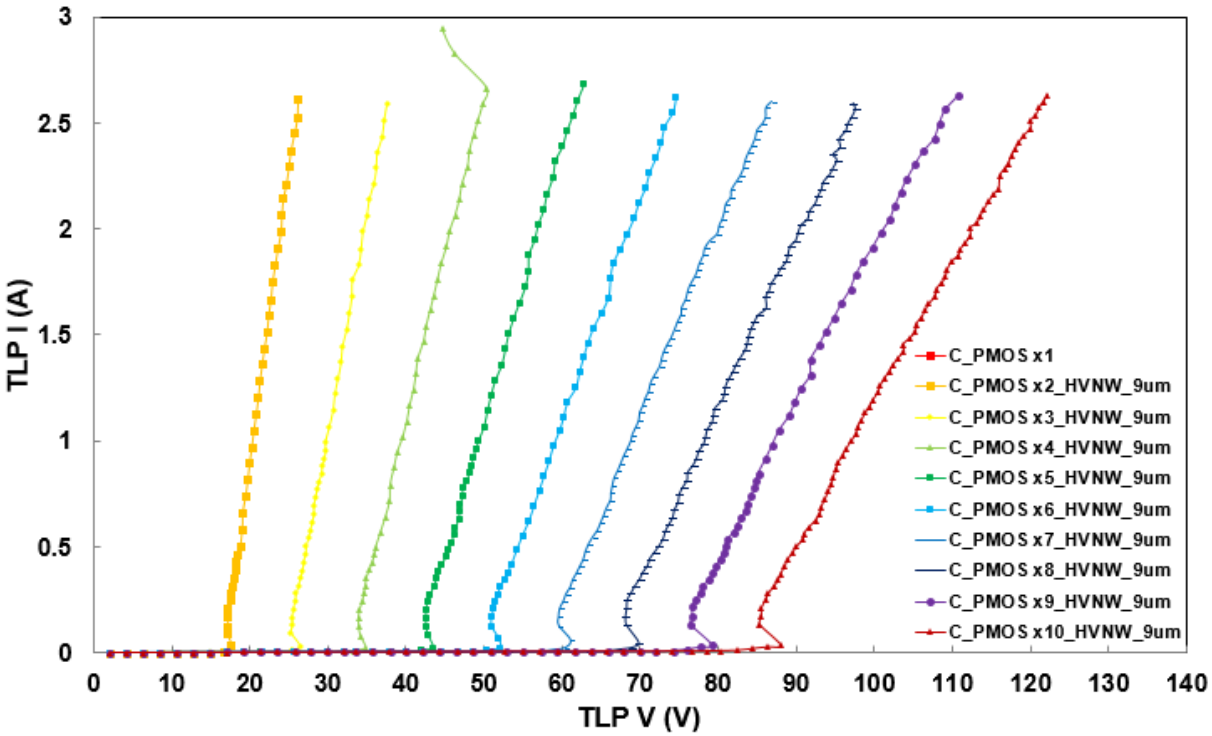


Fig. 3.43 The TLP-measured I-V characteristics of type C (9μm)

Table 3.23

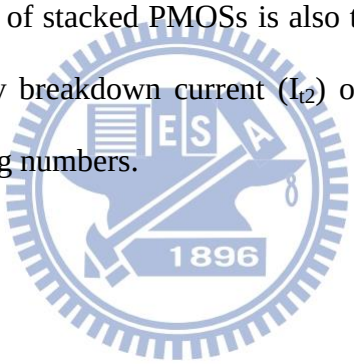
The measurement data of type C (9μm)

	TLP			DC (#)	ESD (*)	
	V_{t1} (V)	V_h (V)	I_{t2} (A)	BV (V)	HBM (kV)	MM (V)
2 units	17.58	17.03	2.52	16.1	5	300
3 units	26.42	25.32	2.51	24.2	5	300
4 units	34.82	33.92	2.59	32.4	5	350
5 units	43.43	42.5	2.61	40.5	5	350
6 units	52.02	50.91	2.55	49.3	5	350
7 units	61.09	59.54	2.57	56.6	5	400
8 units	69.83	68.14	2.56	64.8	5	400
9 units	79.2	76.55	2.43	74	5	400
10 units	88	85.35	2.53	81	5	450

#DC BV: I = 1μA *ESD failure criteria: I-V curve shift > 10%

From table 3.14, table 3.15, table 3.16, and table 3.17 (type B), the DC breakdown voltages of 7-PMOSs are limited by HV-NWELL/PWELL junction. The numbers of stacked PMOSs are 8, 9, and 10, DC breakdown voltages are also limited by HV-NWELL/PWELL junction. From table 3.18, and table 3.19, the DC breakdown voltages of stacked PMOSs are lower. Due to the spacings of HV-NWELL and another HV-NWELL are too closer, the DC breakdown voltages of stacked PMOSs are not the multiple of the DC breakdown voltage of single PMOS.

From table 3.20, table 3.21, table 3.22, and table 3.23 (type C), the DC breakdown voltages of stacked PMOSs are the multiple of the DC breakdown voltage of single PMOS. The total holding voltage of stacked PMOSs is the multiple of the holding voltage of single PMOS. The total trigger voltage of stacked PMOSs is also the multiple of the trigger voltage of single PMOS. The secondary breakdown current (I_{t2}) of stacked PMOSs are almost the same in spite of different stacking numbers.



3.3.3 Discussion

The TLP measured I-V curves of 2-PMOSs with the three types of guard ring layout are shown in Fig. 3.44. The detailed characteristics of 2-PMOSs with different types of guard ring layout are listed in Table 3.24.

Table 3.24 also shows area information. Guard rings occupy lots of area. The total area are composed by LV PMOS area and guard ring area. Higher I_{t2}, smaller total area and higher V_h are important for the stacking purpose, so combine these parameters into the factor, (I_{t2} x V_h)/A, for evaluating performance.

The TLP measured I-V curves of 3-PMOSs with the three types of guard ring layout are shown in Fig. 3.45. The detailed characteristics of 3-PMOSs with different types of guard ring layout are listed in Table 3.25.

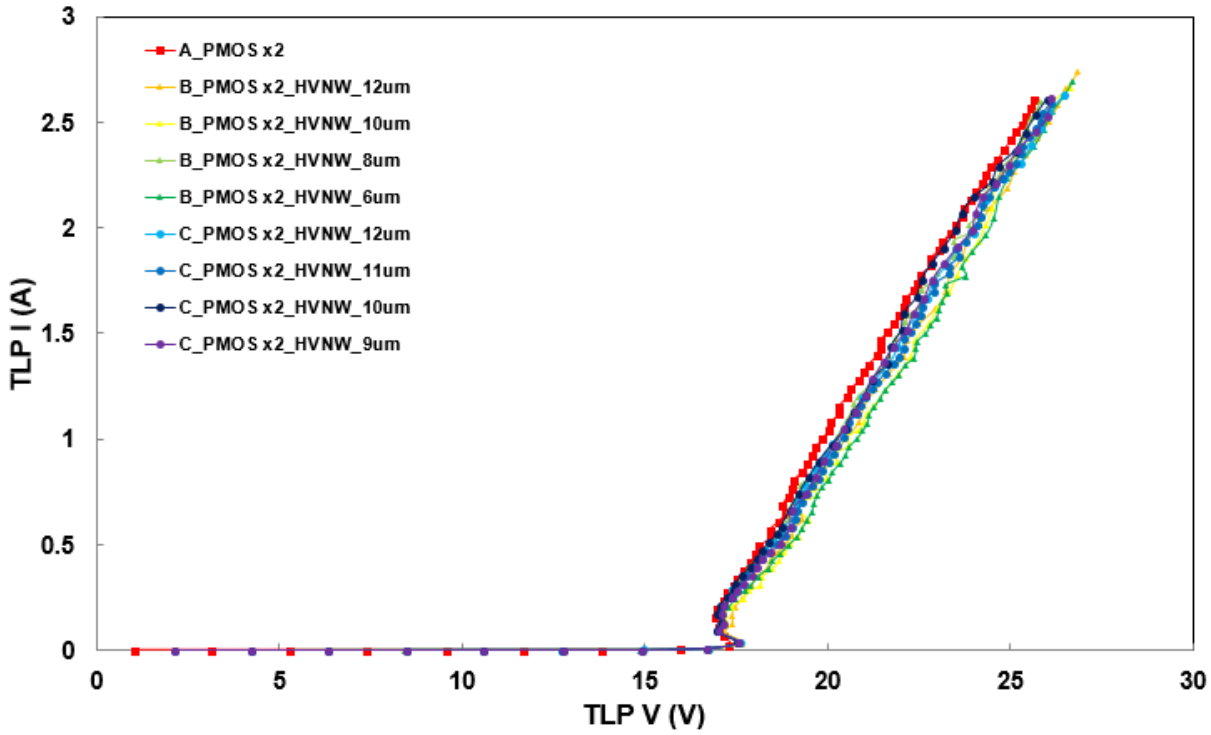


Fig. 3.44 The TLP-measured I-V characteristics of 2-PMOSs with different types of layout

Table 3.24

Area information and comparison of 2-PMOSs

2 unit	HVNW spacing (μm)	DC BV (V)	TLP I_{t2} (A)	Area (μm²)			I_{t2}/ Total area (10^8 A/m²)	(I_{t2}x V_h)/ Total area (10^8 VA/m²)
				LV	Guard ring	Total		
Type A	12	16.5	2.56	4350	9398	13748	1.86	31.51
Type B	12	16.1	2.55	4350	5208	9558	2.67	45.87
	10	16.1	2.54	4350	5055	9405	2.7	46.09
	8	16.2	2.53	4350	4902	9252	2.73	46.33
	6	16.1	2.52	4350	4750	9100	2.77	47.23
	4	11.8	-	4350	4597	8947	-	-
	2	8	-	4350	4444	8794	-	-
Type C	12	16.1	2.66	4350	6884	11234	2.37	40.24
	11	16.2	2.59	4350	6800	11150	2.32	39.42
	10	16.1	2.47	4350	6715	11065	2.23	37.82
	9	16.1	2.62	4350	6631	10981	2.39	40.7

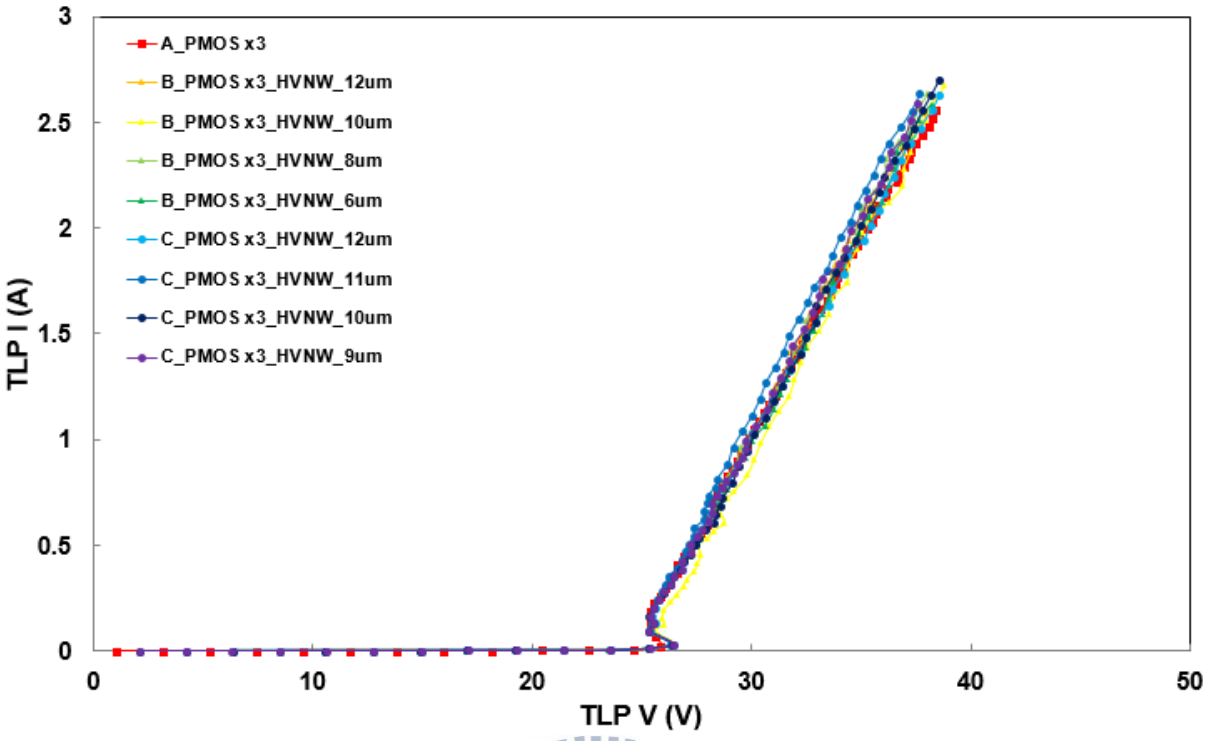


Fig. 3.45 The TLP-measured I-V characteristics of 3-PMOSs with different types of layout

Table 3.25

Area information and comparison of 3-PMOSs

3 unit	HVNW spacing (μm)	DC BV (V)	TLP I_{t2} (A)	Area ($μm^2$)			I_{t2}/ Total area (10^8 A/m^2)	(I_{t2} x V_h)/ Total area (10^8 VA/m^2)
				LV	Guard ring	Total		
Type A	12	24.9	2.52	6525	13763	20288	1.24	31.48
Type B	12	24.2	2.54	6525	8270	14795	1.72	43.64
	10	24.2	2.59	6525	7964	14489	1.79	45.91
	8	24.3	2.56	6525	7659	14184	1.8	45.61
	6	24.3	2.51	6525	7354	13879	1.81	45.81
Type C	12	24.2	2.56	6525	10495	17020	1.5	38.12
	11	24.2	2.55	6525	10326	16851	1.51	38.23
	10	24.3	2.63	6525	10157	16682	1.58	40.02
	9	24.2	2.51	6525	9989	16514	1.52	38.49

The TLP measured I-V curves of 4-PMOSs with the three types of guard ring layout are shown in Fig. 3.46. The detailed characteristics of 4-PMOSs with different types of guard ring layout are listed in Table 3.26.

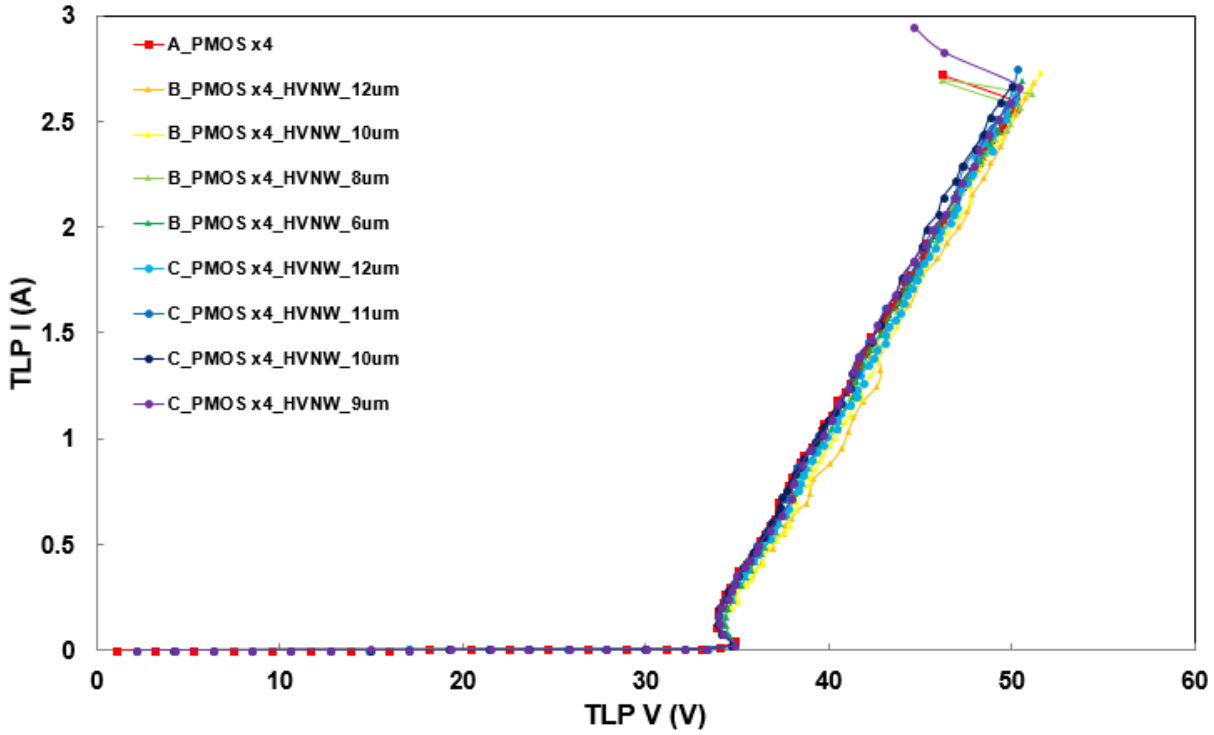


Fig. 3.46 The TLP-measured I-V characteristics of 4-PMOSs with different types of layout

Table 3.26

Area information and comparison of 4-PMOSs

4 unit	HVNW spacing (μm)	DC BV (V)	TLP I_{t2} (A)	Area (μm^2)			I_{t2}/ Total area (10^8 A/m^2)	(I_{t2} x V_h)/ Total area (10^8 VA/m^2)
				LV	Guard ring	Total		
Type A	12	32.4	2.56	8700	18129	26829	0.95	32.13
Type B	12	32.3	2.53	8700	13332	22032	1.15	39.28
	10	32.3	2.58	8700	10874	19574	1.32	45.03
	8	32.4	2.69	8700	10416	19116	1.41	47.94
	6	32.4	2.62	8700	9957	18657	1.4	48.09
Type C	12	33.2	2.59	8700	14106	22806	1.14	38.79
	11	32.4	2.58	8700	13853	22553	1.14	38.68
	10	32.3	2.59	8700	13599	22299	1.16	39.32
	9	32.4	2.59	8700	13346	22046	1.17	39.69

The TLP measured I-V curves of 5-PMOSs with the three types of guard ring layout are shown in Fig. 3.47. The detailed characteristics of 5-PMOSs with different types of guard ring layout are listed in Table 3.27.

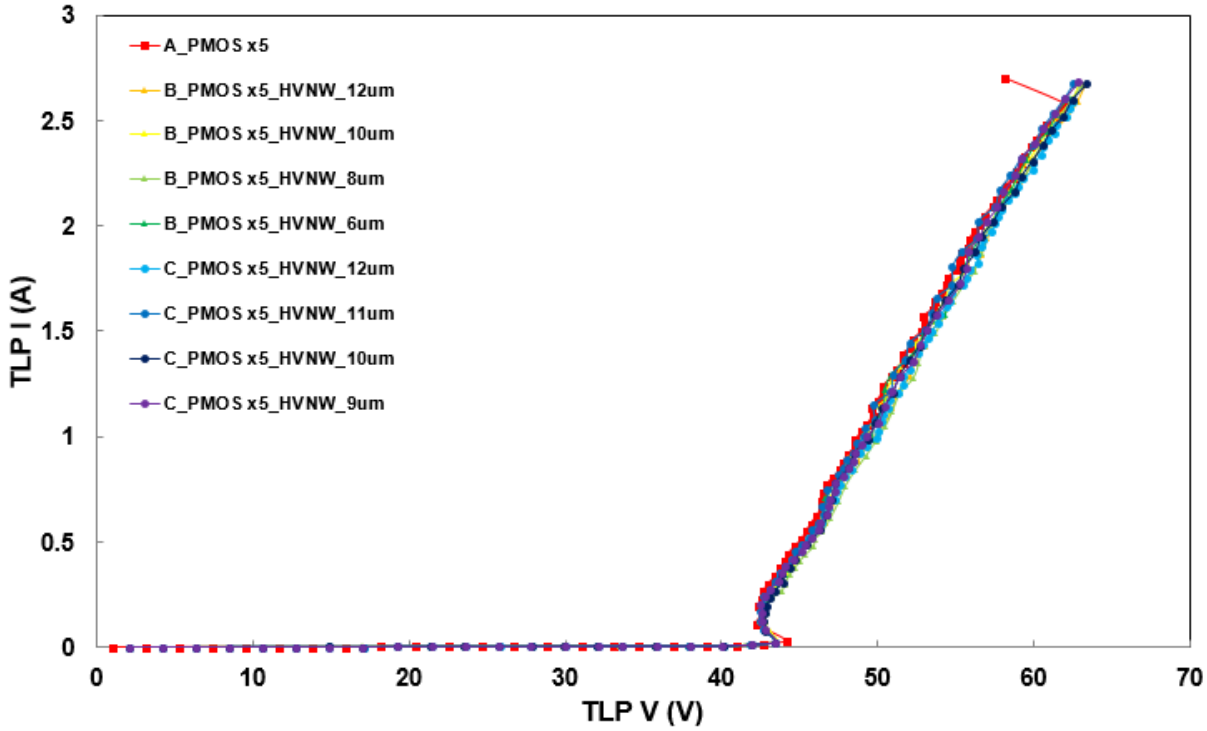


Fig. 3.47 The TLP-measured I-V characteristics of 5-PMOSs with different types of layout

Table 3.27

Area information and comparison of 5-PMOSs

5 unit	HVNW spacing (μm)	DC BV (V)	TLP I_{t2} (A)	Area (μm^2)			I_{t2}/ Total area (10^8 A/m^2)	(I_{t2}x V_h)/ Total area (10^8 VA/m^2)
				LV	Guard ring	Total		
Type A	12	40.5	2.51	10875	22494	33369	0.75	31.7
Type B	12	40.4	2.45	10875	14394	25269	0.97	41.24
	10	40.5	2.6	10875	13783	24658	1.05	44.94
	8	40.5	2.6	10875	13172	24047	1.08	45.93
	6	40.5	2.53	10875	12561	23436	1.08	46.08
Type C	12	40.5	2.48	10875	17716	28591	0.87	37.03
	11	40.5	2.46	10875	17379	28254	0.87	36.91
	10	40.5	2.6	10875	17042	27917	0.93	39.74
	9	40.5	2.61	10875	16704	27579	0.95	40.38

The TLP measured I-V curves of 6-PMOSs with the three types of guard ring layout are shown in Fig. 3.48. The detailed characteristics of 6-PMOSs with different types of guard ring layout are listed in Table 3.28.

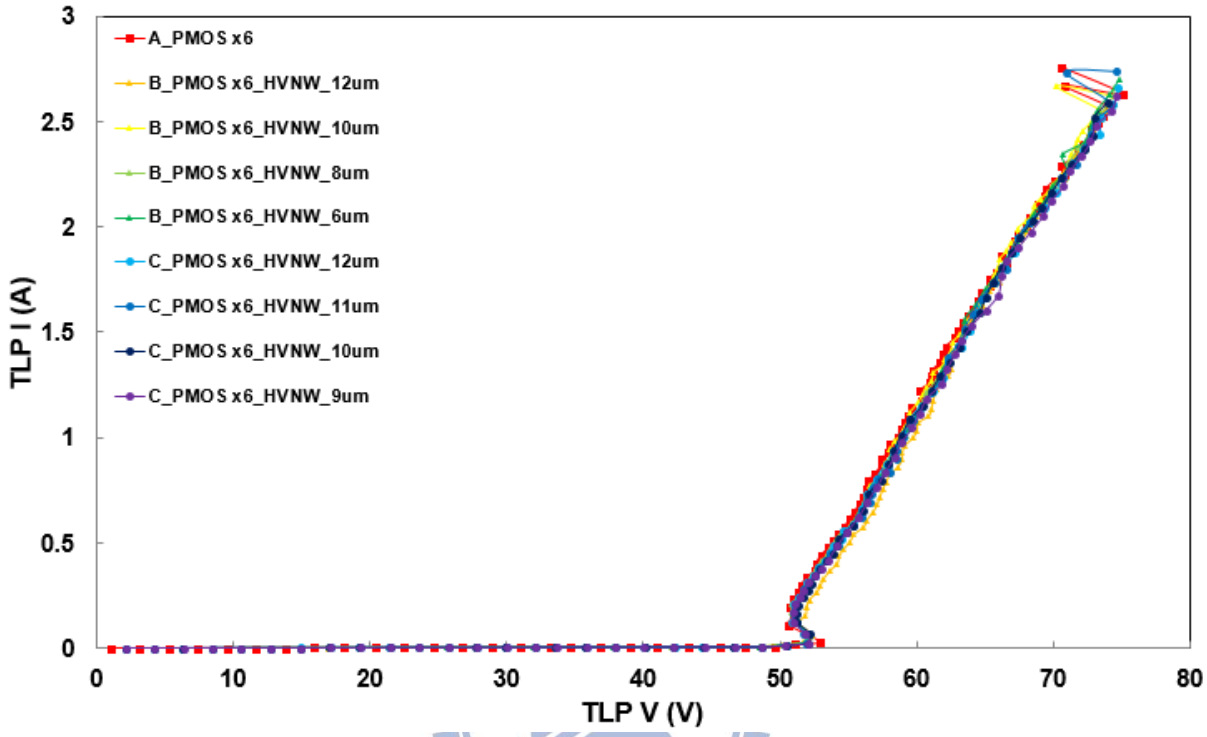


Fig. 3.48 The TLP-measured I-V characteristics of 6-PMOSs with different types of layout

Table 3.28

Area information and comparison of 6-PMOSs

6 unit	HVNW spacing (μm)	DC BV (V)	TLP I_{t2} (A)	Area (μm^2)			I_{t2}/ Total area (10^8 A/m^2)	(I_{t2} x V_h)/ Total area (10^8 VA/m^2)
				LV	Guard ring	Total		
Type A	12	48.6	2.5	13050	26859	39909	0.63	31.89
Type B	12	48.4	2.55	13050	17455	30505	0.84	43.12
	10	48.4	2.49	13050	16692	29742	0.74	37.81
	8	48.6	2.59	13050	15929	28979	0.89	45.26
	6	48.2	2.48	13050	15165	28215	0.88	44.85
Type C	12	49.2	2.58	13050	21327	34377	0.75	38.18
	11	48.6	2.44	13050	20905	33955	0.72	36.7
	10	48.4	2.52	13050	20484	33534	0.75	38.38
	9	49.3	2.55	13050	20062	33112	0.77	39.2

The TLP measured I-V curves of 7-PMOSs with the three types of guard ring layout are shown in Fig. 3.49. The detailed characteristics of 7-PMOSs with different types of guard ring layout are listed in Table 3.29.

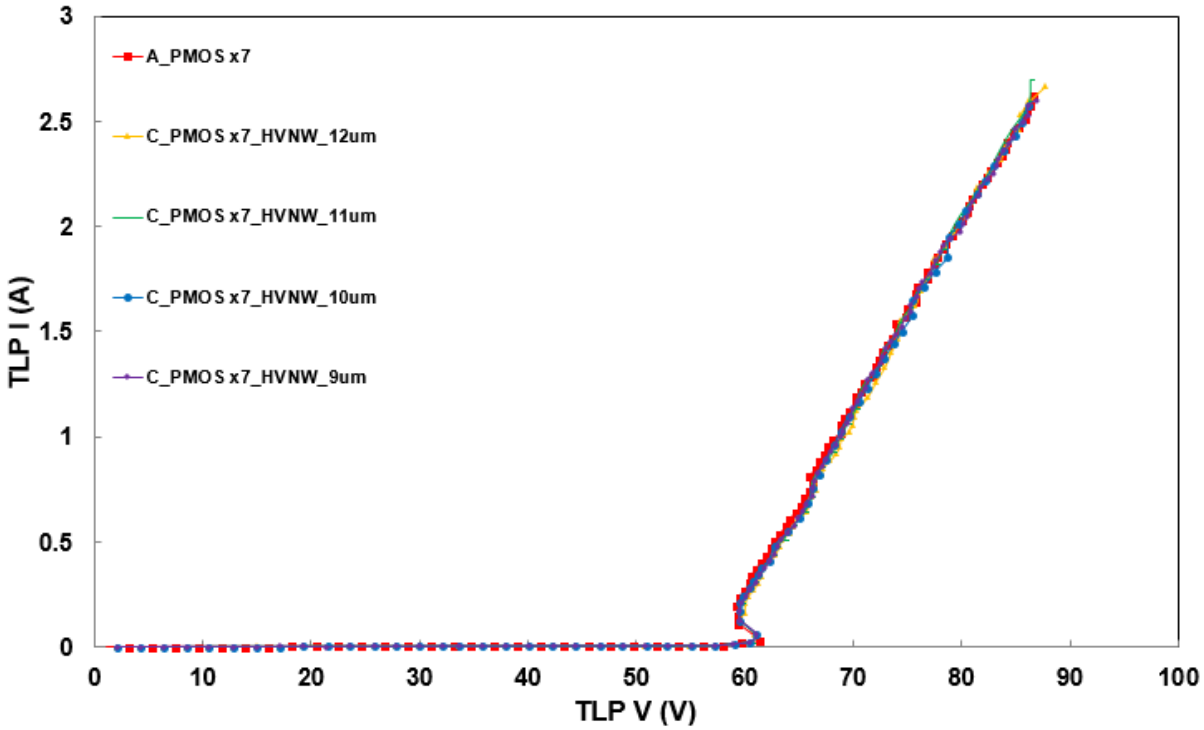


Fig. 3.49 The TLP-measured I-V characteristics of 7-PMOSs with different types of layout

Table 3.29

Area information and comparison of 7-PMOSs

7 unit	HVNW spacing (μm)	DC BV (V)	TLP I_{t2} (A)	Area (μm^2)			I_{t2}/ Total area (10^8 A/m^2)	(I_{t2} x V_h)/ Total area (10^8 VA/m^2)
				LV	Guard ring	Total		
Type A	12	56.6	2.57	15525	30925	46450	0.55	32.58
Type B	12	52	2.5	15525	20217	35742	0.7	42.06
	10	51.2	2.47	15525	19301	34826	0.71	42.42
	8	51	-	15525	18385	33910	-	-
	6	49.4	-	15525	17469	32994	-	-
Type C	12	56.6	2.6	15525	24638	40163	0.65	38.77
	11	56.6	2.6	15525	24132	39657	0.66	39.26
	10	56.6	2.49	15525	23626	39151	0.64	38.07
	9	56.6	2.57	15525	23120	38645	0.67	39.89

The TLP measured I-V curves of 8-PMOSs with the three types of guard ring layout are shown in Fig. 3.50. The detailed characteristics of 8-PMOSs with different types of guard ring layout are listed in Table 3.30.

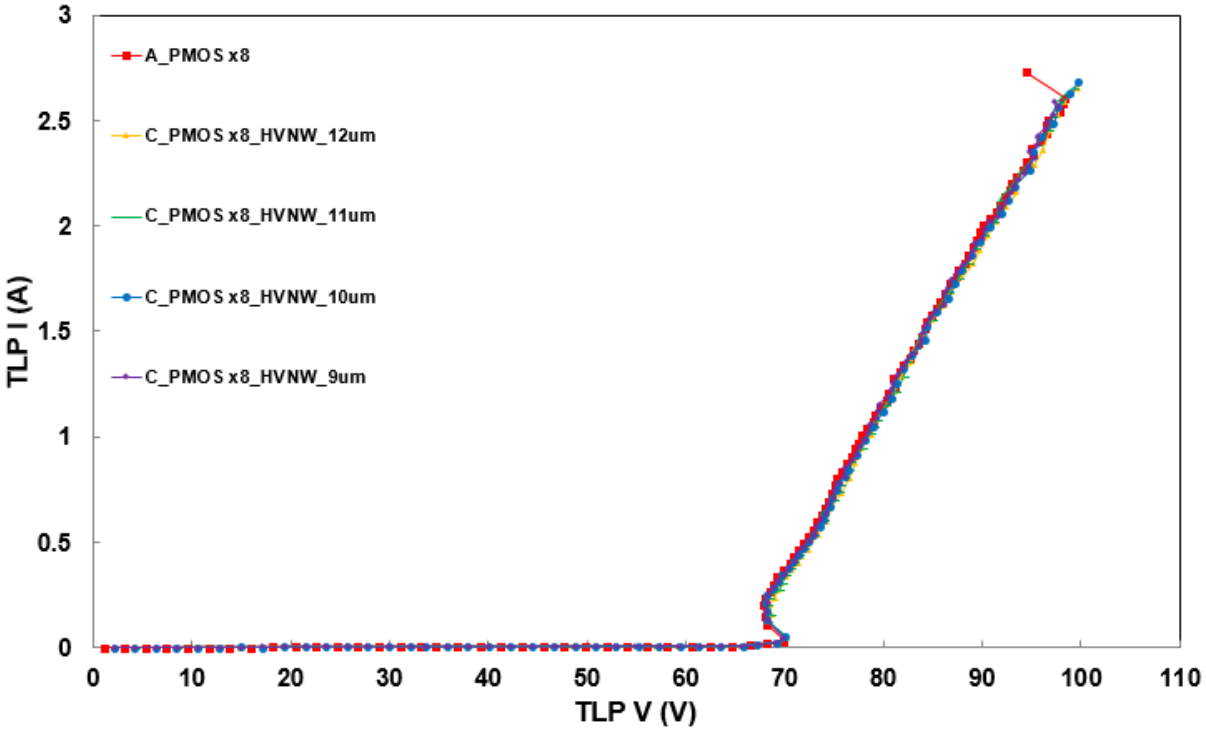


Fig. 3.50 The TLP-measured I-V characteristics of 8-PMOSs with different types of layout

Table 3.30

Area information and comparison of 8-PMOSs

8 unit	HVNW spacing (μm)	DC BV (V)	TLP I_{t2} (A)	Area (μm²)			I_{t2}/ Total area (10^8 A/m²)	(I_{t2}x V_h)/ Total area (10^8 VA/m²)
				LV	Guard ring	Total		
Type A	12	64.8	2.54	17400	35590	52990	0.48	32.53
Type B	12	52	2.6	17400	23579	40979	0.63	43
	10	51.2	-	17400	22511	39911	-	-
	8	51.2	-	17400	21442	38842	-	-
	6	48.8	-	17400	20373	37773	-	-
Type C	12	64.8	2.59	17400	28548	45948	0.56	38.24
	11	64.8	2.59	17400	27958	45358	0.57	38.94
	10	64.8	2.63	17400	27368	44768	0.59	40.13
	9	64.8	2.56	17400	26777	44177	0.58	39.52

The TLP measured I-V curves of 9-PMOSs with the three types of guard ring layout are shown in Fig. 3.51. The detailed characteristics of 9-PMOSs with different types of guard ring layout are listed in Table 3.31.

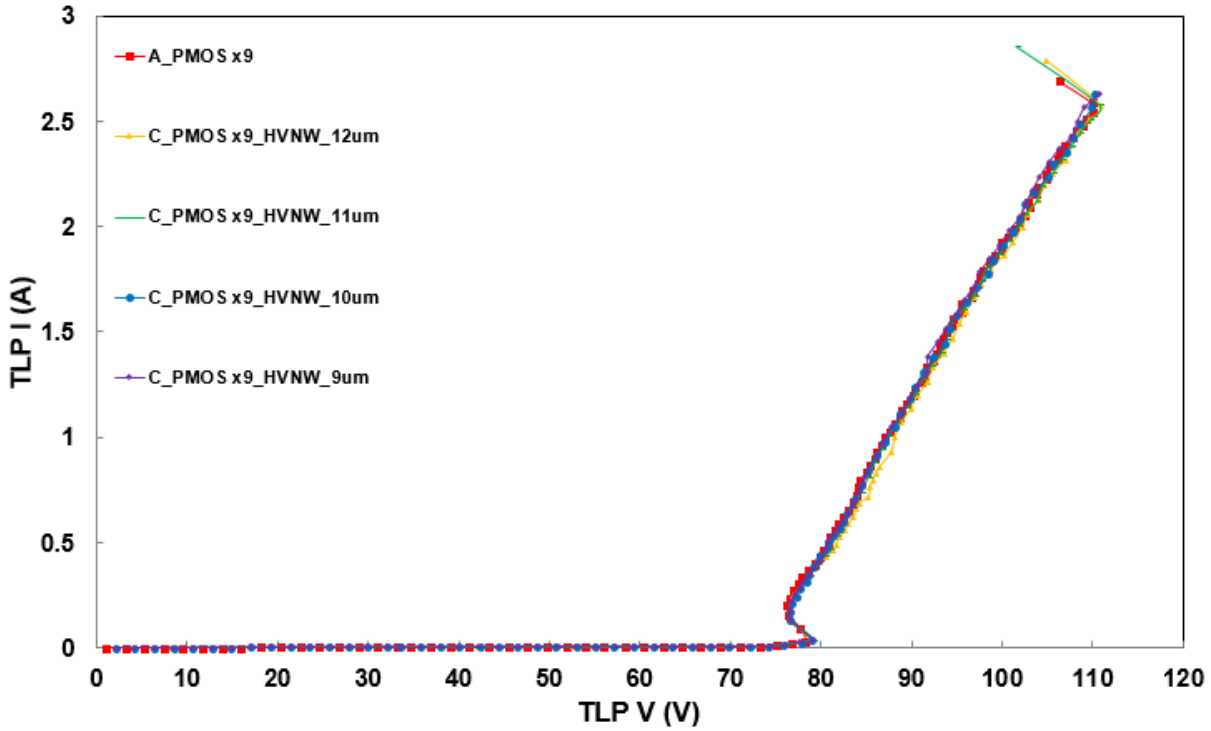


Fig. 3.51 The TLP-measured I-V characteristics of 9-PMOSs with different types of layout

Table 3.31

Area information and comparison of 9-PMOSs

9 unit	HVNW spacing (μm)	DC BV (V)	TLP I_{t2} (A)	Area (μm^2)			I_{t2}/ Total area (10^8 A/m^2)	(I_{t2}x V_h)/ Total area (10^8 VA/m^2)
				LV	Guard ring	Total		
Type A	12	73	2.51	19575	39955	59530	0.42	32.02
Type B	12	52	2.58	19575	26641	46216	0.56	43.12
	10	51.4	-	19575	25420	44995	-	-
	8	51.4	-	19575	24198	43773	-	-
	6	50	-	19575	22977	42552	-	-
Type C	12	72.8	2.44	19575	32159	51734	0.47	35.99
	11	72.8	2.58	19575	31484	51059	0.51	39.1
	10	72.8	2.56	19575	30810	50385	0.58	44.4
	9	74	2.43	19575	30135	49710	0.49	37.51

The TLP measured I-V curves of 10-PMOSs with the three types of guard ring layout are shown in Fig. 3.52. The detailed characteristics of 10-PMOSs with different types of guard ring layout are listed in Table 3.32.

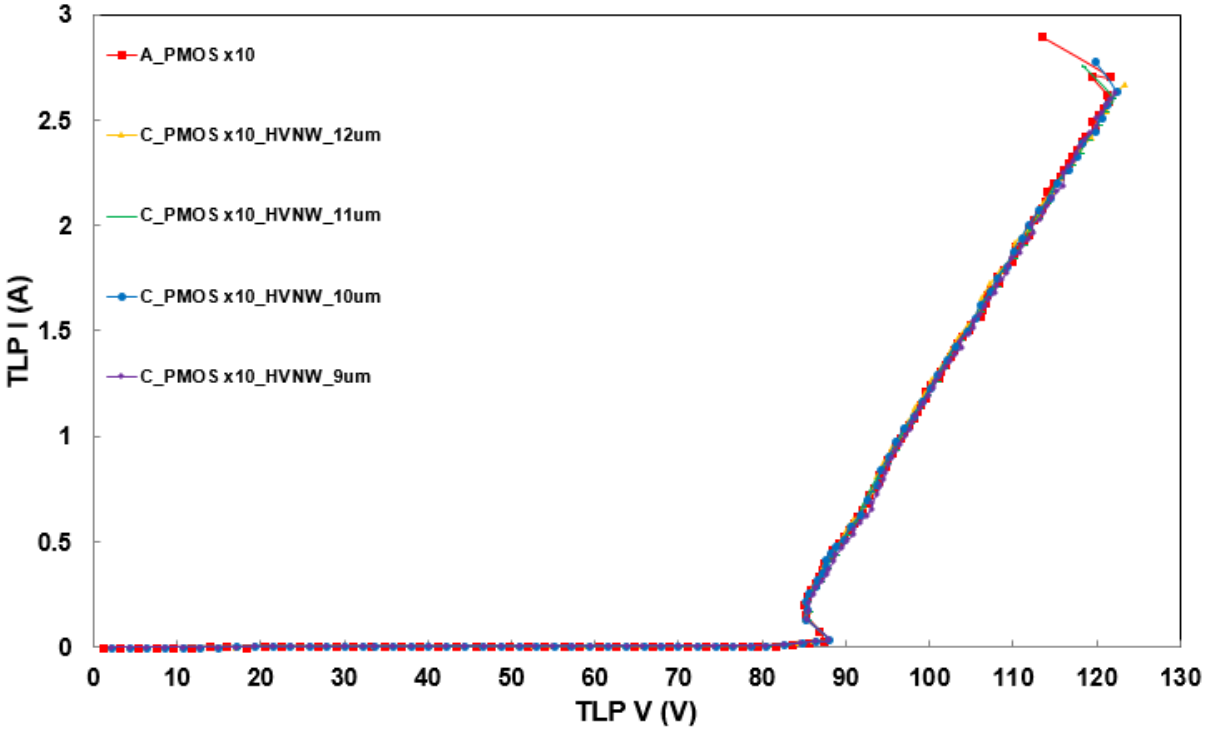


Fig. 3.52 The TLP-measured I-V characteristics of 10-PMOSs with different types of layout

Table 3.32

Area information and comparison of 10-PMOSs

10 unit	HVNW spacing (μm)	DC BV (V)	TLP I_{t2} (A)	Area (μm²)			I_{t2}/ Total area (10^8 A/m²)	(I_{t2}x V_h)/ Total area (10^8 VA/m²)
				LV	Guard ring	Total		
Type A	12	81	2.71	21750	44321	66071	0.41	34.84
Type B	12	52	2.64	21750	29703	51453	0.51	43.75
	10	51.6	-	21750	28329	50079	-	-
	8	51.4	-	21750	26955	48705	-	-
	6	50.2	-	21750	25581	47331	-	-
Type C	12	80.8	2.48	21750	35770	57520	0.43	36.62
	11	81	2.48	21750	35011	56761	0.44	37.54
	10	81	2.45	21750	34252	56002	0.44	37.44
	9	81	2.53	21750	33493	55243	0.46	39.26

From above tables, the numbers of stacked PMOSs are from two to six, the type B of guard ring layout is good choice for ESD protection. The factor, (I_{t2} x V_h)/A, of the type B gets higher value, and the value of the type A is smallest. The type B performs best in this factor, and is suitable for the number of stacked PMOSs from two to six. However, the numbers of stacked PMOSs are from seven to ten, the DC breakdown voltages of stacked PMOSs are lower than expected supply voltages. The type C performs best in this factor, and is suitable for the number of stacked PMOSs from seven to ten.

Table 3.33 shows the type A (typical) for stacked PMOSs can multi-finger uniform turn-on. Table 3.34 shows the type B (12μm) for stacked PMOSs can multi-finger uniform turn-on. Table 3.35 shows the type C (12μm) for stacked PMOSs also can multi-finger uniform turn-on.

Table 3.33
Multi-finger uniform turn-on of type A (typical)

	V_{t1} (V)	V_h (V)	I_{t2} (A)	Total Area (μm^2)	I_{t2}/ Total area (10^8 A/m^2)	(I_{t2}x V_h)/ Total area (10^8 VA/m^2)
2 units	17.3	16.94	2.56	13748	1.86	31.51
3 units	25.85	25.39	2.52	20288	1.24	31.48
4 units	34.88	33.83	2.56	26829	0.95	32.13
5 units	44.12	42.27	2.51	33369	0.75	31.7
6 units	52.87	50.62	2.5	39909	0.63	31.89
7 units	61.33	59.24	2.57	46450	0.55	32.58
8 units	69.88	67.77	2.54	52990	0.48	32.53
9 units	78.29	76.24	2.51	59530	0.42	32.02
10 units	87.25	84.98	2.71	66071	0.41	34.84

Table 3.34

Multi-finger uniform turn-on of type B (12μm)

HVNW spacing 12μm	V_{t1} (V)	V_h (V)	I_{t2} (A)	Total Area (μm^2)	I_{t2}/ Total area (10^8 A/m²)	(I_{t2}x V_h)/ Total area (10^8 VA/m²)
2 units	17.66	17.18	2.66	9558	2.67	45.87
3 units	26.42	25.37	2.54	14795	1.72	43.64
4 units	34.76	34.16	2.53	22032	1.15	39.28
5 units	43.42	42.52	2.45	25269	0.97	41.24
6 units	52.36	51.33	2.55	30505	0.84	43.12

Table 3.35

Multi-finger uniform turn-on of type C (12μm)

HVNW spacing 12μm	V_{t1} (V)	V_h (V)	I_{t2} (A)	Total Area (μm^2)	I_{t2}/ Total area (10^8 A/m²)	(I_{t2}x V_h)/ Total area (10^8 VA/m²)
2 units	17.6	16.98	2.55	11234	2.37	40.24
3 units	26.45	25.41	2.56	17020	1.5	38.12
4 units	34.79	34.03	2.59	22806	1.14	38.79
5 units	43.43	42.56	2.48	28591	0.87	37.03
6 units	51.96	50.9	2.58	34377	0.75	38.18
7 units	60.86	59.64	2.6	40163	0.65	38.77
8 units	70.13	68.28	2.59	45948	0.56	38.24
9 units	78.82	76.58	2.44	51734	0.47	35.99
10 units	87.9	85.17	2.48	57520	0.43	36.62

From above tables, the factor, (I_{t2} x V_h)/A, of the type A almost gets same value. The type B and the type C also gets similar value, respectively. The stacked PMOSs with different guard ring layout types can turn-on uniformity. It is good for high-voltage ESD protection.

The holding voltages (V_h) and secondary breakdown current (I_{t2}) of stacking number _type A are shown in Fig. 3.53.

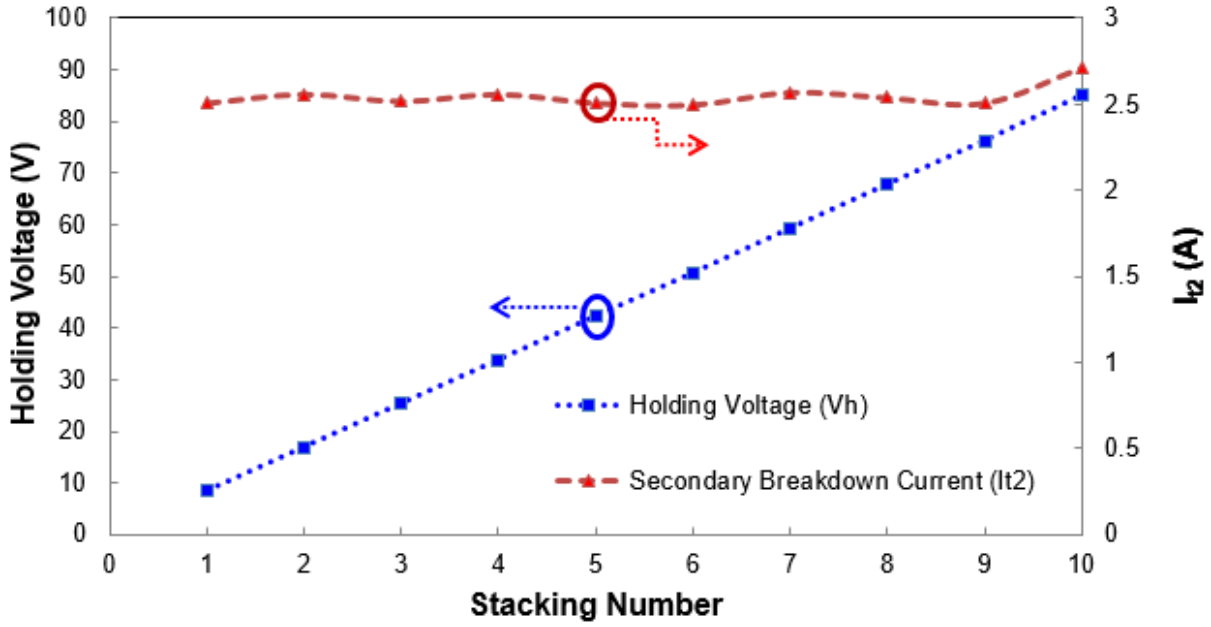


Fig. 3.53 The V_h and I_{t2} of stacked PMOSs with the type A of guard ring layout

The holding voltages (V_h) and secondary breakdown current (I_{t2}) of stacking number _type B are shown in Fig. 3.54.

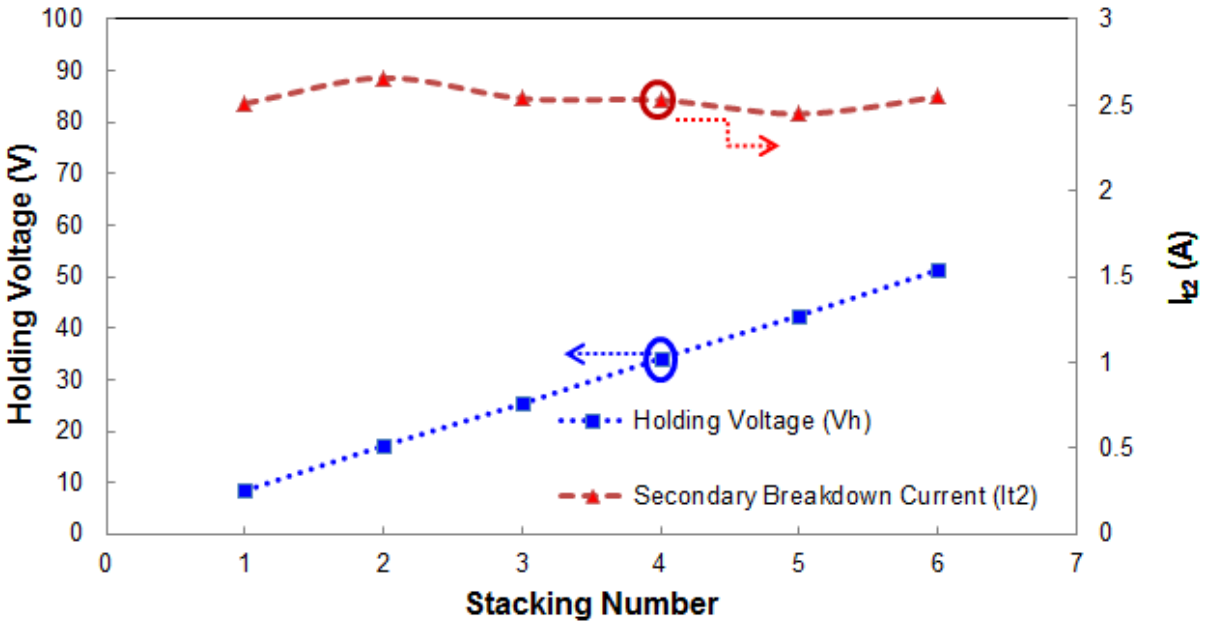


Fig. 3.54 The V_h and I_{t2} of stacked PMOSs with the type B of guard ring layout

The holding voltages (V_h) and secondary breakdown current (I_{t2}) of stacking number _type C are shown in Fig. 3.55.

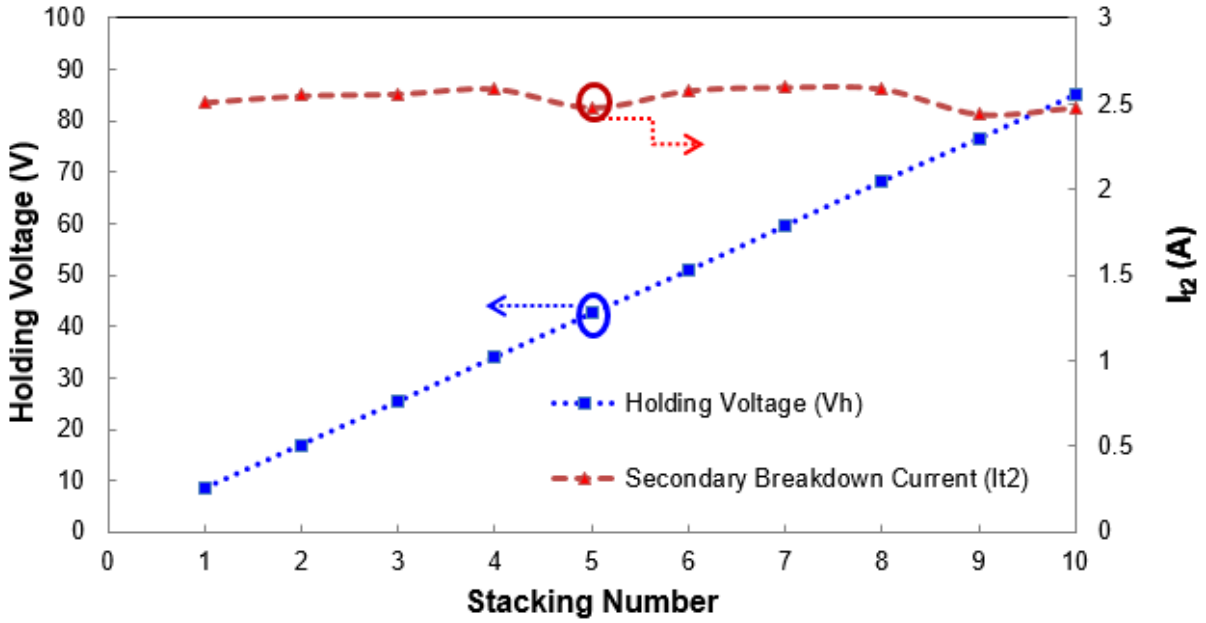


Fig. 3.55 The V_h and I_{t2} of stacked PMOSs with the type C of guard ring layout

In the three types of different guard ring layout, the total holding voltage of stacked PMOSs is the multiple of the holding voltage of single PMOS. The secondary breakdown current (I_{t2}) of stacked PMOSs are almost the same in spite of different stacking numbers. The type B and type C can reduce the layout area, and they have the same ESD robustness with the type A.

For high-voltage ESD protection, the TLP measured I-V curves of 60V ESD devices are shown in Fig. 3.56. 60V ESD devices include the 60V typical HV PMOS and the type C_PMOS x8_HVNW_12μm. The 60V typical HV PMOS is drawn with the total width of 5000μm and a channel length of 0.45μm. Each LV PMOS in the stacked configuration is drawn with the total width of 360μm and a channel length of 0.8μm. The detailed characteristics of 60V ESD devices are listed in Table 3.36.

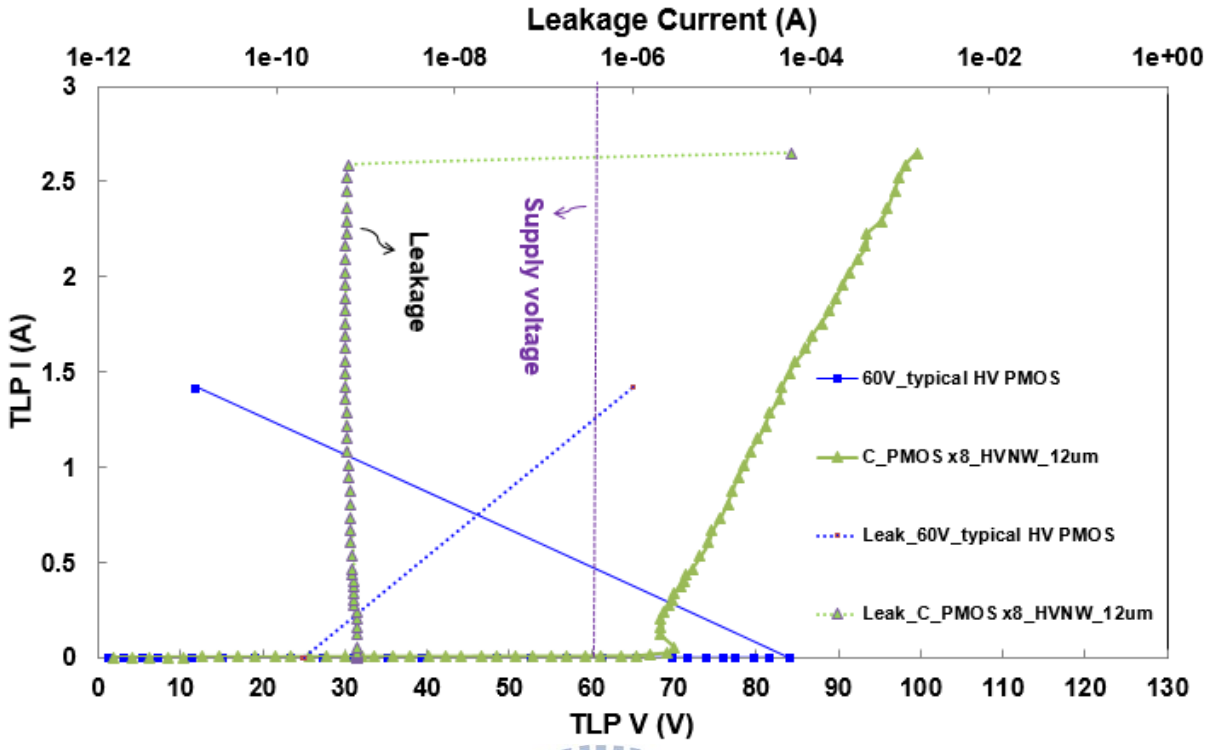


Fig. 3.56 The TLP-measured I-V characteristics of 60V ESD devices

Table 3.36

Summary of 60V ESD devices

		DC	TLP			ESD (wafer level)		Size		
		V_{BD} @1μA (V @1μA)	V_{t1} (V)	V_h (V)	I_{t2} (A)	HBM (+) (kV)	MM (+) (V)	Total Area (μm²)	I_{t2}/ Total area (10^8 A/m²)	(I_{t2}x V_h)/ Total area (10^8 VA/m²)
60 V	Typical HV PMOS W/L=5000μm/ 0.45μm	87.2	83.9	-	0	<0.5	<50	47624	-	-
	PMOS x8 - type C (12μm) W/L=360μm/0.8μm	64.8	70.13	68.28	2.59	5	400	45948	0.56	38.24

For high-voltage ESD protection, the TLP measured I-V curves of 80V ESD devices are shown in Fig. 3.57. 80V ESD devices include the 80V typical HV PMOS and the type C_PMOS x10_HVNW_12μm. The 80V typical HV PMOS is drawn with the total width of

5000μm and a channel length of 0.45μm. Each LV PMOS in the stacked configuration is drawn with the total width of 360μm and a channel length of 0.8μm. The detailed characteristics of 80V ESD devices are listed in Table 3.37.

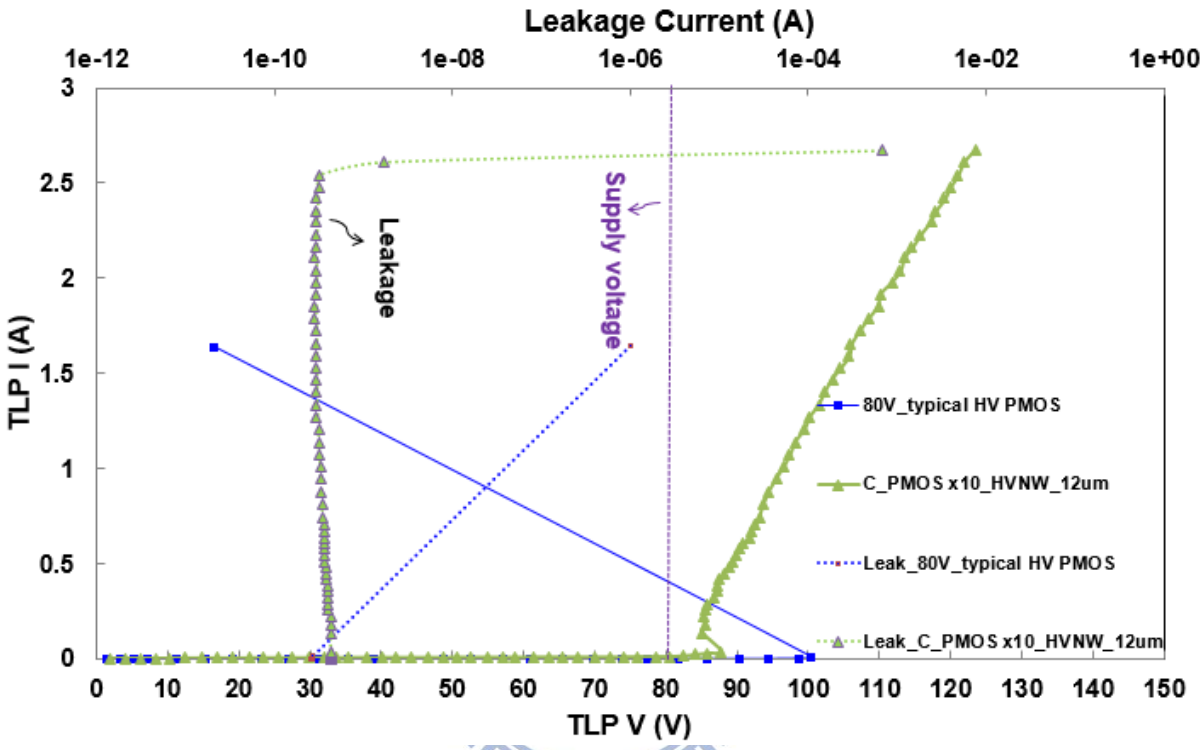


Fig. 3.57 The TLP-measured I-V characteristics of 80V ESD devices

Table 3.37

Summary of 80V ESD devices

		DC	TLP			ESD (wafer level)		Size		
		V_{BD} @1μA (V @1μA)	V_{t1} (V)	V_h (V)	I_{t2} (A)	HBM (+) (kV)	MM (+) (V)	Total Area(μm²)	I_{t2}/ Total area (10^8 A/m²)	(I_{t2}x V_h)/ Total area (10^8 VA/m²)
80 V	Typical HV PMOS W/L=5000μm/ 0.45μm	103	100.26	-	0.01	<0.5	<50	65474	0.02	-
	PMOS x10 - type C (12μm) W/L=360μm/0.8μm	80.8	87.9	85.17	2.48	5	450	57520	0.43	36.62

The typical HV devices have larger layout area, but they have lower ESD robustness. After the trigger voltages, the typical HV devices are failed. However, stacked PMOSs have high holding voltage and good ESD robustness. The stacked PMOSs are the best choice for HV ESD protection.

3.4 Summary

Stacked PMOSs with different guar-ring layouts has been investigated in a 0.5-μm HV process for HV applications. From above results with TLP-measured I_{t2} and ESD test, the type D among the four types of guard-ring layout is the best choice for the stacked PMOSs structure for HV ESD protection. The stacked PMOSs with guard-ring layout of type D can achieve both of good ESD robustness and high latchup-free immunity with reasonable total layout area.

Stacked PMOSs were verified in a VIS 0.25-μm BCD process. From the chapter 3.3, the type B and type C have same ESD robustness with the type A (typical), but they have smaller layout area. By adjusting the stacking numbers of stacked PMOSs, it can provide effectively ESD protection for various HV applications. The stacked configuration of LV PMOSs with optimized guard-ring layout is recommended for on-chip ESD protection design in HV IC products.

Chapter 4

Conclusions and Future Work

4.1 Conclusions

Stacked PMOSs have been verified their good ESD robustness with high holding voltage. The dependence of layout parameters on ESD robustness of stacked LV PMOSs. In this work, the stacked LV PMOS devices have been successfully verified in a VIS 0.5-μm HV process and 0.25-μm 80V BCD process. Stacked LV PMOSs have better ESD robustness in different HV process.

Stacked PMOSs with different guar-ring layouts has been investigated in a 0.5-μm HV process for HV applications. From the chapter 3.1 and 3.2, the stacked PMOSs with guard-ring layout of type D can achieve both of good ESD robustness and high latchup-free immunity with reasonable total layout area. By adjusting the stacking numbers of stacked PMOSs, it can provide effectively ESD protection for various HV applications. Stacked PMOSs with different guar-ring layouts has been investigated in a 0.25-μm BCD process for HV applications. The ESD devices should be surrounded by the guard ring in real circuit application. The ESD device can reduce the layout area, and it can achieve same ESD robustness and high latchup-free immunity.

4.2 Future Work

4.2.1 New Type Device

The cross-sectional view of stacked structure with two LV PMOSs is shown in Fig. 4.1. The new type device have not PWELL under the STI. The DC breakdown voltage is not limited by HVNW/PWELL junction. The spacing between each HV-NWELL ring in the new type is 12μm. The HVNW spacing spites from 12μm to 4μm.

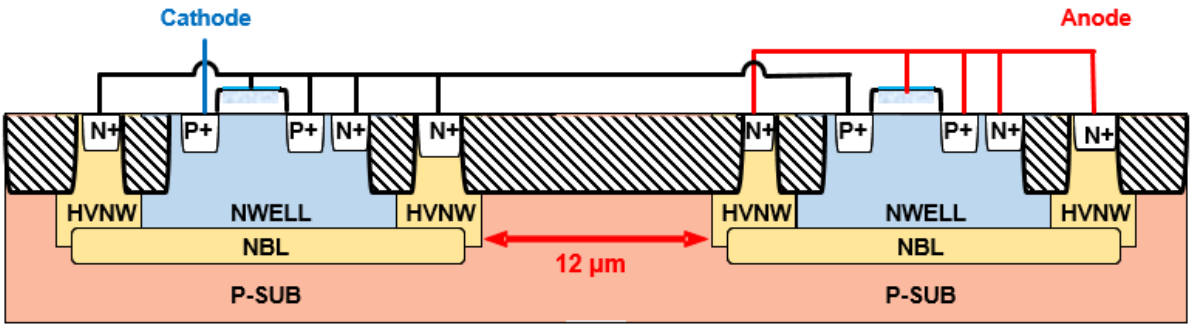


Fig. 4.1 The cross-sectional views of new type stacked structure with two LV PMOSs drawn

4.2.2 Guard Ring in Real Circuit Application

In chapter 3.3, the type C of guard ring layout can reduce layout area, and they also have good ESD robustness. In addition, the ESD devices should be surrounded by the P+ guard ring in real circuit application. The ESD device without the P+ guard ring can reduce the layout area, but it might cause the latchup issue under the normal circuit operation. The top view of new structure is shown in Fig. 4.2. The spacing between HV-NWELL ring and P+ guard ring in new type need to spite.

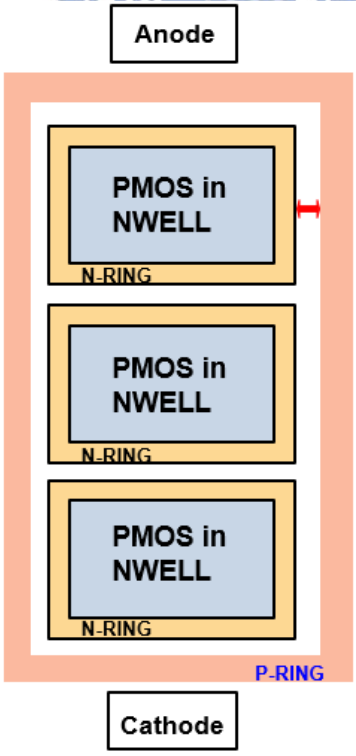


Fig. 4.2 The top view of new type stacked structure in real circuit application

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