國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

高介電係數 / 金屬閘極製程之
靜電放電防護設計與研究

ESD Protection Design in 28nm
High-K / Metal Gate Process

研 究 生：張品歆　　(Pin-Hsin Chang)
指導教授：柯明道教授 (Prof. Ming-Dou Ker)
共同指導教授：林群祐教授 (Prof. Chun-Yu Lin)

中華民國一〇三年十一月

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碩士論文

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摘要

隨著製程的演進，元件的尺寸不斷的縮小，金氧半場效電晶體的閘極(gate)氧化層厚度越來越薄，以達到積體電路操作速度快以及低功耗的目的，然而，外在環境的靜電並沒有減少，雖然在 50 奈米以下的製程已經引入了高介電係數的材質以提高等效的氧化層厚度(Effective Oxide Thickness, EOT)，然而元件對靜電的敏感度依舊很高，使得靜電放電(Electrostatic Discharge, ESD)防護成為先進製程中很重要的可靠度議題之一。

為了釋放高能量的靜電電流，在電晶體中寄生的雙極性電晶體(Bipolar Junction Transistor, BJT)扮演著重要的角色，在全晶片靜電放電防護架構中，於輸入/輸出(I/O)腳

位(pin)和 VDD 電源線間使用閘極接 VDD 之 P 型金氧半場效電晶體(gate-VDD PMOS, GDPMOS)，以及在輸入/輸出腳位和 VSS 電源線間使用閘極接地之 N 型金氧半場效電晶體(gate-grounded NMOS, GGNMOS)。在本論文中，為了達成靜電放電防護元件能承受更大的電流及高效率的使用面積之目的，在布局上使用多指狀(multi-finger)結構，而在 GGNMOS 中由於寄生的 BJT 之電流增益(beta gain)較大而導致驟回效應(snapback)明顯而造成先導通的指根上會先燒毀之不均勻導通現象，所以，增加通道寬度並沒有使 NMOS 的靜電耐受度呈線性上升，為了改善此情況，本論文中在每根指頭的源極(source)插入 pickup 使每根指狀結構的寄生 BJT 的基底(base)之電阻值相同，然而，由於相較於沒有加入 pickup 的寄生 BJT 之基底電阻較小以致不容易被導通(turn-on) ，因此，其靜電耐受度下降;另外，晶片驗證結果發現 GDPMOS 無論是加大通道寬度或者在源極插入 pickup，其靜電耐受度皆維持在很低的值，因此在第四章中提出一個新穎的結構提高以 PMOS 為基底的靜電放電防護元件之靜電耐受度。以上研究在 28 奈米的高介電係數/金屬閘極製程下實現。

在第四章中提出了一個PMOS鑲嵌在傳統的矽控整流器(Silicon-Controlled Rectifier, SCR)中之結構，其使用了 CMOS 標準製造過程中，為了降低觸發電壓(trigger voltage, Vt1)會加在 NMOS 之汲極(drain)加入 P 型的靜電放電佈植(P-ESD Implant)，所以不需要額外的光罩及花費，另外，相較於 GDPMOS 以及 GGNMOS，此結構擁有單位面積下靜電耐受度較高，其中靜電耐受度包括人體靜電放電模型(Human-Body Model, HBM)及元件充電模型(Charged-Device Model, CDM)、均勻導通、寄生電容較小之特性，以及可免於栓鎖效應(latch-up)的危險等優點，因此，此設計非常適合使用在製造成本越來越昂貴、閘極氧化層厚度越來越薄以及操作電壓越來越低的先進製程中作為靜電放電防護的元件。此設計成功在 28 奈米的高介電係數 /金屬閘極製程下實現。

ESD Protection Design in 28nm High-K / Metal Gate Process

Student: Pin-Hsin Chang **Advisor: Prof. Ming-Dou Ker**
Co-Advisor: Prof. Chun-Yu Lin

Department of Electronics Engineering &Institute of Electronics
National Chiao-Tung University

Abstract

With the on-going shrinking of CMOS technologies, the devices in the integrated circuits (ICs) have been fabricated with ultra-thin gate oxide thickness to attain high speed and low power consumption. However, electrostatic discharge (ESD) events were not scaled down with the scaling in CMOS technologies. Although the high-k dielectric has been introduced in sub-50-nm CMOS technologies, the MOS transistors are still sensitive to ESD. Therefore, ESD has become the major concern of reliability for ICs in nanoscale CMOS technology.

To discharge the high ESD energy without causing damage to integrated circuits, the turn-on behavior of parasitic bipolar junction transistors (BJTs) inherent in NMOS or PMOS transistors plays an important role. The NMOS and the PMOS with gate connected to source

have been used as the ESD clamp devices, that is to say, gate-grounded NMOS (GGNMOS) and gate-VDD PMOS (GDPMOS). In order to discharge more ESD current and use area efficiently, the transistors utilize the multi-finger structure. The GGNMOS has obvious snapback phenomenon due to large current gain of parasitic NPN BJT. The first turn-on finger will be burn out and results in nun-uniform turn-on issue. Thus, the ESD robustness is not increasing with enlarging the width of ESD devices. In this work, inserting inner pickups in source side of MOS transistors is to improve ESD level. Measurement results indicate that additional pickups decrease the ESD robustness of the NMOS transistors because the base resistor value becomes smaller. Then, the ESD robustness of PMOS transistors almost keeps the same value whether raising the width of channel or inserting inner pickups into source side. The above statement is discussed in Chapter 2. With a view to improve the ESD performance of PMOS-based ESD clamp devices. A novel ESD protection design is proposed in and is presented in chapter 3.

In chapter 3, a novel ESD protection design by using PMOS device with embedded silicon-controlled rectifier (SCR) is proposed in this work. This design employs the P-ESD implant which is put in the drain side of NMOS to lower the trigger voltage in a standard step of CMOS process. Hence, there is no need for extra mask/cost. Besides, the proposed device has the higher ESD robustness per area, more uniform turn-on behavior, and lower parasitic capacitance than GGNMOS and GDPMOS. Additionally, the proposed device has been tested to be free from latchup event. Accordingly, the proposed device can be a better solution for ESD protection in sub-50-nm CMOS process that cost becomes more expensive, the gate oxide thickness is getting to thinner, and the supply voltage is becoming lower. The above works in chapter 3 and chapter 4 have been designed, fabricated, and characterized in a 28-nm high-k/metal gate CMOS process.

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在碩士班的兩年之中，特別感謝柯明道老師和林群祐老師對我耐心指導鼓勵，柯明道老師在 ESD 方面深厚的專業知識、經驗及謹慎的研究態度讓我獲益良多，老師為研究群爭取許多福利和資源讓實在非常感恩，總是亦師亦友的林群祐老師非常有親切感，即使老師很忙或者身體不舒服，總是非常耐心的指導和提醒我研究上的事情，另外，老師總是能夠兼顧工作及家庭生活實在很佩服也很值得學習。

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張品歆

103 年 11 月於竹塹交大

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Chapter1

Introduction

1.1 Introduction to Whole-Chip ESD Protection Design

1.1.1 Whole-Chip ESD Protection Design Scheme

The ESD phenomenon occurs during the fabrication, transportation, package and assembly processes. The accumulated charges are bypassed from an object to its surrounding environment, generally regard as ground or earth, through ICs. ICs may malfunction or burn out. Hence, the ESD protection is needed for any two pins of the ICs to discharge high energy ESD current. Typical whole-chip ESD protection scheme [1] is demonstrated in Fig. 1.1. Fig. 1.2 shows that each I/O pin would have two ESD protection devices to construct two paths to power line and ground line, respectively. Besides, power-rail clamp would provide an ESD path from power line to ground line. In addition, the ESD protection devices or circuits are kept off when the IC is under its normal operating condition.

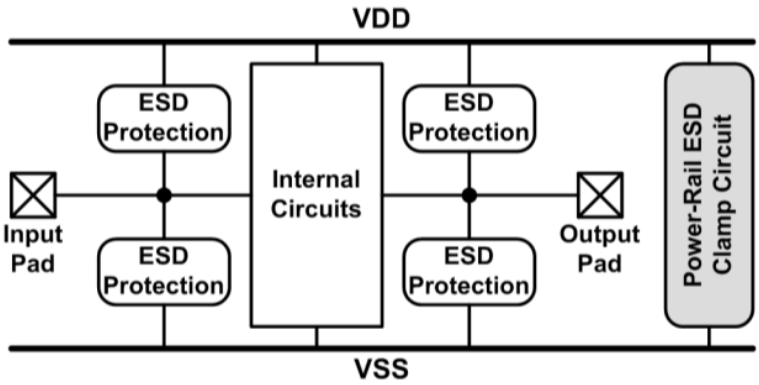


Fig.1.1. A typical whole-chip ESD protection scheme.

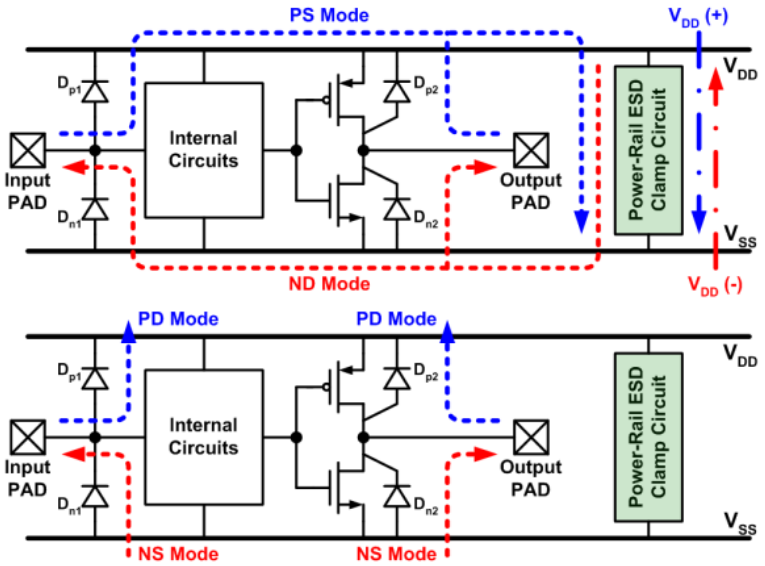
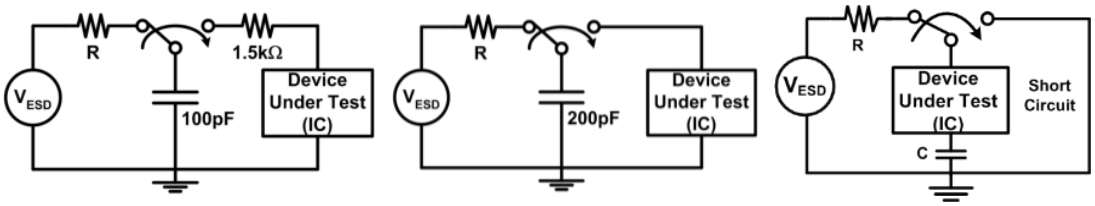


Fig.1.2. ESD tests on IO pins for HBM and MM.

1.1.2 Measurement Methods

ESD robustness can be tested in several ways. It is generally required 2kV in human body model (HBM), 200V in machine mode (MM), and 1kV in charged device model (CDM). Transmission line pulse (TLP) system and very fast TLP (VF-TLP) will help engineering to observe the characteristics of ESD protection devices.

Charges will be accumulated in human bodies, and machines. When one pin of ICs connects with the object with charges and another pin of ICs is connected to ground, the discharging paths are appeared. Depending on various objects with charges, different testing standards are developed. The equivalent models of HBM and MM are illustrated in Fig. 1.3 (a) and (b). Besides, Charges will be accumulated in ICs due to friction. When one pin of ICs touches ground, the accumulated charges are conducted to ground by the pin. The equivalent models of CDM are illustrated in Fig. 1.3 (c).



(a) (b) (c)

Fig.1.3. Equivalent circuits of (a) HBM, (b) MM, and (c) CDM.

In this thesis, there are four ESD methods be measured and the related information are listed below. First, the human-body-model (HBM) ESD robustness is tested according to the ESDA/JEDEC joint standard [2]. The failure criterion is defined as the I-V curve seen between test pads shifting over 30% from its original curve after ESD stressed at every ESD test level. Second, a transmission-line-pulsing (TLP) system with a 10ns rise time and a 100-ns pulse width is used to evaluate the trigger voltage (Vt1), holding voltage (Vhold), and secondary breakdown current (It2) of the test devices in the time domain of HBM ESD event. Third, the charge-device-model (CDM) ESD robustness is tested according to the ESDA/JEDEC joint standard [3]. The failure criterion is defined as the I-V curve seen between test pads shifting over 10% from its original curve after ESD stressed at every ESD test level. Last, Another very fast TLP (VF-TLP) system with 0.2-ns rise time and 1ns pulse width is also used to capture the transient behavior of the test devices in the time domain of charged-device-model (CDM) ESD event.

1.2 Motivation

As CMOS technologies keep scaling down, the integrated circuit (IC) realized in CMOS technology is susceptible to an electrostatic discharge (ESD) event which may damage the IC products [4], [5]. Therefore, on-chip ESD protection circuits must be equipped for the pads that may be stressed by ESD. Although the high-k dielectric has been introduced in

sub-50-nm CMOS technologies, the MOS transistors are still sensitive to ESD [6], [7]. Moreover, because the average cost of a die in sub-50-nm technologies is expensive, it is important to optimize ESD protection circuit to have a high ESD robustness within limited layout area. To achieve effective ESD protection, the voltage across the ESD protection circuit during ESD stresses should be carefully designed. Fig. 1 shows the ESD design window of an IC, which is defined by the power-supply voltage (VDD) of the IC, the failure level of ESD protection circuit, and the gate-oxide breakdown voltage (VBD) of MOSFET. First, the trigger voltage (Vt1) and holding voltage (Vh) of ESD protection circuit must be lower than the gate-oxide breakdown voltage of MOSFET to prevent the internal circuits from damage before the ESD protection circuit is turned on during ESD stresses. Second, the trigger voltage and holding voltage of the ESD protection circuit must be higher than the power-supply voltage of the IC to prevent the ESD protection circuits from being mistriggered under normal circuit operating conditions. Moreover, the turn-on resistance (Ron) of ESD protection circuit should be minimized to reduce the joule heat generated in the ESD protection circuit and the clamping voltage of the ESD protection circuit during ESD stresses. As CMOS technology is continuously scaled down, the power-supply voltage is decreased and the gate oxide becomes thinner, which leads to reduced gate-oxide breakdown voltage of MOSFET. Typically, the gate-oxide breakdown voltage is decreased to only ~5 V in sub-50-nm CMOS technologies [7]. As a result, the ESD design window becomes much narrower in nanoscale CMOS technologies. Furthermore, ESD protection circuits need to be quickly turned on during ESD stresses in order to provide efficient discharging paths in time.

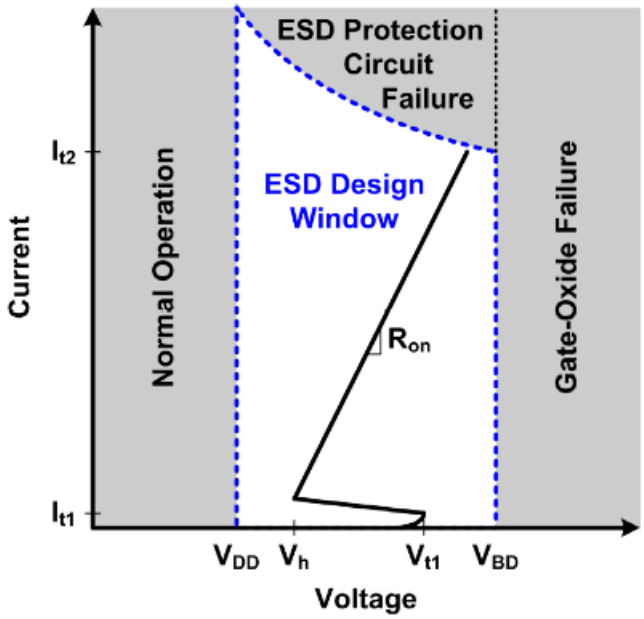


Fig.1.4. ESD design window.

1.3 Thesis Organization

In this thesis, there are four chapters. Whole-chip ESD protection design, research measurement methods, and motivation are introduced in chapter 1 . Chapter 2 investigates the phenomenon of pickup structure on ESD robustness of multi-finger MOS transistors. The MOS transistors contain GGNMOS and GDPMOS. This part has been fabricated in a 28-nm high-K/metal gate CMOS process Chapter 3 brings out a novel ESD protection design that is PMOS device with embedded SCR to improve ESD robustness. Besides, the proposed device possesses three types. The design has been fabricated in a 28-nm high-K/metal gate CMOS process and in a 0.18-μm CMOS process. In the last chapter, conclusions and future work are discussed.

Chapter2

Investigation on Multi-finger ESD Protection MOS Transistors with Inner Pickups

2.1 Introduction

2.1.1 Turn-On Mechanism of MOS Transistors under ESD Event

The inherent lateral bipolar transistor junction (BJT)s in MOS transistors are triggered on to discharge high ESD current under ESD event. Both avalanche breakdown and turn-on of the parasitic lateral BJT are included in the turn-on mechanisms. In order to present the turn-on mechanism of MOS transistors under ESD zap, the MOS transistors with gate, source, and substrate at zero potential is considered and the I-V curve is shown in Fig. 2.1

For GGNMOS, the inherent parasitic BJT path is N+ drain junction, P-Well and the N+ source junction that is illustrated in Fig. 2.2 (a). Under ESD condition, the parasitic NPN BJT is turned on to clamp the low clamping voltage to protect gate oxide of internal circuits. The current in the reverse bias at the drain-substrate (N+/P-Well) junction is rising with the increasing ESD current. Plenty of electron-hole pairs are produced due to the avalanche breakdown effect at the base-drain reverse bias junction. The electrons drift towards to the high potential of drain contact, and the holes are swept to the low potential of the substrate contact contributes to a substrate current, Isub. Isub is continuous increasing to forward the base-emitter (P-Well/N+) junction. Then, the parasitic NPN BJT can be regarded as turn-on.

For GDPMOS, the inherent parasitic BJT path is P+ source junction, N-Well and the P+ drain junction that is depicted in Fig. 2.2 (b) When ESD event occurs, the parasitic PNP BJT is turned on to clamp the low clamping voltage to protect gate oxide of internal circuits. The current in the reverse bias at the drain-substrate (P+/N-Well) junction is climbing with the

elevating ESD current. Lots of electron-hole pairs are generated due to the avalanche breakdown effect at the base-drain reverse bias junction. The electrons drift towards are swept to the high potential of substrate contact, and the holes are swept to the low potential of the drain contact contributes to a substrate current, Isub. Isub is continuous ascending to forward the base-emitter (N-Well/P+) junction. Then, the parasitic PNP BJT can be viewed as turn-on.

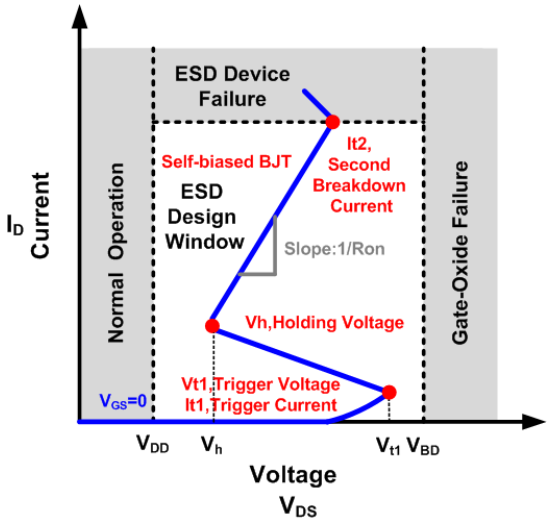
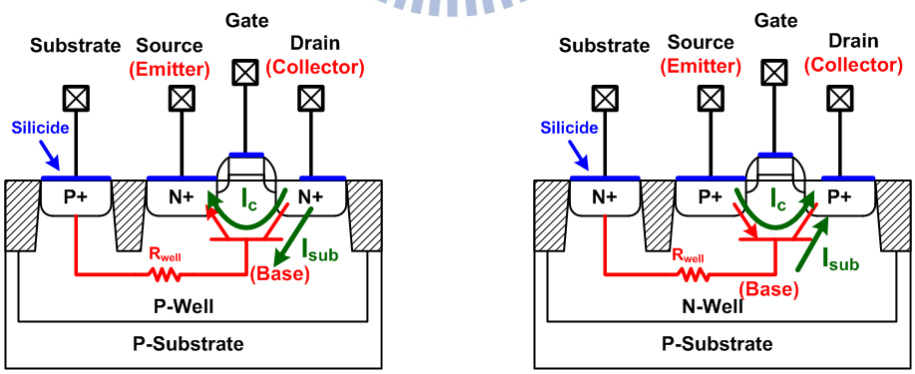


Fig.2.1. I-V curve of MOS transistor with VGS=0.



(a) (b)

Fig.2.2. Cross-section view of (a) NMOS and (b) PMOS.

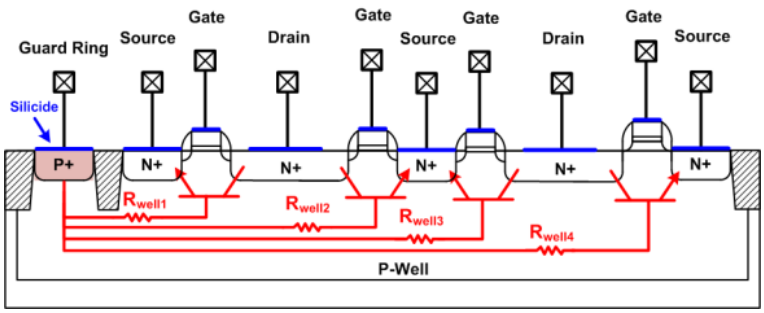
In Fig. 2.2(b), Vt1 and It1are the trigger voltage and current of the parasitic BJT. Once the parasitic lateral BJT can be turned on when the avalanche breakdown happens and the drain current is sufficient to elevate the voltage potential of base to forward the base-emitter

junction, the voltage of device can be clamped to low called holding voltage (Vhold). Now, a negative resistance is perceived. Then, the I-V curve exhibits a positive resistance and can sustain high ESD current. The Isub is supposed to retain to make the parasitic BJT is turn-on. Eventually, the parasitic BJT will be durable failed owing to thermal failure, and the failure current level called second breakdown current (It2).

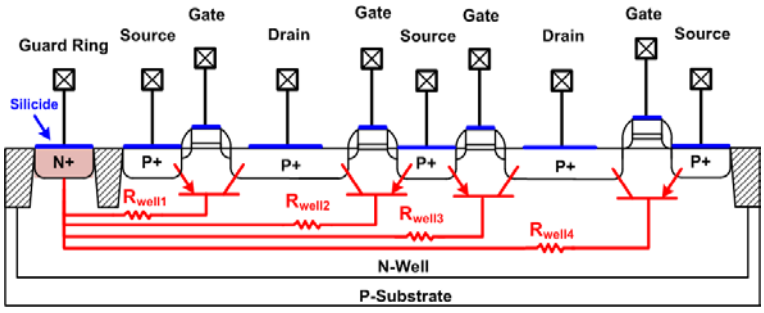
2.1.2 Non-Uniform Turn-On Issue in MOS Transistors

NMOS transistor has non-uniform turn-on issue. There are two major reasons. The first one is obvious snapback characteristic. The second one is asymmetrical layout structure in multi-finger that is illustrated in Fig. 2.3 (a). Thanks to large current gain of parasitic NPN BJT, the snapback characteristic is evident. This demonstrates that the holding voltage can be clamped low voltage in singer-finger. However, the distance of parasitic from base to substrate guard ring is different. The largest parasitic base resistance can be turned on firstly in the center of multi-finger. Then, the voltage of the finger is clamped at low voltage that make other finger can't be turned on until the first turn-on finger is burned out.

PMOS transistor has no non-uniform turn-on issue. The snapback trait is weak since the current gain of parasitic PNP BJT is small. Thus, the trigger voltage and holding voltage is almost the same. The layout structure of GDPMOS in multi-finger is shown in Fig. 2.3 (b).



(a)



(b)

Fig.2.3. (a) Cross-section view of multi-finger NMOS and (b) PMOS.

2.2 Motivation

To discharge the high ESD energy without causing damage to internal circuits, the typical whole-chip ESD protection scheme is shown in Fig. 2.4, where a gate grounded NMOS (GGNMOS) and a gate-VDD PMOS (GDPMOS) is used. The turn on of parasitic bipolar junction transistor (BJT) inherent in GGNMOS and GDPMOS plays an important role [8]- [10].

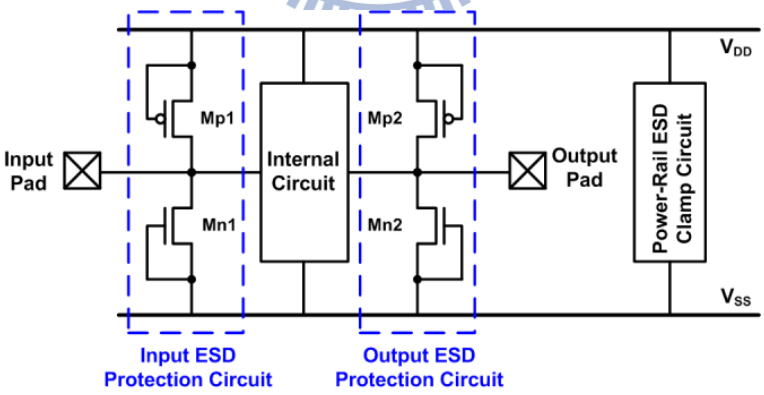


Fig.2.4. Whole-chip ESD protection scheme.

When the GGNMOS and GDPMOS is under ESD stress, the parasitic NPN BJT and PNP BJT will be triggered to discharge ESD current. To sustain the required ESD level, such a GGNMOS and GDPMOS is often designed with large dimension, which is often drawn

with the multi-finger style to reduce the total occupied layout area.

However, it has been reported that multi-finger GGNMOS in some CMOS processes can not be uniformly turned on under ESD stress[11]. That is, even if a larger multi-finger GGNMOS is used as the ESD protection circuit, uniform conduction of all fingers is hard to achieve, and hence the expected ESD level can not be realized. To solve this problem, adding additional pickups into the layout may be a solution. It has been reported that the effect of additional layout pickups to the ESD robustness of GGNMOS in submicron CMOS technologies [12].

Besides, it has been shown that GDPMOS are often used to discharge the ESD current path from I/O pin to VDD pin which is ND mode. In this mode, the ESD current goes through the parasitic diode (P+/N-Well). In the PD mode, the ESD current goes through the parasitic PNP BJT and the ESD level is very low. To conquer challenge, adding additional pickups into the layout may be a method. It has been reported that the effect of additional layout pickups to the ESD robustness of GDPMOS in submicron CMOS technologies. It has been reported that the effect of additional layout pickups to the ESD robustness of GGNMOS in submicron CMOS technologies [13].

In this work, the effect of additional layout pickups to the ESD robustness of GGNMOS and GDPMOS is implemented in a 28-nm high-k/metal gate CMOS process.

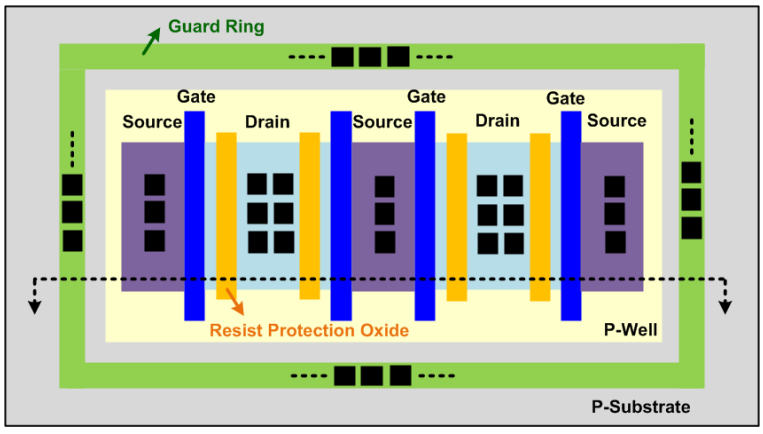
2.3 Multi-Finger GGNMOS with Inner Pickups

2.3.1 Device Structure and Chip Photo

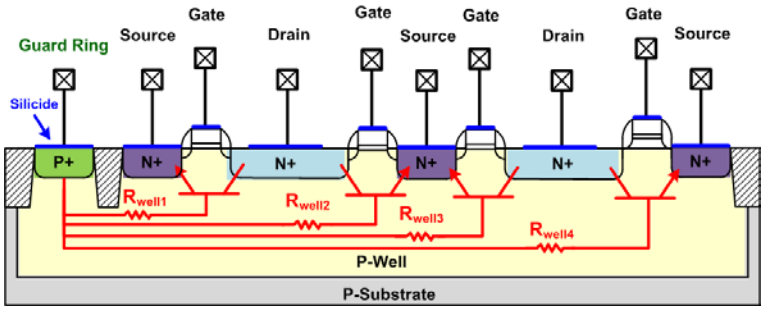
The layout top view and the device cross-sectional view of an ESD protection multi-finger GGNMOS is shown in Fig. 2.5. In the multi-finger GGGMOS structure with P+ guard ring surrounding it, due to the different distances from the base regions of each parasitic NPN BJT to the P+ guard ring, the base resistance of NPN BJT in the central region of the

multi-finger GGNMOS is higher than those in the side regions (Rwell4 > Rwell3 > Rwell2 > Rwell1). Therefore, in the multi-finger GGNMOS structure, the fingers in center are always triggered on faster than the others under ESD stress. As long as the center fingers are triggered on, the ESD stress voltage is clamped to the snapback holding voltage of GGNMOS. The other non-turned-on fingers in the side regions may not be triggered on before the first turned-on fingers are burned out.

Fig. 2.6 shows the layout top view and the device cross-sectional view of an ESD protection multi-finger GGNMOS with an additional P+ pickup at source side. The additional P+ pickup in GGNMOS is connected to the P+ guard ring. With the additional P+ pickup inserted into the GGNMOS, the base resistance (Rwell) of each parasitic NPN BJT can be effectively balanced. From the view point of layout symmetry of parasitic BJT, inserting additional P+ pickups in source side of GGNMOS can improve turn-on uniformity during ESD stresses. However, it is known that the lower Rwell value of parasitic lateral BJT leads to the higher trigger current (It1) of GGNMOS. As a result, GGNMOS may be hard to turn on. To clarify this issue, the effect of additional layout pickups to ESD robustness of multi-finger GGNMOS in a 28-nm high-k/metal gate CMOS process is studied.

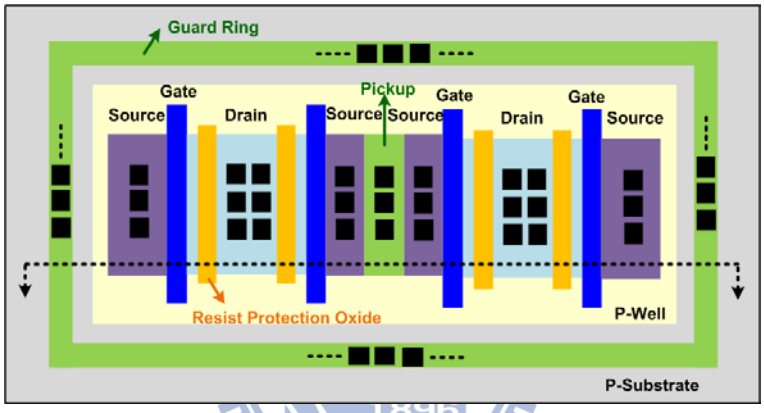


(a)

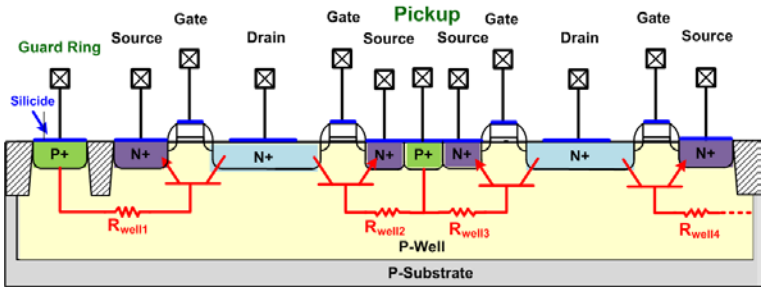


(b)

Fig.2.5. (a) Layout top view and (b) device cross-sectional view of multi-finger GGNMOS without additional pickup.



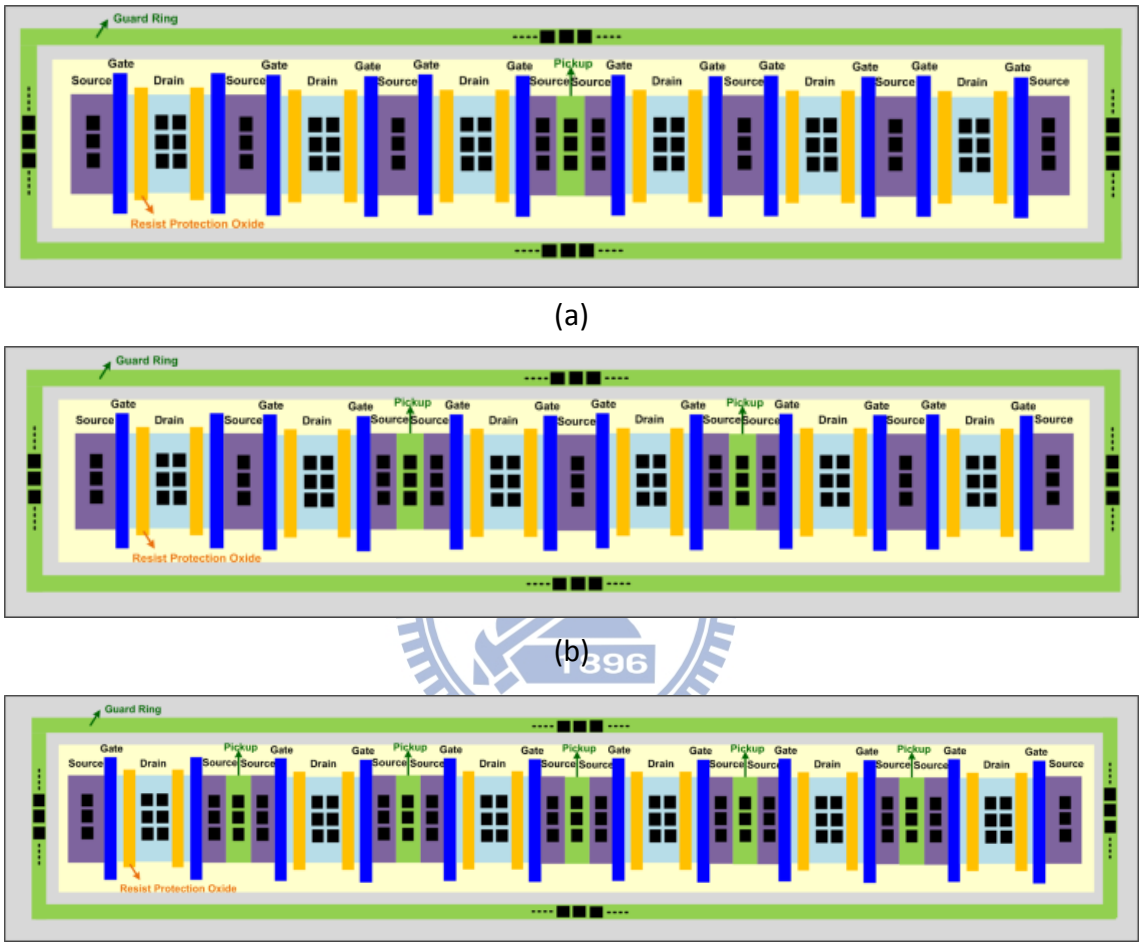
(a)



(b)

Fig.2.6. (a) Layout top view and (b) device cross-sectional view of multi-finger GGNMOS without additional pickup.

The multi-finger GGNMOS with different numbers of P+ pickups are studied. The layout top views of GGNMOS with 1, 2, and 5 P+ pickups are shown in Figs. 2.7 (a), (b), and (c), respectively. All the test GGNMOS have the same effective device dimension of 240 μ m and the same layout style, except for the P+ pickups.



(a)

(b)

(c)

Fig.2.7. Layout top view of multi-finger GGNMOS with different number of pickups: (a) pickup=1, (b) pickup=2, and (c) pickup=5.

The test circuits about GGNMOS have been fabricated that are shown in Fig. 2.8 in a multi-project wafer (MPW).

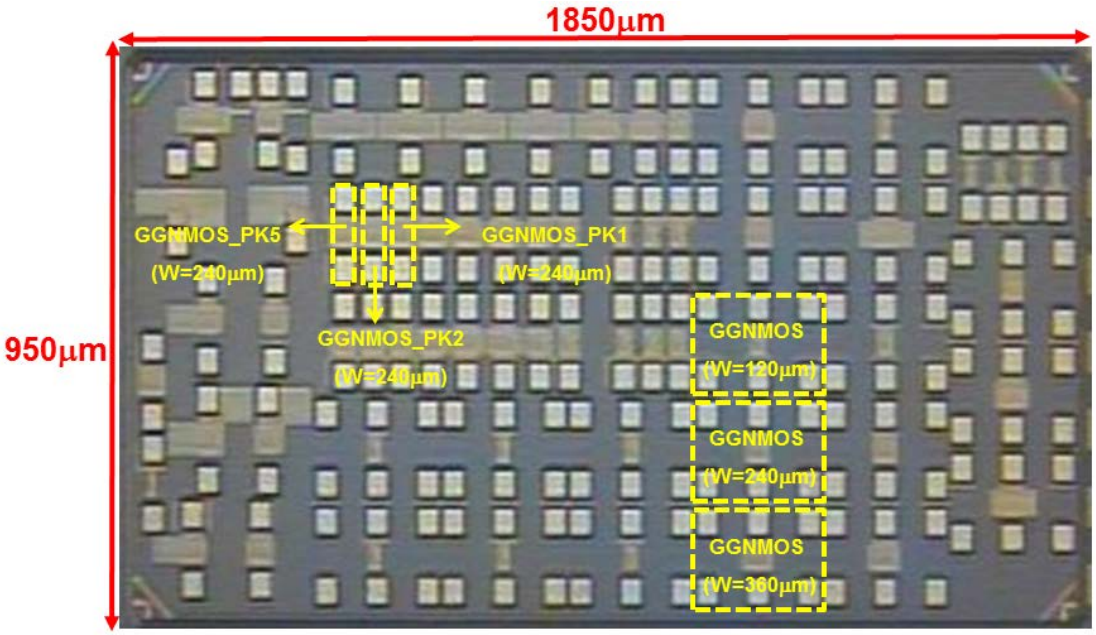


Fig.2.8. Chip photograph of test circuits about GGNMOS.

2.3.2 Measurement Results

To investigate the turn-on behavior and the I-V curve in high current region of the ESD protection circuit, the TLP is used. The TLP-measured I-V characteristics of the GGNMOS are shown in Fig. 2.9 and 2.10. The trigger voltage (Vt1), the trigger current (It1), the holding voltage (Vh), the secondary breakdown current (It2), and HBM level of the GGNMOS with different number of P+ pickups are compared in Figs. 11~13.

Another very fast TLP VF-TLP is used to evaluate the ESD protection circuit in faster ESD-transient events. The VF-TLP-measured I-V characteristics of the GGNMOS are shown in Fig. 2.14 and 2.15. The trigger voltage (Vt1), the trigger current (It1), the holding voltage (Vh), the secondary breakdown current (It2), and CDM level of the GGNMOS with different number of P+ pickups are compared in Figs. 16~18.

It can be found that the It2 is ascending while the effective channel is increasing of the GGNMOS with multi-finger structure. Besides, the GGNMOS with more pickups have the

poor performances (higher Vt1, higher It1, higher Vh, higher Ron, and lower It2) under TLP tests, and the HBM level is drop.

Under VF-TLP tests, the It2 is ascending while the effective channel is increasing of the GGNMOS with multi-finger structure. Besides, the GGNMOS with more pickups do not degrade their Ron and It2, while other performances degraded (higher Vt1, higher It1, and higher Vh), and the CDM level is maintained.

From the point view of heat dissipation, the shorter time means the shorter pulse width that produce less heat. Thus, the It2 under VF-TLP tests in comparison to that under TLP tests is higher in the same test device.

From these experimental results, it is clear that inserting additional layout pickups into the multi-finger GGNMOS can not improve the ESD robustness in 28-nm high-k/ metal gate CMOS process.

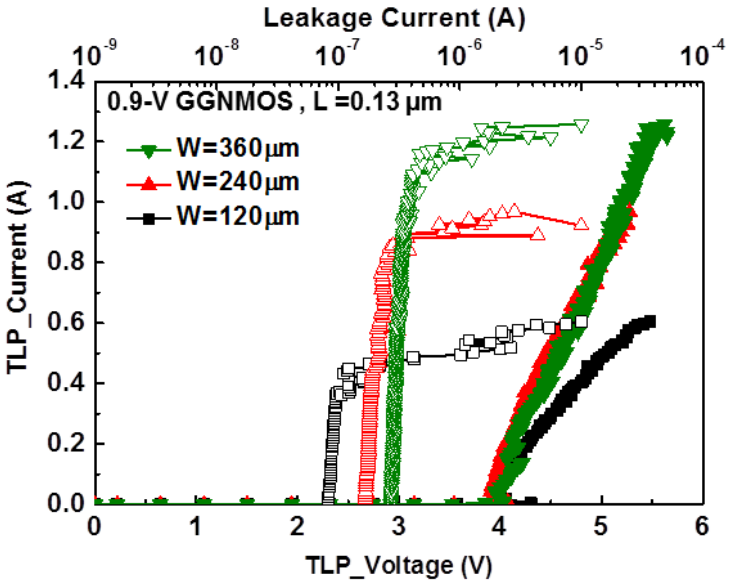


Fig.2.9. Measured TLP I-V curves of GGNMOS with different multi-finger width.

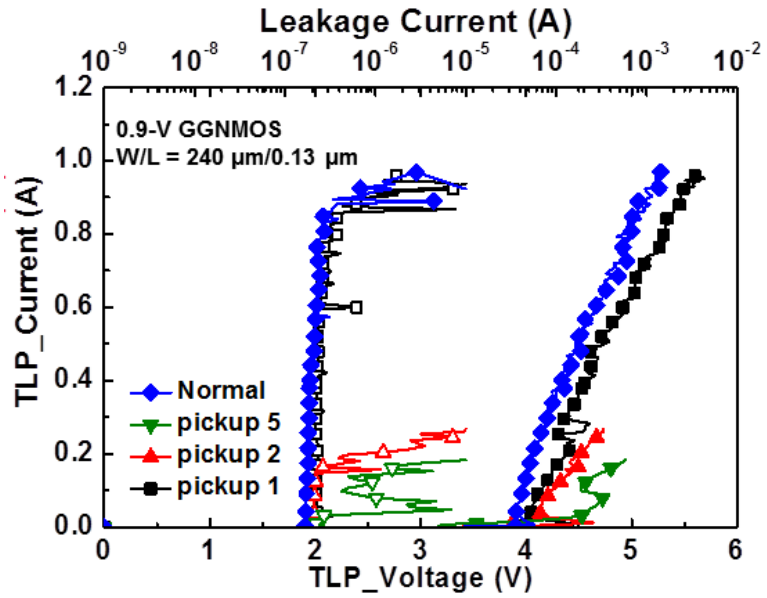


Fig.2.10. Measured TLP I-V curves of GGNMOS with different pickup numbers.

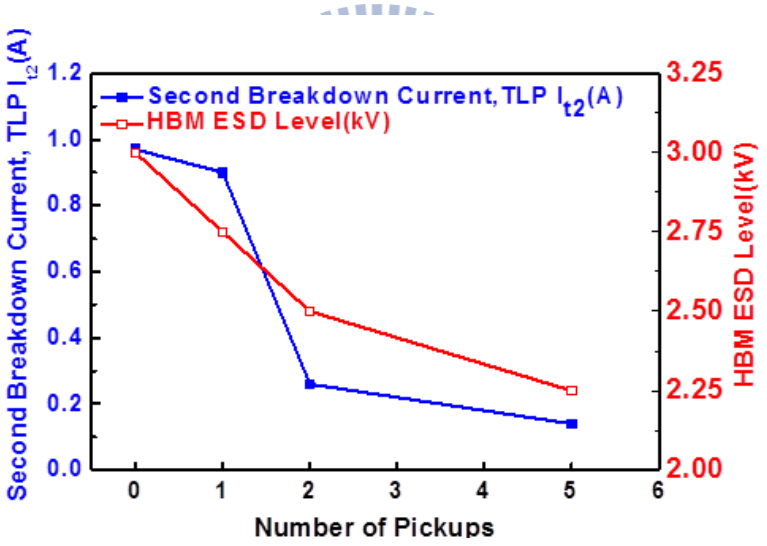


Fig.2.11. Measured the dependence of It2(TLP) and HBM level on different pickup numbers of GGNMOS.

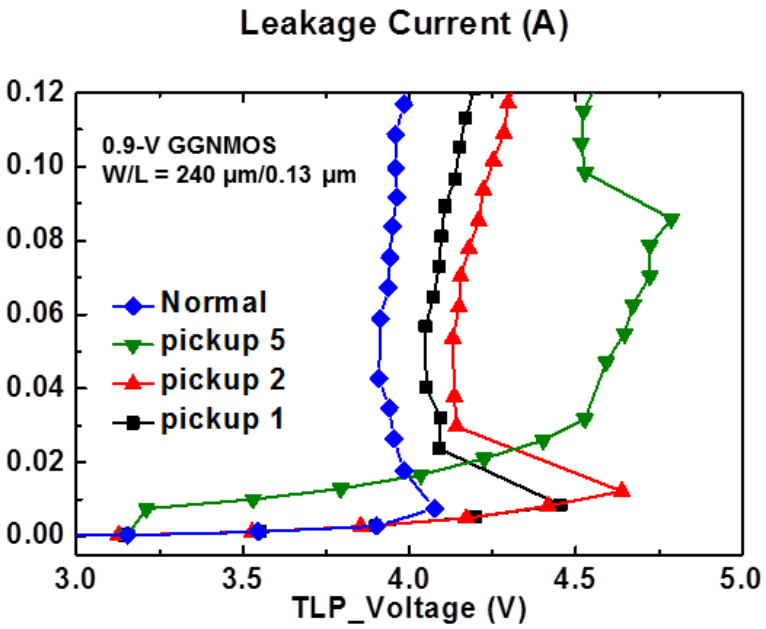


Fig.2.12. The zoom-in of TLP I-V curves of GGNMOS with different pickup numbers.

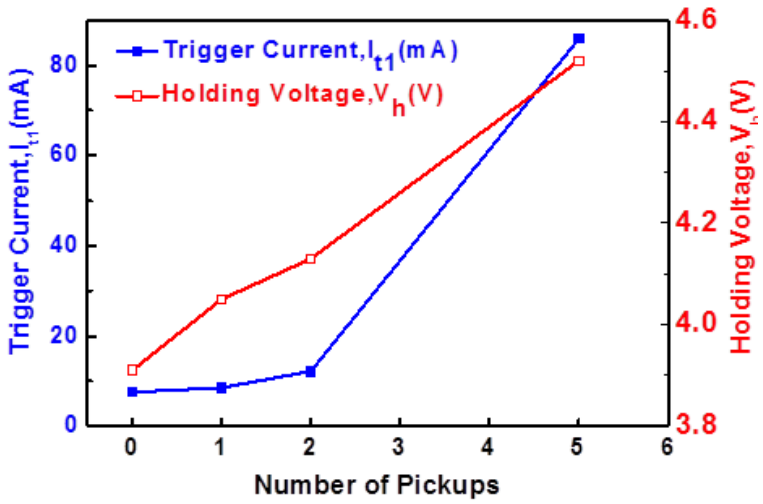


Fig.2.13. Measured the dependence of It1(TLP) and Vh on different pickup numbers of GGNMOS.

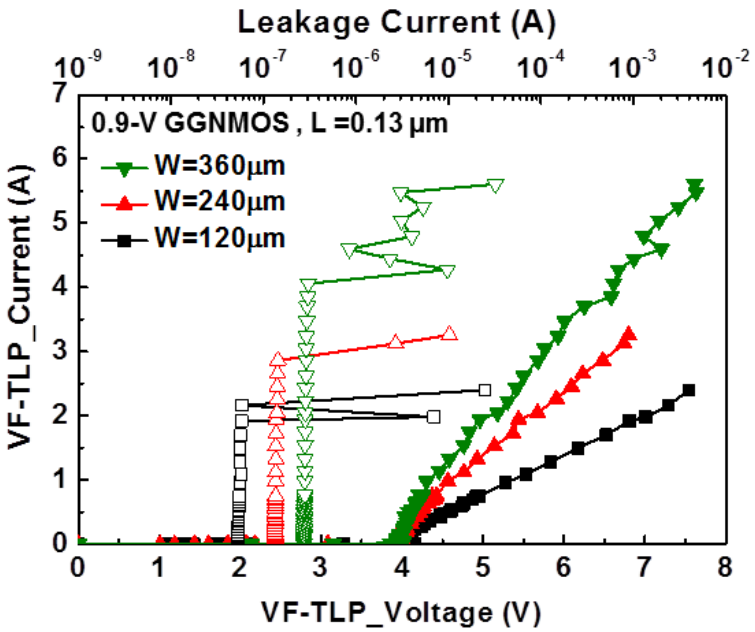


Fig.2.14. Measured VF-TLP I-V curves of GGNMOS with different multi-finger width.

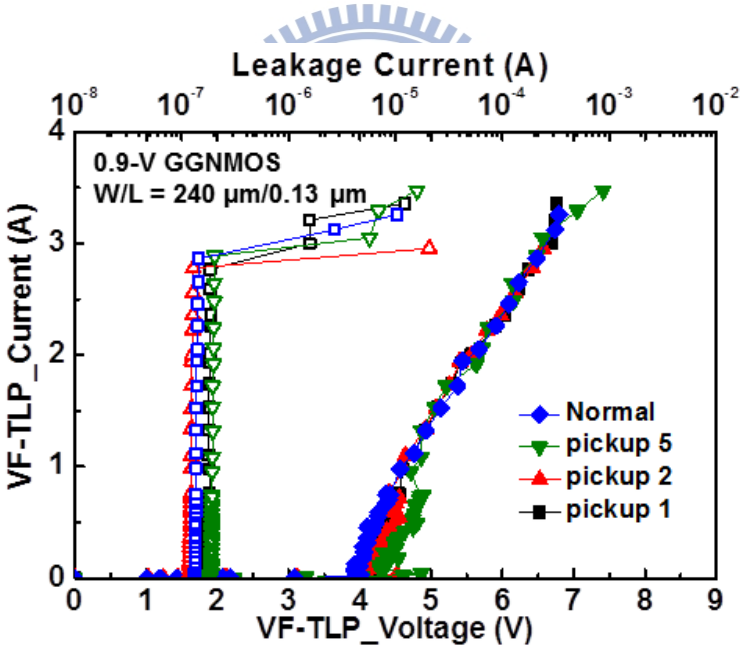


Fig.2.15. Measured VF-TLP I-V curves of GGNMOS with different pickup numbers.

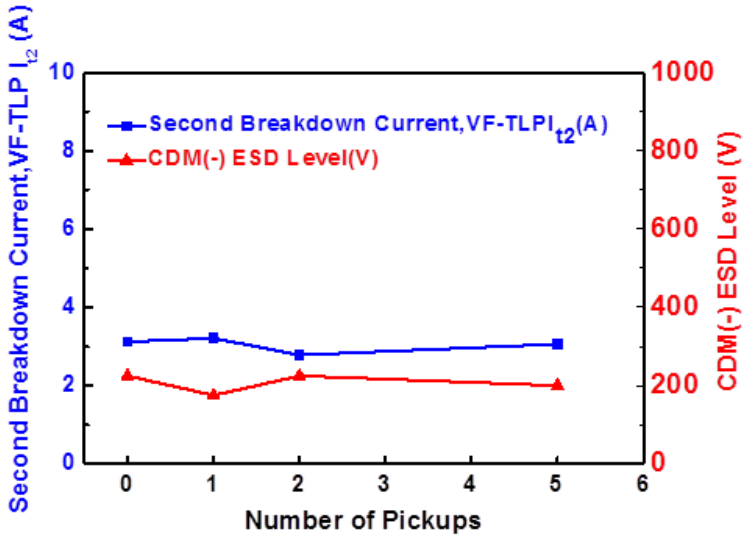


Fig.2.16. Measured the dependence of It2(VF-TLP) and CDM level on different pickup numbers of GGNMOS.

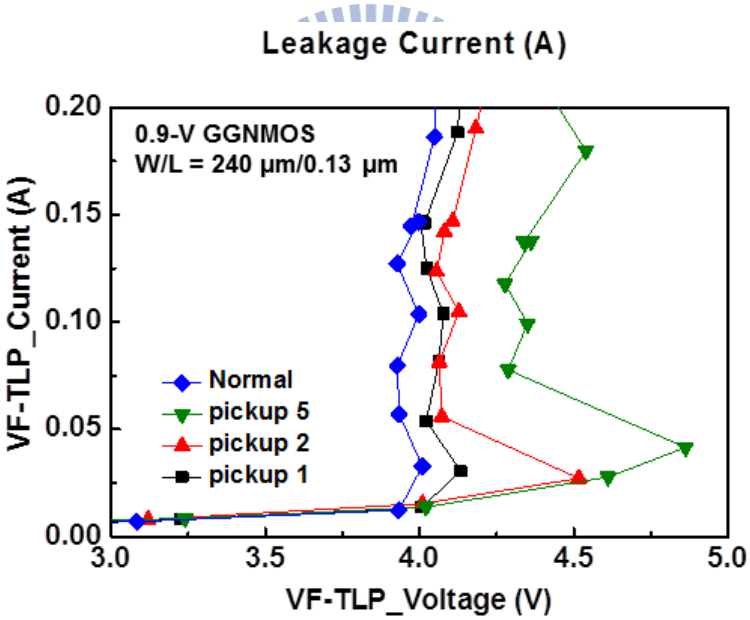


Fig.2.17. The zoom-in of VF-TLP I-V curves of GGNMOS with different pickup numbers.

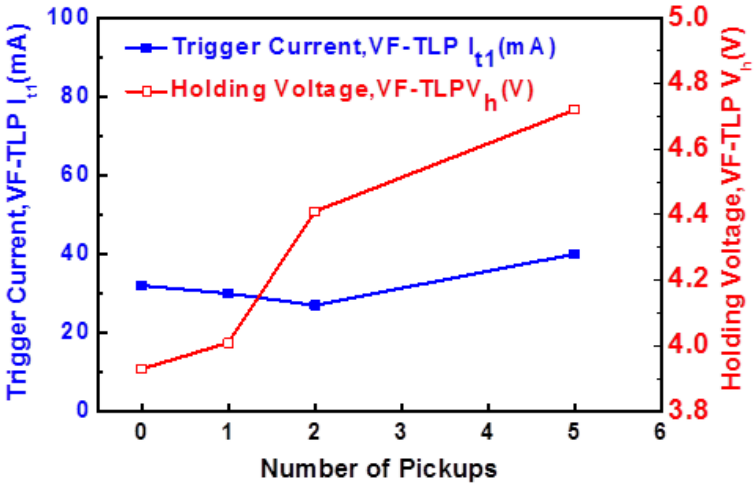


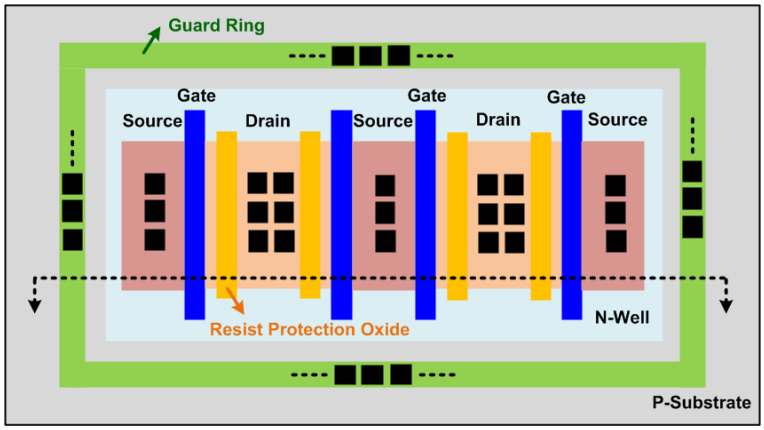
Fig.2.18. Measured the dependence of It1(VF-TLP)and Vh on different pickup numbers of GGNMOS.

2.4 Multi-Finger GDPMOS with Inner Pickups

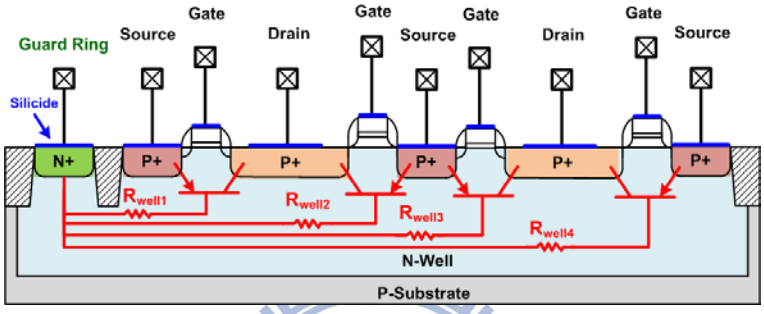
2.4.1 Device Structure and Chip Photo

The layout top view and the device cross-sectional view of an ESD protection multi-finger GDPMOS is shown in Fig. 2.19. In the multi-finger GDPMOS structure with N+ guard ring surrounding it, due to the different distances from the base regions of each parasitic PNP BJT to the N+ guard ring, the base resistance of PNP BJT in the central region of the multi-finger GDPMOS is higher than those in the side regions (Rwell4 > Rwell3 > Rwell2 > Rwell1). Therefore, in the multi-finger GDPMOS structure, the center fingers are always triggered on faster than the others under ESD stress. As long as the center fingers are triggered on, the ESD overstress voltage is not clamped to the snapback holding voltage of GDPMOS because the holding voltage and the trigger voltage is almost the same. Hence, GDPMOS has no non-uniform turn-in issue.

Fig. 2.20 shows the layout top view and the device cross-sectional view of an ESD protection multi-finger GDPMOS with an additional N+ pickup at source side. The additional N+ pickup in GDPMOS is connected to the N+ guard ring. With the additional N+ pickup inserted into the GDPMOS, the base resistance (Rwell) of each parasitic PNP BJT can be effectively balanced. From the view point of layout symmetry of parasitic BJT, inserting additional N+ pickups in source side of GDPMOS can improve turn-on uniformity during ESD stresses. However, it is known that the holding voltage and the trigger voltage is almost the same. As a result, GDPMOS may not be influence by adding inner pickups. To clarify this issue, the effect of additional layout pickups to ESD robustness of multi-finger GDPMOS in a 28-nm high-k/metal gate CMOS process is studied.

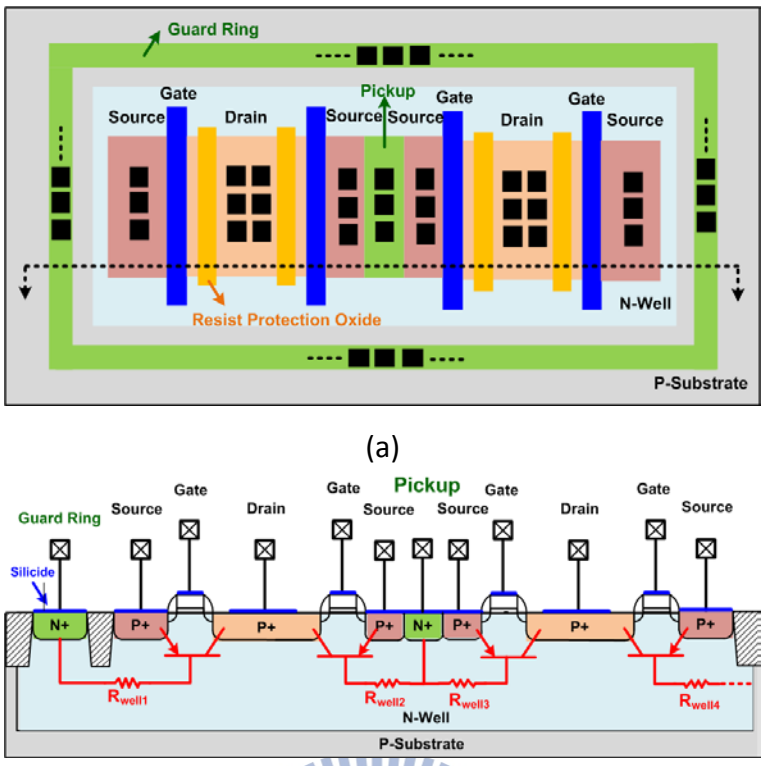


(a)



(b)

Fig.2.19. (a) Layout top view and (b) device cross-sectional view of multi-finger GDPMOS without additional pickup.



(a)

(b)

Fig.2.20. (a) Layout top view and (b) device cross-sectional view of multi-finger GDPMOS without additional pickup.

The multi-finger GDPMOS with different numbers of N+ pickups are studied. The layout top views of GDPMOS with 1, 2, and 5 N+ pickups are shown in Figs. 2.21 (a), (b), and (c), respectively. All the test GDPMOS have the same effective device dimension of 240 μm and the same layout style, except for the N+ pickups.

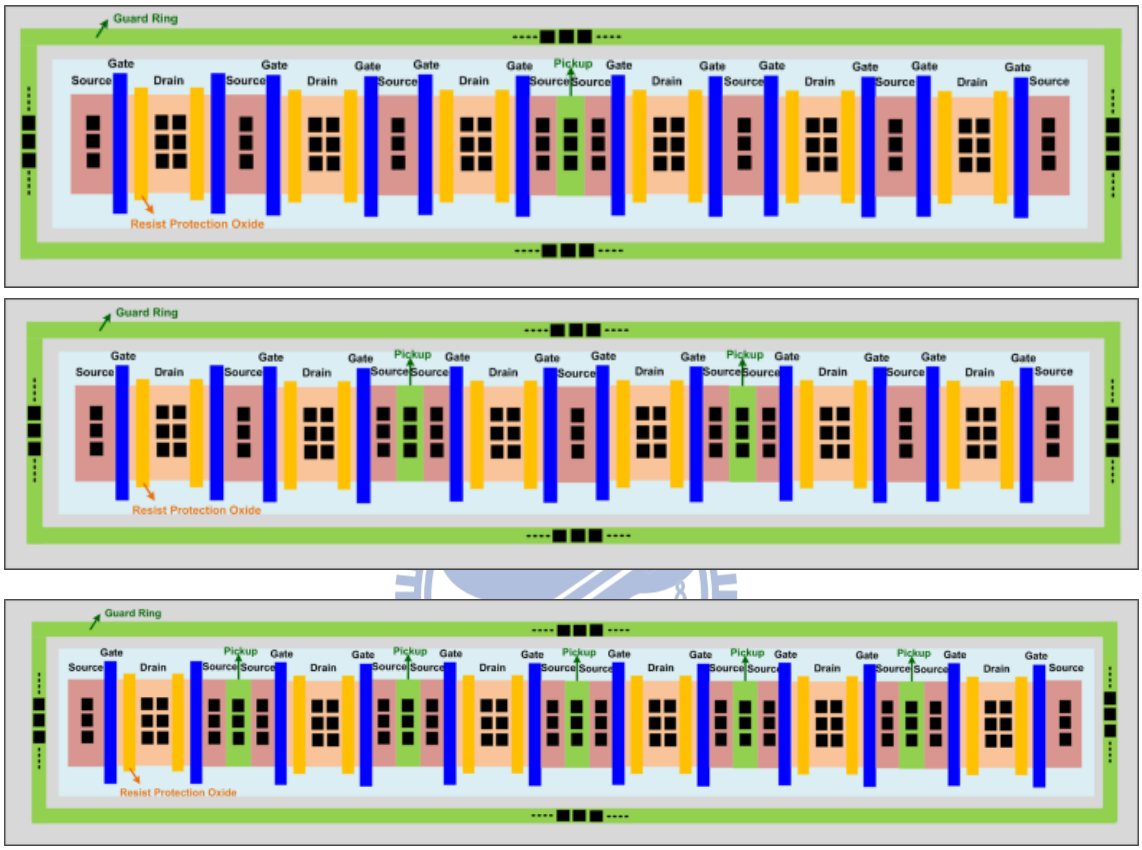


Fig.2.21. Layout top view of multi-finger GGNMOS with different number of pickups: (a) pickup=1, (b) pickup=2, and (c) pickup=5.

The test circuits about GDPMOS have been fabricated that are shown in Fig. 2.22 in a multi-project wafer (MPW).

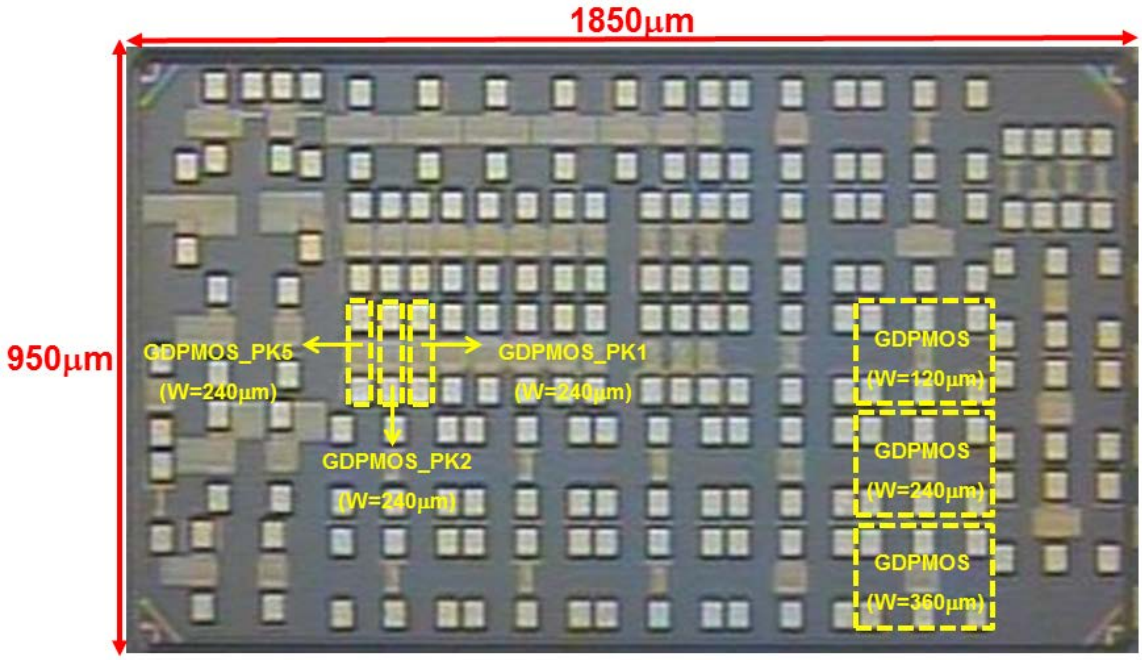


Fig.2.22. Chip photograph of test circuits about GDPMOS.

2.4.2 Measurement Results

In order to inspect the turn-on behavior and the I-V curve in high current region of the ESD protection circuit, the TLP is used. The TLP-measured I-V characteristics of the GDPMOS are shown in Fig. 2.23 and 2.24. The trigger voltage (Vt1), the secondary breakdown current (It2), and HBM level of the GDPMOS with different number of N+ pickups are compared in Figs. 25~27.

Another very fast TLP VF-TLP is used to estimate the ESD protection circuit in faster ESD-transient events. The VF-TLP-measured I-V characteristics of the GDPMOS are illustrated in Fig. 2.28 and 2.29. The trigger voltage (Vt1), the trigger current (It1), the holding voltage (Vh), the secondary breakdown current (It2), and CDM level of the GDPMOS S with different number of N+ pickups are compared in Figs. 30~32.

It can be found that the It2 is keeping while the effective channel is increasing of the GDPMOS with multi-finger structure. Besides, the GDPMOS with more pickups have the poor performances (higher Vt1, and lower It2) under TLP tests, and the HBM level is falling.

Under VF-TLP tests, the It2 is rising while the effective channel is increasing of the GDPMOS with multi-finger structure. Besides, the GDPMOS with more pickups slightly upgrade their It2, while other performances is decline (higher Vt1, higher It1, and higher Vh), and the CDM level is scarcely rising.

From the point view of heat, the shorter time means the shorter pulse width that produce less heat. Thus, the It2 under VF-TLP tests in comparison to that under TLP tests is higher in the same test device.

From these experimental results, it is obvious that inserting additional layout pickups into the multi-finger GDPMOS S can not improve the ESD robustness in 28-nm highk/ metal gate CMOS process.

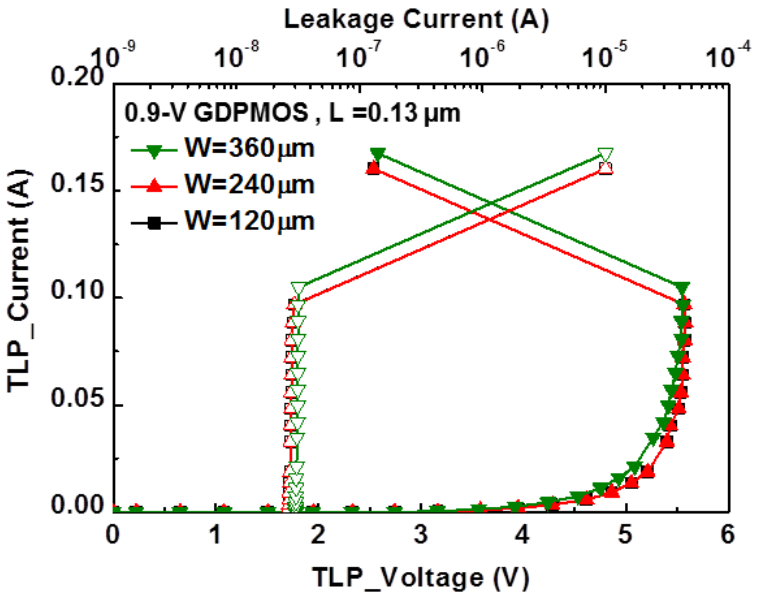


Fig.2.23. Measured TLP I-V curves of GDPMOS with different multi-finger width.

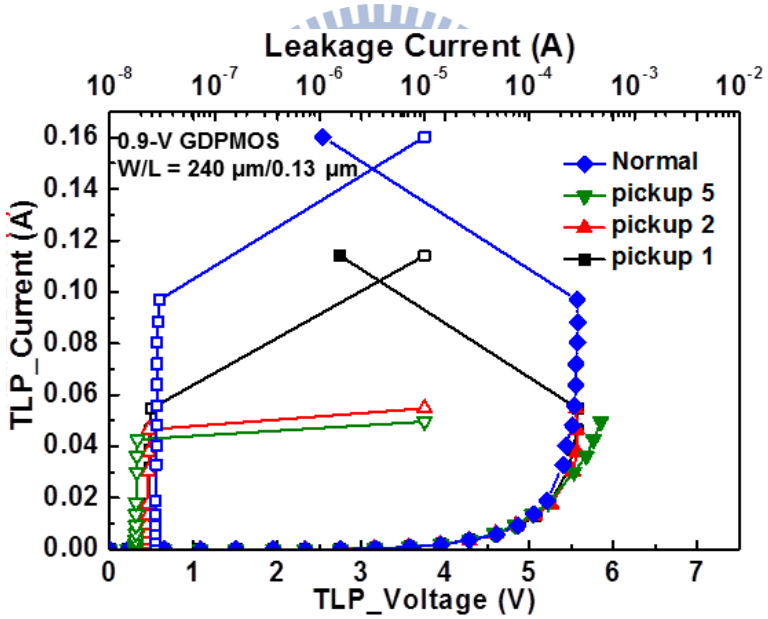


Fig.2.24. Measured TLP I-V curves of GDPMOS with different pickup number.

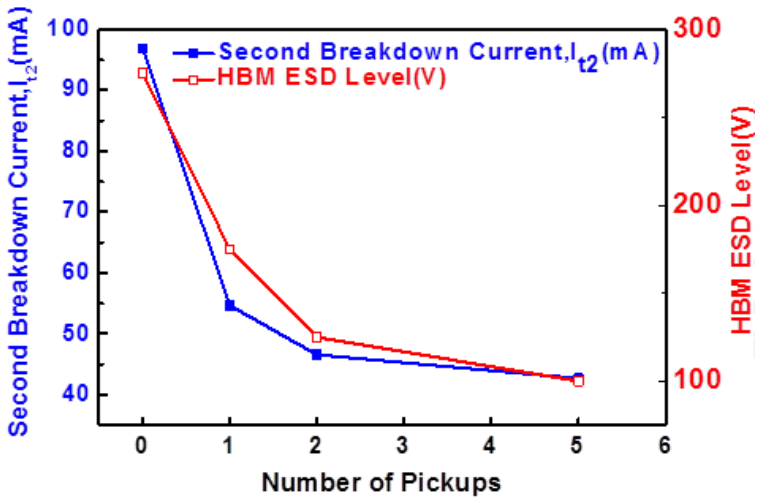


Fig.2.25. Measured the dependence of It2(TLP) and HBM level on different pickup numbers of GDPMOS.

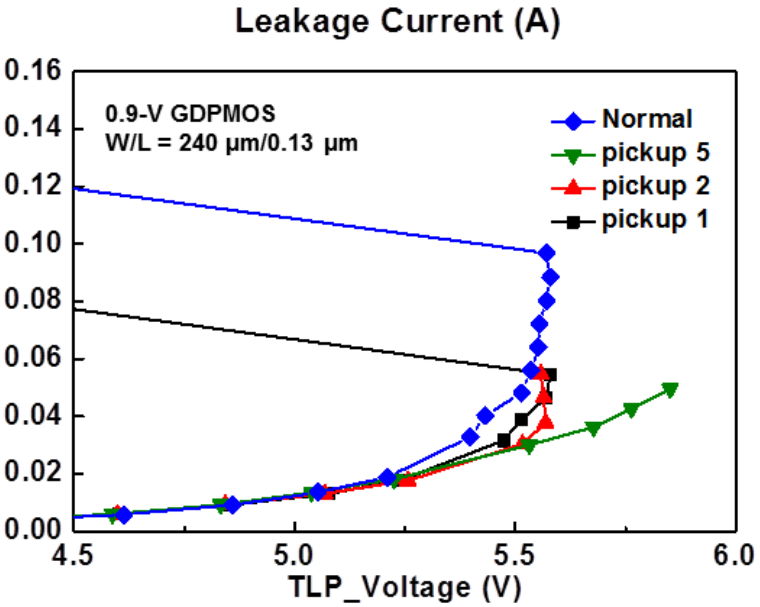


Fig.2.26. The zoom-in of TLP I-V curves of GDPMOS with different pickup numbers.

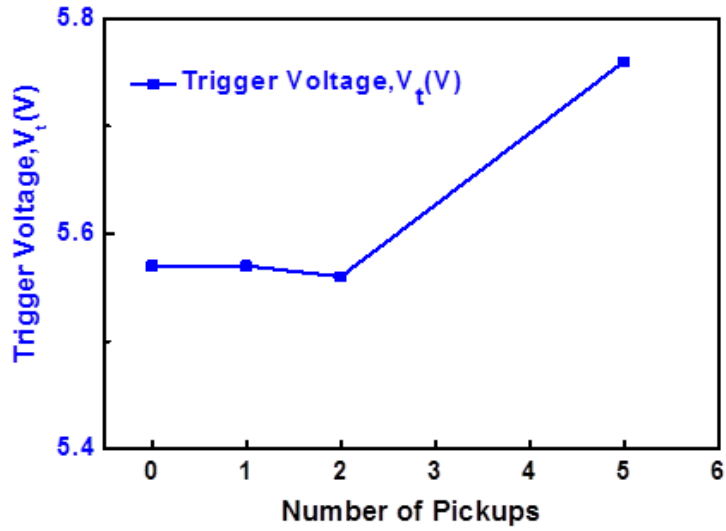


Fig.2.27. Measured the dependence of It1(TLP) on different pickup numbers of GDPMOS.

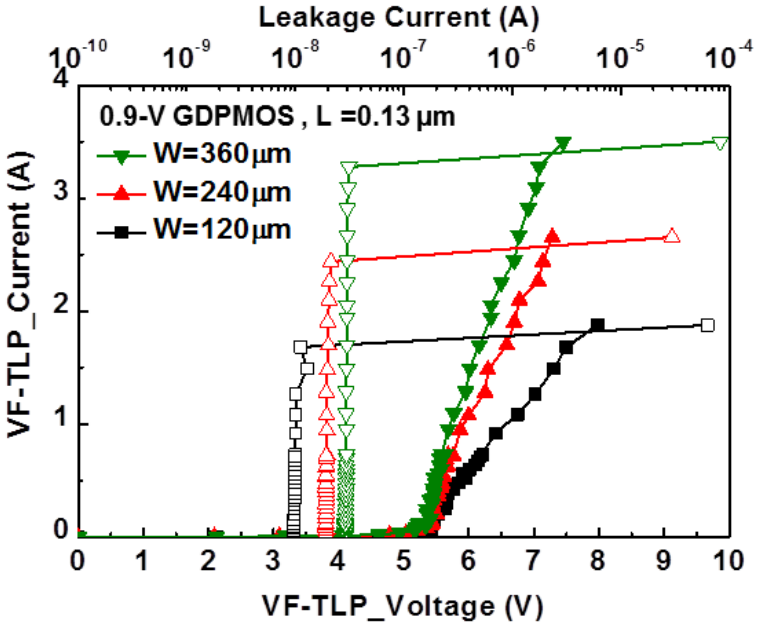


Fig.2.28. Measured VF-TLP I-V curves of GDPMOS with different multi-finger width.

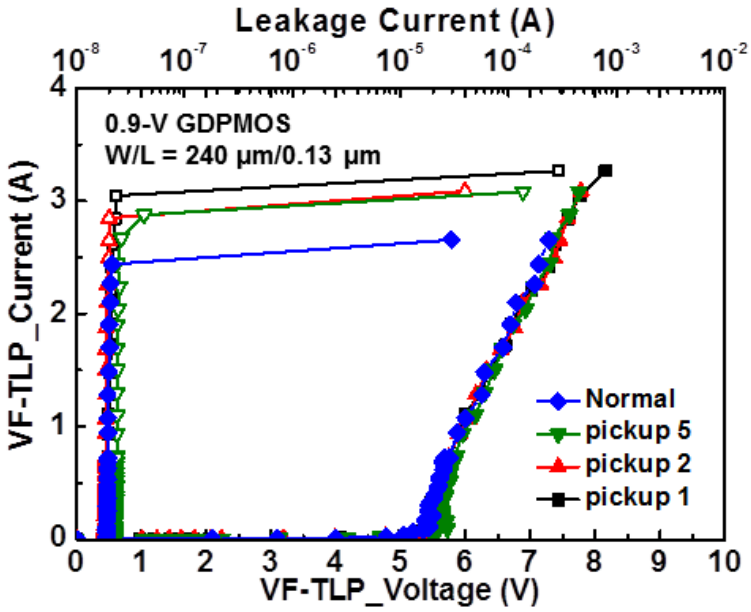


Fig.2.29. Measured VF-TLP I-V curves of GDPMOS with different pickup number.

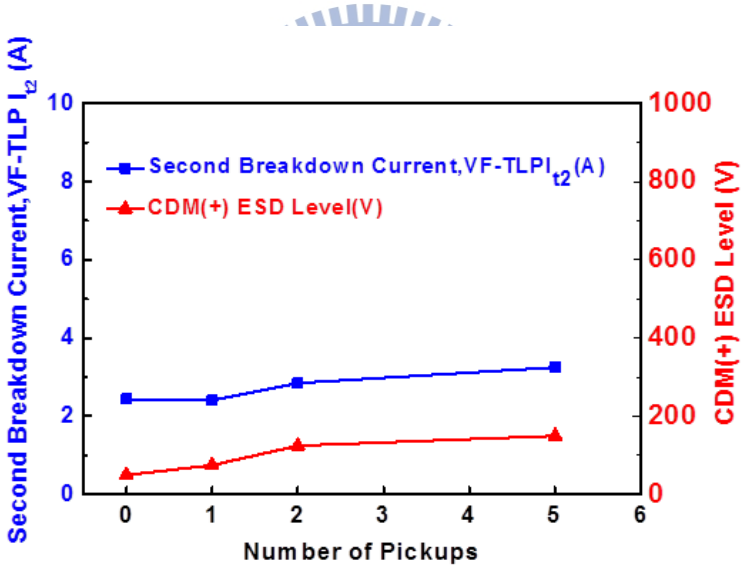


Fig.2.30. Measured the dependence of It2(VF-TLP) and CDM level on different pickup numbers of GDPMOS.

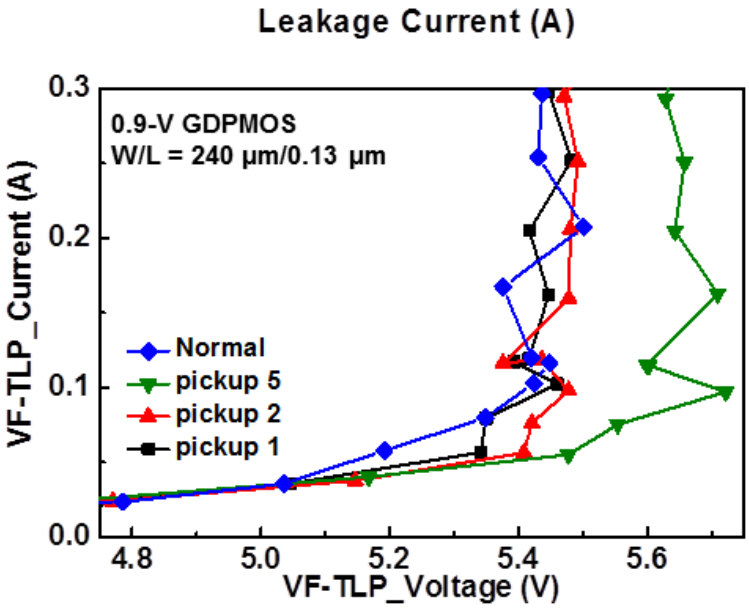


Fig.2.31. The zoom-in of VF-TLP I-V curves of GDPMOS with different pickup numbers.

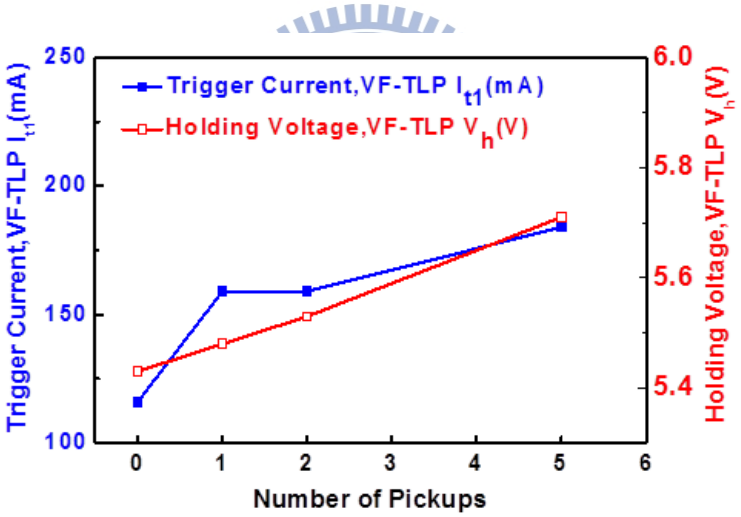


Fig.2.32. Measured the dependence of It1(VF-TLP)and Vh on different pickup numbers of GDPMOS.

2.5 Summary

Effect of additional layout pickups to the ESD robustness of GGNMOS and GDPMOS in the 28-nm high-k/metal gate CMOS process has been studied in this work. Experimental results show that inserting additional pickups has negative impact to the ESD protection level of GGNMOS and has scarcely impact to the ESD protection level of GDPMOS. Besides, layout area of GGNMOS and GDPMOS expands due to the insertion of additional pickups. All experiment data of the GGNMOS and GDPMOS are listed in Table 2.1 and Table 2.2, respectively. Therefore, additional pickups are not suggested for ESD protection multi-finger GGNMOS and GDPMOS in 28-nm high-k/metal gate CMOS process.

Table 2.1 The measurement data of GGNMOS

Test Device	Silicide Blocked	W/L (μm/μm)	Pickup Number	TLP				HBM (kV) step = 0.25 (kV)	VF-TLP				CDM(V) step = 25 (V)	
				V_{t1} (V)	I_{t1} (mA)	I_{t2} (A)	V_h (V)	Charge Voltage (+)	V_{t1} (V)	I_{t1} (mA)	I_{t2} (A)	V_h (V)	Charge Voltage (+)	Charge Voltage (-)
GGNMOS	Yes (Drain)	120/0.13	0	4.30	3.29	0.60	3.98	1.50	4.15	13	1.92	4.01	275	75
		240/0.13	0	4.07	7.55	0.97	3.91	3.00	4.01	32	2.86	3.93	325	225
			1	4.45	8.51	0.90	4.05	2.75	4.13	30	3.21	4.01	250	175
			2	4.64	12.17	0.26	4.13	2.50	4.46	27	2.85	4.41	350	225
			5	4.90	85.90	0.14	4.52	2.25	4.89	40	3.29	4.72	350	200
		360/0.13	0	4.04	65.16	1.25	3.95	4.50	4.02	36	5.47	3.93	425	525

Table 2.2 The measurement data of GDPMOS

Test Device	Silicide Blocked	W/L (μm/μm)	Pickup Number	TLP				HBM (V) step = 25 (V)	VF-TLP				CDM(V) step = 25 (V)	
				V_{t1} (V)	I_{t1} (mA)	I_{t2} (A)	V_h (V)	Charge Voltage (+)	V_{t1} (V)	I_{t1} (mA)	I_{t2} (A)	V_h (V)	Charge Voltage (+)	Charge Voltage (-)
GDPMOS	Yes (Drain)	120/0.13	0	NA	NA	0.091	NA	200	5.43	98	1.68	5.43	100	100
		240/0.13	0	NA	NA	0.096	NA	275	5.43	116	2.44	5.43	50	125
			1	NA	NA	0.054	NA	175	5.59	159	2.41	5.48	75	125
			2	NA	NA	0.046	NA	125	5.57	159	2.43	5.53	125	275
			5	NA	NA	0.042	NA	100	5.74	184	3.25	5.71	150	300
		360/0.13	0	NA	NA	0.091	NA	325	5.33	380	3.27	5.33	100	425

Chapter3

Improving ESD Robustness of PMOS Device with Embedded SCR in Advanced CMOS Process

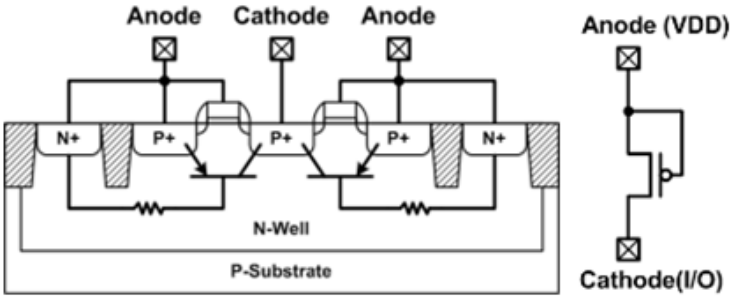
3.1 Introduction and Motivation

To discharge the high ESD energy without causing damage to integrated circuits, the tum on of parasitic bipolar junction transistors (BJTs) inherent in NMOS or PMOS transistors plays an important role. The NMOS and the PMOS with gate connected to source have been used as the ESD clamp devices, that is to say, gate-grounded NMOS (GGNMOS) and gate-VDD PMOS (GDPMOS). The device cross-sectional view of the GGNMOS and the GDPMOS are shown in Figs. 3.1 and 3.2, respectively. When the GGNMOS or the GDPMOS is under ESD stress, the parasitic NPN (N+, P-well, and N+) or PNP (P+, N-well, and P+) BJT will be triggered to discharge ESD current. Since the electron mobility is higher than the hole mobility in the CMOS technologies, the turn-on efficiency of NPN embedded in NMOS is much better than that of PNP embedded in PMOS. Therefore, the NMOS-based ESD clamp devices have the better ESD robustness [14]. The PMOS-based ESD clamp devices can be used with no snapback or low-leakage applications, because the leakage current of NMOS was often larger than that of PMOS in advanced CMOS technologies [14], [15]. Of course, the device dimension of PMOS should be larger than that of NMOS to achieve the same ESD robustness.

In order to enhance the turn-on efficiency of PMOS-based ESD clamp device, a novel ESD protection design by using PMOS device with embedded silicon-controlled rectifier (SCR) is proposed in this work.

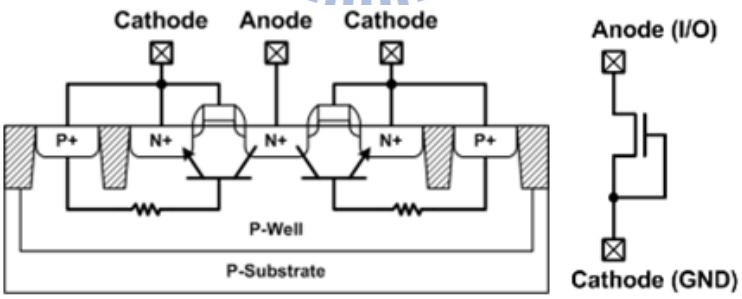
The SCR device has been reported to be useful for ESD protection due to its high ESD

robustness, small device size, and excellent clamping capabilities (low holding voltage and small turn-on resistance) [16]-[21]. Besides, the SCR device can be safely used without latchup danger in advanced CMOS technologies with low supply voltage [22]. It has been reported that ESD protection design for I/O cells with embedded SCR [23] and the high-voltage output arrays with embedded SCR [24]. The novel design of PMOS device with embedded SCR will be presented in Section 3.2 and 3.3. The proposed device has been verified in a 28-nm high-K/metal gate CMOS process.



(a) (b)

Fig.3.1. (a) Cross-sectional view and (b) schematic circuit of GGNMOS.



(a) (b)

Fig.3.2. (a) Cross-sectional view and (b) schematic circuit of GDPMOS.

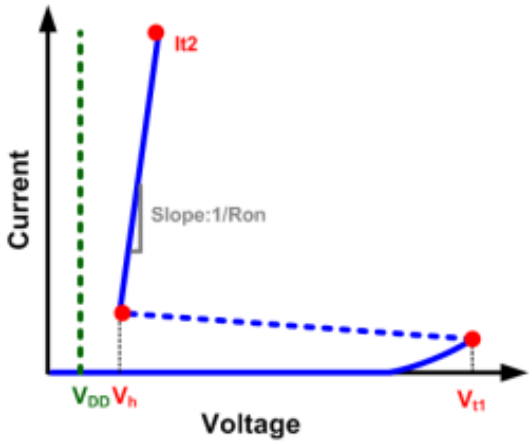


Fig.3.3. The I-V characteristics of the traditional SCR.

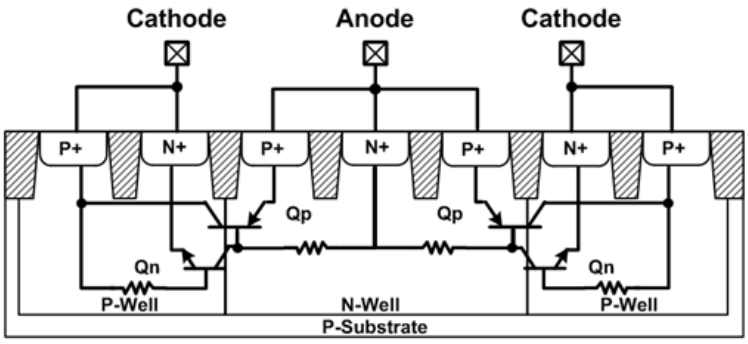


Fig.3.4. Cross-sectional view of the traditional SCR.

3.2 The Proposed ESD Protection Design

3.1.2 Device Structure and Chip Photo

The device cross-sectional view of the proposed PMOS device with embedded SCR is shown in Fig.3.5, where the P-ESD denotes the p-type ESD implantation [25]. In this design called the proposed device (type A), additional N+ region and the drain of the PMOS are added into the cathode side of the proposed device (type A). Besides, the P-ESD layer at cathode side is used to isolate the N-Well and N+ region. The SCR path consists of P+, N-Well, P+/P-ESD, and N+. As ESD zapping from the anode to the cathode, the PMOS device will quickly breakdown to discharge the initial ESD current through the parasitic PNP,

and then the positive-feedback regenerative mechanism of PNP (P+, N-Well, and P+/P-ESD) and NPN (N-Well, P-ESD, and N+) results in the SCR path highly conductive to discharge the major ESD current. Under normal circuit operating conditions, the PMOS is turned off and the SCR is also kept off. The test devices have been fabricated in a multi-project wafer (MPW). Fig. 3.6 shows the chip photograph of the test circuits.

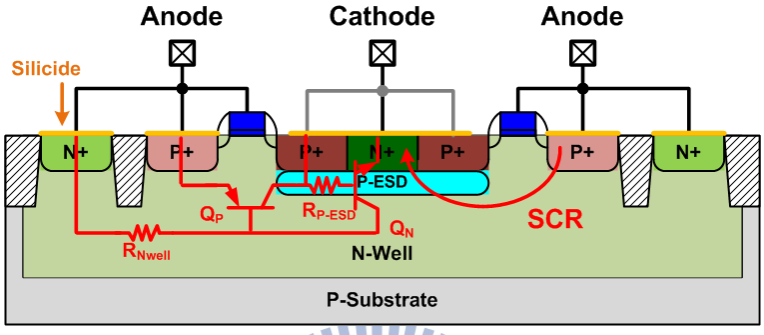


Fig.3.5. Cross-sectional view of the proposed PMOS device with embedded SCR.

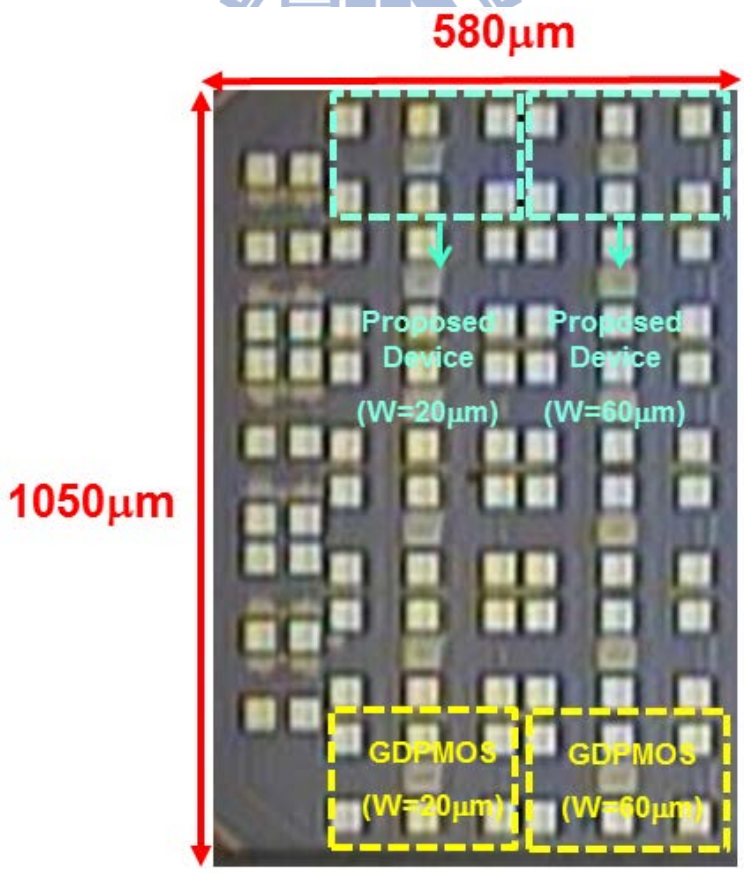


Fig.3.6. Chip micrograph of test devices.

3.1.3 TLP Characteristics

The TLP-measured I-V curves of the proposed devices (type A) and GDPMOS are shown in Fig. 3.7. The GDPMOS are hard to turn on. Besides, the proposed devices (type A)with 20- μ m and 60- μ m widths have no snapback phenomenon and the TLP TLP-measured I-V curves are almost the same as GDPOS in the same dimension . The results indicate that the ESD level is super low in this process and the SCR path is not turn-on before the GDPMOS embedded in the proposed device (type A) are burned.

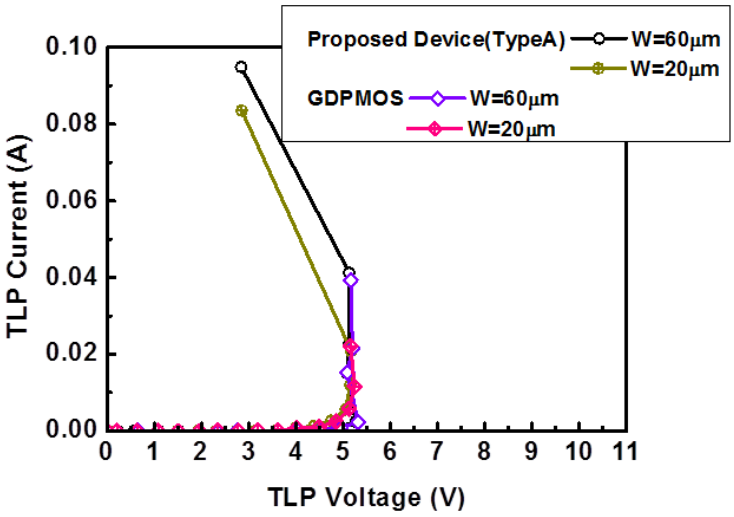


Fig.3.7. Measured TLP I-V curves of the test device (W=20- μ m and 60- μ m).

3.1.4 Failure Analysis

After ESD test, the scanning electron microscope (SEM) was used to find the failure locations. Fig. 3.8 shows the SEM photograph of the proposed device with 60- μ m width after 150-V HBM ESD test. Fig. 3.9 is the cross-section view of the proposed device with 60- μ m width. The failure points are located at the GDPMOS paths and the gate oxide. The SEM photograph indicates that the embedded SCR can not be turned on before the GDPMOS embedded in the proposed device are burned under HBM ESD stress.

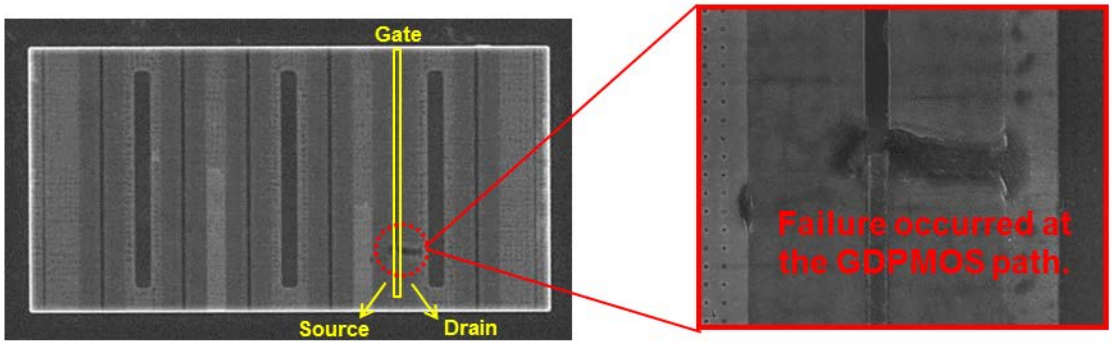


Fig.3.8. SEM photo of the proposed device (W=60 μ m) after HBM ESD tests.

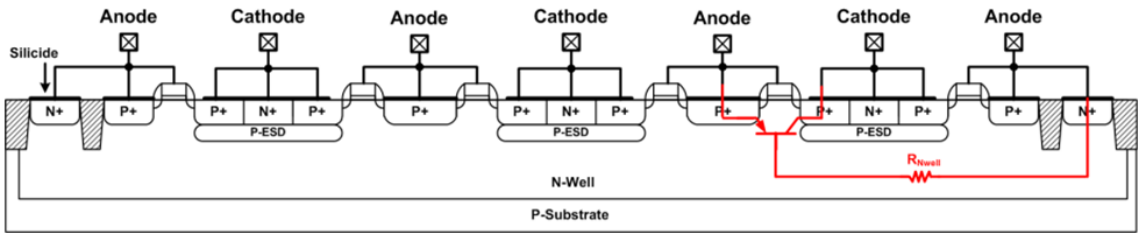


Fig.3.9. Cross-sectional view of the proposed device (W=60 μ m).

3.1.5 Summary

According to the TLP measured results and SEM photo, the PMOS device was quickly breakdown to discharge the initial ESD current through the parasitic PNP. However, the positive-feedback regenerative mechanism of PNP (P+/P-ESD, N-well, and P+/P-ESD) is still not happened and then the GDPMOS is burned out. Because, the barrier height of P+/P-ESD is lower than that N+/P-ESD at cathode. Thus, the ESD level is very low of GDPMOS in this process and the proposed device is not turned on.

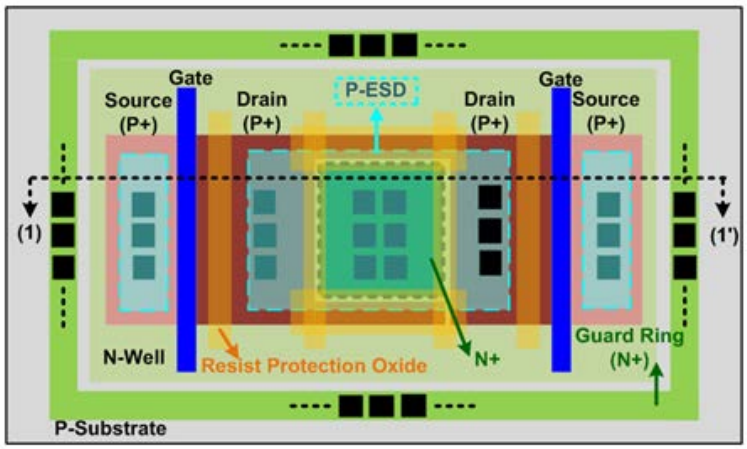
3.2 Modified the Proposed ESD Protection Design in 28-nm High-K Metal Gate Process

3.2.1 Device Structure and Chip Photo

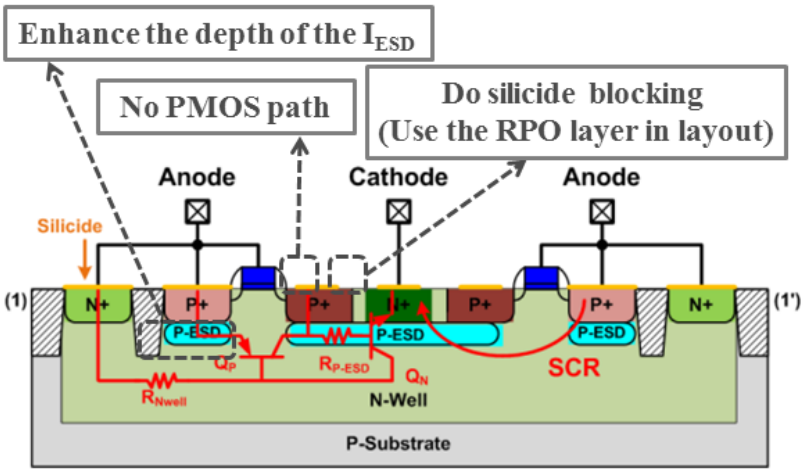
The layout top view and cross-sectional view of the modified device (type B) are shown in Fig. 3.10 (a) and (b). In this design, the proposed device (type A) in section 3.2 is modified.

This N+ of the proposed device is separated from the P+ that is the drain of the GDPMOS, and the silicide blocking is used on the surface of this N+ and P+. Besides, the P-ESD layer at anode side is used to enlarge the SCR path. The SCR path consists of P+/P-ESD, N-well, P+/P-ESD, and N+. As ESD zapping from the anode to the cathode, the PMOS device will quickly breakdown to discharge the initial ESD current through the parasitic PNP, and then the positive-feedback regenerative mechanism of PNP (P+/P-ESD, N-well, and P+/P-ESD) and NPN (N-well, P-ESD, and N+) results in the SCR path highly conductive to discharge the major ESD current.

To reduce the trigger voltage of an SCR device, the trigger current can be sent into the base terminal of NPN BJT in the SCR device. The trigger current is inversely related to the trigger voltage of the SCR device; therefore, some trigger techniques have been reported, such as the gate-coupled, substrate-triggered, and GGNMOS-triggered techniques [21]. This part will be measured in section 3.3.5. The test devices have been fabricated in a multi-project wafer (MPW). Fig. 3.11 shows the chip photograph of the test circuits.



(a)



(b)

Fig.3.10. (a) Layout top view and (b) cross-sectional view of the modified proposed device.

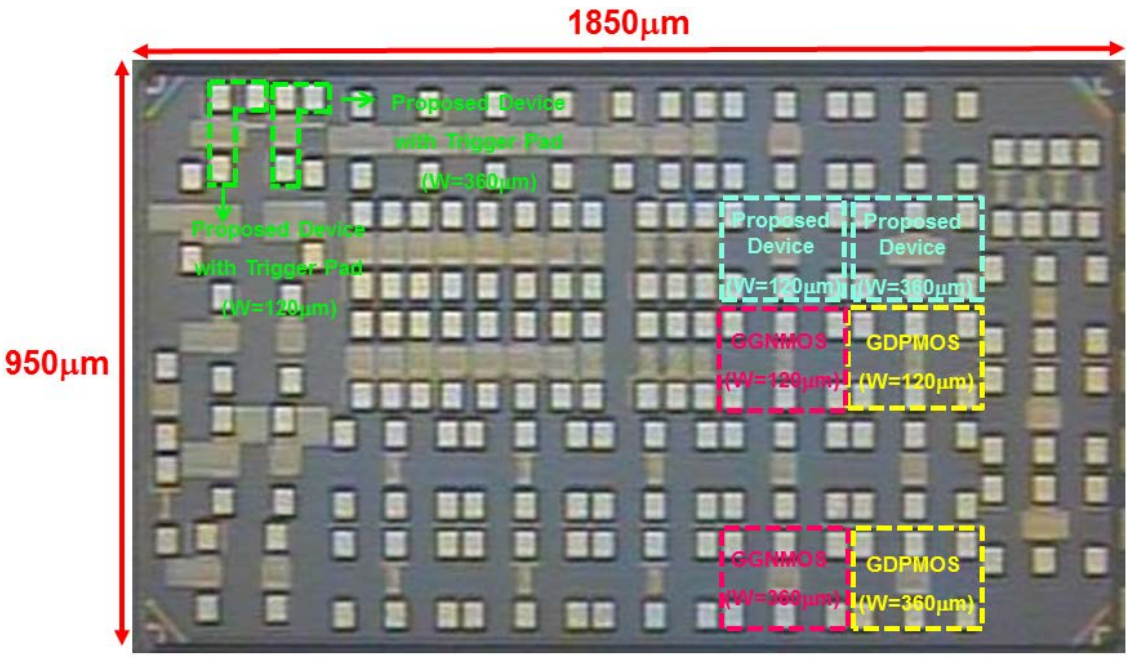


Fig.3.11. Chip micrograph of test devices.

3.2.2 ESD Robustness and System-Level ESD test

According to the measurement results, the proposed devices with 120- μm and 360- μm widths can pass 7.5-kV and 8-kV HBM ESD tests, respectively, while the GGNMOS can only pass 1.5-kV and 3.5-kV HBM ESD tests, respectively. The GDPMOS even can not pass 0.5-kV HBM ESD tests.

From the measurement results, the proposed devices (type B) with 120-μm and 360-μm widths can pass +725-V and over than +2-kV CDM ESD tests, respectively, while the GGNMOS/GDPMOS can only pass +225-V/ +100-V and +275-V/+100 CDM ESD tests, respectively. Besides, the proposed devices with 120-μm and 360-μm widths can pass -125-V and over than -2-kV CDM ESD tests, respectively, while the GGNMOS/GDPMOS can only pass -75-V/ -100-V and -250-V/-325 -V CDM ESD tests, respectively. Moreover, the ESD current goes through parasitic diode (P-well, and N+), BJT (P+, N-well , and P+), and SCR (P+/P-ESD, N-well, P-ESD, and N+) path of the GGNMOS, GDPMOS, and proposed device when positive CDM ESD tests that means zap positive voltage to the well of the test devices. In addition, the ESD current goes through BJT (N+, P-well , and N+), parasitic diode (P+, and N-well),and BJT (N+, P-ESD, N-well) path of the GGNMOS, GDPMOS, and proposed device when positive CDM ESD tests that means zap negative voltage to the well of the test devices.

According to IEC 61000-4-2, two test modes have been specified, which are the air-discharge and contact-discharge test mode. The proposed devices (type B) with 360-μm widths can pass 7-kV in air-discharge test mode and 4-kV in contact-discharge test mode

3.2.3 TLP and VF-TLP I-V Characteristics

The TLP-measured I-V curves of the proposed device (type A and type B) are shown in Fig. 3.12 and Fig. 3.13, respectively. The proposed devices (type A)with 120-μm re tough to be turned on totally because Vt1 is not enough to make the parasitic NPN BJT to be turned on. Besides, the Vt1 of the proposed devices (type A) with 360-μm widths is sufficient to let the parasitic NPN BJT to be turned on. The parasitic NPN and PNP BJT are independent on each other, so the snapback phenomenon is not strong.

The proposed devices (type B)with 120-μm and 360-μm widths can achieve the TLP-measured It2 of 3.43A and 4.87A, respectively. The consequence indicates that the

modified propose device that is called the proposed device (type B) is verified successfully. The SCR path is observed due to the strong snapback effect.

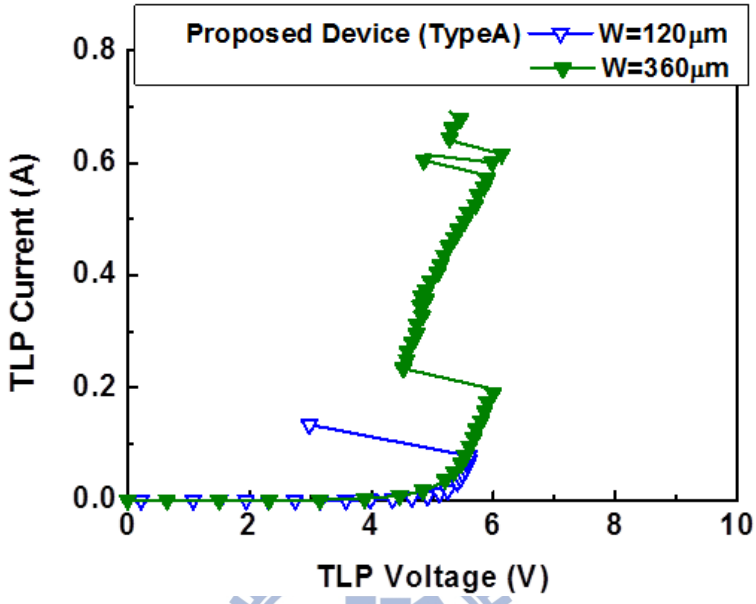


Fig.3.12. Measured TLP I-V curves of the test device type A (W=120- μ m and 360- μ m).

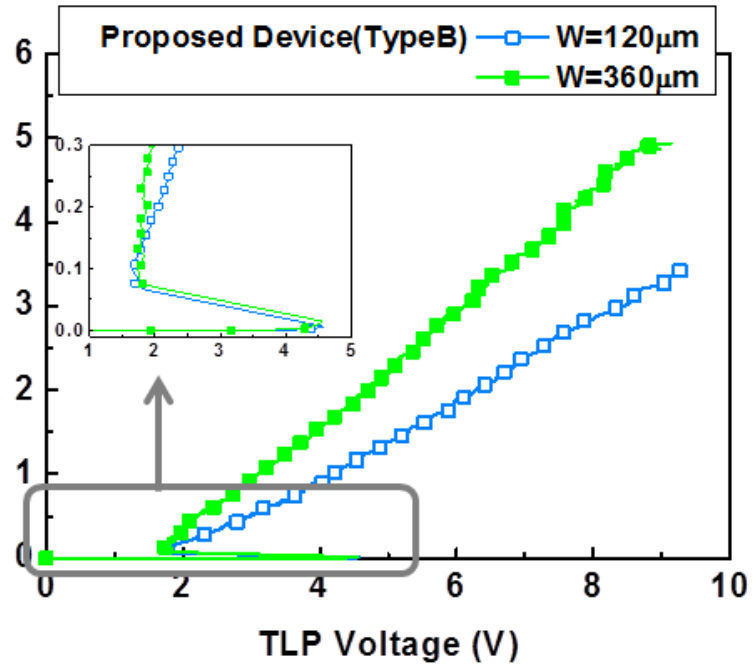


Fig.3.13. Measured TLP I-V curves of the test device type B (W=120- μ m and 360- μ m).

The TLP-measured I-V curves of the test devices are shown in Fig. 3.14. The proposed devices (type B)with 120- μ m and 360- μ m widths can achieve the TLP-measured It2 of

3.43A and 4.87A, respectively, while the GGNMOS have only 0.60A and 1.25A, respectively. The GDPMOS are hard to turn on. The holding voltages of the proposed devices are ~1.7V, while those of the GGNMOS are ~4V. The holding voltages of the proposed devices exceed VDD (0.9V in the given CMOS process), which is safe from latchup event. The proposed ESD protection design with lower Vhold and higher It2 is more suitable for ESD protection. The Ron of the proposed devices (type B)is much bigger than the traditional SCR, because the most part of current goes through P+/P-ESD, N-well, P+/P-ESD, and N+ and fewer current goes through P+/P-ESD, N-well, P-ESD, and P+. Thus, the cross-section area of the critical interface are small than the traditional SCR. The smaller cross-section area, and the higher Ron.

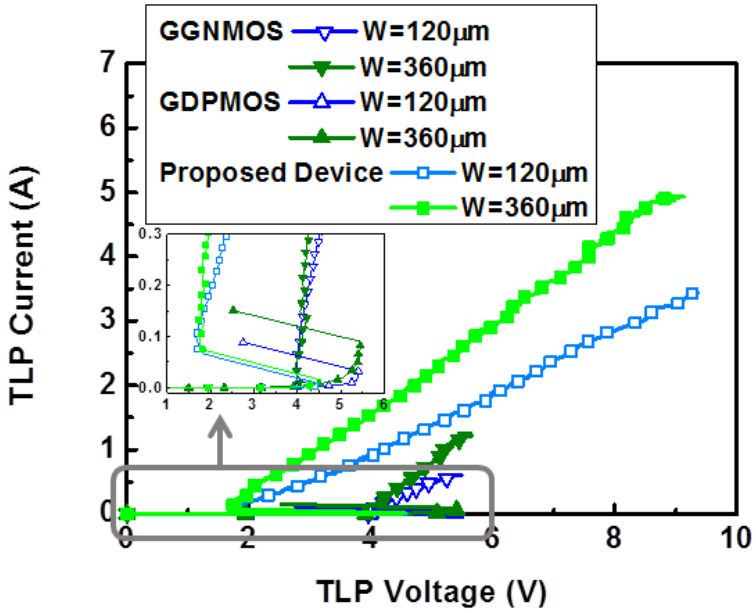


Fig.3.14. Measured TLP I-V curves of the test devices (W=120- μm and 360- μm).

The VF-TLP-measured I-V curves of the test devices are shown in Fig. 3.15. The VF-TLP-measured It2 of the proposed devices with 120- μm and 360- μm widths are 2.49A and 4.05A, respectively, while those of the GGNMOS/GDPMOS are only 1.94A/1.68A and 4.44A/3.47A, respectively. The measurement results show that all the test devices are fast enough to be turned on under the fast CDM-like ESD-transient events.

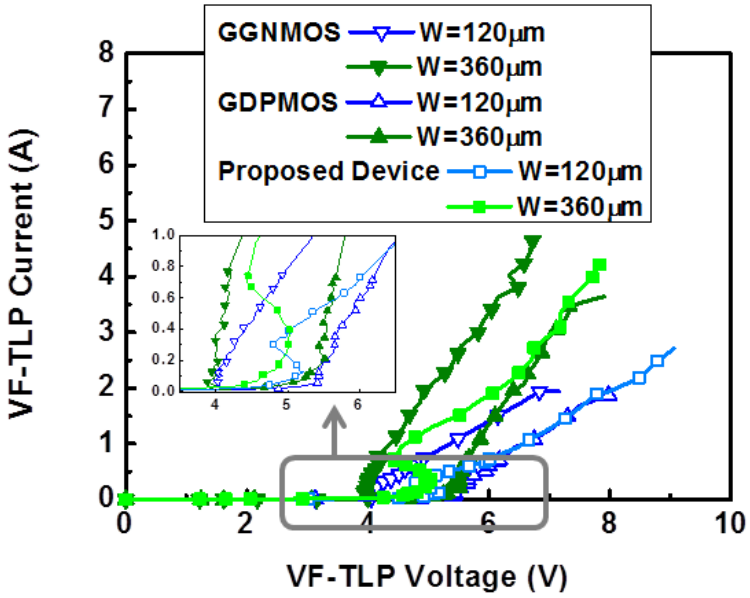


Fig.3.15. Measured VF-TLP I-V curves of the test devices (W=120- μ m and 360- μ m).

3.2.4 Parasitic Capacitance

If the ESD protection device is adopted at an I/O pad, the parasitic capacitance should be considered. The two-port S-parameters of the test devices are measured on wafer. The parasitic effects of the pads and metal routing have been removed by using the de-embedding technique [26]. The parasitic capacitance of each test device was extracted from the S-parameters. Fig. 3.16 shows the extracted parasitic capacitances of the test devices. The parasitic capacitances of the proposed devices with 120- μ m and 360- μ m widths are 90.1fF and 233.5fF, respectively, while those of GGNMOS/GDPMOS are 201.8fF/172.6fF and 607.4fF/480.3fF, respectively.

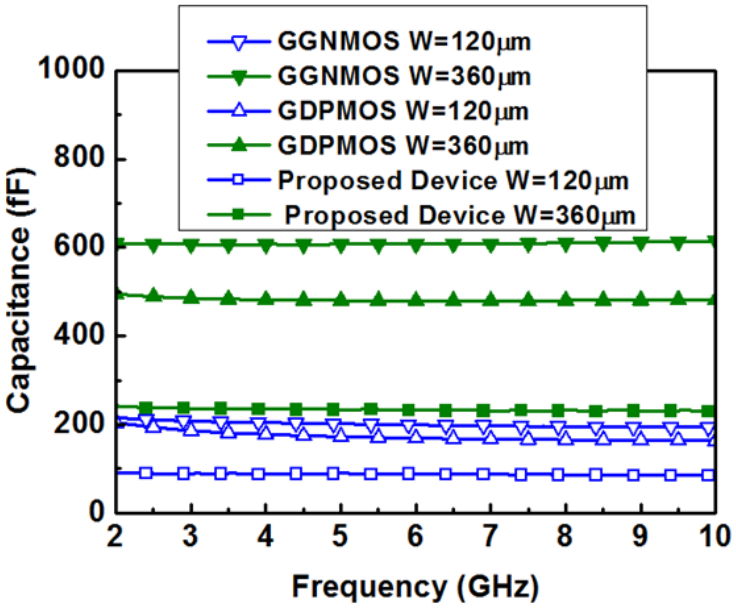


Fig.3.16. Measured parasitic capacitances.

3.2.5 Trigger Mechanism

To investigate the relationship between the trigger current and the trigger voltage, additional trigger pad is connected to the PMOS device with embedded SCR, as shown in Fig. 3.17.

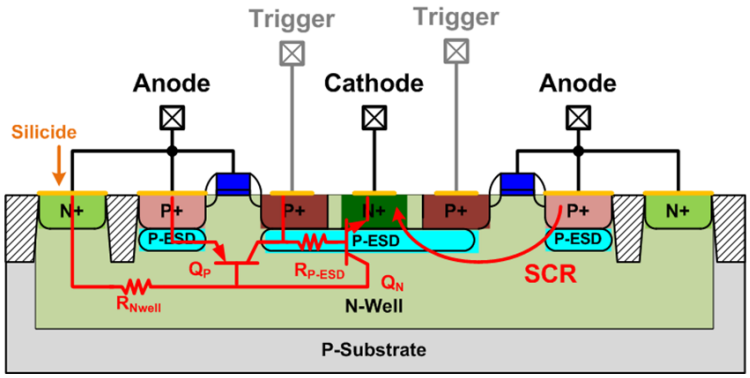


Fig.3.17. Cross-sectional view and of proposed device (type B) with trigger pad.

The dc trigger current (Itrig) was injected into the trigger pad of the proposed device, as measuring the TLP I-V curves. Fig. 3.18 exhibits the measurement setup that employ Keithley 2400 source meter to provide Itrig for the proposed device while the proposed device under

TLP tests. Fig. 3.19 and Fig. 3.20 show the TLP-measured I-V curves of the proposed device under different trigger currents. The trigger voltage of the proposed device can be further reduced with the larger trigger current. If the trigger current is continually increased, the trigger voltage of the proposed device will be reduced to a value close to its holding voltage. Besides, the trigger current will not degrade the holding voltage, turn-on resistance, and secondary breakdown current of the test devices. All experiment data are listed in Table 3.1.

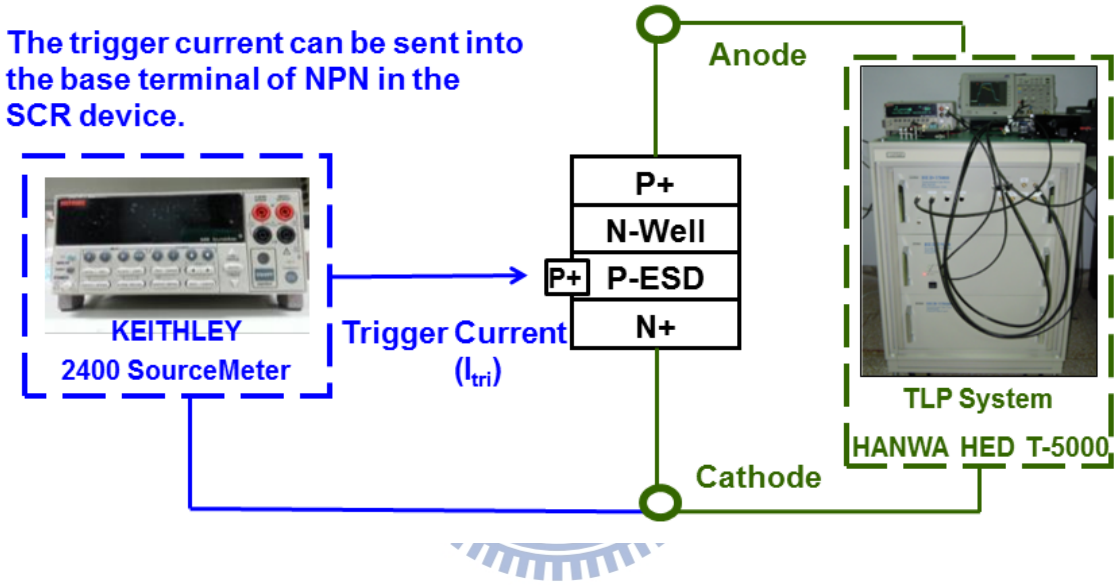


Fig.3.18. Measurement setup from dc trigger to observe TLP I-V curves.

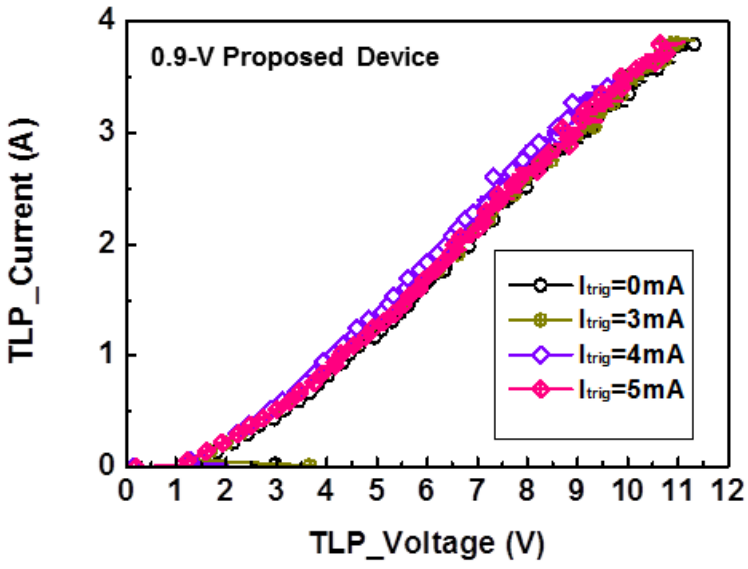


Fig.3.19. TLP-measured I-V curves of the proposed device (W=120- μ m) under different dc

Itri.

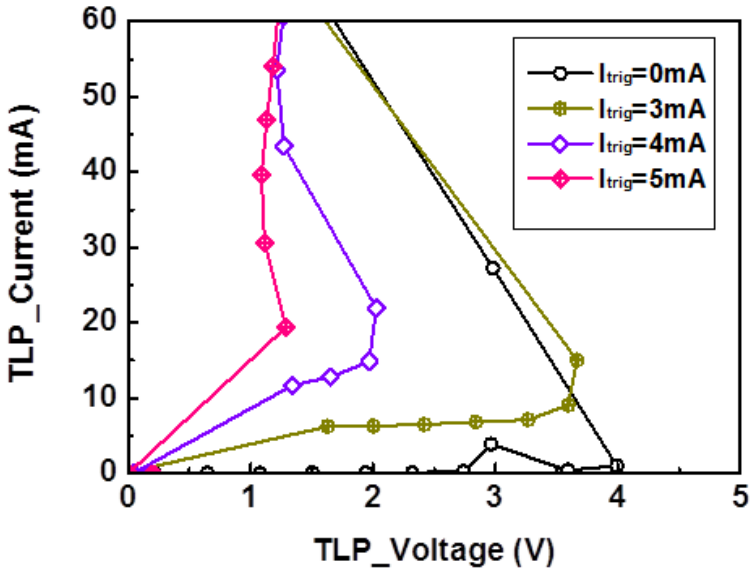


Fig.3.20. The zoom-in of TLP I-V curves of the proposed device under different dc Itri.

Table 3.1 The relation between trigger voltage and off-chip trigger current from keithley 2400 source meter

Itri(mA)	0	3	4	5
Vt1(V)	3.99	3.66	2.02	1.28
TLP It2(A)	3.83	3.86	3.47	3.40

The dc I-V curves of the proposed devices under different trigger currents are also measured. Fig. 3.21 exhibits the measurement setup that employ Tek370 that is a dc curve tracer to provide Itrig for the proposed device while the proposed device under Tek370 tests. The dc I-V curves are shown in Fig. 3.22. The trigger voltage of the proposed device can be further reduced with the larger trigger current that is shown in Fig. 3.23.The holding voltages of the proposed devices under dc measurement are ~1.14V, which are lower than those under TLP measurement with different pulse widths due to the self-heating effect. All experiment data are listed in Table 3.2.

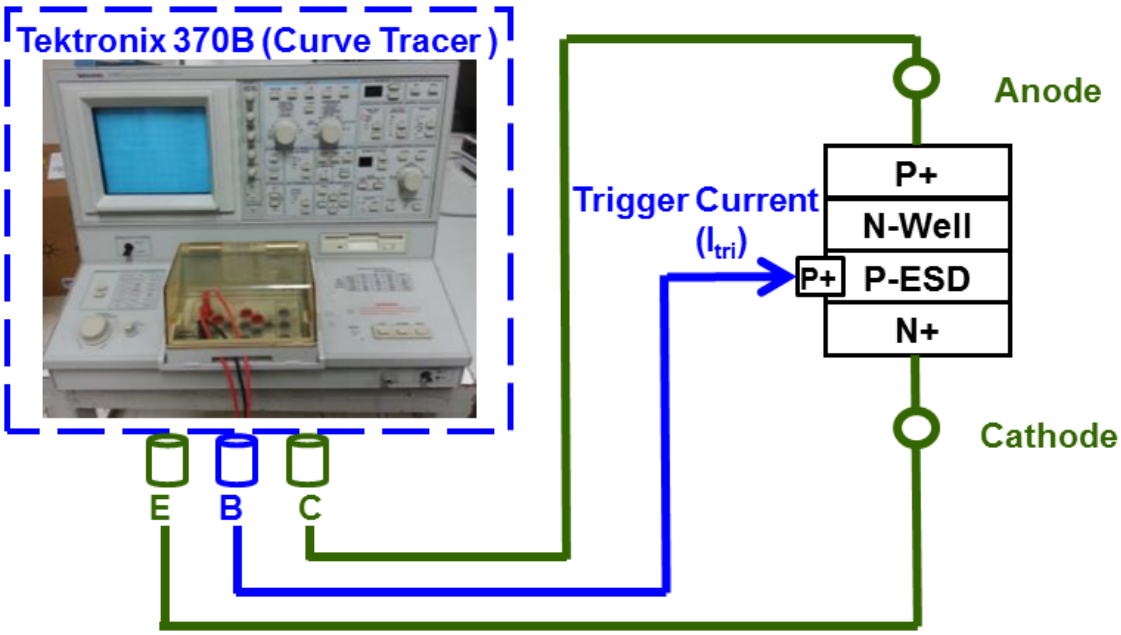


Fig.3.21. Measurement setup from dc trigger to observe DC I-V curves.

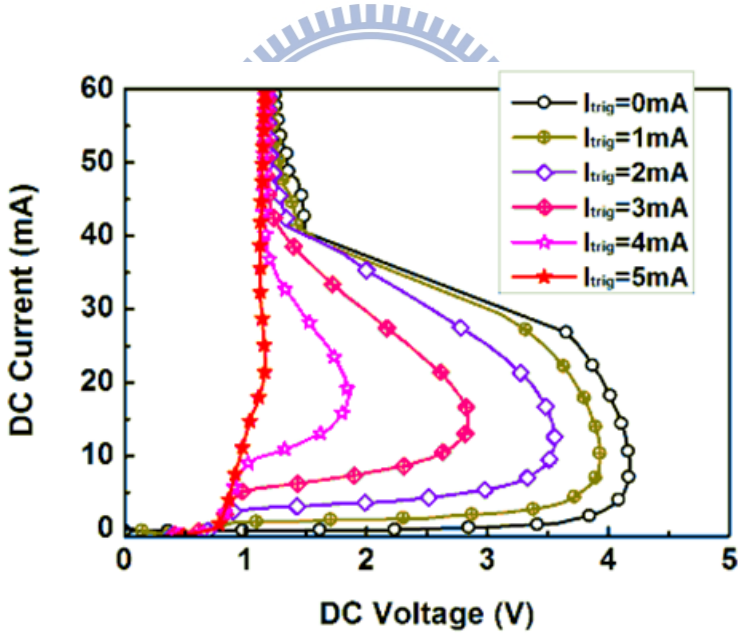


Fig.3.22. DC-measured I-V curves of the proposed device (W=120- μ m) under different dc I_{tri}.

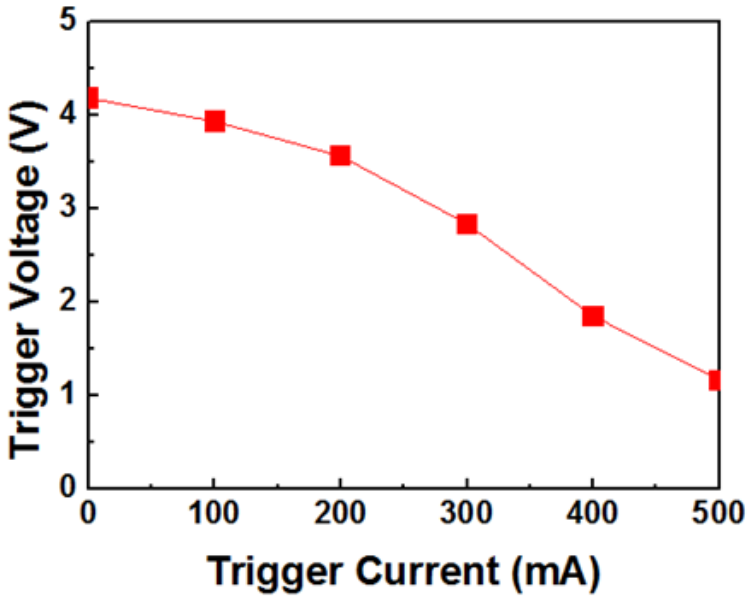


Fig.3.23. Relationship between the trigger voltage and the trigger current.

Table 3.2 The relation between trigger voltage and off-chip trigger current from Tek370

Itri(mA)	**0**	**1**	**2**	**3**	**4**	**5**
Vt1(V)	4.18	3.93	2.56	2.84	1.86	1.17

The trigger current (Itrig) from the different off-chip trigger circuits was injected into the trigger pad of the proposed device, as measuring the TLP I-V curves. Fig. 3.24 exhibits the measurement setup that utilize different off-chip trigger circuits to provide Itrig for the proposed device while the proposed device under TLP tests. Fig. 3.25 (a) and (b) show the TLP-measured I-V curves of the proposed device under different trigger currents. The trigger voltage of the proposed device can be further declined with the larger trigger current from different off-chip trigger circuits. If the trigger current is continually increased, the trigger voltage of the proposed device will be reduced to a value close to its holding voltage. Besides, the value of RC constant is bigger and the trigger voltage of the proposed device is smaller. In addition, the capacitance is dominant. RC constant value is selected to be distinguished ESD event from the normal operation condition and the RC constant is at least ~ 0.1 μ s because the pulse width of ESD is about 100ns. Moreover, the trigger current will not degrade the

holding voltage, turn-on resistance, and secondary breakdown current of the test devices.

All experiment data are listed in Table 3.3.

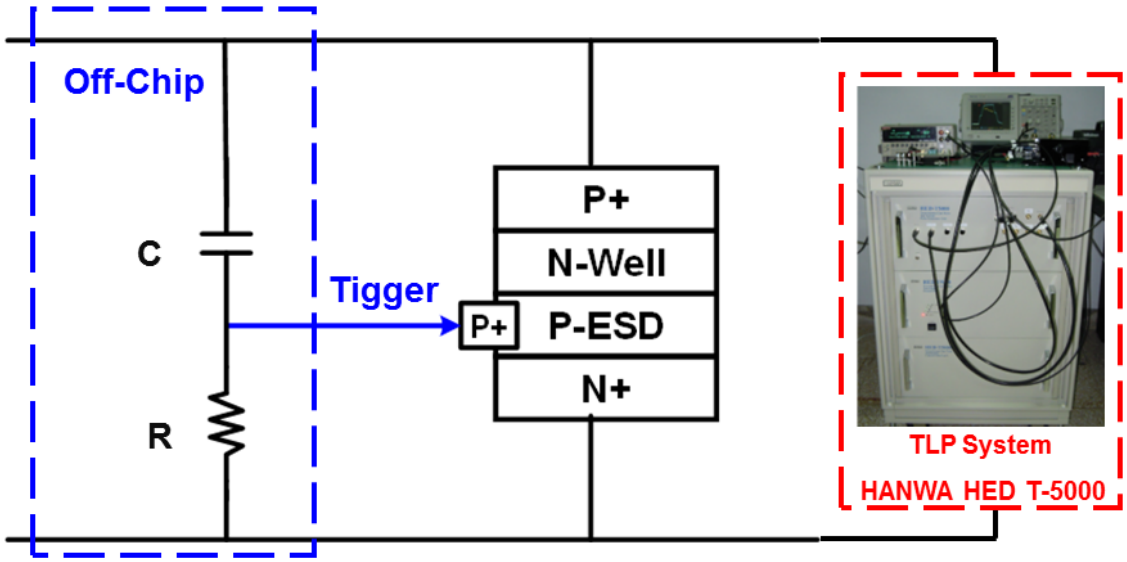


Fig.3.24. Measurement setup from C-R coupled trigger to observe TLP I-V curves.

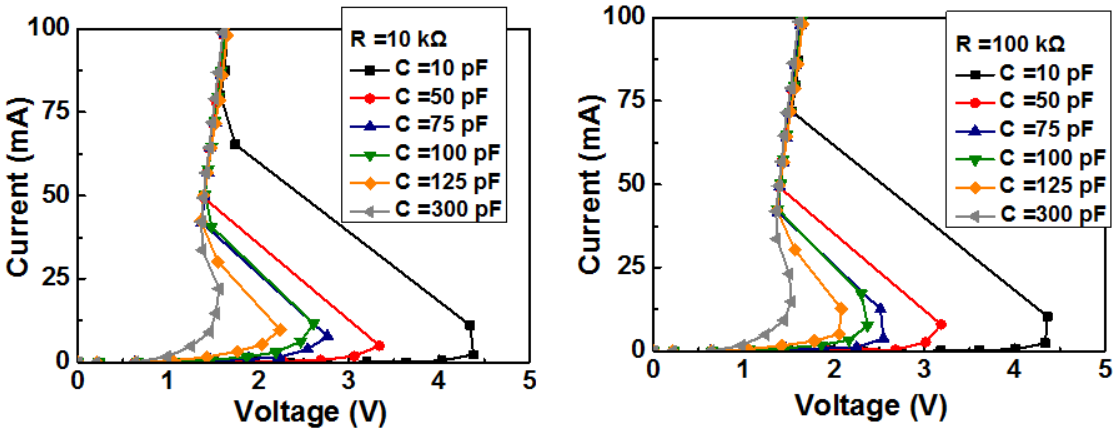


Fig.3.25. TLP-measured I-V curves of the proposed device (W=120- μ m) under different trigger circuit (a) various C value when R=10kΩ (b) various C value when R=100kΩ.

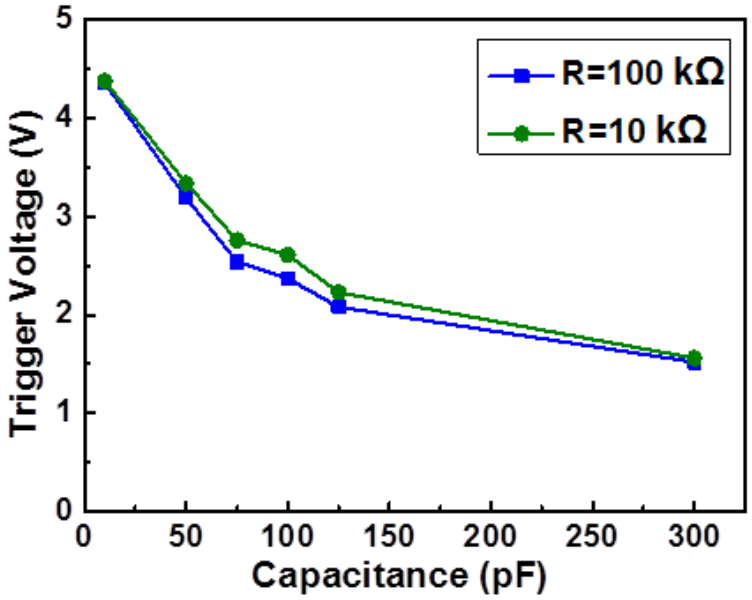


Fig.3.26. Relationship between the trigger voltage and the trigger current under different trigger circuit.

Table 3.3 The relation between trigger voltage and off-chip trigger current from CR coupled

R (kΩ)	**w/o**	**w/o**	**10**						**100**					
C (pF)	**w/o**	**100**	**10**	**50**	**75**	**100**	**125**	**300**	**10**	**50**	**75**	**100**	**125**	**300**
Vt (V)	4.40	2.49	4.38	3.34	2.76	2.61	2.23	1.56	4.36	3.19	2.54	2.37	2.08	1.52

3.2.6 Transient-Induced Latchup (TLU) Test

If the ESD protection device is used as the power-rail ESD clamp device, the latchup immunity should be considered. To evaluate the latchup immunity of the proposed device, the transient-induced latchup (TLU) was tested [27], [28] and the measure setup is shown in Figs. 3.27 . A 200-pF charging capacitor is used to store the charges as the TLU-triggering source, and then the stored charges are discharged to the test device through the relay. Figs. 3.28 (a) and (b) show the measured transient voltage waveforms of the proposed device under the TLU tests with charging voltage of +10V and -10V, respectively. Before the TLU tests, the voltage across the proposed device was 0.9V, which is the VDD voltage in the given CMOS process. During the TLU tests, the measured voltage waveforms are influenced

simultaneously by the underdamped sinusoidal voltage. After the TLU tests, the voltage across the proposed device was returned to 0.9V. From the TLU test results, the proposed device can immune to the latchup issue.

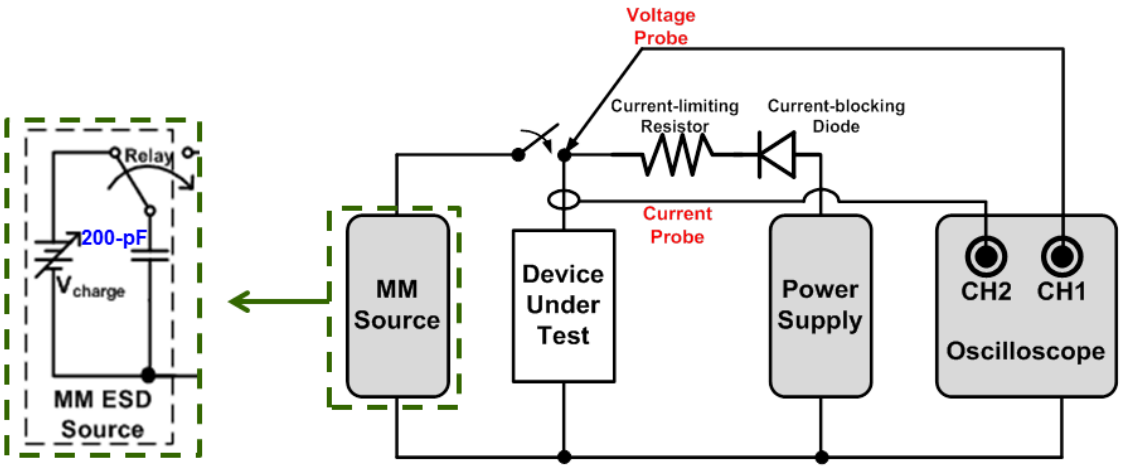
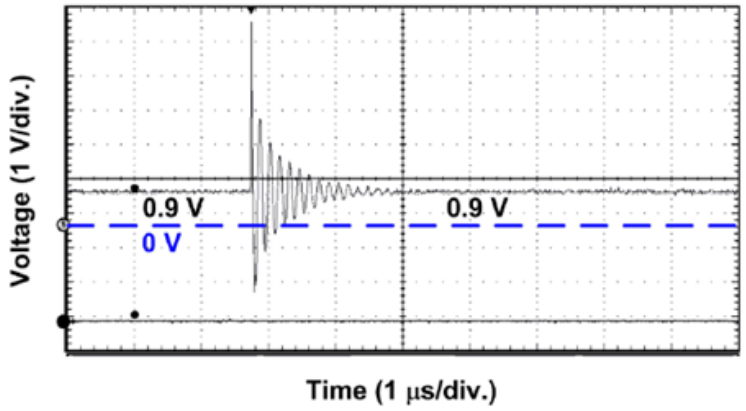
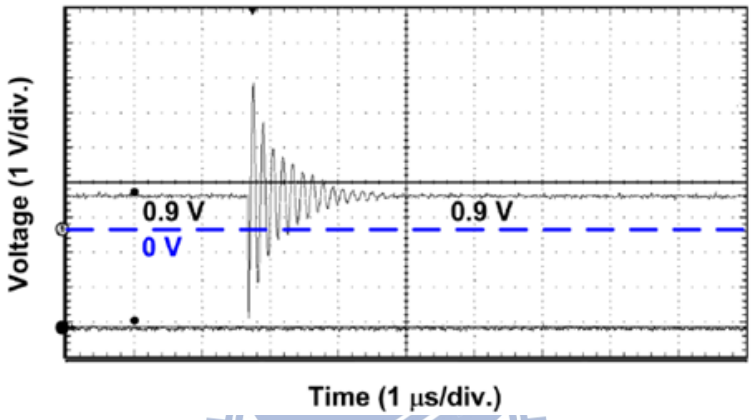


Fig.3.27. Measurement setup of a transient-induced latchup test.



(a)



(b)

Fig.3.28. Measured voltage waveforms on proposed device (W=120 μ m) under TLU tests with charging voltage of (a) +10V and (b) -10V.

3.2.7 Failure Analysis

After ESD test, the scanning electron microscope (SEM) was used to find the failure locations. Fig. 3.29 shows the SEM photograph of the proposed device with 120- μ m width after 8-kV HBM ESD test and step voltage of HBM ESD test is 0.5-kV. The failure points are located at the SCR paths and the gate oxide. The SEM photograph indicates that the embedded SCR can be uniformly turned on under HBM ESD stress. In addition, the proposed devices with360- μ m width can pass 8-kV HBM ESD tests and there are no failure point is observed on the SEM photo that are shown in Fig. 3.30.

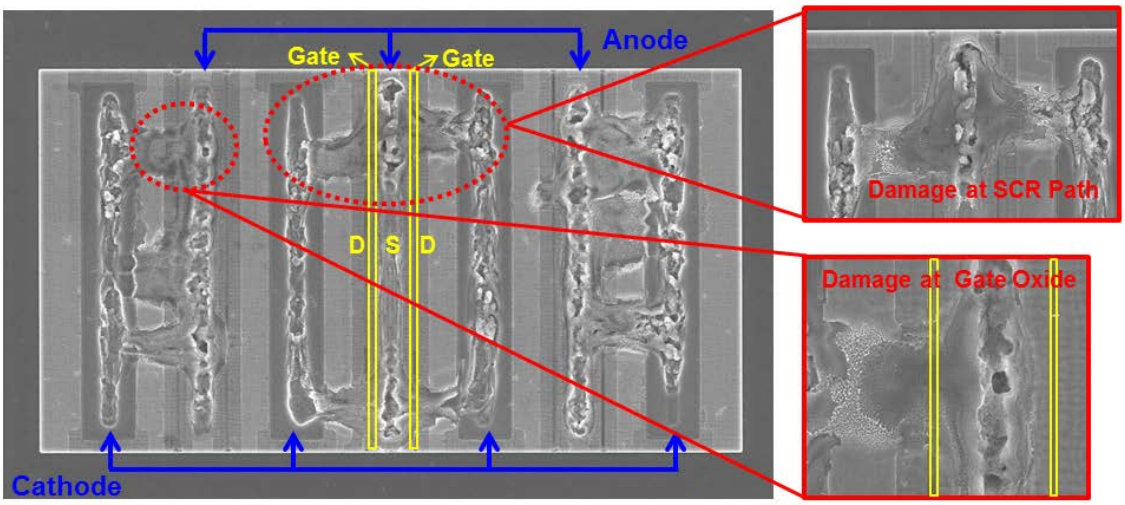


Fig.3.29. SEM photo of proposed device (W=120 μ m) after 8-kV HBM ESD tests.

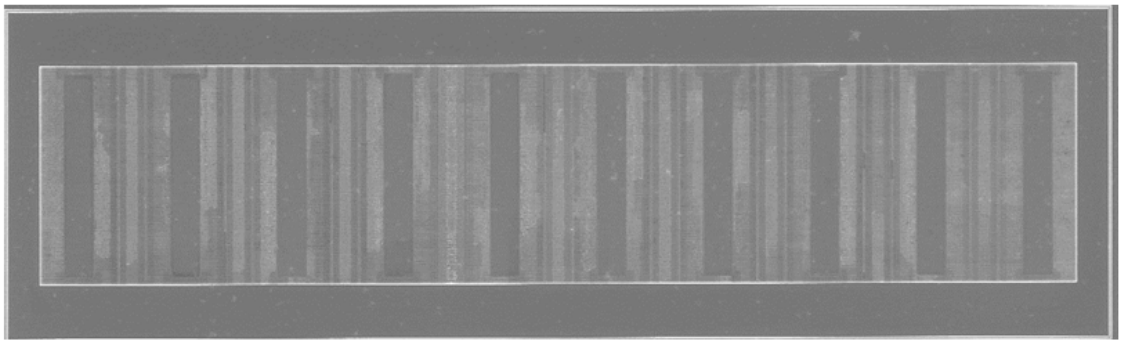


Fig.3.30. SEM photo of proposed device (W=360 μ m) after 8-kV HBM ESD tests.

3.2.8 Summary

The new ESD protection device of PMOS with embedded SCR has been designed, fabricated, and characterized in a 28-nm high-k/metal gate CMOS process. Modifying from the PMOS with additional P-type ESD implantation, the proposed device combines P+/P-ESD, N-well, P-ESD, and N+ to form the embedded SCR path. Verified in silicon chip, the proposed device (type B) with 120-μm/360-μm width has 7.5-kV/ higher than 8-kV HBM ESD robustness and 90.1-fF/233.5-fF parasitic capacitance, which is much better than the GGNMOS or GDPMOS. Besides, the proposed device has been tested to be free from latchup event. Therefore, the proposed device can be a better solution for ESD protection in sub-50-nm CMOS process. All experiment data of the test devices in a 28-nm high-k/metal gate CMOS process are listed in Table 3.4.

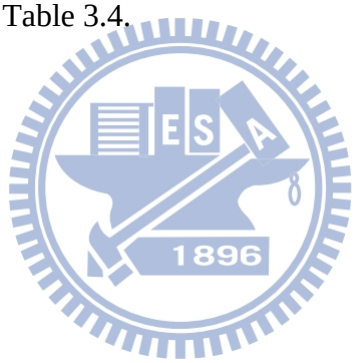


Table 3.4 The measurement data of test devices in a 28-nm high-k/metal gate CMOS process

		GGNMOS		GDPMOS		Proposed Device (Type B)	
Channel Width		**120μm**	**360μm**	**120μm**	**360μm**	**120μm**	**360μm**
Channel Length		**0.13μm**	**0.13μm**	**0.13μm**	**0.13μm**	**0.13μm**	**0.13μm**
TLP Vt1		4.30V	4.04V	N/A	N/A	4.58V	4.55V
TLP Vhold		3.98V	3.95V	N/A	N/A	1.66V	1.74V
TLP Ron		2.3Ω	1.3Ω	N/A	N/A	4.2Ω	1.5Ω
TLP It2		0.60A	1.25A	N/A	N/A	3.43A	4.87A
VF-TLP Vt1		4.06V	4.00V	5.41V	5.30V	5.22V	5.04V
VF-TLP Vhold		4.01V	3.88V	5.39V	5.25V	4.79V	4.40V
VF-TLP Ron		1.9Ω	0.7Ω	2.2Ω	0.6Ω	2.1Ω	0.7Ω
VF-TLP It2		1.94A	4.44A	1.68A	3.47A	2.49A	4.05A
HBM ESD Robustness		1.5kV	3.5kV	<0.5kV	<0.5kV	7.5kV	>8kV
CDM ESD Robustness	**Charge Voltage (+)**	225	275	100V	325V	725V	>2kV
	Charge Voltage (-)	75	250	100V	100V	125V	>2kV
Parasitic Capacitance		194 fF	614.5fF	164 fF	482.3fF	84.8fF	231.4fF

3.3 Modified the Proposed ESD Protection Design in 0.18-μm Process

3.3.1 Device Structure and Chip Photo

The modified proposed device added reverse path is called proposed device (type C) as shown in Fig. 3.31. In order to discharge more ESD current from the cathode to the anode of the proposed device (type B), P+ is inserted into cathode. Then, the parasitic diode (P+/P-ESD, N-Well/N+) is created. The reverse path of proposed device (type C) is parasitic diode (P+/P-ESD, N-Well/N+), while the reverse path of proposed device (type B) is parasitic npn (N+, P+/P-ESD, N-Well/N+) BJT. The ESD robustness of parasitic diode is higher than parasitic BJT.

The test devices have been fabricated in a multi-project wafer (MPW). Fig. 3.32 shows the chip photograph of the test circuits.

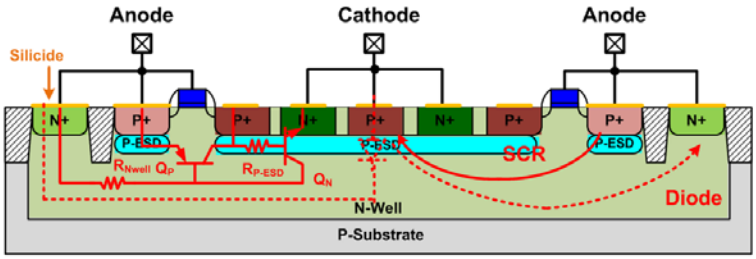


Fig.3.31. Cross-sectional view of the modified proposed device added reverse path.

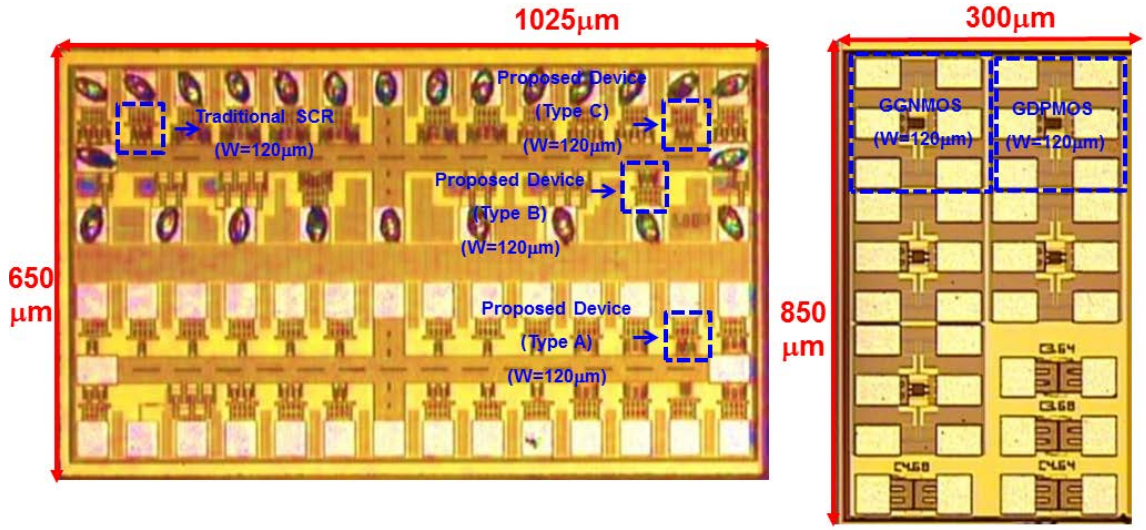


Fig.3.32. Chip micrograph of test devices.

3.3.2 ESD Robustness

Through the measurement results, the proposed devices including type A, B, and C with 120-μm widths can all pass 8-kV HBM ESD tests, while the GGNMOS/GDPMOS can only pass 2-kV and 1-kV HBM ESD tests, respectively. Besides, the traditional SCR can pass 8-kV HBM ESD tests.

3.3.3 TLP Characteristics

The TLP-measured I-V curves of the test devices 120-μm with width are shown in Fig. 3.33. The proposed devices with type A, type B, and type C can achieve the TLP-measured It2 of 7.14A, 8.27A and 8.17A, respectively, while the GGNMOS/GDPMOS have only 1.14/0.68A and 1.25A. The It2 of the traditional SCR is 9.48A. The holding voltages of the proposed devices are ~2V, while those of the GGNMOS/GDPMOS are ~4V/6V. The holding voltage of the traditional SCR is ~2. The holding voltages of the proposed device with type A, type B, and type C below VDD (1.8V in the given CMOS process) is 1.66/1.38V/1.67V, which is danger from latchup event.

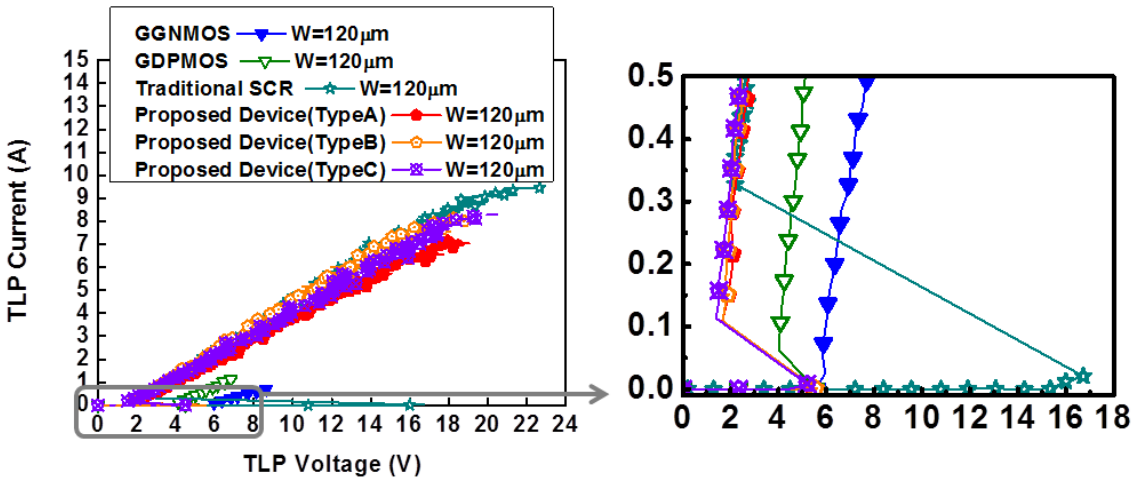


Fig.3.33. Measured TLP I-V curves of the test devices (W=120-μm).

3.3.4 DC Characteristics

The Tek370-measured I-V curves of the test devices 120-μm with width are shown in Fig. 3.34. The holding voltages of the proposed device with type A, type B, and type C are 1.29V, 1.08V and1.56V, respectively, while the GGNMOS/GDPMOS is 4.05/5.5A. The holding voltage of the traditional SCR is 1.6. The holding voltage tested by curve tracer Tek370 and TLP are below VDD (1.8V in the given CMOS process). It means the proposed has latchup danger.The holding voltages of the proposed devices under dc measurement are lower than those under TLP measurement with different pulse widths due to the self-heating effect.

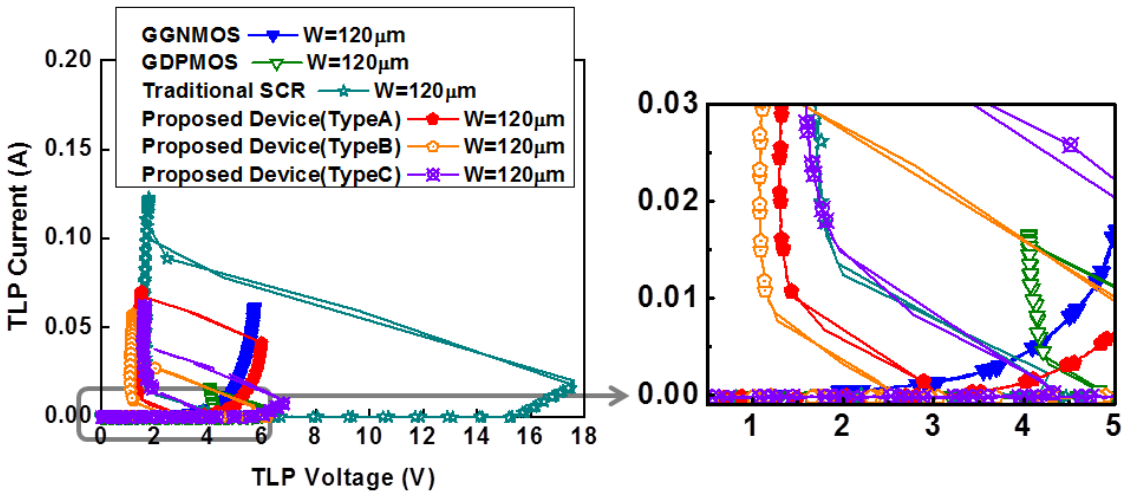


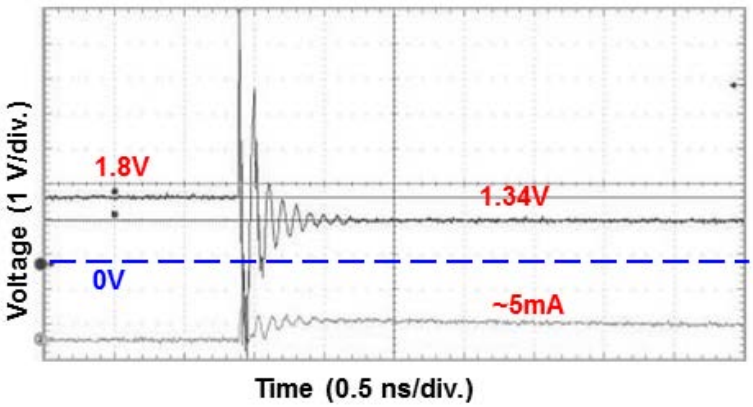
Fig.3.34. Measured Tek370 I-V curves of the test devices (W=120- μ m).

3.3.5 Transient-Induced Latchup (TLU) Test

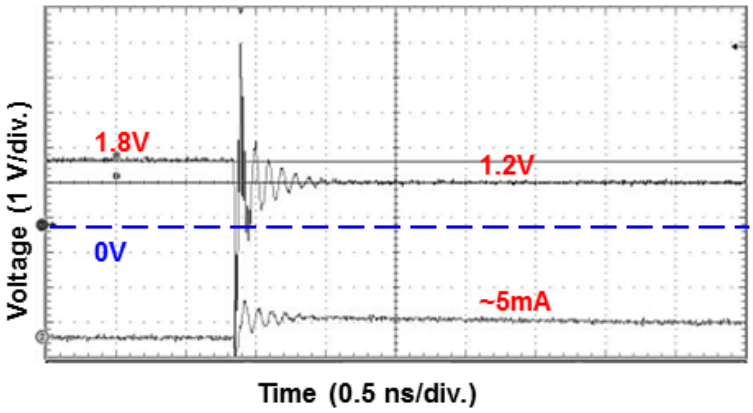
Figs. 3.35 (a) and (b) show the measured transient voltage waveforms of the proposed device under the TLU tests with charging voltage of +15V and -15V, respectively and the device latches on and the current flows constantly.. Before the TLU tests, the voltage across the proposed device was 1.8V, which is the VDD voltage in the given CMOS process.

During the TLU tests, the measured voltage waveforms are influenced simultaneously by the underdamped sinusoidal voltage.

After the TLU tests, the device is biased at 1.8 V, and the voltage waveform is clamped at 1.3 V that less than the 1.8V of VDD after the transient noise injection.



(a)



(b)

Fig.3.35. Measured voltage waveforms on proposed device (W=120 μ m) underTLU tests with charging voltage of (a) +10V and (b) -10V.

3.4 Summary

The new ESD protection device of PMOS with embedded SCR has been designed, fabricated, and characterized in a 0.18-μm CMOS process. Verified in silicon chip that all test devices with 120-μm, the proposed devices (type A, type B, and type C) have higher ESD robustness with over than 8-kV HBM level that is advantage of the traditional SCR and lower trigger voltage that is advantage of the MOS transistors. However, the holding voltages about~1.6-V of the proposed devices are lower than supply voltage 1.8-V given in CMOS process. Hence, the proposed devices can be in series with staked diode to enhance the holding voltage in future work that is discussed in section 4.2.2. All experiment data of the test devices in a 0.18-μm CMOS process are listed in Table 3.5.

Table 3.5 The measurement data of test devices in a 0.18-μm CMOS process

Device Name	**Total Width (μm)**	**Tek370B**	**TLP System**			**ESD Tester**
		V_h(V)	**V_{t1}(V)**	**V_h(V)**	**I_{t2}(A)**	**HBM(kV) step=0.5(kV)**
GDPMOS	120	5.5	~5.95	~5.95	0.68	1
GGNMOS	120	4.05	5.55	4.01	1.14	2
Proposed Device (TypeA)	120	1.29	5.41	1.66	7.14	>8
Proposed Device (TypeB)	120	1.08	5.2	1.38	8.27	>8
Proposed Device (TypeC)	120	1.56	5.54	1.67	8.17	>8
Traditional SCR	120	1.6	16.73	2.15	9.45	>8

Chapter4

Conclusions and Future works

4.1 Conclusions

Effect of additional layout pickups to the ESD robustness of GGNMOS and GDPMOS in the 28-nm high-k/metal gate CMOS process has been studied in this work. Experimental results show that inserting additional pickups has negative impact to the ESD protection level of GGNMOS and has scarcely impact to the ESD protection level of GDPMOS. Besides, layout area of GGNMOS and GDPMOS expands due to the insertion of additional pickups. Therefore, additional pickups are not suggested for ESD protection multi-finger GGNMOS and GDPMOS in 28-nm high-k/metal gate CMOS process.

The new ESD protection device of PMOS device with embedded SCR has been designed, fabricated, and characterized in a 28-nm high-k/metal gate CMOS process. Modifying from the PMOS with additional P-type ESD implantation, the proposed device combines P+/P-ESD, N-well, P-ESD, and N+ to form the embedded SCR path. Verified in silicon chip, the proposed device (type B) with 120-μm/360-μm width has 7.5-kV/ higher than 8-kV HBM ESD robustness and 90.1-fF/233.5-fF parasitic capacitance, which is much better than the GGNMOS or GDPMOS. Besides, the proposed device has been tested to be free from latchup event. Therefore, the proposed device can be a better solution for ESD protection in sub-50-nm CMOS process.

The new ESD protection device of PMOS with embedded SCR has been designed, fabricated, and characterized in a 0.18-μm CMOS process. Verified in silicon chip that all test devices with 120-μm, the proposed devices (type A, type B, and type C) have higher ESD robustness with over than 8-kV HBM level that is advantage of the traditional SCR and

lower trigger voltage that is advantage of the MOS transistors. However, the holding voltages about~1.6-V of the proposed devices are lower than supply voltage 1.8-V given in CMOS process. Hence, the proposed devices can be in series with staked diode to enhance the holding voltage in future work.

4.2 Future works

To improve the turn-on efficiency, there are two methods to reduce the trigger voltage of proposed device. Besides, adding stacked diodes into the proposed device can enhance the holding voltage to be applied in different process.

In Fig. 4.1 shows the proposed device with current trigger circuit and stacked diode string. The ESD detection circuit contains resistor, capacitor, and inverter. The RC value is designed with a time constant about ~1 μs to distinguish ESD stress events (with a rise time in nanoseconds) from normal power-on operation condition (with a rise time in milliseconds) [10]. In normal power-on operation condition, the output of the inverter is logic low because the input of the inverter can catch up with the transition (from low to high) of power-on. Thus, there is no trigger current flow into the proposed device. Under a positive ESD voltage stress on power line pin, the node that connects resistor and capacitor is logic low means the input of the inverter is logic low and the output of the inverter is logic high. Hence, the inverter send current into the base of parasitic NPN BJT in proposed device. Then, the proposed device can be much quickly to turn-on to discharge high ESD energy.

Fig. 4.2 shows the proposed device with gate couple circuit and stacked diode string. In normal power-on operation condition, the node that connects resistor and the gate of PMOS that embedded in the proposed device is logic high. Thus, the PMOS is kept off. During a positive ESD voltage stress on power line pin, the node that connects resistor and the gate of PMOS that embedded in the proposed device is logic low. Hence, the PMOS is turned on to

assist to trigger the proposed device and lower the trigger voltage of the proposed device.

There is latchup issue when the total holding voltage of the ESD protection device is lower than supply voltage. In this part, adding stacked diode can enhance the total holding voltage of the power-rail ESD clamp circuits. The sum of the clamping voltage of the proposed device and the turn-on voltage of stacked diode under ESD stress is the total holding voltage of the power-rail ESD clamp circuits. Besides, the turn-on voltage of stacked diode is dependent on the number of diode. Therefore, enhancing the total holding voltage by adjusting the number of diode makes the proposed device avoid the latchup issue, and can be widely utilized in various process that have different supply voltage.

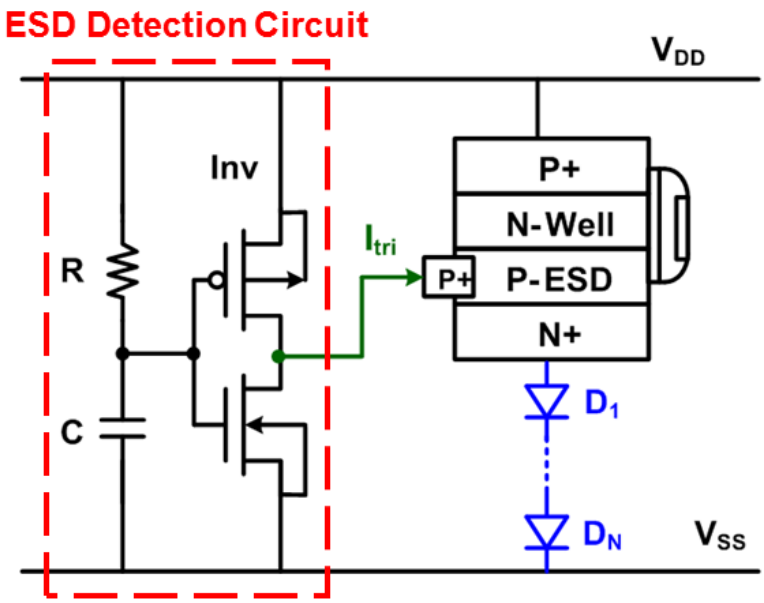


Fig.4.1. Proposed device with current trigger circuit and stacked diode string.

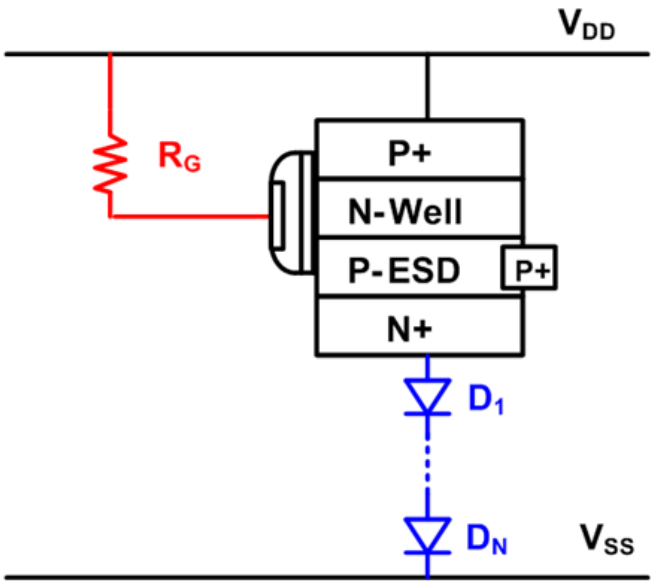


Fig.4.2. Proposed device with gate couple circuit and stacked diode string.

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Vita

姓　　名：張　品　歆

學　　歷：

國立豐原高中　(94 年 9 月~97 年 6 月)

私立逢甲大學電機工程學系　(97 年 9 月~101 年 6 月)

國立交通大學電子研究所碩士班　(101 年 9 月~103 年 11 月)

研究所修習課程：

積體電路之靜電防護設計特論	柯明道 教授
半導體物理及元件(一)	汪大暉 教授
半導體物理及元件（二）	汪大暉 教授
半導體物理及元件(一)	侯拓宏 教授
元件與電路模擬特論	蘇　彬 教授
奈米電子元件	荊鳳德 教授
奈米高頻工程	荊鳳德 教授
功率積體電路	陳柏宏 教授
固態物理	霍斯科 教授

Email：pinhsin0611@gmail.com