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碩士論文

系統層級靜電放電防護之暫態偵測電路設計

Design of On-Chip Transient Detection Circuit for System-Level ESD Protection

研 究 生：張志航　　(Chih-Hung Chang)

指導教授：柯明道 教授　(Prof. Ming-Dou Ker)

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ABSTRACT (CHINESE)

隨著半導體製程與積體電路設計的進步，混合式訊號設計之積體電路的應用越來越廣泛，功能也越來越複雜。而電晶體尺寸縮小化，氧化物層較薄和通道較窄，使得積體電路產品更易受到靜電放電 (Electrostatic Discharge, ESD) 的破壞，所以靜電放電的防護設計在微電子產品的可靠度上是一個重要的課題。

近年來，系統層級靜電放電的問題受到重視，許多微電子產品即使通過元件層級靜電放電 (Component-Level ESD) 的規範測試，仍然無法達到系統層級靜電放電 (System-Level ESD) 的防護要求。在系統層級靜電放電防護的測試條件下，靜電放電的能量快速耦合 (Coupling) 至微電子產品的電源線 (Power Line) 上，使得微電子產品功能故障、系統當機或是工作在不正常的狀態，甚至損毀。於是，在傳統的防護方法中，加入了不同的濾波器或是抗雜訊的分離元件，這樣的方法，雖提昇產品系統層級 ESD 的免疫能力，但是，卻明顯增加了微電子產品的生產成本。所以，對系統層級靜電放電防護而言，應用在半導體製程的積體電路設計防護方法可以整合於晶片系統中具有其重要性。

本論文首先於第三章提出了採用 0.15-μm 金氧半導體製程的一個系統層級靜電放電

暫態偵測電路設計，經由相關模擬以及量測證實，此暫態偵測電路能夠偵測到系統層級靜電放電在電源線上所造成的暫態電壓，並且能夠記憶此訊號且轉換出邏輯訊號。而相關量測方式包括：系統層級靜電放電測試及電性快速脈衝測試（EFT Test）。

其次，利用暫態偵測電路搭配韌體（Firmware）共同設計來提昇系統層級之靜電放電的免疫能力，將在第四章研究討論，在此利用暫態偵測電路所偵測到的訊號去停止系統的時脈（Clock），藉此避開靜電放電所產生的系統時脈毛刺 (glitch) 所導致的系統故障及當機。經由實驗量測證實，此一方法，明顯提昇系統層級之靜電放電的免疫能力。

最後，這份論文總共分成五個章節。第一章是有關於系統層級靜電放電防護國際法規的內容；第二章介紹了傳統用來解決系統層級靜電放電防護的方法；第三章則是暫態偵測電路的設計以及相關模擬及實驗量測結果；第四章提出了硬體及韌體共同設計的方法，用來提昇系統層級之靜電放電的免疫能力；第五章為此份論文的結論和未來展望。

Design of On-Chip Transient Detection Circuit for System-Level ESD Protection

Student: Chih-Hang Chang **Advisor: Prof. Ming-Dou Ker**

Degree Program of Electrical and Computer Engineering

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ABSTRACT (ENGLISH)

As the improvement of semiconductor process and technology, the mixed-signal integrated circuits have been widely used in industrial electronic products. As the transistor size continues to shrink, the thinner oxide and shallower junction depth in advance technology, microelectronic products are more susceptible to ESD damage. Therefore, ESD protection has become an important reliability issue in CMOS ICs.

Recently, system-level ESD is an increasingly important reliability issue in CMOS IC products. It has been also reported that reliability issues still exist in CMOS ICs under system-level ESD tests, even though they have passed component-level ESD specifications. In the system-level ESD testing, ESD-induced energy is coupled to the power and ground lines of microelectronic products, which can cause microelectronic system into locked state, frozen state, or even hardware damage. Thus, in traditional solutions, extra discrete components are often added on printed circuit board (PCB) to suppress system-level ESD events in microelectronic products. However, those discrete components are substantially increasing the cost of microelectronic products. Therefore, the chip-level solutions to meet

high system-level ESD specification for microelectronic products are strongly requested by IC industry.

In chapter 3, a transient detection circuit has been investigated to detect the fast electrical transients on the power line (V_{DD}) and ground line (V_{SS}) under system-level ESD tests. The proposed on-chip transient detection circuit has been fabricated in a 0.15-μm CMOS process with 3.3-V devices. The circuit performance has been evaluated by system-level ESD tests. It has been confirmed that the transient detection circuit can detect and memorize the occurrence of the positive and negative fast electrical transients on the power and ground lines of CMOS ICs.

Second, the transient detection circuit with hardware/firmware co-design has been investigated in chapter 4. Due to the generation of glitches from system clock under system-level ESD or EFT test, therefore, a method of using transient detection circuit to stop system clock is proposed, it can avoid these glitches to cause the malfunction and frozen of the microelectronic system. Anyway, according to the experimental results, it has been improved the system-level ESD tests immunity.

This thesis is divided into five parts. In chapter 1, international standards about system-level ESD are generally guided. In chapter 2, some traditional solutions to overcome system-level ESD events are collected and introduced. In chapter 3, a novel on-chip transient detection circuit is proposed. In chapter 4, the transient detection circuit with hardware/firmware co-design has been simulated in detail and circuit performance has been verified under system-level ESD tests. The last chapter includes conclusions and future works.

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Chapter 1

Introduction

1.1. Motivation

Electrostatic discharge (ESD) is an important part of integrated circuits (ICs) design for many years, as the semiconductor technology level continue to increase, and process geometries continue to shrink, more complicated functions are integrated into single chip to decrease the cost of microelectronic products. Due to thinner oxide and shallower junction depth in advanced technology, microelectronic products equipped with CMOS ICs are more susceptible to electrostatic discharge damage. Therefore, ESD protection has become an important reliability design in CMOS ICs products. In order to verify the robustness of the ESD productions against the ESD-induced energy, many international standards have been established. Generally, component-level ESD and system-level ESD are two kinds of specifications to verify the ESD robustness of the CMOS ICs products. The major difference between component-level ESD and system-level ESD specifications is that whether the equipment under test (EUT) with or without power supply. Component-level ESD tests are used to simulate the well-controlled environment, such as factory environment. To characterize component-level ESD susceptibility of CMOS ICs, the test method should follow three ESD test standards: human-body-model (HBM), machine-model (MM), charge-device-model (CDM) [1]-[3].

Recently, in many companies, the product features have met customer requirements, but the system-level ESD tests are far lower than customer expectation. Therefore, it is an increasingly important reliability issue in microelectronic products [4], [5]. Under

system-level ESD test, the ESD-generated transient electrical voltage with quite large amplitude and fast period can randomly exist on power line (V_{DD}), ground line (V_{SS}), and input/output (I/O) pins. This energy may cause malfunction or hardware destructions, such as logic data losing or the chip burning out. In order to ensure the yield of the microelectronic products, several electromagnetic compatibility (EMC) regulations are defined. The microelectronic products are required to evaluate system performances under test standard of system-level ESD test. In the system-level ESD test standard of IEC 61000-4-2 [6], the microelectronic products are required to sustain the ESD-generated voltage of ±8kV (±15kV) under contact-discharge (air-discharge) test mode to achieve the immunity requirement of "level 4". Unfortunately, it has been reported that even though some COMS IC products have passed component-level ESD specifications, they are still susceptible to system-level ESD stresses. The experimental results have confirmed the power and ground lines of microelectronic products no longer maintain the normal operating voltage under system-level ESD tests, but underdamped sinusoidal waveforms with an amplitude of several tens to hundreds of volts and period of several tens of nanoseconds instead [4]. From previous studies, it has been reported the super twisted nematic (STN) liquid crystal display (LCD) panel keeps in locked state and shows error display after system-level ESD tests [7].

In traditional solutions, extra discrete components are added to suppress system-level ESD events in microelectronic products [8]. Those discrete components including ferrite bead, magnetic core and transient voltage suppressor (TVS) are used to decouple, absorb or bypass the electrical transients generating from system-level ESD zapping, but using discrete components, the total cost of microelectronic products will increase substantially. Additionally, the requirement of ESD level is often depended on customer-defined specifications and ESD protection designs need to be different for various product applications. It is more challenging to achieve ESD level high enough than before. Therefore,

system-level ESD protection design plays an important role in many kinds of CMOS IC products. As a result, the chip-level solutions to meet high system-level ESD specification for microelectronic products are strongly requested by IC industry.

1.2. Introduction of International Standard

ESD is an important reliability issue on CMOS IC products, especially in the advanced technology. Many international associations, such as ESDA (Electrostatic Discharge Association), AEC (Automotive Electronics Council), EIA (Electronic Industries Alliance), JEDEC (Joint Electron Device Engineering Council), and MIL-STD (US Military Standard), etc, have drawn up the different ESD standards for all kinds of ESD conditions. All of the international standards described above are component-level ESD standards. The component-level ESD standards defined the test environment, test methods, and the corresponding ESD test level. In order to verify the robustness of CMOS ICs under system-level ESD events, many international companies adopt other specifications, such as IEC 61000-4-2 (system-level ESD events) and IEC 61000-4-4 (EFT events). IEC 61000-4 is a part of the IEC 61000 series, and the mainly contents of part 4 are about testing and measurement techniques. In this section, the international standards are described below.

1.2.1. IEC 61000-4-2 Specification

The object of the standard, IEC 61000-4-2 is to establish a common and reproducible basis for evaluating the performance of CMOS ICs inside the electrical/electronic microelectronic products. This standard specifies typical waveform of the discharge current, test levels, test equipment, test set-up, and test procedure. In order to verify the disturbance of CMOS ICs under system-level ESD tests, the ESD gun is used to zap the ESD-induced energy to the EUT. Fig. 1.1 (a) shows the equivalent circuit of ESD gun. The energy storage

capacitor, the discharge resistor, and the discharge switch shall be placed as close as possible to the discharge electrode. Moreover, the equivalent circuit of the human body model is shown in Fig. 1.1 (b). Comparing with the two equivalent circuits, the storage capacitor in Fig. 1.1 (a) is 150pF, and that in Fig. 1.1 (b) is 100pF. That means, the ESD-induced energy stored in the system-level ESD condition is larger than that in the component-level ESD condition. The discharge resistors used in the Fig. 1.1 (a) and (b) are 330Ω and 1.5kΩ, respectively. Therefore, the ESD-induced energy generating from ESD gun in system-level ESD test has faster rise time than that in component-level ESD test. Fig. 1.2 shows the typical waveform of the discharge current under system-level ESD test (IEC 61000-4-2) and component-level ESD test (MIL-STD 883). Under 8-kV ESD zapping condition, the peak current in system-level ESD test is about five times larger than that in component-level ESD test. In order to compare the test results obtained from different ESD generators, the characteristics of the waveform of discharge current are listed in table 1.1. Table 1.2 shows the test level (test voltage) of component-level ESD test, such as HBM, MM and CDM. The system-level ESD test levels with contact discharge and air discharge test modes are shown in Table 1.3. Contact discharge is the preferred test method and air discharge shall be used when contact discharge cannot be applied. It is important to note that the severity of each test level is not equivalent between the two methods. The discharge electrodes of two test modes are shown in Fig. 1.3.

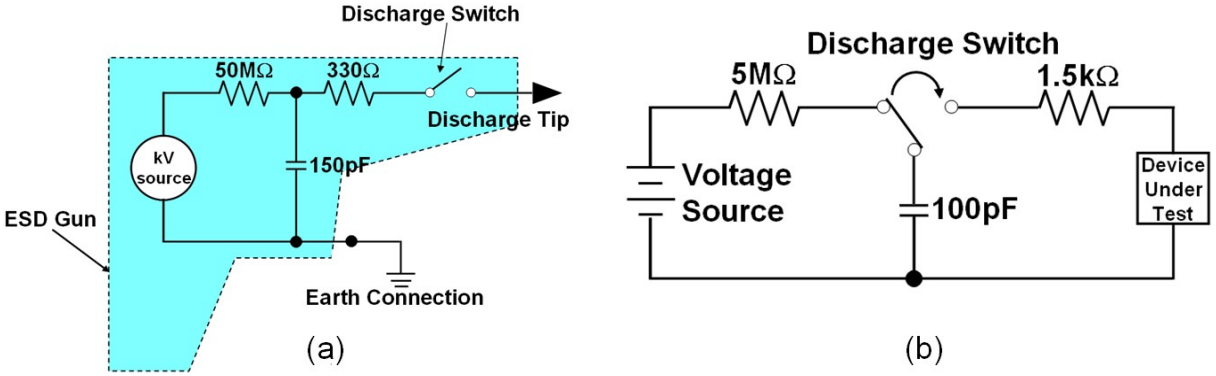


Fig. 1.1 The equivalent circuits of (a) ESD gun which is used to zap the ESD-induced energy under system-level ESD test and of (b) human body model under component-level ESD test.

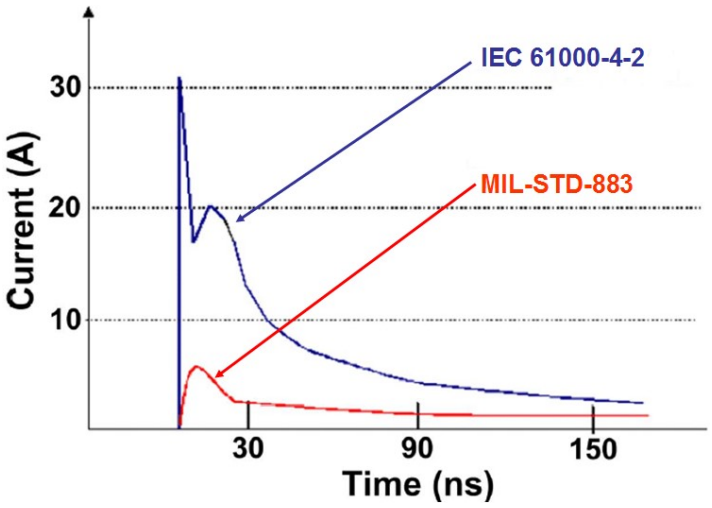


Fig. 1.2 Under 8-kV ESD zapping, the peak current in system-level ESD test is about five times larger than that in component-level ESD test.

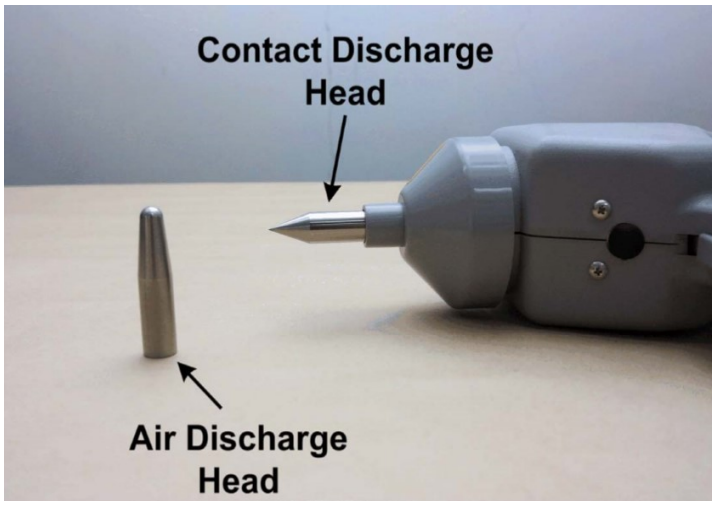


Fig. 1.3 Discharge electrodes of ESD gun which is used under system-level ESD test with contact discharge mode and air discharge mode.

Table 1.1 Waveform parameters of discharge current.

Level	Indicated Voltage (kV)	First Peak current ±10% (A)	Rise Time (ns)	Current (±30%) at 30ns (A)	Current (±30%) at 60ns (A)
1	2	7.5	0.7 to 1	4	2
2	4	15	0.7 to 1	8	4
3	6	22.5	0.7 to 1	12	6
4	8	30	0.7 to 1	16	8

Table 1.2 Component-level ESD specifications.

Model Name	Test Voltage
Human Body Model	>2000V
Machine Model	>200V
Charge Device Model	>1000V

Table 1.3 System-level EMC/ESD specifications - test levels.

Contact Discharge		Air Discharge	
Level	Test Voltage	Level	Test Voltage
1	±2kV	1	±2kV
2	±4kV	2	±4kV
3	±6kV	3	±8kV
4	±8kV	4	±15kV
X	Specified by Customer	X	Specified by Customer

To compare Table 1.2 with Table 1.3, the test voltage of system-level ESD is larger than component-level ESD, no matter with contact discharge or air discharge. Noteworthiness, the voltage waveforms are different for each method due to the different test methods of test. According to these phenomena, system-level ESD tests affect the system operation of the microelectronic products more seriously than component-level ESD tests. Table 1.4 shows the evaluation of system-level ESD test results, the test results shall be classified in terms of hardware damage, loss function or degradation of performance of the EUT. Generally speaking, the microelectronic product should reset itself automatically after system-level ESD test to pass the “class B” specification at least. The EUT shall be operated within the specified climatic conditions to avoid unnecessary influence from electromagnetic environment of the laboratory. The measurement setup of system-level ESD test is shown in Fig. 1.4 and the elaboration of this setup will be followed in chapter 3.

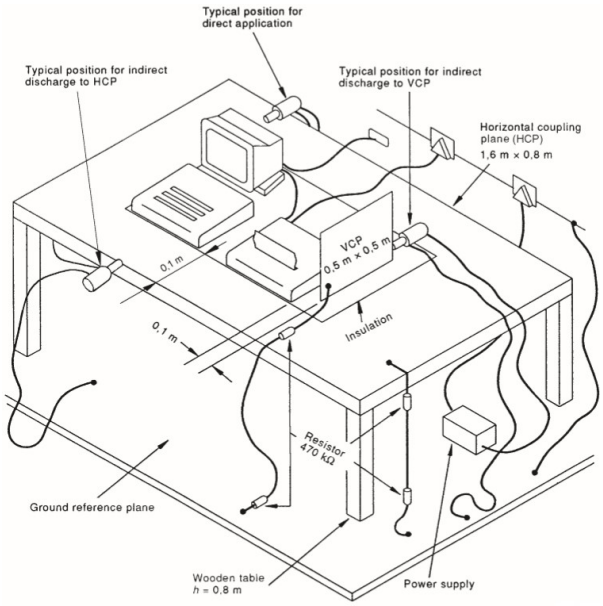


Fig. 1.4 Measurement instruments of system-level ESD test.

Table 1.4 Recommended classifications of system-level ESD test results.

Criterion	Classification
Class A	Normal performance within limits specified by the manufacturer, requestor or purchaser.
Class B	Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention. **(Automatic Recovery)**
Class C	Temporary loss of function or degradation of performance, the correction of which requires operator intervention. **(Manual Recovery)**
Class D	Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.

1.2.2. IEC 61000-4-4 Specification

IEC 61000-4-4 is an international standard which gives immunity requirements and test procedures related to electrical fast transients (EFT) [9]. EFT disturbances commonly exist in industrial environment where electromechanical switches are used to connect and disconnect. The EFT test intends to demonstrate the immunity of electronic equipments against transient disturbances originating from switching transients, such as interruption of inductive load,

relay constant bounce, etc.

According to the standard of IEC 610004-4, the equivalent circuit diagram of EFT generator is shown in Fig. 1.5 and the major elements are listed in Table 1.5. In particular, the impedance matching resistor R_m (50Ω) and the DC blocking capacitor C_d (10nF) are defined in the standard. The charging capacitor C_c is used to store the charging energy and R_c is the charging resistor. The R_s is used to shape the pulse duration. The effective output impedance of the generator is 50Ω.

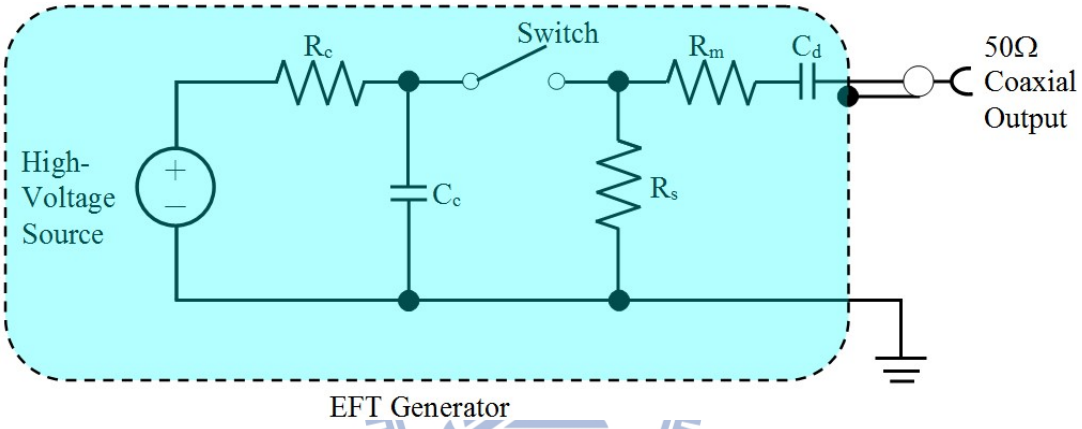


Fig. 1.5 The equivalent circuit of EFT generator.

Table 1.5 Characteristics of the EFT generator.

Parameter	Definition
R_c	Charge Resistor
C_c	Energy Storage Capacitor
R_s	Impulse Duration Shaping Resistor
R_m	Impedance Matching Resistor (= 50Ω)
C_d	DC Blocking Capacitor (=10nF)

During EFT tests, the power lines of the CMOS ICs inside the microelectronic products no longer maintain their initial voltage levels. A number of fast transients would couple into power, ground, and I/O pins randomly causing the ICs inside the EUT to be upset or frozen after EFT zapping. The characteristics of such a high-voltage-level EFT-induced disturbance

are listed in Table 1.6 and shown in Fig.1.6 [9]. The test voltage waveforms of these fast transients with the repetition frequency of 5kHz and 100kHz. The use of 5kHz repetition rate (repetition period of 0.2ms) is the traditional EFT test and 100kHz (repetition period of 10us) is closer to reality. For EFT pulse with the repetition frequency of 5kHz, there are totally seventy-five pulses in each burst string and the burst duration time is 15ms, and the period between two adjacent bursts is 300ms. Similarly, for EFT pulse with the repetition frequency of 100kHz, there are seventy-five pulses in each burst string and the burst duration time is only 0.75ms. The rise time and duration of a single pulse voltage waveform must accord with the characteristics which are listed in Table 1.7 and shown in Fig. 1.7. A voltage pulse waveform with rise time of 5ns±30% and duration of 50ns±30% occurs on the test pins of EUT under EFT tests. The EFT test levels for testing power supply ports and testing I/O, data and control ports of the EUT are list in Table 1.8. The voltage peak for I/O, data and control port is half of the voltage peak for testing power supply port. Level "X" is an open level, which is specified in the dedicated equipment specification.

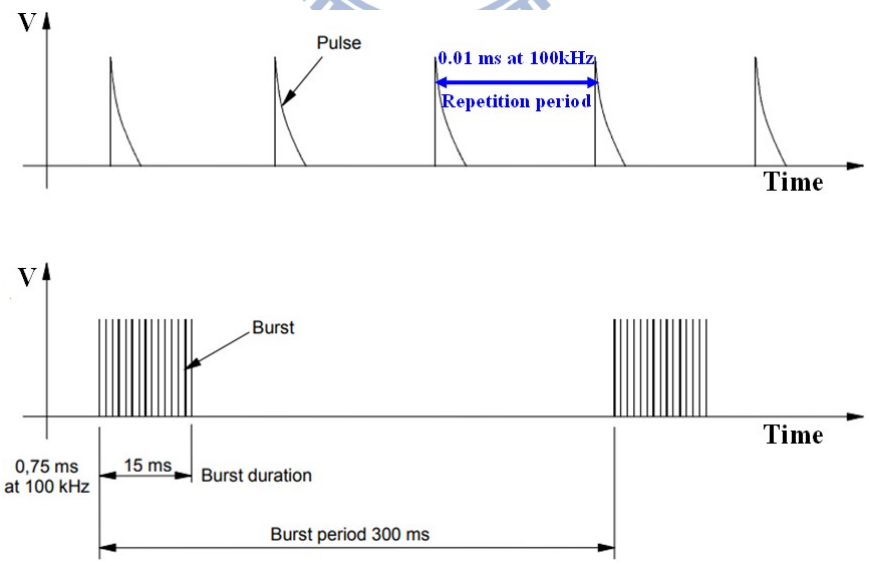


Fig. 1.6 General graph of fast transient/burst.

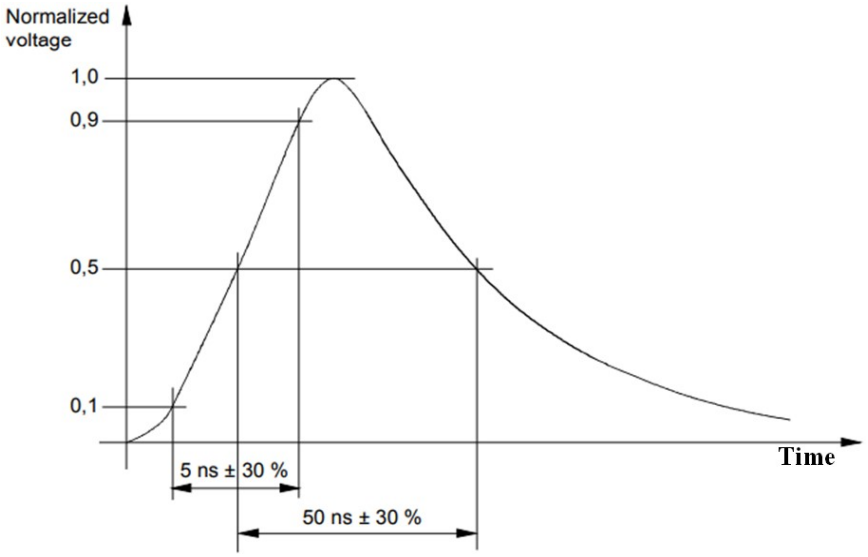


Fig. 1.7 Voltage waveform of a single pulse in each burst.

Table 1.6 Characteristics of the fast transient/burst

Repetition Rate (kHz)	Repetition Period (ms)	Pulse Number	Burst Duration (ms)	Burst Period (ms)
5	0.2	75	15	300
100	0.01	75	0.75	300

Table 1.7 Characteristics of a single pulse in each burst.

Parameter	Value
Frequency	5 kHz or 100 kHz
Rise Time	5ns ± 30%
Duration	50ns ± 30%

Table 1.8 Specifications - test levels.

Level	On power and PE (protective Earth) ports		On I/O (Input/Output) Signal, Data and Control ports	
	Voltage Peak (kV)	Repetition Rate (kHz)	Voltage Peak (kV)	Repetition Rate (kV)
1	0.5	5 or 100	0.25	5 or 100
2	1	5 or 100	0.5	5 or 100
3	2	5 or 100	1	5 or 100
4	4	5 or 100	2	5 or 100
X	Specified by Customer	Specified by Customer	Specified by Customer	Specified by Customer

1.3. Thesis Overview

From the previous introduction, how to solve the system-level ESD events has become an important issue for the microelectronic products. The target of this thesis is to find a chip-level solution towards system-level ESD problems. Therefore, this thesis would be divided into five chapters.

In chapter 2, some traditional techniques to solve system-level ESD events are introduced. In chapter 3, a novel on-chip transient detection circuit for detecting system-level ESD and EFT protection is proposed. In chapter 4, a hardware / firmware co-design method is proposed which can avoid system-level ESD. Finally, in chapter 5, the conclusions and future works of this thesis are given.

Chapter 2

Solutions to Overcome System-Level Electrical Transient Disturbance

2.1. Background

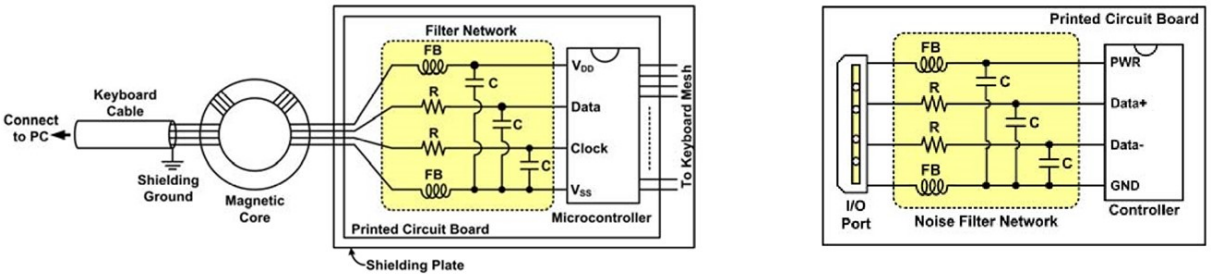
ESD is a serious reliability event that causes electrical overstress (EOS) on microelectronic products. For a long time, terminal products endlessly encounter customer return due to EOS. Besides ESD protection design and ESD verification of microelectronic products, manufacturers need to focus more on ESD reliability of CMOS ICs. If CMOS ICs are weak against ESD, the products cannot have good ESD reliability. For component-level ESD protection, some simple methods are used to protect CMOS ICs against ESD events, such as diode and grounded-gate NMOS (GGNMOS), In addition, to provide strong protection against transient disturbance, other protection methods and new structure device have been proposed and investigated to enhance immunity against large impulse current. Although component-level ESD has been enhanced and passed the specification (e.g., HBM 8kV), but in system-level ESD is still not meet specification. Therefore, system-level ESD protection plays an important role in many kinds of CMOS IC products. As shown in Fig. 1.2, the peak current in system-level ESD test is about five times larger than that in component-level ESD test under 8-kV ESD zapping condition. For this reason, the system-level ESD protection methods are different from component-level ESD protection methods.

Recently, IC designers gradually pay more attentions to the system-level ESD events. More and more test methods have been published to investigate the system-level ESD events.

It would provide IC designers with an appropriate way for obtaining more analysis methods on the transient disturbance protection. For traditional solution for microelectronic products against system-level ESD tests, the basic concept is to use these filters to bypass or absorb the large transient disturbance. Since for the advanced technology, system-on-a-chip (SOC) has become a trend to provide multi-function integration and save cost, how to avoid system-level ESD stresses causing SOC system locked in frozen state would become an important design topic.

2.2. Traditional System Design Solutions

In order to improve the immunity of microelectronic products to achieve the strict ESD specifications, system designers can take many approaches to prevent ESD damage. One of the system design solution against system-level ESD events is to add some discrete noise-decoupling components or board-level noise filters on the printed circuit board (PCB), these examples are shown in Fig. 2.1(a) and (b). [8], [10]



(a) (b)

Fig. 2.1 The system solution to overcome the system-level ESD issue by adding extra discrete components to absorb or bypass the electrical fast transients (a) in keyboard and (b) in USB I/O port.

These discrete components are used to decouple, bypass or absorb the transient noise generated form system-level ESD events. Therefore, the discrete components can reduce the

transient energy of transient disturbance coupled on power line of CMOS ICs. Moreover, adding some noise-decoupling components can even clamp the transient voltage at low level to avoid ESD damage on internal circuits of CMOS ICs. Some discrete noise-bypassing components for system-level ESD protection, such as transient voltage suppressor (TVS), or low-pass noise filters, they have been reported and would discuss in the following sections [11].

2.2.1 Transient Voltage Suppressor (TVS)

TVS is commonly used to improve the system-level ESD immunity of microelectronic products. It can provide ESD discharge path under system-level ESD tests. Usually, TVS is located near the power pins and the I/O pins of CMOS ICs to provide system-level ESD protection in the PCB. The main function of TVS is to absorb high peak as a surge device under ESD tests. It is an open circuit during normal circuit operation and a short to ground during ESD events. The peak pulse power of TVS can be estimated by

$$P_{peak} = I_{pp} \times V_{clamp} \tag{1}$$

Where I_{pp} is the maximum lightning current that TVS can bypass, and V_{clamp} is the voltage when I_{pp} is applied across the device. Device with lower clamping voltage during ESD stress conditions can sustain higher ESD level. Although TVS can be an ESD protector, its immunity performance is not well enough compared to other discrete components. Moreover, TVS often has high capacitive loading, which can cause distortion on high data rate signals. As a result, TVS is not suitable for high speed applications.

For ESD protections, there are many types of TVS components, such as varistor, metal oxide varitors (MOVs), and zener diode, etcs. Varistors are made of ceramic materials. Compared with TVS components, MOVs have lower capacitance. However, for high speed

interface applications, the capacitance of MOVs is still not low enough to cause signal distortion. Moreover, MOVs has high impedance with low clamping voltage. When the voltage across this device is high, the resistance value would drop to a low level. The voltage drop across the varistor will dramatically increase as the current increases. As a result, if the ESD clamping voltage is too high, varistor is difficult to protect electronic products.

2.2.2 Low-Pass Noise Filter

To meet the strict system-level ESD specification, different types of board-level noise filters have been investigated to improve the immunity of CMOS ICs inside the microelectronic products under system-level ESD tests [12]. Adding board-level noise filter between noise trigger source and CMOS ICs can absorb, bypass, or decoupling ESD-generated energy to avoid ESD damage on EUT. Several types of board-level noise filters, such as capacitor filter, LC-like filter (2^{nd}-oredr), and π-section filter (3^{rd}-order), as shown in Fig. 2.2, have been investigated and confirmed the enhancement of system-level ESD immunity. For evaluating the system-level ESD test of DUT, these three different types of filters are investigated. Among different noise filter network, the higher-order noise filters have better performance to enhance the system-level ESD test of DUT, and thus better immunity against system-level ESD events. Experimental data is shown Fig.2.3 [12].

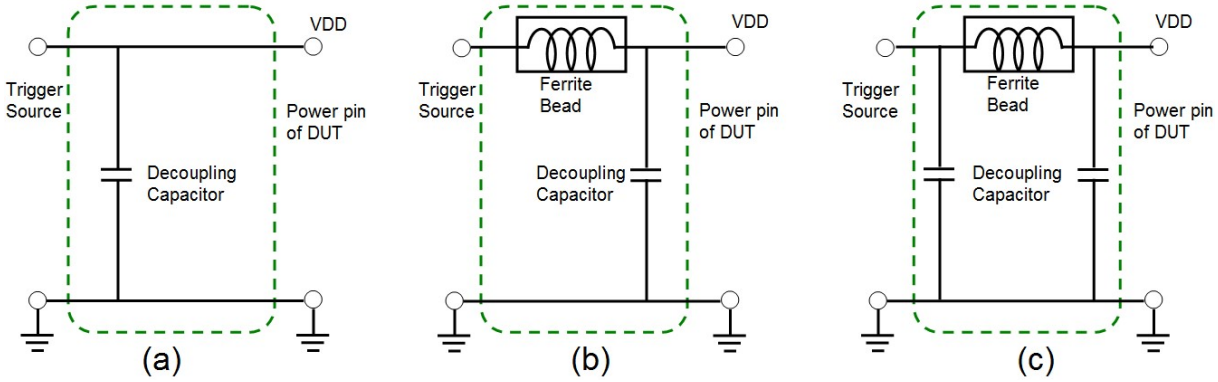


Fig. 2.2 Board-level noise filter of (a) capacitor filter, (b) LC-like filter, and (c) π-section filter.

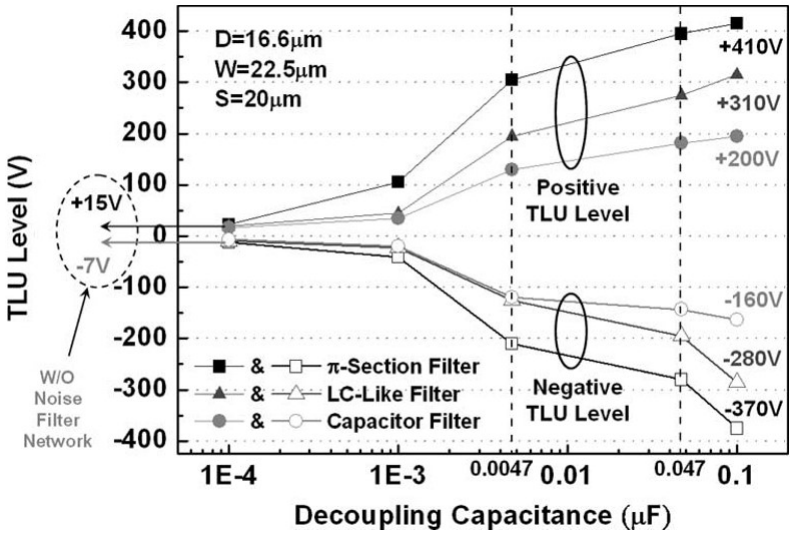


Fig. 2.3 Relations between the decoupling capacitance and the TLU level of the DUT under three types of noise filter networks: capacitor filter, LC-like filter, and π-section filter [12].

2.2.3 Design Concept of Printed Circuit Board (PCB)

While discrete ESD components are used to suppress the effect of system-level ESD events, PCB design is another important topic on ESD protection design. A simple diagram was shown in Fig. 2.1. To design the printed circuit board against system-level ESD events, few concepts needs to be taken into account. First, the induced magnetic current into circuit loop will be proportional to the size of the loop [11]. Therefore, minimizing the loop size on the PCB is a critical design for ESD reliability enhancement. Second, place the circuit devices on the PCB as close as possible to minimize the lengths of signal and power lines. It can avoid receiving too much energy generating from system-level ESD events.

2.2.4 External Hardware Timer

Another method which is completely different from the previous solutions is to regularly check the system abnormal conditions by using an external hardware timer, such as watch dog

timer. This timer is a computer hardware timing device to reset the operation system when the main program is locked or frozen due to some fault conditions. Moreover, this hardware timer is often designed with registers or flip flops. However, During system-level ESD or EFT tests, the logic states stored in the registers or flip flops of hardware timer would sometimes also be destroyed, still causing malfunction or frozen condition in the system operation. Therefore, this kind of timer is not a stable way to protect microelectronic products against system-level ESD events.

2.3. Hardware/Firmware Co-Design

The above solutions try to solve system-level ESD events by off-chip designs, which would occupy additional chip area. It has been reported that the ESD protection device required more IC area to achieve 2 kV HBM ESD protection when the gate oxide thickness shrinks, as shown in Fig 2.4 [13].

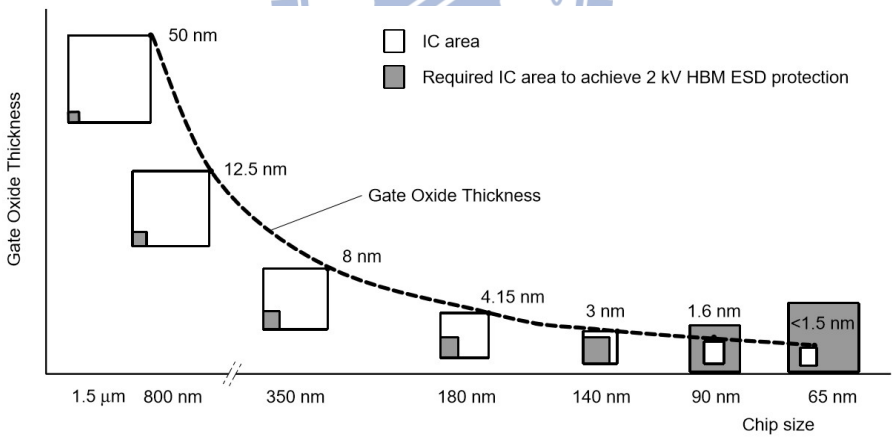


Fig. 2.4 Required IC area for ESD protection as a function of chip size [13].

Moreover, in order to provide strong ESD protection against transient disturbance, some of the methods associated with hardware/firmware co-design will be introduced in the next sub-section.

2.3.1. Using Low Voltage Detector (LVD) Detects ESD Events

This method uses a low voltage detector (LVD) to detect the system-level ESD or EFT events. A simple LVD system diagram is shown Fig. 2.5. The output (V_{OUT}) of LVD provides a signal for firmware check when the power (VDD) is below the reference voltage (VREF) during system-level ESD or EFT tests. As the same time, the firmware will execute recovery operation to restore the microelectronic system to a desired steady state as soon as possible. Such an approach, it seems effective to enhance the system-level ESD or EFT immunity, unfortunately, VREF is also susceptible to the ESD-induced transient disturbance. Therefore, this method sometimes does not detect ESD event, which is not a stable way to enhance microelectronic products under system-level ESD or EFT tests.

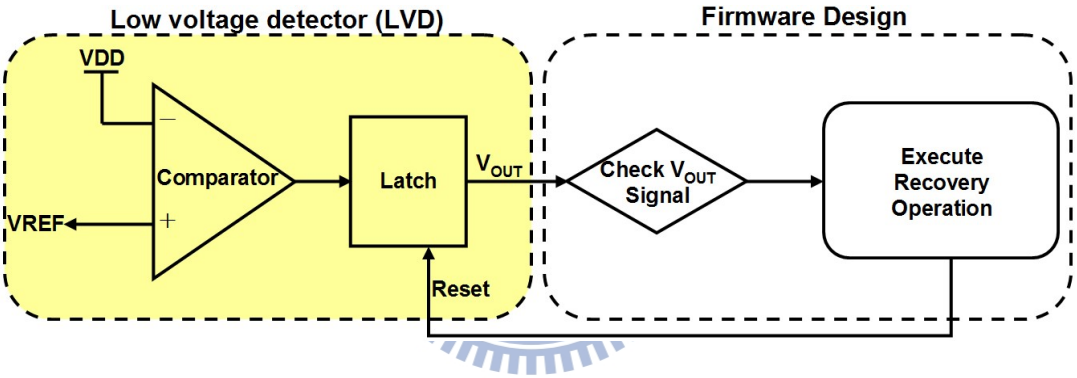


Fig. 2.5 A simple LVD system is used to detect system-level ESD events.

2.3.2. Using Transient Detection Circuit Detects ESD Events

Another method, as the hardware/firmware co-design case shown in Fig. 2.6 [15], the detection results (V_{OUT}) from the on-chip transient detection circuit can be temporarily stored as a system recovery index for firmware check. The transient detection circuit is designed to detect and memorize the occurrence of system-level ESD events. For example, the output (V_{OUT}) state in the on-chip transient detection circuit and the firmware index are initially set to “high” state. When the fast electrical transient happens, the on-chip transient detection circuit can detect the fast electrical transient and then change the output (V_{OUT}) state from

"high" state to "low" state. The system recovery index is changed to "low" state, which will be checked by the firmware to automatically recover all system functions to a stable state as soon as possible. After the recovery procedure, the output state of the on-chip transient detection circuit and the firmware index are re-set to "high" state again for detecting the next electrical transient disturbance events. Moreover, it had been proven that the hardware/firmware co-design can effectively improve the robustness of the industrial products against electrical transient disturbance [8].

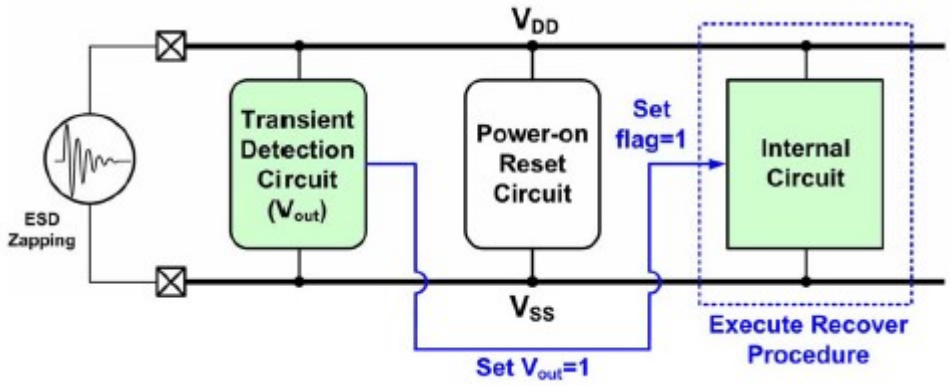


Fig. 2.6 Hardware/firmware co-design for system recovery by using the detection results of the on-chip transient detection circuit [15].

For display system protection design with thin-film transistor (TFT) liquid crystal display (LCD) panel, multiple power systems are needed for electrical display functions, as shown in Fig. 2.7 [14]. For example, in the backside of source driver IC, the analog power line (VDDA) is used for digital-to-analog converter circuit and digital power line (VDDD) is used for shifter register to store display signals. The transient detection circuit, designer for detecting and memorizing the occurrence of ESD-induced transient disturbance, can connect with VDDD power line to implement the hardware/firmware protection design in display system. The detection results from the detection circuit can be temporarily stored as a system

recovery index for firmware check. In the beginning, the output (V_{OUT}) state of the detection circuit is initially reset to “high” state. When the electrical transients happen, the detection circuit can detect the occurrence of system-level ESD-induced transient disturbance and transit the output (V_{OUT}) to “low” state. At this moment, the firmware index is also changed to “low” state to initiate automatic recovery operation to restore the microelectronic display system to a desired stable state as soon as possible. After the automatic recovery operation, the output of the detection circuit and the system recovery index are reset to “high” state again for detecting the next ESD-induced electrical transient disturbance events.

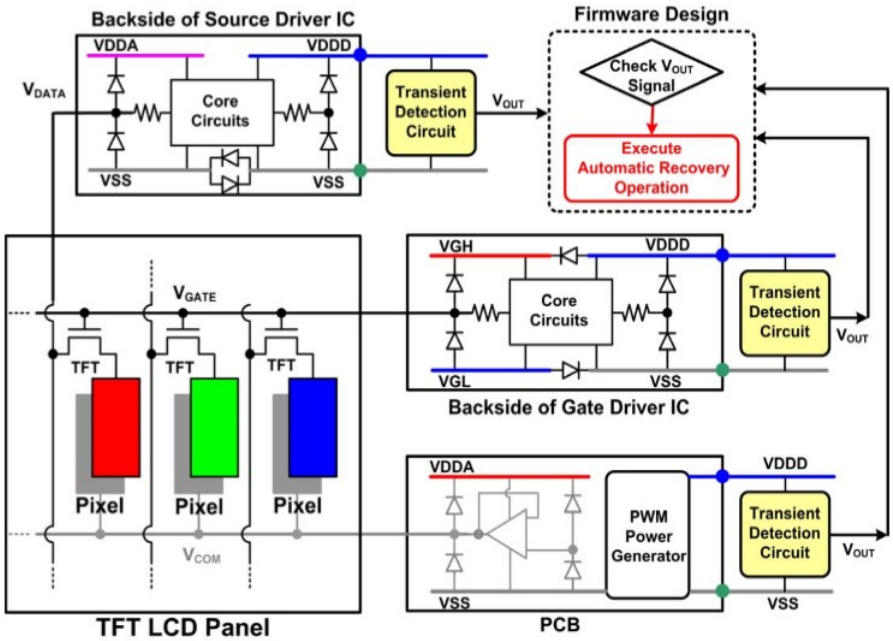


Fig. 2.7 Hardware/firmware system co-design with transient detection circuit in display panel product [14].

2.4. Summary

System-level ESD protection has become more and more important for IC industry. Several methods have been discussed and analyzed in this chapter. TVS can provide ESD energy discharge path under system-level ESD or EFT tests, but its drawback is nonlinear resistance characteristic. Board-level noise filter on PCB is another method to enhance

system-level immunity, but the occupied area should be taken into account as well. Above all, traditional solutions toward system-level ESD immunity have some limitation, either in the aspect of occupied area or cost. Moreover, hardware/firmware co-design with transient detection circuit can improve the system-level ESD immunity, which has been reported [8], [14]. On-chip detection circuit can be used to save PCB and provide detection signal for firmware to execute the automatic system recovery procedures. Based on these requests, the on-chip solutions will be developed in advance and to be the trend for future solution for system-level ESD events.

Chapter 3

Design of On-Chip Transient Detection Circuit

3.1. Background

System-level ESD have been investigated during the system-level ESD events, the power line and ground line of the microelectronic products would be disturbed with high-energy ESD-induced transient noise. Such high ESD-induced noise on the power line and ground line can lead to data loss, malfunction, or hardware damage of microelectronic products. According to the IEC 61000-4-2 standard, microelectronic products are recommended to pass "class" B at least. That means, the system should be designed with automatic detection function to detect the fast transients, it can automatically reset itself and restore to stable state after ESD zapping. In recent years, on-chip transient detection circuit has proposed to co-operate with hardware/firmware system to achieve the system auto recovery procedures. Moreover, from the published experimental results, it has been confirmed that chip-level co-design can successfully improve system-level ESD immunity.

3.2. Prior Art

Four transient detection circuits for system-level ESD protections have been proposed [8], [15]-[17]. The circuit diagram of the first on-chip transient detection circuit is shown in fig. 3.1 (a). There are two latch logic gates used as the ESD sensor unit to detect the system-level ESD events on the power and ground lines. Coupling capacitors can be added between the input/output nodes of latch and V_{DD}/V_{SS} lines in order to enhance the sensitivity of the ESD sensor to fast transients on the V_{DD}/V_{SS} line. It has been analyzed that the NMOS

in the inverters of sensor_1 in fig. 3.1 (a) is designed with a larger W/L ratio than that of the PMOS to make the latch locking at logic “0”, easily. The PMOS in the inverters of sensor_2 is designed with a larger W/L ration than that of the NMOS to make the latch easily locking at logic “1” [8].

The second transient detection circuit is designed with latch logic gates and capacitors shown in fig. 3.1 (b). In this transient detection circuit, the capacitors C_{P1} ($C_{P2)}$ is used to detect the positive (negative) fast electrical transients. A latch circuit composed of two inverters is used to memorize the logic state after the system-level ESD tests. It has been confirmed that the W/L ratio of inverters in the latch and the coupling capacitance will strongly influence the sensitivity of this detection circuit. Before the system-level ESD tests, the NMOS (M_{nr}) can provide a reset function to pull down node A and then the output of the detection circuit (V_{OUT}) can be set logic to “0”. During the system-level ESD tests, when the voltage of V_{DD} is below the voltage of V_{SS}, the parasitic diode of PMOS such as M_{p1} and M_{p2} would be turned on. Therefore, this circuit can detect the positive system-level ESD events. Similarly, the parasitic diodes of NMOS such as M_{n1} and M_{n2} would be turned on under the negative system-level ESD stress.

The third one is designed with RC-based circuit structure to realize the transient detection circuit, as shown in Fig. 3.1 (c). The two inverter latch is used to memorize the logic state before and after the system-level ESD events. The NMOS (M_{nr}) provides the reset function to set the output (V_{OUT}) logic state to be initially low. Under system-level ESD stress, due to RC time constant delay, the PMOS device of INV_1 would be turned on by the overshooting ESD voltage, and then M_{n1} can pull down the output voltage level and thus change the output logic state from logic “0” to logic “1”. Therefore, the third proposed transient detection can successfully detect and memorize the occurrence of system-level ESD events.

The last one uses RC-based circuit structure without latch circuit to implement the detection function, as shown in Fig. 3.1(d). The PMOS device (M_{p1}) helps to memorize the logic state before and after the system-level ESD stress. The NMOS device (M_{nr}) provides the reset function to set the initial output (V_{OUT}) logic state to be initially low. During the fast electrical transient disturbance, RC-time constant delay would urge PMOS device (M_{p1}) to turn on by overshooting ESD voltage, and then the output logic state would transfer from logic "0" to logic "1". Therefore, this transient detection circuit can detect and memorize the occurrence of system-level ESD events.

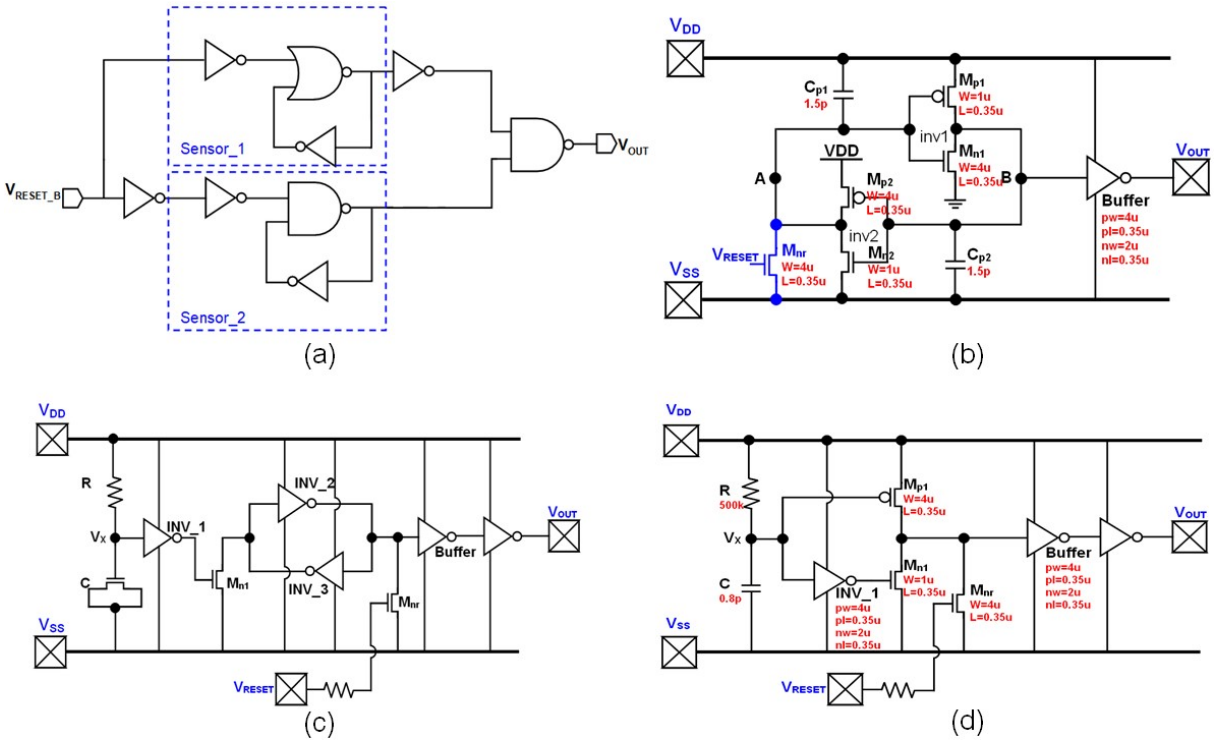


Fig. 3.1 Previous transient detection circuit composed of (a) a sensor circuit, (b) a latch circuit with additional capacitors (C_{p1} and C_{p2}), (c) RC-based detection cell, and (d) RC circuit without latch cell.

3.2.1. Simulation Parameter in HSPICE Simulator Tool

3.2.1.1 System-Level ESD Tests

It has been reported that the V_{DD}/V_{SS} lines of CMOS ICs will be influenced during system-level ESD zapping conditions [8]. The power and ground lines of microelectronic ICs no longer maintain the normal voltage levels, but an underdamped sinusoidal voltage with amplitude of several hundred volts instead. Fig. 3.2 (a) and (b) show the measured V_{DD} waveforms on the CMOS ICs inside EUT with the positive and negative ESD zapping, respectively. According to the measured results, the proper parameters of the simulated voltage source such as frequency, damping factor, voltage amplitude, and delay time can be constructed. Therefore, a specific time-dependent voltage source [15] can be given by

$$V(t) = V_0 + V_A \times \exp\left(-(t - t_d)D_{Factor}\right) \times \sin\left(2\pi D_{Freq}(t - t_d)\right) \qquad (2)$$

It is used to apply an underdamped sinusoidal voltage on the V_{DD}/V_{SS} lines of CMOS ICs, as shown in Fig. 3.3 to investigate the performance of proposed on-chip transient detection circuit.

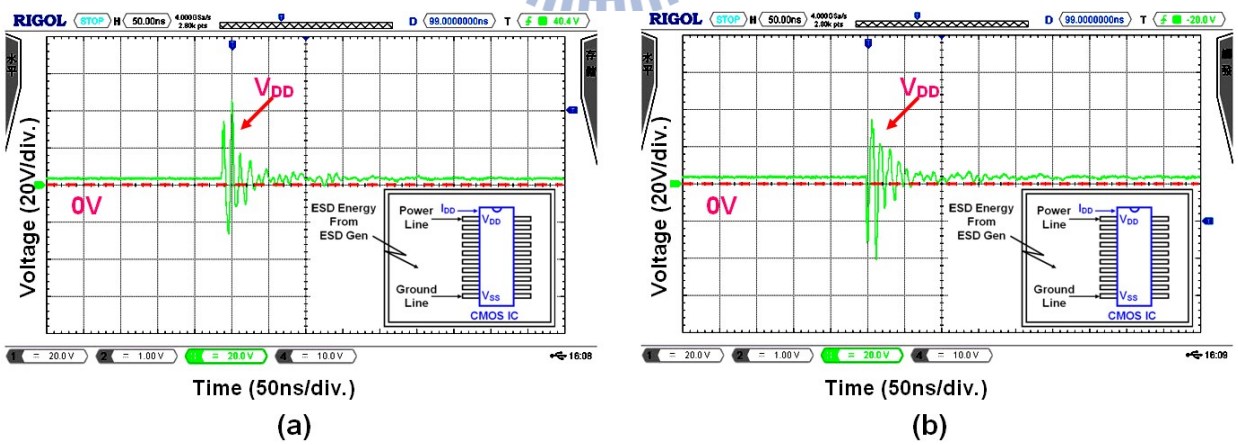


Fig. 3.2 Measured V_{DD} waveforms under system-level ESD tests with ESD voltage of (a) +1000V and (b) -1000V.

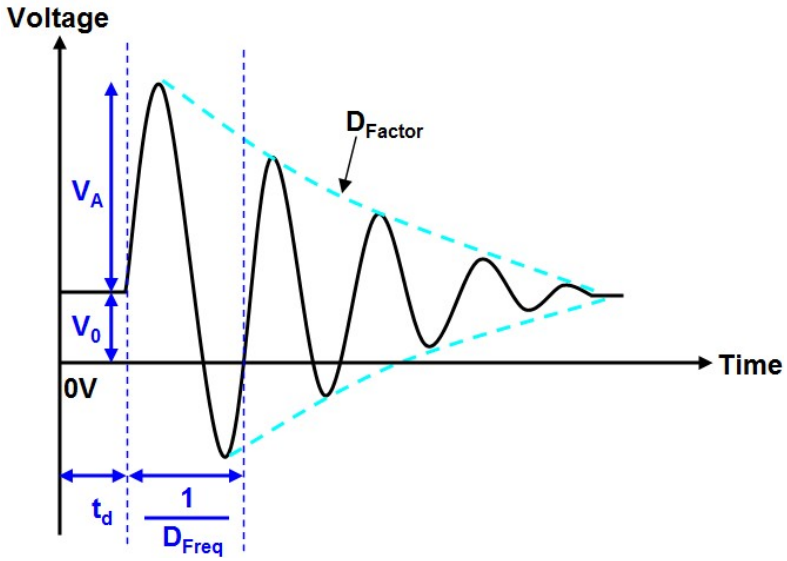


Fig. 3.3 The specific time-dependent underdamped sinusoidal waveforms applied on the power and ground lines to simulate the disturbance under system-level ESD zapping.

3.2.1.2 Electrical Fast Transient (EFT) Tests

It has been reported that the V_{DD}/V_{SS} lines of CMOS ICs will be influenced during electrical fast transient testing [18]. The power lines of the CMOS ICs no longer maintain their initial voltage levels. An exponential pulse time-dependent voltage source with rise/fall time constant parameters is used to simulate EFT-induced transient disturbance on the power lines of CMOS ICs. The rising edge of this exponential time-dependent voltage pulse is expressed as

$$V_{p(rise)}(t) = V_1 + (V_2 - V_1) \times \left[1 - \exp\left(- \frac{Time - t_{d1}}{\tau_1} \right) \right] \quad \text{,when } t_{d1} \le t \le t_{d2}. \tag{3}$$

The falling edge of the exponential voltage pulse is expressed as

$$V_{p(fall)}(t) = V_1 + (V_2 - V_1) \times \left[1 - \exp\left(- \frac{t_{d2} - t_{d1}}{\tau_1} \right) \right] \times \exp\left(- \frac{Time - t_{d2}}{\tau_2} \right) \quad \text{,when } t \ge t_{d2}. \tag{4}$$

With the proper parameters such as rise (fall) time constant τ_1 (τ_2), rise (fall) delay time t_{d1} (t_{d2}), initial DC voltage value V_1, and exponential pulse voltage V_2, the exponential voltage

source can be constructed to simulate the EFT-induced disturbance under EFT tests as shown in Fig. 3.4.

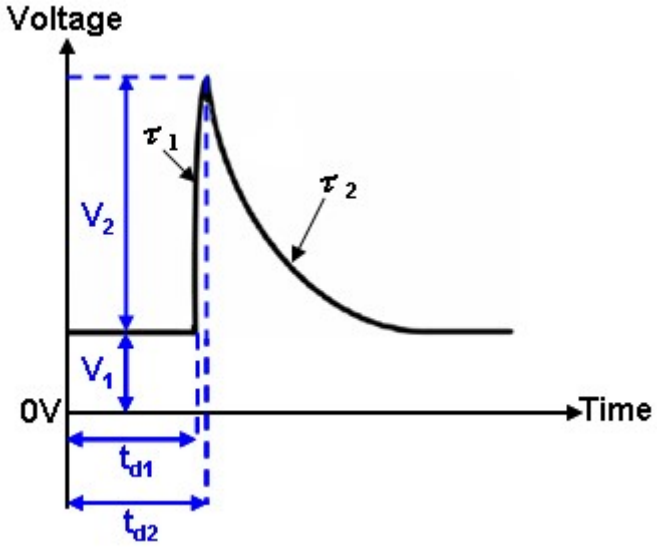


Fig. 3.4 The specific time-dependent exponential pulse waveform applied on the power lines to simulate the disturbance under EFT zapping.

3.3. New Proposed On-Chip Transient Detection Circuit

The new on-chip transient detection circuit is designed to detect the positive or negative fast electrical transients during the system-level ESD or EFT tests. Under the normal circuit operation condition (V_{DD}=3.3 V), the output state of the new proposed on-chip transient detection circuit is kept at 0 V as logic "0". After the transient disturbance, the output state will transit from 0 V to 3.3 V. Therefore, the new proposed on-chip transient detection circuit can detect and memorize the occurrence of system-level electrical transient disturbance events.

3.3.1. Circuit Structure

The schematic diagram of proposed on-chip transient detection circuit consisted of transient detection block, memory block, and output buffer block is shown Fig. 3.5. In this

transient detection circuit, a coupling capacitor (C_p) acts as a sensor which is used to detect the ESD-induced transient disturbances. R_0 is a protection resistor, which is mainly used to protect the gate of NMOS (M_{n0}). PMOS (M_{p1}), the memory block helps to memorize the logic state before and after the system-level ESD stress. The NMOS (M_{nr}) and PMOS (M_{pr}) are designed to provide the reset function while the V_{RESET} (V_{RESET_B}) input signal attains to logic high (low), and then NMOS (M_{nr}) and PMOS (M_{pr}) can be turned on to set the output logic state to "0". Under system-level ESD tests, the node V_A will be rapidly boosted by the coupling capacitor and the potential on the gate of NMOS (M_{n0}) is increased toward to V_{DD} rail, and the M_{n0} device can be turned on. Consequently, the node V_B can be changed from high voltage level to low voltage level. Therefore, the output voltage of the transient detection circuit can be transferred to high logic level to detect and memorize the occurrence of system-level ESD events.

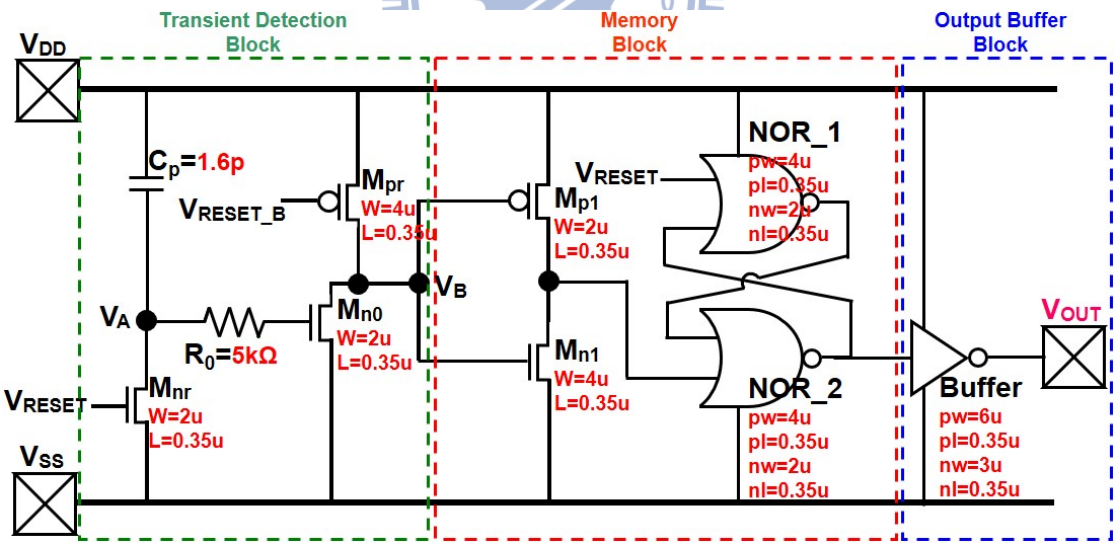


Fig. 3.5 Schematic diagram of the new proposed transient detection circuit.

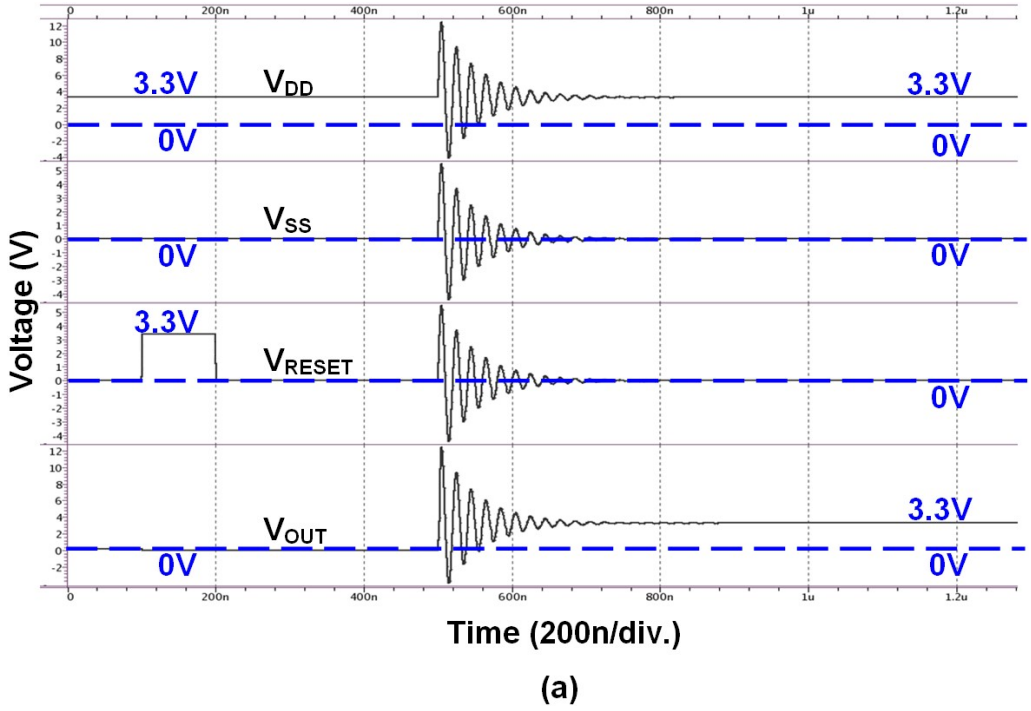
Table 3.1 Device dimension of the proposed transient detection circuit.

Device	M_{pr}	M_{p1}	M_{nr}	M_{n0}	M_{n1}
Size (μm)	W=4 L=0.35 M=1	W=2 L=0.35 M=1	W=2 L=0.35 M=1	W=2 L=0.35 M=1	W=4 L=0.35 M=1
Device	NOR_1	NOR_2	Buffer	C_p(MIM)	R_0(HR-poly)
Size (μm)	PW=4 PL=0.35 NW=2 NW=0.35	PW=4 PL=0.35 NW=2 NW=0.35	W=1 L=0.15 M=1	W=20 L=20 M=2	W=1u L=5u

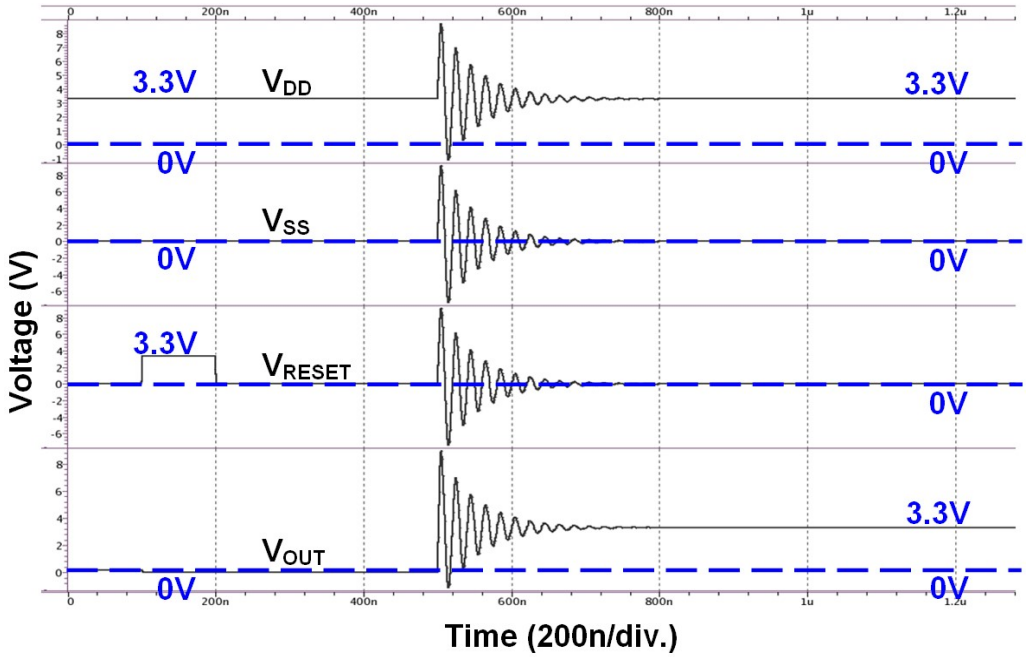
3.3.2. HSPICE Simulation Results under System-Level ESD Test

A time-dependence voltage source with different parameters such as frequency, damping factor, and voltage amplitude has been constructed to simulate the system-level ESD events. Because of the disturbance on the V_{DD}/V_{SS} lines under system-level ESD stress occurs randomly, there are many different combinations of voltage source parameters applied on the V_{DD} or V_{SS}. In order to investigate the performance of the transient detection circuit under different conditions, the simulated results are shown in Fig. 3.6 and Fig. 3.7. The simulated V_{DD}, V_{SS}, V_{RESET}, and V_{OUT} waveforms with positive-going (negative-going) underdamped sinusoidal voltage on both V_{DD} and V_{SS} lines are used to simulate the positive (negative) system-level ESD zapping conditions. In the following HSPICE simulation with underdamped sinusoidal waveforms on V_{DD}/V_{SS} lines, the same parameters of D_{Factor}=2x10^7S^{-1}, D_{Freq}=50MHz, t_d=500ns are used in both positive and negative underdamped sinusoidal voltage source, whereas the only different is the value of voltage amplitude. Firstly, the initial V_{DD} voltage is maintained at 3.3V and the relative V_{SS} is 0V. Secondly, logic high voltage pulse is used to trigger the reset function of the transient detection circuit causing the initial output voltage at 0V and the memory block would store this logic state. Fig. 3.6 (a)

(Fig. 3.7 (a)) shows the overshooting (undershooting) voltage amplitude coupled on both V_{DD}/V_{SS} lines, and the voltage amplitude on V_{DD} is lager than that on V_{SS}. On the contrary, the overshooting (undershooting) voltage couple on both V_{DD} and V_{SS} shown in Fig. 3.6 (b) (Fig. 3.7 (b)), but that on the V_{SS} is lager. During different system-level ESD conditions, the V_{DD}/V_{SS} begins to jiggle rapidly from 3.3V/0V and the output node V_{OUT} is disturbed simultaneously. As the results, after V_{DD}/V_{SS} returns to its normal voltage level of 3.3V/0V, the output voltage of the transient detection circuit will be changed from 0V to 3.3V.

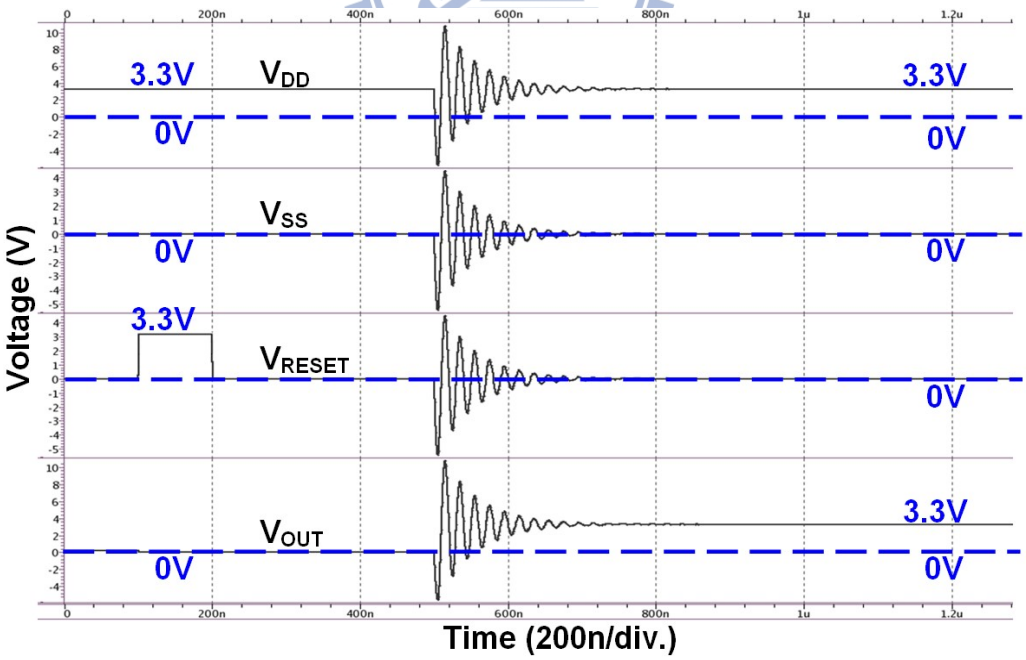


(a)

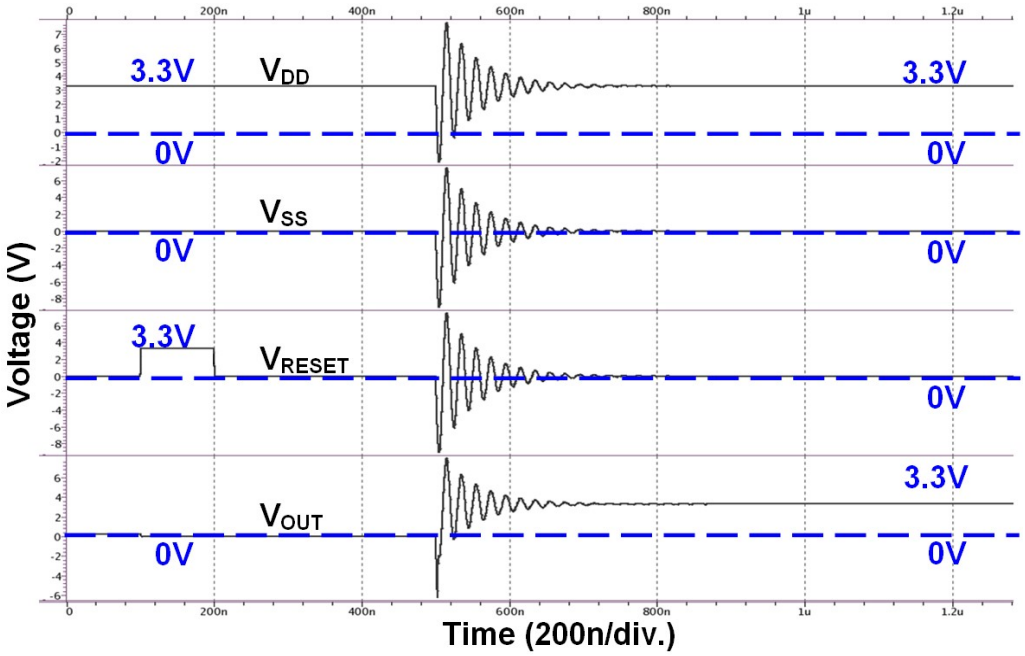


(b)

Fig. 3.6 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit with positive-going underdamped sinusoidal voltage on both V_{DD} and V_{SS}. (a) the overshooting amplitude on V_{DD} is larger than that on V_{SS}. (b) the overshooting amplitude on V_{SS} is larger than that on V_{DD}.



(a)



(b)

Fig. 3.7 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit with negative-going underdamped sinusoidal voltage on both V_{DD} and V_{SS}. (a) the undershooting amplitude on V_{DD} is larger than that on V_{SS}. (b) the undershooting amplitude on V_{SS} is larger than that on V_{DD}.

The routing traces may be different for power lines and ground lines on the PCB shown in Fig. 3.8 [15]. According to this reason, coupling path from the ESD zapping source to the V_{DD} and V_{SS} inside ICs may be different. A signal delay of 5-ns between V_{DD} and V_{SS} waveforms under system-level ESD zapping has been measured [15], as shown in Fig. 3.9. In order to simulate this signal delay condition, a 5-ns delay time between the V_{DD} and V_{SS} is applied on the underdamped sinusoidal waveforms with positive-going and negative-going shown in Fig. 3.10 (a) and (b). From the simulated results with a signal delay between V_{DD} and V_{SS}, the on-chip transient detection circuit can still detect the fast electrical transients.

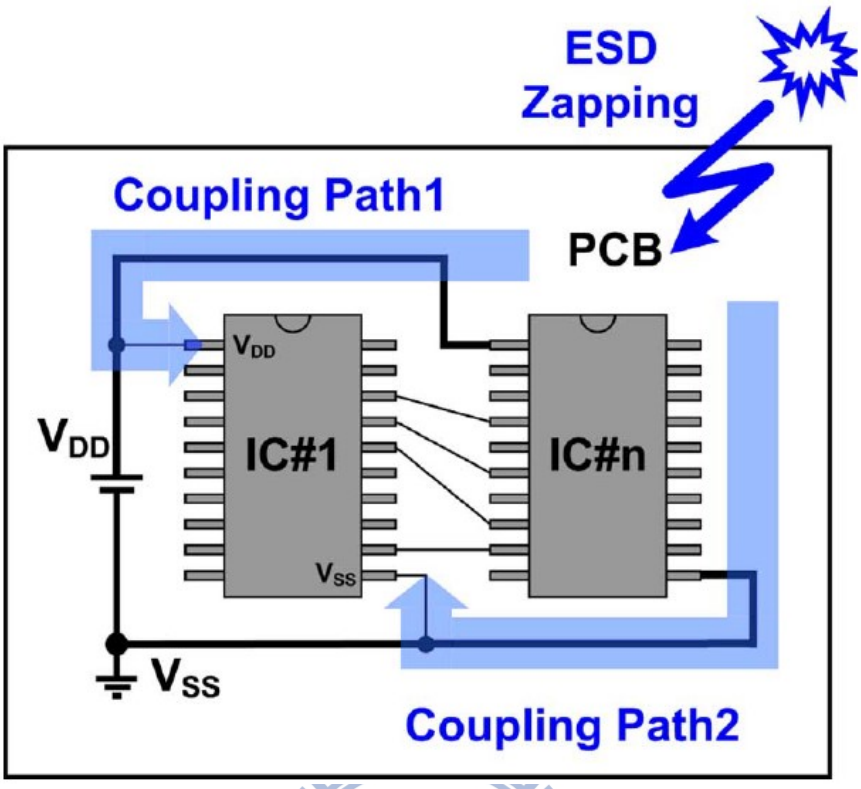


Fig. 3.8 Different coupling path from the ESD zapping source to V_{DD} and V_{SS} pins of CMOS IC on the PCB.

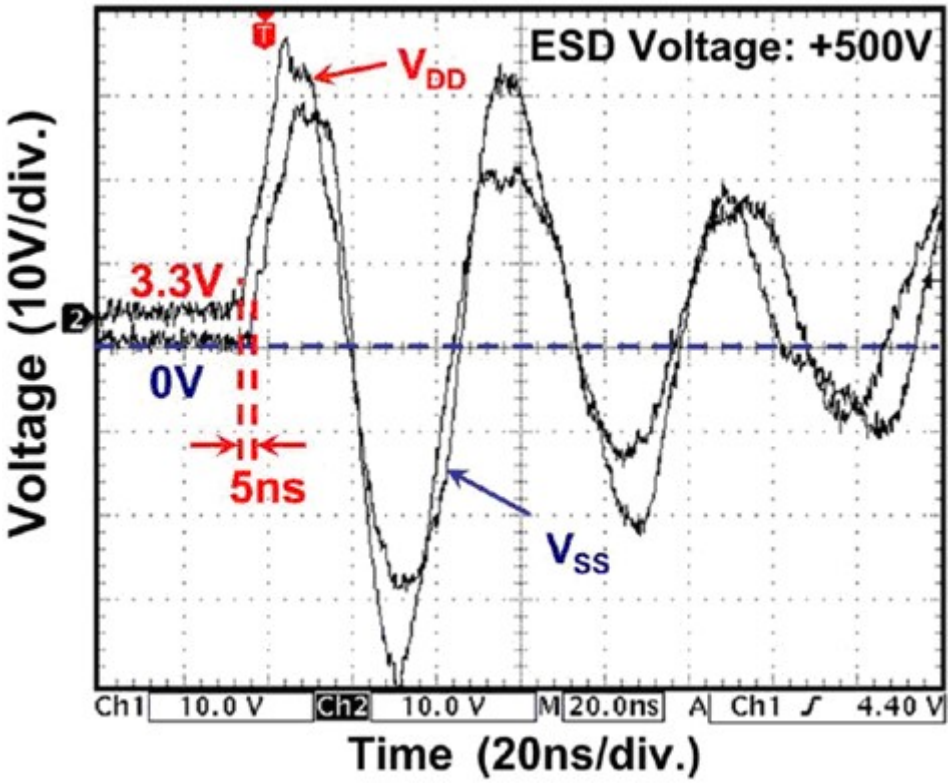


Fig. 3.9 Time delay between the measured V_{DD} and V_{SS} waveforms is due to the different

coupling path [15].

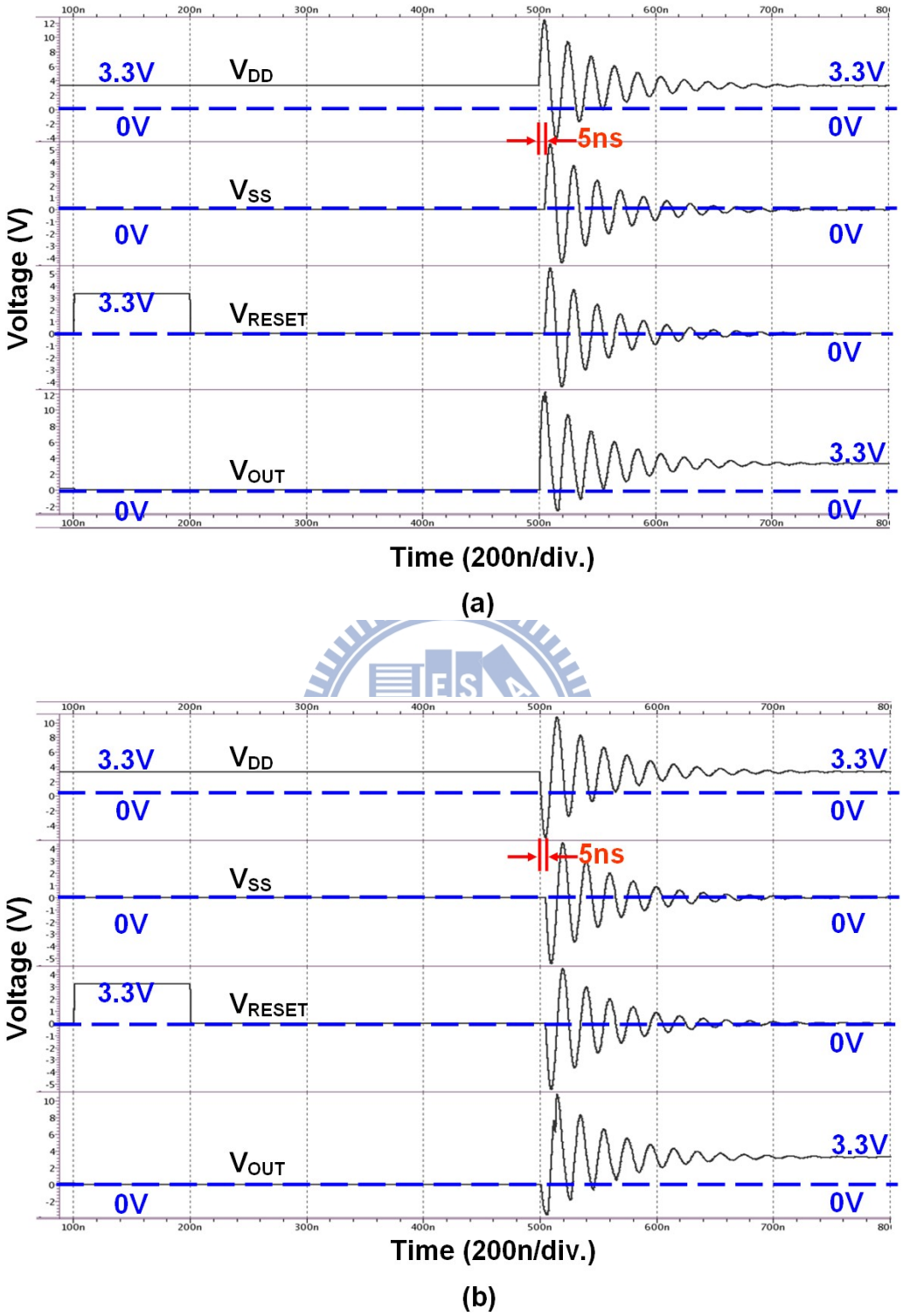
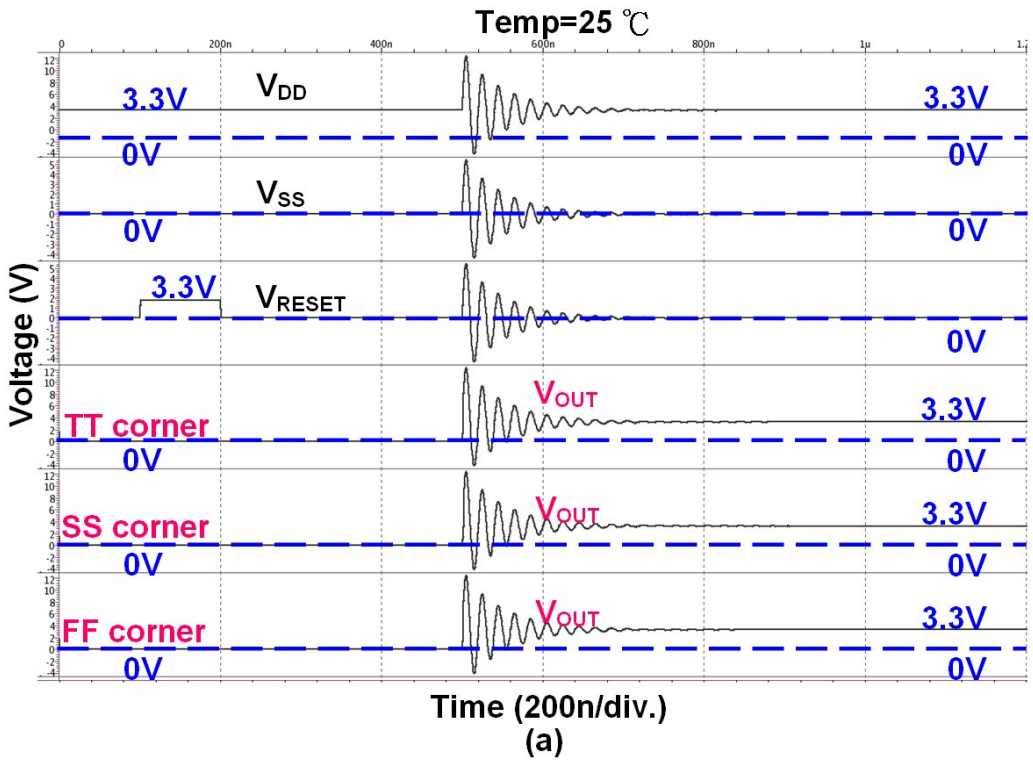


Fig. 3.10 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit under (a) positive-going underdamped sinusoidal voltage on both V_{DD} and V_{SS} With 5ns delay time and under (b) negative-going underdamped sinusoidal voltage on both V_{DD} and V_{SS} With

5ns delay time.

In addition, the process variations and ambient temperature may affect the circuit behavior, therefore, these conditions are used to simulate, the simulation waveforms are shown in Fig. 3.11 (a), (b) and (c). from the simulated results with process variations (TT, SS and FF corner) and ambient temperature (25℃, -40℃ and 100℃), the transient detection circuit can still detect the fast electrical transients.



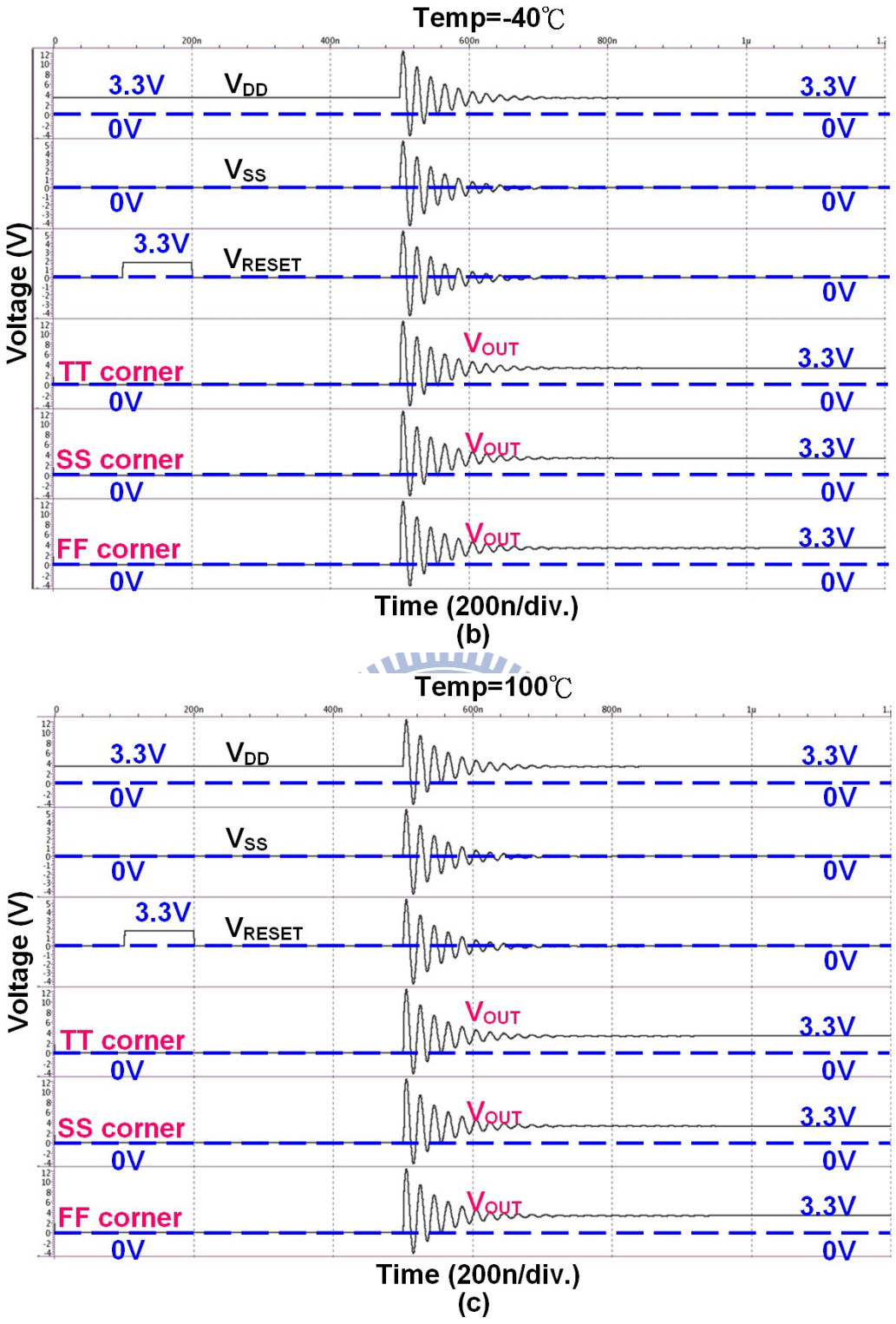


Fig. 3.11 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit under positive-going underdamped sinusoidal voltage with process corner and (a) ambient temperature at 25°C, (b) ambient temperature at -40°C and (c) ambient temperature at 100°C.

3.3.3. HSPICE Simulation Results under EFT Test

In order to achieve the requirement of a single exponential pulse under EFT tests, parameters of τ_1=3ns, τ_2=25ns, and t_{d1}-t_{d2}=10ns are used to simulate the positive or negative time-dependent voltage waveforms, in addition, the initial DC voltage on the power line (V_{DD}) of the transient detection circuit is still at 3.3V.

The simulated V_{DD}, V_{RESET}, and V_{OUT} waveforms of the proposed on-chip transient detection circuit with a positive or negative exponential voltage pulse on the V_{DD} are shown in Fig. 3.12 (a) and (b). To reset the output voltage level of the transient detection circuit to 0V, a logic high voltage pulse is applied on the reset function. Then, the exponential voltage source with amplitude of +15V is used to simulate the positive EFT-induced transient disturbance on the power lines under EFT tests. V_{DD} begins to increase rapidly from 3.3V to 13V, and the output voltage of transient detection circuit is influenced at the same time as shown in Fig 3.12 (a). Similarly, the exponential voltage source with amplitude of -15V is used to simulate the negative EFT-induced transient disturbance on the power lines under EFT tests. V_{DD} begins to decrease rapidly from 3.3V to -13V, and the output voltage of transient detection circuit is influenced simultaneously as shown in Fig 3.12 (b). After the positive or negative transient disturbance duration, V_{DD} returns to its initial voltage level of 3.3V and the output state of the transient detection circuit changes from 0V to 3.3V.

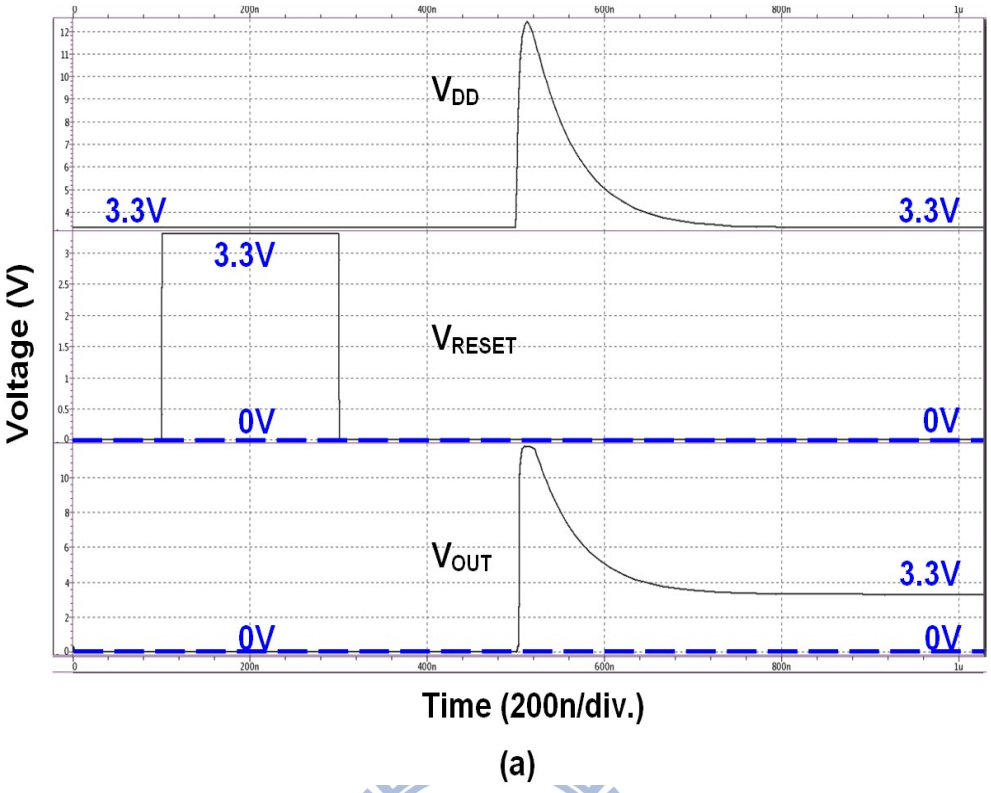


Fig. 3.12 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit under (a) positive exponential pulse on V_{DD} with amplitude of +15V.

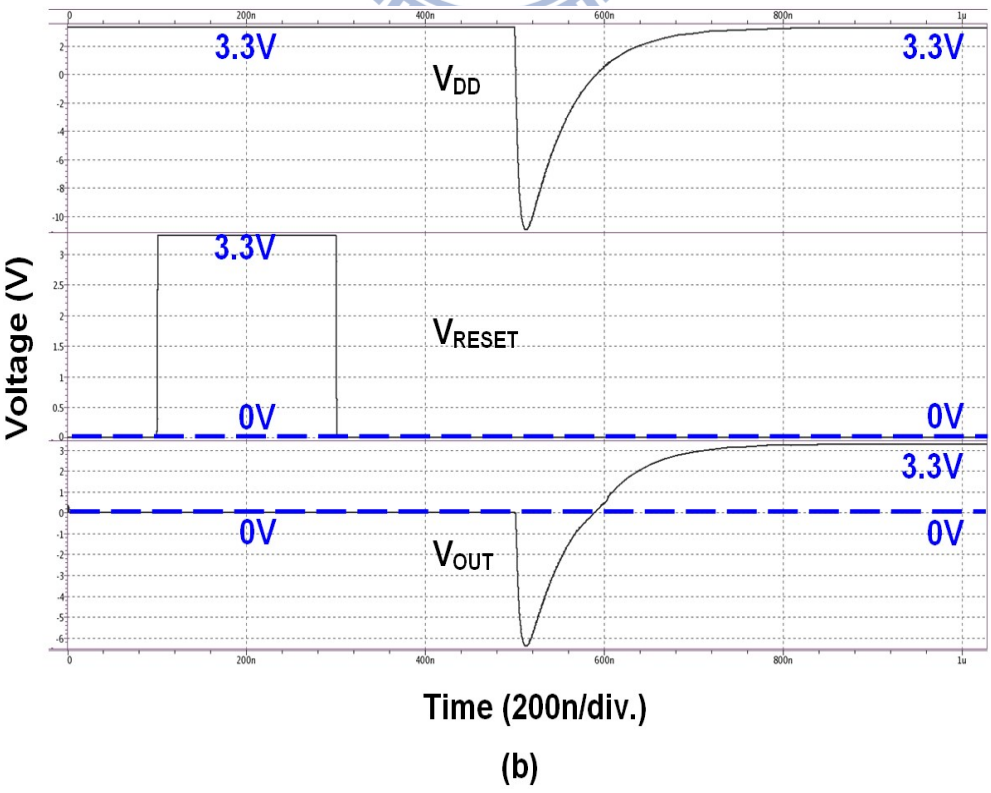


Fig. 3.12 Simulated V_{DD}, V_{SS}, V_{RESET} and V_{OUT} waveforms of the transient detection circuit under (b) negative exponential pulse on V_{DD} with amplitude of -15V.

3.4. Experimental Results

As shown in Fig. 3.13, the transient detection circuit has been equipped with the on-chip ESD protection circuit in a chip. It has been fabricated in a 0.15-μm CMOS process with 3.3-V devices. In this test, the output signal of the transient detection circuit will be buffered to I/O, therefore, it can be measured on I/O. The chip layout and photo are shown in Fig. 3.14(a) and (b).

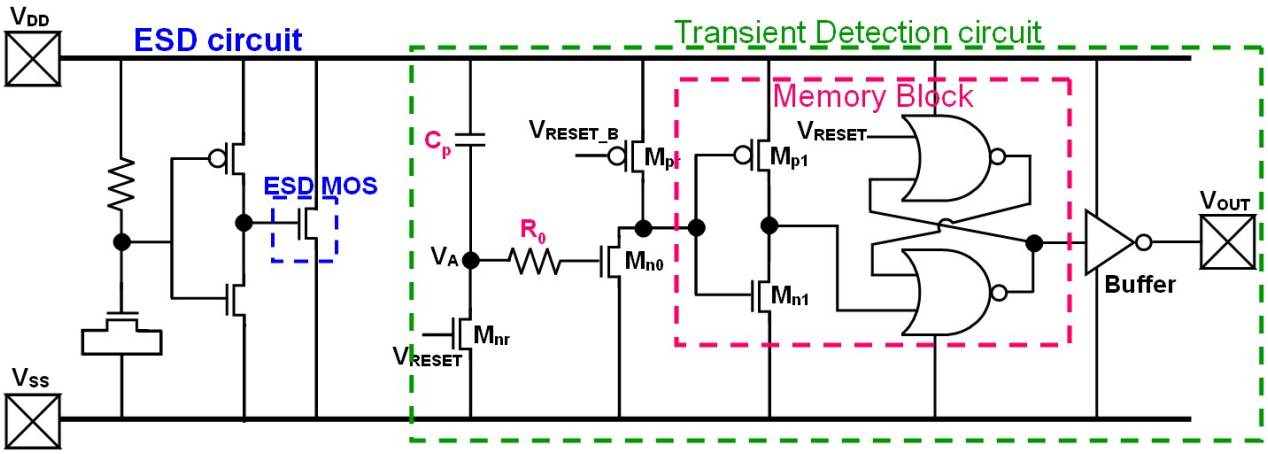


Fig. 3.13 Schematic diagram of the transient detection circuit equipped with the ESD circuit.

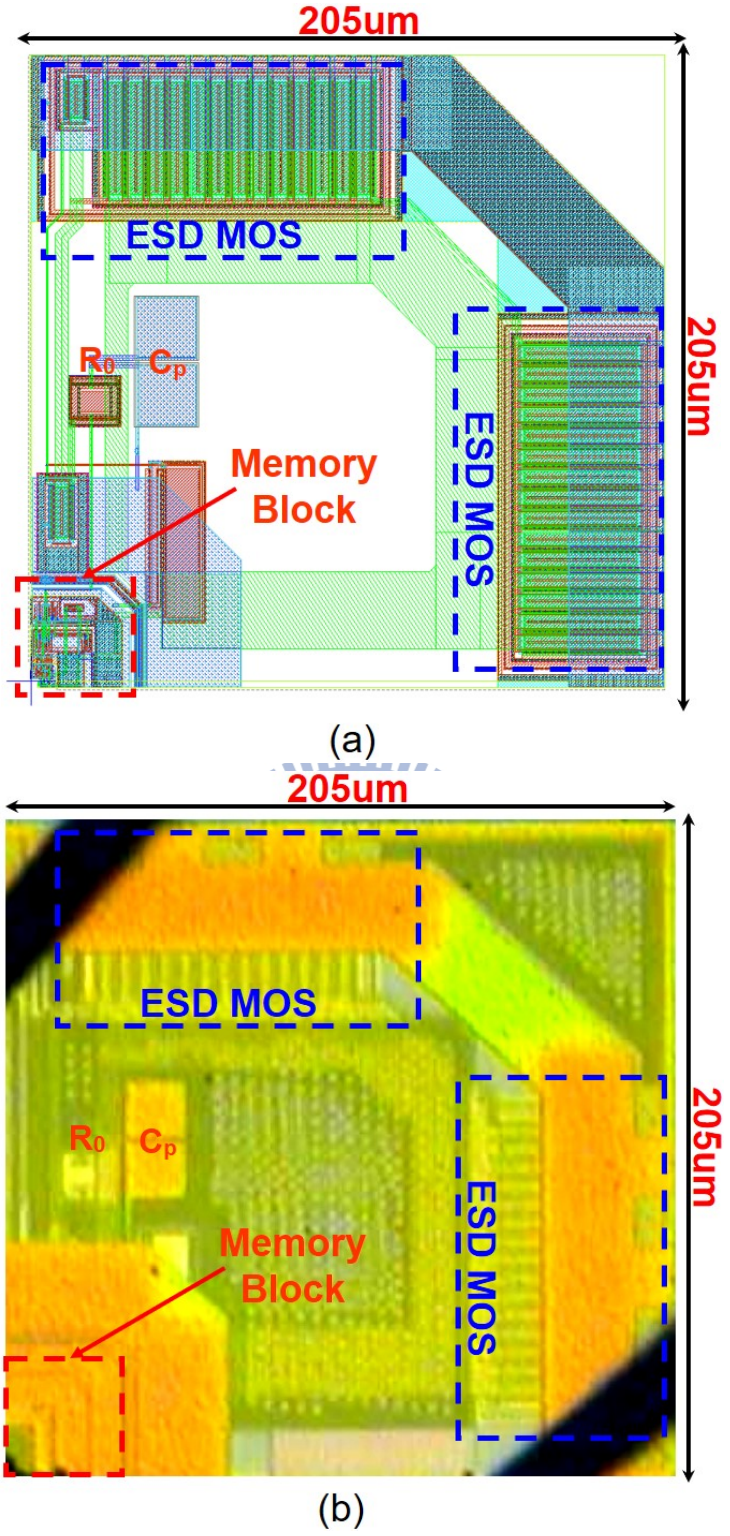


Fig. 3.14 (a) chip layout and (b) photo of the new proposed transient detection circuit is fabricated in a 0.15-μm CMOS process with 3.3-V devices.

3.4.1. Measurement Setup for System-Level ESD Test

In IEC 61000-4-2, two test modes have been specified, which are the air-discharge and contact-discharge test mode. In the case of contact discharge test mode, the sharp discharge tip is used to simulate the mechanical ESD damage on the EUT. The contact discharge is applied to the conductive surfaces of the EUT (direct application) or to the coupling planes (indirect application). Contact discharge is further divided into direct discharge to the system under test, and indirect discharge to the horizontal or vertical coupling planes. Fig. 3.15 shows the measurement setup of the system-level ESD test standard with indirect contact-discharge test mode. The measurement setup of system-level ESD test consists of a wooden table on the grounded reference plane (GRP). In addition, an insulation plane is used to separate the EUT from the horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470kΩ resistor in series [6]. When the ESD gun zaps the HCP, the electromagnetic interference (EMI) coming from ESD gun will be coupled into all CMOS ICs inside EUT. The power lines of CMOS ICs inside EUT will be disturbed by the ESD-coupled energy.

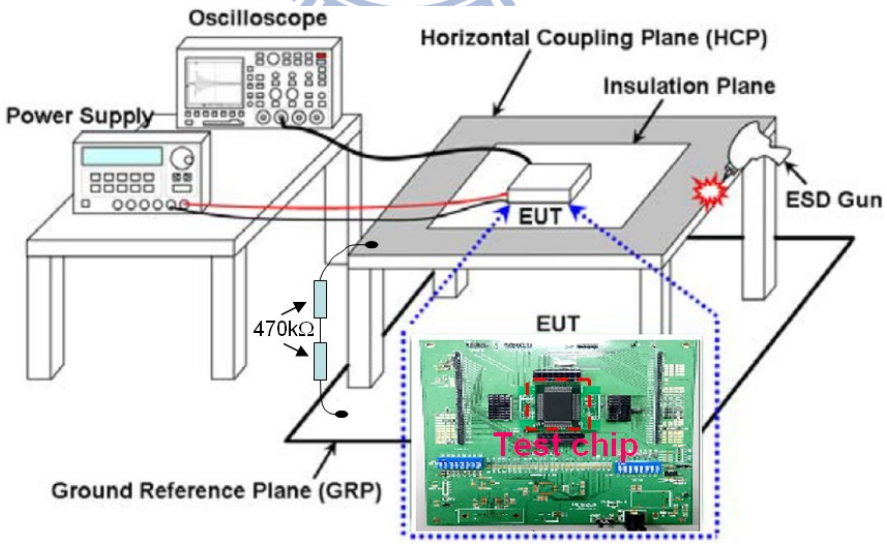


Fig. 3.15 Measurement setup for system-level ESD test with indirect contact-discharge test mode [6] to evaluate the detection function of the on-chip transient detection circuit.

3.4.2. System-Level ESD Test Results

With above measurement setup, the circuit function of the proposed detection circuit after system-level ESD tests can be evaluated. By monitoring the oscilloscope, the transient responses on power line of CMOS ICs can be recorded and analyzed. Before each system-level ESD test, the initial output voltage (V_{OUT}) of the proposed detection circuit is reset to 0V. After each system-level ESD test, the output voltage (V_{OUT}) is monitored to check its final voltage level. Thus, the function of the proposed detection circuit can be evaluated under system-level ESD tests, but in order to protect the test equipment, the ESD zapping voltage is set at 1kV.

Under system-level ESD test with positive ESD voltage of +1.0kV, the measured V_{DD} and V_{OUT} waveforms of the proposed transient detection circuit is shown in Fig. 3.16 (a). The power and ground lines of the transient detection circuit are disturbed with ESD stress, the V_{DD} begins to rapidly increase from the normal voltage level of 3.3V. Meanwhile, V_{OUT} begins to change under such a high-energy ESD stress. During the fast transient disturbance, V_{DD} and V_{OUT} are influenced simultaneously. After system-level ESD test with positive ESD voltage, V_{DD} and V_{SS} return to the original operation voltage level of 3.3V and 0V. Finally, the output voltage level of the proposed transient detection circuit can transit from 0V to 3.3V.

In addition, under system-level ESD test with negative ESD voltage of -1.0kV, the measured V_{DD} and V_{OUT} waveforms of the proposed transient detection circuit is shown in Fig. 3.16 (b). During the ESD-induced transient disturbance, V_{DD} begins to rapidly decrease from the normal voltage level of 3.3V. Finally, the output voltage level of the proposed transient detection circuit can transit from 0V to 3.3V.

Therefore, the new proposed on-chip transient detection circuit can successfully detect the electrical transient disturbance under system-level ESD tests with positive and negative

ESD voltages.

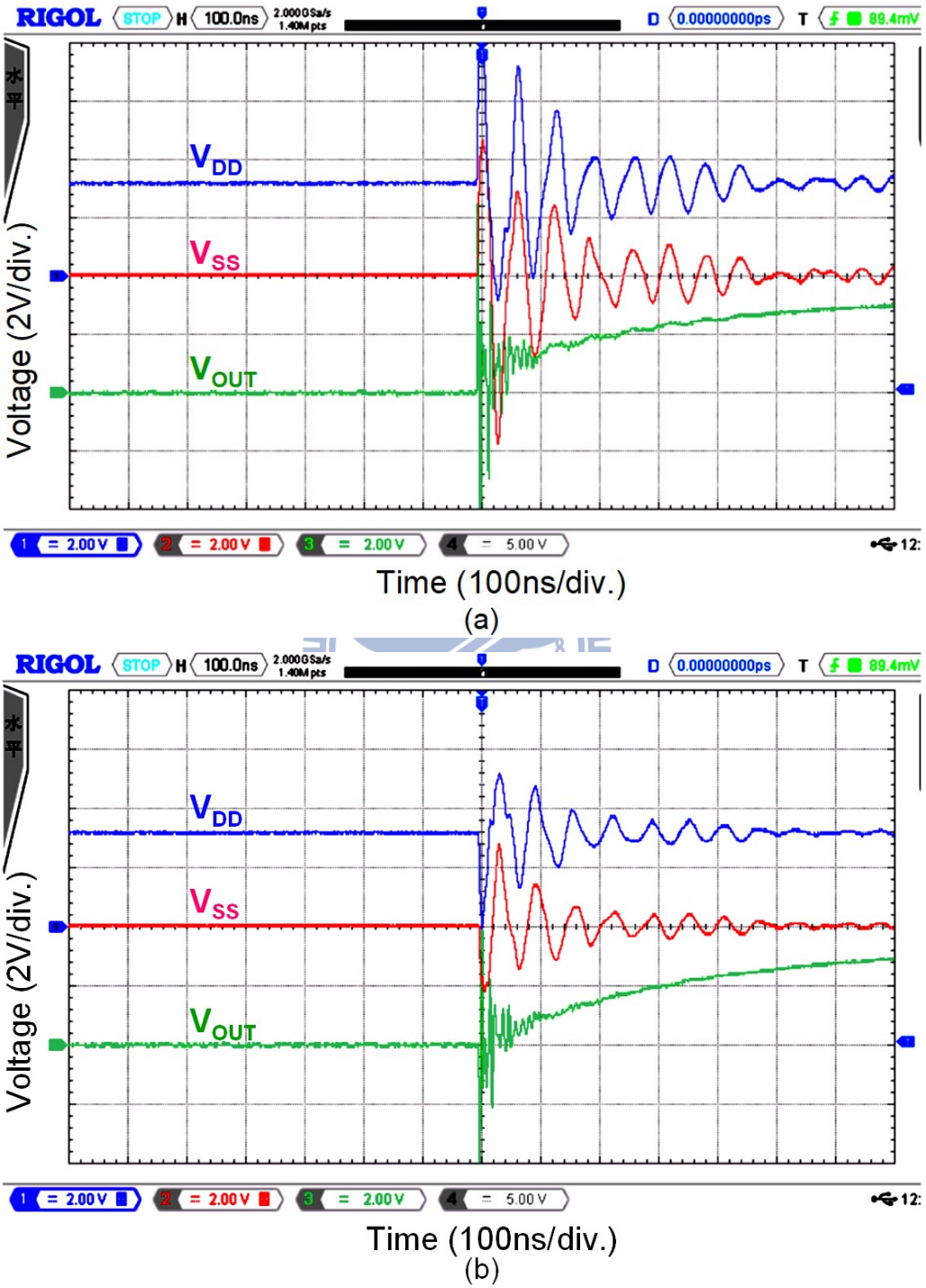


Fig. 3.16 Measured V_{DD}, V_{SS} and V_{OUT} transient responses on the proposed transient detection circuit under system-level ESD test with (a) ESD voltage of +1kV and (b) -1kV.

3.5. Comparison

In this chip, the prior art circuits (Fig. 3.1b [15] and Fig. 3.1d [16]) was also fabricated in a 0.15-μm CMOS process with 3.3-V devices. Now, comparing the prior art circuits and the new proposed transient detection circuit, first, under system-level ESD testing, the prior art circuits (Fig. 3.1b and Fig. 3.1d) can detect minimum positive ESD voltage of +0.86kV and +0.72kV, respectively. For the new proposed transient detection circuit is +0.83kV. Second, under system-level ESD with negative ESD voltage，the prior art circuits (Fig. 3.1b and Fig. 3.1d) are -0.97kV and -0.85kV, respectively. The new proposed transient detection circuit is -0.91kV. Therefore, in detecting the minimum ESD voltage, the performance of the new proposed transient detection circuit is better than prior art circuit [15].

In addition, comparing the layout area, the area of the figure 3.1b is smaller than the new proposed transient detection circuit, and the area of the figure 3.1d [16] is larger than the new proposed transient detection circuit. These comparative items are listed in table 3.2.

Table 3.2 Performance and comparison list.

Comparative items	This work	Prior art [15]	Prior art [16]
Detection minimum voltage (kV)	+0.83 / -0.91	+0.86 / -0.97	+0.72 / -0.85
Layout area(μm^2)	1209	1073	2390

3.6. Summary

In this chip, the transient detection circuit has been equipped with the ESD circuit in a chip, and fabricated in a 0.15-μm CMOS process with 3.3-V devices. It has been investigated and designed by using HSPICE simulator tool. The system-level ESD test is adopted to verify the proposed on-chip transient detection circuits. From the experimental results, the output of

transient detection circuit can transit from 0V to 3.3V after ESD voltage zapping. Therefore, it has been confirmed that the transient detection circuit can successfully detect and memory the occurrence of ESD-induced transient disturbance.

Accord to the previous research [8], it is reasonable that with hardware/firmware co-design method, the output state of the proposed on-chip transient detection circuit can be used as the firmware index to provide an effective solution against the system malfunction caused by ESD-induced electrical transient disturbance.

Chapter 4

Improve System-Level ESD by Hardware / Firmware Co-Design

4.1 Background

In the previous experimental results, it had been confirmed that the transient detection circuit could successfully detect the occurrence of ESD-induced transient disturbance. This means that hardware / firmware co-design can be implemented on the system operation. The simple conception is shown in Fig 4.1 [8]. When the fast electrical transient happens, the on-chip transient detection circuit can detect the fast electrical transient to change the output state V_{OUT} to logic 1, and the firmware executes the recover procedure to recover all system functions to a stable state as soon as possible. After the reset and recover procedures, the states in the transient detection circuit and the ESD flag are reset to logic 0 again for detecting the next ESD events. Moreover, it had been reported that the hardware / firmware co-design can effectively improve the robustness of the industrial products against electrical transient disturbance [8].

Recently, the requirement of system-level ESD and EFT tests level are often depended on customer-defined specifications. In order to meet customer requirements, in this work target, the microelectronic products are required to sustain the ESD-generated voltage of ±12kV (±18kV) under contact-discharge (air-discharge) test mode to achieve the immunity criterion of “class B” level in the IEC 61000-4-2 standard.

The new proposed hardware / firmware co-design will be introduced In this chapter, by using this method can successfully increase system-level ESD test level and improve the

microelectronic products against electrical transient disturbance.

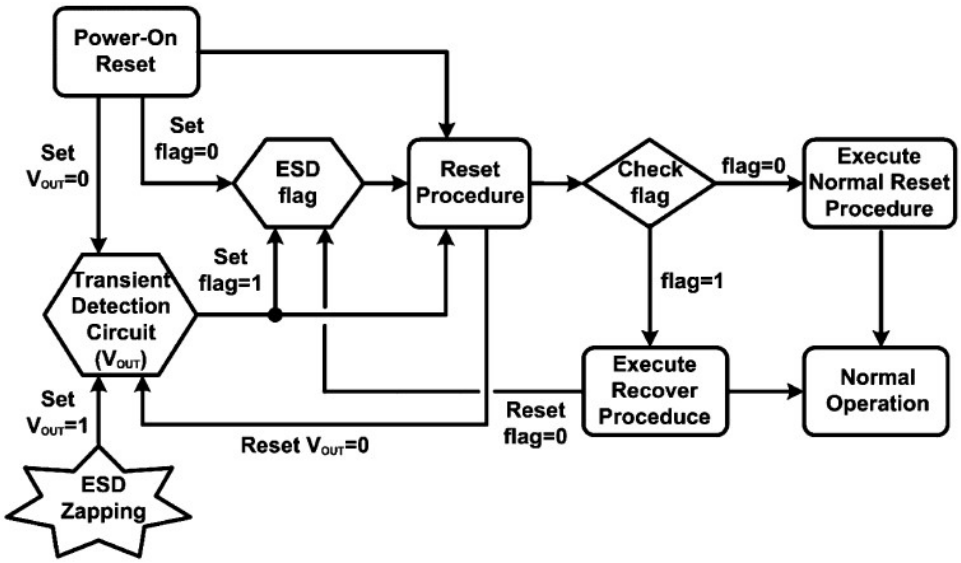


Fig. 4.1 Firmware flowchart to reset or recover the system if the on-chip transient detection circuit detects the ESD-induced transient disturbance [8].

4.2 Design a New Reset Method

Under system-level ESD test, because of the ESD-induced transient disturbance leads to malfunction of the microelectronic system, the main reason for system failure is not enough system reset time. There are three types of signals to provide system reset, such as Power-On Reset (POR), Brown-Out Reset (BOR), and External Reset (XRES). During system-level ESD or EFT test, the ESD-generated transient electrical voltage with quite large amplitude to the power line, at this moment, the POR, BOR, and external reset may have the opportunity to be triggered. Typically, the system reset time needs to maintain several of microseconds and then the microelectronic system can restore to a steady state. However, these reset signals are triggered by the ESD-induced disturbance, the system reset time is a hundred nanoseconds only, therefore, the microelectronic system can not return to a normal state, which leads to malfunction of the microelectronic system.

4.2.1 Traditional Reset Method

The tradition reset method is shown Fig. 4.2. Usually, PORB, BORB, and XRESB are inverted signals from the POR, BOR, and XRES, respectively. These signals are connected to the input of the "AND" gate, then the output of the "AND" gate is divided into two terminals, one is connected to the input of the "OR" gate, the other end is connected to the delay cell, and then the output of the delay cell is connected to the other input of the "OR" gate. When any input of the "AND" gate is logic "0", the signal time must exceed the delay cell time, the system reset mechanism can be started. The main function of the delay cell to prevent the reset signal which is not affected the glitch, and the delay time is designed about 20ns~30ns.

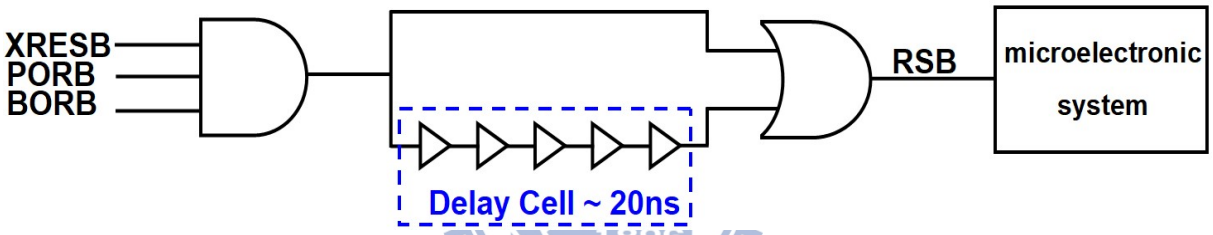


Fig. 4.2 Traditional reset method, when any input of the "AND" gate is logic "0" and the signal must exceed the delay cell time, the system reset mechanism can be started.

A simple circuit diagram including POR, BOR, and external reset is shown in Fig 4.3. In order to simulate the ESD zapping to power lines, the system-level ESD simulation parameters are loaded into simulator, and then the behavior of these circuits are simulated by using HSPICE, the simulation waveforms are shown in Fig 4.4(a), (b) and (c), respectively. In order to observe the convenience, the waveform of VSS is subtracted from the waveform of POR, BOR and XRESB, respectively. First, XRESB has a low-pass filter that can filter out the high-frequency signals, therefore, XRESB is not affected. However, During the ESD zapping, PORB and BORB have been changed from logic "1" to "0", the time of the logic "0" is about 200 ns and it is more than delay cell time, therefore, the microelectronic system will

be reset. Due to the reset-time is short, the microelectronic system cannot be restored to a steady state, which leads to malfunction of the microelectronic system.

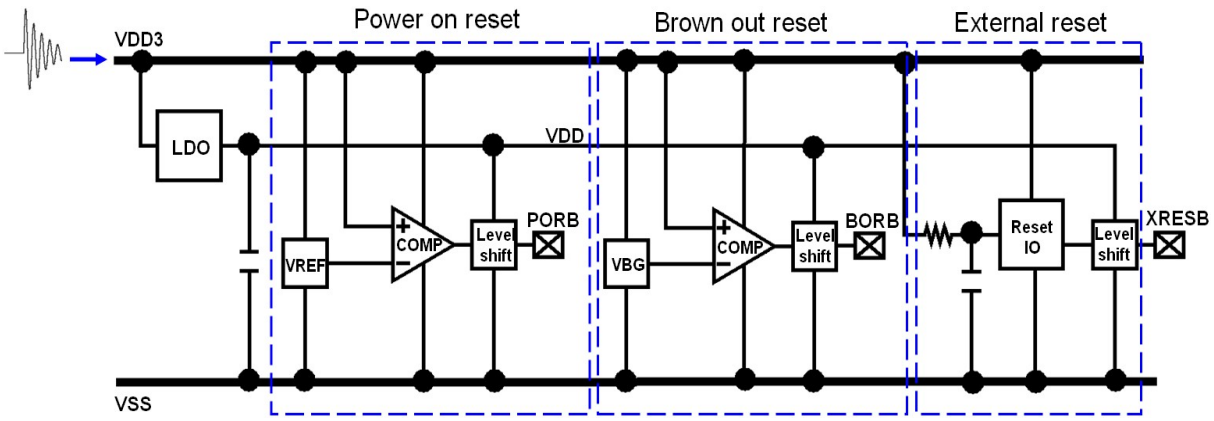
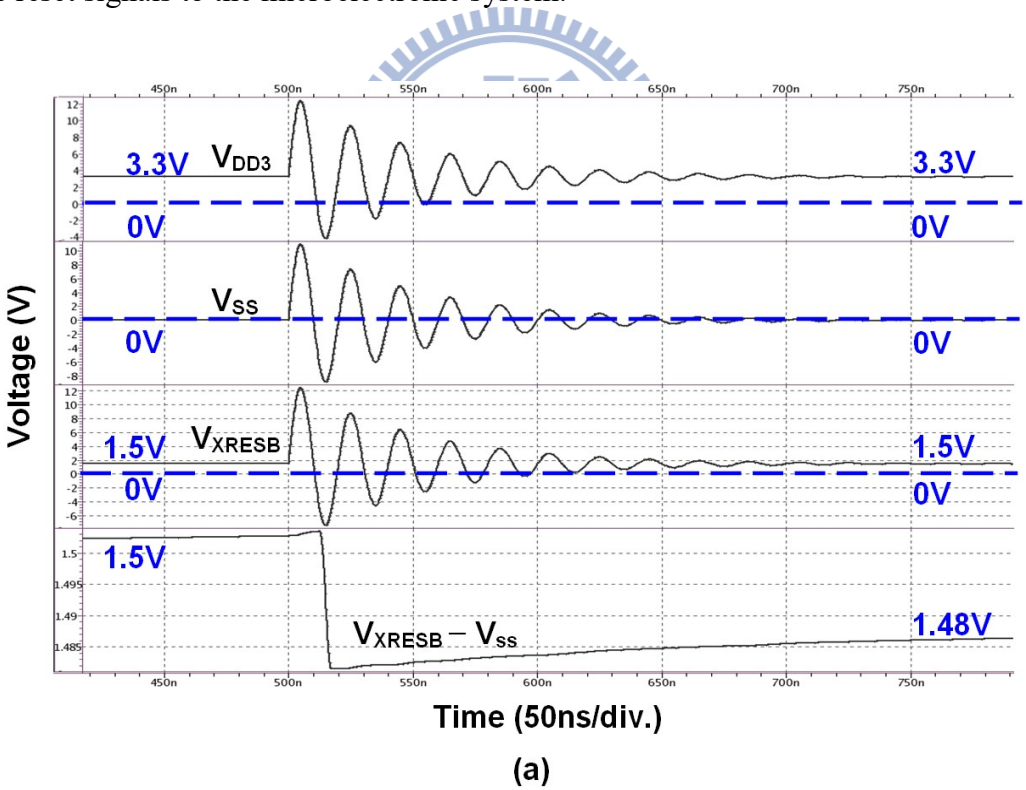


Fig. 4.3 The simulation block diagram includes POR, BOR and external reset; these circuits provide reset signals to the microelectronic system.



(a)

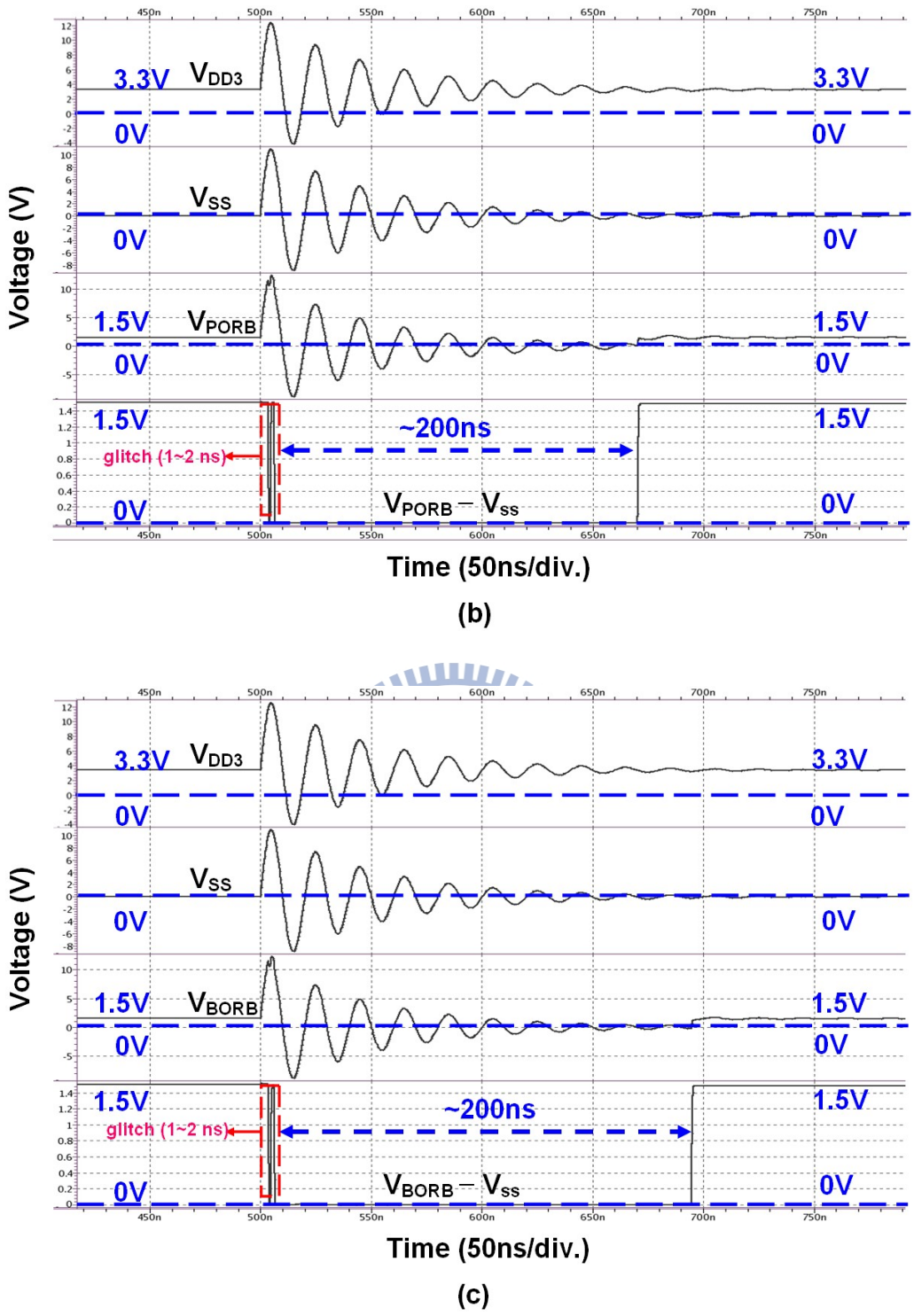


Fig. 4.4 Simulated positive-going under-damped sinusoidal voltage (a) XRESB, (b) PORB, (c) BORB.

4.2.2 New Proposed Reset Method

It has been reported that waveforms are measured under system-level ESD tests, as shown Fig 4.5 [15], from the ESD-induced transient disturbance to the power steady state, the time for power stable is about 1μs. In the new proposed reset method, the time of the delay cell is designed about 1.5 μs. The new proposed reset method is shown in Fig. 4.6. The new delay cell consists of resistor and capacitor that act a low-pass filter. By using the resistance and the capacitance to adjust the delay time, however, if the capacitance is used to adjust delay time, the layout area will be increase, therefore, the delay time adjustment will use the resistance. In fact, it requires several mega-Ω if the resistance is used to adjust delay time, this layout is still increased the area. Under such considerations, long channel NMOS (M_{nl}) and PMOS (M_{pl}) will be used, which not only increase the resistance but also reduce the layout area. In addition, MIM capacitor is used in this design, which provides a stable capacitance to obtain accurate delay time; therefore, the output signal of the circuit is not disturbed by the power within the delay time. Finally, in order to avoid ESD reliability issue, the tie high and tie low cells will be used to protect gate oxide of the M_{nl} and M_{pl}. The new delay cell is called a de-bounce circuit (DEB_CKT). The circuit schematic and layout are shown in Fig. 4.7 (a), (b), and the component size is list in table 4.1.

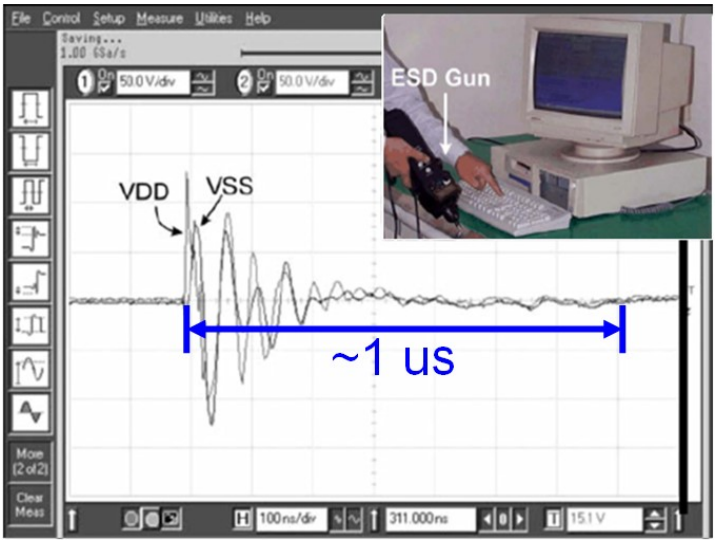


Fig. 4.5 Measured V_{DD} and V_{SS} waveforms of the microcontroller ICs inside the keyboard with an ESD voltage of +1000 V zapping on the HCP under system-level ESD test [15].

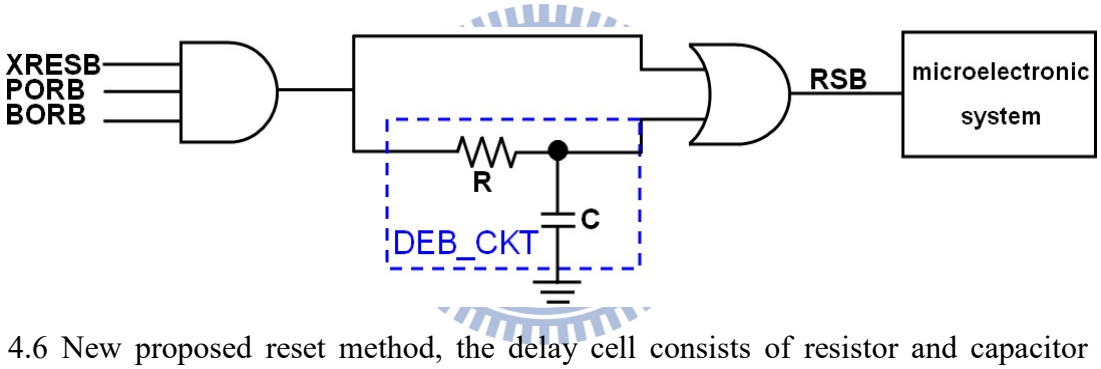
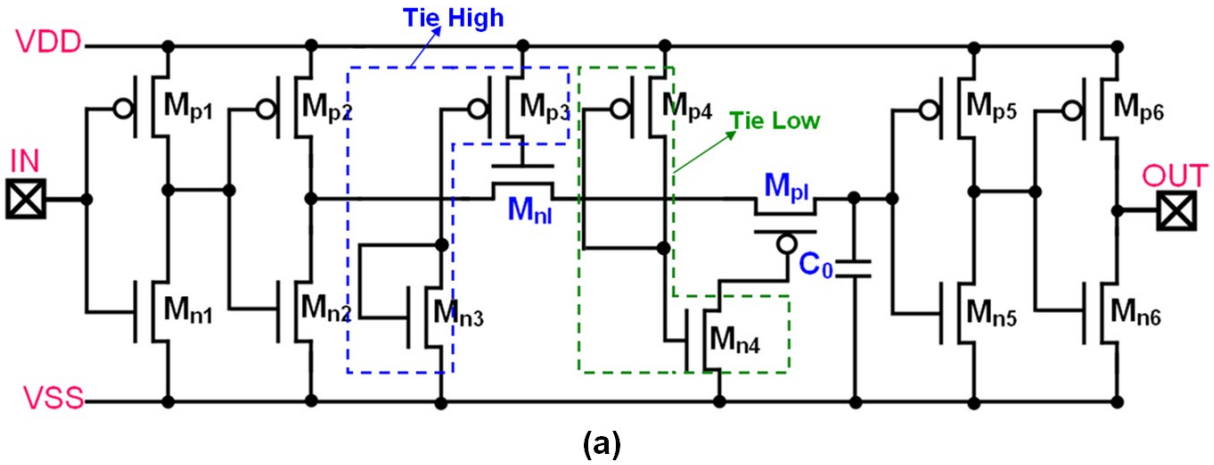


Fig. 4.6 New proposed reset method, the delay cell consists of resistor and capacitor as a low-pass filter. The delay cell is called a de-bounce circuit (DEB_CKT).



(a)

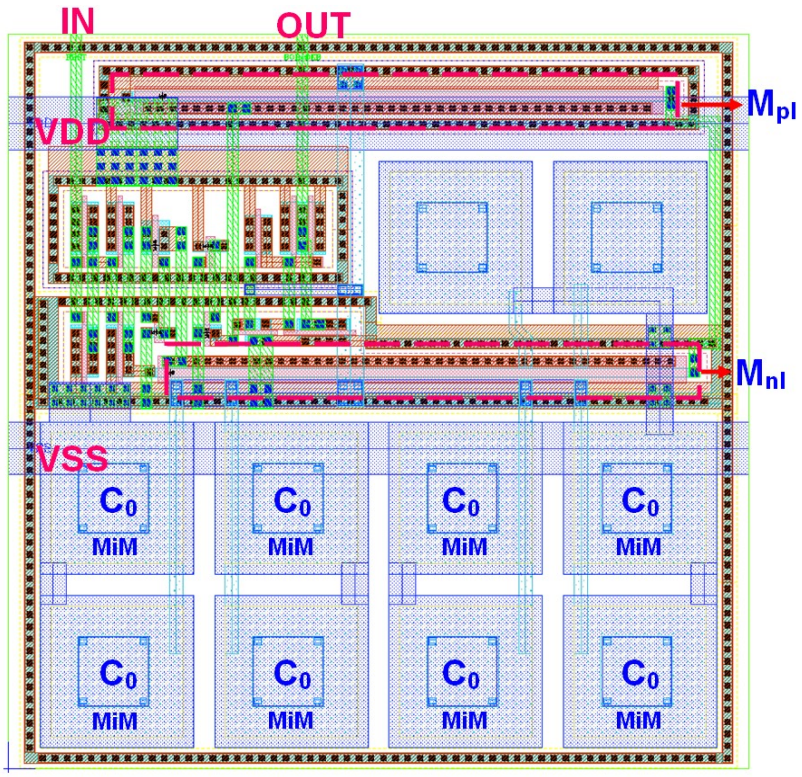


Fig. 4.7 The de-bounce circuit uses a long channel NMOS and PMOS instead of resistances. (a) circuit schematic and (b) circuit layout

Table 4.1 Device dimension of the de-bounce circuit.

Device	M_{p1}	M_{p2}	M_{p3}	M_{p4}	M_{p5}
Size (μm)	W=2 L=0.15 M=1	W=2 L=0.15 M=1	W=1.3 L=0.15 M=1	W=0.35 L=0.35 M=1	W=1.5 L=0.15 M=1
Device	M_{p6}	M_{pl}	M_{n1}	M_{n2}	M_{n3}
Size (μm)	W=4 L=0.15 M=1	W=0.35 L=20 M=1	W=1 L=0.15 M=1	W=1 L=0.15 M=1	W=0.35 L=0.35 M=1
Device	M_{n4}	M_{n5}	M_{n6}	M_{nl}	C_0
Size (μm)	W=0.6 L=0.35 M=1	W=1 L=0.15 M=1	W=2 L=0.15 M=1	W=0.35 L=20 M=1	W=5 L=5 M=8

Next, in order to simplify the simulation, BOR circuit with DEB_CKT are simulated together, the input of DEB_CKT connects to output of BOR, and this circuit is shown in Fig. 4.8. Similarly, the system-level ESD simulation parameters are loaded into simulator, and then to observe and compare the two waveforms, one is BORB and the other is BORB_DEB. The simulation waveforms are shown in Fig. 4.9 (a) and (b). Similarly, In order to observe the convenience, the waveform of BORB subtracts the waveform of VSS during system-level ESD test, BORB_DEB is still logic "1". Therefore, the new reset method can avoid the microelectronic system reset.

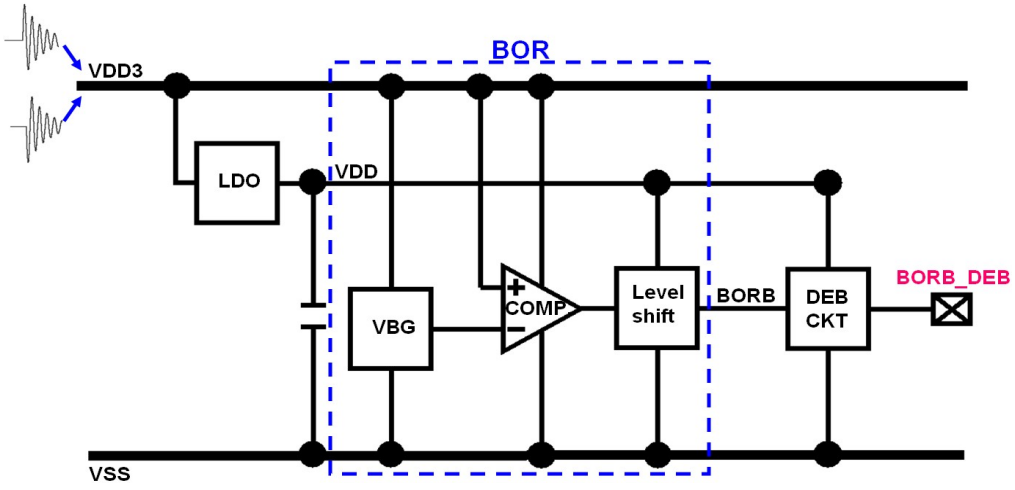


Fig. 4.8 Simple of BOR with DEB_CKT simulation circuit block diagram.

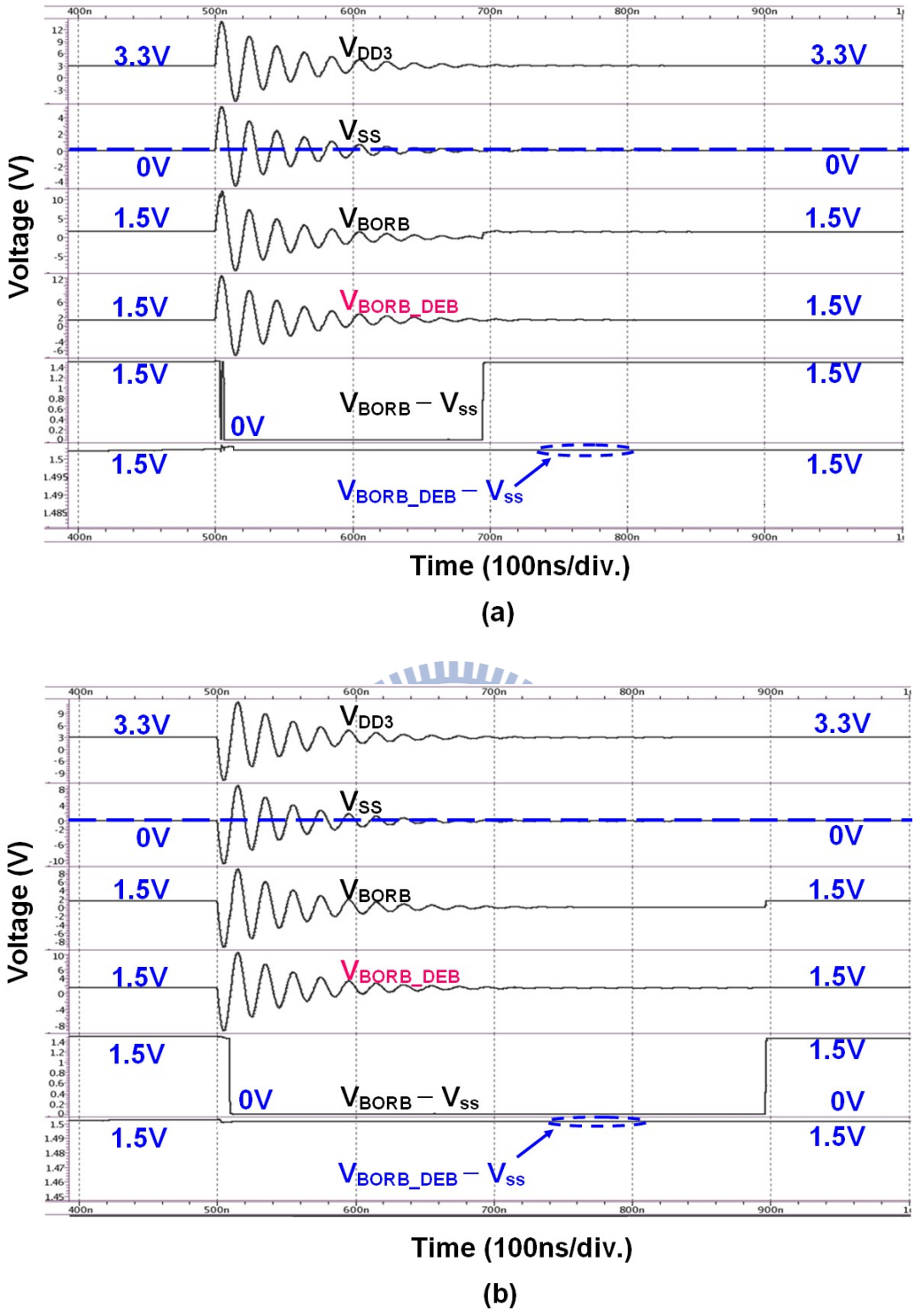
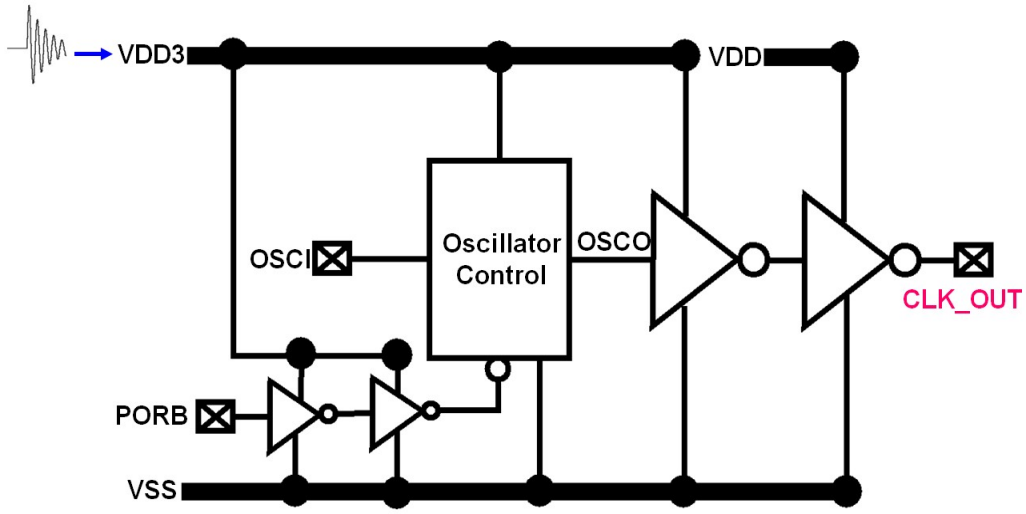


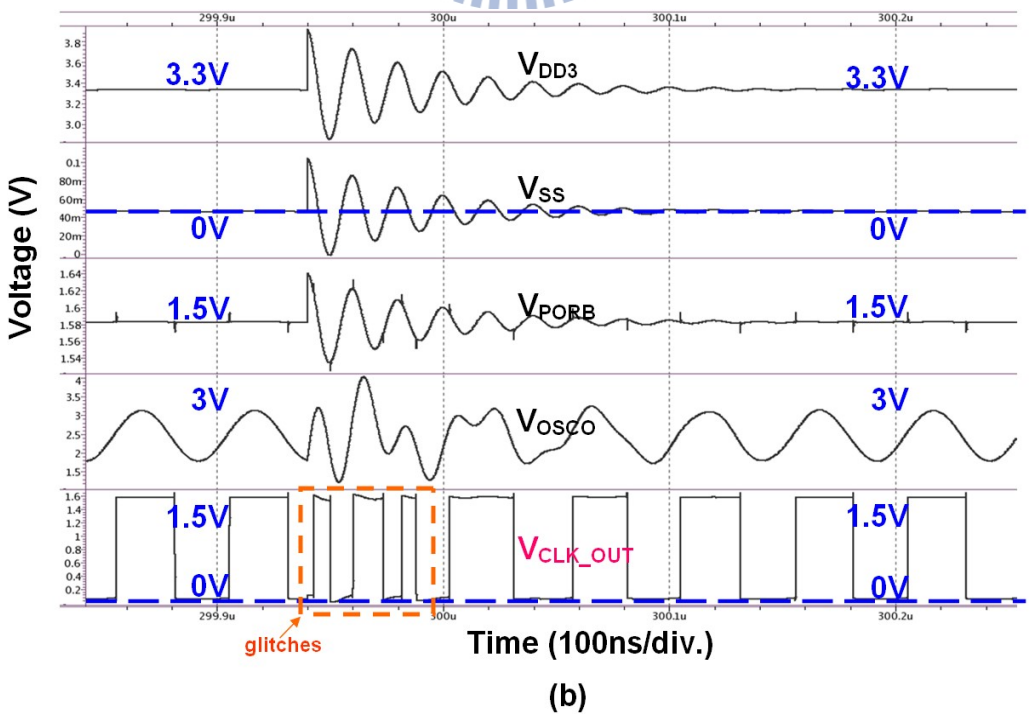
Fig. 4.9 Simulated V_{DD3}, V_{SS}, BORB and BOR_DEB waveforms under (a) positive-going under-damped sinusoidal voltage and under (b) negative-going under-damped sinusoidal voltage.

4.3 New Proposed Method of Hardware / Firmware Co-design

Another problem is the generation of glitches from system clock under system-level ESD or EFT test, the simulation circuit and waveform are shown in Fig 4.10 (a) and (b). These glitches will cause the timing issues and execute unexpected instructions that lead to the microelectronic system to freeze.



(a)



(b)

Fig. 4.10 (a) simple simulation block diagram. (b) Simulated oscillator output waveform under positive-going under-damped sinusoidal voltage.

Under system-level ESD or EFT tests, in order to avoid these glitches which cause the malfunction of the microelectronic system, a new method of hardware / firmware co-design is proposed, and then this firmware flowchart is shown in Fig. 4.11. First, explanation this firmware flowchart, the power-on reset provides a signal, this signal sets the transient detection circuit output to logic '0' during power ramp, therefore, the output of the transient detection circuit is logic "0" in normal operation. When the fast electrical transient happens, the transient detection circuit can detect the occurrence of system-level electrical-transient disturbance and transit the output state to logic "1". At this moment, the system-check Vout is also changed to logic "1", and the firmware executes the stop clock and the count. In the stop clock procedure, before these glitches are generated, CPU clock has been stopped by the output of transient detection circuit. Then, use this procedure, CPU will not execute any instructions, therefore, the microelectronic system will not freeze. Moreover, in the counting procedure, after the counter counts a fixed time, it will provide a signal to restore the CPU clock and reset the output of the transient detection circuit to logic "0" for detecting next ESD events. Whether this method effectively improves the system-level ESD, which is described in the next section.

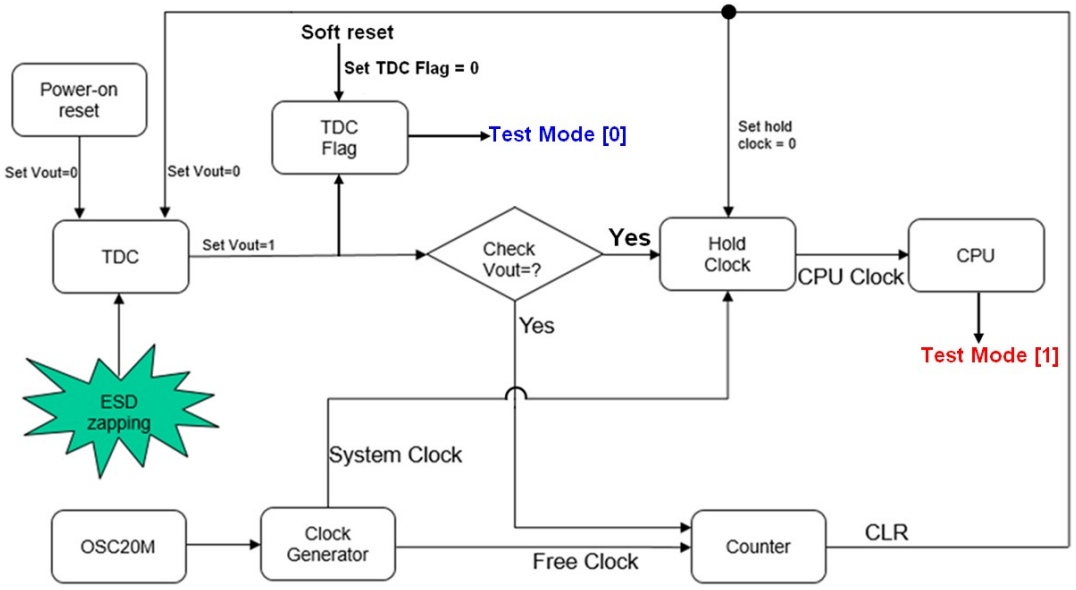


Fig. 4.11 Firmware flowchart to stop system clock when electrical transients happen.

4.4 Experimental Results

The metal layers form parasitic resistors and capacitors in the CMOS IC. These parasitic resistors and capacitors can attenuate the energy of the ESD zapping. If the transient detection circuit is placed on one side of the CMOS IC and then the ESD gun zaps the other side of the CMOS IC, the transient detection circuit may not be able to detect the ESD-induced disturbance. The diagram is shown in Fig. 4.12. Therefore, in order to avoid this situation, the configuration of transient detection circuit will be placed on the four corners of the CMOS IC to increase the detection capability. In addition, to verify the new proposed hardware / firmware co-design structure, this chip is fabricated in a 0.15-μm CMOS process with 3.3-V devices, the chip photo and layout are shown in Fig. 4.13 (a) and (b).

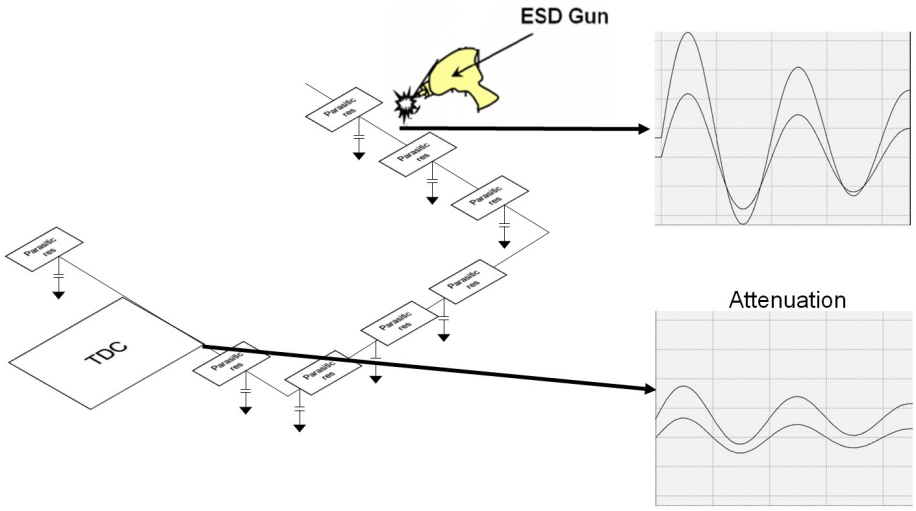
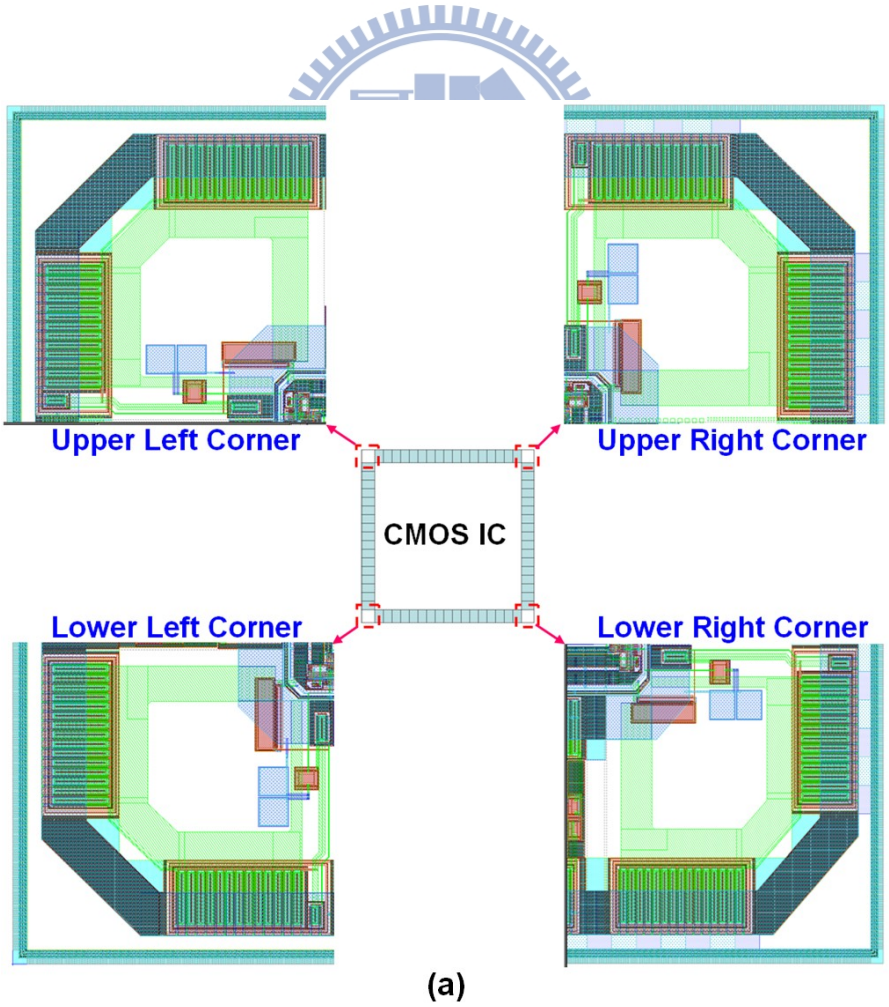


Fig. 4.12 the energy of ESD zapping is attenuated from parasitic capacitor and resistor, the transient detection circuit may not be able to detect the signal.



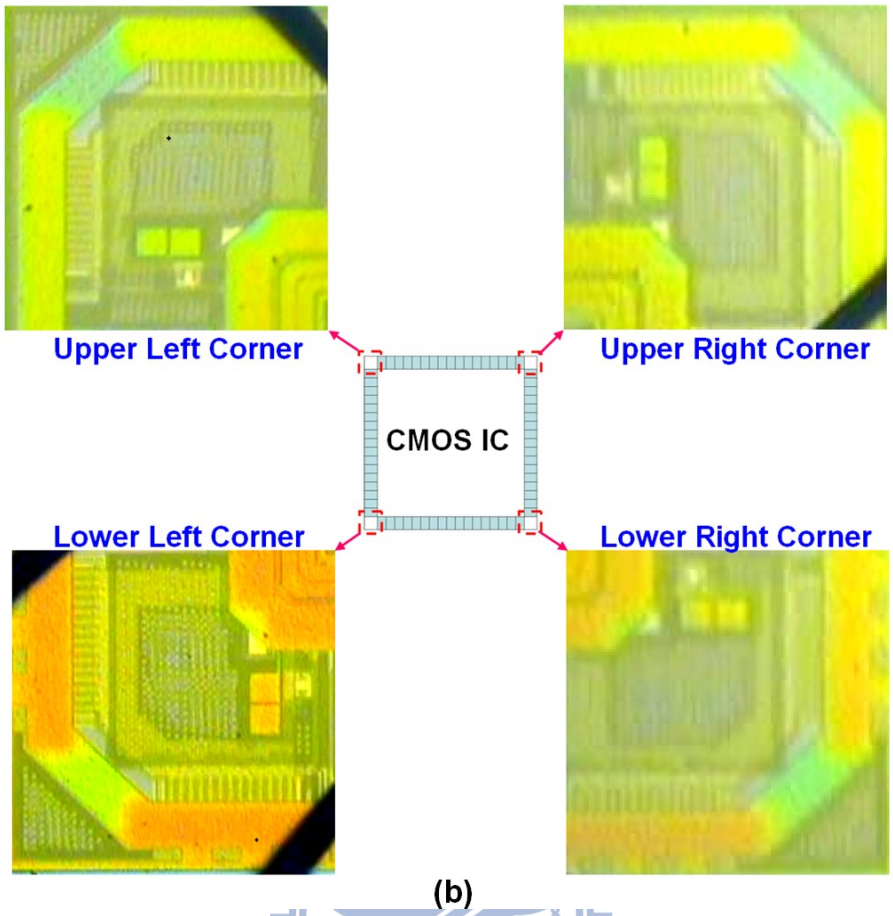


Fig. 4.13 There are four transient detection circuits that placed on the four corners of the CMOS IC, (a) chip layout and (b) photo.

4.4.1 System-level ESD Test on the Evaluation Board

To verify new proposed hardware / firmware co-design under system-level ESD tests, these waveforms are measured by using an evaluation board, as shown in Fig. 4.14. In this design, the stop clock can be set four different time intervals, 1ms, 2ms, 4ms, and 8ms, respectively. Moreover, the purpose of stopping the clock is intended to protect the system operation of the CMOS IC, which is not affected by the ESD zapping during the stop clock to improve system-level ESD or EFT test immunity.

The simple test plan is shown in Fig. 4.15. When the ESD zapping, the firmware receives the logic “1” from the output of the transient detection circuit, at the same time, the

stop clock mechanism is started, immediately. Subsequently, the flag of the transient detection circuit is transferred to logic “1”, but the CPU clock has been stopped, consequently, this signal can be observed after the CPU clock recovery. Once the CPU clock is restored, the output of transient detection circuit will reset to logic “0” at next a clock cycle. There are two signals can measure the waveform by using I/O, one is the CPU clock, the other is the TDC flag, and then the expected waveforms are shown in Fig 4.16.

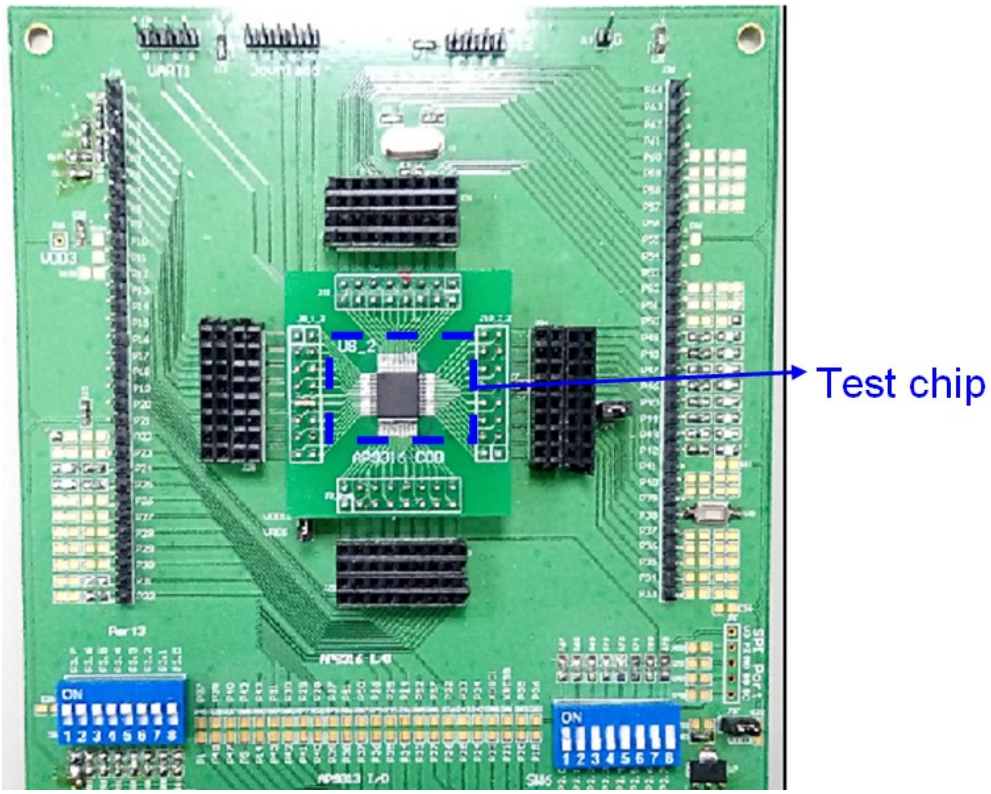


Fig. 4.14 The evaluation board is used to verify new proposed hardware / firmware co-design under system-level ESD tests.

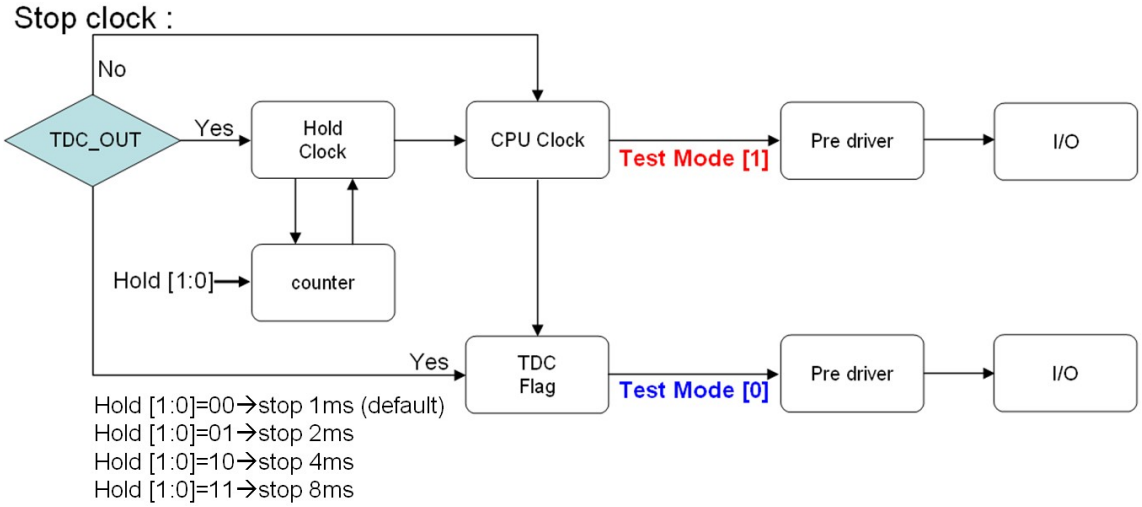


Fig. 4.15 The simple test plan for new proposed hardware / firmware co-design.

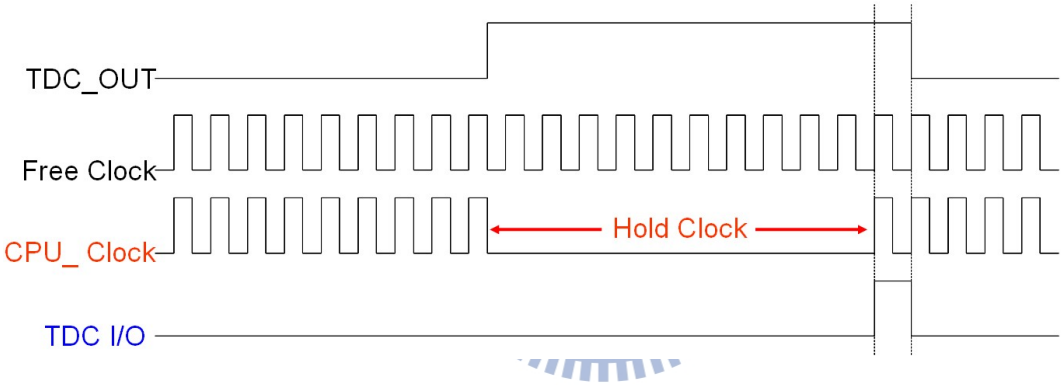


Fig. 4.16 The expected waveforms for new proposed hardware/firmware co-design.

Next, two waveforms have been measured under system-level ESD test, respectively. They are shown in Fig. 4.17. According to the measurement, the CPU clock has been stopped during ESD zapping (+1kV), and the time interval is about 1ms, therefore, the TDC flag can be observed after the CPU clock recovery. At next clock period, the TDC flag is reset to logic "0" again. Moreover, each time interval is also measured, but the measurement at 4ms and 8ms does not meet expectation since the measurement stop time interval is only 3ms and 4.3ms. However, the overall circuit behavior is consistent with the design expectations. These waveforms are shown in Fig. 4.18 (a), (b), (c), and (d). At last, there is one point should be paid attention, the CPU clock is stopped during ESD zapping, its clock status can not be

changed, in this way, the operation system of the CMOS ICs can be maintained during the ESD zapping.

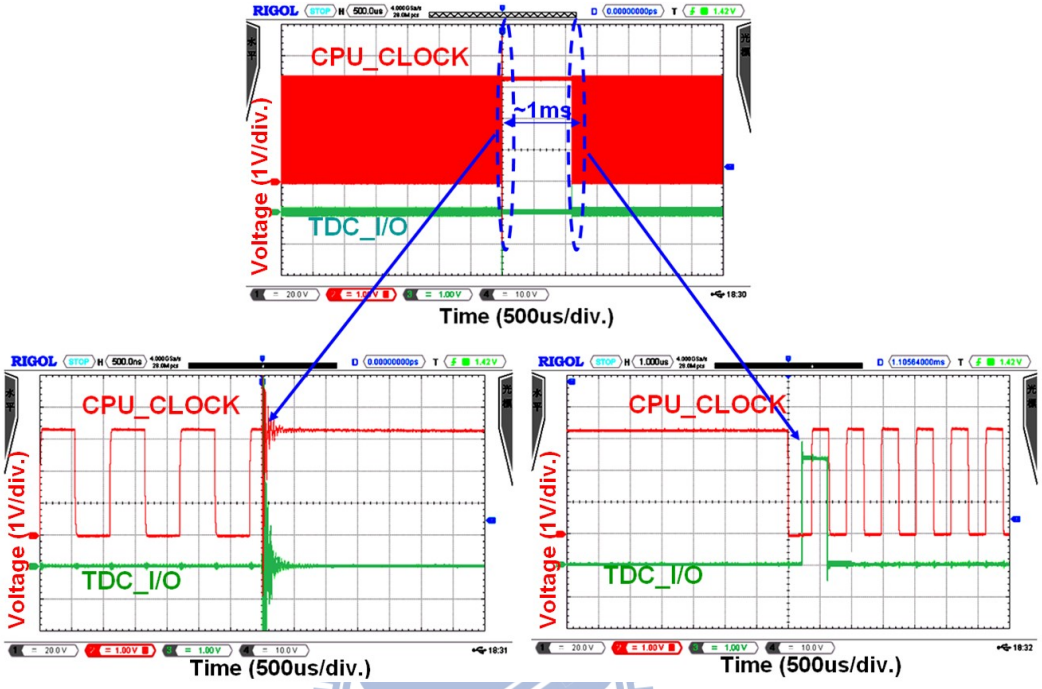


Fig. 4.17 Two waveforms have been measured under system-level ESD test with ESD voltage of +1kV.

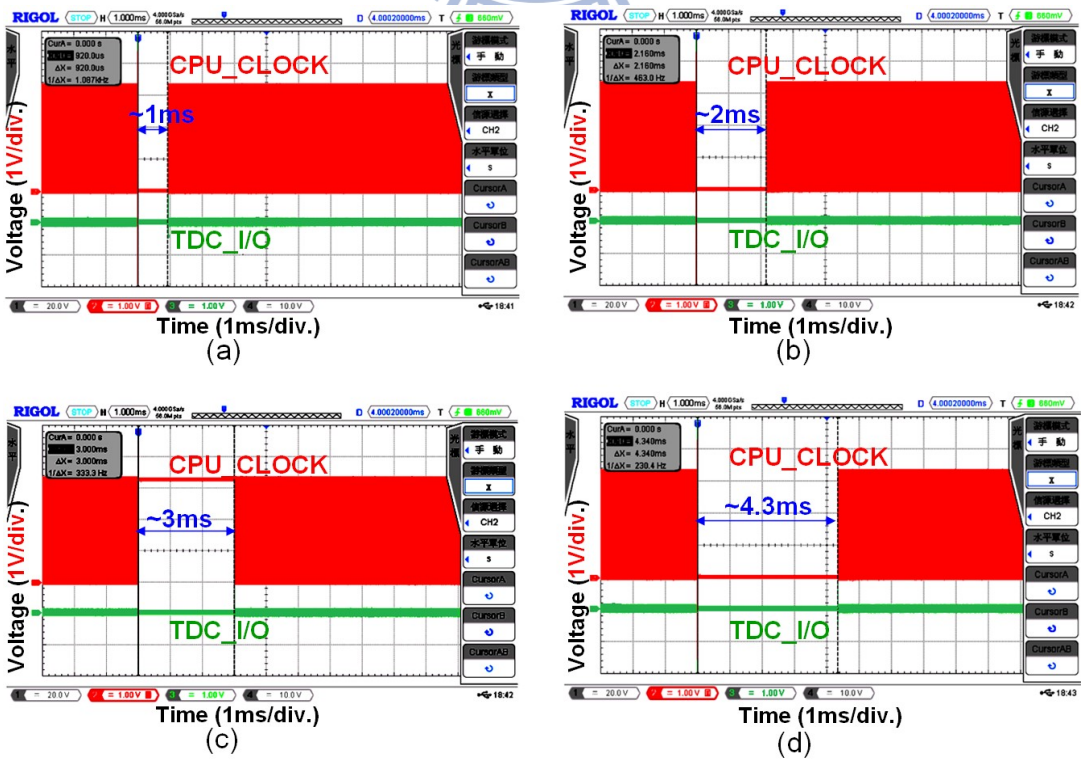


Fig. 4.18 The time interval is measured under system-level ESD test with ESD voltage of +1kV, respectively, (a) 1ms, (b) 2ms, (c) 4ms and (d) 8ms.

4.4.2 System-Level ESD Test on the System Module

In this section, the new proposed hardware/firmware co-design is verified in the system module to measure the system-level ESD immunity, this method is built in the CMOS IC product, and the product number is AP9316. The CMOS IC is configured on the electricity meter, which mainly transmits the electricity data from the household to the power company by using the power lines. Alternatively, by using power lines receive information from the power company. For example, the electricity consumption data is transmitted to the power company to calculate the electricity bill. In this way, it can replace the manual recording the electricity meter to calculate the electricity bill. Therefore, the manual recording time and labor costs can be reduced. At last, in the measurement, the system test module consists of a smart electricity meter, and a system board, as shown in Fig. 4.19.

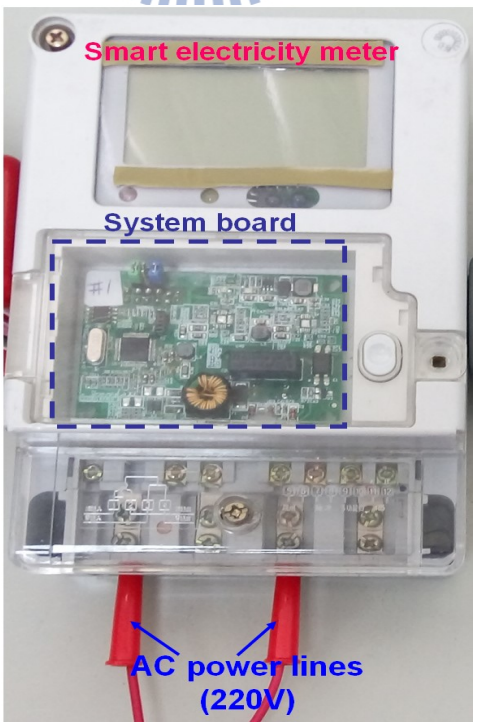


Fig. 4.19 The system test module consists of a smart electricity meter, and a system board.

In order to observe the performance of the system module under system-level ESD tests, there are two indicator lights that are added to the system board, one is the transient detection circuit indicator light, the other is the system operation indicator light. The system module in the normal operation, the system indicator light will remain flashing, and the transient detection circuit indicator light will turn off. When fast electrical transient disturbance is coupled to the power lines of the system module, the CPU clock will be stopped. Therefore, the system indicator light will stop flashing and keep the light on or light off, and at this moment, the indicator light of the transient detection circuit will flash twice, after ESD zapping, the CPU clock back to normal, and then the system indicator light will remain flashing again. The system operation indicator light does not flash after the ESD zapping, it mains that the operation system has been frozen. Conversely, after the ESD zapping, the system operation indicator light remains flashing, it means that the operating system is normal. Therefore, the system operation indicator light can observe the performance of the system module under system-level ESD tests. Moreover, as mentioned in chapter 2, the system board is equipped with a noise filter and TVS to enhance ESD immunity, as shown in Fig. 4.20.

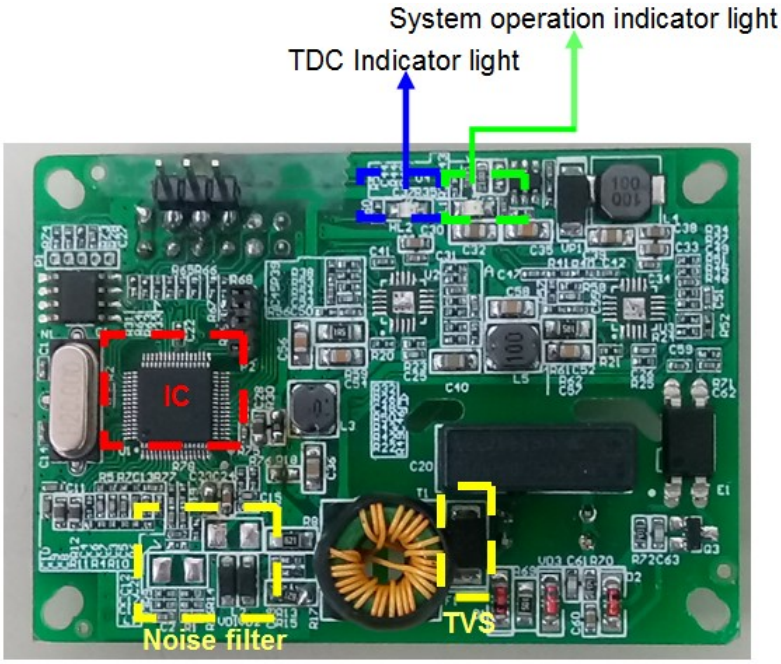


Fig. 4.20 The system board is equipped with a noise filter and TVS to enhance ESD immunity.

To meet the customer requirement, the microelectronic products are required to sustain the ESD-generated voltage of ±12kV under contact-discharge test mode to achieve the immunity criterion of “class B” level in the IEC 61000-4-2 standard. These test points are shown in Fig. 4.21.

First, when the transient detection circuit is disabled, the system will be locked in the frozen state with ESD zaps of ±8kV, it means that the system indicator light does not flash after the ESD zapping, therefore, the operation system is judge to fail. Secondly, when the transient detection circuit is enabled, the system will be locked in the frozen state with ESD zaps of ±16kV. The test results for each test point are listed in table 4.2. According to test results, it has achieved the requirement of the customer, and the new proposed hardware/firmware co-design with transient detection circuit has successfully improved the system-level ESD immunity.

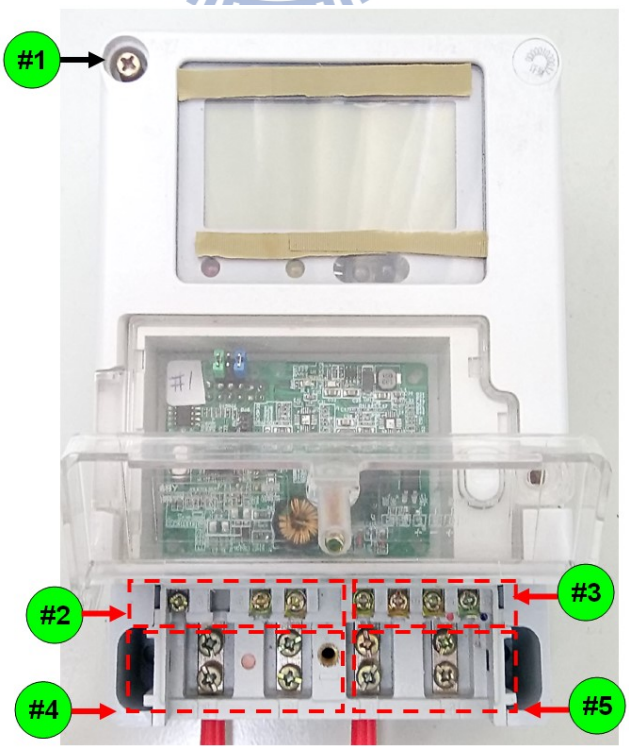


Fig. 4.21 Test points definition on smart meter under system-level ESD tests with contact-discharge test mode.

Table 4.2 System module measurement results, disable and enable the system hardware / firmware co-design, respectively.

Zapping Location	ESD Zapping Voltage = ±8kV	ESD Zapping Voltage = ± 15kV
	Disable the system Hardware/Firmware Co-Design	**Enable** the system Hardware/Firmware Co-Design
#1	**Class B**	**Class A**
#2	**Class C**	**Class A**
#3	**Class C**	**Class A**
#4	**Class C**	**Class A**
#5	**Class C**	**Class A**

4.5 Summary

The new proposed hardware / firmware co-design with the transient detection circuit has been designed and fabricated in a 0.15-μm CMOS process with 1.5-V and 3.3-V devices. In order to enhance the system-level ESD immunity, the system board is equipped with noise filters and TVS to reduce the ESD-induced transient disturbance on the power lines of the CMOS ICs. Under system-level ESD tests, the transient detection circuit is disabled, the system will be locked in the frozen state when ESD zaps to ±8kV. Relatively, the transient detection circuit is enabled, the system-level ESD has increased from ±8kV to ±15kV. Therefore, according to test results, the new proposed hardware / firmware co-design with the transient detection circuit has met the customer's requirements and successfully improved the system-level ESD immunity.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this thesis, a new on-chip transient detection circuit has been proposed in chapter 3. The circuit performances have been investigated by using simulation tool HSPICE. From the simulation results, the output voltage level of transient detection circuit can be changed from logic 0 to logic 1 after system-level ESD and EFT events.

The transient detection circuit has been fabricated in a 0.15-μm CMOS process with 1.5-V devices and 3.3-V devices. From the experimental results in chapter 3, the output of transient detection circuit can transit from 0V to 3.3V when fast electrical transient disturbance is coupled to the power lines.

It has been reported that the hardware and firmware co-design with transient detection circuit to solute the system frozen of the microcontroller or display panel when system-level ESD event happened, in this method, the system could auto-recover from upset to the normal operation, and the system can achieve the criterion of “class B” level in the IEC 61000-4-2 standard.

In order to meet the requirement of the customer to achieve contact discharge ±12kV and the criterion of “class B” level in the IEC 61000-4-2 standard. In chapter 4, a novel proposed hardware / firmware co-design with transient detection circuit has been fabricated in a 0.15-μm CMOS process with 1.5-V and 3.3-V devices. According to the measurement results, if the transient detection circuit is turned off, the system will be locked in the frozen state when ESD zaps to ±8kV. Relatively, if the transient detection circuit is turned on, the

system-level ESD has been increased from ±8kV to ±15kV, it has achieved the requirement of the customer, and successfully improved the system-level ESD immunity.

5.2 Future Work

In this thesis, the transient detection circuit is arranged on the I/O, therefore, it needs to be far from the oscillator circuit to prevent the transient detection circuit from being triggered.

In system applications, the hardware and firmware co-design with transient detection circuit to stop the CPU clock, to prevent the CPU from executing the program due to glitches. However, from experiment results, when the ESD zaps to ±16kV, the operation system has been frozen to lead to malfunction of the CMOS IC. Therefore, how to solve the system failure to improve the system-level ESD test level, it should be further investigated.

Symbol Description

CDM : Charged Device Model.

DUT : Device Under Test.

EOS : Electrical Over Stress.

ESD : Electrostatic Discharge.

EFT : Electrical fast transient.

HBM : Human Body Model.

MM : Machine Model.

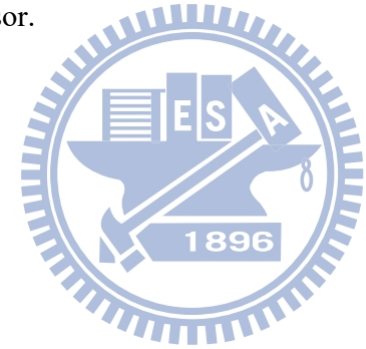
TVS : Transient voltage suppressor.

kV : kilo voltage.

μs : microsecond.

ms : millisecond.

ns : nanosecond.



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