國立交通大學

電子研究所

博士論文

高壓製程之靜電放電防護設計與閂鎖效應防制研究

ESD Protection Design and Latchup Prevention in High-Voltage BCD Technology

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指導教授：柯明道 (Ming-Dou Ker)

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高壓製程之靜電放電防護設計與閂鎖效應防制研究

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摘要

隨著高壓製程積體電路於車用電子、面版驅動電路、電源供應器及電源管理等應用的普及化，靜電放電防護能力已成為影響電子產品可靠度的主要因素之一。對於使用在這些應用的輸出輸入介面和作為靜電放電保護元件的高壓擴散式金氧半電晶體(laterally diffused MOS, LDMOS)而言，除了電晶體本身複雜的元件結構外，其高觸發電壓(trigger voltage)及低持有電壓(holding voltage)的特性，往往使得高壓積體電路的靜電放電防護能力不足，並有可能產生閂鎖效應(latchup)或類似閂鎖效應(latchup-like)的危險。因此如何開發有效的靜電放電防護設計，是目前這些高壓積體電路設計上的重要課題之一。

傳統上，矽控整流器(Silicon-Controlled Rectifier, SCR)因其良好的靜電放電耐受能力而被廣泛作為靜電放電防護元件使用，但由於雙載子注入效應(double carrier injection) 和正回授機制導致的低持有電壓特性，使其困擾於閂鎖效應的風險而難以廣泛應用於高壓積體電路。因此，第二章中提出了一個具有高持有電壓的新型矽控整流器，藉由在其佈局中加入寄生雙載子電晶體(Bipolar Junction Transistor, BJT)結構，可以有效破壞矽控整流器中固有之正迴授路徑，進而提高其持有電壓。另外，有鑑於閂鎖效應為毫秒等級的可靠度測試，針對高壓元件使用傳輸線脈衝系統(Transmission-Line-Pulsing system)量測得到的持有電壓已不具備說服力，因此直流曲線分析儀(DC curve tracer)和暫態觸發閂鎖效應測試(transient-induced latchup test)也被使用來驗證新型矽控整流器的閂鎖效應免疫能力，此新型矽控整流器已於一個 0.25 微米高壓 BCD (Bipolar CMOS DMOS)製程中獲得實驗驗證。

在高壓積體電路製程技術中，為了使高壓電晶體能承受高操作電壓，製程上的複雜度與確保高壓元件可靠度的困難度也隨之增加，如何提高靜電放電防護元件的耐受能力並同時避免閂鎖效應的發生，往往具有相當的困難度與挑戰。因此，第三章提出

使用堆疊架構的低壓電晶體作為高壓積體電路的靜電放電防護元件，不僅能避開高壓製程複雜度所導致的可靠度問題，也能藉由堆疊架構針對不同操作電壓調整堆疊個數以符合應用所需之靜電放電防護設計窗口，其靜電放電防護能力已於一個 0.25 微米高壓 BCD 製程中獲得實驗驗證，能防護一個監測車用電池模組積體電路之高壓輸入端抵抗高達八千伏特的人體靜電放電模式(Human Body Model, HBM)靜電轟擊。另外，傳統不同操作電壓之電路區塊一般由各自相對應的高壓元件提供靜電放電防護，因此本章節也提出了共享路徑(sharing path)的概念，單一串堆疊之低壓電晶體能夠提供數個不同操作電壓區塊的靜電放電防護，不需額外設計相應之高壓元件，如此不僅能大幅減少佈局面積，降低晶片製造成本，也能提供有效率的靜電流泄放路徑，進一步增加全晶片的靜電放電防護能力。

本論文第四章開始為高壓製程佈局結構之閂鎖效應防制研究。閂鎖效應是 CMOS 積體電路產品設計上一項常見的問題，嚴重時可導致晶片損毀無法正常工作，由於高壓積體電路製程的額定電源、供應電壓一般皆高於數十伏特，在高壓積體電路中寄生的矽控整流器，其持有電壓一般皆遠低於其額定電源供應電壓，這意味著閂鎖效應在高壓積體電路中往往是難以避免的，導致閂鎖效應在高壓積體電路中扮演著一個極關鍵的角色。本章節即針對各種不同的元件結構及佈局參數對於閂鎖效應敏感度的相互關係進行研究，藉由不同佈局測試結構與實驗結果驗證，可進一步評估萃取出能通用在高壓積體電路中的閂鎖效應防制之佈局準則。

目前發展的系統單晶片積體電路為了符合產品需求，其系統具有多種電壓準位和不同功能之積體電路，而為了防止不同電路區塊間發生閂鎖效應導致電路功能損毀，不同電壓區塊間需要制訂相關之佈局準則。第五章即針對可能潛在於高壓 BCD 製程中高壓和低壓電晶體間的寄生閂鎖效應路徑進行研究。在實驗結果中發現了具有低持有電壓的寄生矽控整流器(SCR)路徑，它可能會影響 CMOS 積體電路產品的靜電放電耐受度，因此，高壓和低壓元件間的佈局準則應嚴謹定義，以避免寄生路徑的發生。

最後，第六章總結了本篇論文的主要結果，並且提出一些關於未來可以持續進行研究的討論。本論文所提出的新型元件設計與測試結構皆搭配實體晶片進行驗證，所有研究成果皆已發表於國際期刊或國際知名學術會議。

ESD Protection Design and Latchup Prevention in High-Voltage BCD Technology

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Abstract

Nowadays, the smart power technology has been developed and used to fabricate the display driver circuits, power switch, motor control systems, and so on. However, the process complexity and the reliability of high-voltage (HV) devices have become more challenging compared with the low-voltage (LV) devices. Among the various reliability specifications, on-chip electrostatic discharge (ESD) protection has been known as one of the important issues in HV integrated circuits (ICs). ESD is an inevitable event during fabrication, packaging and testing processes of integrated circuits. ESD protection design is therefore necessary to protect ICs from being damaged by ESD stress energies.

In Chapter 2, the modified silicon-controlled rectifier (SCR) fabricated in a 0.25-μm HV Bipolar-CMOS-DMOS (BCD) technology has been proposed to seek for both effective ESD protection and latchup immunity. Experimental results show that one of the proposed SCRs has a high holding voltage of up to ~30 V in the 100-ns Transmission- line-pulsing (TLP) measurement results. However, through the experimental verification by using transient-induced latchup (TLU) test, the holding voltage of such proposed device decreases to ~20V. It is due to the increased bipolar junction transistor (BJT) current gains of the SCR path induced by the Joule heating effect in the long-term measurement. Such phenomenon

is an unavoidable issue that should be carefully taken into consideration when applying SCR device for ESD protection in the HV applications.

In Chapter 3, an on-chip ESD protection solution has been proposed in a 0.25-μm HV BCD process by using LV devices with stacked configuration For HV applications. Experimental results in silicon chip have verified that the proposed design can successfully protect the 60-V pins of a battery-monitoring IC against over 8-kV human-body-model (HBM) ESD stress. Moreover, stacked LV devices with sharing path technique can be more area-efficient to implement the whole-chip ESD protection in the HV CMOS ICs.

In Chapter 4, the optimization of guard ring structures to improve latchup immunity in an HV double-diffused drain MOS (DDDMOS) process with the DDDMOS transistors has been investigated in a silicon test chip. The measurement results demonstrated that the test devices isolated with the specific guard ring structure of n-buried layer can highly improve the latchup immunity.

In Chapter 5, the latchup path which may potentially exist at the interface between HV and LV circuits in a HV BCD technology has been investigated. Owing to the multiple well structures used to realize the HV device in the BCD process, the expected latchup path in the test structure was hardly triggered. However, a parasitic SCR path featuring a very low holding voltage is found in the experiment silicon chip. It may influence the ESD robustness of CMOS IC products with the HV and LV circuits integrated together. Thus, the layout rules at HV and LV interface should be carefully defined to avoid the occurrence of unexpected parasitic path.

Chapter 6 summarizes the main results of this dissertation, where the future works based on the new proposed designs and test structures are discussed as well. The related works in this dissertation have been published in several international journals or conferences.

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戴　嘉　岑

謹誌於竹塹交大

民國一零六年十二月

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Chapter 1

Introduction

In this chapter, the background and the organization of this dissertation are provided. First, the applications of high-voltage (HV) technologies are briefly introduced. Then, in addition to reviewing the test standards of electrostatic discharge (ESD) related to this dissertation, the on-chip ESD protection considerations and challenges in HV technologies are introduced. Finally, the organization of this dissertation is described.

1.1 Applications of High-Voltage Technologies

Recently, HV technologies are extensively utilized in various applications, such as automotive electronics, display drivers, power managements, and so on. The applications for HV devices can be classified into four categories in terms of their current and voltage handling requirements [1]. The first category has low operating current levels below 1 A. Typical examples include the telecommunications and display drivers. In these applications, integrating multiple small-size transistors on a single chip for more functionality is feasible to provide a cost-effective solution. The second category is applications with relatively low operating voltages below 100 V. Typical examples are automotive electronics and power supplies for computers. For these applications, the silicon power MOSFET with the characteristics of low on-resistance and fast switching speed are mainly used. The third category has high operating voltages above 200 V. Lamp ballasts, consumer appliances, and electric vehicle drivers are examples for this category. Some special power transistors such as insulated gate bipolar transistor (IGBT) are developed because the on-resistance of silicon power MOSFET is too large for these applications. The fourth category has very high operating voltages above 5000 V. High power motor controls in power transmission and distribution systems are examples for

this category. The silicon power MOSFET and IGBT are used to replace the traditional silicon power thyristor because of their greater characteristics for these applications.

1.2 General ESD Protection Design in CMOS Integrated Circuits

In semiconductor industry, electrostatic discharge (ESD) is one of the most universal reliability threats to the semiconductor products. ESD are typically discharged in few nanoseconds with thousands of volts and peak currents of several amperes, which can harm the internal electronic components of semiconductor products [2]. Effective ESD protection designs have been essential, not just optional, for the CMOS integrated circuit (IC) products used in analog, digital, power, RF, optoelectronic, and biomedical applications. To predict and qualify the ESD robustness level of IC products, there are three component-level models proposed and standardized to simulate the typical ESD events that happen during fabrication, package, and assembling process of IC products. The first model, human-body model (HBM), simulates the static charges stored in human body being discharged through a packaged IC to ground [3]. The second model, machine model (MM), simulates the ESD events discharging from handling machines or testing equipment through a packaged IC to ground [4]. The third model, charged-device model (CDM), simulates the discharging of charges accumulated in the substrate of packaged IC by triboelectric effect or induction during IC manufacturing [5]. General commercial requirements for the IC products are requested to sustain at least 2-kV HBM, 200-V MM, and 500-V CDM ESD stresses.

Because any input/output (I/O), power (VDD), or ground (VSS) pins of a packaged IC can be randomly zapped to the grounded pins during ESD events, on-chip ESD protection design is required for every pin against ESD damage [6]. Fig. 1.1 shows a typical whole-chip ESD protection network for general CMOS ICs. ESD protection elements are placed near I/O pins to divert ESD currents to the power rails. The power-rail ESD clamp circuit placed between VDD and VSS rails is able to provide an efficient low-impedance path for discharging ESD

current and should be kept off for blocking DC operating voltage. This ESD protection network can protect the internal circuits from ESD damages between any pin-to-pin combinations.

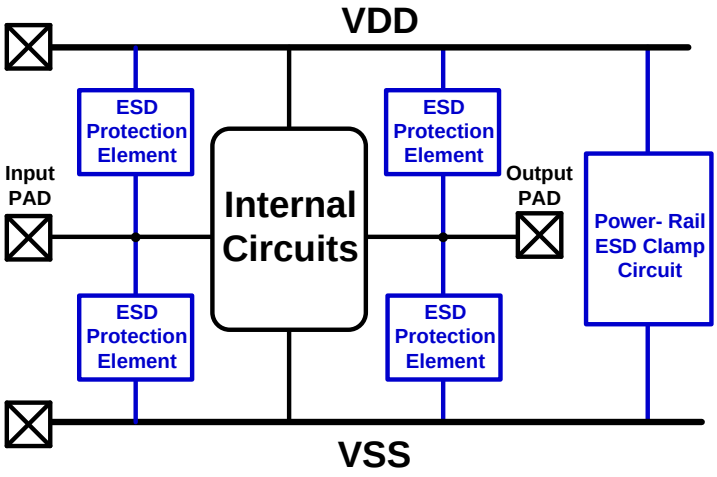


Fig. 1.1. Scheme of typical whole-chip ESD protection network for general CMOS ICs.

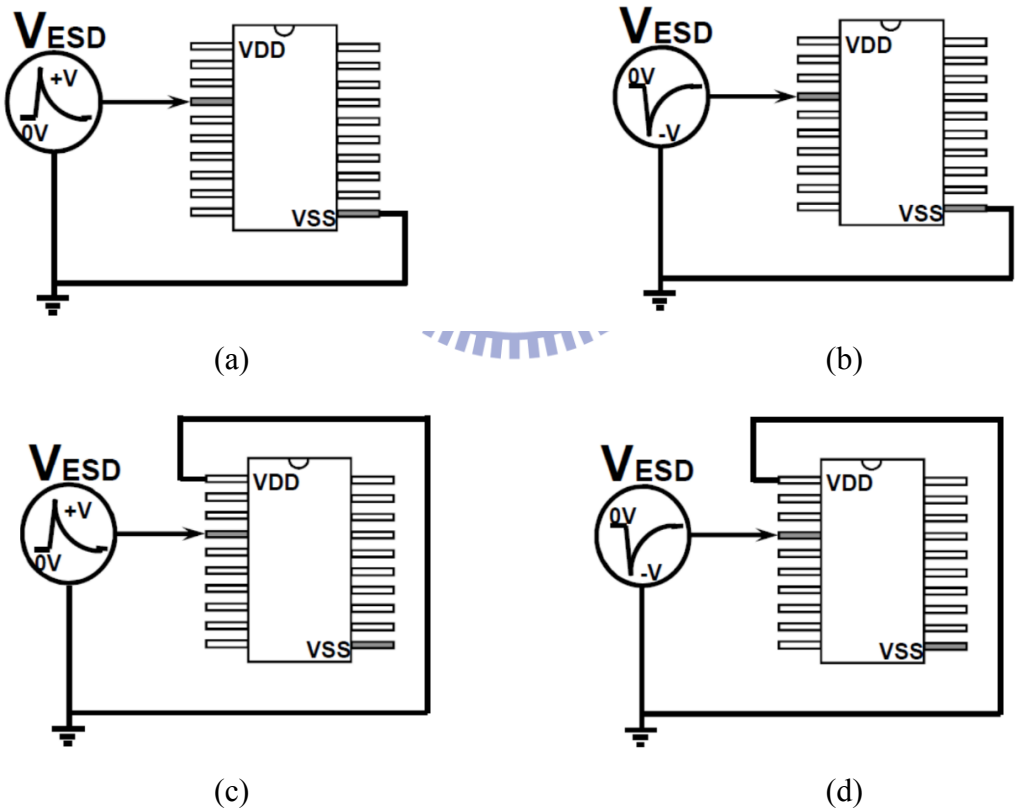
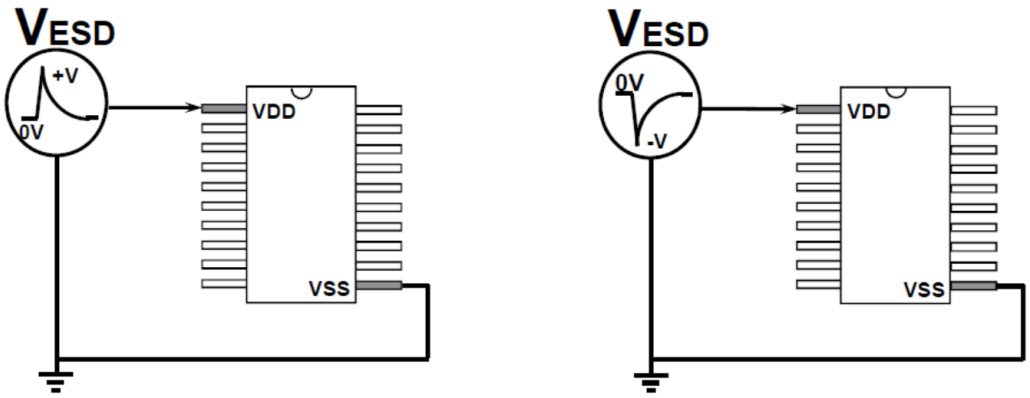


Fig. 1.2. ESD test modes for I/O pins of a packaged IC with (a) positive-to-VSS (PS), (b) negative-to-VSS (NS), (c) positive-to-VDD (PD), and (d) negative-to-VDD (ND).



(a) (b)

Fig. 1.3. ESD test modes with (a) positive and (b) negative ESD stresses between power pins.

In addition, since ESD stresses would be either positive or negative, four tests modes at I/O pins with respect to the grounded VDD or VSS pins, such as PS (positive-to-VSS), NS (negative-to-VSS), PD (positive-to-VDD), and ND (negative-to-VDD), are specified in the ESD test standards as shown in Fig. 1.2. The ESD stresses between VDD and VSS pins are also specified to verify the whole-chip ESD protection capability, as shown in Fig. 1.3.

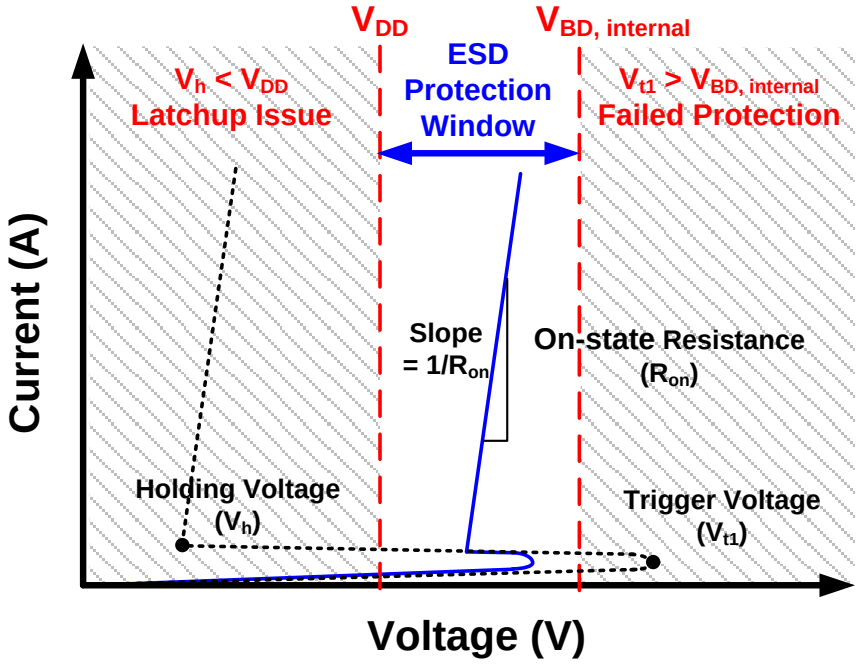


Fig. 1.4. Typical ESD protection design window for general CMOS ICs.

To guarantee the effectiveness of ESD protection design, the I-V characteristics of ESD protection devices should fit into the ESD protection design window, as the blue curve illustrated in Fig. 1.4 [7]. Breakdown voltage (V_{BD}) and supply voltage (VDD) of internal circuits divide the plot into three parts. To get successful ESD protection, the trigger voltage (V_{t1}) should be smaller than the breakdown voltage of internal circuits. Furthermore, to avoid latchup or latchup-like issue, the holding voltage (V_{hold}) should be greater than the supply voltage of internal circuits. The on-state resistance (R_{on}) of the ESD protection device should be as small as possible for an efficient ESD protection.

1.3 ESD Protection Considerations in High-Voltage Technologies

With the characteristics of high power consumption and harsh operating environment in the various HV applications, HV CMOS ICs are in urgent need of rigid reliability designs. HV transistors are developed to sustain operating voltages from several tens to more than thousands of volts, but their ESD robustness doesn't scale with the rated blocking voltage. Due to the complicated device structures in HV processes, guaranteeing the ESD robustness of HV transistors is much more challenging than for low-voltage (LV) transistors.

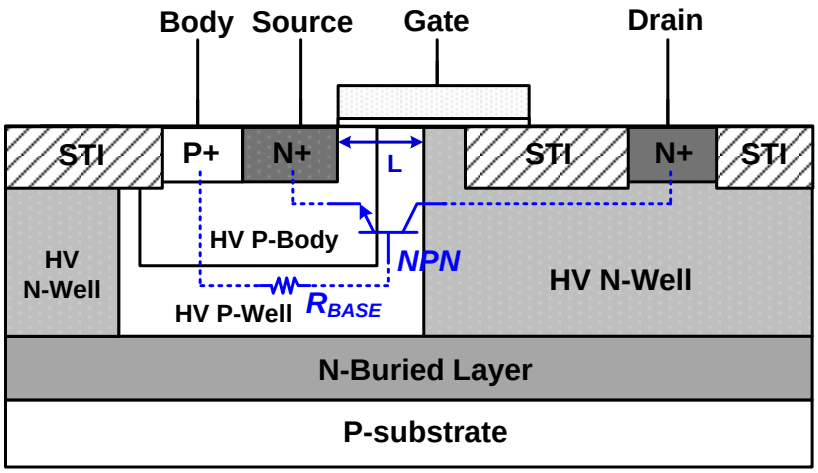


Fig. 1.5. Device cross-sectional view of 60-V nLDMOS in a 0.25-μm HV BCD process.

Traditionally, the HV transistor like Laterally-Diffused MOS (LDMOS) was often adopted as on-chip ESD protection device in the HV applications [8]. For example, Fig. 1.5 shows the device structure of a traditional 60-V n-type LDMOS (nLDMOS) fabricated in a 0.25-μm HV Bipolar-CMOS-DMOS (BCD) process. Fig. 1.6 shows the I-V characteristics of gate-grounded 60-V nLDMOS measured by Transmission-Line-Pulsing (TLP) system. TLP system has been extensively used as an analysis tool to complement the HBM and MM ESD test results. The holding voltage of nLDMOS after snapback breakdown was smaller than the circuit operating voltage. During normal circuit operation, the noise might unpredictably trigger the parasitic NPN bipolar junction transistor (BJT) inherent in the nLDMOS, and the supply voltage keeps the parasitic BJT turned on continuously. Such HV ESD device would be easily burned out after a period of time under the circuit normal operating condition. Thus, the nLDMOS was very susceptible to latchup-like issue. Moreover, in [8], the ESD robustness of nLDMOS doesn't linearly increase as the enlargement of device dimension. The nLDMOS may cause multi-finger non-uniform turn-on effect due to its low holding voltage. The parasitic BJT inherent in the nLDMOS are often unevenly triggered after snapback breakdown. Accordingly, a large-size nLDMOS often exhibits poor ESD protection level when used as an on-chip ESD protection device.

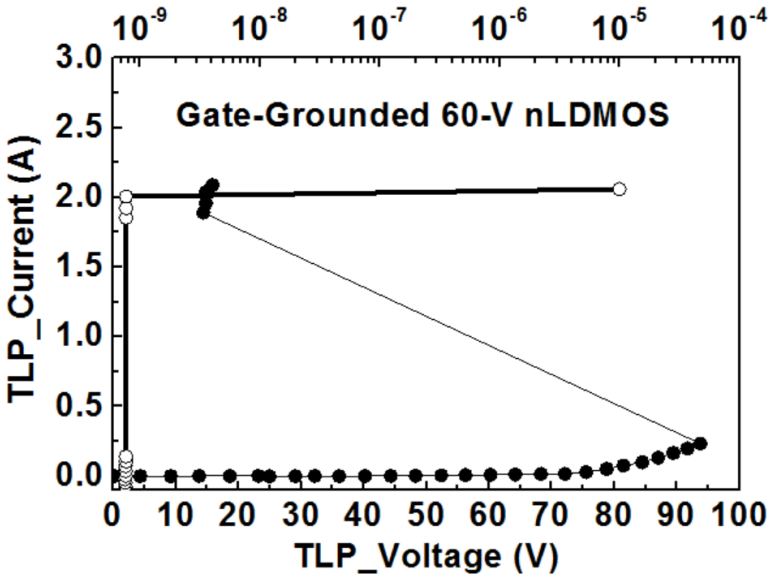
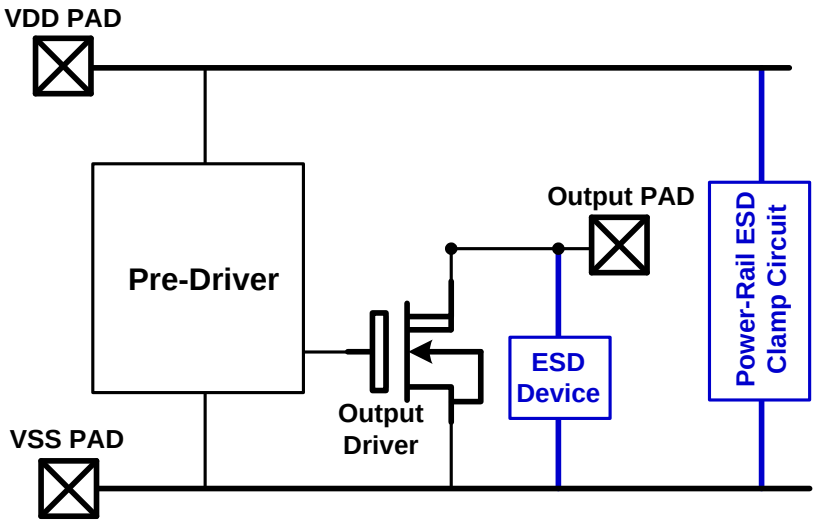
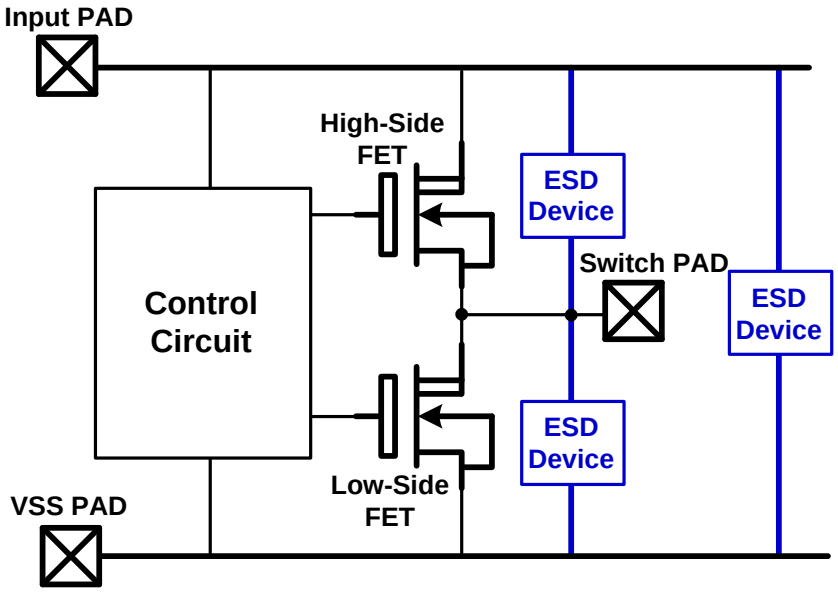


Fig. 1.6. I-V characteristics of gate-grounded 60-V nLDMOS measured by TLP system.



(a)



(b)

Fig. 1.7. ESD protection scheme for the applications of (a) LED driver and (b) DC-DC buck converter.

In some HV applications, the additional ESD protection elements are placed in parallel with the output driver. For example, the simplified circuit diagrams of ESD protection schemes for LED driver and DC-DC converter are illustrated in Figs. 1.7(a) and 1.7(b), respectively. The ESD protection strategies are greatly impacted by the circuit specifics. In Fig. 1.7(a), it should be noticed that the power-rail ESD clamp circuit is unable to discharge ESD current when ESD

stress zaps at the output pin with respect to the grounded VSS pin. The ESD device at the output pin has to take all the ESD current. In Fig. 1.7(b), the ESD protection considerations for the high operating voltage and fast switching pin with narrow ESD protection design window often create significant challenges to ESD design engineers. Thus, the solutions for on-chip ESD protection design in the HV applications are valuable and strongly requested by the IC industries.

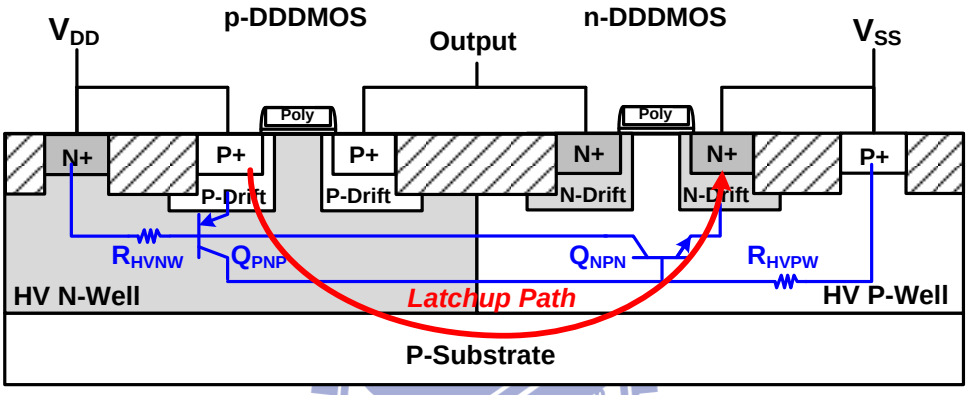


Fig. 1.8. Device cross-sectional views of p-DDDMOS and n-DDDMOS transistors in a HV DDDMOS process, where the latchup path is formed by two parasitic BJTs, a vertical PNP BJT (Q_{PNP}) and a lateral NPN BJT (Q_{NPN}).

1.4 Latchup Issue in High-Voltage Technologies

When HV devices are used in HV CMOS ICs, it is difficult to eliminate the possible occurrence of latchup or latchup-like issue induced by the external glitches or inductive load [9], [10]. Latchup originates from the parasitic P–N–P–N structure in the bulk CMOS technology, which can be modeled as two cross-coupled PNP BJT (Q_{PNP}) and NPN BJT (Q_{NPN}). Fig. 1.8 shows an example of the parasitic latchup path that potentially exists between p-DDDMOS and n-DDDMOS transistors in a HV double-diffused drain MOS (DDDMOS) process. This parasitic latchup path may be accidently fired if the transient overshooting or undershooting noise appears at power (VDD), ground (VSS), or input/output (I/O) pads. Once

such parasitic latchup path is triggered, it will dominate the circuit function, and a huge current will be induced by the positive feedback regeneration from those two parasitic BJTs. Consequently, this huge current may result in the circuit malfunction or even worse chip burn-out danger.

Latchup in HV CMOS ICs usually suffers worse situation than LV CMOS ICs because of the high circuit-operating voltage and multi-layer structure. If latchup or latchup-like issue is initiated by any latchup-triggering events, HV CMOS ICs are often seriously damaged by the latchup-generated high power. Therefore, improving the latchup immunity is one of major reliability issues in HV CMOS ICs.

1.5 Dissertation Organization

The traditional HV ESD protection devices such as LDMOS perform poorly and suffer latchup-like risk in the HV BCD process mainly because of the low holding voltage and weak ESD robustness. This dissertation explores different design alternatives to achieve efficient ESD protection level, with focus on the increment of holding voltage as well as the consumption of silicon area. In addition, the ESD levels of the proposed ESD protection devices in this dissertation are only judged by using the HBM ESD tester for a basic verification.

Chapter 2 presents a new layout structure to increase the holding voltage of traditional SCR device for HV applications. By adding parasitic BJT structure into the traditional SCR device, the double-carriers injection and positive feedback in this proposed SCR can be suppressed. In addition, whereas latchup event is a reliability issue with the time duration longer than milliseconds, the I–V characteristics of the proposed SCR are also measured by DC curve tracer (Tek370B) to validate its holding voltage. Furthermore, transient-induced latchup (TLU) test is applied to verify the measurement results [11].

Chapter 3 presents an on-chip ESD protection solution by using LV p-type devices with

stacked configuration For HV applications. The ESD performance of stacked LV devices will be compared with the new proposed HVSCR in Chapter 2. Moreover, the proposed ESD protection design using stacked LV devices has been verified to protect the HV pins of a battery-monitoring IC under HBM ESD stress.

Chapter 4 presents the investigation of guard ring structures to improve latchup immunity in an HV DDDMOS process with the DDDMOS transistors. The latchup immune levels of test devices which are isolated with different guard ring structures of n-buried layer will be verified by using latchup trigger current test.

Chapter 5 presents the investigation of a latchup path which may potentially exist at the interface between HV and LV circuits in a HV BCD technology. The DC curve tracer (Tek370B) is used to verify the I–V characteristics of such parasitic path. Furthermore, the measurement results are verified by the TLU test.

Finally, summary for the main results of this dissertation is in Chapter 6. Discussions about the future works and the extension based on this dissertation are also arranged in this section.

Chapter 2

Study of High-Holding-Voltage SCR for ESD Protection and Latchup immunity in High-Voltage BCD Process

2.1 Background

The HV technology has been widely used in power management, driver ICs, and automotive electronics. In these HV IC products, ESD is one of the major reliability issues. To protect the internal circuits successfully, the characteristics of on-chip ESD protection elements must be within the ESD protection design window. Due to the high supply voltage and structure complexity of HV devices, it is more challenging to guarantee the reliability of on-chip ESD protection element for HV applications than that for LV applications.

Traditionally, LDMOSs, BJTs, and SCR devices had been adopted as on-chip ESD protection devices in HV technologies [12]-[14]. Some prior works focused on analyzing and improving the ESD robustness of LDMOS with embedded SCR in HV BCD processes [15], [16]. However, the holding voltage of LDMOS with the embedded SCR under a snapback breakdown condition is much lower than the supply voltage. Although the ESD robustness is significantly improved, such a characteristic of low holding voltage would make the HV ICs vulnerable to the latchup risk during normal circuit operations in a noisy environment. The latchup issue often results in IC function failure or destruction. This shortcoming motivated the development of the ESD protection device with latchup-free immunity. Some prior studies had reported that using weak-snapback HV device as the ESD protection element is easily adjusted to fit the requirement [17]–[19].

In this chapter, a modified SCR fabricated in a 0.25-μm HV BCD technology has been proposed to seek for both effective ESD protection and latchup immunity. One of the proposed

SCRs can achieve high holding voltage of up to ~30 V in the 100-ns TLP measurement results. Moreover, whereas latchup event is a reliability issue with the time duration longer than milliseconds, the I–V characteristics of the proposed SCRs are also measured by DC curve tracer (Tek370B) to validate their holding voltage. Furthermore, transient-induced latchup (TLU) test is applied to verify the measurement results.

2.2 Turn-on Operation of Traditional SCR

Traditional SCR is formed with p-n-p-n structure, which could be equivalent as a cross-coupled n-p-n and p-n-p BJTs. The device cross-sectional view and its equivalent circuit diagram in a CMOS technology are illustrated in Fig. 2.1. The p-n-p (Q_{PNP}) and n-p-n (Q_{NPN}) BJTs share the n-well and p-well regions as their collector and base regions. The junction between n-well and p-well is reversely biased with a space-charge region in the SCR structure. The collector current of each BJT acts as the base current for the opposite one. To switch an SCR device into its forward conducting state, the product of current gains of the cross-coupled BJTs has to be larger than or equal to one, i.e.,

$$\beta_{p-n-p} \cdot \beta_{n-p-n} \geq 1 \ . \tag{2.1}$$

The typical I–V characteristic of traditional SCR is drawn in Fig. 2.2. V_{trig} (I_{trig}) and V_{hold} (I_{hold}) are referred to as the trigger voltage (current) and holding voltage (current), respectively. According to the previous studies [1]-[5], the holding voltage (V_{hold}) of SCR device can be expressed as

$$V_{Hold} = V_p + V_n + \iint \frac{q}{\varepsilon_s}[p - n + N_D - N_A]dxdx' + \int \frac{J}{q(nu_n + pu_p)}dx \ . \tag{2.2}$$

The first and second terms, V_p and V_n, are the voltage drops in the p+ and n+ regions, respectively. The third term is the voltage drop in the space-charge region at the n-well/p-well junction. The p, n, N_D, N_A are the concentrations of hole, electron, n-well doping, and p-well

doping, respectively. The fourth term is the ohmic voltage and will always increase with the current density J.

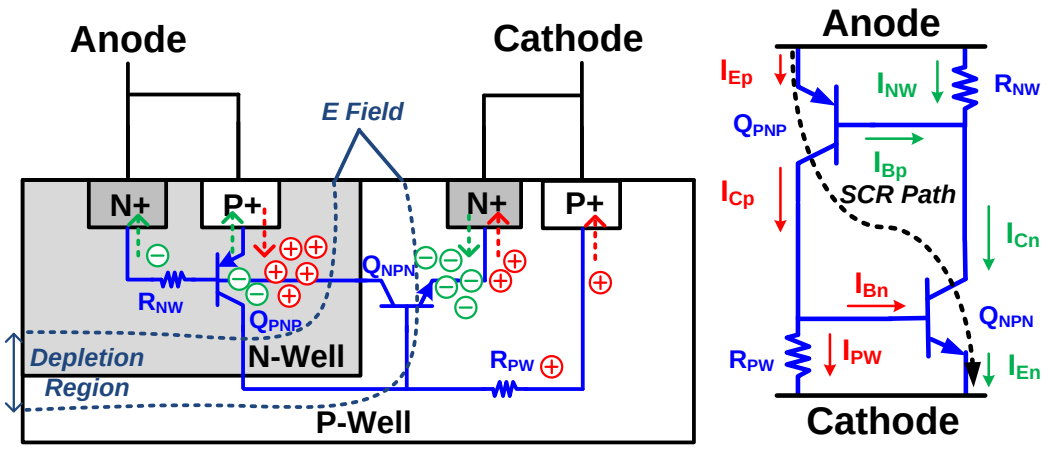


Fig. 2.1. Device cross-sectional view and equivalent circuit diagram of traditional SCR in a CMOS technology.

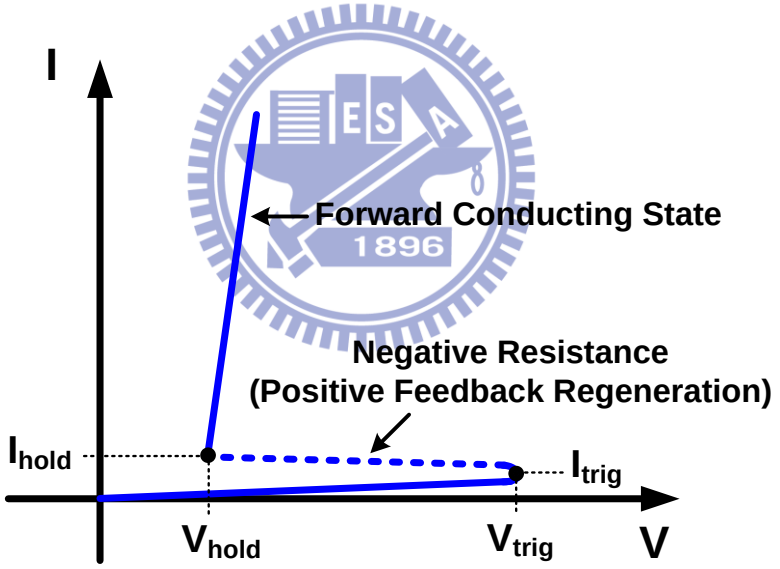


Fig. 2.2. Typical I–V characteristic of traditional SCR in a CMOS technology.

When SCR device is avalanche breakdown and switched into forward conducting state, the collapse of voltage drop is mainly caused by the voltage reduction in the space-charge term of Equation (2.2). Owing to the regenerative feedback of cross-coupled n-p-n and p-n-p BJTs, the electrons and holes are continuously injected into the n-well and p-well regions, and then the electrical field in the space-charge region at the n-well/p-well junction is gradually reduced.

The avalanche generation with high electrical field is hence mitigated due to the double carrier injection. Afterwards, the n-well and p-well regions are modulated as quasi-neutral region when the concentrations of injected holes and electrons that become much higher than the doping concentrations of n-well and p-well regions are equal to each other. Finally, the SCR device in the forward conducting state can be simplified as a p–i–n diode with small voltage drop and low power dissipation [20].

2.3 Prior Study on High-Holding-Voltage SCR

Though traditional SCR usually exhibited efficient ESD protection level, the characteristic of low holding voltage made itself very susceptible to latchup danger in the HV applications. Recently, some techniques have been proposed to optimize SCR device for high holding voltage, such as adding parasitic structure [21], modulating emitter wells [22], embedding PIN diode junction [23], and so forth.

In the previous study [21], a parasitic n-p-n BJT ($Q_{NPN'}$) was added into the traditional SCR device, as illustrated in Fig. 2.3. By partly diverting the SCR current through this additional BJT, it could reduce the positive feedback regeneration of the inherent p-n-p (Q_{PNP}) and n-p-n (Q_{NPN}) BJTs, and hence suppress the electron and hole injection efficiency. To compensate the lack of such carriers, the impaction ionization rate induced by electric field becomes higher for the avalanche-generated carriers. Such a high electric field, therefore, gives rise to a high holding voltage. In the modified SCR, the dummy poly gate near cathode side was added to reduce the base width and increase the current gain of the additional BJT ($Q_{NPN'}$). The TLP measurement results of the SCR devices are shown in Fig. 2.4. In Fig. 2.4(a), the holding voltage of the conventional SCR is ~3 V. In Fig. 3(b), the holding voltage of the modified SCR is increased to ~7.7 V, while the breakdown voltages of both devices are almost the same. Moreover, the failure current (I_{t2}) of the modified SCR is as high as the conventional

SCR without any degradation.

The TLU test was used to simulate the noise disturbance under the normal circuit operating condition. The TLU measurement setup is shown in Fig. 2.5, where the MM ESD source was used to generate the transient noise into the power supply of device under test. The test results of the SCR devices are shown in Figs. 2.6 and 2.7. In Fig. 2.6, after transient noise triggering, the voltage was clamped down to ~2 V. On the contrary, the voltage across the modified SCR was still kept at 5 V, as shown in Fig. 2.7. This previous study had demonstrated that the modified SCR exhibits good latchup immunity for the 5-V circuit applications.

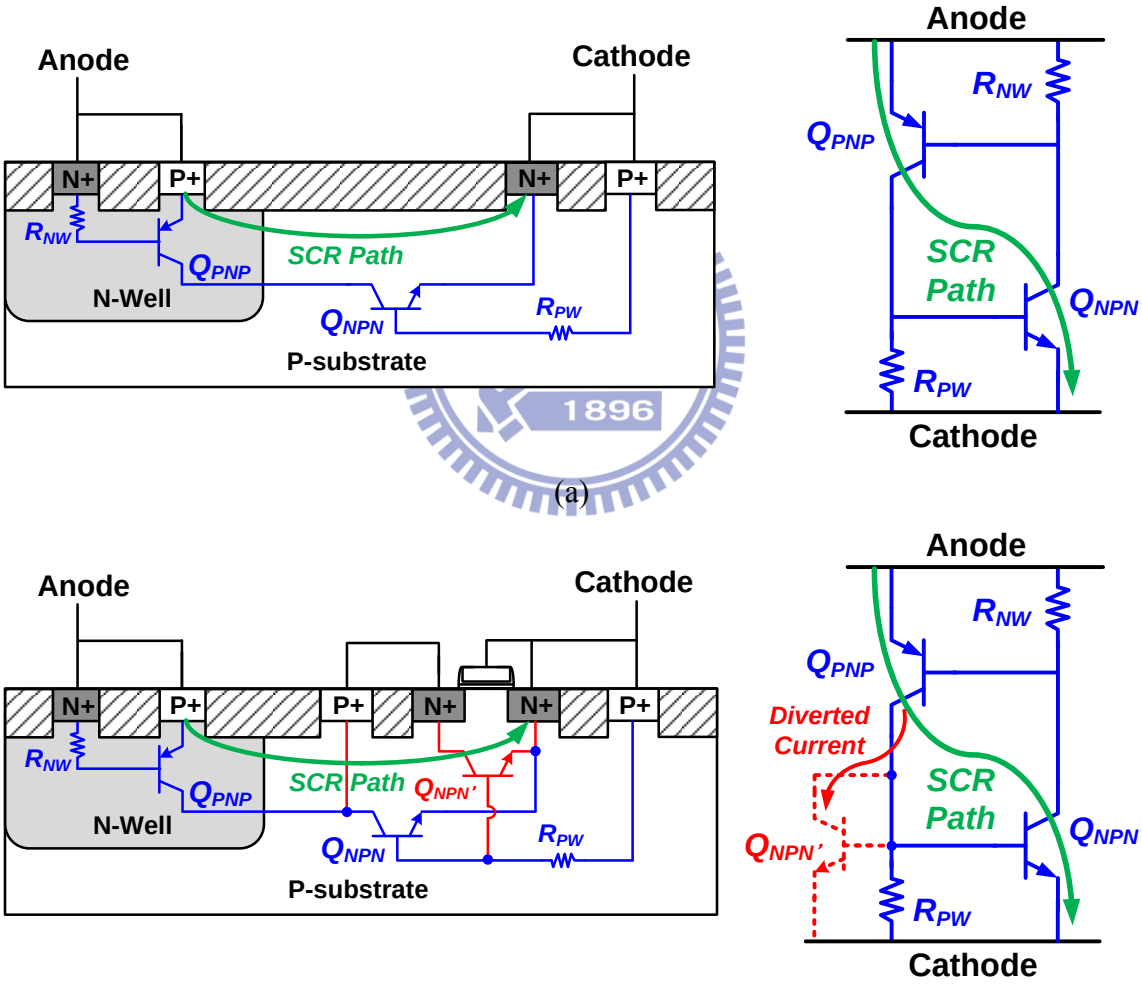
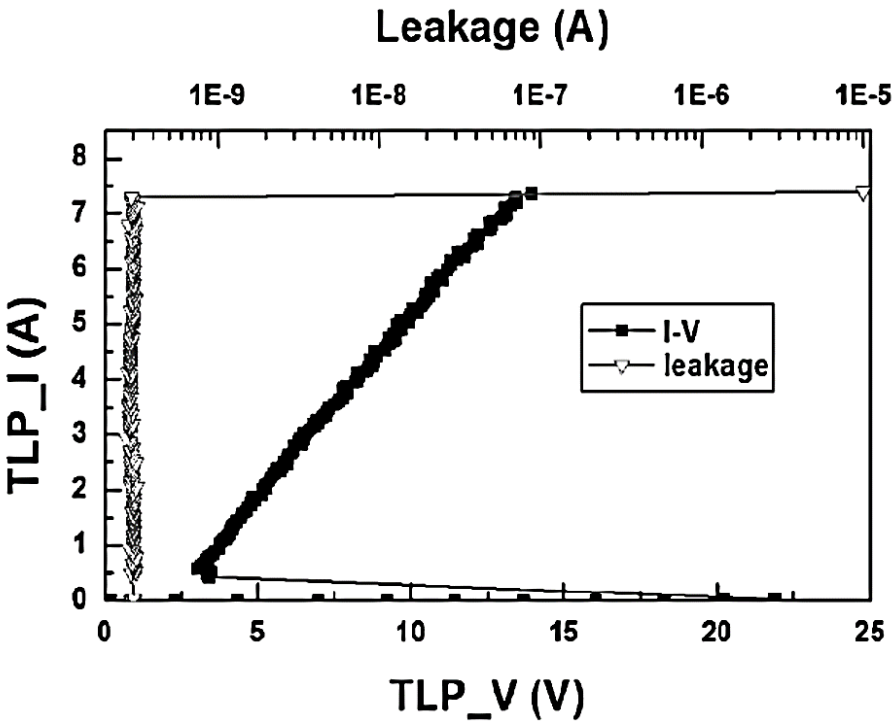
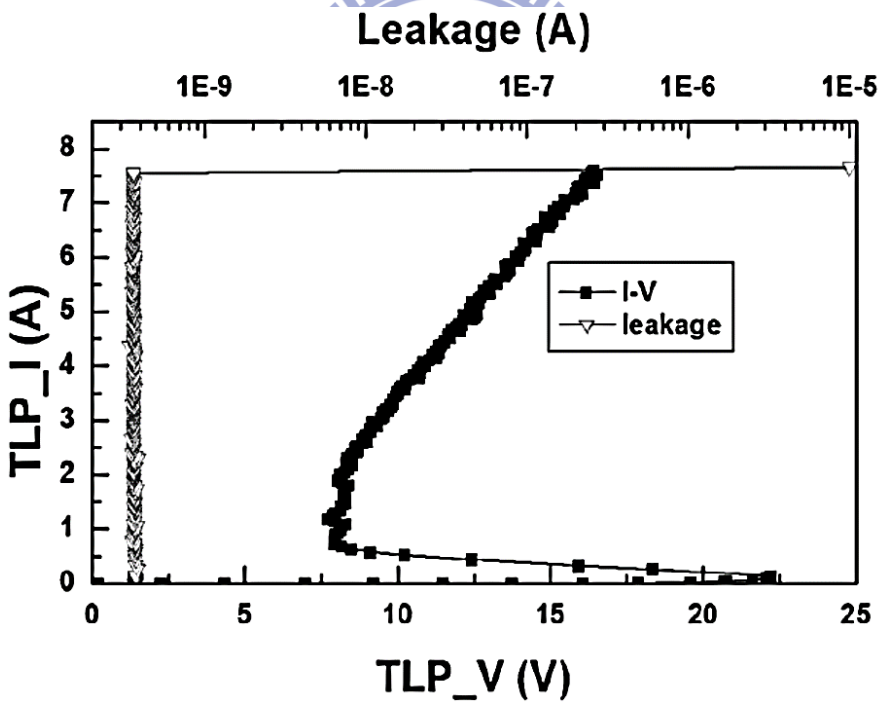


Fig. 2.3. Cross-sectional view and equivalent circuit diagram of (a) conventional SCR, and (b) modified SCR with additional n-p-n BJT ($Q_{NPN'}$) in the previous study [21].



(a)



(b)

Fig. 2.4. I–V characteristics of (a) conventional SCR and (b) modified SCR measured by TLP system in the previous study [21].

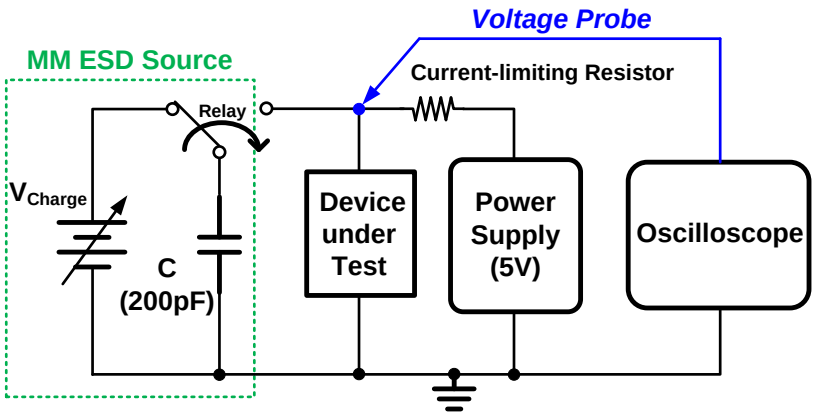


Fig. 2.5. Measurement setup of TLU test in the previous study [21].

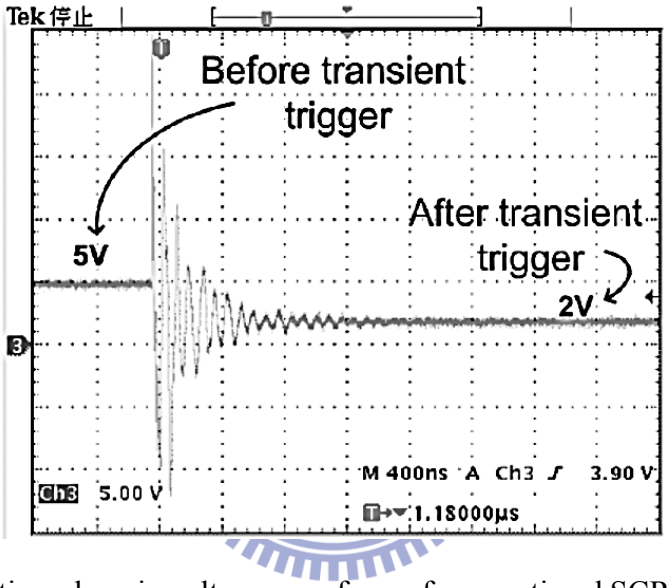


Fig. 2.6. Measured time-domain voltage waveform of conventional SCR in the previous study [21].

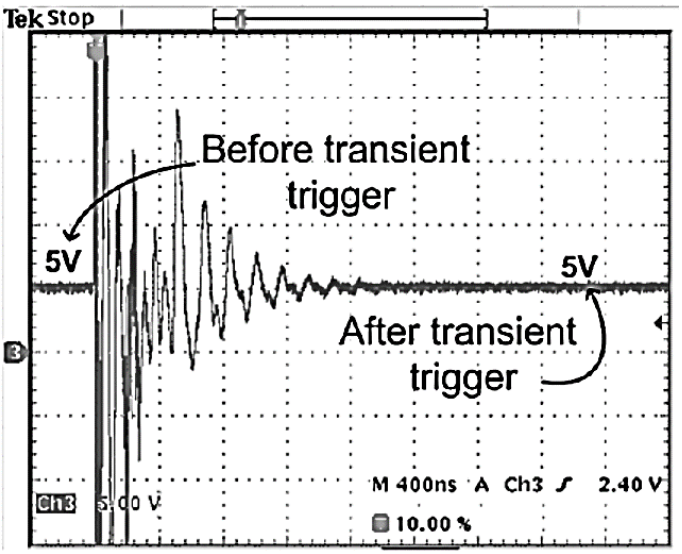


Fig. 2.7 Measured time-domain voltage waveform of modified SCR in the previous study [21].

2.4 New Proposed High-Holding-Voltage SCR in a 0.25-μm 5/12/20/40/60/80V BCD Process

2.4.1 Proposed Device Structures

Based on the prior study [21], a modified high-voltage SCR (HVSCR) structure realized with HV wells has been proposed in a 0.25-μm 5/12/20/40/60/80V BCD process to achieve high holding voltage.

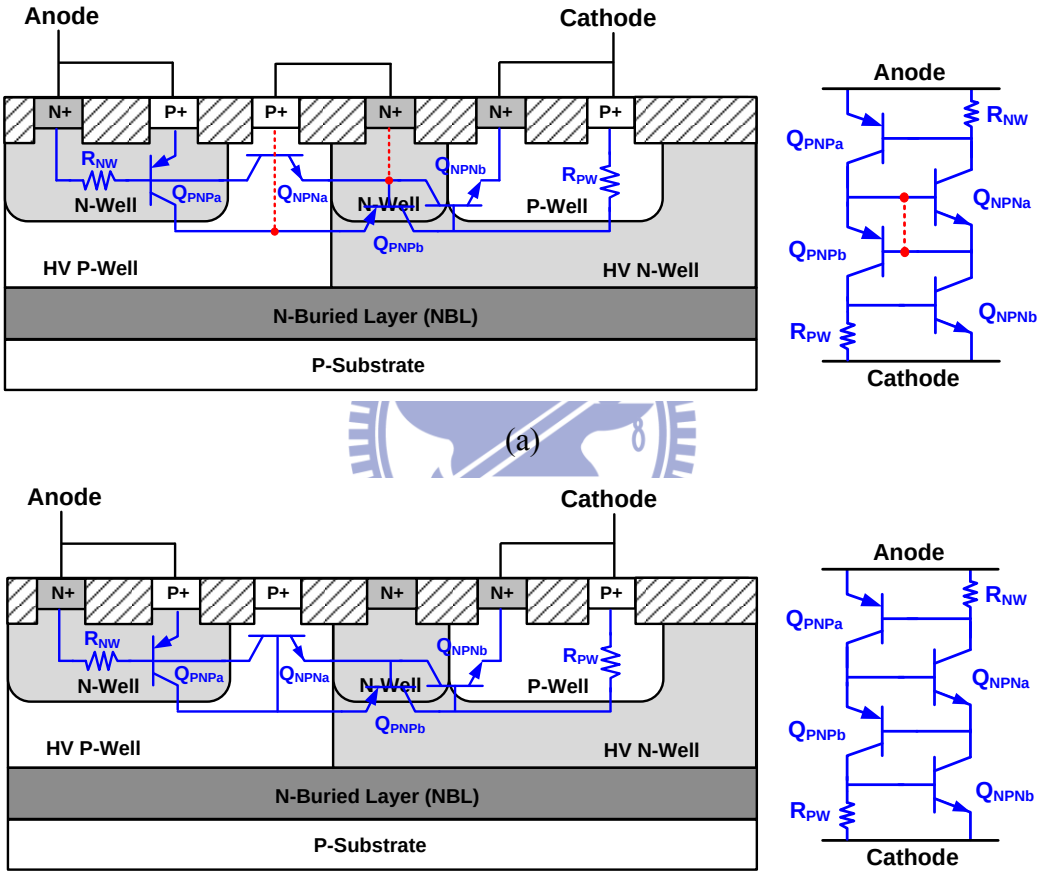
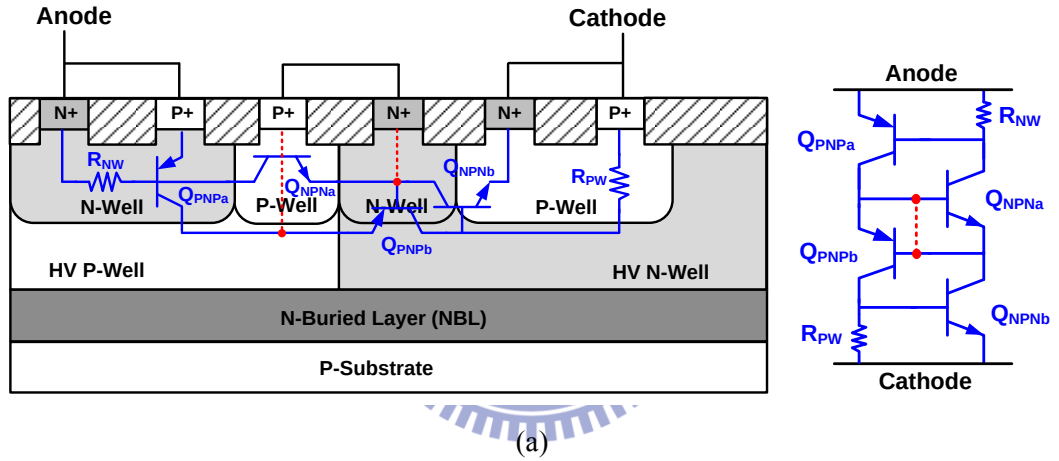


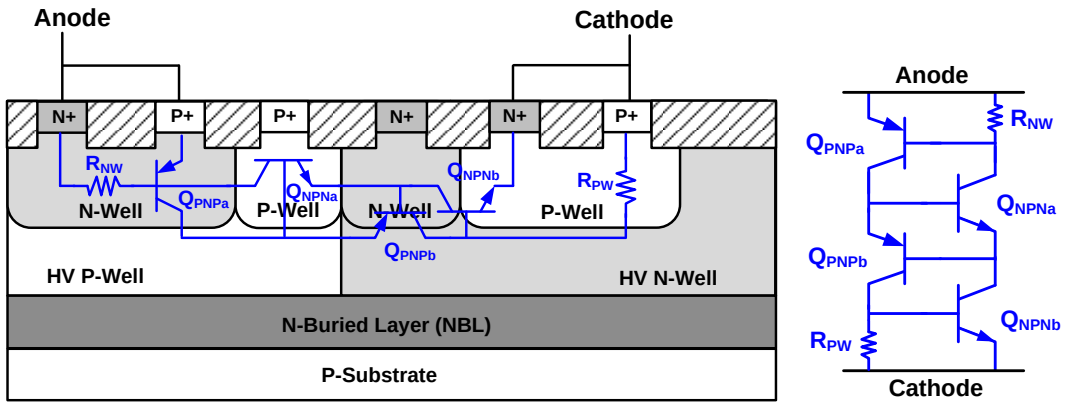
Fig. 2.8. Cross-sectional views and equivalent circuit diagrams of the proposed HVSCR_A (a) with, and (b) without, PN-connection path.

The cross-sectional view and equivalent circuit diagram of the proposed type-A HVSCR (HVSCR_A) are shown in Fig. 2.8(a). The n-well (NW) and HV n-well (HVNW) are added to surround the p-well (PW) region of cathode side and both kept floating. The HV p-well (HVPW)

region near anode side is surrounded by HVNW and n-buried layer (NBL) for the isolation from p-substrate. The p-type doping (p+) and the n-type doping (n+) regions are added in HVPW and HVNW, respectively. By electrically connecting those doping regions, an additional path (PN-connection path) from the collector of upper p-n-p BJT (Q_{PNPa}) to the collector of lower n-p-n BJT (Q_{NPNb}) is established, as the red dashed line illustrated in Fig. 2.8(a). The flowing hole and electron carriers within the SCR path under the conduction state can be partly diverted through such additional path. It can suppress the positive feedback of the original SCR path for a higher holding voltage. Fig. 2.8(b) shows the diagram of the HVSCR_A without PN-connection path.



(a)



(b)

Fig. 2.9. Cross-sectional views and equivalent circuit diagrams of the proposed HVSCR_B (a) with, and (b) without, PN-connection path.

Further modified from the structure of the HVSCR_A, the proposed Type-B HVSCR (HVSCR_B) illustrated in Fig. 2.9(a) is inserted with PW in HVPW to enhance the conduction efficiency of the additional path. Fig. 2.9(b) shows the diagram of the HVSCR_B without PN-connection path. Each proposed SCR is drawn with width of 200 μm and anode-to-cathode spacing (S) of 14 μm. Compared with the traditional SCR, each proposed SCR is composed of a six-layer p-n-p-n-p-n structure. It forms a stacked SCR configuration in the equivalent circuit diagram that includes stacked p-n-p (Q_{PNPa}, Q_{PNPb}) and n-p-n (Q_{NPNa}, Q_{NPNb}) BJTs. The layout top view for these proposed SCRs are shown in Fig. 2.10. The diffusions of HVPW and HVNW rings can be electrically connected with metal layer to build the PN-connection path.

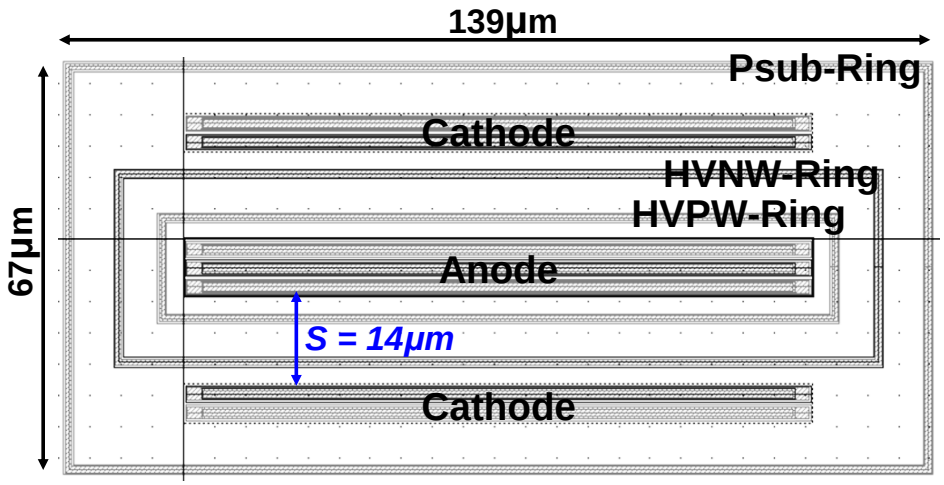
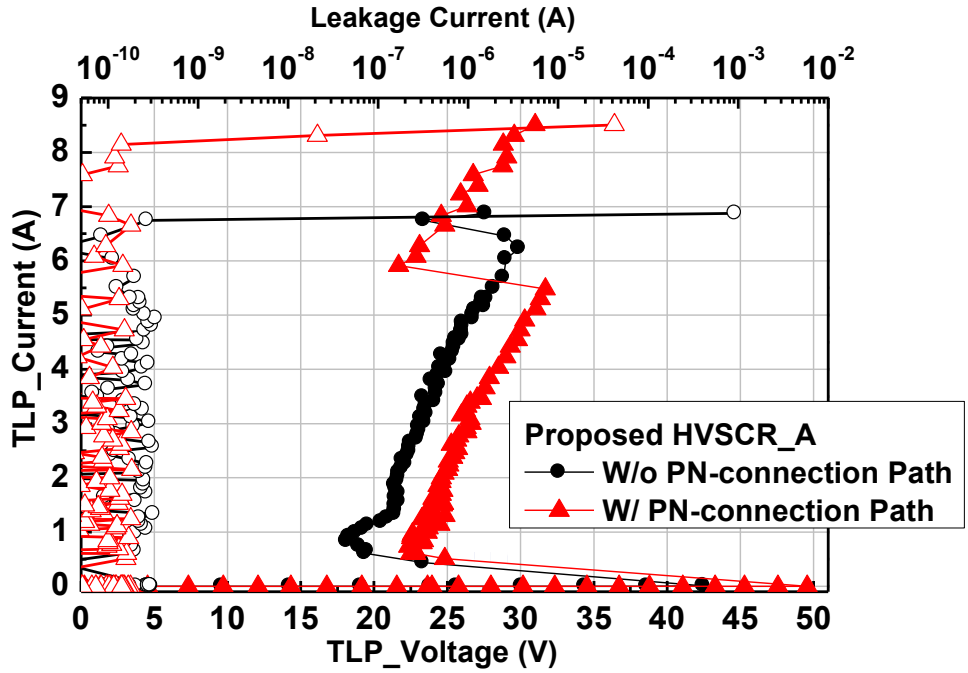


Fig. 2.10. Layout top view of the proposed SCRs in this 0.25-μm 5/12/20/40/60/80V BCD process.

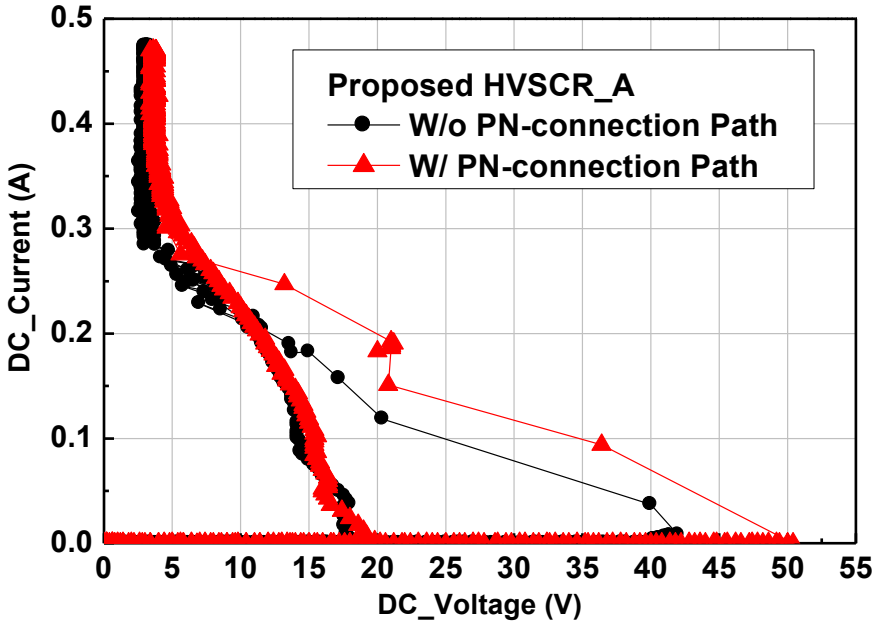
2.4.2 TLP and DC Measurement Results

Fig. 2.11(a) shows the 100-ns TLP measurement results of the HVSCR_A. The leakage currents are measured at 30 V. The TLP-measured holding voltage of the HVSCR_A without and with PN-connection path are 18.1 and 21.7 V, respectively. However, in the DC test results shown in Fig. 2.11(b), the DC-measured holding voltage of the HVSCR_A without and with PN-connection path are 2.8 and 3.4 V, respectively. The reason causing such difference between

TLP and DC test results is the increased BJT current gains of the SCR path induced by the Joule heating effect in the DC measurement [11]. Accordingly, adding PN-connection path in the HVSCR_A can only slightly increase its holding voltage.

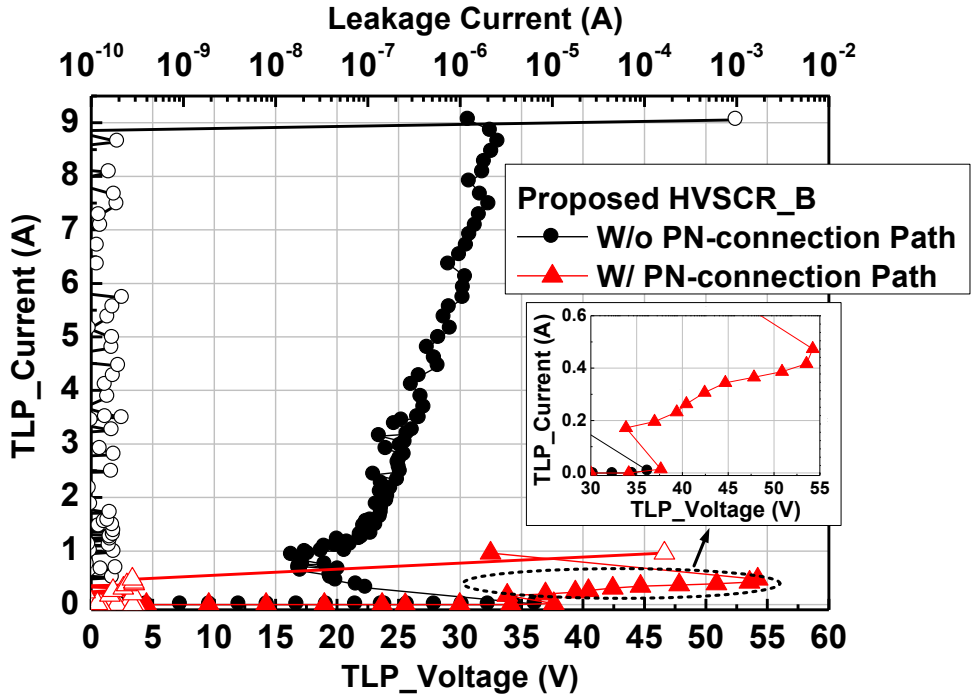


(a)

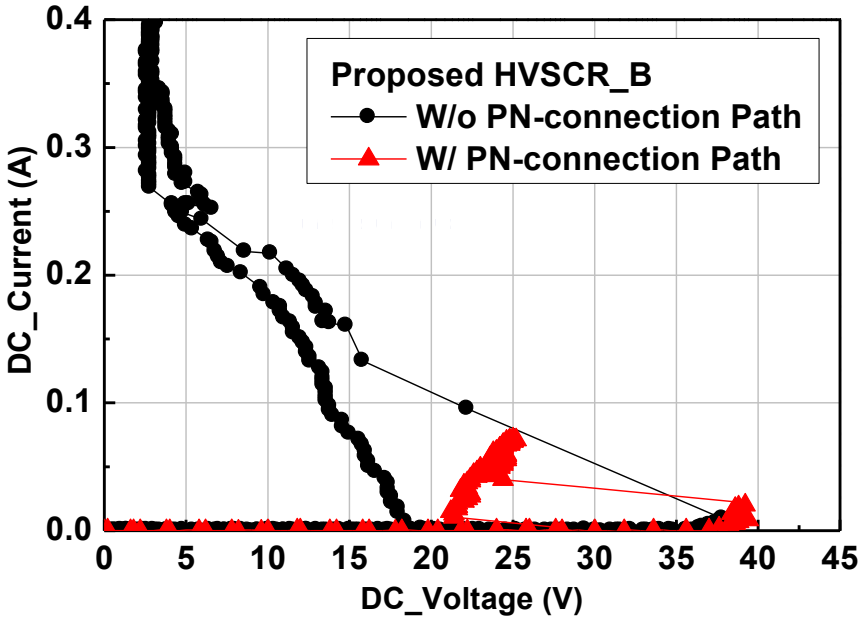


(b)

Fig. 2.11. I–V characteristics of the proposed HVSCR_A without or with PN-connection path measured by (a) TLP system and (b) DC curve tracer.



(a)



(b)

Fig. 2.12. I–V characteristics of the proposed HVSCR_B without or with PN-connection path measured by (a) TLP system and (b) DC curve tracer.

The TLP and DC measurement results of the HVSCR_B are shown in Figs. 2.12(a) and 2.12(b), respectively. The TLP-measured holding voltage of the HVSCR_B with PN-connection path can rise to 33.8 V, and its DC-measured holding voltage is up to 21.4 V. Such high holding voltage is due to the enhanced conduction efficiency of the additional path in the HVSCR_B inserting PW in HVPW. Thus, adding PN-connection path in the HVSCR_B can significantly increase its holding voltage. However, the TLP-measured failure current (I_{t2}) of the HVSCR_B with PN-connection path is only 0.47 A. The detailed test results of the proposed SCRs are summarized in Table 2.1, such as device dimension, DC breakdown voltage (V_{BD}), DC-measured holding voltage (DC V_{hold}), TLP-measured holding voltage (TLP V_{hold}), TLP-measured failure current (TLP I_{t2}), and so on.

Table 2.1

Comparison of Test Results of Proposed HVSCR Devices

HVSCR Type	Type-A (W/o PN)	Type-A (W/ PN)	Type-B (W/o PN)	Type-B (W/ PN)
Width (μm)	200	200	200	200
Layout Area (μm^2)	9313	9313	9313	9313
V_{BD} (V)	36	48	34	34
DC V_{hold} (V)	2.8	3.4	2.8	21.4
TLP V_{hold} (V)	18.1	21.7	16.9	33.8
TLP I_{t2} (A)	6.74	8.14	8.84	0.47
HBM ESD level (V)	>8000 *	>8000 *	>8000 *	1000
HBM / Layout Area (V/μm^2)	>0.859	>0.859	>0.859	0.107
ESD Robustness	Good	Good	Good	Bad
Latchup Issue for 20-V Application	Risky	Risky	Risky	Safe
* limited by ESD test equipment.				

In addition, the ESD protection levels of the proposed SCRs are further judged by the HBM ESD tester. The proposed SCRs can exhibit high HBM ESD level of above 8 kV except the one with the highest holding voltage. The reason is that a high holding voltage may cause a

high electric power to burn out the device during the conduction state, and hence degrade the device's ESD protection level. For the 20-V circuit applications, the proposed HVSCR_B with a high holding voltage of above 20 V can be applied for ESD protection and avoid latchup risk.

2.4.3 Transient-induced Latchup Test Results

To verify the TLP and DC measurement results, TLU test is applied in this work. TLU test is an effective test method to evaluate the susceptibility of CMOS ICs to the latchup induced by transient noises. The measurement setup for this TLU test is shown in Fig. 2.13. In the TLU test, the device under test (DUT) is initially biased at normal circuit operating voltage of 30 V. A transient noise is injected into DUT from the trigger source with a pre-charged voltage (V_{charge}). From the measured voltage and current waveforms shown in Figs. 2.14(a) and 2.14(b), the HVSCR_A without and with PN-connection path both clamp the supply voltages to ~4 V, which are similar to their values of DC-measured holding voltage. From the test results shown in Figs. 2.15(a) and 2.15(b), the HVSCR_B without and with PN-connection path clamp the supply voltages to ~4 and ~24 V, respectively, which are also similar to their DC-measured holding voltage. In consequence, the TLU test has verified that the proposed SCR devices can greatly clamp the supply voltage to their own DC-measured holding voltage.

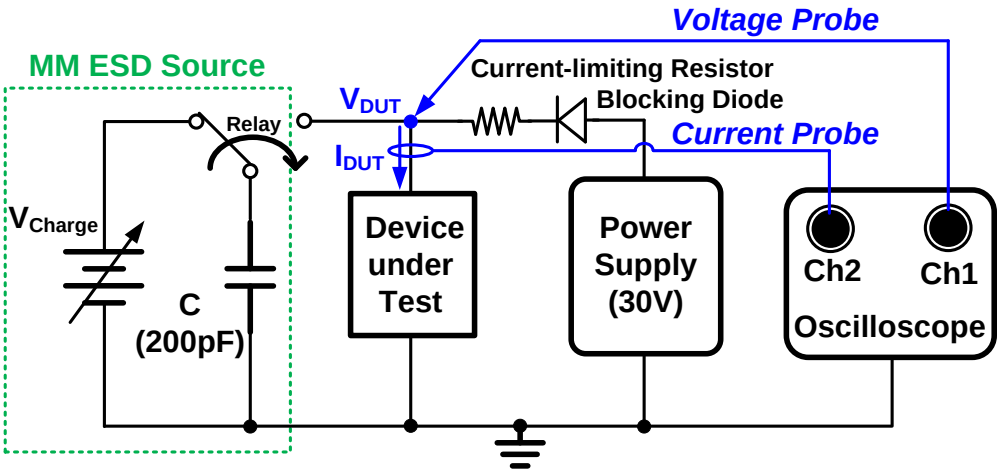
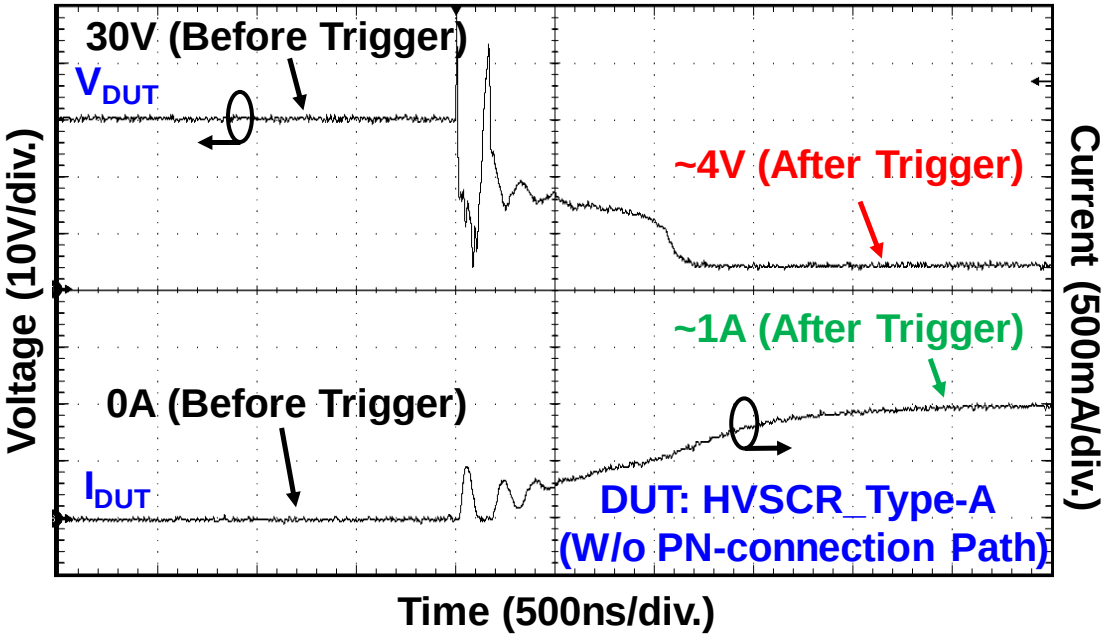
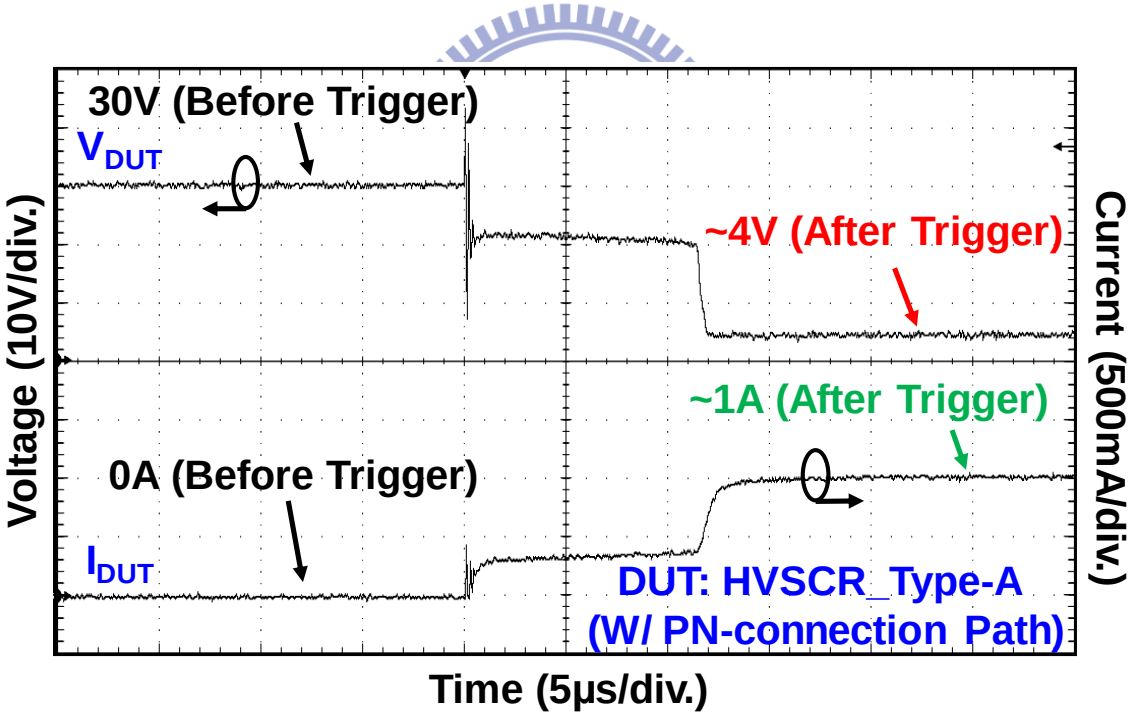


Fig. 2.13. Measurement setup of TLU test for the new proposed SCRs.

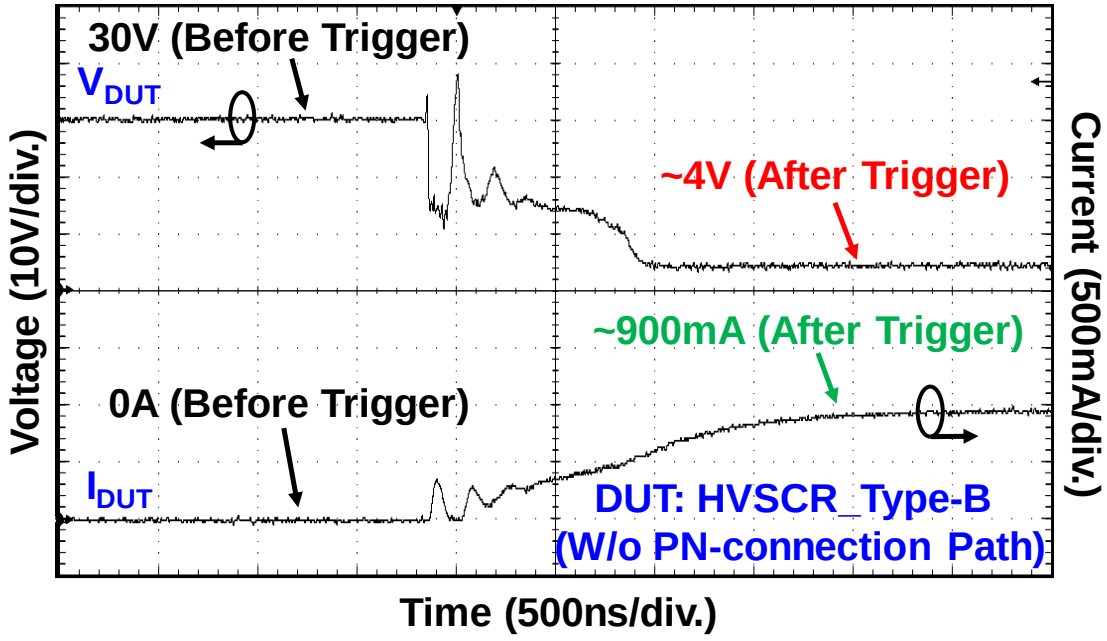


(a)

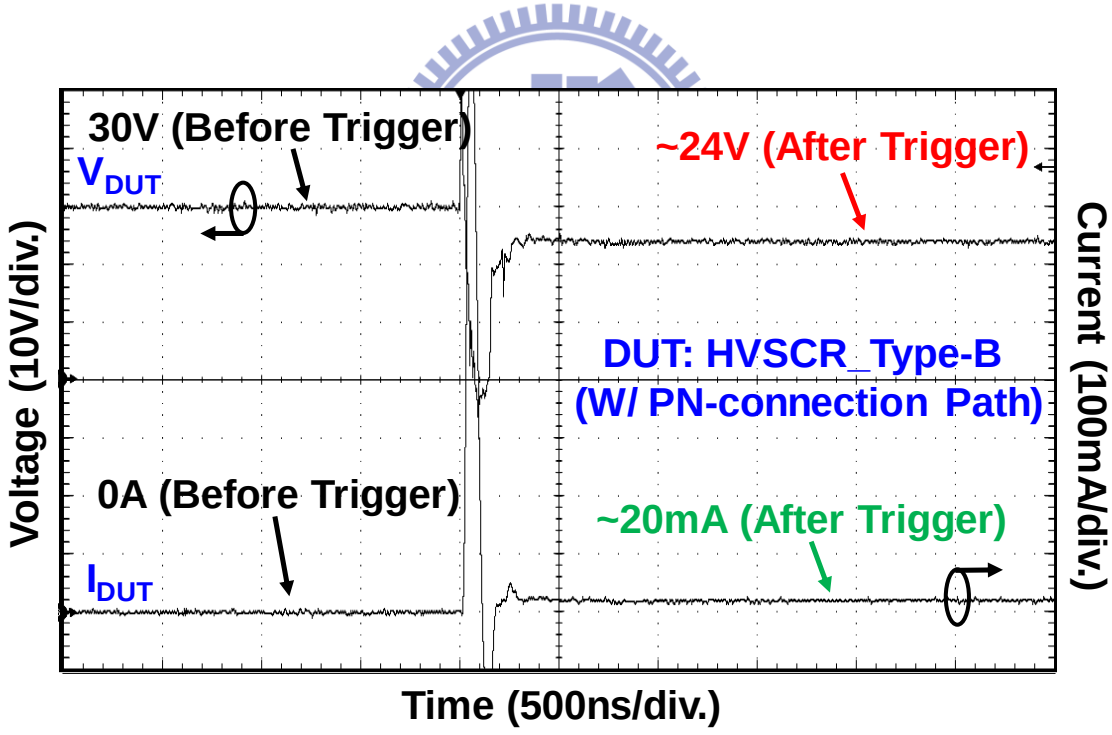


(b)

Fig. 2.14. Measured time-domain voltage and current waveforms of the proposed HVSCR_A (a) without, and (b) with, PN-connection path.



(a)



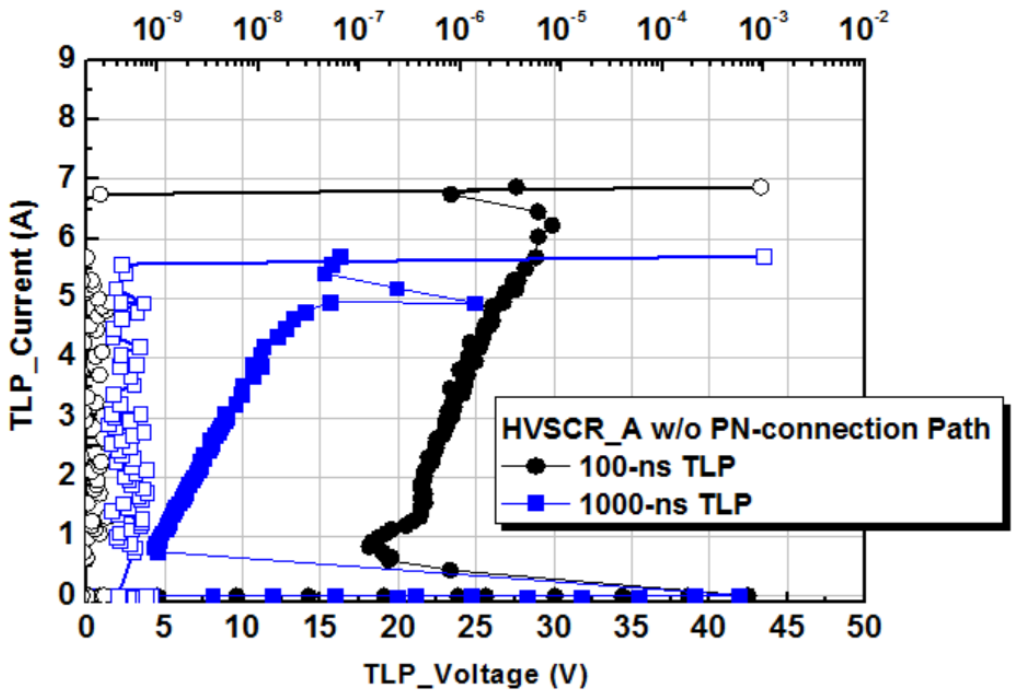
(b)

Fig. 2.15. Measured time-domain voltage and current waveforms of the proposed HVSCR_B (a) without, and (b) with, PN-connection path.

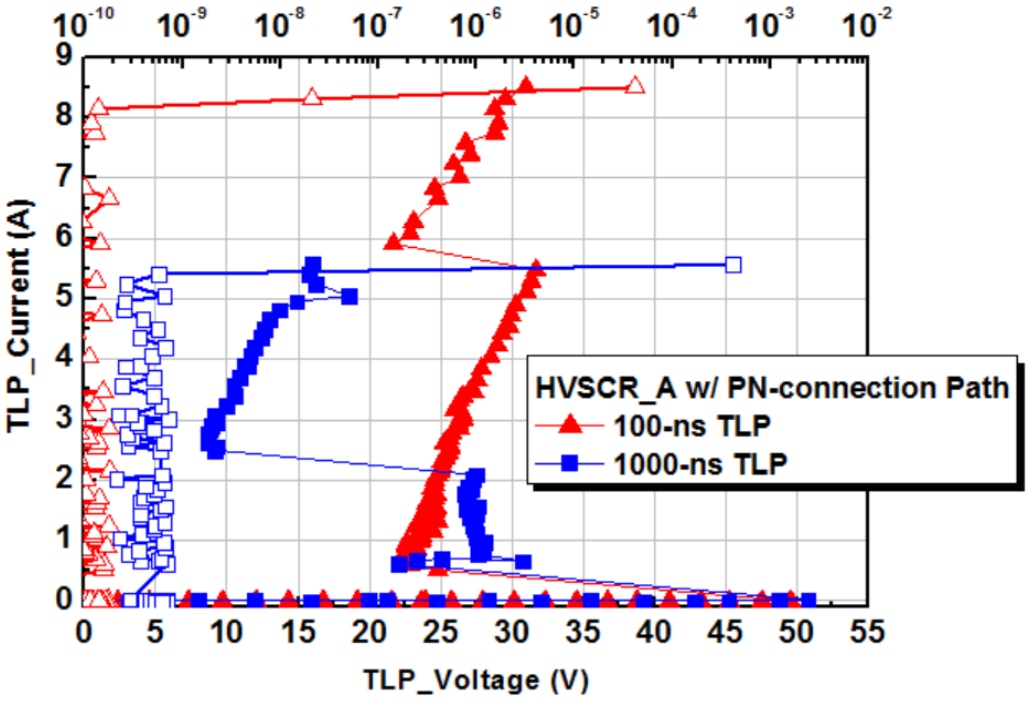
2.4.4 Discussion

The I-V characteristics of the proposed HVSCRs, measured by100-ns and 1000-ns TLP system, are shown in Figs. 2.16 and 2.17. In Fig. 2.16(a), the 1000-ns TLP-measured holding voltage of the proposed HVSCR_A without PN-connection path is ~5 V, which is similar to its DC-measured holding voltage. In Fig. 2.16(b), the 1000-ns TLP-measured holding voltage of HVSCR_A with PN-connection path has double snapback phenomenon due to the multiple junction breakdown. It is first triggered into the first snapback region with holding voltage of ~27 V. Then, with higher TLP-generated power, it is triggered into the second snapback region with holding voltage of ~10 V, which is close to its DC-measured holding voltage. In Fig. 2.17(a), the 1000-ns TLP-measured holding voltage of the proposed HVSCR_B without PN-connection path is similar to its DC-measured holding voltage. However, In Fig. 2.17(b), the 1000-ns TLP-measured I-V characteristics of HVSCR_B with PN-connection path is slightly bent outward. Because the 1000-ns TLP test results can be well covered by the DC test results, the detailed operation mechanism inside such proposed HVSCRs will not be discussed in this work. However, the turn-on mechanism of this HVSCR still needs more detailed understanding. It can be a good topic with some optimized device structures for future studies.

According to the above measurement results and Ref. [6], the real holding voltage of HV devices fabricated in multiple HV wells must be verified by DC measurement. Moreover, TLU test is more effective to monitor the holding voltage roll-off in time domain and observe the real value. As the TLU test results shown in Figs. 2.14 and 2.15, the time durations for measuring the real holding voltage of the proposed SCRs in TLU test are at least longer than 1.8μs, which is long enough to judge the real holding voltage.

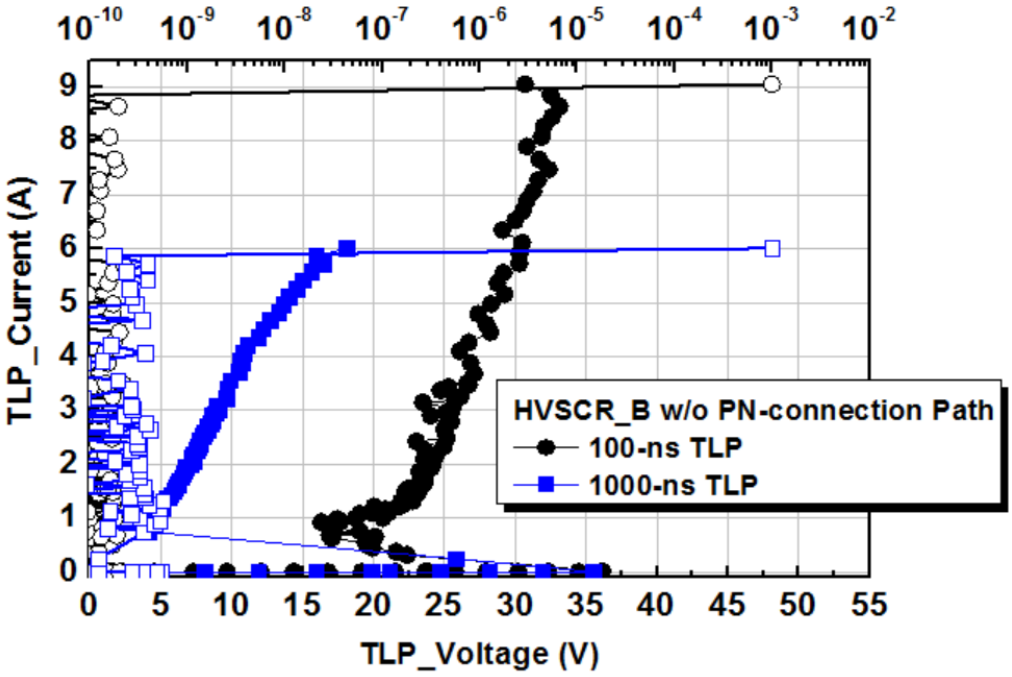


(a)

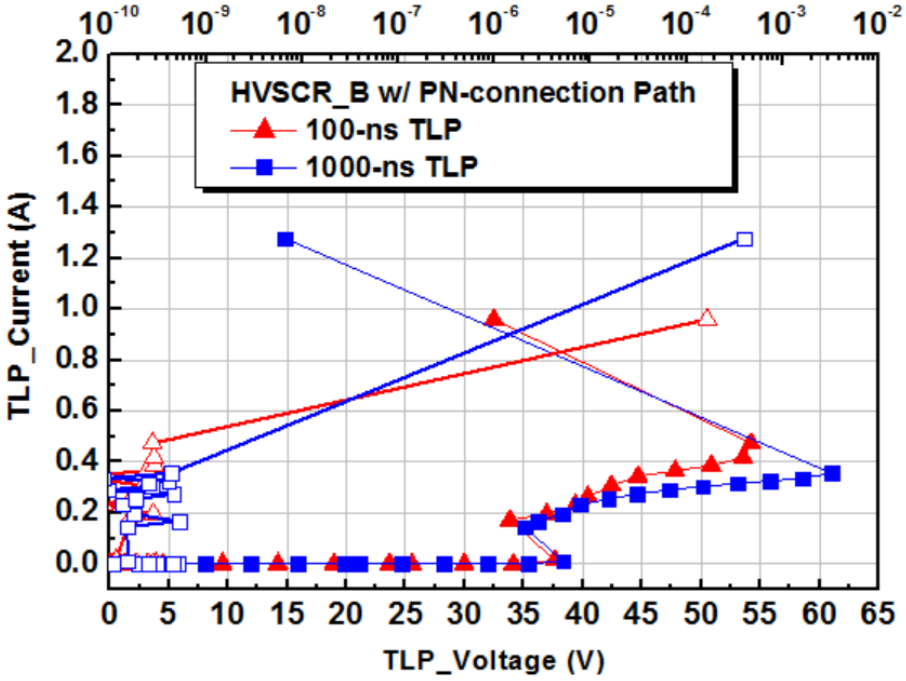


(b)

Fig. 2.16. I-V characteristics of the proposed HVSCR_A (a) without and (b) with PN-connection path, measured by100-ns and 1000-ns TLP system.



(a)

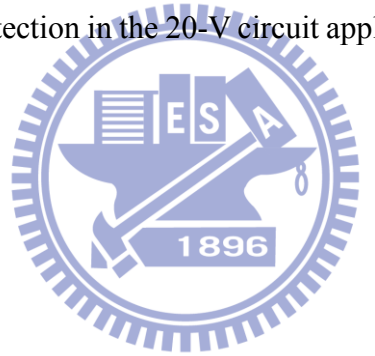


(b)

Fig. 2.17. I-V characteristics of the proposed HVSCR_B (a) without and (b) with PN-connection path, measured by100-ns and 1000-ns TLP system.

2.5 Summary

The characteristics of the proposed SCRs have been investigated in a 0.25-μm 5/12/20/40/60/80V BCD technology. Experiment results show that one of the proposed SCRs has a high holding voltage of up to ~30 V in the 100-ns TLP measurement results. However, through the experiment verification by using TLU test, the holding voltage of such proposed device decreases to ~20 V. The Joule heating effect could dramatically decrease the holding voltage of the proposed SCR even if it is fabricated in a six-layer p-n-p-n-p-n structure. Such phenomenon is an unavoidable issue that should be carefully taken into consideration when developing special modification on such HV devices for ESD protection in the 0.25-μm HV BCD technology. Moreover, the proposed HVSCR device with DC holding voltage larger than 20 V can be applied for ESD protection in the 20-V circuit application without any latchup risk.



Chapter 3

Study of ESD Protection Design with Stacked Low-Voltage Devices for High-Voltage Applications

3.1 Background

On-chip ESD protection design in smart power technology is a challenging issue due to high supply voltage and multiple doped layers in HV processes. In order to protect the internal circuits against ESD damage, HV ESD protection devices are applied to all input/output (I/O), power (VDD/VSS), and switch (SW) pads. Traditionally, the weak-snapback HV devices like PNP BJTs are usually used as main ESD protection when considering ESD robustness and latchup issues. Nevertheless, the HV devices usually exhibit weak current capability per layout area because of high power dissipation for their multi-layer structures. To get sufficient ESD robustness, such HV devices were often fabricated with a large silicon area to meet the industry standards. Different from the HV devices, low-voltage (LV) devices have the characteristics of simple device structure and high current capability. In some HV circuit applications, multiple LV devices cascaded for the specific circuit functions are able to sustain high supply voltage without DC breakdown issue [24]. According to the prior study, stacked LV devices can be another way to achieve high holding voltage for ESD protection in the HV applications.

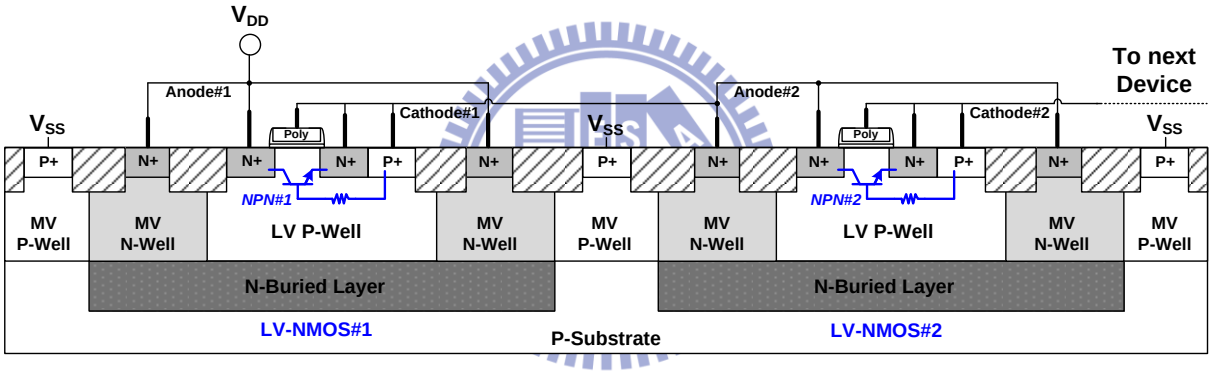
This chapter continues to investigate the LV devices with stacked configuration as HV ESD protection design. To achieve both effective ESD protection level and latchup immunity, the stacked LV devices will be verified in a 0.25-μm 5/40/60V BCD process and compared with the proposed HVSCRs in chapter 2. Moreover, the desired ESD protection design window for the HV pins of a battery-monitoring IC fabricated in a 0.25-μm 5/40/60V BCD technology can be easily satisfied by utilizing the stacked LV devices, rather than developing special

modification on the HV devices.

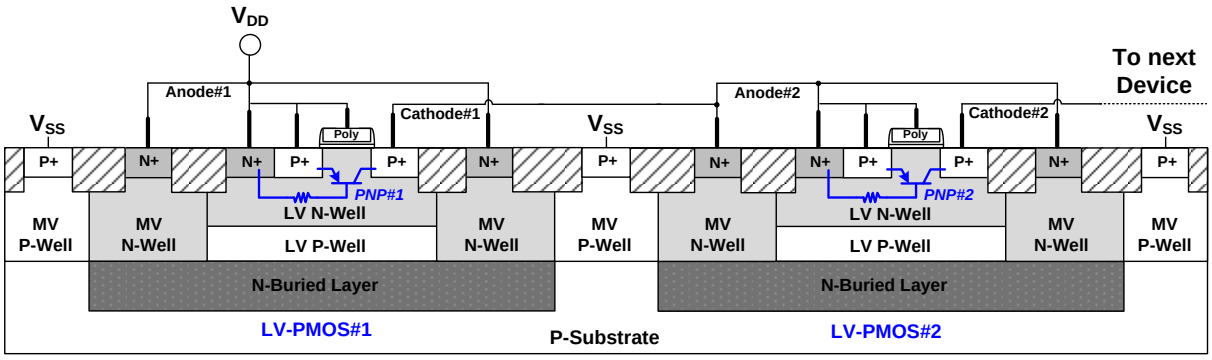
3.2 Comparison between Stacked Low-Voltage Devices and High-Holding-Voltage SCR for ESD Protection in High-Voltage Applications

3.2.1 Proposed LV Devices with Stacked Configuration

In this work, the different stacked LV devices have been proposed in a 0.25-μm 5/40/60V BCD process for HV ESD protection design. The ESD robustness of those stacked LV devices are verified for the comparison with the high-holding-voltage SCR presented in Chapter 2.

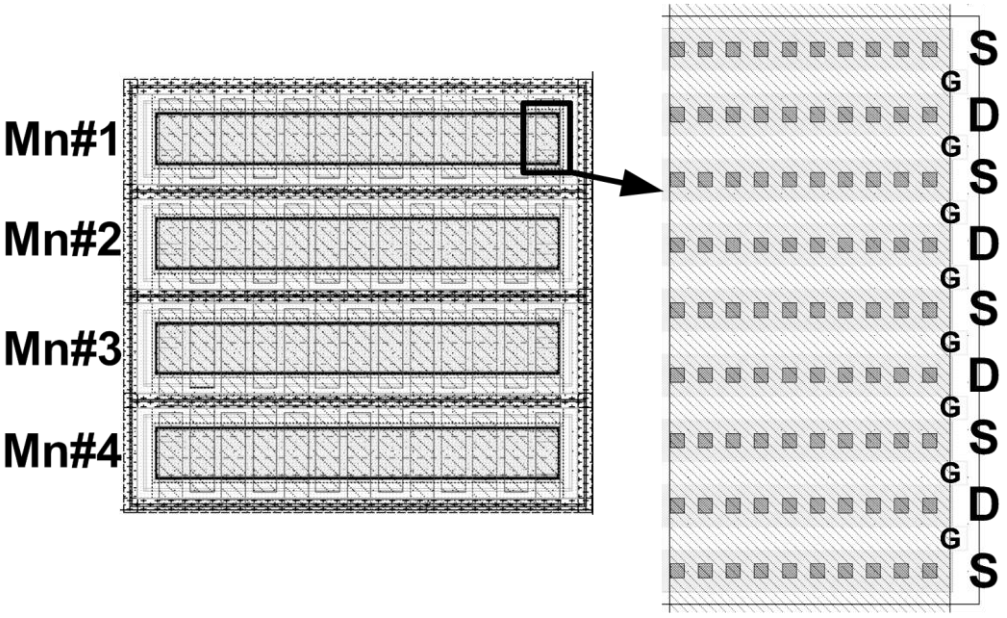


(a)

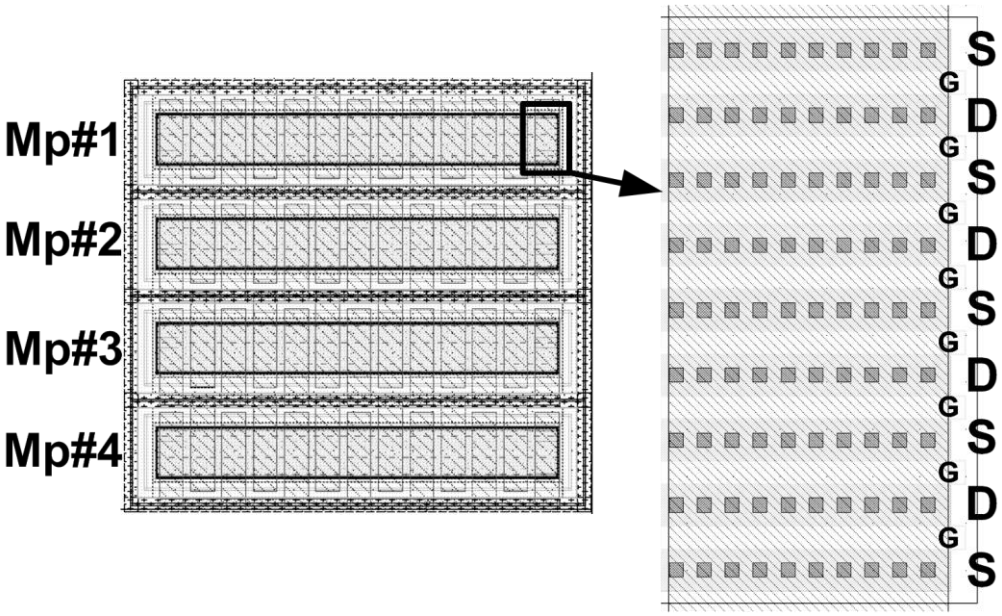


(b)

Fig. 3.1. The cross-sectional views of (a) stacked LV-NMOS, and (b) stacked LV-PMOS, with each device surrounded by n-buried layer (NBL) in a 0.25-μm 5/40/60V BCD process.



(a)



(b)

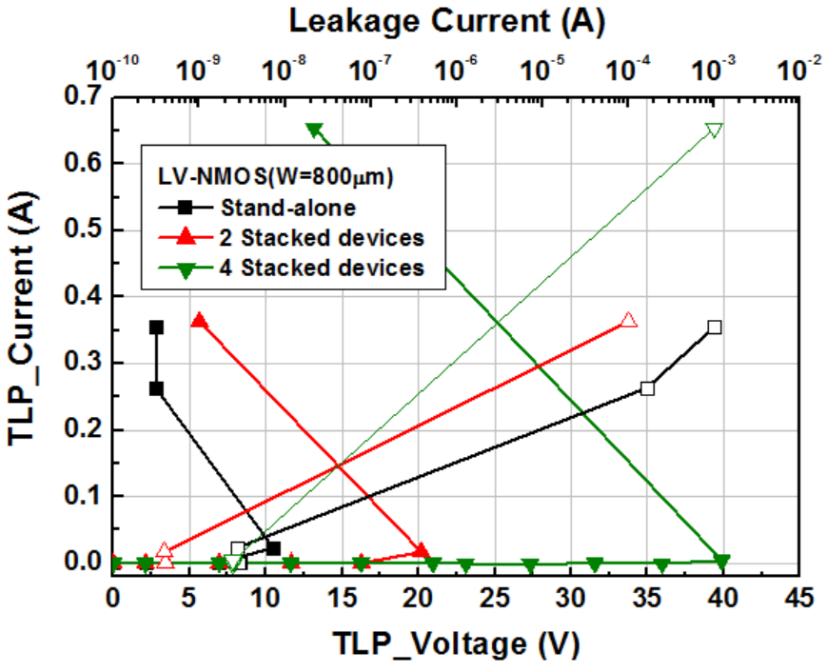
Fig. 3.2. The layout top views of (a) 4 stacked LV-NMOS, and (b) 4 stacked LV-PMOS, where each device is drawn with minimum spacing in a 0.25-μm 5/40/60V BCD process.

The stacked configurations with LV n-type MOS (LV-NMOS) and LV p-type MOS (LV-PMOS) are shown in Fig. 3.1(a) and 3.1(b), respectively. The device dimensions are chosen as W/L of LV-NMOS = 800 μm / 0.5 μm and LV-PMOS = 800 μm / 0.5 μm, where the medium-

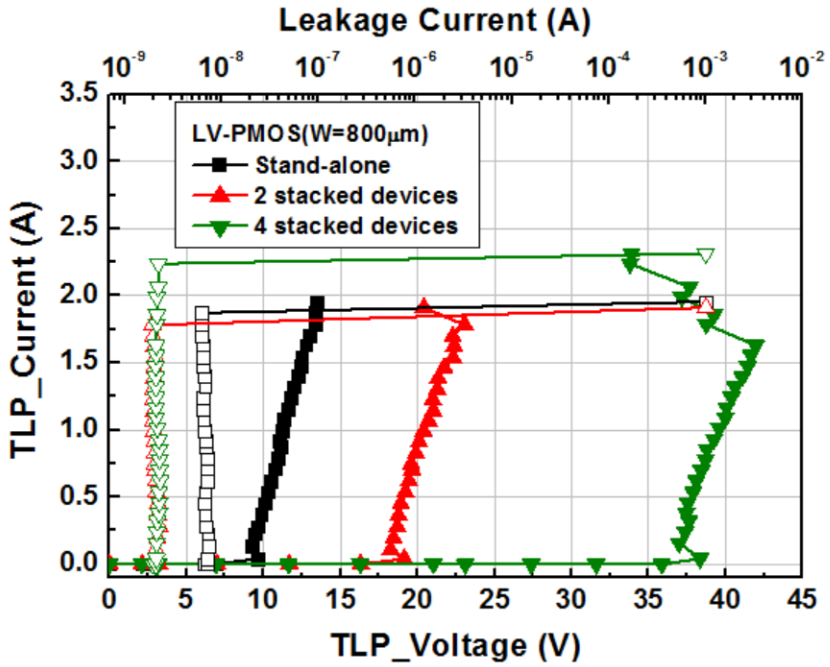
voltage (MV) n-well, MV p-well, and n-buried layer (NBL) are used to isolate the bias between each device and bulk. According to the foundry-provided rules, the devices isolated with MV wells can prevent unexpected breakdown path from the VDD-connected MV n-well to the VSS-connected MV p-well under 40-V circuit applications. All the LV devices are kept in off state and stacked with different stacking numbers of 1, 2, and 4, respectively. Their inherent parasitic NPN or PNP BJTs, as designated in Fig. 3.1, are used as main ESD dissipation path. The LV devices are fabricated with 5-V standard devices in this 0.25-μm HV BCD process. The layout top views of such LV devices are shown in Figs. 3.2(a) and 3.2(b), where each device is drawn with minimum layout spacing at drain and source sides to guarantee its high ESD robustness and minimize the silicon footprint. The layout area of the 4 stacked LV-NMOS is 107 μm x 114 μm, which is the same as the 4 stacked LV-PMOS.

Figs. 3.3a(a) and 3.3a(b) show the TLP-measured results of LV-NMOS and LV-PMOS with different stacking numbers, respectively. The LV-NMOS stacks are unable to enter snapback region and have poor failure current levels. By contrast, all the LV-PMOS stacks can have high failure currents greater than 1.5 A after entering snapback region. The trigger voltage and holding voltage of the LV-PMOS stacks can be linearly scaled by adjusting the stacking numbers. In addition, the breakdown voltage of each stand-alone LV device is ~9 V. It is linearly increased to ~36 V by stacking four devices.

Moreover, the dependence of on-state resistance (R_{on}) on different stacking numbers (SN) of stacked LV-PMOS is shown in Fig. 3.3b, where the extracted trend line equation is inserted. The R_{on} of single, stacked 2, and stacked 4 LV-PMOS are ~2.33, ~2.8, and ~3.47 Ω, respectively. The value is linearly increased with the stacking numbers. The parasitic resistance from the TLP system to the test device is ~2 Ω, which is extrapolated from the trend line. The pure R_{on} of single LV-PMOS device is ~0.37 Ω, which is extracted from the slope of trend line.



(a)



(b)

Fig. 3.3a. TLP I-V characteristics of (a) LV-NMOS stacks, and (b) LV-PMOS stacks, with different stacking numbers of 1, 2, and 4.

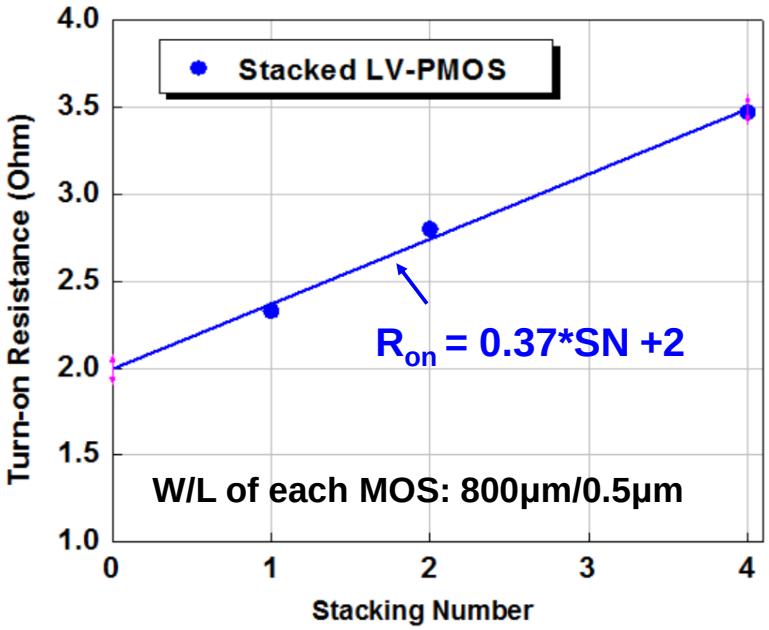


Fig. 3.3b. Dependence of on-state resistance (R_{on}) on stacked LV-PMOS with different stacking numbers (SN) of 1, 2, and 4.

The HBM ESD tester is used to investigate their ESD robustness. From the measurement results, the 4 stacked LV-PMOS has HBM level of up to 2400 V, but the 4 stacked LV-NMOS has only 200-V HBM level. The reason can be found through the SEM images, as shown in Figs. 3.4 and 3.5. The ESD failure locations indicate that the LV-NMOS stacks suffer from serious non-uniform turn-on effect due to the minimum spacing in layout design. In contrast to LV-NMOS, the LV-PMOS stacks with weak-snapback behavior can conduct the ESD current more uniformly, and hence exhibit better ESD protection levels. Besides, only one ESD failure location was found at the last device in the LV-PMOS stack. It implies that the minimum layout spacing can strongly influence the current distribution through the stacked devices during ESD stress.

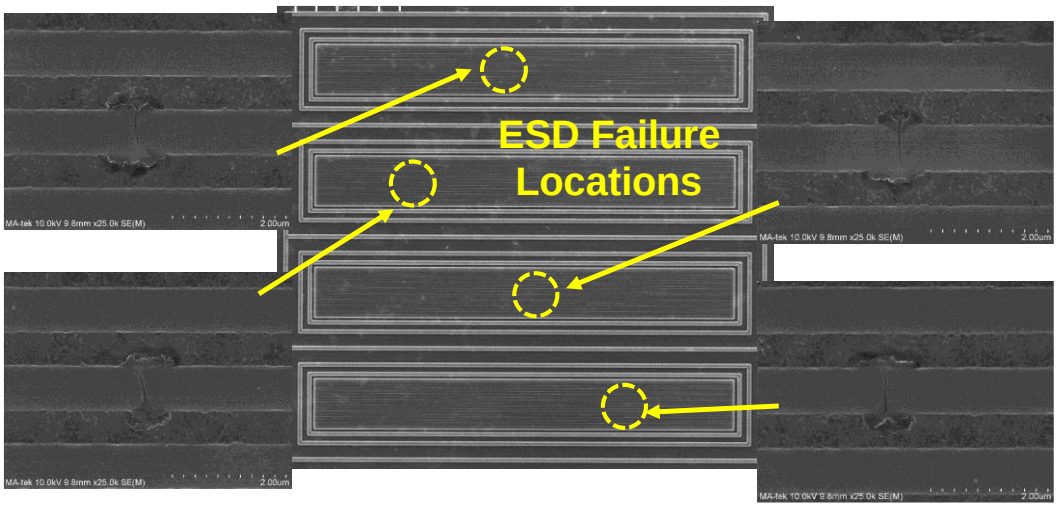


Fig. 3.4. The SEM image of 4 stacked LV-NMOS after 400-V HBM ESD stress.

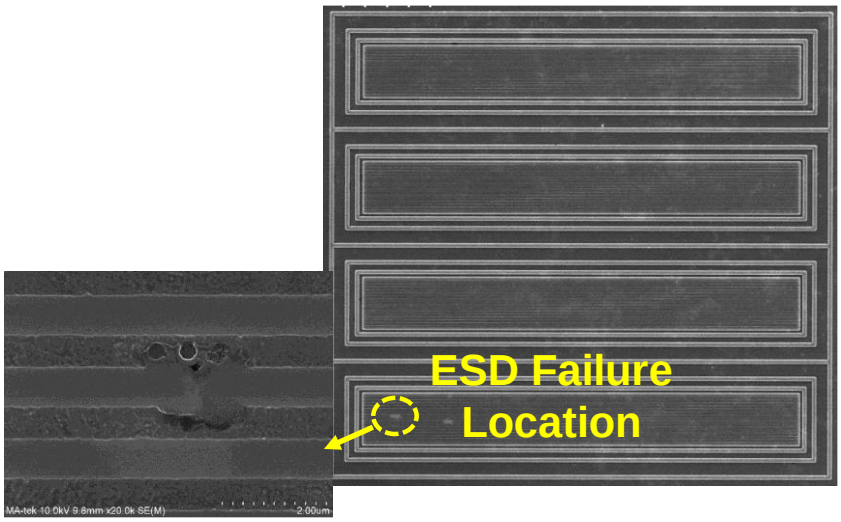


Fig. 3.5. The SEM image of 4 stacked LV-PMOS after 2500-V HBM ESD stress.

3.2.2 Comparison of ESD Performance between Stacked Low-Voltage Devices and High-Holding-Voltage SCR

In order to compare with the test results of the proposed HVSCRs in Chapter 2, the test results of the stacked 4 LV-PMOS and the HVSCR_B with PN-connection path are listed in Table 3.1, when considering the latchup immunity in the 20-V circuit applications. The holding voltage of the HVSCR_B with PN-connection path is ~21 V, which is immune to latchup danger in the 20-V circuit applications. However, its HBM ESD level per layout area is only ~0.107 (V/μm^2), which is much lower than the test result of LV-PMOS stack (~0.195 V/μm^2). Although

the proposed HVSCR_B can avoid latchup issue in this HV application, it still needs some optimization to improve its weak ESD performance. As reported in Chapter 2, the Joule-heating effect could dramatically decrease the holding voltage of the proposed SCR even if it was fabricated in a six-layer p-n-p-n-p-n structure. On the contrary, there is no degradation on holding voltage from the DC measurements with the stacked LV devices.

In consequence, the stacked configuration of LV devices is an efficient way to achieve both effective ESD protection and latchup-free design, as compared to the special modified HV devices, in the HV BCD process. Moreover, the characteristics of stacked LV devices with different layout designs are further investigated and reported in the related studies [25], [26].

Table 3.1

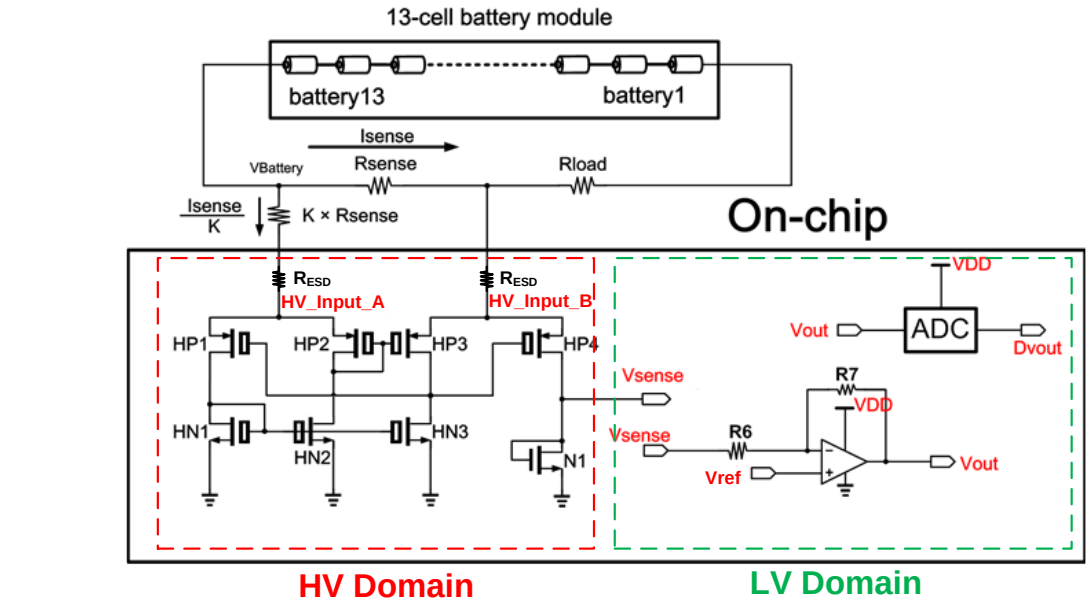
Comparison of ESD Performance of Stacked LV-PMOS and HVSCR_B

Device Type	LV-PMOS (Standard Type)	HVSCR_B (with PN Path)
Technology	0.25-μm HV BCD	0.25-μm HV BCD
W/L of each Device (μm)	800/0.5	200
Stacking Number	4	1
Layout Area (μm^2)	12356	9313
V_{BD} (V)	36	34
DC V_{hold} (V)	37	21.4
TLP V_{hold} (V)	36	33.8
TLP I_{t2} (A)	1.6	0.47
HBM Level (V)	2400	1000
HBM / Layout Area ($V/\mu m^2$)	0.195	0.107
ESD Robustness	Good	Bad
Latchup Issue for 20-V Application	Safe	Safe

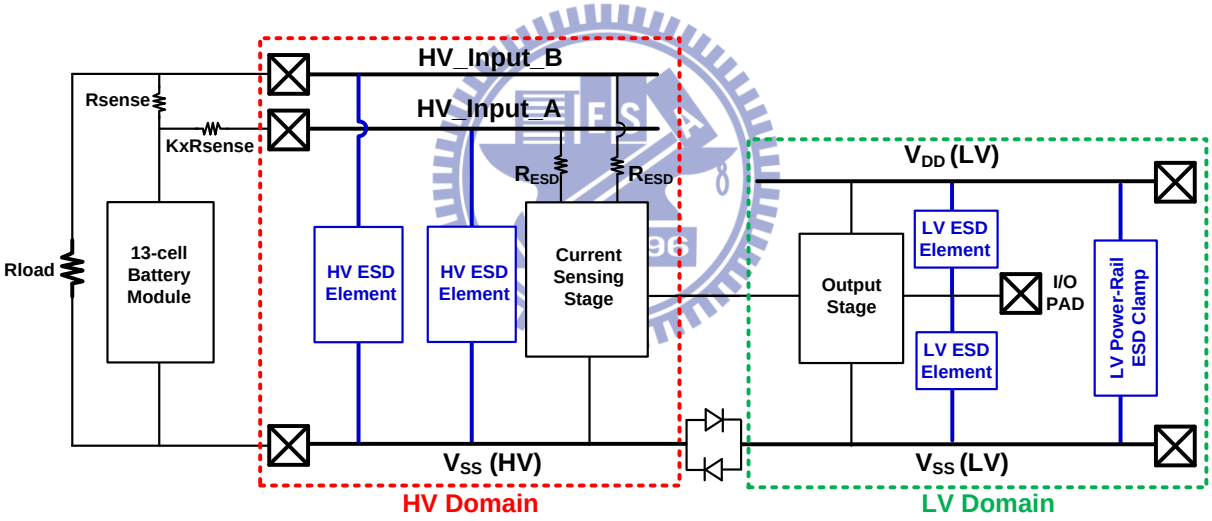
3.3 ESD Protection Design with Stacked Low-Voltage P-type Devices for High-Voltage Pins of Battery-Monitoring IC

This work continues to verify the stacked configuration of LV devices for the HV application. The structures of the stacked LV devices and its ESD protection effectiveness for the 60-V pins of a battery-monitoring IC are proposed and verified in a 0.25-μm 5/40/60V BCD process.

The circuit scheme of the battery-monitoring IC realized in this work is shown in Fig. 3.6(a), where the HV and LV devices are realized with 60-V and 5-V standard devices, respectively, in this 0.25-μm HV BCD process. The operating voltage of VDD (LV) pin is 5 V, and the battery voltage is ~55 V at HV input pins A and B (Va and Vb). This circuit is designed to sense the battery current by HV input pins A and B (Va and Vb) for power management system in the electrical vehicles. Fig. 3.6(b) shows the scheme of whole-chip ESD protection design for this battery-monitoring IC including HV and LV domains. In LV domain, the circuit block of output stage is protected by the LV ESD protection elements and LV power-rail ESD clamp between VDD (LV) and VSS (LV) power rails. In HV domain, the circuit block of current sensing stage is protected by HV ESD protection elements which consist of the stacked LV devices. The LV-PMOS and p-type field-oxide device (LV-PFOD) are used in this work. Fig. 3.7 shows the micrograph of whole chip including the battery-monitoring IC and ESD protection devices, which has been fabricated in this 0.25-μm 5/40/60V BCD process.



(a)



(b)

Fig. 3.6. (a) Circuit scheme of the battery-monitoring IC. (b) Whole-chip ESD protection scheme for the battery-monitoring IC.

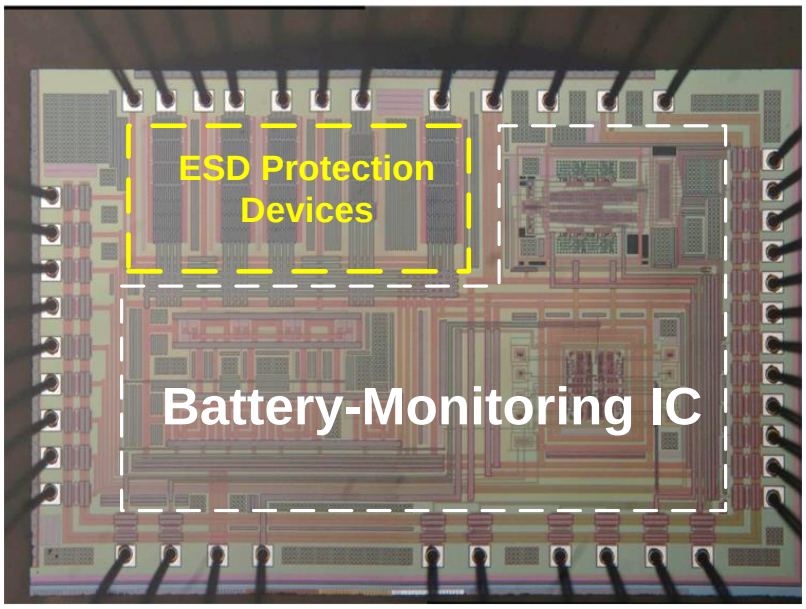
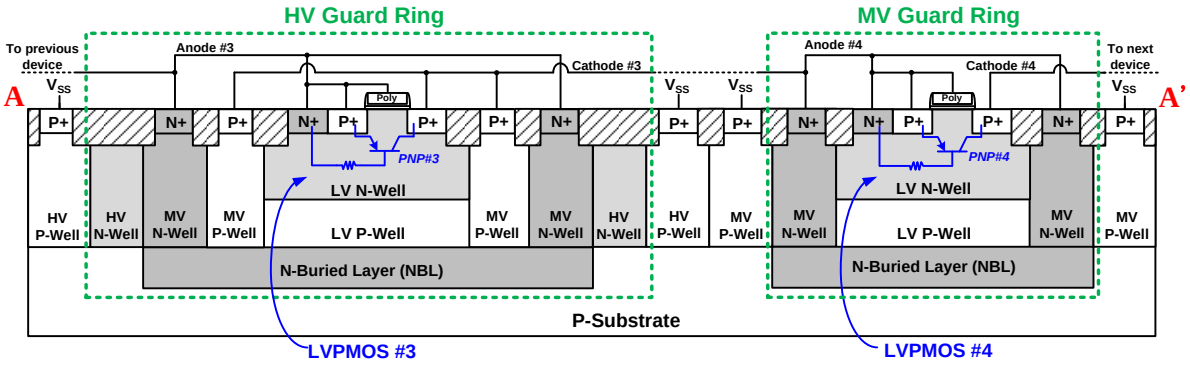


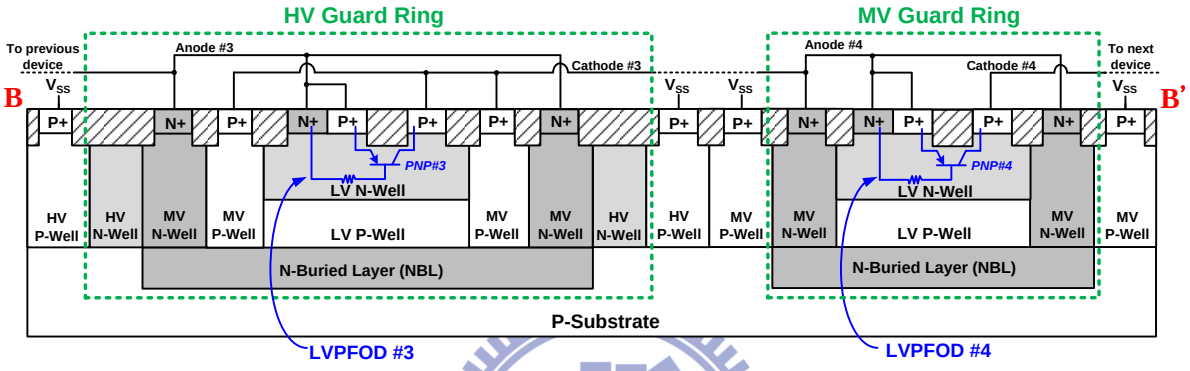
Fig. 3.7. Micrograph of whole chip fabricated in a 0.25-μm 5/40/60 V BCD process.

3.3.1 Proposed Stacked LV Devices for HV Input Pins

Figs. 3.8(a) and 3.8(b) show the cross-sectional view of the stacked LV-PMOS and LV-PFOD, respectively, where the MV n-well, HV n-well, and NBL are used to isolate the bias between the body of each device and the common p-type substrate to avoid breakdown when the HV signal is applied. According to the foundry-provided information, the maximum breakdown voltage between MV n-well and MV p-well is ~50 V, and between HV n-well and HV p-well is ~100 V, which should be taken into consideration when they are used in the stacked structure. FOD device features a gate-less structure compared to MOS device. Their inherent parasitic PNP BJTs, as main ESD dissipation path, are also designated in these plots. The device dimension of each LV-PMOS is chosen as W/L of 2400 μm / 0.5 μm with minimum layout spacing at drain and source sides to guarantee its high ESD robustness and to minimize the silicon area. The device dimension of each LV-PFOD is chosen the same as that of LV-PMOS. The drain-to-source breakdown voltage (BV) of each LV-PMOS or LV-PFOD is ~9 V in the given process. Thus, the stacked number is chosen as 7, so the total BV is adjusted to be over 60 V to sustain the input signal of ~55 V at the HV input pins.



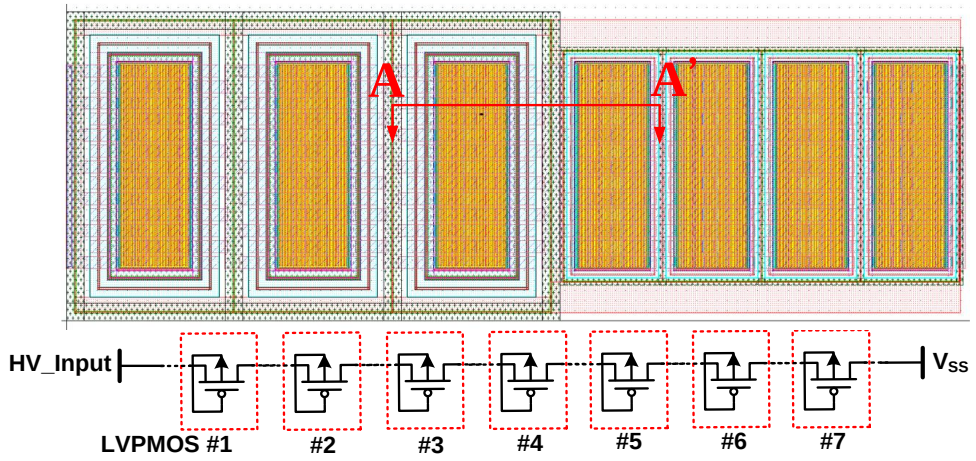
(a)



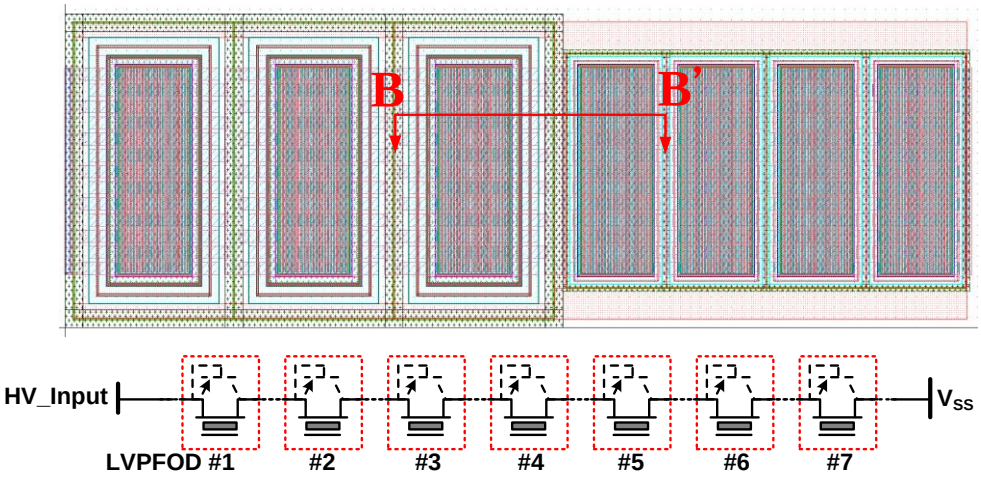
(b)

Fig. 3.8. Cross-sectional views of 2 cascaded devices with (a) LV-PMOS and (b) LV-PFOD, respectively.

The layout top view of 7 stacked devices with LV-PMOS and LV-PFOD are shown in Figs. 3.9(a) and 3.9(b), respectively. The cross-sectional views of 2 cascaded devices along the A-A' and B-B' lines in Figs. 3.9(a) and 3.9(b) can correspond to Figs. 3.8(a) and 3.8(b), respectively. In consideration of a high voltage drop at the junction of the anode-connected LV n-well of the first 3 cascaded devices to the common p-type substrate when the stacked devices are triggered on by ESD stress, the HV guard rings is individually used for them to avoid the unwanted junction breakdown. The last 4 cascaded devices are individually surrounded by the MV guard rings due to the lower voltage drop at the junction of the MV n-well and the MV p-well, which can save the area footprint of the stacked structure.



(a)



(b)

Fig. 3.9. Layout top views of (a) 7 stacked LV-PMOS and (b) 7 stacked LV-PFOD, respectively.

3.3.2 ESD Robustness of Proposed Design

To investigate the turn-on behavior of ESD device during high ESD current stress, the TLP generator with a pulse width of 100 ns and a rise time of 10 ns is used to measure the snapback I-V curves of the stacked devices. The TLP-measured I-V curves of these two stacked structures are shown in Fig. 3.10 and the test results are listed in Table 3.2. The ESD robustness is measured by the ESD tester with HBM model. The TLP-measured failure current (I_{t2}) of stacked LV-PMOS and LV-PFOD are 5.37 A and 5.18 A, respectively. The holding voltage (V_{hold}) of these two stacked structures are both higher than ~55 V to avoid the latchup risk, and

their BV are higher than ~60 V as expected. The stacked LV-PMOS shows its HBM level of 6.5 kV, and stacked LV-PFOD shows over 8 kV. The holding voltage and on-state resistance (Ron) of LV-PFOD are higher than that of LV-PMOS because the thick oxide structure in FOD not only reduces the beta gains of intrinsic PNP BJTs but also increases its series resistance.

Furthermore, it is found that the TLP-measured failure current is not so consistent with the HBM level from the measurement results of stacked LV-PMOS. The failure mechanism of such inconsistent phenomenon had been reported in the literature [27]–[29]. This may be attributed to the gate oxide (GOX) failure under HBM ESD test. The device that has thin gate oxide structure can be easily damaged during HBM ESD stress to cause a miscorrelation between TLP and HBM ESD test results.

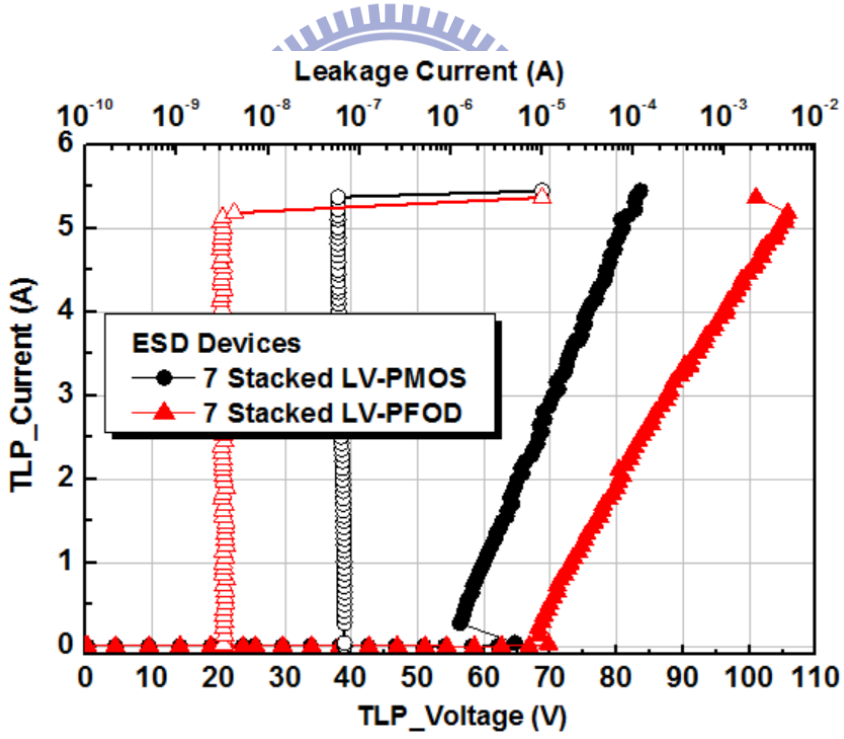


Fig. 3.10. TLP-measured I-V curves of stacked LV-PMOS (black dot) and LV-PFOD (red dot).

Table 3.2

Comparison of ESD Performance of Stacked LV-PMOS and LV-PFOD

Device Type	LV-PMOS	LV-PFOD
Stacking Number	7	7
Layout Area (μm^2)	153 x 440	153 x 440
W/L of each Device (μm)	2400/0.5	2400/0.5
BV (V)	61.54	66.12
TLP V_{hold} (V)	56.35	68.19
TLP I_{t2} (A)	5.37	5.18
HBM Level (V)	6500	> 8000 *
I_{t2} / Layout area ($mA/\mu m^2$)	0.079	0.077
* limited by ESD test equipment.		

3.3.3 Verification of ESD Protection on HV Input Pin

To verify ESD protection effectiveness of the stacked devices to protect the HV input pin, the measurement setup is shown in Fig. 3.11. HV input pin (Va or Vb) is connected in parallel with stacked devices under HBM ESD test. The resistance R_{ESD}, chosen as 2kΩ, is used to limit HBM ESD current into HV circuit block, but not disturb the normal HV circuit function. After every HBM ESD stress, the leakage current of device under test (DUT) is measured with a ramped DC bias at room temperature (25 ºC) until breakdown occurs. When the leakage current abruptly increases up to 1 μA, the corresponding bias voltage is judged as the breakdown voltage. The failure criterion is that the post-stress I-V curve shows more than 10% deviation from its fresh I-V curve.

Fig. 3.12 shows the I-V curves of the HV input pin Vb without any ESD protection device. Its pure HBM ESD level is smaller than 0.5 kV. Then, the I-V curves of the HV pin Vb protected by the stacked LV devices are measured after each HBM ESD test, as shown in Figs. 3.13 and 3.14. In Fig. 3.13, the I-V curves of HV pin Vb with stacked LV-PMOS did not show any degradation after 6.5-kV HBM ESD test. However, after 7-kV HBM ESD stress, the I-V curve

of HV pin Vb with stacked LV-PMOS shifts over 10% from its original curve. Thus, the HBM ESD level of HV input pin protected by the stacked LV-PMOS is judged to be 6.5 kV. In Fig. 3.14, the I-V curves of HV pin Vb with stacked LV-PFOD did not show any obvious degradation after 8-kV HBM ESD stress. Thus, the HBM ESD level of the HV pin Vb protected by the stacked LV-PFOD can be over 8 kV. The ESD test results on the HV pin Va are the same as those of HV pin Vb, due to the symmetric circuit structure in the current sensing stage. The test results are also summarized in Table 3.3. Without using the stacked LV-PMOS or LV-PFOD to protect the HV pin, its original HBM ESD level is below 500 V. Through the practical ESD test on the silicon chip, it has been verified that the stacked LV devices can provide effective ESD protection for those 60-V HV pins in the battery-monitoring IC.

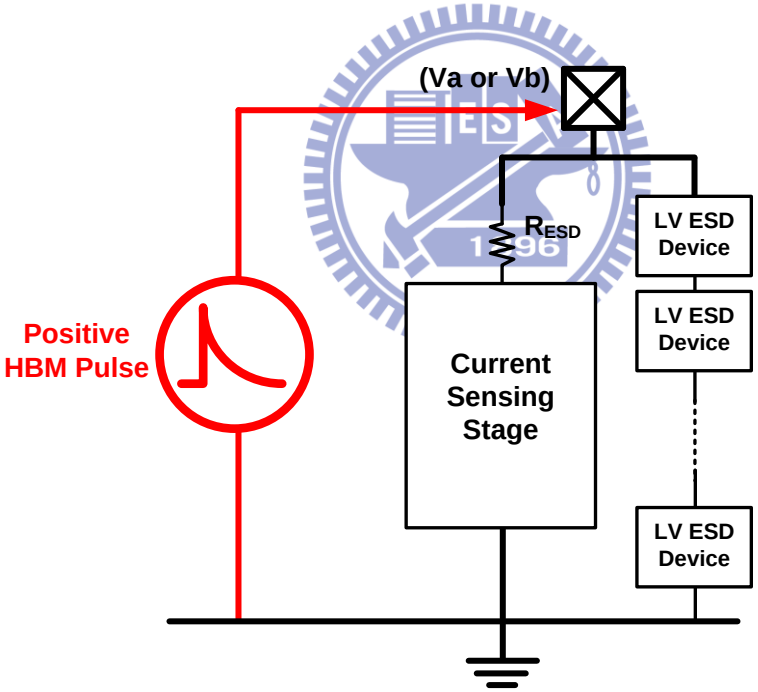


Fig. 3.11. Measurement setup for HBM ESD test on the HV input pin (Va or Vb) protected by the stacked LV devices.

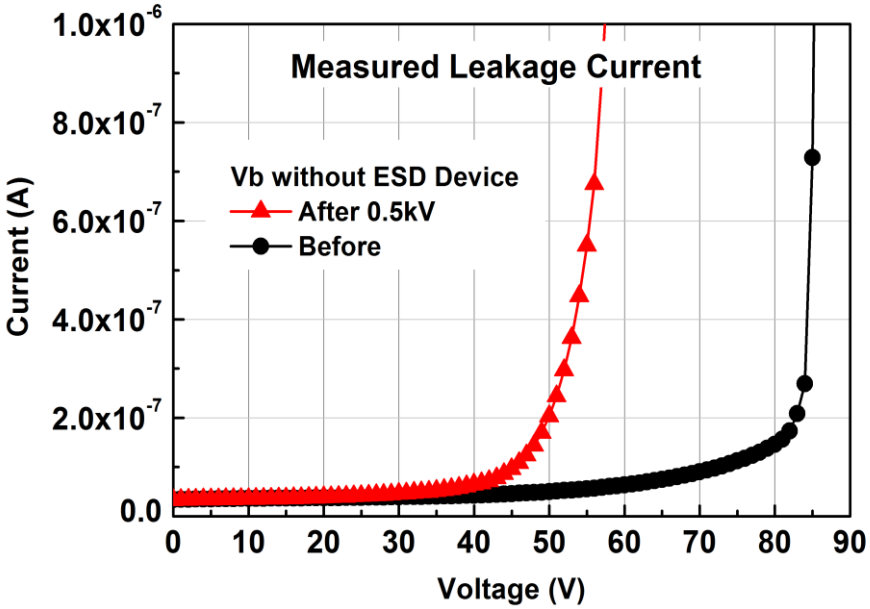


Fig. 3.12. Measured leakage currents of HV pin Vb after each HBM ESD test.

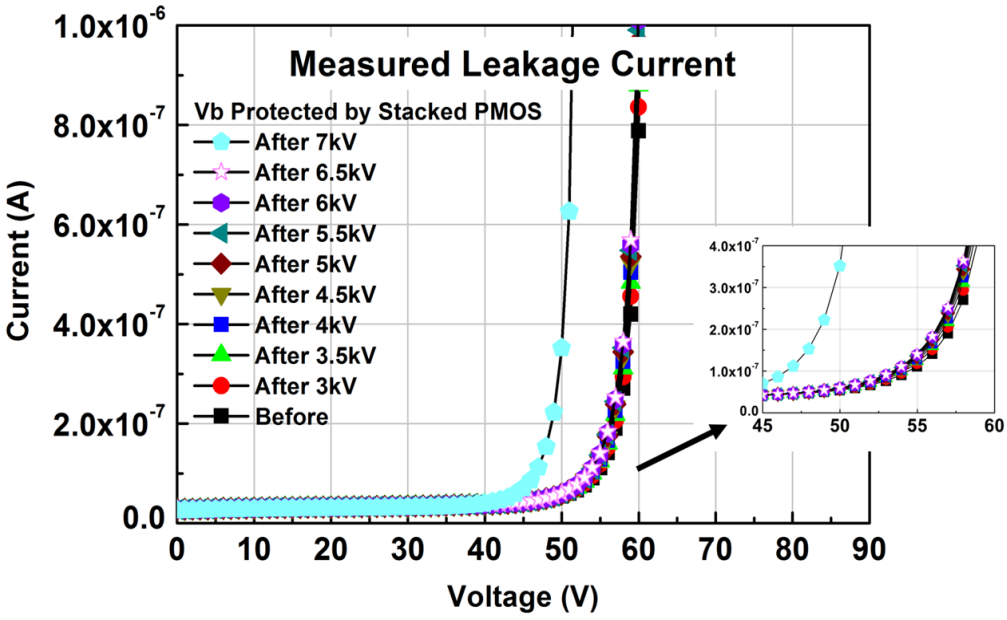


Fig. 3.13. Measured leakage current on the HV pin Vb, protected by the stacked LV-PMOS, after each HBM ESD test.

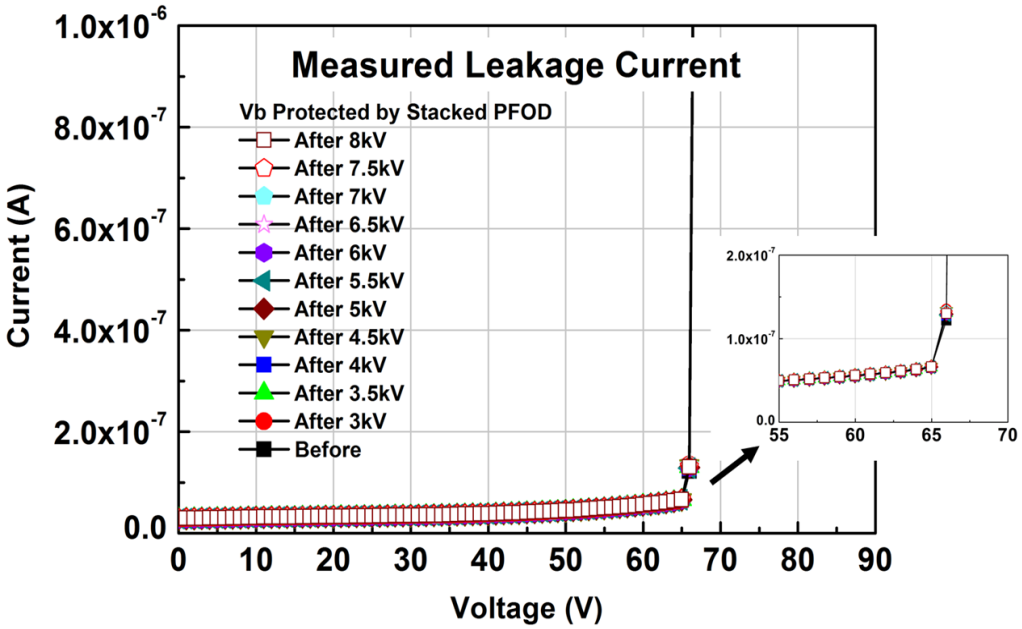


Fig. 3.14. Measured leakage current on the HV pin Vb, protected by the stacked LV-PFOD, after each HBM ESD test.

Table 3.3

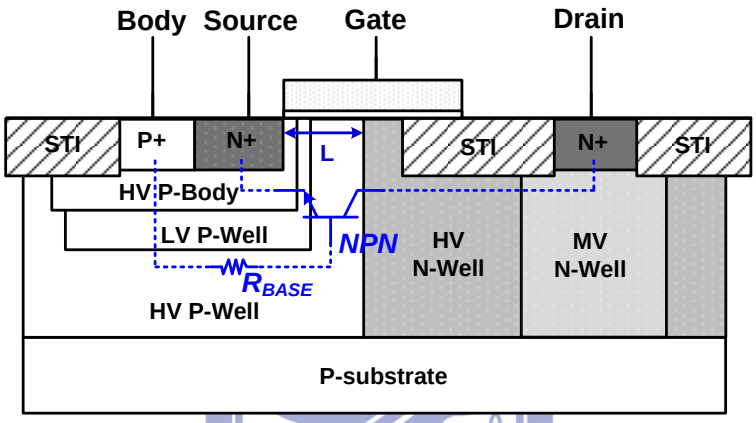
ESD Robustness of the HV Pin with/without ESD Protection Element

HV Pin with / without ESD Protection Element	HBM ESD Level (kV)
HV Pin (Va or Vb)	< 0.5
HV Pin (Va or Vb) with Stacked LV-PMOS	6.5
HV Pin (Va or Vb) with Stacked LV-PFOD	> 8

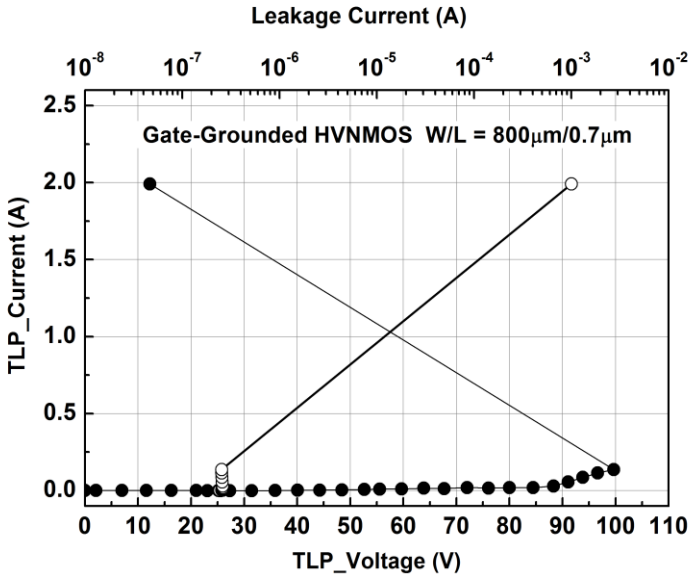
3.3.4 Discussion

To verify the intrinsic ESD robustness of 60-V nLDMOS in the given 0.25-μm HV BCD process, the stand-alone nLDMOS was also drawn and fabricated in the same process. The device structure of standard nLDMOS in this process is shown in Fig. 3.15(a). The multiple doping wells, such as HV p-body, LV p-well, and MV n-well, are used to maximize the device's

safe operating area (SOA) [19]. The TLP-measured I-V curves of stand-alone nLDMOS with W/L of 800 μm / 0.7 μm is shown in Fig. 3.15(b). The failure current of this HV NMOS is only ~0.2 A, even if its channel width is as large as 800 μm. The HBM ESD level of such a stand-alone HV NMOS is around ~300 V. The self-protection ability of such HV devices in the 0.25-μm HV BCD process against ESD stress is very weak. Thus, the ESD protection solution proposed in this work is an effective way to protect the HV CMOS ICs against ESD stress.



(a)



(b)

Fig. 3.15. (a) Device structure of the HV nLDMOS in a 0.25-μm HV BCD process. (b) TLP-measured I-V curves of the stand-alone HV nLDMOS with a W/L of 800 μm / 0.7 μm.

A Typical ESD protection design with different power-rail ESD clamp circuits in a CMOS IC with different power domains (e.g., VDD1 > VDD2 > VDD3 > VDD4) is illustrated in Fig. 3.16. The power-rail ESD clamp circuits should be added near those power pads for an effective ESD protection. However, it often consumes large silicon footprint with high fabrication cost to apply the corresponding HV ESD protection devices for their own power domain. Based on the proposed stacked LV devices in this work, the ESD protection elements with stacked configuration can be applied as the power-rail ESD clamps for the different power domains, as illustrated in Fig. 3.17. The different power domains can hence share some part of the stacked ESD protection elements for their own ESD protection. Moreover, by using this sharing path, only one ESD protection stack can handle the ESD protection not only in each power domain but also across the separated power domains. According to such design concept, LV-device stack can be an area-efficient way to implement the ESD protection networks in the HV BCD technologies. This design concept can be further studied and verified in the future work.

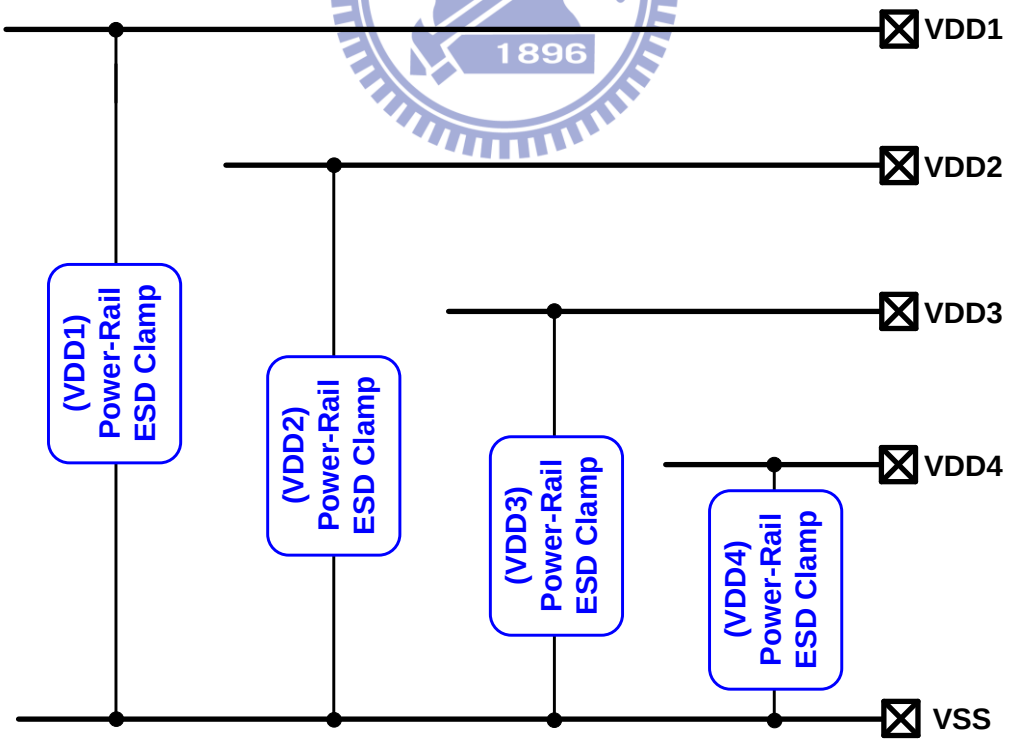


Fig. 3.16. Typical ESD protection design with different power-rail ESD clamp circuits in a CMOS IC with different power domains.

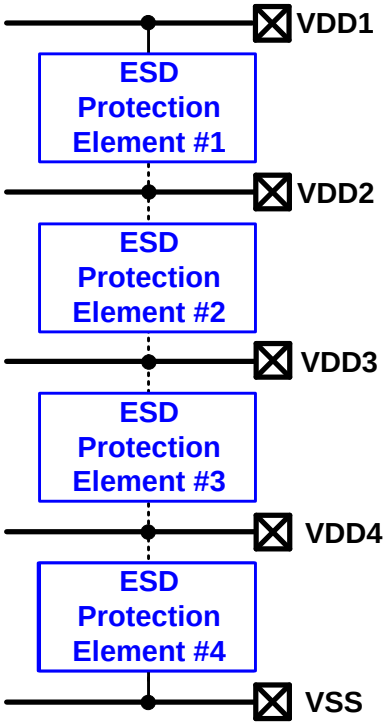


Fig. 3.17. One stacked ESD protection elements for power-rail ESD protection across different power domains.

3.4 Summary

In this chapter, HV ESD protection design realized by stacked LV devices has been proposed and verified in a 0.25-μm 5/40/60V BCD process. By adjusting the stacking number of LV devices, the total holding voltage and total breakdown voltage of the stacked devices can be higher than the maximum supply voltage of the protected pins to avoid either latchup issue or breakdown event during the normal HV circuit operation. From the experimental results, the stacked LV devices can successfully protect the 60-V input pin of HV circuit block against 8-kV HBM ESD stress. Stacked structure of LV devices can be an appropriate ESD protection solution to fit the required ESD protection window in the various high-voltage applications, without developing special modification on the HV devices with additional mask layers and process steps. Moreover, stacked LV devices with sharing path technique can be more area-efficient to implement the whole-chip ESD protection in the HV BCD technologies.

Chapter 4

Optimization of Guard Ring Structures to Improve Latchup Immunity in a High-Voltage DDDMOS Process

4.1 Background

Latchup is one of the most important reliability issue to CMOS ICs, especially in the HV applications. Due to the high circuit-operating voltage and structure complexity of HV devices, HV CMOS ICs would be seriously damaged by the latchup-generated high power if latchup was triggered. In order to suppress the occurrence of latchup event, many techniques had been reported by applying process modulation [30], [31], layout optimization [32]–[35], or even circuit design of active guard ring [36]. Among the previous studies, inserting the double guard rings with grounded p-well ring and VDD-connected n-well ring in the latchup path to absorb both majority and minority carriers is one of the most effective designs. However, there was less study to investigate the influence of guard ring structures of the double-diffused drain MOS (DDDMOS) device and their layout parameters on latchup immunity in the HV DDDMOS technology. This HV DDDMOS technology features multiple voltage levels with various types of devices such as CMOS, DDDMOS, and BJT devices. The n-type and p-type well structures with different doping levels and junction depths in this process would greatly influence the latchup occurrence.

In this work, the latchup characteristics of DDDMOS transistors with the different guard ring structures are investigated in silicon through the latchup trigger current test (I-test). The related methods and test procedures to investigate the latchup immunity of integrated circuits with latchup trigger current test had been defined in the Joint Electron Device Engineering Council (JEDEC) standards [37]. The trigger characterizations for latchup I-test are defined in

the up-to-dated standard (JESD78E), where the highest latchup I-test level has been specified of greater than 100 mA. Accordingly, nowadays many IC design houses develop their IC products with latchup immunity of over ±100 mA current trigger as their desired specification. In addition, layout parameters such as the anode-to-cathode spacing and the guard ring width are also studied to find their impacts on latchup immunity. In order to verify the holding voltage of HV latchup test structures, the DC curve tracer (Tek370B) is also used. It is demonstrated that the test devices isolated with the specific guard ring structure of n-buried layer (NBL) and double-diffused layer can highly improve the latchup immunity in this 18-V DDDMOS process.

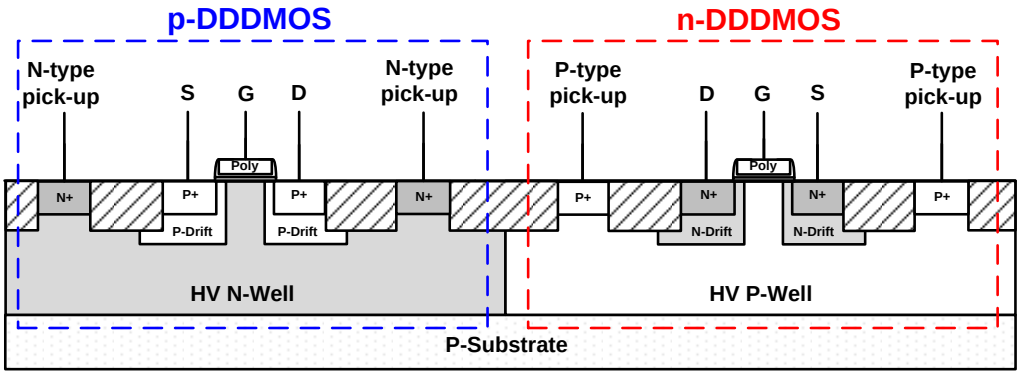


Fig. 4.1. Device structures of p-type and n-type DDDMOS transistors in an 18-V DDDMOS technology.

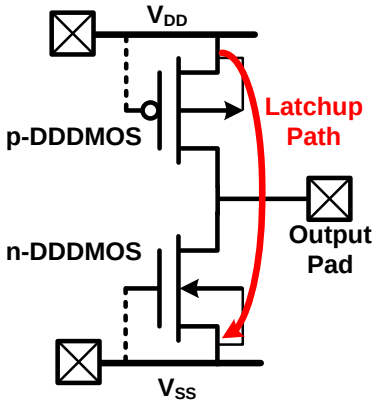


Fig. 4.2. Circuit scheme of the proposed test structure with p-type and n-type DDDMOS transistors, which is used to simulate an output buffer in the I/O cells.

4.2 Proposed Test Structures

The devices studied in this work are implemented in an 18-V DDDMOS technology. The device structures of p-type and n-type DDDMOS transistors are shown in Fig. 4.1, where the drift regions under both drain and source sides of each device are used to increase the junction breakdown voltage to sustain high operating voltage. In HV CMOS ICs, the latchup path in I/O cells was often triggered by external overshooting or undershooting voltage/current glitches. In this work, the optimization of layout rules and guard ring structures is investigated to improve latchup immunity in an output buffer. The proposed test structures are drawn with the p-type and n-type DDDMOS transistors, as illustrated in Fig. 4.2, where the latchup path exists from the VDD-connected source of the p-DDDMOS, through the HV n-well and HV p-well, to the VSS-connected source of the n-DDDMOS. The channels of both DDDMOS devices are kept in off state by connecting its gate to its source for studying the influence of layout structure on latchup.

Figs. 4.3(a), 4.3(b), 4.3(c), and 4.3(d) show the cross-sectional view of different guard-ring test structures of with type A, B, C, and D, respectively. To get better latchup immunity, all the test transistors are surrounded by guard rings. Test structure A consists of a pair of p-DDDMOS and n-DDDMOS. Each transistor is surrounded by only one guard ring, which is the base guard ring of each transistor. This structure is used as a reference structure for comparing with other test structures. Test structure B consists of the transistors pair that each transistor is surrounded by double guard rings. The second guard ring, which encircles the first guard ring of each transistor, is used to collect the minority carriers in the p-substrate. Test structure C consists of the transistors pair surrounded by double guard rings, but an n-buried layer (NBL) is added under n-DDDMOS. Test structure D consists of the transistors pair surrounded by double guard rings, with two NBL layers added under the p-DDDMOS and the n-DDDMOS, respectively.

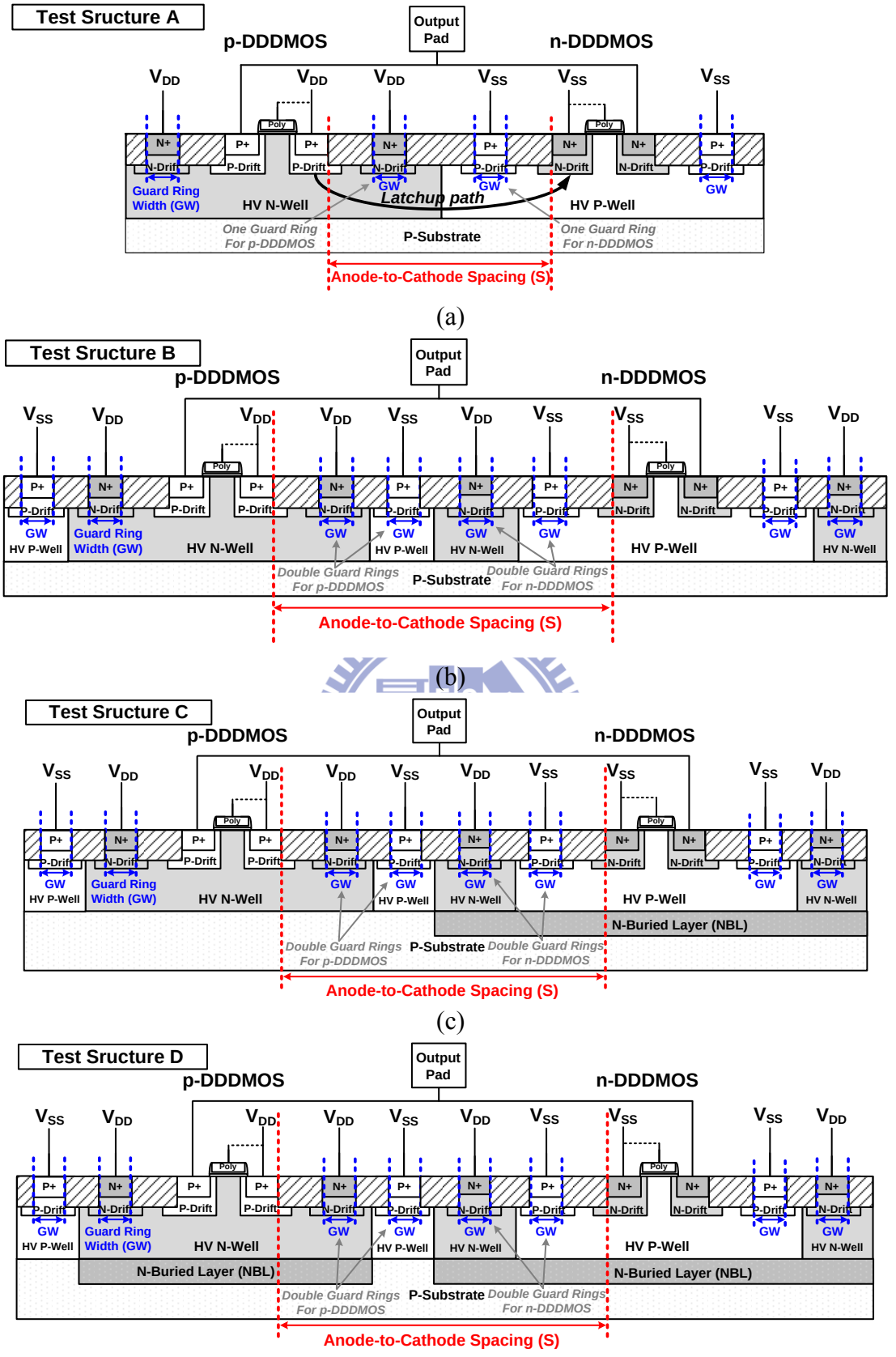


Fig. 4.3. Device cross-sectional views of the proposed latchup test structures (a) A, (b) B, (c) C, and (d) D, with a pair of p- and n-DDDMOS transistors in each test structure.

Compared with test structures A and B, the n-DDDMOS in test structures C and D is totally isolated from the p-substrate. The NBL structure is used to further improve the guard ring efficiency. In addition, some layout parameters such as the anode-to-cathode spacing (S) and the guard ring width (GW) are investigated. The improvement obtained by adding double-diffused regions (n-drift or p-drift layers) under the guard rings are also studied. The simplified layout top views of latchup test unit for test structures A, B, C, and D are shown in Fig. 4.4, indicating the related layout parameters.

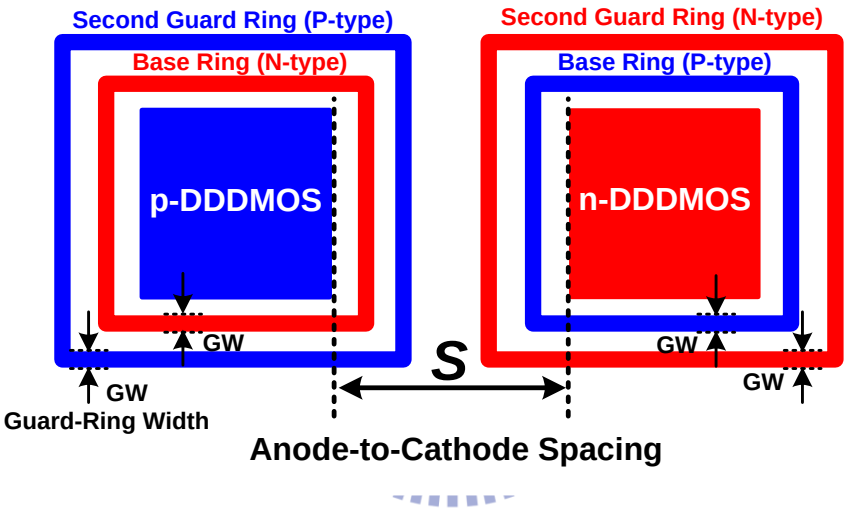


Fig. 4.4. Simplified layout top view of latchup test unit for the test structures A, B, C, and D.

4.3 Experimental Results

4.3.1 DC I–V Characteristics

To investigate the latchup characteristics of the proposed test structures, the latchup DC I–V curves are measured by Tek370B curve tracer. All the test results are measured at a room temperature of 25 °C. If the holding voltage of these test structures is greater than VDD, the latchup occurrence can be avoided. The I–V characteristics traced from VDD to VSS of the test structures with a minimum anode-to-cathode spacing of 13.4 μm and a guard ring width of 1 μm is shown in Fig. 4.5, where the holing voltage of those test structures are all bellow 5 V. It

implies that the latchup paths in the test structures C and D will be still induced even with the NBL to isolate the devices. As shown in Fig. 4.6, when the anode-to-cathode spacing is increased to 20 μm, the trigger voltage and holding voltage of all test structures are slightly increased. As shown in Fig. 4.7, when the anode-to-cathode spacing is increased to 30 μm, the trigger voltage and holding voltage of all test structures are moderately increased, but the holding voltage is still lower than the operating voltage VDD of 18 V in the given process. Even extending the guard ring width to 3 μm, the holding voltage of all test structures is still lower than the operating voltage of 18 V. Among the test structures, the test structure D has the highest DC trigger (the switching point) current, and test structure A has the lowest one. A higher trigger current means a better latchup immunity, which can be further verified in the JEDEC latchup trigger current test.

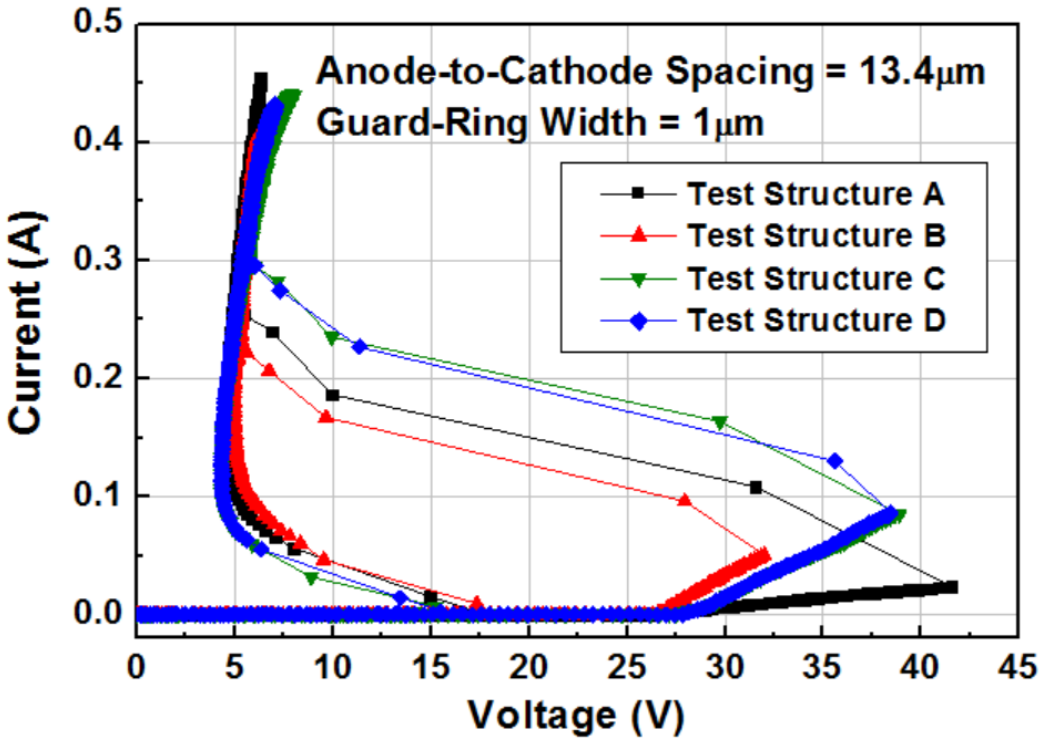


Fig. 4.5. Latchup I–V characteristics of different test structures measured from VDD to VSS with S of 13.4 μm, under the same guard ring width of 1 μm.

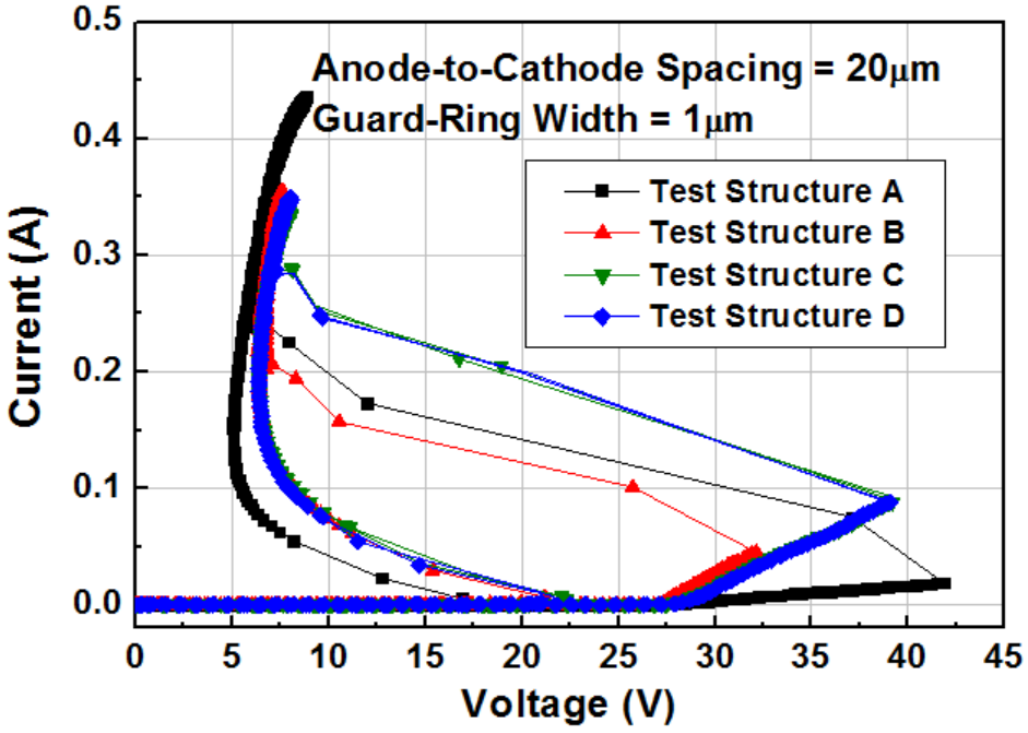


Fig. 4.6. Latchup I–V characteristics of different test structures measured from VDD to VSS with S of 20 μm, under the same guard ring width of 1 μm.

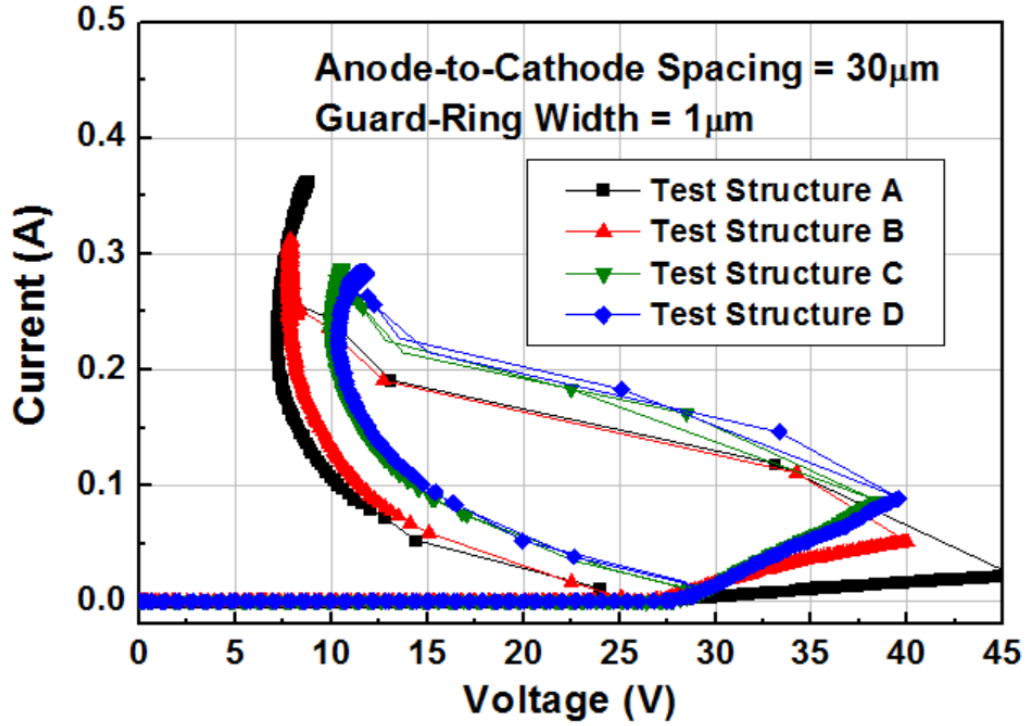


Fig. 4.7. Latchup I–V characteristics of different test structures measured from VDD to VSS with S of 30 μm, under the same guard ring width of 1 μm.

4.3.2 Latchup Trigger Current Test

Because the holding voltages of test structures are all smaller than the operating voltage VDD of 18 V in the given process, there is another way to verify their latchup immunity by using the latchup trigger current test specified in the JEDEC standard (JESD78E). The measurement setup of JEDEC latchup trigger current test applied to the output buffer is exploited in Fig. 4.8, with an 18 V supply at VDD pin, a current pulse generator applied to the output pin, and an oscilloscope to monitor the waveforms of the VDD pin voltage and the injected current. The positive or negative trigger current pulse from the pulse generator is injected to the output pin of the test structure to investigate whether the latchup is triggered on, or not. If the test structure is triggered into latchup, a decrease on the voltage waveform of VDD pin can be found to judge the occurrence of latchup.

The measured waveforms of test structure A with the anode-to-cathode spacing of 13.4 μm and the guard ring width of 1 μm, under the negative trigger current test with trigger current pulses of -100 and -300 mA, are shown in Figs. 4.9(a) and 4.9(b), respectively. To avoid electrical overstress (EOS) events and to successfully detect the fired latchup state of the test structure, the pulse width is chosen as 1 ms, and the pulse step is 100 mA.

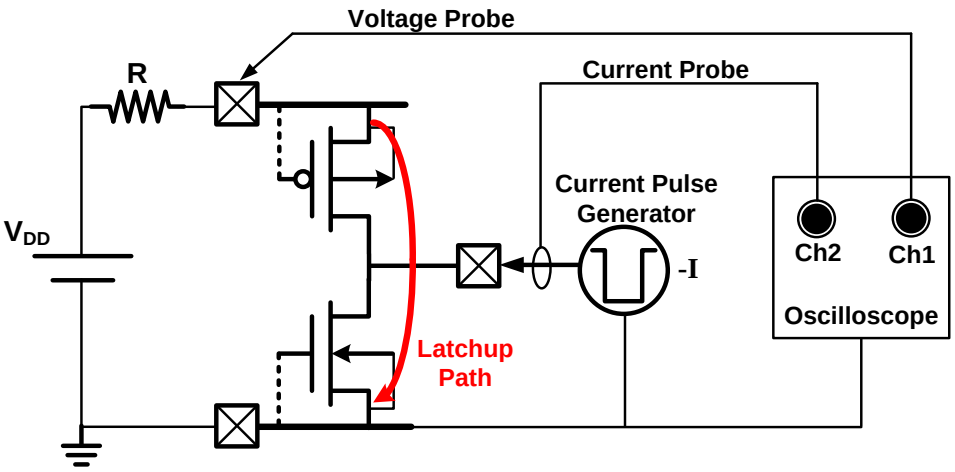
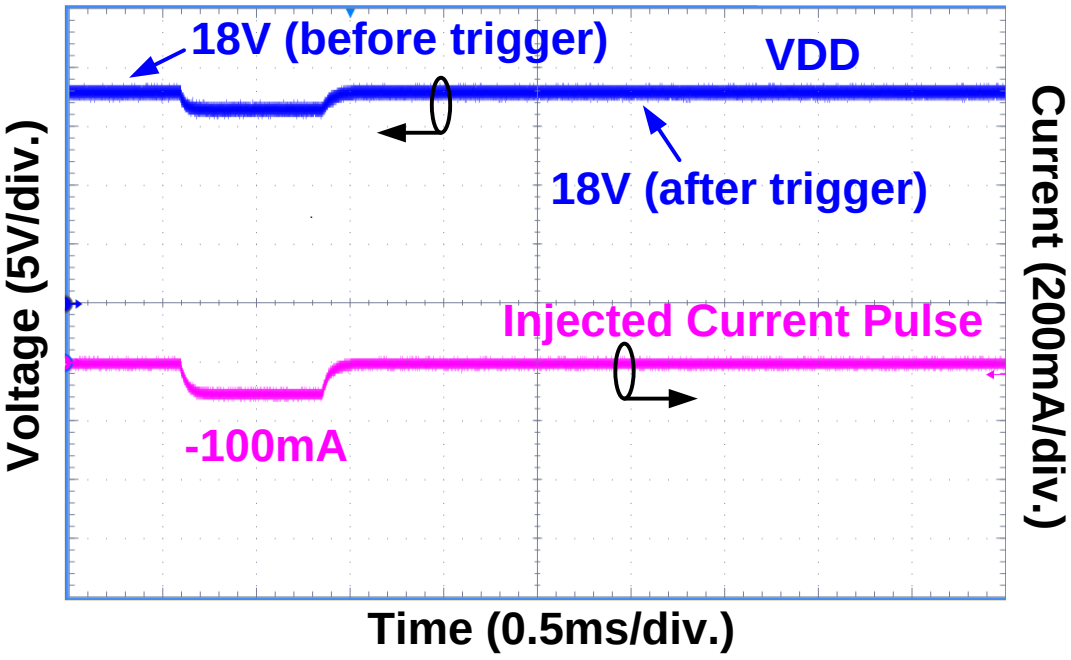
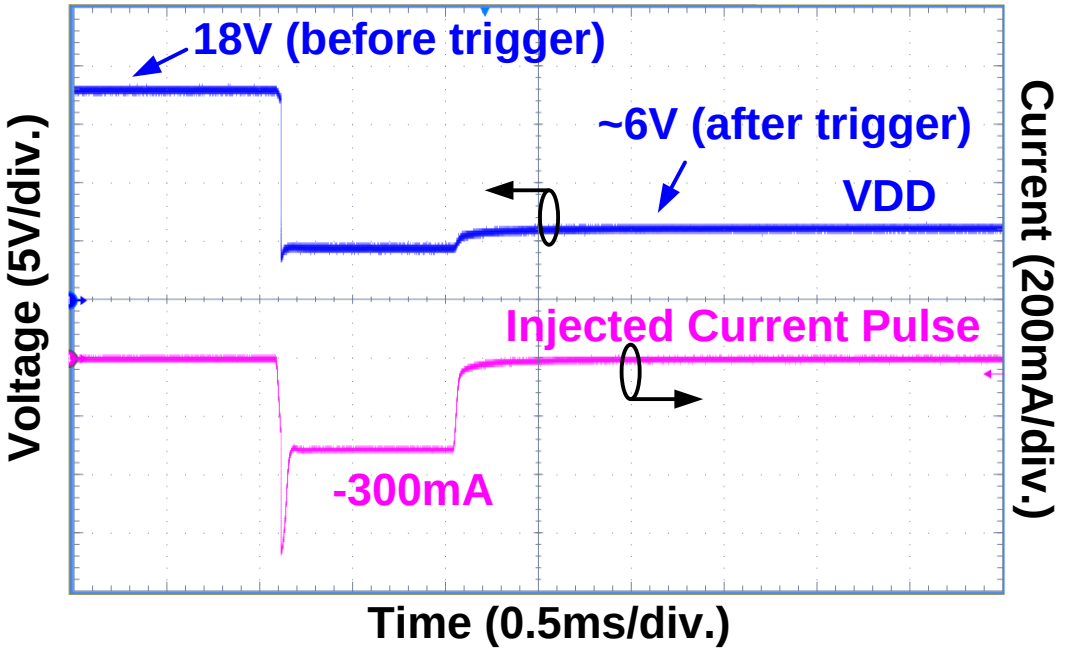


Fig. 4.8. Latchup test for the test structures with the positive or negative latchup trigger current at each output pad.



(a)



(b)

Fig. 4.9. Measured waveforms of test structure A under negative latchup trigger current test with the trigger current of (a) -100-mA, and (b) -300-mA, injected to the output pad.

The voltage at VDD pin is kept at 18 V if the applied trigger current at the output pad did not fire on the latchup path of the test structure, as shown in Fig. 4.9(a). But the voltage at VDD

pin is dropped down to ~6 V while the latchup path is triggered on, as that shown in Fig. 4.9(b). The initial undershooting glitch in the negative trigger current waveform is caused by the current compensation in the current pulse generator, which can be ignored. Thus, by adjusting the trigger current level with repeated experimental procedures, the threshold level of trigger current to initiate latchup occurrence can be found.

Furthermore, more detailed examinations to verify the latchup immunity are measured by using a latchup test machine, Thermo Scientific MK.1, with 10-ms pulse width and 25-mA pulse step. Fig. 4.10 shows the measured relations between the positive latchup trigger current under the different anode-to-cathode spacings of 13.4, 20, and 30 μm for different test structures but with the same guard ring width of 1 μm. In the figure, the test structure w/o drift means that the drift layers are not added under the guard rings in the test structure. The latchup trigger current of all test structures are moderately increased by the increase of anode-to-cathode spacing. Among the test results of different test structures with the same anode-to-cathode spacing, the test structure A has the lowest latchup trigger current, below 150 mA, because the devices in this structure A are only surrounded by the base guard rings. Test structure B has a higher latchup trigger current than that of test structure A due to use of the double guard rings. By using the double guard rings as well as the NBL to isolate the devices, both test structures C and D have almost the same latchup trigger currents of above 600 mA, and exhibit the highest current level among the test structures. In addition, the drift layers under the guard rings can increase the latchup trigger current by at least 25 mA, compared with the results of those structures without drift layers. As the measured results in Fig.9, the test structure D can sustain the positive latchup trigger current of over 800 mA, when its anode-to-cathode spacing is 30 μm.

Fig. 4.11 shows the measured relations of different test structures between the positive latchup trigger current and the different anode-to-cathode spacings of 16.5, 20, and 30 μm under the same guard ring width of 2 μm. The positive latchup trigger current of all test structures are

moderately increased by the increase of the anode-to-cathode spacing. Fig. 4.12 shows the measured relations of different test structures between the positive latchup trigger current and the different guard ring widths of 1, 2, and 3 μm under the same anode-to-cathode spacing of 20 μm. For the test structures A, the increased guard ring width can improve the positive current level greatly. However, for test structures B, C, and D, the current level can only be improved slightly by the increased guard ring width. From the comparison of test results between the test structures B and C, the guard ring efficiency in n-DDDMOS can be improved greatly by using the NBL layer. That is, adding NBL under the n-type device can greatly improve the latchup immunity in positive latchup trigger current test. As the measured results in Fig. 4.12, the test structure D with a guard ring width of 3 μm and the anode-to-cathode spacing of 20 μm can sustain the positive latchup trigger current of up to 900 mA.

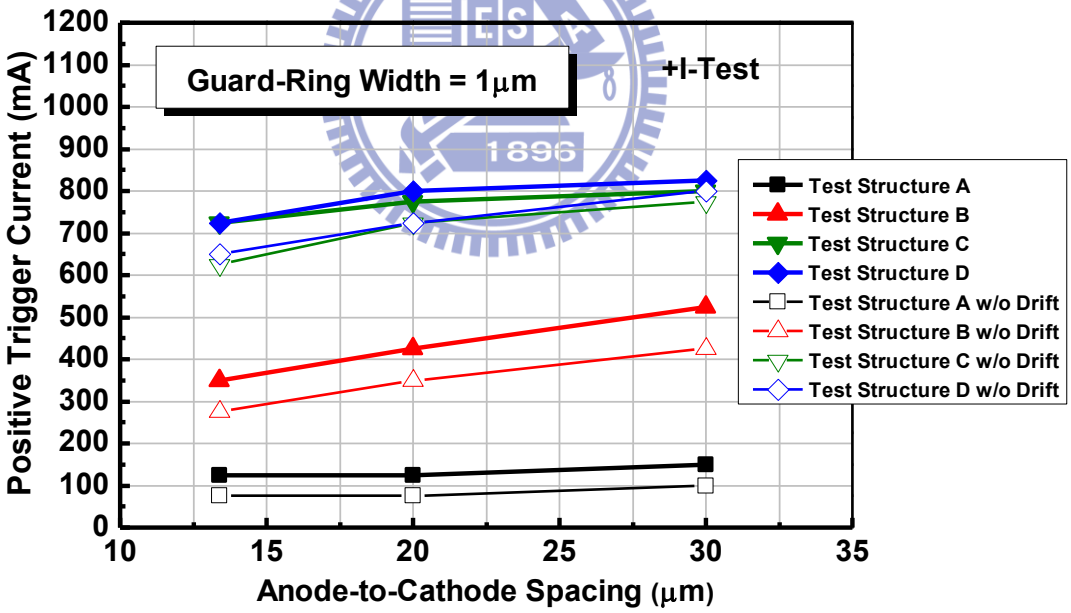


Fig. 4.10. Relations between the positive latchup trigger current on output pad and the anode-to-cathode spacings of 13.4, 20, and 30 μm for different test structures A, B, C, and D under the same guard ring width of 1 μm.

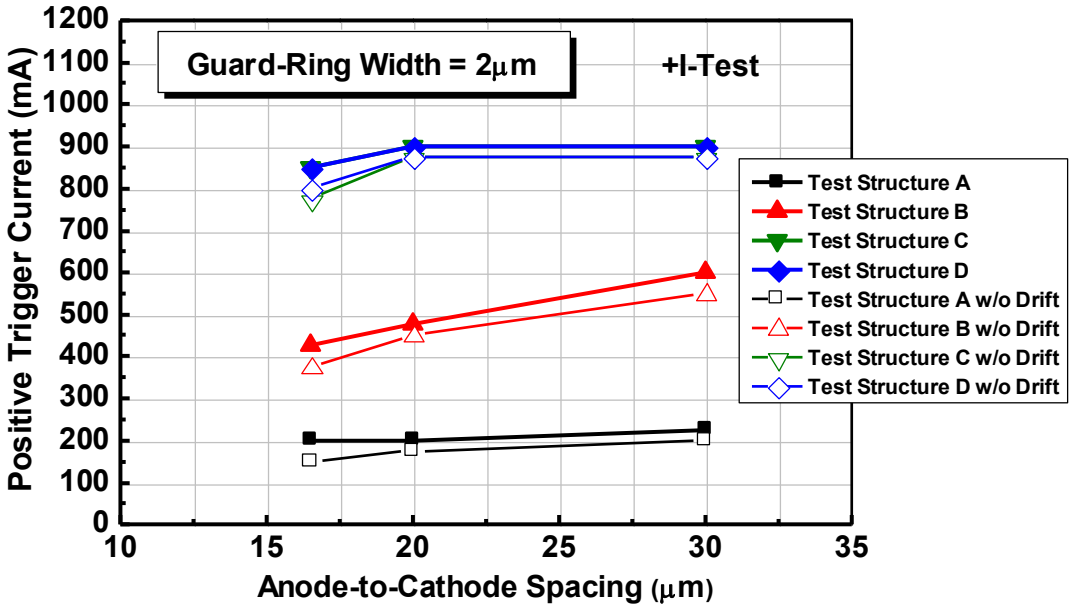


Fig. 4.11. Relations between the positive latchup trigger current on output pad and the anode-to-cathode spacings of 16.5, 20, and 30 μm for different test structures A, B, C, and D under the same guard ring width of 2 μm.

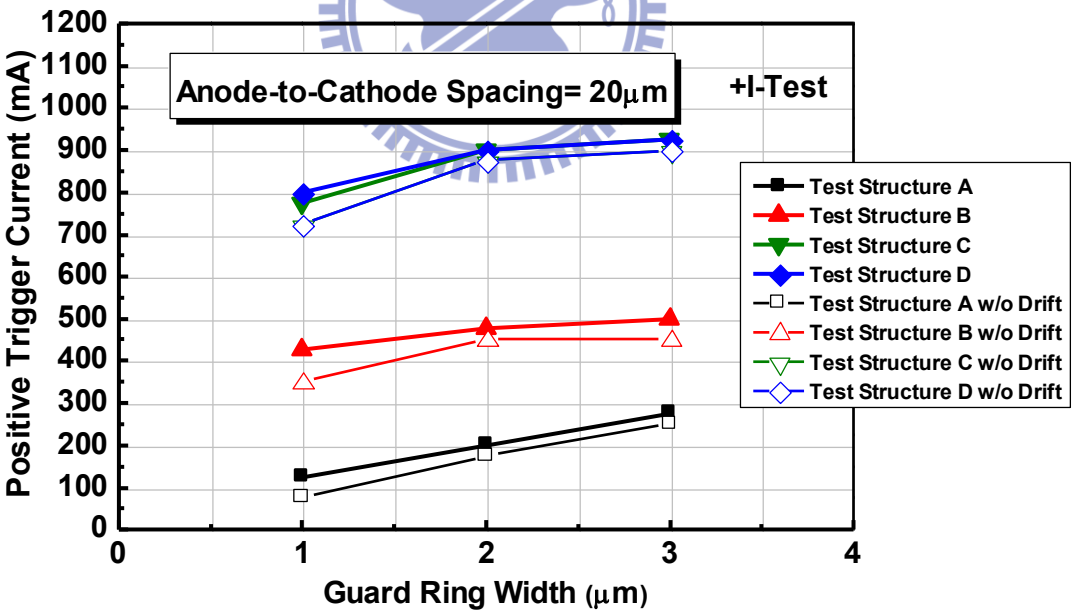


Fig. 4.12. Relations between the positive latchup trigger current on output pad and the guard ring widths of 1, 2, and 3 μm for different test structures A, B, C, and D under the same anode-to-cathode spacing of 20 μm.

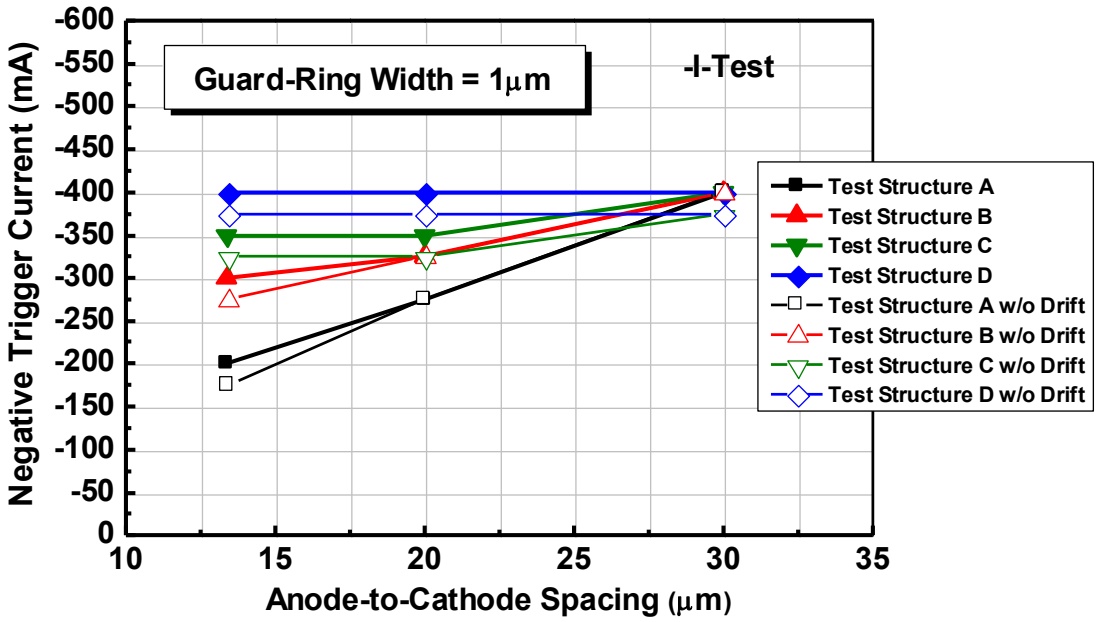


Fig. 4.13. Relations between the negative latchup trigger current on output pad and the anode-to-cathode spacings of 13.4, 20, and 30 μm for different test structures A, B, C, and D under the same guard ring width of 1 μm.

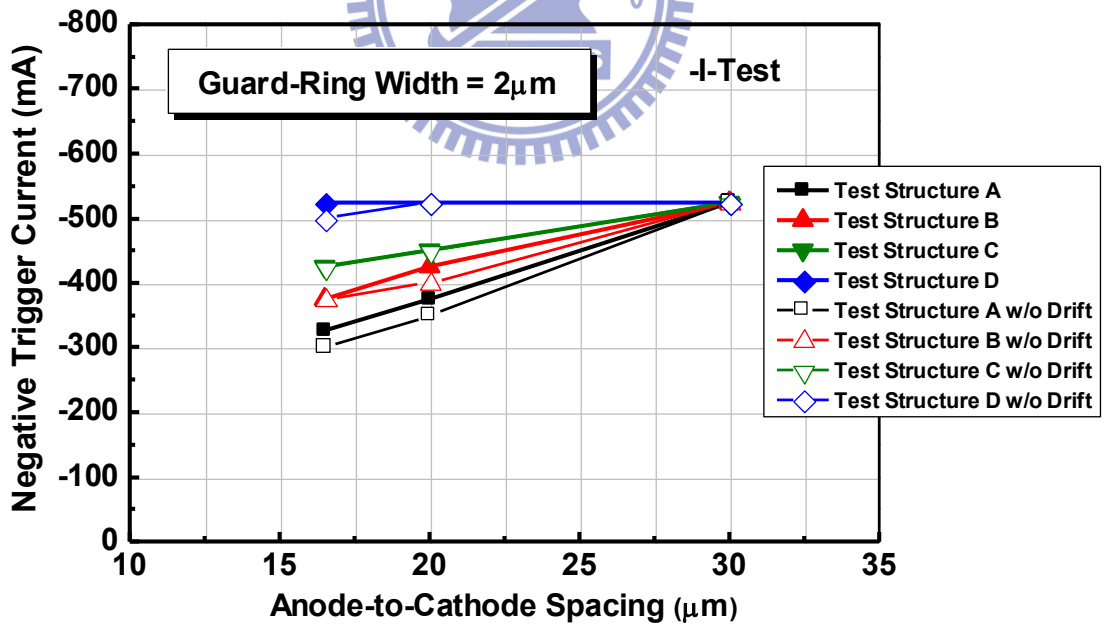


Fig. 4.14. Relations between the negative latchup trigger current on output pad and the anode-to-cathode spacings of 16.5, 20, and 30 μm for different test structures A, B, C, and D under the same guard ring width of 2 μm.

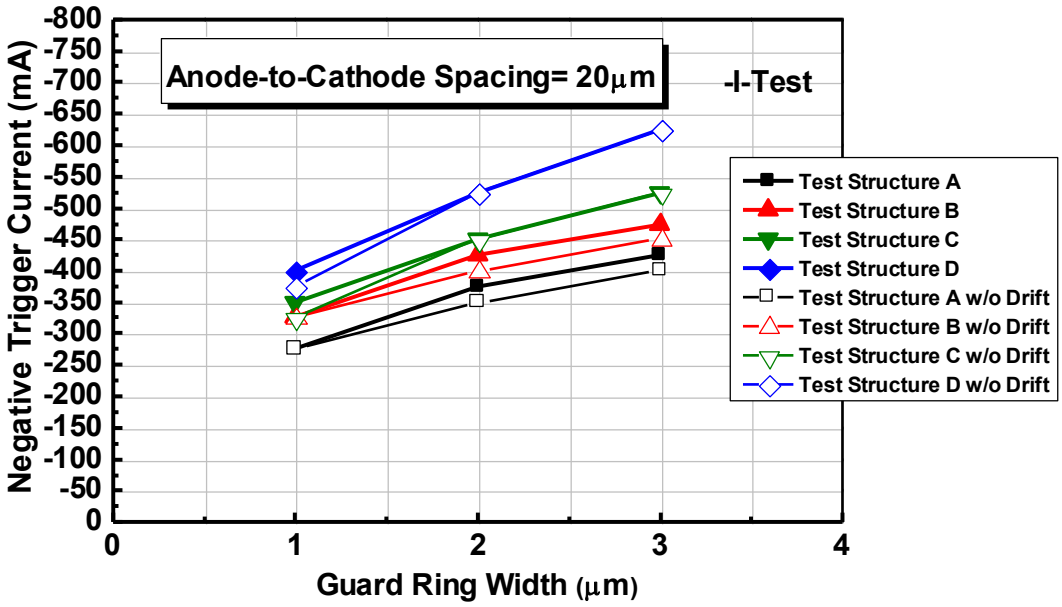


Fig. 4.15. Relations between the negative latchup trigger current on output pad and the guard ring widths of 1, 2, and 3 μm for different test structures A, B, C, and D under the same anode-to-cathode spacing of 20 μm.

Similarly, the latchup immunity under negative latchup trigger current test can be also observed. Figs. 4.13 and 4.14 show the measured relations between the negative latchup trigger current and the different test structures under the different guard ring widths of 1 and 2 μm, respectively. Fig. 4.15 shows the measured relations of different test structures between the negative latchup trigger current and the different guard ring widths under the same anode-to-cathode spacing of 20 μm. The latchup trigger current of all test structures can be increased by an increased guard ring width and the added drift layers, as the measured results in the positive trigger current test. For test structures A, B, and C, the negative latchup trigger current can be greatly increased by the extension of the anode-to-cathode spacing. Nevertheless, for the test structure D, although it has the highest current level, increasing the anode-to-cathode spacing has no improvement on latchup immunity under negative latchup trigger test. It was suspected that the latchup path in test structure D from the VDD-connected source of p-DDDMOS to the

VSS-connected source of n-DDDMOS was not fired. This phenomenon can be further investigated by the failure analysis.

Compared with test structure C, the test structure D has much higher negative latchup trigger current (over -600mA, as shown in Fig. 4.15). The guard ring efficiency in p-DDDMOS can be improved greatly by using NBL. Adding NBL under the p-type device can greatly improve the latchup robustness in the negative latchup trigger current test.

In addition, the immune trigger current level can be simply predicted by extracting the trend line from the test results. For Example, Fig. 4.16 shows the extracted equation from the relation between the positive trigger current (+I) and the guard ring width (GW) in the typical test structure B. The extracted equation has a slope of 37 (mA/μm) with intercept of 390 mA. Fig. 4.17 shows the extracted equation from the relation between the negative trigger current (–I) and the guard ring width (GW) in the typical test structure B. The extracted equation has a slope of -75 (mA/μm) with intercept of -260 mA. These values can be used to predict the immune trigger current level improved by the guard ring width.

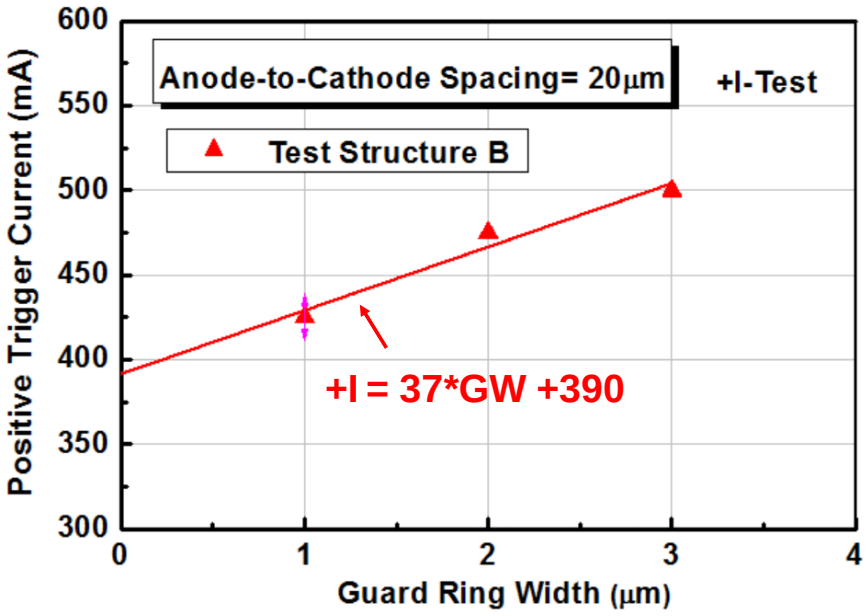


Fig. 4.16. Extracted equation from the relation between the positive latchup trigger current (+I) and the guard ring width (GW) in the test structure B.

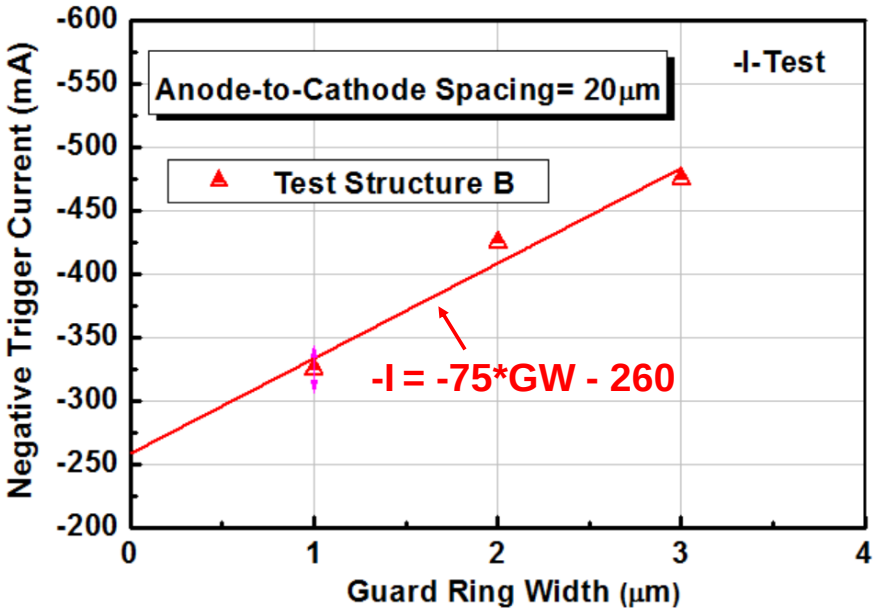


Fig. 4.17. Extracted equation from the relation between the negative latchup trigger current (-I) and the guard ring width (GW) in the test structure B.

4.3.3 Failure Analysis

Figs. 4.18, 4.19, and 4.20 show the SEM photographs of the test structures A, B, and D, respectively, with the latchup-induced damage after the injection of negative latchup trigger current under the same guard ring width of 2 μm and anode-to-cathode spacing of 20 μm. It is obviously found that the test structure D got damaged in the both regions of p-DDDMOS and n-DDDMOS with the burn-out traces between these two devices, as the results shown in the test structures A and B. Accordingly, the failure analysis verified that the latchup path indeed occurred in the test structure D to induce damage.

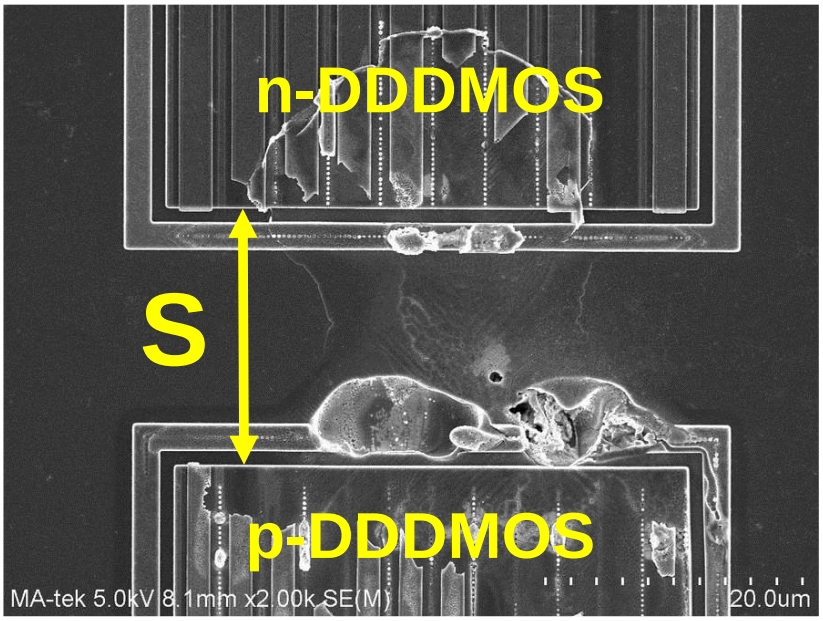


Fig. 4.18. SEM image of test structure A to show the latchup-induced damage after the injection of negative latchup trigger current, under the same layout parameters.

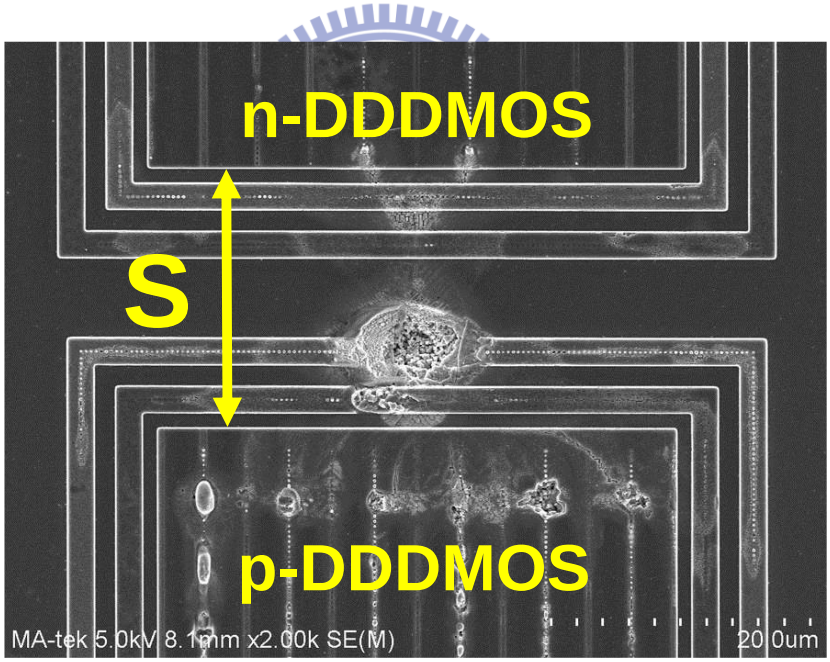


Fig. 4.19. SEM image of test structure B to show the latchup-induced damage after the injection of negative latchup trigger current, under the same layout parameters.

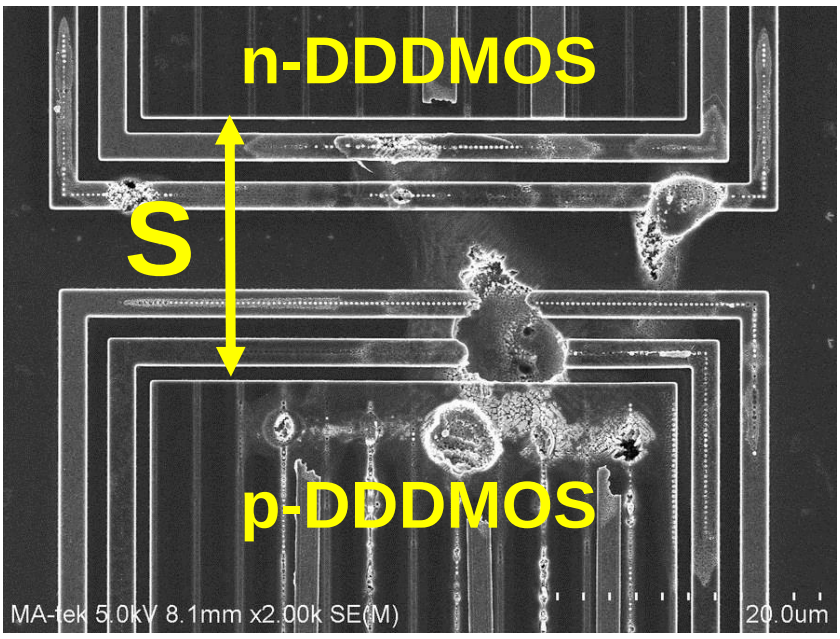


Fig. 4.20. SEM image of test structure D to show the latchup-induced damage after the injection of negative latchup trigger current, under the same layout parameters.

4.4 Summary

The characteristics of HV latchup have been investigated in a HV DDDMOS process. Four test structures are used to evaluate the latchup immunity of HV device structures. Among the test structures, the test structure D can exhibit the highest latchup immunity against the negative and positive latchup trigger current because of the highest guard ring efficiency. Using the NBL-based isolation structure is able to achieve good latchup immunity and save the layout area of HV output buffers without extending the distance between the p-type and n-type MOS devices. Furthermore, the drift layers can be also applied to optimize the guard ring structure for better latchup prevention in HV CMOS ICs.

Chapter 5

Investigation on Unexpected Latchup Path between HV-LDMOS and LV-CMOS in a High-Voltage BCD Technology

5.1 Background

Recently, smart power technology that can integrate both LV and HV devices in a single silicon chip provides a cost-effective solution for high voltage and high current capabilities while increasing performance and reliability. With the integration of both HV and LV devices in the same chip, the voltage levels of HV domain are often significantly above the voltage levels of LV domain. There have been some related studies on the latchup failures between different power domains [38], [39]. As a result, solutions are strongly needed to avoid latchup risk at the HV and LV interface in CMOS IC products.

In this work, the characteristic of a potential latchup path between HV LDMOS and LV CMOS transistors is investigated in a 0.25-μm 5-V/60-V BCD technology. In order to verify the holding voltage (V_{hlod}) of the latchup path, the DC curve tracer (Tek370B) is also used. A parasitic SCR path is found in the experiment silicon chip that fabricated by this HV BCD technology. The current-trigger latchup test is further used to investigate the characteristics of the parasitic paths between these HV and LV devices.

5.2 Proposed Test Structures

The test structure studied in this work is implemented in this 0.25-μm 5-V/60-V BCD technology. The device structures of 60-V pLDMOS and 5-V pMOS transistors are shown in Fig. 5.1. A potential latchup path is expected from the VDDH-connected source of pLDMOS,

through HV n-body, HV p-well, HV n-well, and p-substrate, to the VDDL-connected n-well pickup of LV-pMOS. The simplified circuit scheme of the test structure is illustrated in Fig. 5.2. For studying the influence of layout structure on latchup, the channels of both devices are kept in off state by connecting each device's gate to its own source. The distance (S) of the expected latchup path is 30 μm in the silicon chip. Both devices are drawn with channel width of 50 μm. $V_{Trigger}$ pin will be used in the current-trigger latchup test. Fig. 5.3 shows the layout top view of test structure with HV and LV devices, where the distance (S) and device sizes (W_H and W_L) are designated. The $V_{Trigger}$ node in Fig. 5.1 will be used in the current-trigger latchup test.

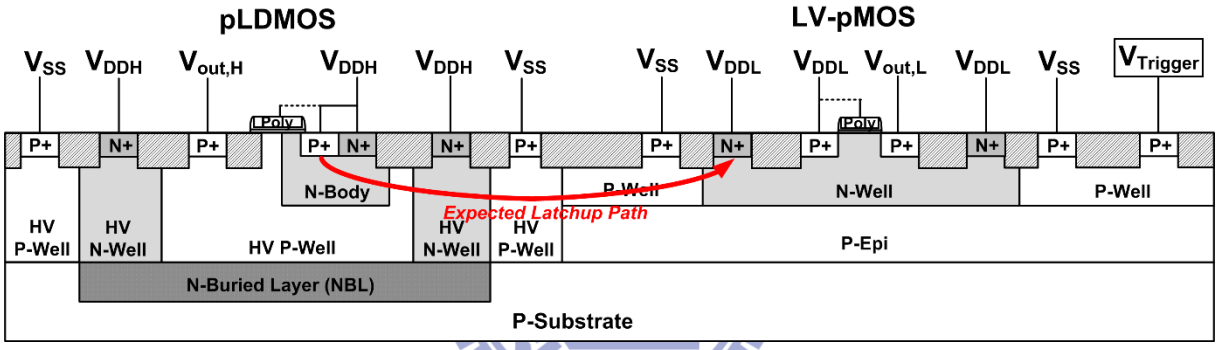


Fig. 5.1. Device structures of 60-V pLDMOS and 5V LV-pMOS in the HV BCD technology. The expected potential latchup path is designated.

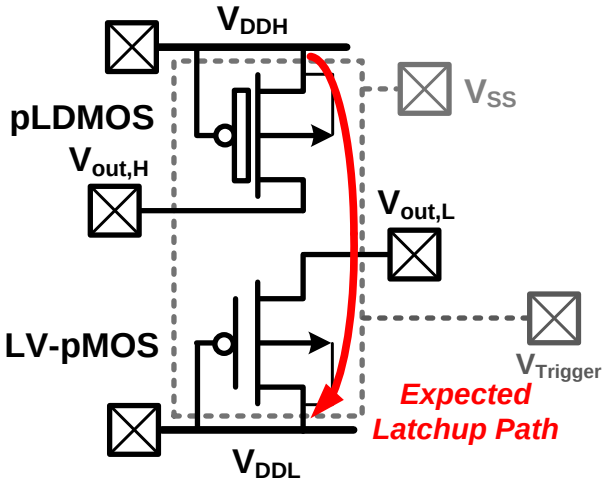


Fig. 5.2. Circuit scheme to show the possible latchup path in the test structure with 60-V pLDMOS and 5-V LV-pMOS.

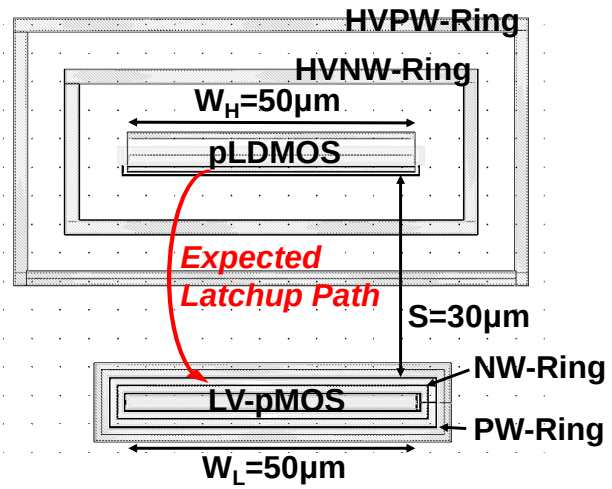


Fig. 5.3. Layout top view of the test structure with 60-V pLDMOS and 5V LV-pMOS.

5.3 Experimental Results

5.3.1 DC I–V Characteristics

To investigate the latchup characteristics of the test structure, the latchup DC I–V curves are measured by Tek370B curve tracer under room temperature of 25 °C. Fig. 5.4 shows the DC I–V characteristics traced between pLDMOS and LV-pMOS under different parasitic paths. Curve 1 is traced from V_{DDH} to V_{DDL} with V_{SS} grounded. The trigger voltage (V_{t1}) is up to 80V, but no snapback phenomenon is found. To further study the characteristic of this path, curve 2 is traced from V_{DDH} to V_{DDL} while V_{SS} is floating. As shown in Fig. 5.4, a snapback curve can be detected with a V_{hold} of ~60 V. On the other hand, a parasitic path, which is from the $V_{OUT,H}$ of pLDMOS, through HV n-well and p-substrate, to the V_{DDL}-connected n-well pickup of LV-pMOS, is also measured. Curve 3 is traced from $V_{OUT,H}$ to V_{DDL} with V_{SS} grounded. The V_{t1} of this path is also up to 80V with no snapback phenomenon. However, when V_{SS} is floating, different from the result of curve 3, the curve 4 shows a strong snapback behavior with V_{hold} of only ~1 V.

In the test results of curves 1 and 2, the path from V_{DDH} to V_{DDL} is formed with a six-layer p-n-p-n-p-n path due to the multiple well structures in pLDMOS. Thus, it will lead this path to

have a high V_{hold}. In the test results of curves 3 and 4, the path from $V_{OUT,H}$ to V_{DDL} is formed with a traditional four-layer p-n-p-n SCR path, so a strong snapback curve is distinctly found. In addition, the test results with V_{SS} grounded are different from the ones without V_{SS} grounded. The reason is that V_{SS} node can collect flowing holes in p-substrate and hence restrict the conduction of npn BJT in the parasitic SCR path.

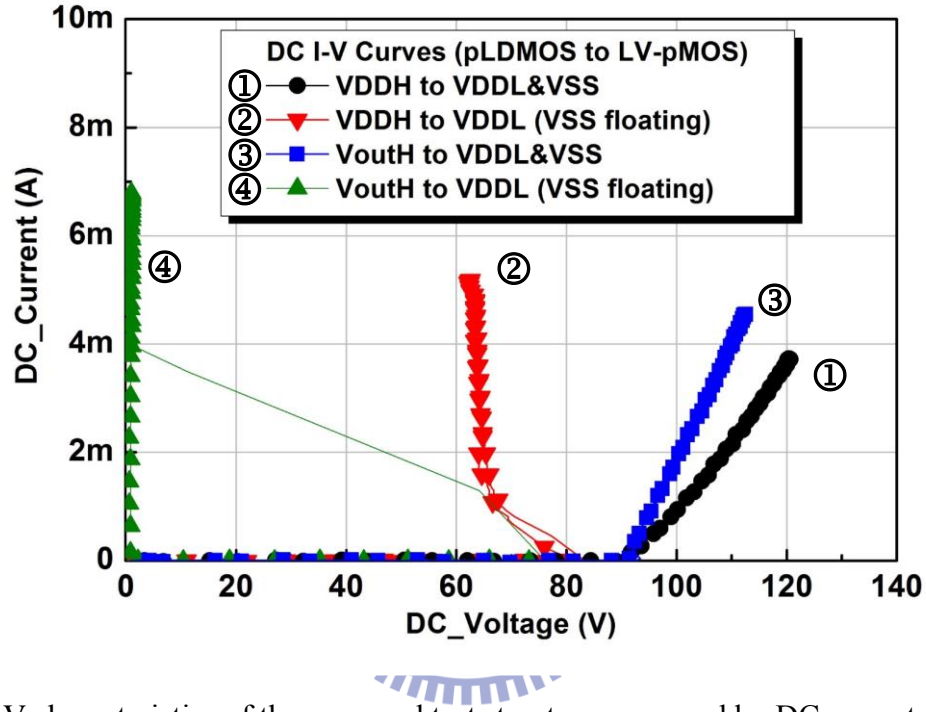
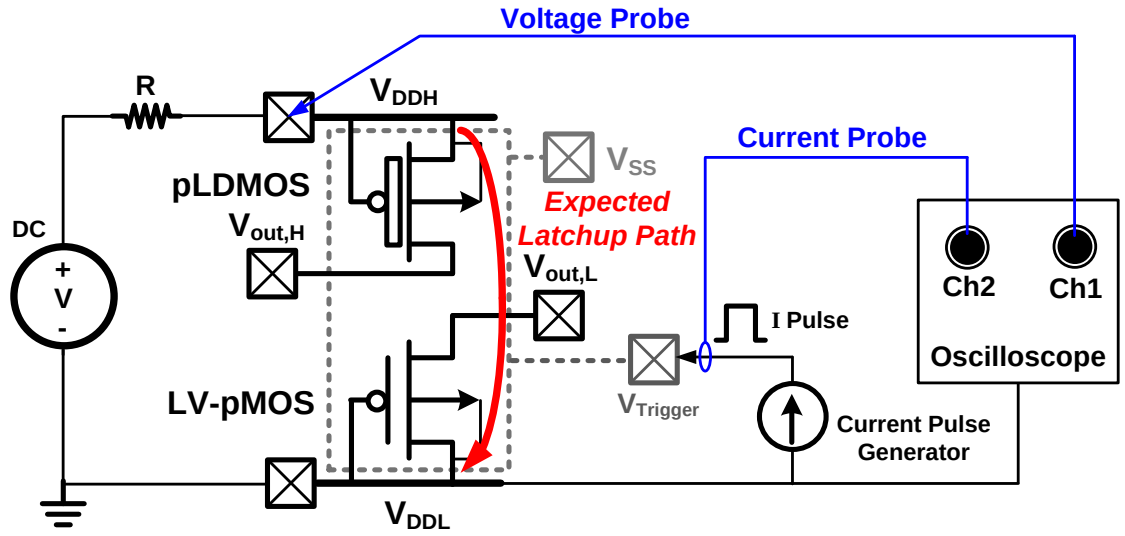


Fig. 5.4. I–V characteristics of the proposed test structure measured by DC curve tracer.

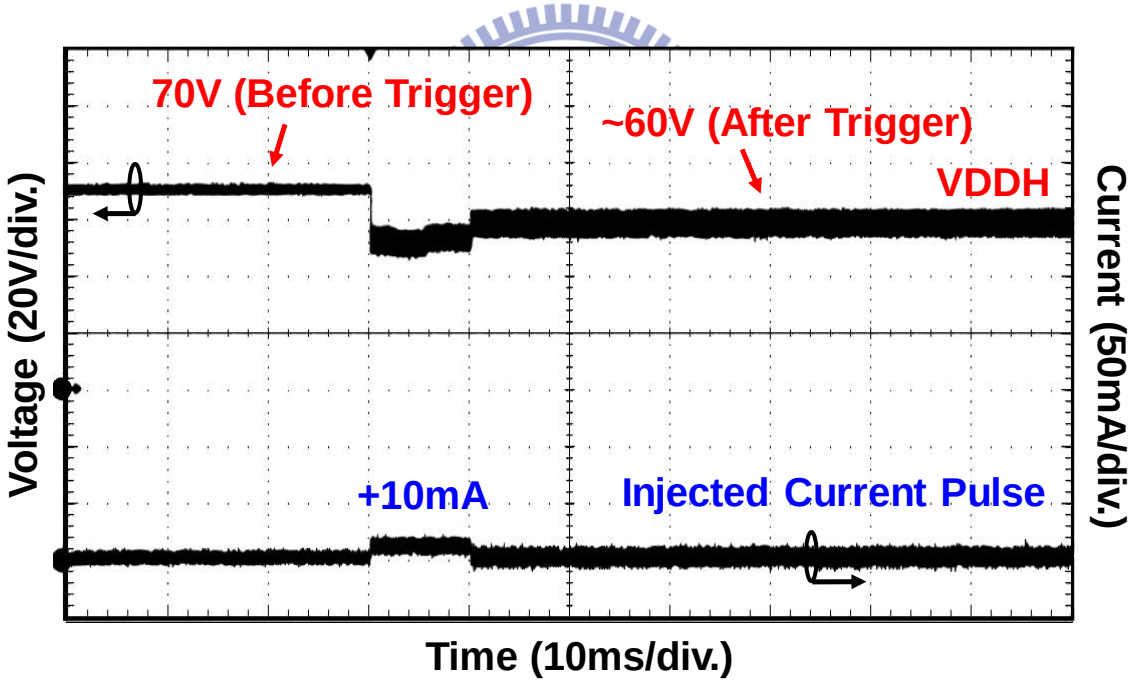
5.3.2 Latchup Trigger Current Test

To verify the latchup immunity, current-trigger latchup test specified in the JEDEC standard (JESD78E) is used. The measurement setup of JEDEC latchup test applied to the test structure is shown in Fig. 5.5(a), with a 60-V DC supply at V_{DDH} pin, V_{DDL} pin grounded, a current pulse generator applied to the $V_{Trigger}$ pin, and an oscilloscope to monitor the waveforms of the V_{DDH} pin voltage and the injected current pulse. The trigger current pulse with a pulse width of 10 ms injected into $V_{Trigger}$ pin is to simulate a transient noise penetrating into the p-substrate within HV and LV devices to induce latchup. If the test structure is triggered into latchup, a decrease on the voltage waveform of V_{DDH} pin can be found to judge the occurrence

of latchup.

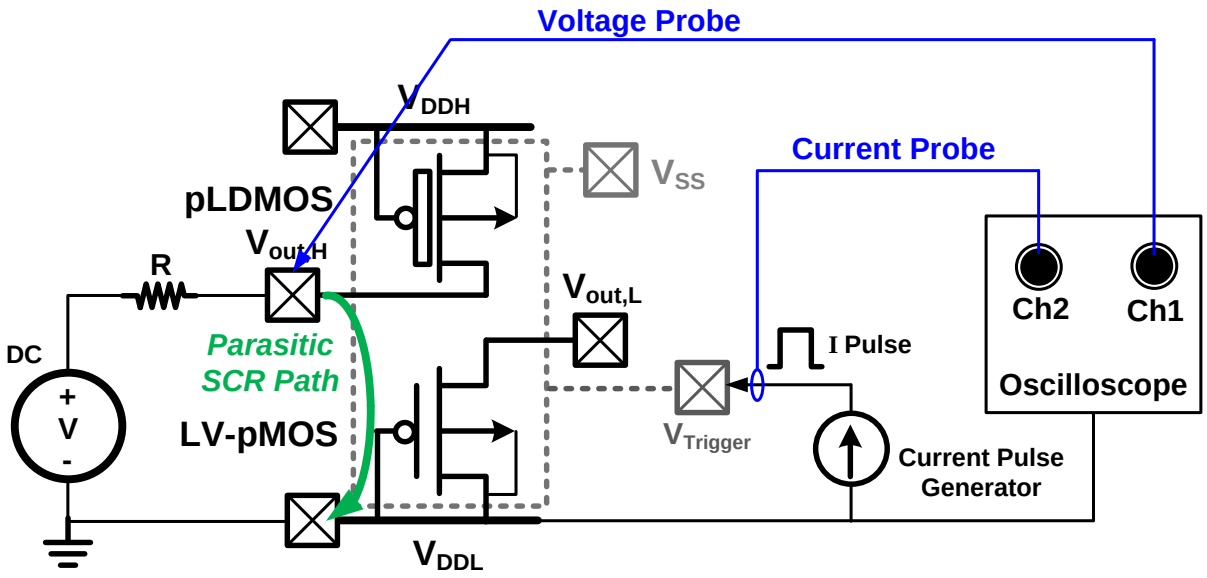


(a)

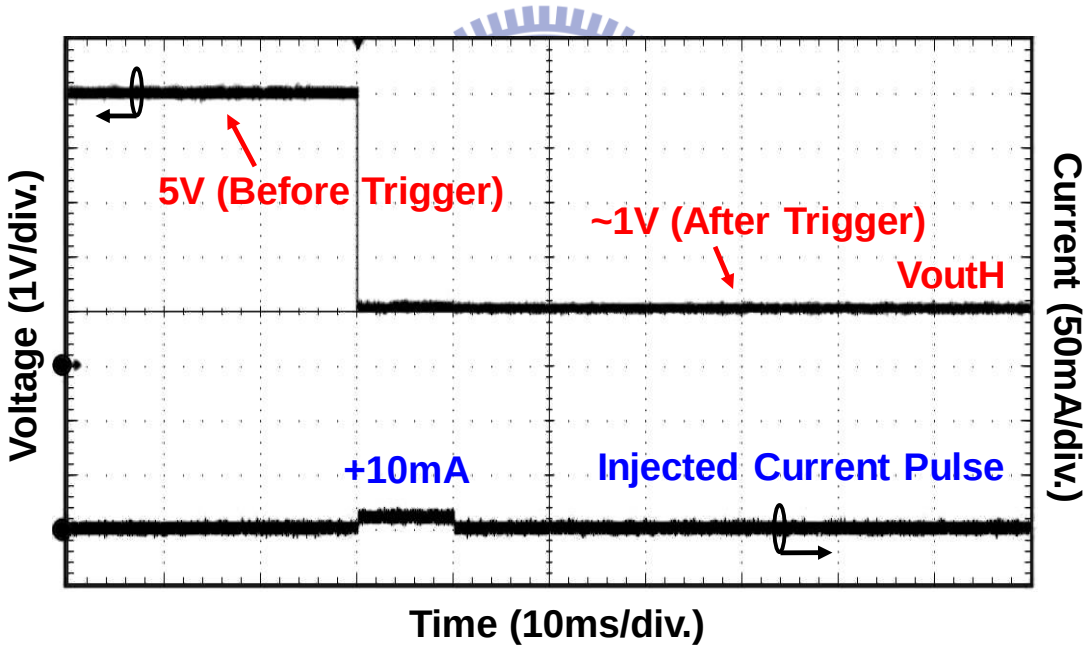


(b)

Fig. 5.5. (a) Latchup measurement on the expected latchup path of the test structure with the positive 10-mA current pulse applied to the $V_{Trigger}$ pad, and (b) measured time-domain voltage and current waveforms on the test structure.



(a)



(b)

Fig. 5.6. (a) Transient triggering measurement on the parasitic SCR path of the test structure with the positive 10-mA current pulse applied to the $V_{Trigger}$ pad, and (b) the measured time-domain voltage and current waveforms on the test structure.

After the transient triggering, no clamped voltage roll-off and no latchup state can be detected even with V_{SS} floating. It is due to the high V_{hold} measured by DC curve tracer in the expected latchup path. To verify the V_{hold} of this path, the latchup trigger measurement is tested again with the DC supply voltage raised to 70V. Fig. 5.5(b) shows the measured time-domain waveforms after the transient triggering of 10-mA current pulse injection. This path clamped the supply voltage to ~60V, which is the same value of V_{hold} under DC curve tracer measurement. A higher V_{hold} means a better latchup immunity. It implies that the latchup issue at HV and LV interface can barely happen if HV device features such complex well structures.

Furthermore, the parasitic SCR path from the $V_{OUT,H}$ pin of the 60-V pLDMOS to the V_{DDL} pin of 5-V LV-pMOS is also measured by the current-trigger latchup test, which is used to verify the measured DC V_{hold} of this parasitic SCR path. The measurement setup is shown in Fig. 5.6(a), with a 5-V DC supply at $V_{OUT,H}$ pin, V_{DDL} pin grounded, V_{SS} pin floating, and a current pulse injection into $V_{Trigger}$ pin. From the measured voltage waveform in Fig. 5.6(b), this path clamped the supply voltage to ~1 V, which is the same value of V_{hold} under DC curve tracer measurement. Such low V_{hold} of this parasitic SCR path may influence the ESD performance of an IC product. It will be further discussed and investigated in the next section.

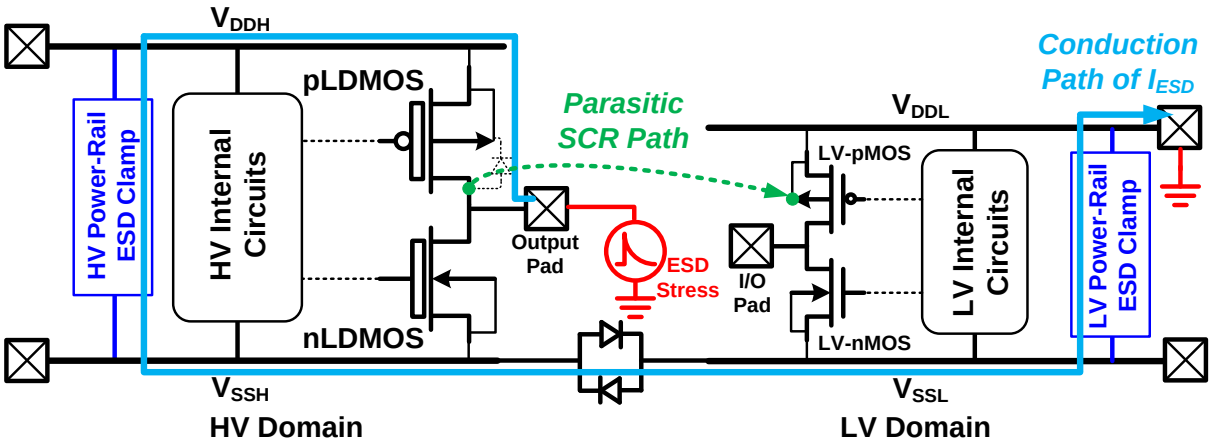


Fig. 5.7. ESD protection design with HV and LV power-rail ESD clamp circuits in a CMOS IC with different power domains.

5.3.3 Impact to ESD Protection

This parasitic SCR path may cause the unexpected ESD current discharging path across the HV/LV interface of the ICs to degrade the ESD robustness of IC products. The typical on-chip ESD protection design with HV and LV power rail ESD clamp circuits in a CMOS IC with different power domains is depicted in Fig. 5.7. If an ESD stress zapping from the output pin of HV domain to the V_{DDL} pin of LV domain, the conduction path of ESD current (I_{ESD}) is generally designed to discharge through the body diode of pLDMOS to the floating V_{DDH} line, then through the HV power-rail ESD clamp circuit to the floating V_{SS} lines, and then through the parasitic diode inherent in the LV power-rail ESD clamp circuit to the grounded V_{DDL} line. (as the blue line indicated in Fig. 5.7) The sum of the different voltage drops along this conduction path can be approximately expressed as

$$V_{IESD} \approx V_{Diode,pLDMOS} + V_{HV\_Clamp} + V_{Diode,VSS} + V_{LV\_Clamp} \ , \qquad (5.1)$$

where $V_{Diode,\ pLDMOS}$ and $V_{Diode,\ VSS}$ are the voltage drops of the body diode of pLDMOS and the bi-directional diodes between V_{SSH} and V_{SSL} ground lines, and V_{HV_Clamp} and V_{LV_Clamp} are the conduction voltage drops of HV and LV power-rail ESD clamp circuits.

However, if the layout spacing between HV and LV p-type devices is too close, the V_{hold} of the parasitic SCR path (shown by the green dashed line in Fig. 5.7) can be lower than the voltage drop of the conduction path in Equation (5.1), and hence it will divert the ESD current when triggered on. An unexpected failure may happen to degrade the ESD robustness, if the device dimension of this parasitic SCR between the HV and LV p-type devices was not large enough to sustain the desired ESD level.

5.3.4 Discussion

There are two recommended ways to prevent the unexpected failure between different power domains. The first way is to simply extend the layout spacing between HV and LV

devices to increase the V_{hold} of the parasitic path, and even insert double guard rings within the parasitic path for reducing the current gains of the parasitic BJTs, as depicted in Fig. 5.8.

On the contrary, the second way is to utilize the parasitic path to improve the ESD robustness. The device dimensions of the adjacent HV and LV p-type devices can be appropriately enlarged to ensure the ESD robustness of this parasitic path. The TLP system is used to investigate the characteristic of the parasitic SCR path in this test structure.

The TLP-measured I-V curve of this parasitic SCR path is shown in Fig. 5.9. The TLP-measured V_{hold} is ~30 V, which is much higher than that in the DC-measured result. Such voltage difference is due to the increased current gain induced by the joule heating effect in the DC measurement. In addition, the TLP-measured failure current (I_{t2}) of this parasitic SCR path is ~4.4 A. With the channel width of 50 μm for both 60-V pLDMOS and 5-V pMOS devices fabricated in this test structure, the I_{t2} per width is calculated as ~0.088 (A/μm). It can be applied to predict the ESD robustness of this parasitic SCR path.

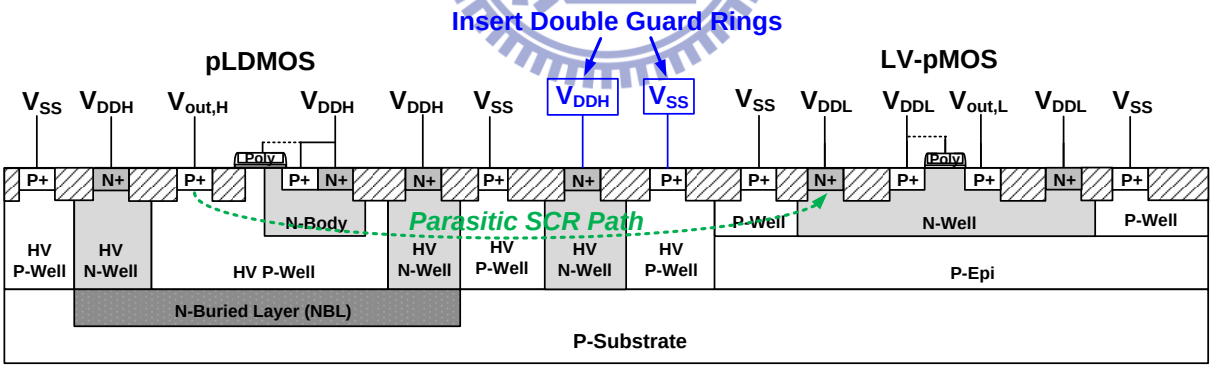


Fig. 5.8. Parasitic SCR path between HV and LV p-type devices in a HV BCD technology with inserted double guard rings.

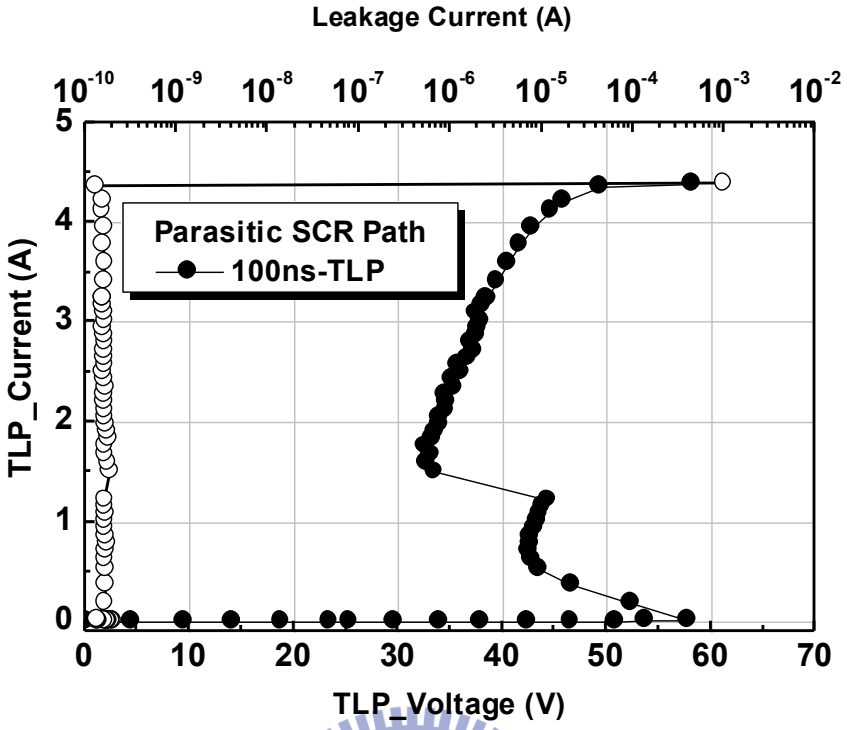


Fig. 5.9. TLP-measured I-V curve of the parasitic SCR path between 60-V pLDMOS and 5-V pMOS devices. (Channel widths for both 60-V pLDMOS and 5-V pMOS devices are 50 μm.)

5.4 Summary

The characteristics of the parasitic paths between HV and LV devices in the test structure have been investigated in a HV BCD technology. It is found that the V_{hold} of the expected latchup path measured by curve tracer is greater than 60 V. Through the experimental verification by using current-trigger latchup test, this expected latchup path is hardly induced. However, an unexpected parasitic SCR path has been found in the silicon chip. Transient triggering measurement has further verified that the parasitic SCR path can be easily triggered. It would cause negative impact to the ESD robustness of IC products due to the ESD current diverting through the unexpected discharging path. Accordingly, layout rules between HV pLDMOS and LV-pMOS devices should be carefully defined to prevent the occurrence of unexpected parasitic path in such a 0.25-μm 5-V/60-V BCD technology.

Chapter 6

Conclusion and Future Works

This chapter summarizes the main contributions of this dissertation. In addition, some suggestions and future works are discusses from the research results.

6.1 Main Results of this Dissertation

Chapter 1 has given a brief introduction of ESD protection, as well as latchup issue, in the HV BCD technologies. In Chapter 2, to prevent latchup issue when applying traditional SCR device in HV CMOS ICs for ESD protection, a new high-holding-voltage HVSCR device using six-layer p-n-p-n-p-n structure with addition of parasitic path is proposed and verified in a 0.25-μm HV BCD process. Through the TLP, DC, and TLU measurements, the experimental results show that this proposed layout structure could highly increase the holding voltage of traditional SCR device even in the long-term measurement. However, the ESD robustness of proposed HVSCR device is dramatically reduced when a high holding voltage is achieved because of high power dissipation. It can be further studied with some optimized layout structures in the future work.

In Chapter 3, an on-chip ESD protection solution for the HV applications has been proposed in a 0.25-μm HV BCD process by using LV devices with stacked configuration. From the experimental results, stacked LV devices which has good ESD robustness without latchup issue is more area-efficient in comparison with the modified HVSCR device proposed in Chapter 2. Following the comparison of ESD robustness between various stacked LV devices and the modified HVSCR, the stacked LV-PFOD is proposed as HV ESD protection element for the 60-V pins of a battery-monitoring IC in a 0.25-μm HV BCD process. Experimental

results in silicon chip have verified that the proposed design can successfully protect the HV pins of battery-monitoring IC against over 8-kV HBM ESD stress. Moreover, stacked LV devices with sharing path technique can be an appropriate ESD protection solution to fit the different ESD protection windows simultaneously in a CMOS IC with multiple power domains. This design concept can be further studied and verified in the future work.

In Chapter 4, the optimization of guard ring structures to improve latchup immunity in an 18 V DDDMOS process with the DDDMOS transistors were together investigated in a silicon test chip. The measurement results demonstrated that the test devices isolated with the specific guard ring structure of n-buried layer can highly improve the latchup immunity. Moreover, the addition of n-buried layer and drift layers can further enhance the immune level in the latchup-trigger current test. The recommended guard ring structures can be applied to the HV circuits in this 18 V DDDMOS process to meet the new required specification in JESD78E standard.

Chapter 5 investigates a latchup path which may potentially exist at the interface between separated power domains in a HV BCD technology. Owing to the multiple well structures used to realize the HV device in the BCD process, the expected latchup path in the test structure was hardly triggered. However, a parasitic SCR path featuring a very low holding voltage was found in the experiment silicon chip. Such a parasitic path is first reported in the literatures. It may influence the ESD robustness of CMOS IC products with different power domains integrated together. Thus, the layout rules at HV and LV interface should be carefully defined to avoid the occurrence of unexpected parasitic path.

6.2 Future Works

With the multiple supply voltages and noisy operating environment in the various HV applications, latchup has been a challenging reliability issue for decades. Developing HV and LV devices with high latchup immunity has been an important target in HV CMOS ICs with

multiple power domains. From the measurement results in Chapter 5, latchup was not fired on between HV and LV domains owing to the complicated HV device structure using multiple layers in this HV BCD process. However, latchup or latchup-like issue may still possibly happen between different power domains when a process with simplified HV device structures is used. For example, the holding voltage from the drain side of HV pLDMOS to LV-PMOS is much smaller than that from its source side because of its "asymmetric" structure in this study. That is to say, for the circuit design with the "symmetric" structure of HV device, such a latchup issue could happen. As a result, the latchup issue between multiple power domains can be further investigated in the HV process using "simplified" or "symmetric" HV device structure, as the possible latchup path illustrated in Figs. 6.1 and 6.2.

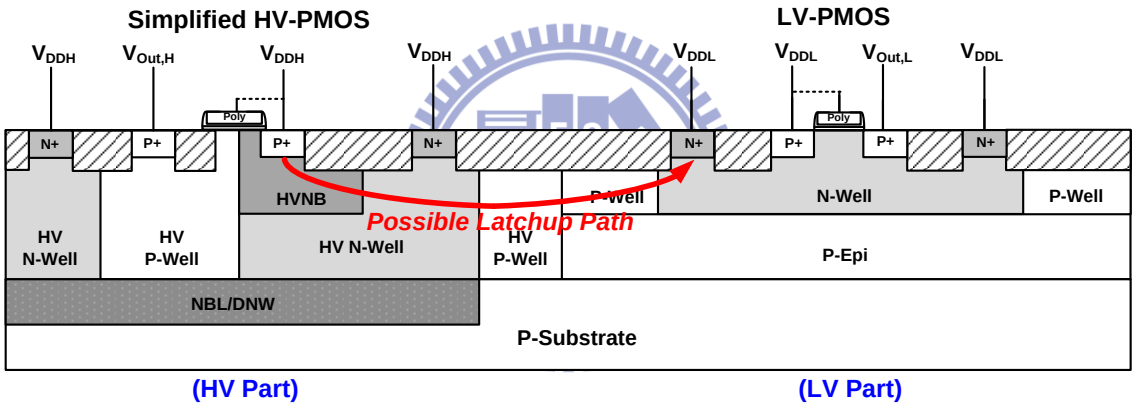


Fig. 6.1. Device structures of a "simplified" HV-PMOS and a LV-pMOS in the HV BCD technology, where the possible latchup path exists from V_{DDH} to V_{DDL}.

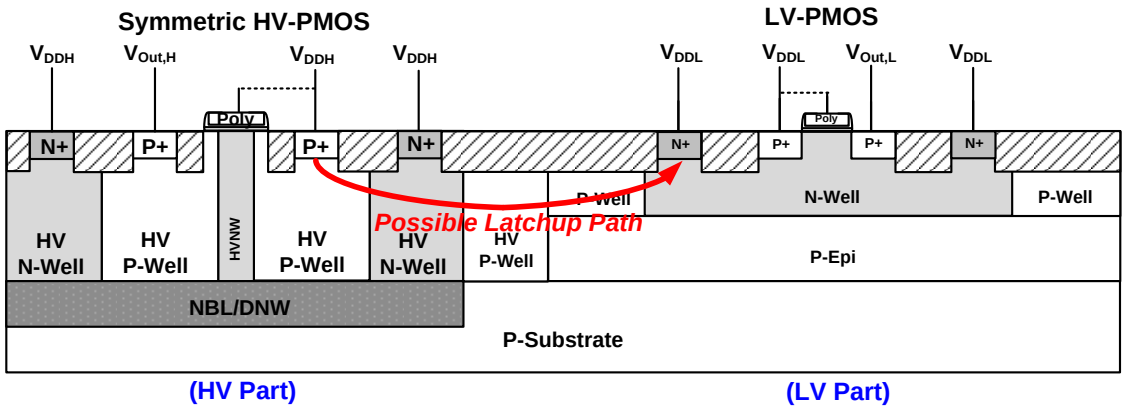


Fig. 6.2. Device structures of a "symmetric" HV-PMOS and a LV-pMOS in the HV BCD technology, where the possible latchup path exists from V_{DDH} to V_{DDL}.

In addition, the layout structure, such as deep n-well (DNW) or n-buried layer (NBL), which is used to isolate low-voltage devices can cause some unexpected latchup issues, as illustrated in Fig. 6.3. For example, in the applications of display drivers or biomedical circuits using the DNW-isolated NMOS with negatively biased source and body, the latchup issue could happen from the GND-connected p-type isolation ring (V_{ISO}) to the negatively biased source (V_{SSL}) of NMOS. (e.g., V_{SSL}= -10 V)

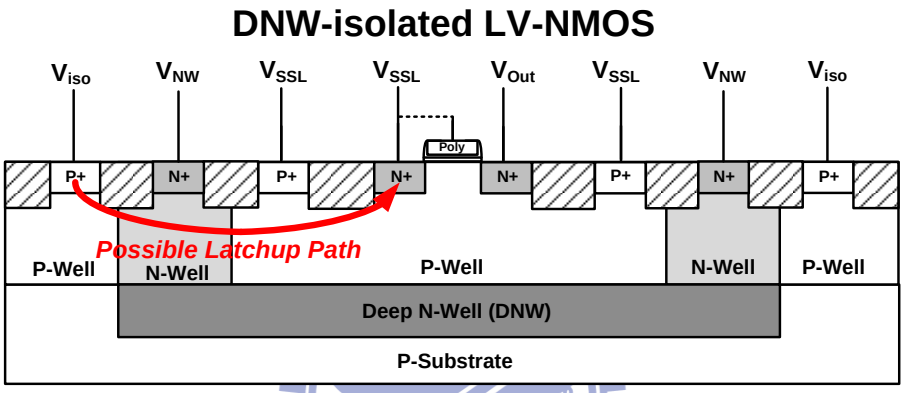


Fig. 6.3. Device structure of a DNW-isolated LV-NMOS in a CMOS technology, where the possible latchup path exists from V_{ISO} to V_{SSL}.

Furthermore, the advanced CMOS technology makes the CMOS ICs more susceptible to latchup issue. As the progress of semiconductor technology that scales down the transistor dimensions towards sub-20nm technology node, the classical planar MOS field-effect transistors (MOSFETs) are replaced by the fin-shaped field-effect transistors (FinFETs) to enable the continued technology scaling. With low power requirements in mobile applications, the supply voltages of the core circuits are reduced as CMOS technologies scale [40]–[43]. Owing to the lower supply voltages below 1 V, there is no latchup issue in the core circuits anymore. However, higher supply voltages (e.g., 1.8 V or 3.3 V) are still required in I/O interface circuits and some analog/power management/RF circuits in sub-20nm CMOS technologies. There have been some related studies of latchup issue in the bulk FinFET

technologies [44], [45]. Based on these studies, the small fin structure can be harmful to latchup immunity due to the increased parasitic resistance and the reduced guard ring efficiency. A narrower fin pitch with a shallower STI (shallow trench isolation) depth can impact the latchup immunity level. Thus, the latchup threats are never eliminated and the sensitivity towards latchup is increased in the bulk FinFET technologies.

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ESD Protection Design and Latchup Prevention in High-Voltage BCD Technology

Publication List

(A) Referred Journal Papers:

1. **Chia-Tsen Dai** and M.-D. Ker, "ESD protection design with stacked high-holding-voltage SCR for high-voltage pins in a battery-monitoring IC," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 1996–2002, May 2016.
2. **Chia-Tsen Dai** and M.-D. Ker, "Optimization of guard ring structures to improve latchup immunity in an 18-V DDDMOS process," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2449–2454, Jun. 2016.
3. **Chia-Tsen Dai** and M.-D. Ker, "Investigation of unexpected latchup path between HV-LDMOS and LV-CMOS in a 0.25-μm 60-V/5-V BCD technology," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3519–3523, Aug. 2017.
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(B) International Conference Papers:

1. **Chia-Tsen Dai** and M.-D. Ker, "Study on ESD protection design with stacked low-voltage devices for high-voltage applications," in *Proc. IEEE International Reliability Physics Symposium*, 2014, pp. EL.5.1–EL.5.2.
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