國立交通大學

電子工程學系　電子研究所碩士班

碩　士　論　文

抑制癲癇發作之

電荷平衡電流刺激器設計

Design of Charge-Balanced Biphasic Stimulus Driver to Suppress Epileptic Seizure in the Low Voltage Process

研 究 生：曾建豪　　(Chien-Hao Tseng)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國一〇三年九月

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碩士論文

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中華民國一〇三年九月

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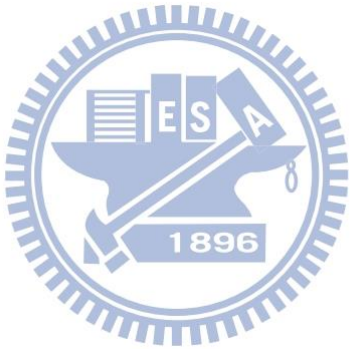
摘要

近年，電刺激技術已常用於醫療方面，例如功能性電刺激 (Functional electrical stimulation) 與治療性電刺激 (Therapeutic electrical stimulation)。透過電流刺激患者的異常神經部位，可使患者恢復部分身體的機能。而隨著積體電路製程的發展，整合智慧型仿生系統於單晶片的目標已變得可行，結合微電子技術、醫學以及生物化學，可以製造應用於不同疾病醫療之生物晶片，例如癲癇晶片。

抑制癲癇的方式為輸出定電流刺激，而人體規格的抑制電流大小需要高達 1-3 mA，從生醫電子安全的考量，需要減少雙向電流的電荷誤差，以避免電荷累積在電極上而造成神經細胞的傷害。此外，電極以及人體組織阻抗會隨著電極擺放位

置以及深度而有所不同，考慮到負載適應性，輸出級需要用到近 10V 高電壓。

為了與智慧型仿生系統中的其他電路做單晶片整合，刺激器電路必須使用低壓製程來實作。此外，系統晶片只提供 1.8V 之供應電壓，所以晶片內部需要藉由 DC-DC 轉換器產生刺激器所需的高工作電壓 VCC。本研究所提出之刺激器電路使用電壓限制技巧，使其能以低壓製程元件來承受高壓，而電晶體不會面臨電性過壓的情形。藉由三位元的控制訊號可輸出 0.5, 1, 1.5, 2, 2.5, 3mA 的輸出電流。整體電路在 TSMC 0.18μm 1.8V/3.3V 低電壓製程下實現。



Design of Charge-Balanced Biphasic Stimulus Driver to Suppress Epileptic Seizure in the Low Voltage Process

Student: Chien-Hao Tseng **Advisor: Prof. Ming-Dou Ker**

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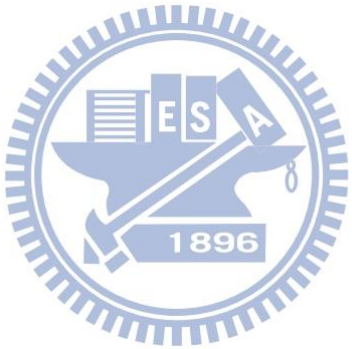
Abstract

Nowadays, the treatment of using electrical stimulation has been investigated and verified, such as functional electrical stimulation (FES) and therapeutic electrical stimulation (TES). By stimulating abnormal nerve sites of the patients, they may restore some body functions. As the CMOS process developed, using an implantable device to provide stimulus current can be accomplished. The biomedical chip is made by the combination of microelectronics, medicine and biochemical such as epilepsy prosthetic SoC.

The methodology to suppress epilepsy seizure is constant current stimulation, and the effective scale of stimulus current for human body is up to 1-3mA. For safety considerations, the stimulus driver should be designed to deliver charge-balanced biphasic current pulses and reduce the mismatch between the anodic and cathodic pulses to avoid charge accumulation and damaging the never cells. In addition, the electrode-tissue impedance varies with the position and depth of the electrodes in human body. Consider the loading adaptation, high voltage supply 10V is required in the output stage.

To be integrated with other circuits into SoC, this work is implemented in low-voltage process. However, the power supply of the SoC is only 1.8V. DC-DC boost converter is required to raise the voltage potential for the stimulus driver. By using voltage limiting technique, the proposed stimulus driver, which consists of low voltage devices, is able to sustain high voltage (10V) without gate-oxide overstress. 3-bit amplitude signals are used to control the scale of stimulus current from 0.5mA to 3mA, with 0.5mA a step. The overall circuit has been fabricated by the TSMC 0.18μm 1.8V/3.3V CMOS process.

Contents



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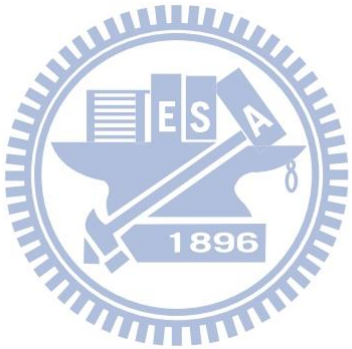

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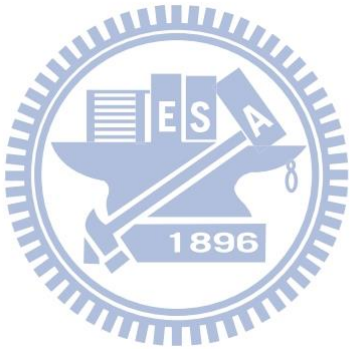


Chapter 1
Introduction

1.1 Motivation

As biomedical science and electronics engineering developed, the combination of them, which is so called bioelectronics, becomes more and more popular. Nowadays, bioelectronics is an important technology in enhancing the quality of life, especially for those who are suffering from physiological difficulties. There are several fabulous applications of bioelectronics such as magnetic resonance imaging (MRI) and electroencephalography (EEG) that cause a revolution in medical science. In recent decades, it has been demonstrated that functional electrical stimulation (FES) and therapeutic electrical stimulation (TES) that transmit artificial electrical signals into nervous system can restore some physical functions of a human [1]. Novel biomimetic microelectronic systems with these techniques will enable treatment of some of presently incurable human handicaps such as hearing loss, blindness (retinal prosthesis), paralysis (neuron-muscular prosthesis), and memory loss (cortical prosthesis) [2]. Epilepsy is also one of diseases investigated to be treated by therapeutic electrical stimulation.

Epilepsy, caused by abnormal discharge activity in brain, is one of the most common neurological disorders and seriously restrains patient's daily life. As medical science progressed, therapies of epileptic seizure include pharmacologic treatment and surgical treatment, pharmacologic treatment are applied in the first place. For patients who do not respond to the medicament, non-reversible brain surgery is in common used. This is risky surgery that might cause functional losses. However, 25% of the

world's 50 million people with epilepsy have seizures that cannot be controlled by medication or epilepsy surgery. The need for new therapeutic options is clear [3]. Nowadays, epilepsy becomes predictable by analyzing EEG in time or frequency domains [4]. Several ways to predict epileptic seizure have been researched such as predictable features and prediction by classification. It has also been demonstrated that the abnormal discharge signal that causes epileptic seizure can be suppressed by FES before epilepsy happens [5]. Compared with the non-reversible surgical treatment, the advantages of electrical stimulation treatment are flexible, recoverable, and non-destructive. Although FES is a feasible method to suppress epileptic seizure, there are several challenges in designing the stimulus driver. Due to different kinds of tissue, locations, and electrode material, the equivalent impedance of electrode and tissue will vary. Moreover, the effective stimulus current to suppress epilepsy seizures is up to 3mA. To provide fixed magnitude of stimulus current, the output voltage varies in a wide range corresponding to the tissue impedance. In addition, high operating voltage may result in problems of gate-oxide overstress, hot-carrier effect, and other reliability issues in the low-voltage process [6]. Furthermore, for an implantable device, safety issue is the most important consideration. In this thesis, the proposed stimulus driver is designed consider with both reliability and safety issue. The stimulus driver with high-voltage-tolerant structure and the technique of charge balance are investigated in this work.

1.2 Thesis Organization

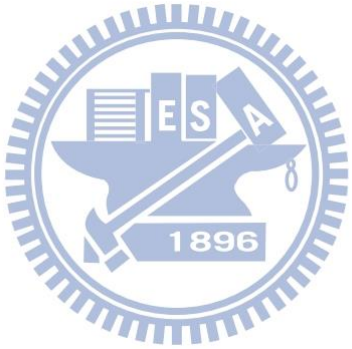
The first chapter, chapter 1, includes the motivation of this work and the thesis organization.

Chapter 2 of this thesis introduces some background knowledge of epilepsy,

epileptic seizures treatment, and implantable stimulus driver.

In chapter 3, design of charge-balanced biphasic stimulus driver to suppress epileptic seizure is proposed. The proposed stimulus driver has been fabricated in the 0.18-μm 1.8-V/3.3-V general purpose process for SoC integration.

The last chapter, chapter 4, recapitulates the major consideration of this thesis and concludes with suggestions for future investigation.



Chapter 2

Background of Epilepsy, Stimulus Driver and Epilepsy SoC Development

2.1 Overview of Epilepsy and Epileptic Treatment

Epilepsy, caused by excessive abnormal discharge in the brain, is a neurological disorder [7]. Brain controls not only almost all the actions of a human but also sensations, emotions, memories, and so on. Signals between brain and different parts of body are delivered through the nervous system which consists of hundreds of thousands of neurons. Action of organism is controlled by motor neurons and sensation of organism is controlled by sensory neurons. These neurons, which are excitable by electrical stimulation, transmit information by transfer of ions such as potassium, chloride, and sodium. As shown in Fig. 2.1(a) [8]. Accumulated ions cause the change of concentration of ions, and by changing concentration of ions, voltage gradient of membrane of neurons generate an action potential which transmits along nervous system and triggers another neuron as shown in Fig. 2.1(b) [9].

Under normal brain activity, brain generates constant and stable electrical signals in certain patterns. Fig. 2.2 shows different waveforms of EEG depending on states of body under normal conditions [10]. These signals transmit along neurons of nervous system in the brain, spinal cord, and ganglia to whole body via neurotransmitters. During epileptic seizure time, abnormal discharges flow through nearby neurons and tissues. Like flowing through a resistor, current flows through nearby tissues will cause voltage drop. If the voltage exceeds the action potential, neurons will be triggered and unexpected signals will be spread out. In this case, normal activities of

brain may be interrupted, and patients' normal physical and emotional functions may be affected. The right side picture of Fig. 2.3 shows the EEG under abnormal brain activities recorded by the electrode array [11].

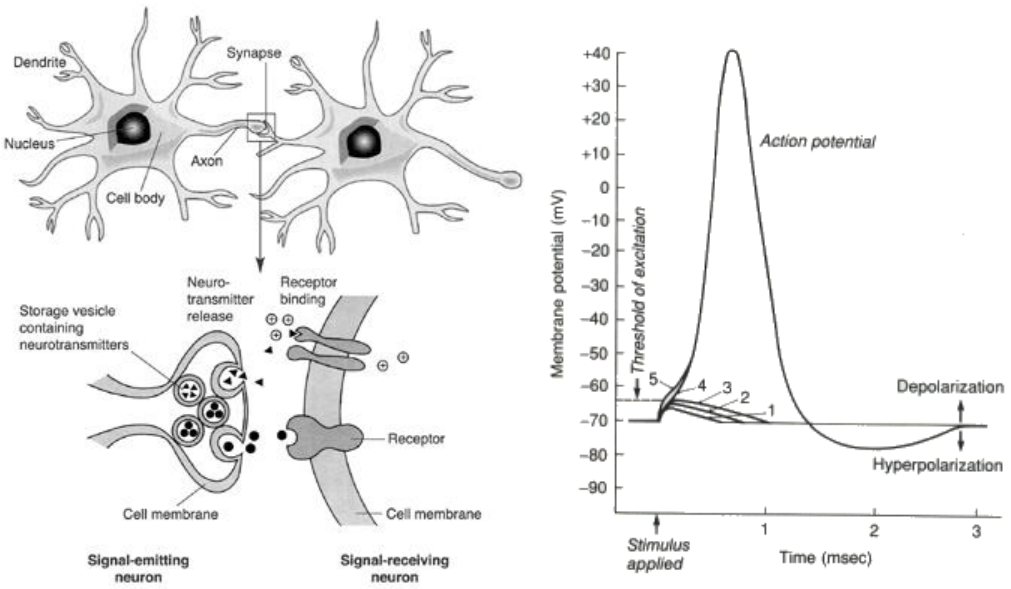


Fig. 2.1 The way neurons transmit signals is that (a) ions are transferred through membrane and accumulate at synapse to generate (b) action potential [8].

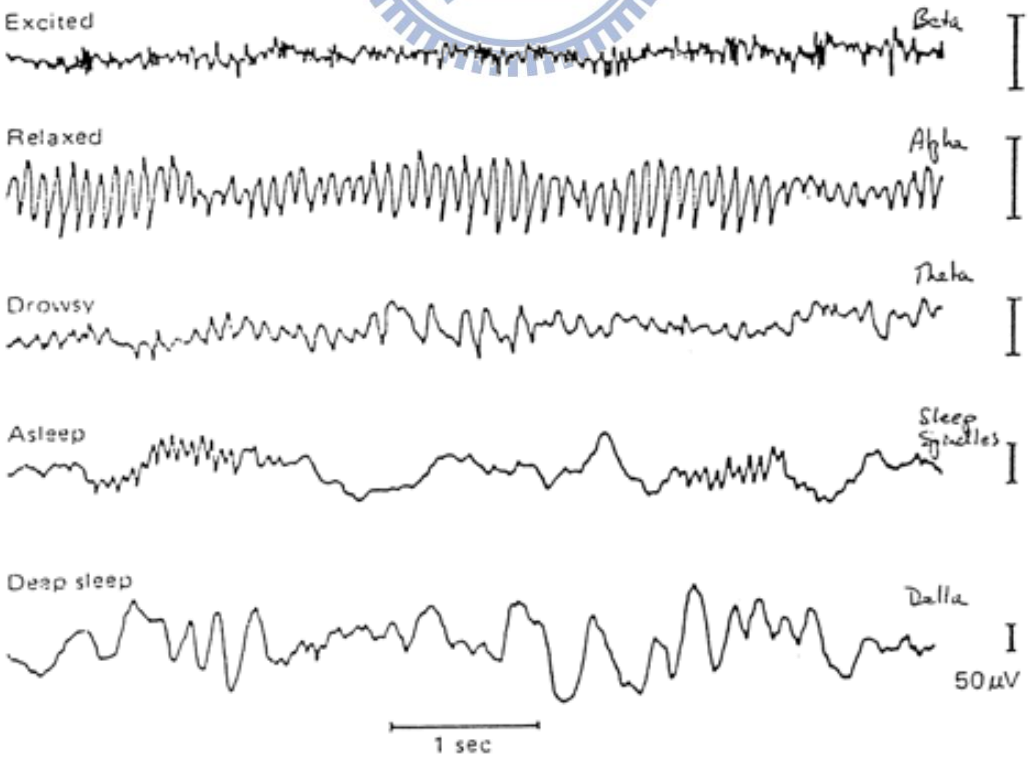


Fig. 2.2. Brain activities under different states [10].

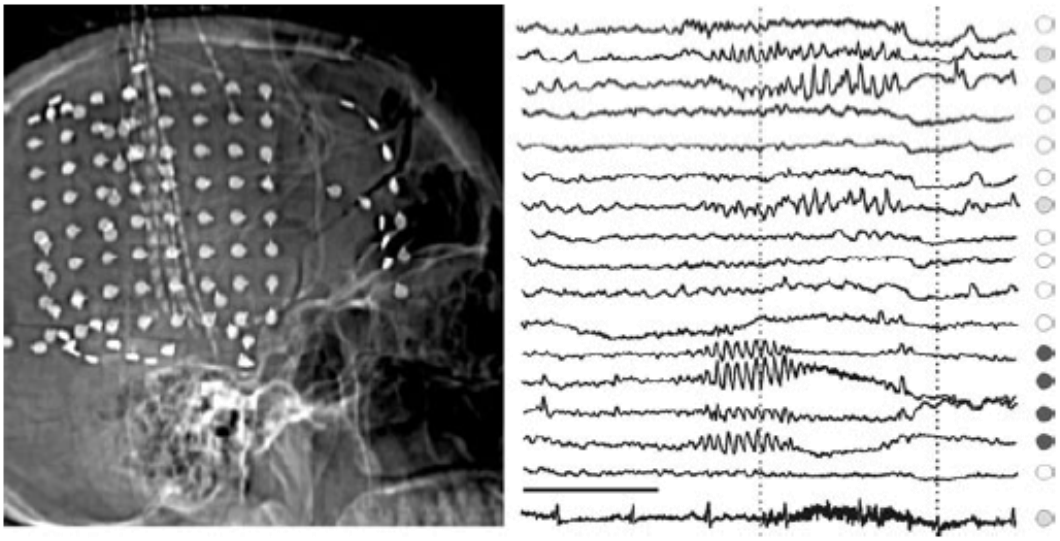


Fig. 2.3. Pictures of an electrode array for recording of the brain activity and the EEG signals of an epileptic patient [11].

Seizure types are most commonly defined and grouped according to the classification proposed by the International League Against Epilepsy (ILAE) in 1981 [12]. Distinguishing between seizure types is important since different types of seizure may have different causes, outcomes and treatments. Seizure types are organized firstly according to whether the source of the seizure within the brain is localized (partial or focal onset seizures) or distributed (generalized seizures) [13]. Partial seizures can be further classified to simple and complex partial seizure. The difference between them is that the patients' consciousness is impaired or not. If it is unimpaired, then it is a simple partial seizure; otherwise it is a complex partial seizure. A partial seizure may spread within the brain, a process known as secondary generalization. Generalized seizures are divided according to the effect on the body but all involve loss of consciousness. There are six main types of generalized seizures: tonic-clonic, tonic, clonic, myoclonic, absence, and atonic seizures. They all involve a loss of consciousness and typically happen without warning. Although most type of epileptic seizures won't last a long time, most of them prolong only one or two minute, epilepsy affects patient's daily life deeply.

Pharmacologic treatment is the most common way used to suppress epileptic seizure. Due to the diversification of epilepsy, there are more than 20 types of medications, and each is developed for specific type of epileptic seizure. According to patients' age, types of epilepsy, syndromes, and intensity of seizure, doctors will choose suitable medications (antiepileptic drugs or AED) for treatment. There are two types of AEDs which can be used: one is narrow spectrum AEDs, and the other is broad spectrum AEDs. While the narrow spectrum AEDs focus on small number of epileptic seizure, the broad spectrum AEDs work for a large group of seizure. However, epilepsy is a complicated disease. There is no standard recipe to decide which medication is the best for an epileptic patient. Besides the effectiveness, side effects are also the mainly consideration for a doctor to write out a prescription. Most of patients' condition of seizure can be ameliorated by AEDs. However, every kind of medicines might sometimes lead to side effects including blurry vision, dizziness, headaches, and fatigue [14]. In addition, these medications might lead to allergic in roughly 10 % of people and can impair blood cell or liver. Unfortunately, there are still many patients who do not respond to AEDs, which is called medically refractory. For these patients, other treatments should be taken into consideration such as surgical treatment.

Except for pharmacologic treatment and surgical treatment, electrical stimulation is a treatment for drug-resistant epilepsy and has been investigated [14]. Advantages of electrotherapy are flexible, recoverable, and non-destructive. There are some feasible methods for stimulation. One is transcranial magnetic stimulation (TMS). As shown in Fig. 2.4(a) [15], TMS is a noninvasive method to cause depolarization or hyperpolarization in the neurons of the brain. Using electromagnetic induction to induce weak electric currents using a rapidly changing magnetic field; this can cause activity in specific or general parts of the brain with little discomfort, allowing for

study of the brain's functioning and interconnections. Another method is deep brain stimulation (DBS), which sends electrical impulses, through implanted electrodes, to specific parts of the brain (brain nucleus) for the treatment of movement and affective disorders. As shown in Fig. 2.4(b).

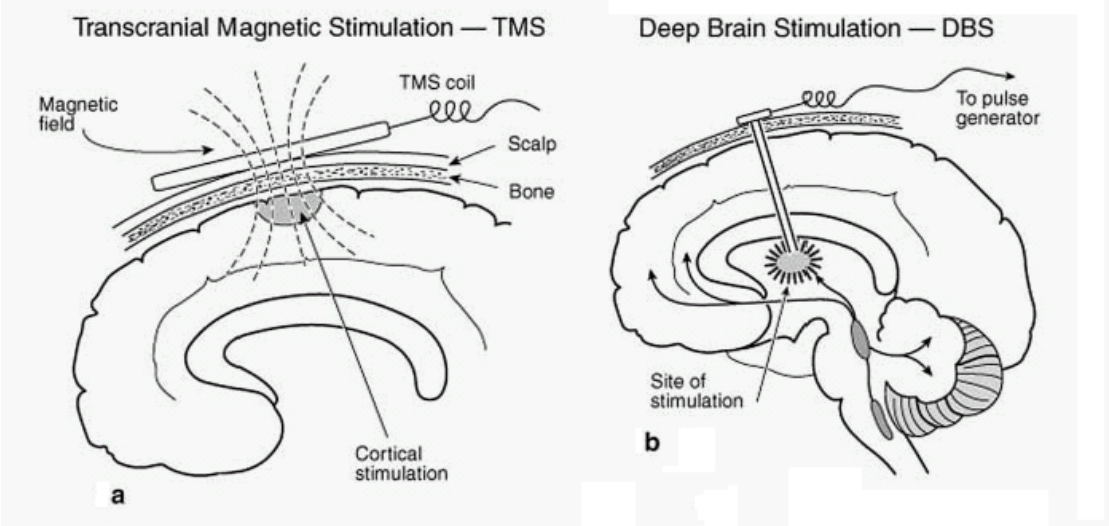


Fig. 2.4. Methods of stimulation (a) Transcranial magnetic stimulation (TMS). (b) Deep brain stimulation (DBS) [15].

2.2 Closed-Loop Neural Prosthetic SoC for Real Time Epiletic Seizure Control

2.2.1 Introduction of Functional Electrical Stimulation(FES)

Functional electrical stimulation (FES) is a technique that provides electrical current to excitable tissue to supple or replace function that is lost in neurologically impaired individuals. In addition to the chronic applications for restoration of function, electrical stimulation has also been used for many therapeutic applications.

The waveform of electrical stimulation pulse is characterized by three parameters: amplitude, pulse width, and pulse frequency. To different position of neurons and different human bodies, each of the parameters may be different. Stimulus waveforms are generally either biphasic or monophasic in shape. A monophasic can induce DC

charge accumulation on the neuron, and the neuron can be injured by chronic DC charge accumulation. Thus, most FES systems adopt biphasic stimulus waveforms, the secondary pulse is used to balance the electrical charge produced by the first pulse, as shown in Fig. 2.5. So the potential damaging electrochemical process can be avoided [16].

Today, implanted functional electrical stimulation (FES) has been successfully used in a large set of applications linked to organic deficiencies and sensory is abilities. More recent attempts have been made to use implanted FES for movements or functions restoration in para- and quadriplegic patients. Some neuroprostheses have already been progressed to commercialization such as restoring hand function, visual, bladder and bowel control, and respiration. The experimental and commercial neuroprostheses such as the lower extremity neuroprosthesis, shown in Fig. 2.6 [17], and epiretinal prosthesis, shown in Fig. 2.7 [18].

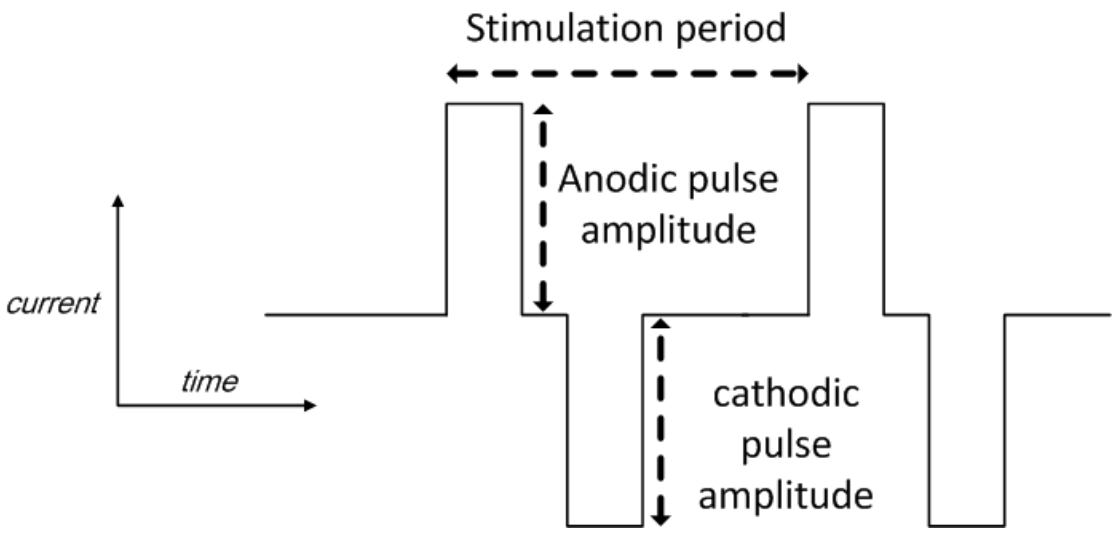


Fig. 2.5. Biphasic stimulation pulse.

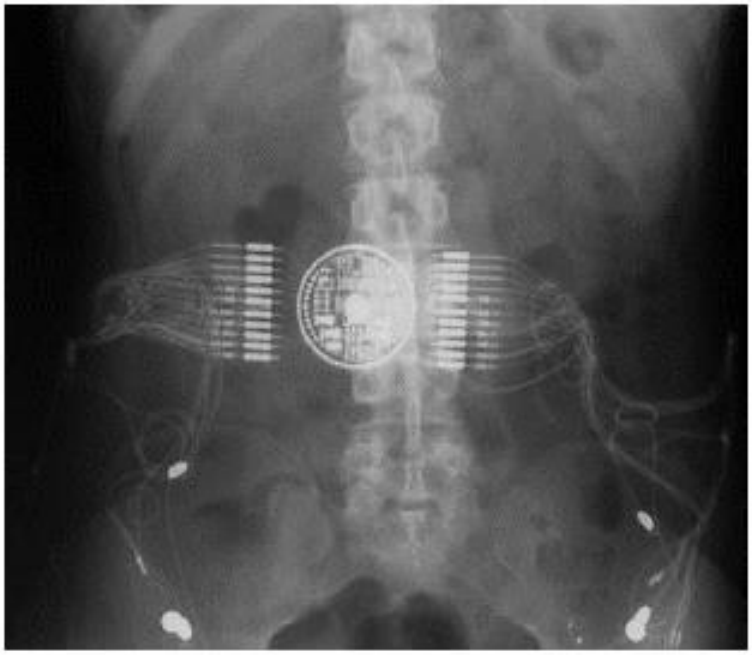


Fig. 2.6. Radiography of the implant to stimulate the lower limbs [17].

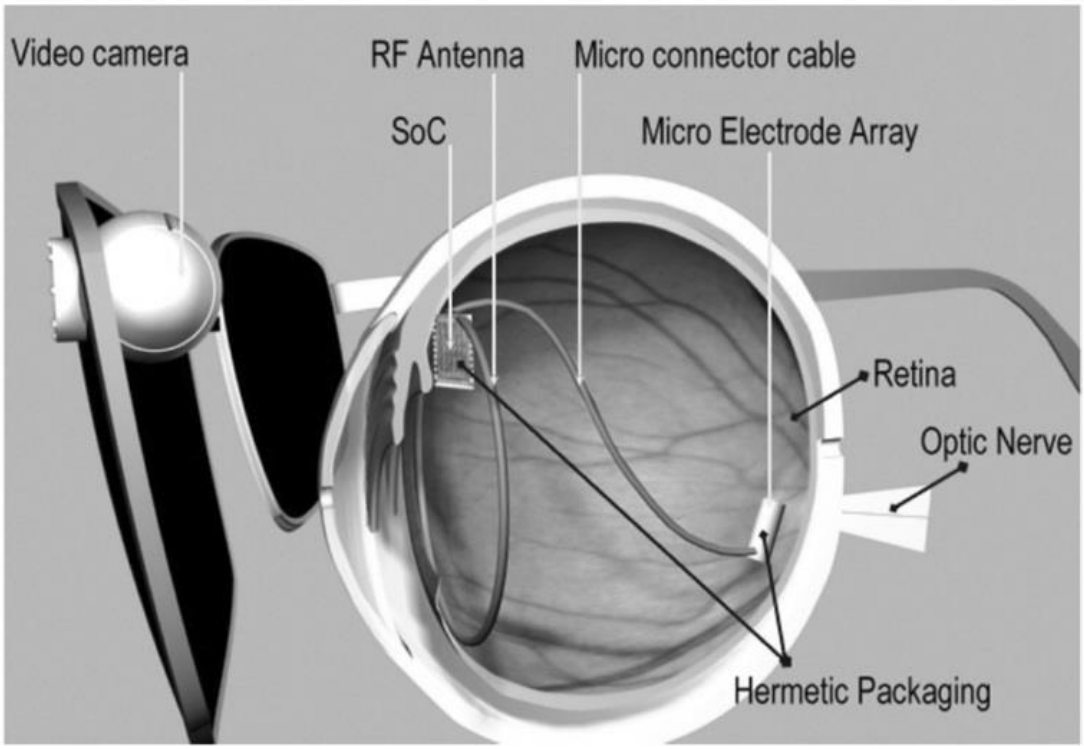


Fig. 2.7. Diagram of the 256-channel epiretinal prosthesis [18].

2.2.2 Epileptic Seizure Detecting and Controlling System

In recent decades, epilepsy becomes predictable by detecting epileptic seizures from EEG in time or frequency domains, and a variety of methods of prediction have been researched. It also has been demonstrated that the abnormal discharge signal that causes epilepsy can be suppressed by FES before epileptic seizures happen. Numerous epileptic seizure detecting and controlling systems has been studied and implemented. The systems for epileptic treatment are mainly classified by stimulus types, open-loop systems and closed-loop systems [19].

Open-loop systems, or so called blind systems, do not respond to physiological activity immediately. The neuroscientists intend to modulate seizures by activating and inactivating region and set the required stimulus current for individual. Open-loop systems regularly turn on and off at a fixed pattern which is determined by neuroscientists before the event. Currently existing systems that approved by FDA are all adopts open-loop systems. Closed-loop systems, so called intelligent systems, are more complicated. The systems are switched on by detecting seizures onset. In comparison with open-loop systems, closed-loop systems can minimize the effect to human body. Closed-loop systems consist of detector, signal analyzer, and stimulus driver. As current researches shown, epileptic seizures could be tracked back to tens of seconds before onset. For example, closed-loop system may be quite effective for epileptic seizure in the hippocampus, where seizures may remain confined for up to 10 seconds prior to propagation [20]. Therefore, a number of algorithms have been proposed for rapidly detecting and classifying the sign of different kind of epileptic seizures. These algorithms analyze the brain activities records from EEG or electrocorticogram (ECOG) and extract the feature of seizure-like brainwave, and the outcome of analysis can be utilized to switch on therapeutic intervention. Due to

complexity of closed-loop systems, power consumption is one of mainly considerations of embedded systems. To sustain a longer battery life of a portable seizure controller, the hardware and software were optimized to achieve lower power consumption. Fig. 2.8 is an example for closed-loop epileptic seizure monitor and controller presented in 2009 [21].

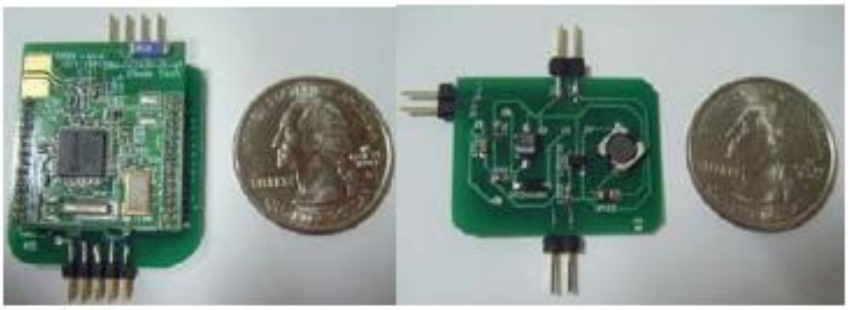


Fig. 2.8. The closed-loop epileptic seizure monitor and controller [22].

2.2.3 Brief Introduction of Implantable Stimulus Driver

As the development of electrotherapy, a variety of implantable stimulus drivers have been researched and presented. Based on the method of stimulation, stimulators are divided into two types: (1) two interface leads per site (bipolar stimulation) and (2) one interface lead per site (monopolar stimulation) shown as Fig. 2.9. For one interface lead per site (monopolar stimulation), we need the positive and negative high voltage sources respectively. For two interface leads per site (bipolar stimulation), the positive high voltage source is required. Moreover, the way of stimulation affects the complexity of the circuit.

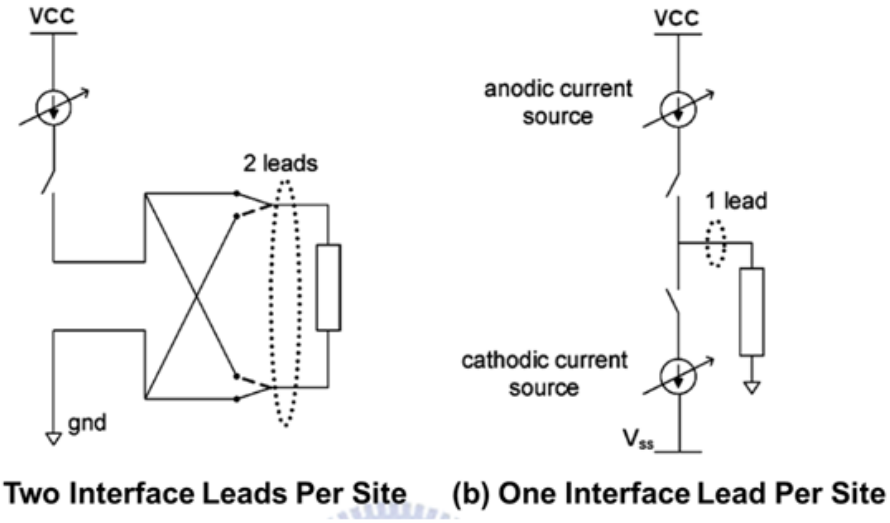


Fig. 2.9. Different stimulation method affects the components in the stimulus driver.

An example of the monopolar stimulation is shown in Fig. 2.10 [23]. This work is used in the epiretinal prosthesis chip. The positive high voltage regulator +12V and negative high voltage regulator -12V provide the electrode voltage. With current mismatch problem, the charge cancellation circuit is added to let the charges on the electrodes release to ground. DAC is used to control the amplitude of the output current. At the output stage, the high voltage (32V) MOSFETs are used to afford 12V voltage so that it could avoid the semiconductor issue such as hot-carriers or punch-through. The output resistance is equal to one resistor R_{elec} series one capacitor C_{elec} with R_{elec}=10kΩ and C_{elec}=100nF. The circuit would realize with additional mask for SoC integration.

Fig. 2.11 indicates the stimulus driver in the bipolar stimulation [25]. This work is also applied in retinal prosthesis. Using 0.35 μm HV CMOS process with 20V power supply, the current mismatch achieves less than 0.4μA smaller than the work in [24]. There are three phases: cathodic phase, anodic phase and shorting phase. In the cathodic phase, S_1 is close to deliver charge to node WE, while anodic to cancel delivered charge. Using shorting alone to achieve charge balance may cause unwanted

neural response to neighboring sites. The output resistance is shown in Fig. 2.11(b) with C_E=100nF, R_F=10MΩ and R_T=9kΩ. Fig. 2.11(c) shows the stimulus circuit. M_{HP2},M_{HP3},M_{HN2} and M_{HN3} are switches which gives the biphasic current into electrode. The current source driver has large output impedance to bias the electrode adaptive operating voltage in R_T=9kΩ. The output stage use an active cascade current source to enlarge the output resistance.

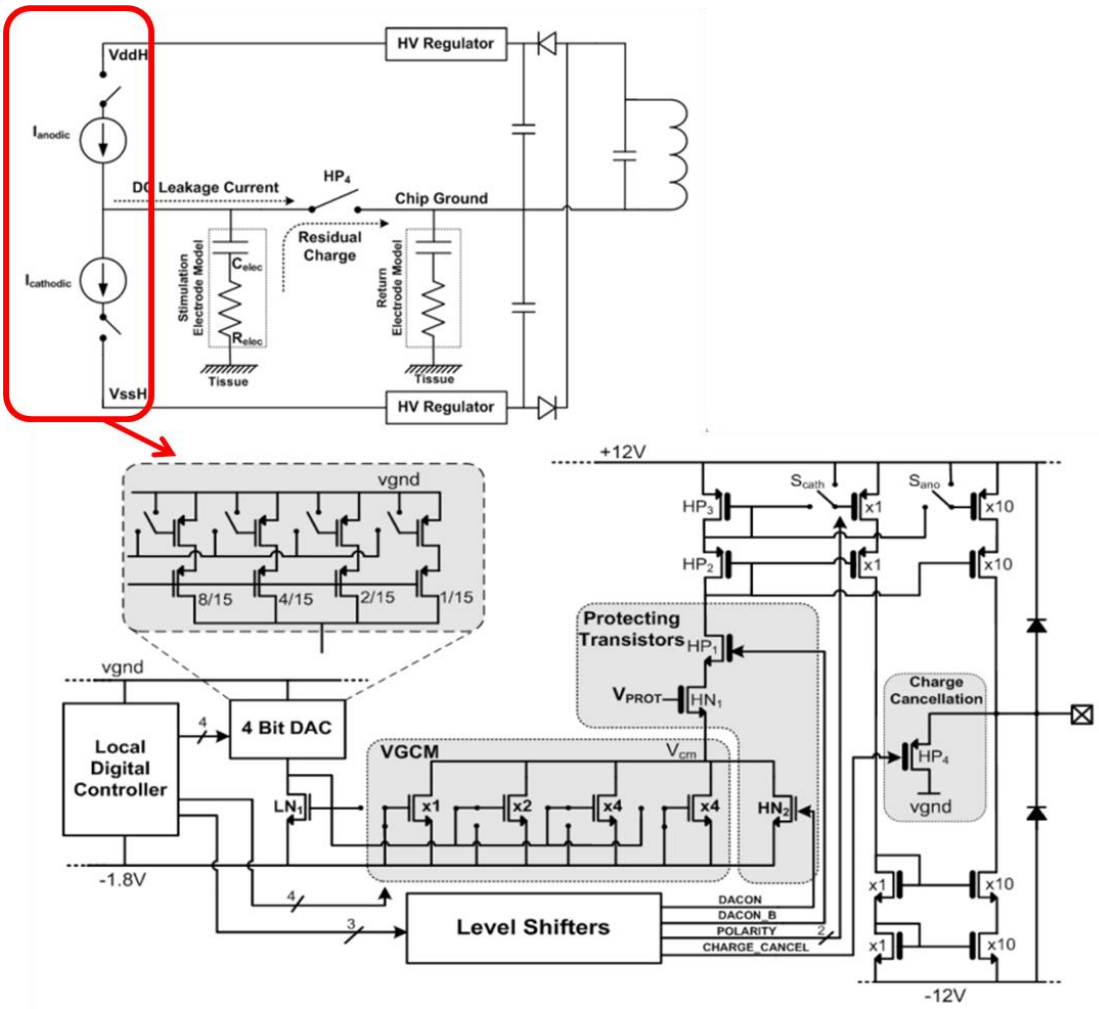


Fig. 2.10. Biphasic stimulator with one-lead per site [23].

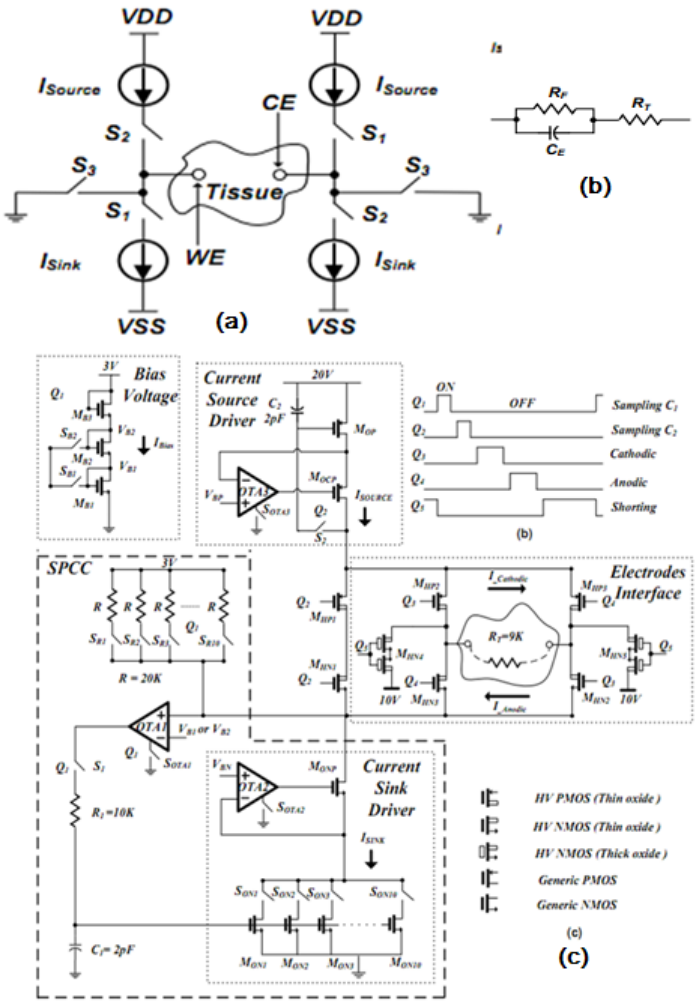


Fig. 2.11. Biphasic stimulator with two-leads per site (bipolar stimulation): (a) circuit model of bipolar stimulus driver (b) circuit model for electrode and tissue surface and (c) bipolar stimulator circuit [24].

Chapter 3

Design of Charge-Balanced Biphasic Stimulus Driver to Suppress Epileptic Seizure on Human Body in the Low Voltage Process

3.1 Introduction

Epilepsy is one of the most common neurological disorder that caused by abnormal discharge in brain. Traditional therapies include pharmacologic treatment and surgical treatment. Pharmacologic treatment is the most common used. For patients who do not respond to the medicament, non-reversible brain surgery is in common use. But the risky surgery may cause functional loss. Furthermore, only 75% do response to traditional therapies [5]. In recent years, functional electrical stimulation (FES) has been demonstrated that can restore some physical functions of a human. Epilepsy is also one of the diseases investigated to be treated by functional electrical stimulation. Nowadays, epileptic seizure becomes predictable by detecting premonition of epileptic seizure from electroencephalography (EEG) or electrocorticogram (ECoG) in time or frequency domains. It has been demonstrated that the epileptic seizure caused by abnormal discharge signals can be suppressed by electrical stimulation before seizure happens. Compare to non-reversible surgical treatment, the advantages of electrical stimulation therapies are harmless to the tissue of the brain. Besides, it can make adjustment arbitrarily and is more flexible. Fig. 3.1 shows the block diagram of an implantable functional electrical stimulation system for epileptic treatment.

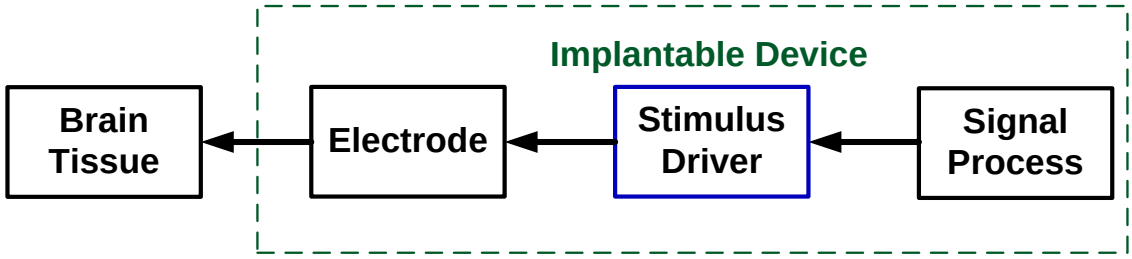


Fig. 3.1. The block diagram of an implantable stimulus driver for epilepsy treatment.

As the transistor size reduces in CMOS technology, the whole system can be integrated into a chip that is implantable, which is also called SoC. Fig. 3.2 shows the architecture of the closed-loop neural-prosthetic SoC for real-time epileptic seizure control, where a signal acquisition unit (SAQ), a bio-signal processor (BSP), an electrical stimulator, a wireless transceiver, and a wireless power supply are integrated [25]. The SAQ and BSP are used to record and recognize seizures. Once a seizure is detected, the BSP sends a command to activate the adaptive stimulator to suppress the abnormal brain activities. Recorded neural signals are transmitted over the MedRadio band (401 to 406MHz) by transceiver to monitor system. Inductive coils over the ISM band (13.56MHz) wirelessly transmit the required power. Data transmission is encoded through a reliable cyclic redundancy check (CRC).

The well-developed CMOS processes had been attractive to realize the implantable device for biomedical electronic applications. But the operation voltage of the stimulator is usually higher than the device normal operating voltage of a low-voltage CMOS process, so the stimulator was usually implemented in the high-voltage CMOS process [26]. According to the request of our biomedical project for epilepsy treatment, the required maximum loading voltage is as high as 9V. For SoC integration purpose, the other circuits including data decoder, rectifier, regulator, demodulator in the implant SoC device are all designed and realized in the low-voltage CMOS process to reduce power consumption. So the stimulator

combined with a high voltage generator implemented in the low-voltage CMOS process is needed [27].

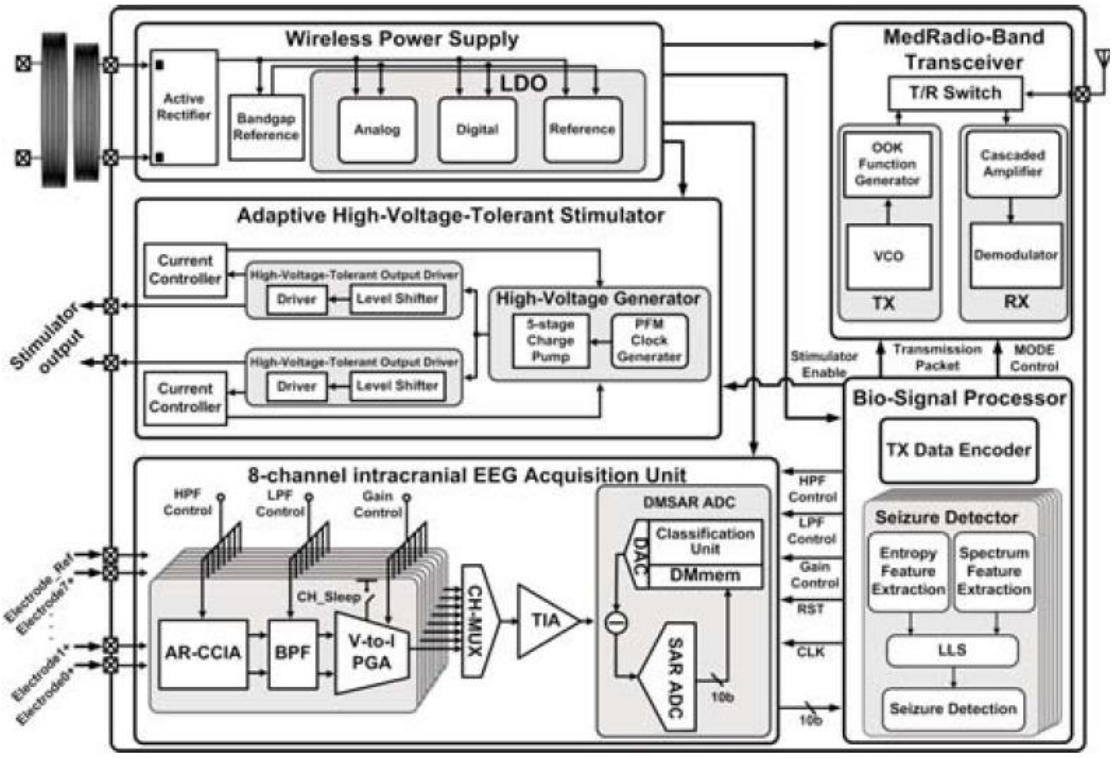


Fig. 3.2 Architecture of the epileptic seizure-control SoC [25].

In this chapter, the design of charge-balanced biphasic stimulator is proposed. Then, the detailed circuit simulation and measurement results of the proposed design will be presented in the following sections. In the fourth section of this chapter, some discussions of the problems found in the measurement and the solutions of these problems are presented. Finally, the summary of the measurement results and the simulation results of the modified stimulus driver are shown in the final section of this chapter.

3.2 Design of Charge-Balanced Biphasic Stimulus Driver

The biphasic current is required in functional electrical stimulation (FES) to make sure the light injury to the cell. For the wider range of the resistance of the electrode and the higher stimulus current, high operation voltage is inevitable in this work. In addition, the mismatch between the anodic and cathodic current pulses leads to residue charge in the tissue. Prolonged electrical stimulation of structures in the central nervous system or of peripheral nerves can induce neural injury [28]. Some papers showed that the safe window of the residue charge accumulated in human body is about 100mV [29]. Since it is medical devices, the reliability and safety are important. In this work, the stimulus driver could self-generate high enough voltage to drive high impedance voltage drop. Furthermore, the reliability is guaranteed for output driver and VCC generator in the low voltage process so the safety is ensured. Within the range of adaptive resistance and capacitance, the proposed stimulus driver would provide the constant current pulses. Besides, charge-balanced techniques are implemented in the stimulus driver to provide safe stimulation.

3.2.1 Impedance Analysis

Before the circuit design, the influence of the loading impedance to our stimulator should be investigated first, and then the architecture of the circuit can be decided and circuit performance can be optimized according the measured loading impedance. The measurement setup is shown in Fig. 3.3. The stimulator (Grass S12X) is connected to the cortical electrodes which implanted in the human body. After stimulation, the parameters such as loading voltage drop and the impedance of this stimulation will be shown on the screen of the stimulator. The equivalent circuit of the electrode-tissue and the measurement results are shown in Fig. 3.4 as for the aspect of resistance and capacitance [30]. Capacitance C_{d1} represents the interface between two

materials (metal and meat). R_f represents the faradaic resistance because of electrochemical process in the electrodes. Rs is the spreading resistance on behalf of the hindrance for the ionic flow. The measurement results, for C_{d1} is about 100nF, for R_f is more than 10MΩ, and for Rs is about 1kΩ~3kΩ.

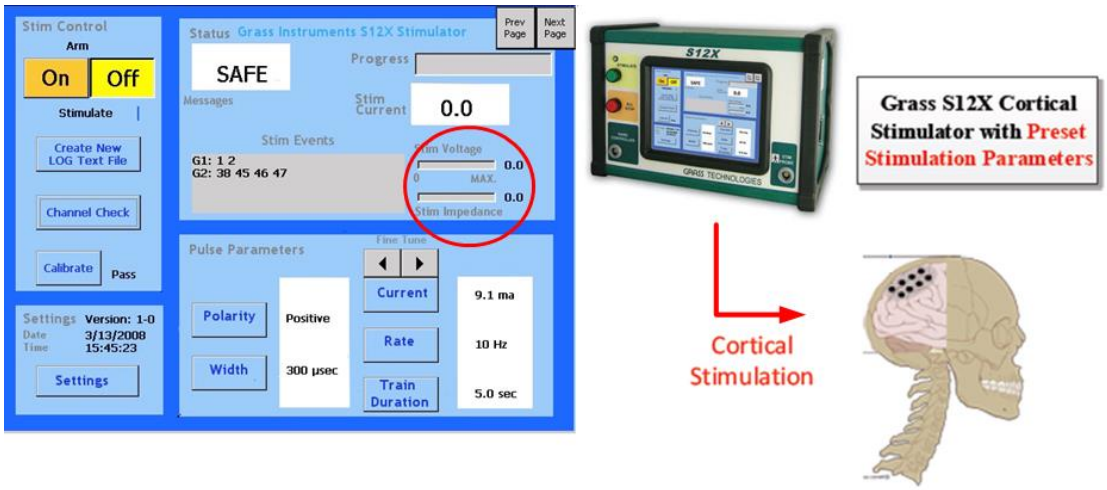


Fig 3.3 Electrode-tissue impedance measurement setup.

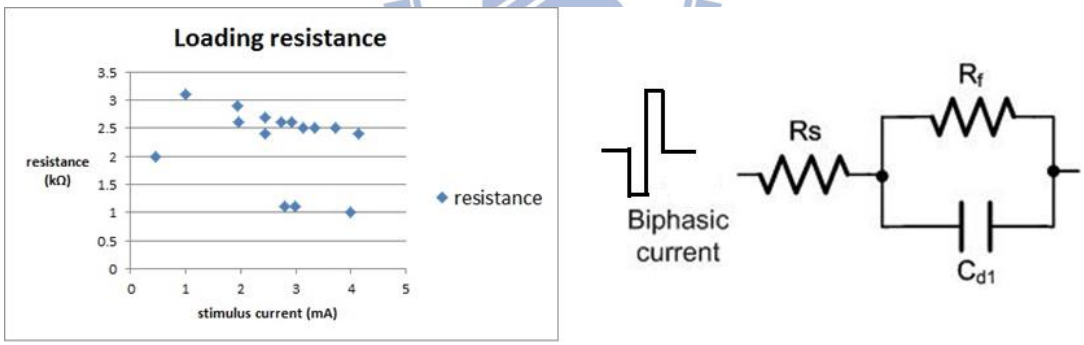


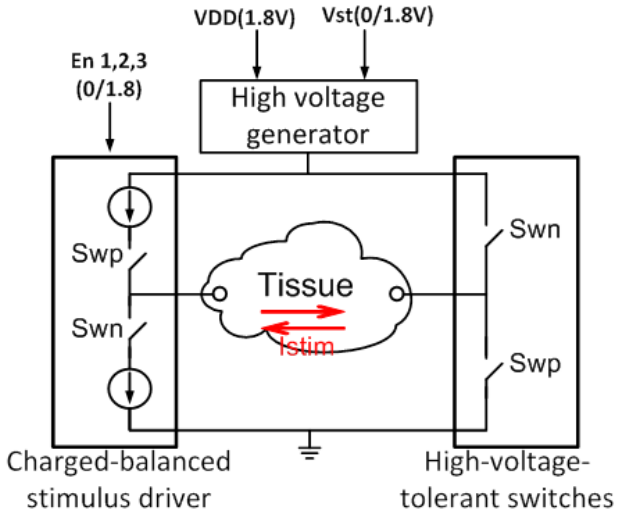
Fig 3.4 Electrode-tissue impedance measurement results and electrode-tissue impedance model [30].

3.2.2 Architecture

The proposed charge-balanced biphasic stimulus driver consists of three parts: output driver, high-voltage-tolerant switches, and VCC generator, as shown in Fig. 3.5. The stimulation methodology of the output driver is bipolar fashion. When in positive

stimulation, switches Swp are closed and switches Swn are open. On the contrast, when in negative stimulation, switches Swp are open and switches Swn are closed. With maximum output stimulus current 3mA, the stimulus current amplitude is controlled by 3 bits enable signals.

From the former section, we have known that depending on different kind of stimulus sites and implanted time, tissue impedance varies from 1kΩ to 3kΩ. And the effective stimulus current is up to 3mA. These specifications results in a large voltage drop up to 9V on the loading. So the high voltage generator is needed to generate 10V VCC for the stimulus driver. To handle with the large rail-to-rail voltage, some techniques are used to avoid low voltage devices from overstress.



Enable signal (En1,2,3)	Stimulus current (Ist.)
001	0.5mA
010	1mA
011	1.5mA
100	2mA
101	2.5mA
110	3mA

Fig 3.5 Circuit architecture and the stimulus current specification of the proposed charge-balanced stimulus driver.

First is the voltage limiting technique, which is often used in this design. The main idea is to control the source voltage of a transistor by giving a suitable gate voltage to meet required reliability, as shown in Fig. 3.6. If there is no current through Mn1 and Mn2, the source voltage of Mn1 and Mn2 will be charged up by leakage current until it is equal to its gate voltage. If there is a current flowing through Mn1

and Mn2, the aspect ratio of the transistor is designed to be large enough so that the V_{GS} of Mn1 and Mn2 are slightly larger than the threshold voltage (V_{th}). The drain voltage of Mn1 and Mn2 is controlled by the source voltage of the transistor cascoded above. The stacked PMOS at output stage works in a similar way. Besides, the deep N-well layer is used to isolate the P-well region of each stacked NMOS from the common P-substrate.

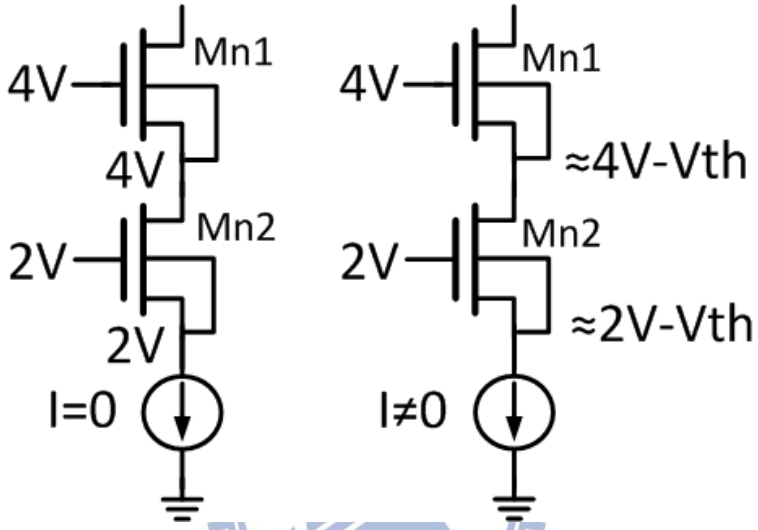


Fig. 3.6. Concept of voltage limiting technique.

Next is the dynamic current mirror, which is used to achieve charge-balanced stimulation. As shown in Fig. 3.7, in the sampling phase, the current source feeds the stimulus current to the diode connected MOSFET Ms. After sampling phase, the sampling switches are open and capacitor Cs maintains the gate voltage thus the drain current of Ms remains equal to Iin. When the output switch is closed, the memorized drain current is available at the output. The accuracy of dynamic current mirrors is independent of the mismatch of the transistors building up the mirror, because the same transistor is sequentially used at the input and the output of the mirror [31].

Fig. 3.8 shows the operation time diagram of the proposed stimulus driver. There are three operation phase in a complete stimulation. First is the sampling phase, use

dynamic current mirror to generate a charge-balanced current source for stimulation. Second and third are positive and negative stimulation phase separately. The anodic and cathodic current pulse are controlled by the control signals pstim and nstim in Fig. 3.8.

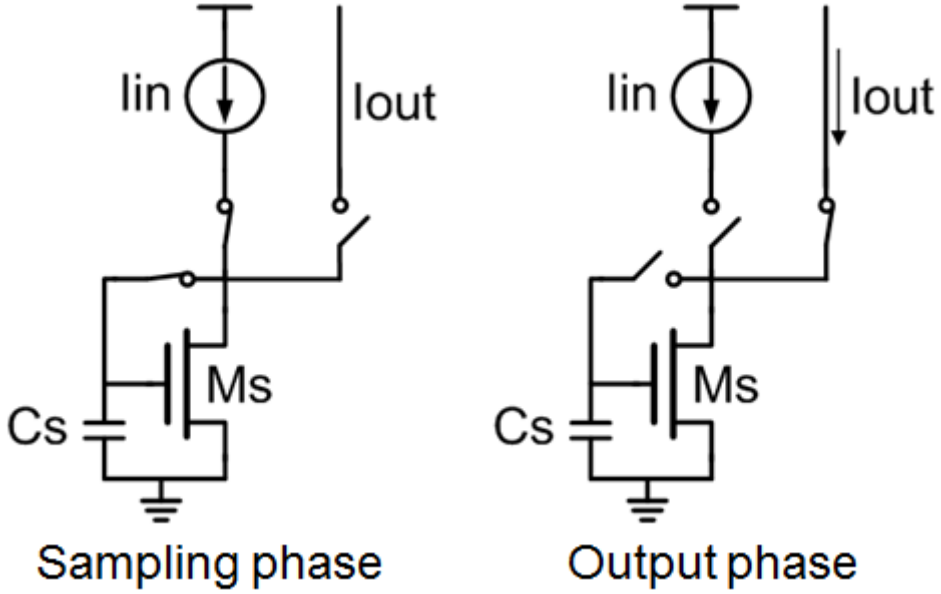


Fig. 3.7 Concept of dynamic current mirror.

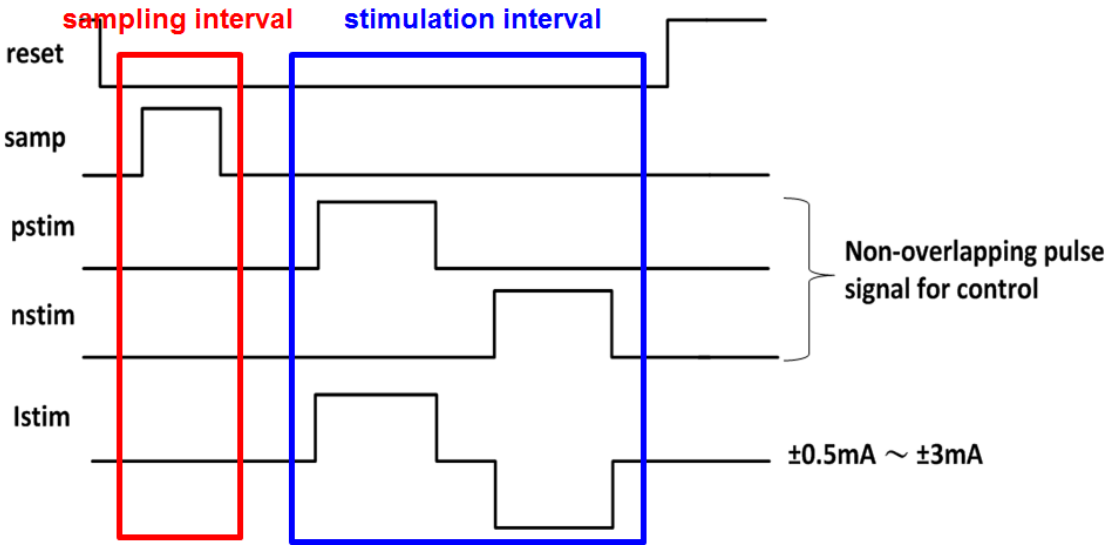


Fig. 3.8 Control signals and output waveform.

3.2.3 Output Driver and High-Voltage-Tolerant Switches Circuit

The circuit implementation of the proposed charge-balanced stimulator is illustrated in Fig. 3.9(a). The stimulus current is generated by the DAC which consists of 1.8V core device, then multiplied by ten to the output stage. The output stage is comprised of stacked 3.3V I/O devices with dynamic gate bias to handle with the high operation voltage.

When in sampling phase, switches S1,Ssmp, and Sbot are closed, the stimulus current feeds to the sampling MOSFET and its gate voltage is memorized in capacitor Cs to create a charge-balanced current source for stimulation. As shown in Fig. 3.9(b). The stacked device under the sampling current source increases the output impedance of the sampling current source, and makes the performance of load regulation better. In addition, switch S1 opens with a little delay to switch Sbot to decrease the influence of the charge injection from S1 to the gate of the sampling current source. This technique is called bottom-plate sampling to enhance the accuracy of the sampling voltage.

After sampling phase, switches S1 and Ssmp are open, and switches S2 and Swp are closed to create the path for positive stimulation. As shown in Fig. 3.9(c). The stimulus current starts from the sampling current source, and then passes through the tissue to ground. All the stacked MOSFETs on the path are given gate bias to keep their drain-to-source voltage under the tolerant voltage. In the next phase, inverted stimulus current is needed to depolarize the cells of these neurons on the tissue. For this reason, switches S2 and Swp are open, and switches Swn and S3 are closed to create the current path for negative stimulation. The stimulus current starts from VCC, and then passes through the tissue to the current sink. As shown in Fig. 3.9(d). After the whole stimulation, the high voltage generator is shut down to save the power.

The headroom voltage of the current sink and the sampling current source are under 1V, to achieve the specification of maximum stimulus current is 3mA, with maximum loading resistance 3kΩ.

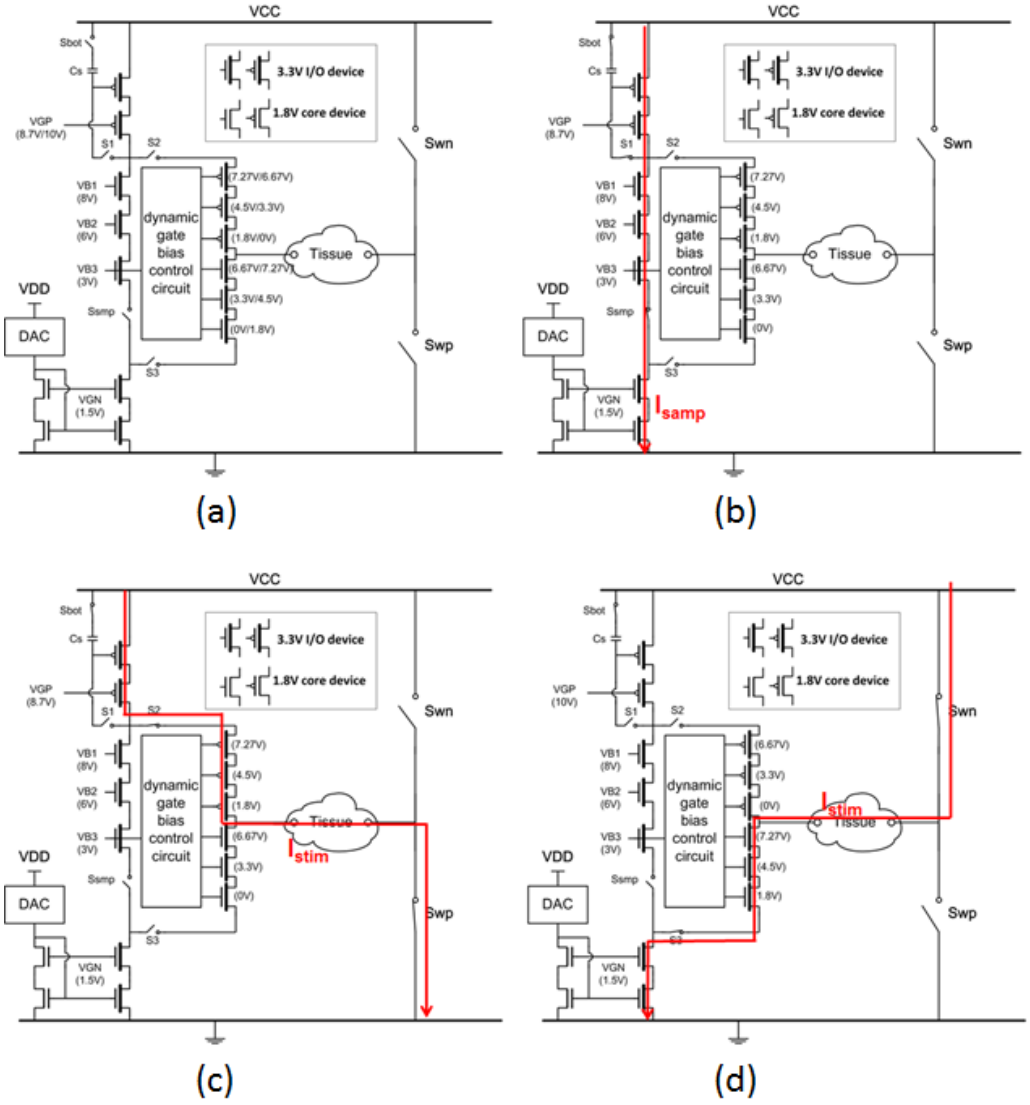


Fig. 3.9 The schematic of the (a) output driver, (b) operation in sampling phase, (c) operation in positive stimulation, and (d) operation in negative stimulation.

Fig. 3.10 shows the schematic of the current DAC and the high-voltage-tolerant switches. The current generated by the reference current source is 10μA. Then the current is amplified by the current DAC and the final stage current mirror. 3-bit amplitude control signals control the current DAC to generate 50~300μA output

current, and then the current is multiplied by ten to the final output stage current mirror. For the high-voltage-tolerant switches, Psw1 turns on for positive stimulation; On the other hand, Nsw1 turns on for negative stimulation. All the stacked MOSFETs are well biased with voltage limiting technique to avoid overstress when switches turn off.

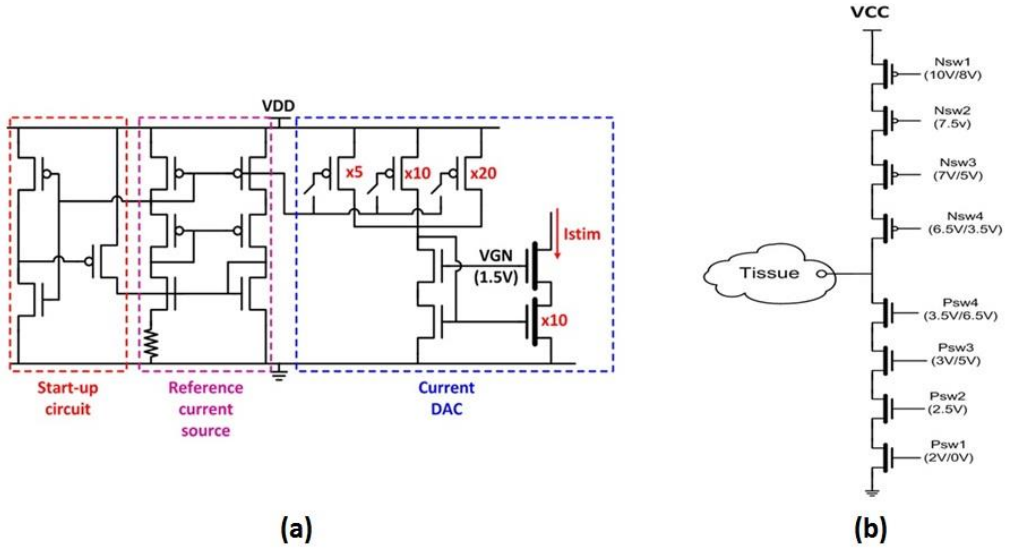


Fig. 3.10 The schematic of (a) current DAC and (b) high-voltage-tolerant switches.

3.2.4 Dynamic Bias Circuit

In this section, the most important part of the voltage limiting technique is introduced. To achieve voltage limiting technique, different level of gate bias voltages are needed. And in different operation phases, these gate bias voltages also need to change. Therefore, the dynamic bias circuit is the core of the proposed stimulus driver, which provides all the gate bias voltage for the stacked MOSFETs to prevent them from overstress.

Fig. 3.11(a) shows the architecture of the dynamic bias circuit. Stacked diode connected NMOS with anodic node connect to VCC, the other node connect to the output of logic circuit. Control the tail node of this stacked diode connected NMOS

chain by logic signal, the voltage divided by this stacked diode connected NMOS chain can be changed by the control logic signal. However, because of the 1.8V external power supply, the changing range of the bias voltage is also restricted under 1.8V. It's not enough to control some switches of the driver. For example, switch S1 needs control signal 7V~10V. Therefore, another bias circuit is needed to generate the high dynamic range gate bias voltage.

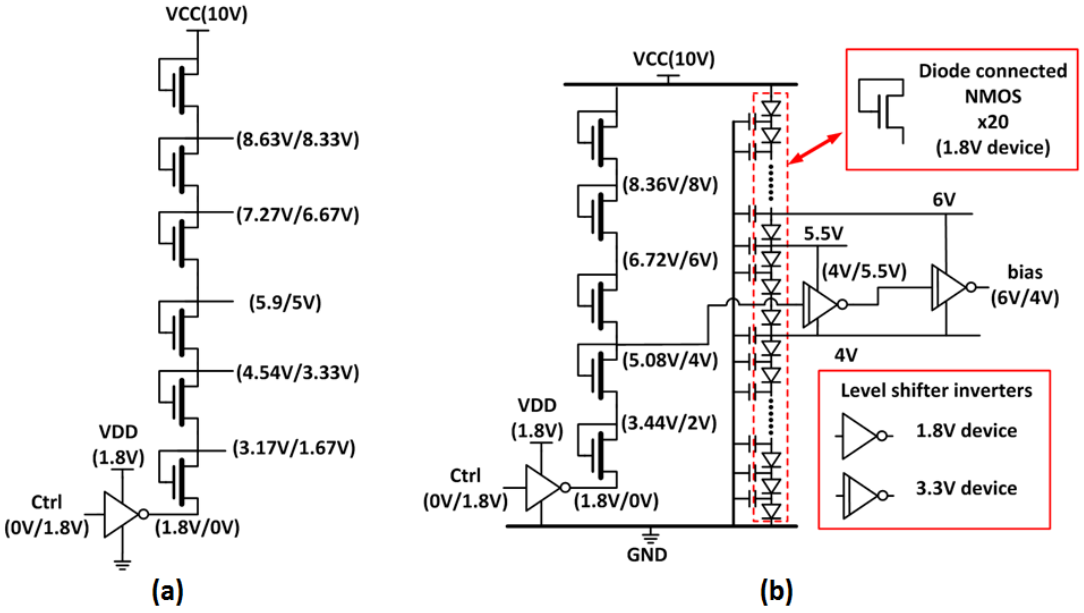


Fig.3.11 The schematic of (a) type I and (b) type II dynamic bias circuit.

The type II dynamic bias circuit is shown in Fig.3.11(b). It combines type I dynamic bias circuit and a level shifter. Twenty diode connected NMOS divide the VCC voltage into equivalent twenty pieces with 0.5V a step. These voltages are used to as the power rails of the level shifter. Then choose a proper logic voltage level output of the type I dynamic bias circuit, as shown in Fig.3.11(b), we choose the output with logic voltage level 5.08V/4V. Then connect the output to inverter chains for level shifting. These inverters are connected to the power rails that we made before by twenty diode connected NMOS. The upper power of these inverters is

connected to 0.5V higher than its input logic voltage level. Because the threshold voltages of the PMOSs in these inverters are higher than 0.5V, the logic voltage level can be shifted to 0.5V larger than the original level. As the example in Fig.3.11(b), the first inverter's upper power rail connected to 5.5V to shift the 5.08V/4V logic voltage level to 5.5V/4V. And then the next upper power rail of the inverter connects to 6V to shift the 5.5V/4V logic voltage level to 6V/4V. By repeating these steps, we can provide all the dynamic range under the 10V VCC voltage. Besides, the switching current of the inverter chains may influence the rail voltages. To provide more stable power rails, all the power rails are connected a capacitor to stabilize the rail voltages.

3.2.5 High Voltage Generator

Fig. 3.12 depicts the architecture of the high voltage generator, which is composed of a 6-stage charge pump, an error amplifier, a voltage-controlled oscillator (VCO), a two-phase clock generator, a set of buffer, and an output capacitor C_B. The high voltage generator has two operation mode controlled by signal Vst. When the stimulator is in stimulation, the signal Vst will be logic 1, and the charge pump start to pump, finally the output voltage VCC from the high voltage generator will be regulated at voltage level 10V. When the stimulator is not in stimulation, the signal Vst will be logic 0, VCO is turned off, and thus the voltage level of VCC is at almost 0 V. The power consumption of the stimulator not in stimulation can be reduced.

The used charge pump circuit is adopted from [32], it can output the high voltage level (> V_{DD}) without the issues of electrical overstress and gate-oxide reliability. The desired output voltage level is at 10V, and V_{DD} is 1.8V, so 6-stage charge pump circuit is used in this high voltage generator, as shown in Fig. 3.13 Because the used charge pump circuit has dual path, it needs two pumping capacitors C_P per stage, thus

a two-phase clock generator, shown in Fig. 3.14, is used to transform one-phase clock to non-overlap two-phase clock. Besides, to handle with the high loading current, these pumping capacitors are up to 100pF. In layout area consideration, we decide to use off-chip capacitors as pumping capacitors.

Under fixed pumping frequency, the voltage level of VCC can be varied with the change of the loading current from VCC, so the pulse frequency modulation (PFM) is adopted to regulate VCC. The amplifier used in high voltage generator, shown in Fig. 3.15, the output Vctrl of this amplifier is adjusted by the voltage difference between the reference voltage and the feedback voltage. The clock frequency of VCO is controlled by Vctrl, and the used VCO circuit is shown in Fig. 3.16. When VCC < 10V, the frequency of clkr will arise until VCC > 10V; and when VCC > 10V, the frequency of clkr will decrease until VCC < 10V. VCC can be regulated almost at the voltage level 10V.

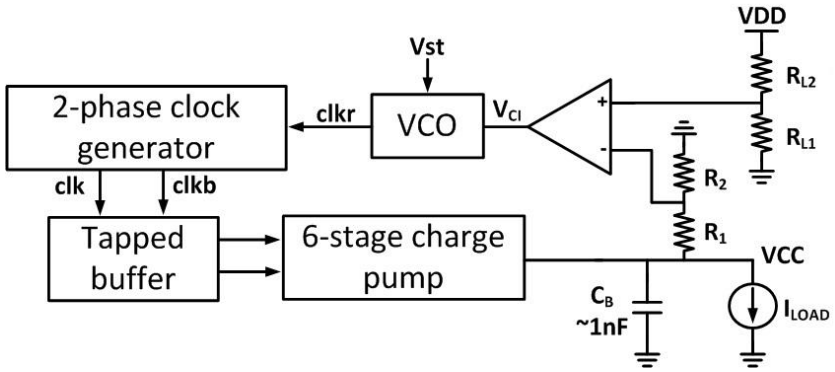


Fig. 3.12 The architecture of the proposed high voltage generator.

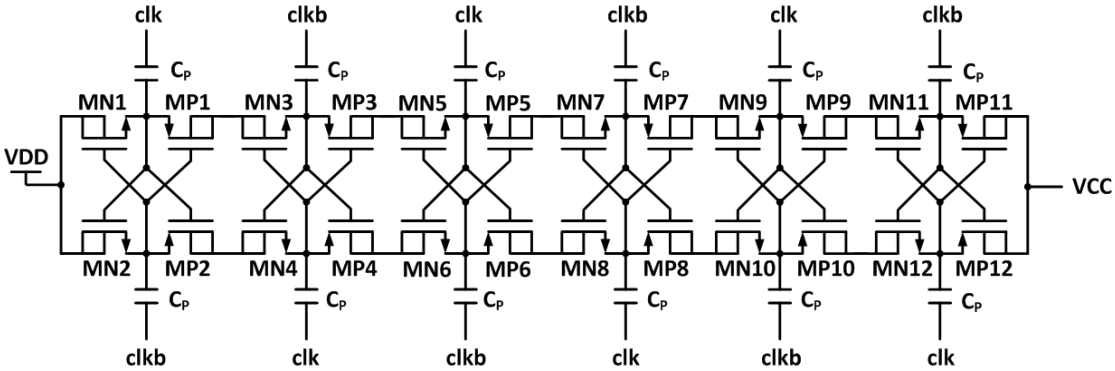


Fig. 3.13 The schematic of 6-stage charge pump circuit [32].

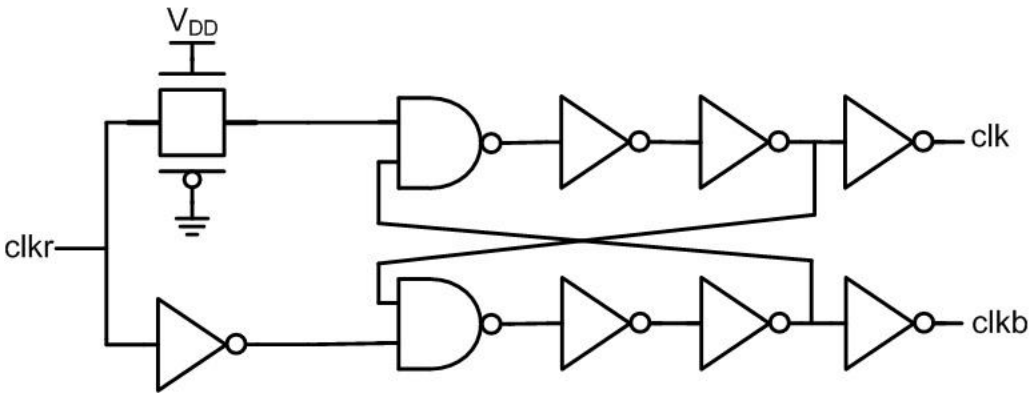


Fig. 3.14 The schematic of non-overlap two-phase clock generator.

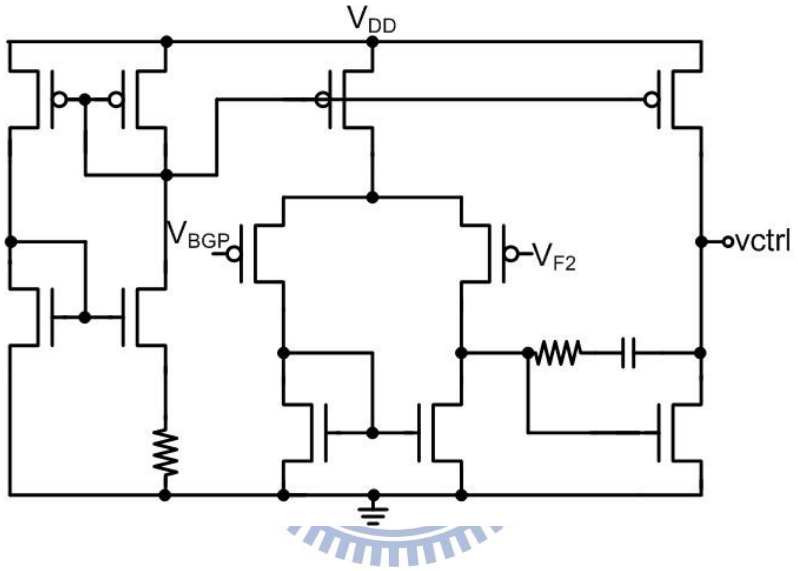


Fig. 3.15 The schematic of two-stage amplifier.

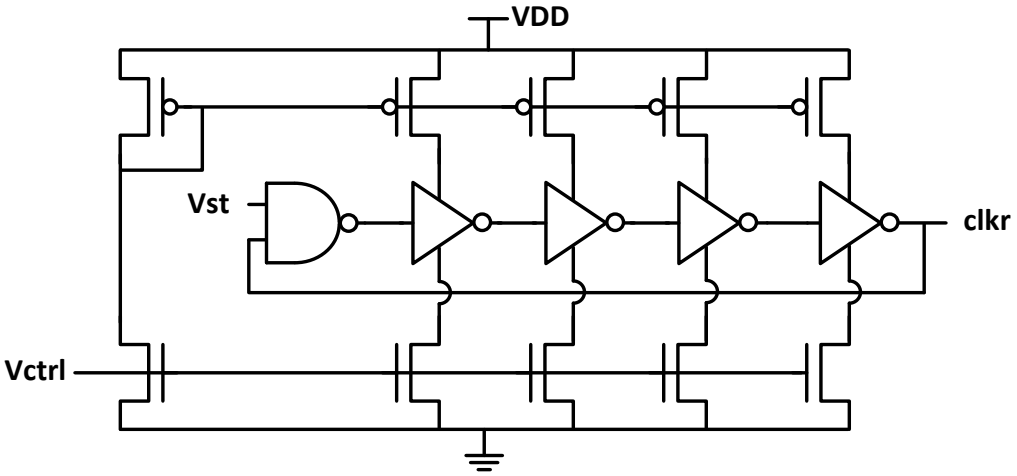


Fig. 3.16 The schematic of voltage controlled oscillator.

3.3 Simulation and Measurement Results

3.3.1 Simulation Results

The proposed stimulator had been simulated in HSPICE with TSMC 0.18μm 1.8V/3.3V CMOS process. Fig. 3.17 shows the simulation result of the high voltage generator. The current dissipation of the dynamic bias circuit is about 500μA. With maximum stimulus current 3mA, the whole loading current is up to 3.5mA. To make sure that the stimulus driver can function well, we overdesign the maximum loading current to 4mA. The maximum operation frequency is about 160MHz, under the state of 4mA loading current.

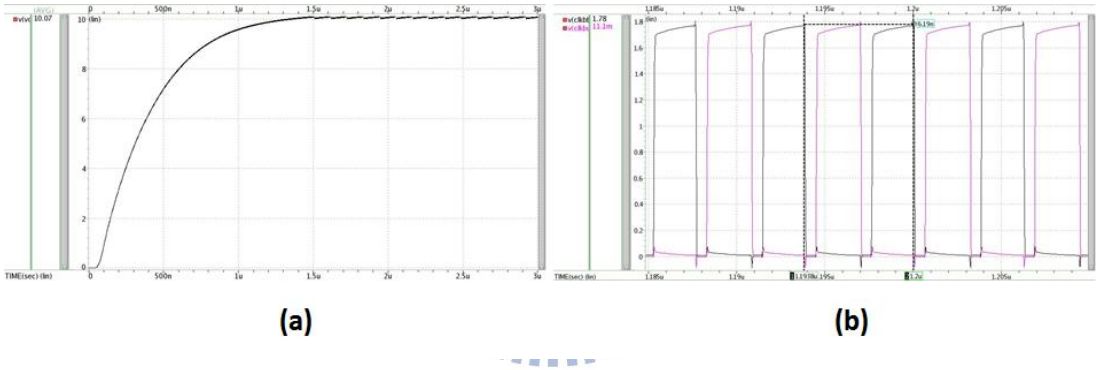


Fig. 3.17 The simulation results of (a) VCC generator with 4mA loading current, and (b) 2-phase non-overlapped clocks.

To verify the function of charge-balanced technique, we had run the MONTE CARLO analysis. Fig. 3.18 (a) and (b) show the waveform of all scale of the stimulus current and the simulation results of MONTE CARLO analysis. Although the devices' size mismatches lead to about 170μA current difference, the maximum mismatch between anodic and cathodic is under 9μA. In addition, we had run the simulation of long term positive stimulation to observe the current mismatch caused by the leakage of the sampling capacitor. As shown in Fig. 3.18 (c). After about 500μs stimulation,

the current mismatch is about 7μA. The function of charge-balanced technique is verified by this simulation.

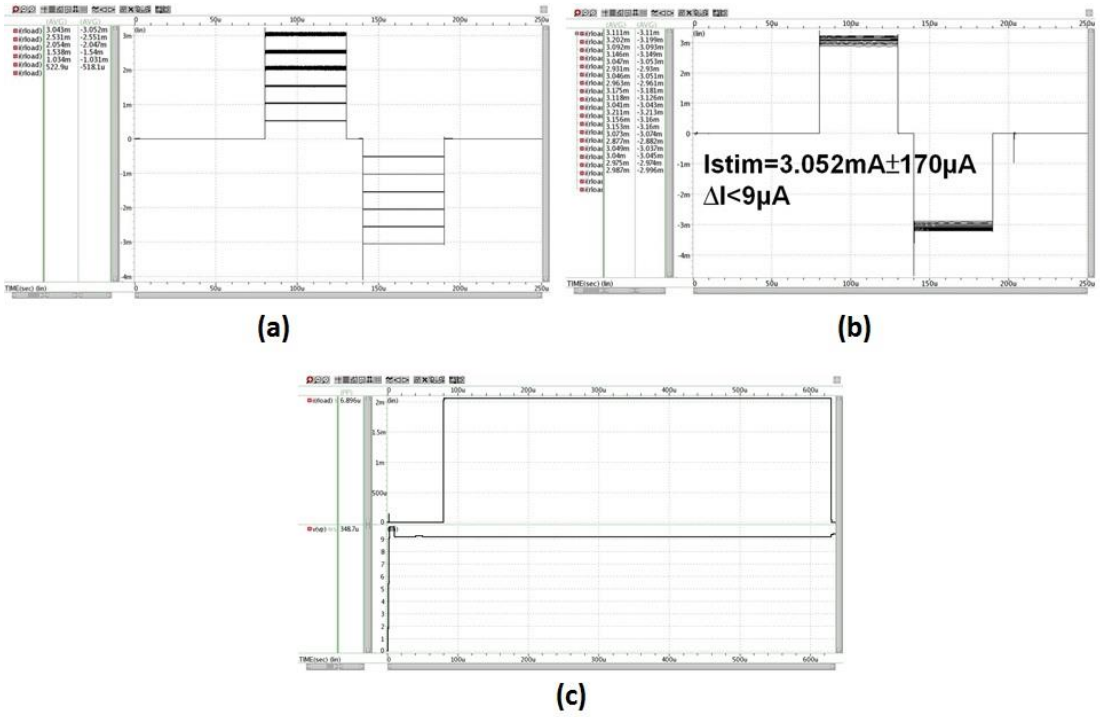


Fig. 3.18 The simulation results of (a) all scale of the stimulus current, (b) MONTE CARLO analysis, and (c) long term positive stimulation.

3.3.2 Measurement Results

The proposed charge-balanced biphasic stimulator had been fabricated in TSMC 0.18μm 1.8V/3.3V CMOS process. The microphotograph of the fabricated chip is shown in Fig. 3.19, which includes a high-voltage-tolerant stimulus driver, a current DAC, and a high voltage generator, and total area is 1.13 × 1.55 mm^2. The chip had been assembled in package for measurement.

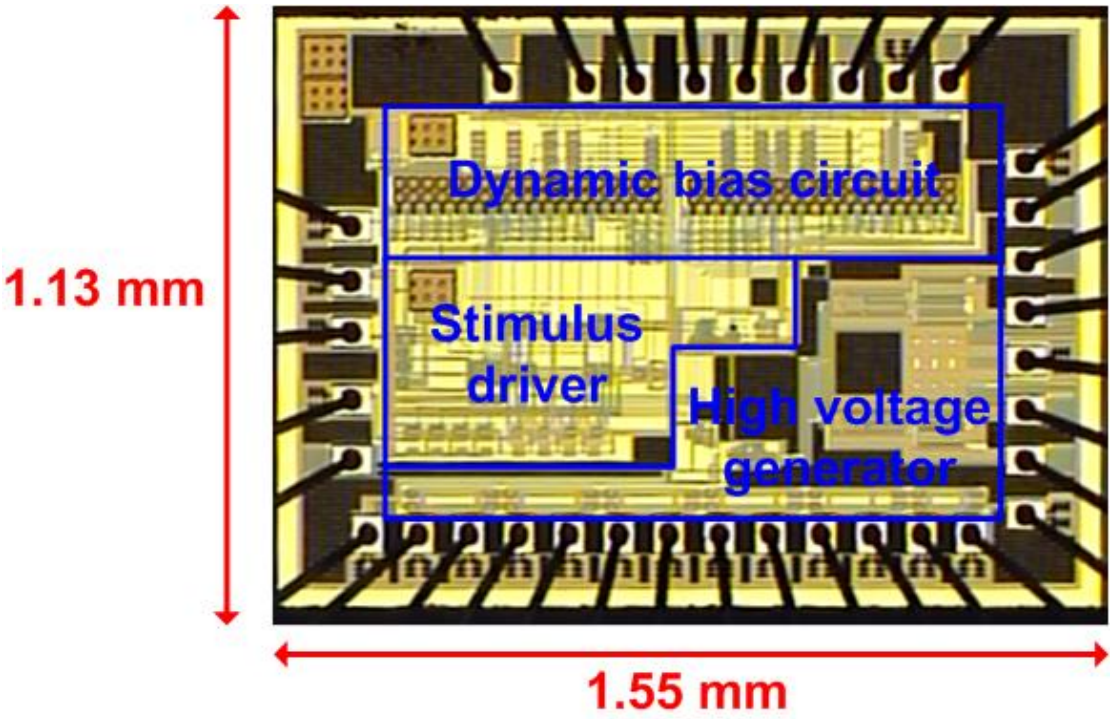


Fig. 3.19 The microphotograph of the fabricated stimulator chip.

Fig. 3.20 shows the measurement setup, Keithley 2400 is used to provide the fixed 1.8V power supply V_{DD}. Two function generators Agilent 81110A are used to provide the control signals. The oscilloscope Agilent DSOX3034A is used to observe the output waveforms.

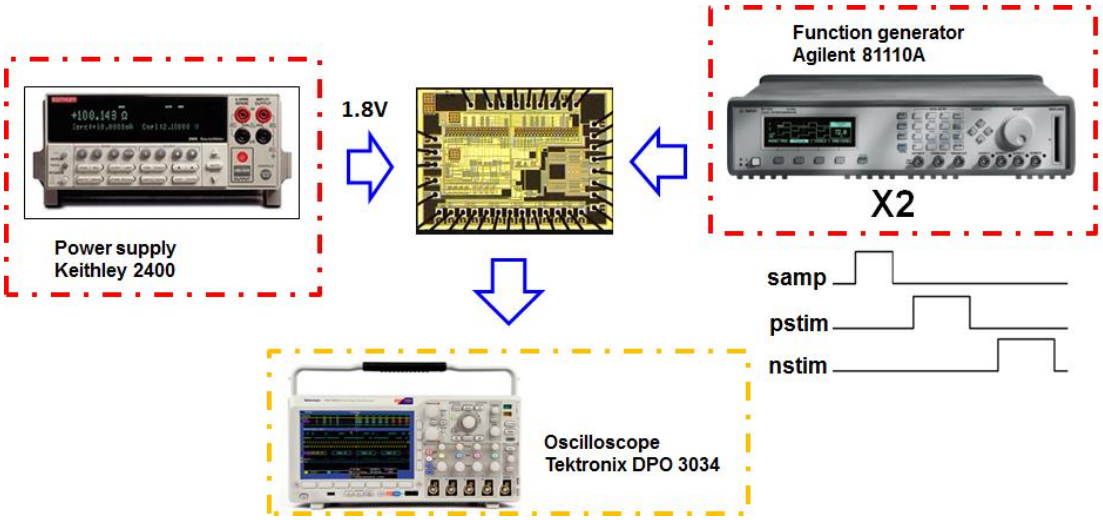


Fig. 3.20 The measurement setup of the power meter, the function generator, the oscilloscope.

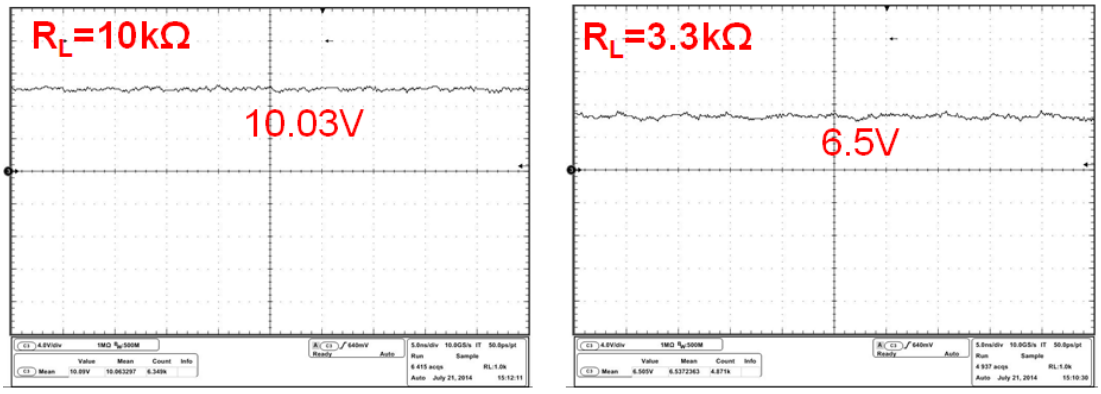


Fig. 3.21 The measurement results of the high voltage generator.

Fig. 3.21 shows the measurement results of the high voltage generator. With loading resistance 10kΩ, the high voltage generator can maintain output voltage 10V. But when loading resistance decrease, which means loading current increase, the high voltage generator can't sustain the higher loading current and the output voltage is decrease. In order to realize what leads to this problem, further measurements of the high voltage generator are done. Fig.3.22 shows the measurement results of 2-phase non-overlapped clocks and the power supply V_{DD} of the tapped buffer. The frequency of the clocks is about 143MHz, which isn't so far away from simulation results, but the clocks are overlapped as shown in Fig. 3.22(a). And because of high switching frequency and large simultaneous current of the tapped buffer, the power supply can't maintain stable at 1.8V. This makes the switching noise problem serious and makes the clocks overlapped. The overlap of pumping clocks may be the reason to the failure.

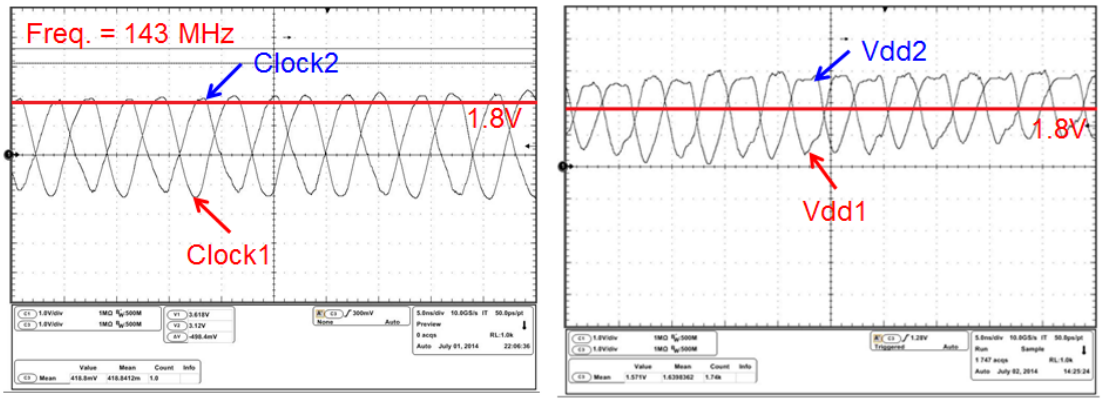


Fig. 3.22 The measurement results of (a) 2-phase clocks (b) V_{DD} of the tapped buffer.

The following measurements of stimulus driver use external 10V power supply as VCC because of the failure of high voltage generator. The measurement results of the stimulus driver are shown in Fig. 3.23. Using a 2kΩ resistor series a 100nF capacitor as the loading tissue model. Fig. 3.23(a) shows the node voltage difference of the loading. When in positive stimulation, the anodic node voltage jump because the loading resistance. Then the anodic node voltage arises slowly as the stimulus current charge the loading capacitor. After positive stimulation, we can observe that the voltage difference between the loading tissue is positive. So inverted stimulus current is needed to discharge the residue charge in the loading capacitor. After the negative stimulation, the voltage difference between the loading tissue is recover to nearly zero. Besides, by measure the node voltage difference between the loading resistor, and then divide to its resistance value, we can get the stimulus current pass through the loading tissue. As shown in Fig. 3.23(b).

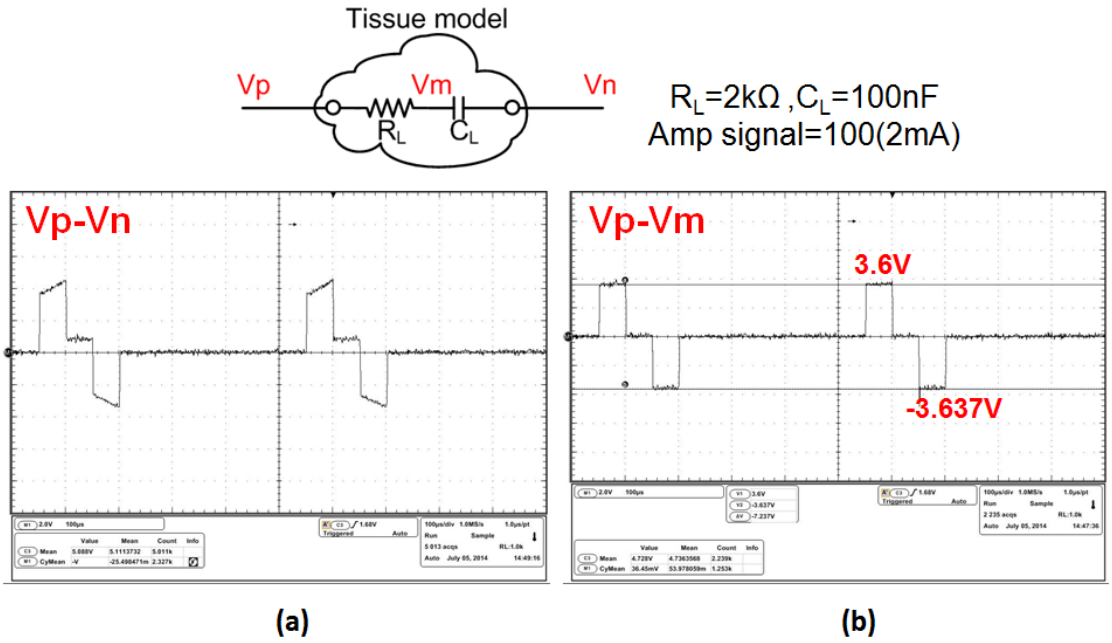


Fig. 3.23 The measurement results of (a) node voltage difference between loading tissue, and (b) node voltage difference between loading resistor.

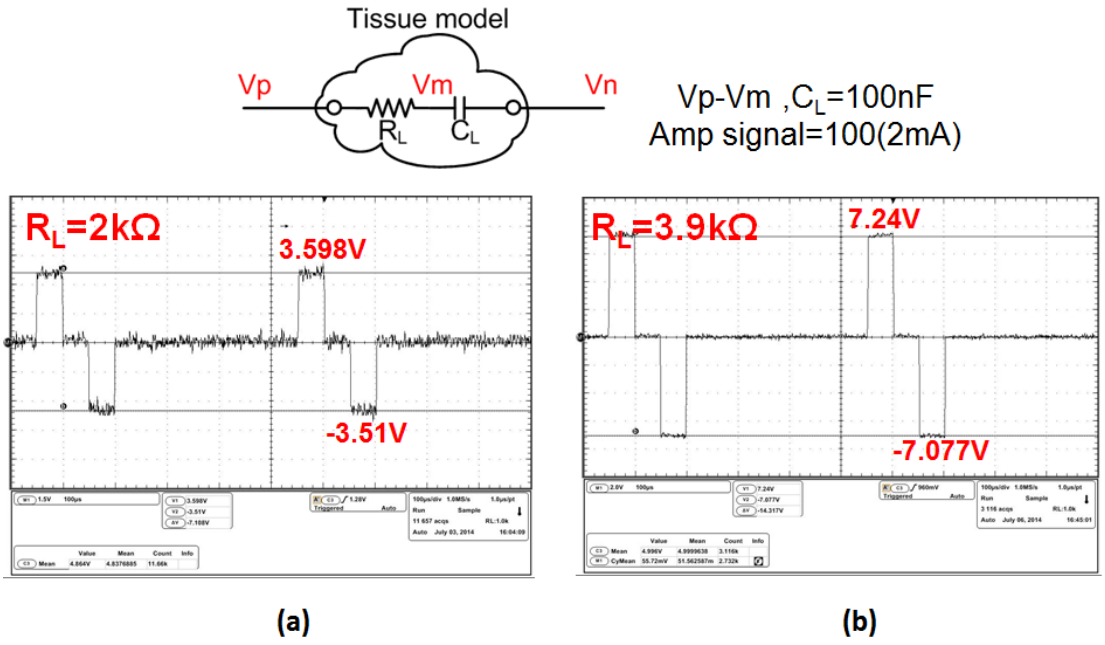


Fig. 3.24 The measurement results of stimulus driver with loading resistance (a) 2kΩ, (b) 3.9kΩ.

Next, the stimulus current under different loading resistance value is measured. As shown in Fig. 3.24. With loading capacitance 100nF and the amplitude signals set at 100(target current 2mA), the stimulus current is still nearly the same under different

loading resistance value.

The next figure, Fig. 3.25, shows the statistical plot of measured stimulus current versus 3-bit amplitude signals. The stimulus current decreases about 10% compare to simulation results, but still remain linear relation to the 3-bit control signals. The 10% degradation of the stimulus current may be caused by the sizing mismatch of the current DAC and the variation of the resistor in the reference current source.

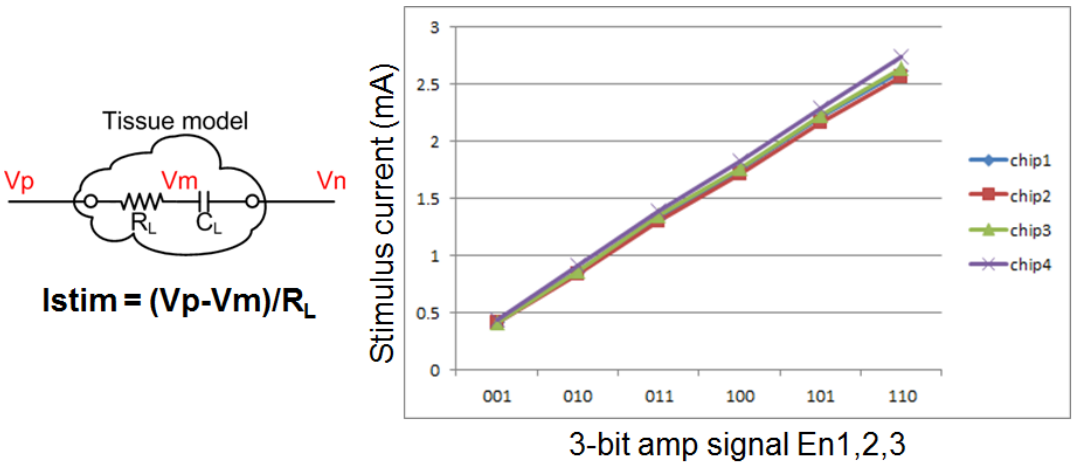


Fig. 3.25 The statistical plot of measured stimulus current versus 3-bit amplitude signals.

The measurement results of the relative current mismatch between anodic and cathodic current pulses under different 4 chips versus 3-bit amplitude signals are shown in Fig. 3.26 and Fig.3.27. Fig. 3.26 shows the absolute value of the relative current mismatch. The maximum current mismatch is under 40μA, with stimulus current pulse width 50μs and loading capacitance 100nF, the residue charge voltage is about 20mV, under the safe window 100mV. Fig. 3.27 shows the mismatch in percentage to the cathodic current source. The maximum mismatch percentage is under 1.7% in the measurement results.

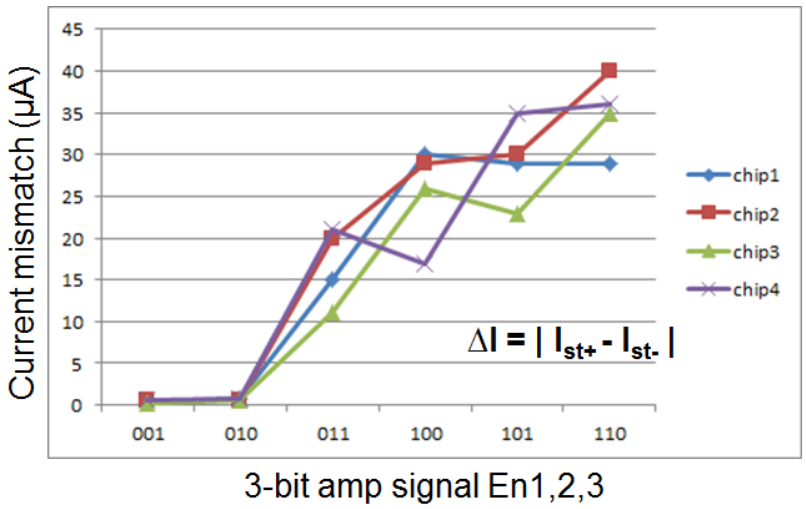


Fig. 3.26 The absolute value of relative mismatch between anodic and cathodic stimulus current.

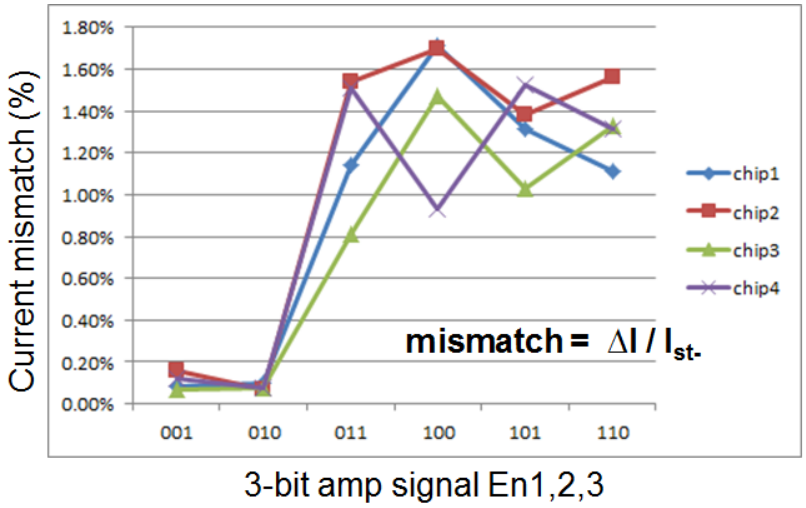


Fig. 3.27 The percentage of relative mismatch between anodic and cathodic stimulus current.

Table 3.1. Summary of the measurement results.

	Spec.	Simulation	Measurement
Vin	1.8V	1.8V	1.8V
VCC	10V	10.1V	External 10V
Stimulus current	0.5mA 1mA 1.5mA 2mA 2.5mA 3mA	0.551mA 1.084mA 1.613mA 2.140mA 2.664mA 3.186mA	0.424mA 0.869mA 1.339mA 1.764mA 2.226mA 2.639mA
Current mismatch	minimum	<1.66%	<1.7%
Standby power	minimum	56.6μW	169.2μW
Process	TSMC 0.18μm 1.8V/3.3V CMOS process		

※Current mismatch = |cathodic-anodic| / cathodic

3.4 Problem Discussion and Circuit Modification

3.4.1 Problem Discussion

During measurement, we found some problems when the loading resistance value is too small. The problem will lead to an irreversible damage of the stimulus driver and make the positive stimulation fail. As shown in Fig. 3.28. The stimulus driver fails to output charge-balanced stimulation.

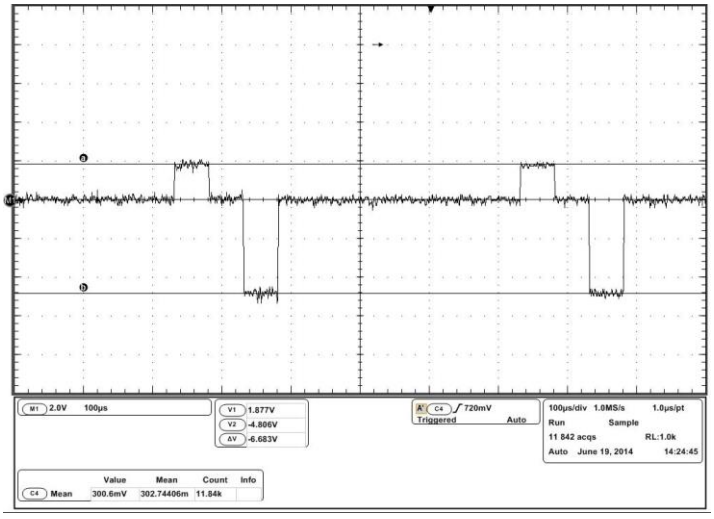


Fig. 3.28 Failure stimulation with low loading resistance value.

Then back to check the circuit design to find the reason, we found that there are some problems of the gate bias voltage on the stimulus path stacked MOSFETs. As shown in Fig. 3.29, because of improper gate bias voltages, some MOSFETs are under overstress and have some damages. The damage leads to the current leakage, which makes the increase of mismatch between positive and negative stimulus current.

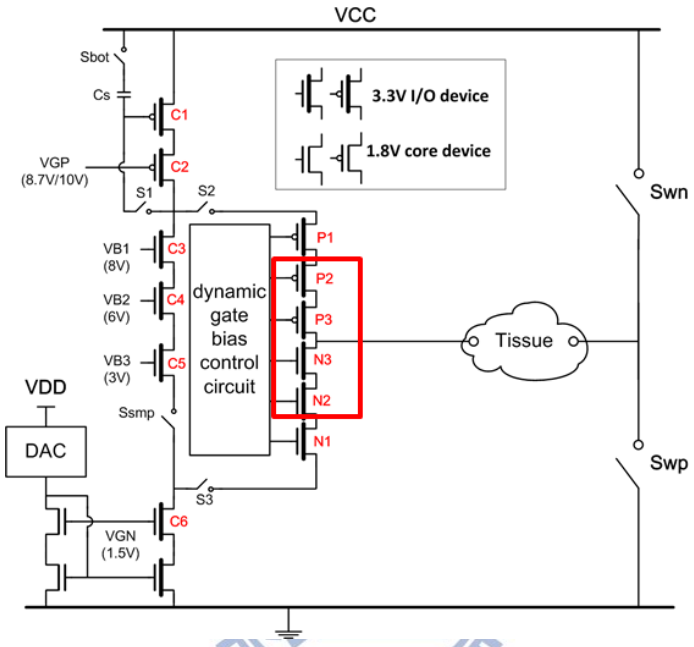


Fig. 3.29 The place that irreversible damage happened.

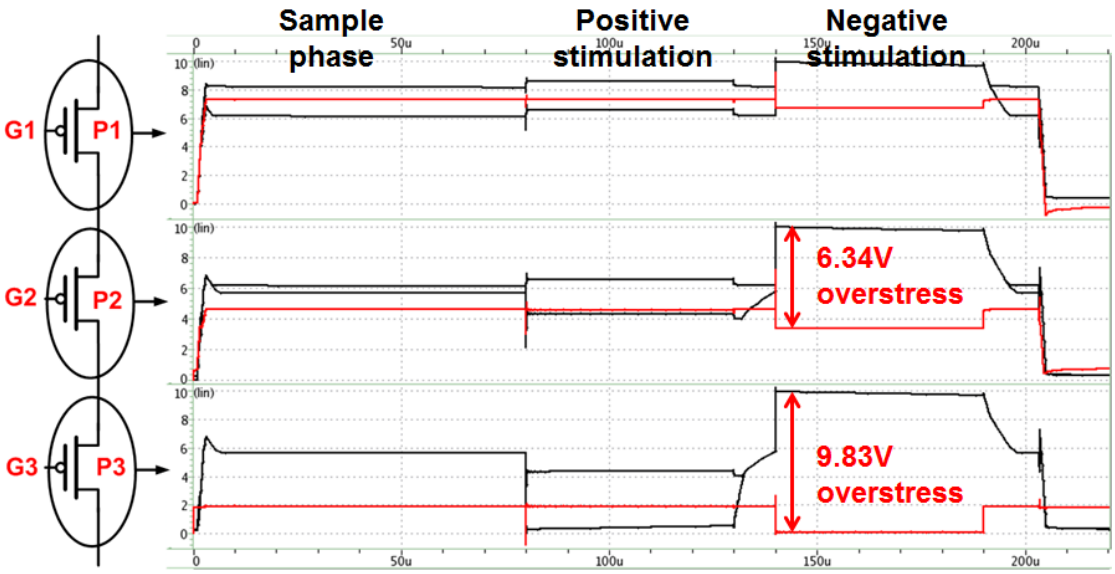


Fig. 3.30 Overstress happen when in negative stimulation.

From Fig. 3.30 we can notice that when loading resistance value is too small, the anodic node voltage will be nearly VCC 10V at negative stimulation. With improper gate bias, the high node voltage causes the overstress on the gate to source and drain. Then to confirm the damage on the stimulator, we do the failure analysis by emission microscope (EMMI). The principle is as below: Infrared emission can occur and be detected in a semiconductor device when excessive electron - hole pair recombination occurs. Failures caused by oxide breakdown, ESD damage, Latch-up, impact ionization and saturated transistors can produce excessive electron - hole pairs. By using an infrared detection tool, one can accurately detect and precisely locate such failure sites. As shown in Fig. 3.31 and Fig. 3.32. The bright dots in the EMMI photo represent the place that higher current flow through. From these EMMI photos we can confirm that there are damages on the gate oxide of the stacked MOSFETs.

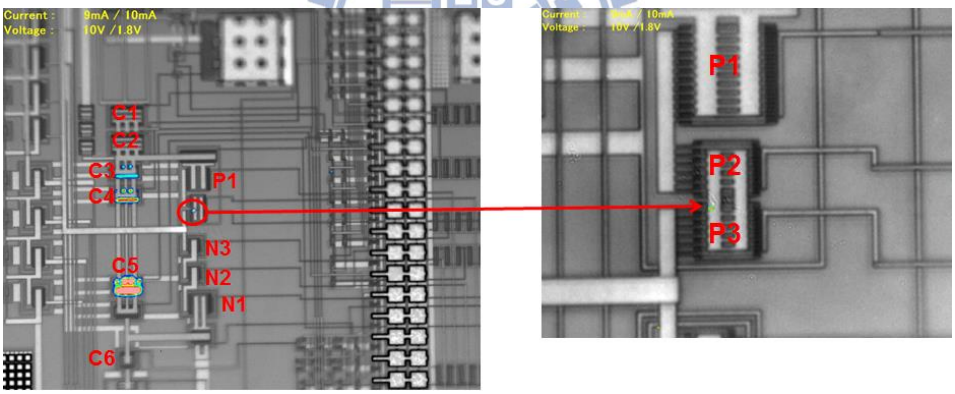


Fig. 3.31 EMMI photo of the stimulus driver operates at sampling phase.

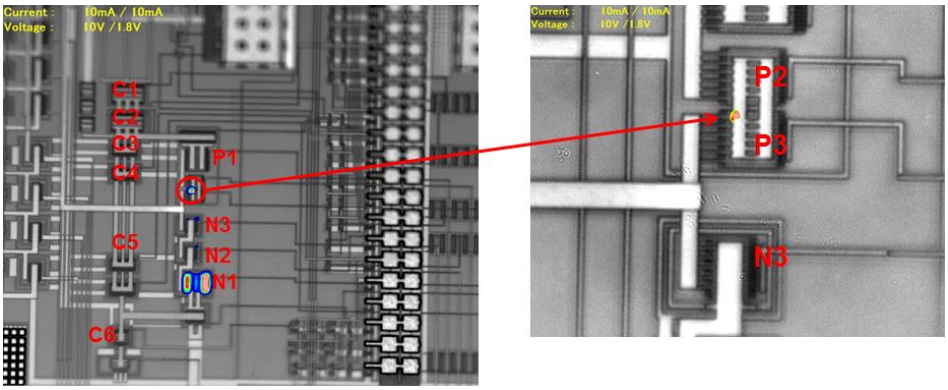


Fig. 3.32 EMMI photo of the stimulus driver operates at negative stimulation.

3.4.2 Circuit Modification and Simulation Results

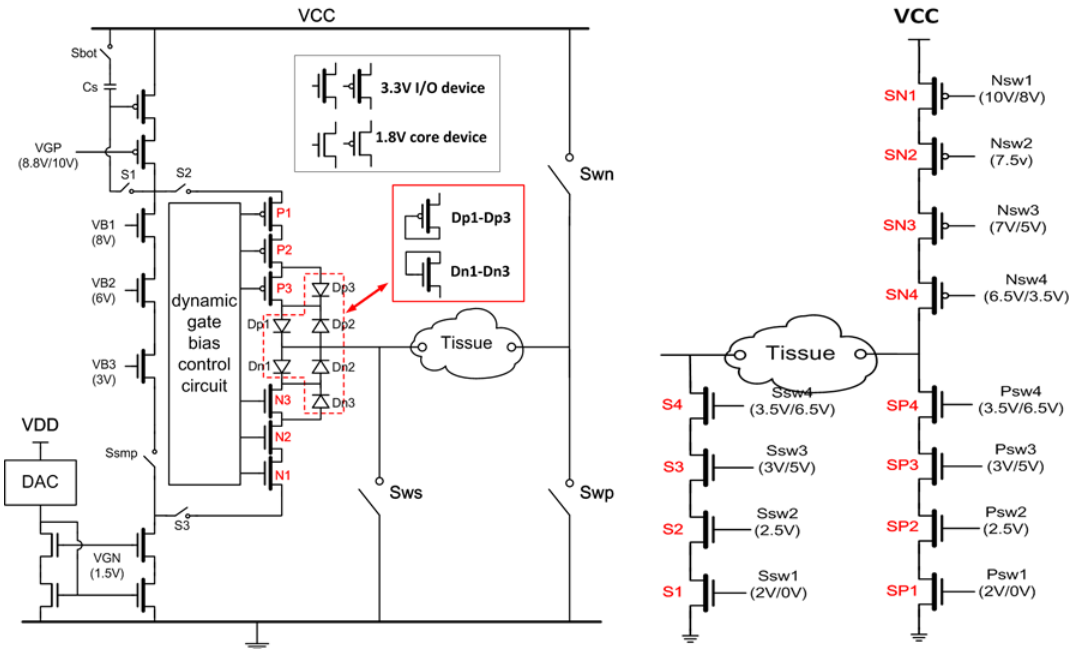


Fig. 3.33 The schematic of the modified stimulus driver and the high-voltage-tolerant switches.

To resolve the overstress problem, some modifications are applied to the stimulus driver. Fig 3.33 shows the schematic of the modified stimulus driver. The anodic node voltage ranges from 0.5V to 9V, which makes it impossible to bias the MOSFET P3 without overstress. So diode connected devices Dp1 and Dn1 are used to provide voltage drop about 2V on the stimulus path to handle with the large node voltage range. The reversed diode connected devices Dp2 and Dn2 are used to keep the anodic nodes of Dp1 and Dn2 at safe operation region. For example, if the voltage drop on tissue is 1V, then the anodic node voltage of Dp1 is about 3V when in positive stimulation. And when change to negative stimulation, the anodic node voltage of the tissue, which is also the cathodic node of Dp1, is going to be about 9V. Without reverse diode connected devices Dp2, the anodic node voltage will remain 3V because the positive stimulus path is floating, the large voltage drop will make Dp1 under overstress. With reverse diode Dp2, the anodic node of Dp1 can charge to

9V minus a threshold voltage by leakage current, which can prevent Dp1 from overstress. In addition, the diode connected devices Dp3 and Dn3 are used to clamp the drain to source voltage under safe window when loading voltage drop is too small. Furthermore, add shorting switches to short the electrodes to ground when stimulation isn't applied. By discharge residue charge to ground when standby to further enhance the safety of the stimulus driver.

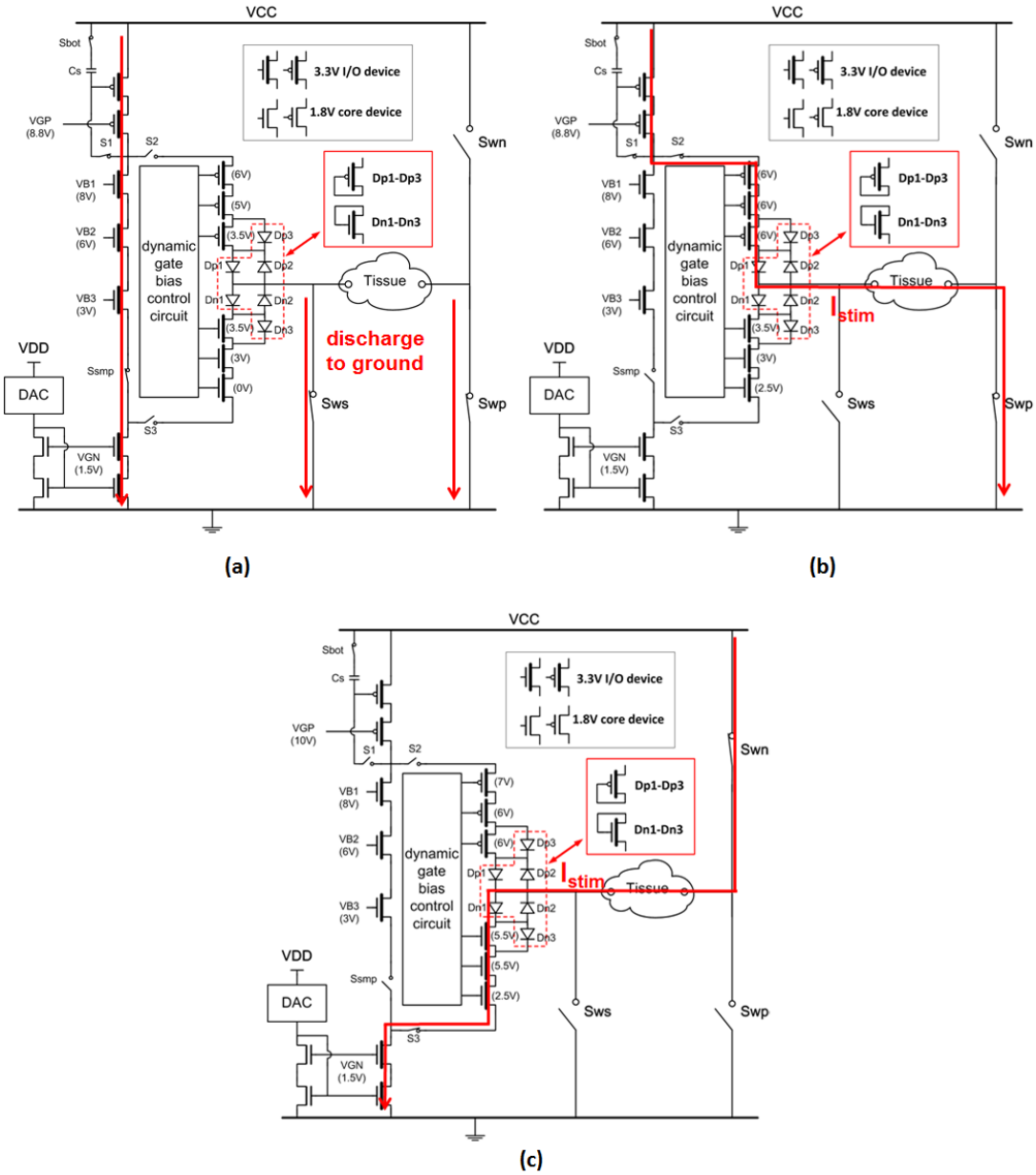
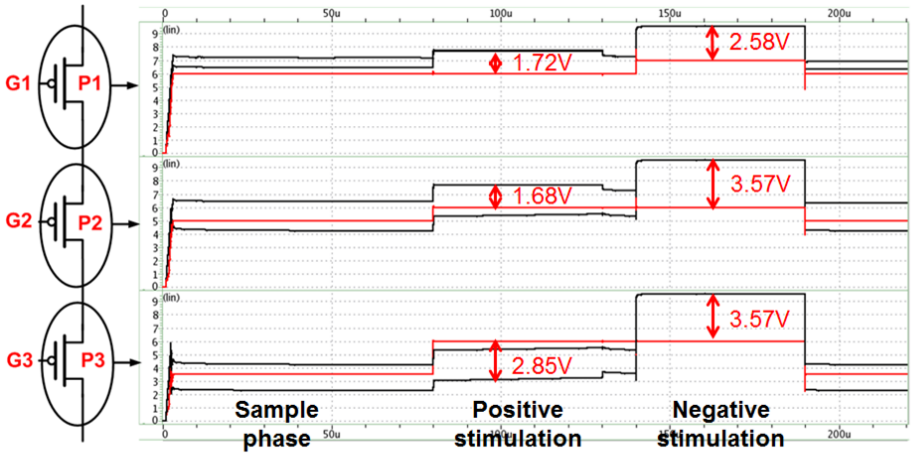
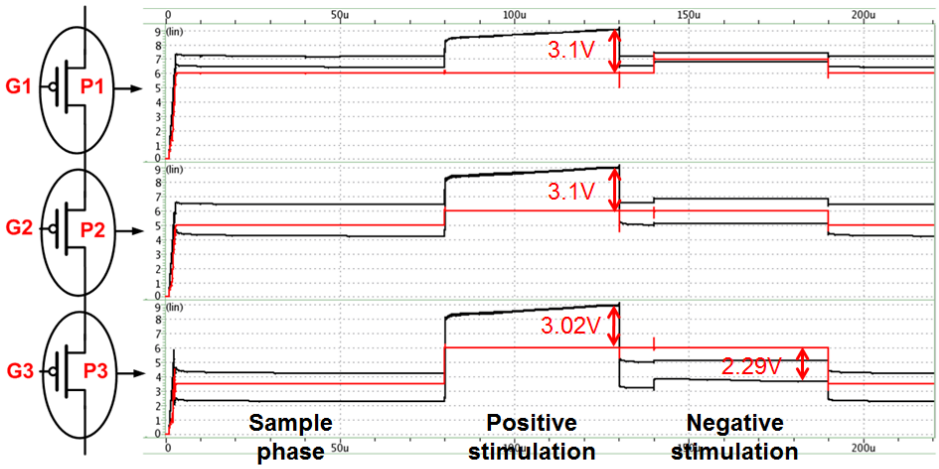


Fig. 3.34 The operation in (a) sampling phase, (b) positive stimulation, and (c) negative stimulation.

Fig. 3.34 shows the schematic of all operation phase. Then we run the HSPICE simulation to check that there is overstress or not on all operation phase or not. The following figures show all the node voltages of the stacked MOSFETs at two extreme situations. First state is loading resistance 0.5kΩ with 0.5mA stimulus current, to represent the lowest voltage drop on the loading tissue. The other state is loading resistance 3.2kΩ with 2mA stimulus current, to represent the highest voltage drop on the loading tissue. Fig. 3.35 shows all the node voltages of the stacked PMOSs under the lowest and highest loading resistance value. The highest voltage drop on gate to source and drain is about 3.57V, which is just under the safe operation region.



(a)



(b)

Fig. 3.35 The node voltages of the stacked PMOSs under the (a) lowest and (b) highest voltage drop on the loading tissue.

Fig. 3.36 shows all the node voltages of the stacked NMOSs under the lowest and highest loading resistance value. The highest voltage drop on gate to source and drain is also about 3.57V, which is just under the safe operation region.

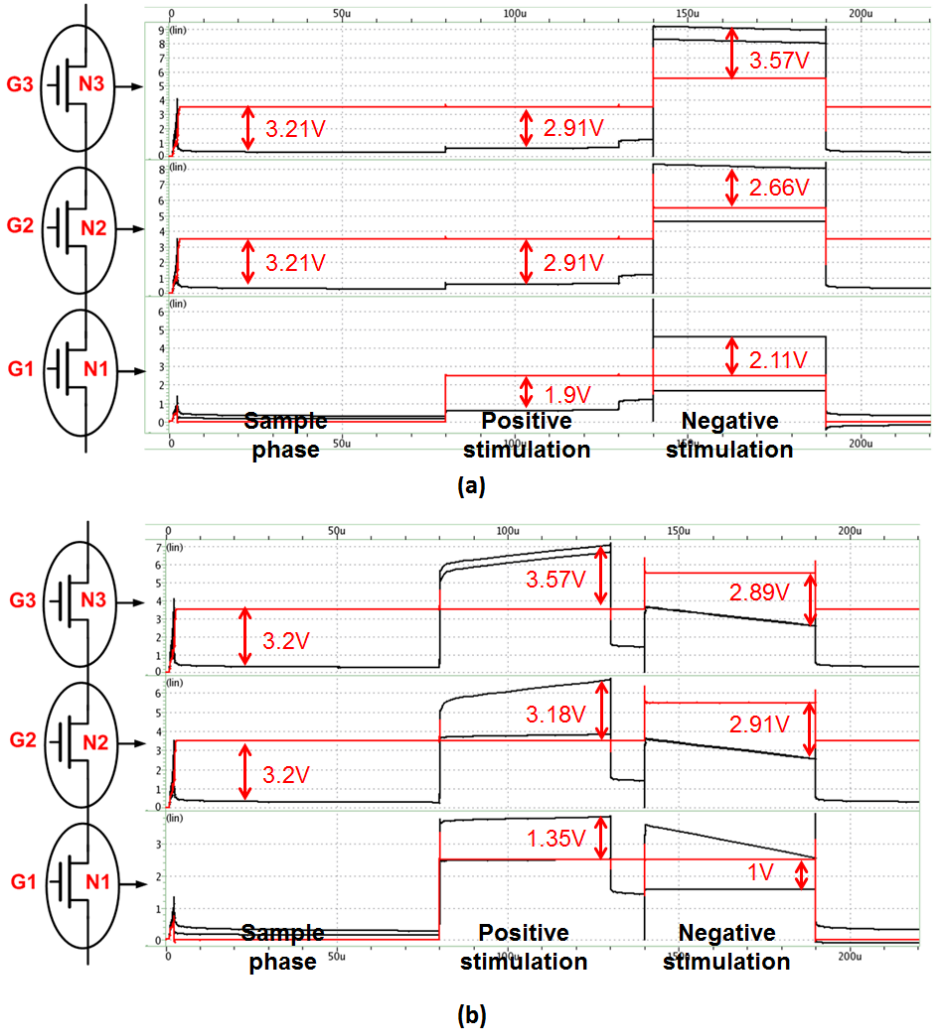


Fig. 3.36 The node voltages of the stacked NMOSs under the (a) lowest and (b) highest voltage drop on the loading tissue.

In the following figure, Fig. 3.37, we present the drain to source voltage drop on the stacked MOSFETs of the stimulus path. Simulations are done under the two extreme loading situations, and check all the operation phase to confirm there is no reliability problem. The maximum drain to source voltage drop under the lowest loading voltage drop is 3.62V, and the maximum drain to source voltage drop under

the highest loading voltage drop is 2.81V. Each of them is under the safe operation region.

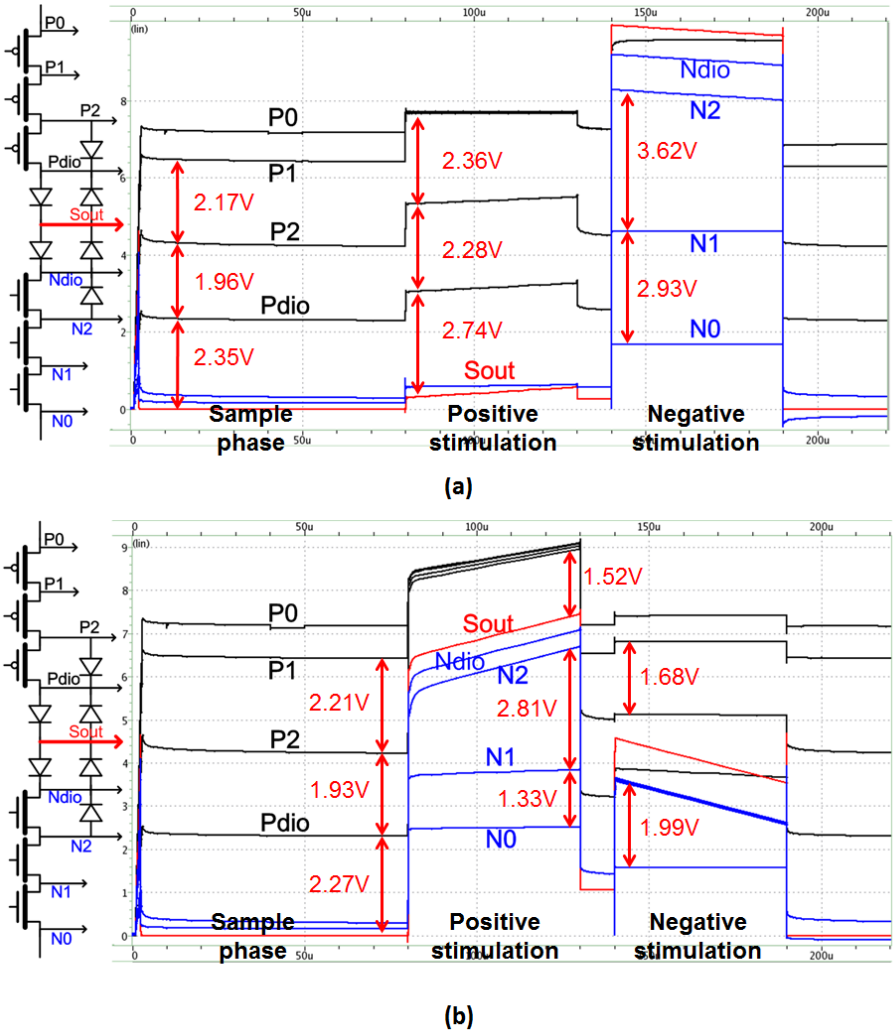


Fig. 3.37 The drain to source voltage drop on the stacked MOSFETs of the stimulus path under (a) the lowest and (b) the highest loading voltage drop.

Then check all the node voltages of the adding shorting switches. The simulation results are shown in Fig. 3.38. With the lowest loading voltage drop, the maximum tolerant gate to source and drain voltage drop is about 3.5V. And with the highest loading voltage drop, the maximum tolerant gate to source and drain voltage is 3.59V. Each of them is under the safe operation region.

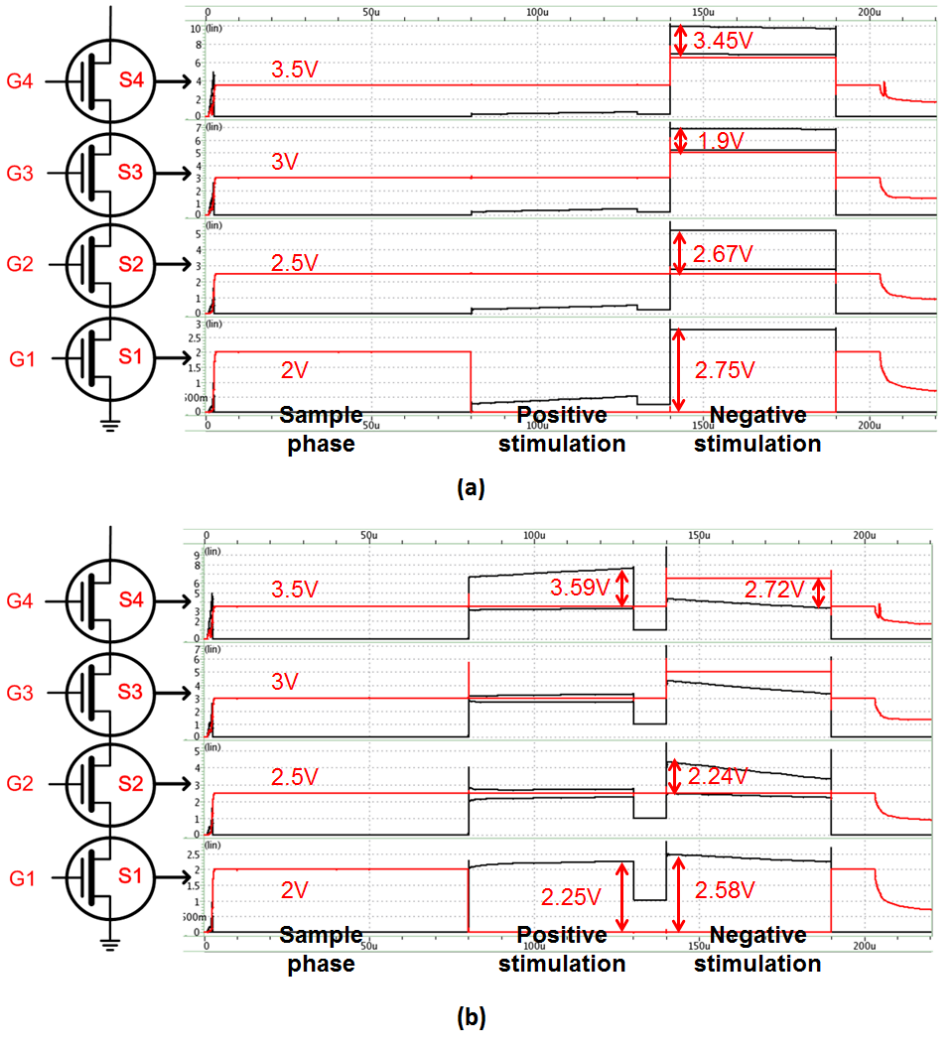


Fig. 3.38 The node voltages of the shorting switches under the (a) lowest and (b) highest voltage drop on the loading tissue.

In the following figure, Fig. 3.39, we present the drain to source voltage drop on the stacked MOSFETs of the shorting switches. Simulations are done under the two extreme loading situations, and check all the operation phase to confirm there is no reliability problem. The maximum drain to source voltage drop under the lowest loading voltage drop is 3.62V, and the maximum drain to source voltage drop under the highest loading voltage drop is 2.81V. Each of them is under the safe operation region.

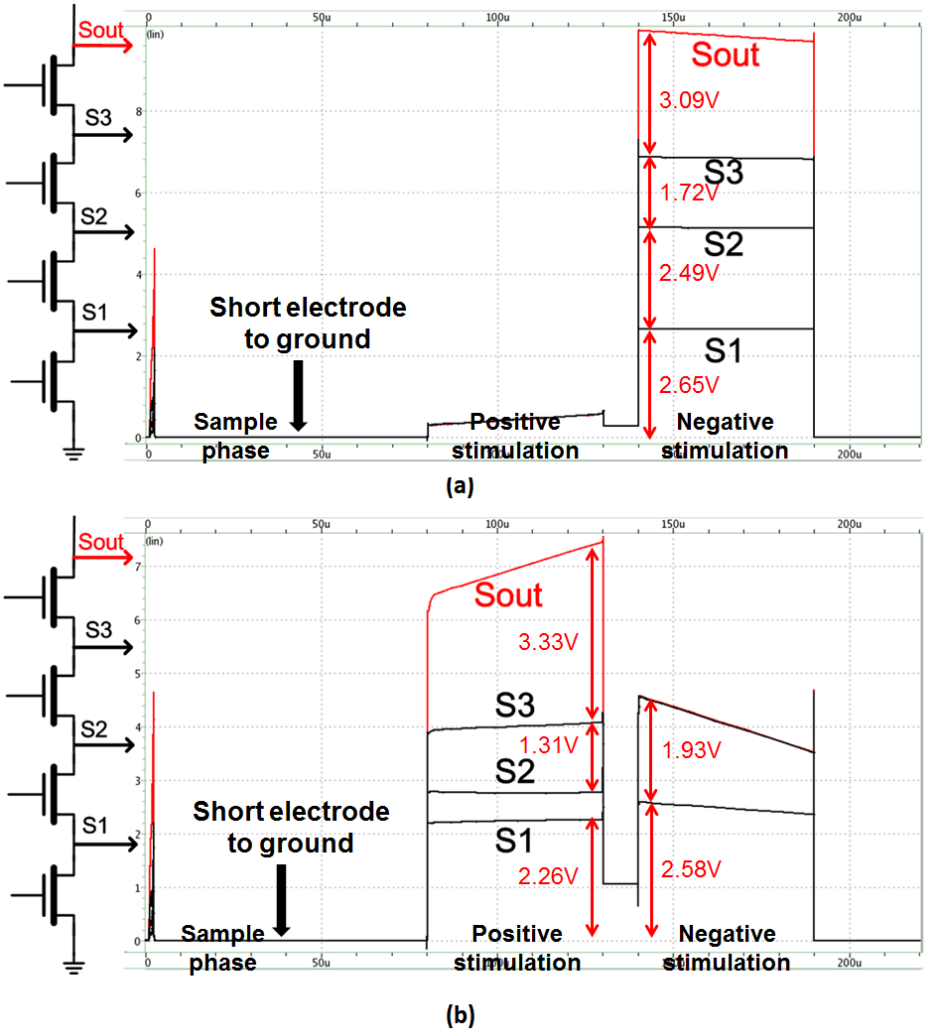


Fig. 3.39 The drain to source voltage drop on the stacked MOSFETs of the shorting switches under (a) the lowest and (b) the highest loading voltage drop.

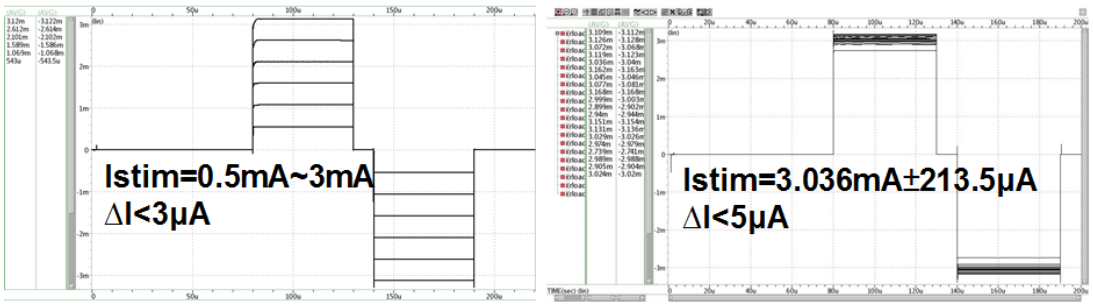


Fig. 3.40 The simulation results of (a) all scale of the stimulus current, and (b) MONTE CARLO analysis of the modified stimulus driver.

MONTE CARLO analysis had been run to verify the function of charge-balanced technique. Fig. 3.18 shows the waveform of all scale of the stimulus current and the simulation results of MONTE CARLO analysis. Despite of the 213.5μA current mismatches caused by the mismatch of the MOS size, the maximum mismatch between anodic and cathodic is under 5μA. The layout and the post-simulation of the modified stimulus driver have been complete and prepared for the next tapeout. The layout photo of the modified stimulus driver are shown in Fig. 3.41. The design will be fabricated in TSMC 0.18μm 1.8V/3.3V CMOS process.

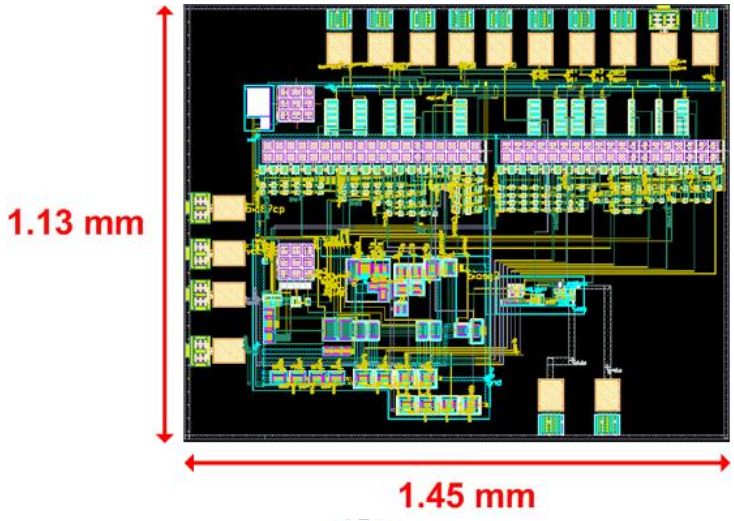


Fig. 3.41 The layout photo of the modified stimulus driver.

Table 3.2 Summary of the modified stimulus driver

	Spec.	Simulation
VDD	1.8V	1.8V
VCC	10V	10V
Stimulus current	0.5mA 1mA 1.5mA 2mA 2.5mA 3mA	0.544mA 1.068mA 1.586mA 2.102mA 2.614mA 3.122mA
Current mismatch	minimum	<0.19%
Standby power	minimum	57.7μW
Process	TSMC 0.18μm 1.8V/3.3V CMOS process	

※Current mismatch = |cathodic-anodic| / cathodic

3.5 Summary

Design of a bipolar biphasic current stimulus driver for epilepsy treatment implant with high-voltage-tolerant consideration is investigated in this chapter. The proposed design had been fabricated in TSMC 0.18μm 1.8V/3.3V CMOS process, because the maximum output voltage is as high as 10V, so dynamic bias technique and stacked MOSFETs configuration are proposed to avoid the problems of electrical overstress and gate-oxide reliability. The proposed charge-balanced biphasic stimulus driver consists of three parts: output driver, high-voltage-tolerant switches, and VCC generator. The VCC generator can work under 1mA loading current, but fail to work when loading current is larger than 1mA. Under the normal operation region, the stimulus driver can provide charge-balanced biphasic stimulus current with mismatch under 40μA. And the amplitude of the biphasic stimulus current from 0.5mA to 3mA can be adjusted by the 3-bit amplitude signal. Finally, the modified stimulus driver is proposed to resolve the defect of the older design, and its layout and post-simulation are complete for the next tapeout.

Chapter 4

Conclusions and Future Works

4.1 Conclusions

To be integrated into SoC with other sub-circuits of the epilepsy treatment implant, this work had been fabricated in TSMC 0.18μm 1.8V/3.3V CMOS process, and the total chip area is 1.13 mm × 1.55 mm. The proposed charge-balanced biphasic stimulus driver consists of three parts: output driver, high-voltage-tolerant switches, and VCC generator. The maximum output stimulus current is 3mA, with loading resistance up to 3kΩ, the operation voltage is up to 9V. So a VCC generator is needed to provide 10V power supply for the stimulus driver. But the tolerant voltage of the transistor in this process is 3.3 V, so stacked MOS configuration and dynamic bias techniques are used to prevent the stimulator from the issues of gate-oxide reliability and electrical overstress.

And for safe stimulation, the residue charge on the tissue needs to be under 100mV. The dynamic current mirror had been implemented to the stimulus driver to achieve this specification, but the function still needs to be verified. Under the normal operation region, the stimulus driver can provide charge-balanced biphasic stimulus current with mismatch under 40μA. But when loading voltage drop is too small, some reliability problems occur and really do damage to the devices.

The modified stimulus driver had been proposed to resolve these reliability problems. The layout and the post-simulation had been complete and prepared for the next tapeout.

4.2 Future Works

4.2.1 Self-biasing High Voltage Output Driver

A self-biasing cascode topology, as shown in Fig. 4.1, allows the line driver to operate at high supply voltage. the gates of the cascode transistors are set by a resistive ladder network. The capacitors parallel with the resistors counteract the overshoot during transients on the gates of the cascade devices due to their parasitic gate-drain capacitance. Without using excess dynamic bias circuit, the self-biasing high-voltage output driver can save a lot of power.

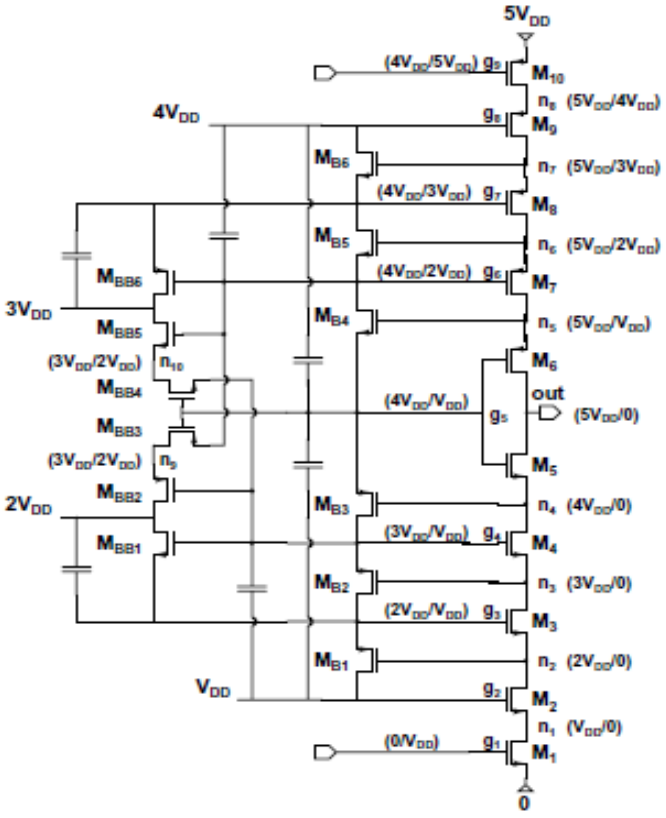


Fig. 4.1 Schematic of the self-biasing high voltage buffer [33].

4.2.2 Failure Checking

Safety issue is the most important for an implant device. The proposed stimulus driver can provide charged-balanced stimulus current only when under normal operation condition. So the failure checking system is needed to check that it is under normal operation condition. As shown in Fig. 4.2. If the electrode voltage is out of operation region, the sensing circuit output a control signal to shut down the stimulation. Adding the sensing circuit to make sure that the stimulus driver provides safe stimulation.

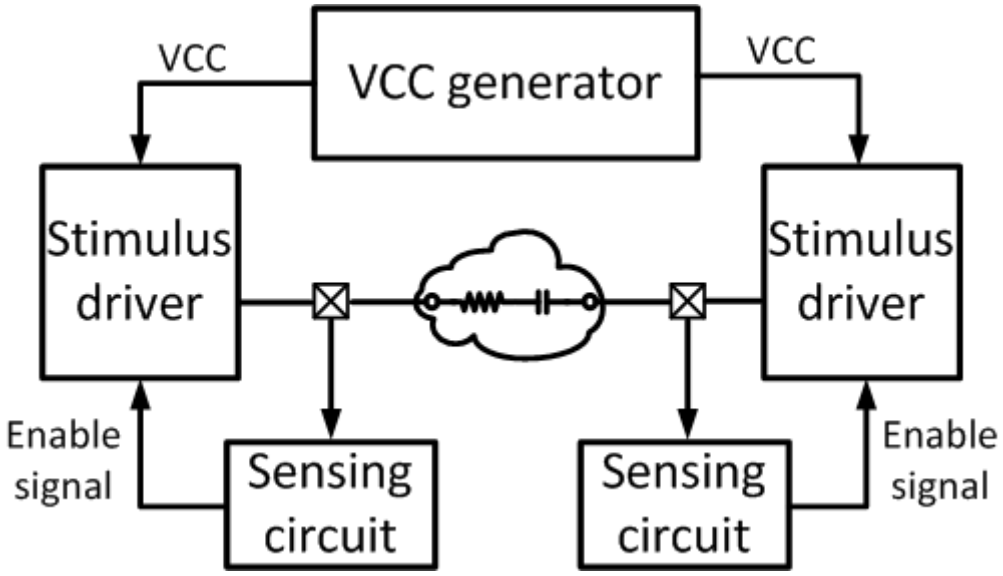


Fig. 4.2 Architecture of failure checking system.

4.2.3 Possible solution for high-voltage generator

The failure of the high-voltage generator is caused by serious switching noise, which is result from the high clock frequency and large simultaneous current of the tapped buffer. To solve the problem, we try to use another structure of high-voltage generator as shown in Fig. 4.3. First we use a rectifier and a voltage doubler to generate DC voltage about 4V, and pass through a regulator to generate a 3.3V power supply. Use the 3.3V power supply as the input of charge pump, the number of

pumping stages can be reduced. As the number of pumping stages reduced, the total amount of pumping capacitors is reduced too. With lower pumping capacitor, the size of tapped buffer can be reduced, and so as to the pumping frequency. If both of them are reduced, the switching noise can also be reduced and the power efficiency of the high-voltage generator can be improved.

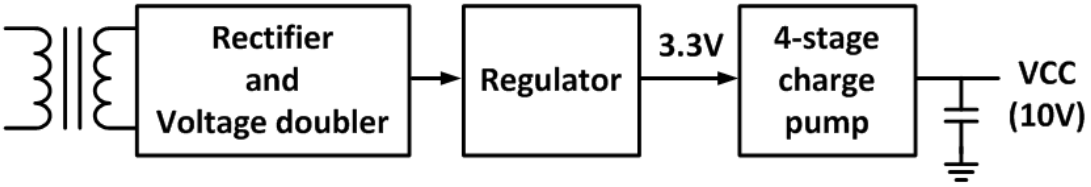


Fig. 4.3 Architecture of the new proposed high-voltage generator with lower pumping stages.

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