國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

運用在人工耳蝸的雙向雙極性

電壓刺激器設計

Design of a Bipolar Biphasic Voltage Stimulator

for Cochlear Implant

in the 0.18μm 1.8V/3.3V CMOS Process

研 究 生：林冠宇　　(Kuan-Yu Lin)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國一〇三年二月

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碩士論文

A Thesis
Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master of Science
in
Electronics Engineering
February 2014
Hsinchu, Taiwan

中華民國一〇三年二月

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摘要

近年來，由於生醫科學與半導體的快速發展，許多植入到人體內的生醫相關的系統單晶片被提出。其中人工耳蝸也是一種植入式生醫相關的系統單晶片，它是用來幫助耳聾的人恢復失去的聽力。而在我們的人工耳蝸計畫中負責生醫相關研究的團隊研發出了一種新型的電極，這種電極必須要使用定電壓的刺激方法才能夠幫助耳聾的人恢復聽覺，所以根據這樣的需求，一個能夠輸出定電壓的刺激器設計被提出。

根據人工耳蝸計畫中的生醫團隊的研究，此電刺激器必須要能夠輸出雙極性的刺激電壓，並且此刺激電壓的大小與刺激時間都必須要能夠根據需求來做調整。

發展已久的互補式金屬氧化物半導體製程非常適合用來實現植入式生醫元件，所以我們的植入式耳蝸會實現在 0.18 微米的互補式金屬氧化物半導體製程，此製程提供了一點八伏特與三點三伏特的元件。但刺激器的最高輸出電壓會高達七伏特，為了避免遭遇到閘極可靠度與電性過壓的問題，在這裡採用了堆疊電晶體與動態偏壓的技巧來避免上述的問題。根據本人工耳蝸計畫中的生醫團隊的研究，為了要使耳聾的病人有足夠的語音理解度，刺激器要能夠同時在耳蝸上刺激四個不同的位置，所以我們的刺激器有四通道的輸出。

植入式人工耳蝸只能透過外部無線傳輸電力到內部，而外部無線傳輸給內部的電壓為一點八伏特。而刺激器的最高輸出電壓為七伏特，所以此刺激器還包含了一個高電壓產生器，它可以將一點八伏特的電壓轉成八點四伏特的電壓給刺激器作使用。

Design of a Bipolar Biphasic Voltage Stimulator for Cochlear Implant in 0.18μm 1.8V/3.3V CMOS Process

Student: Kuan-Yu Lin **Advisor: Prof. Ming-Dou Ker**

Department of Electronics Engineering & Institute of Electronics
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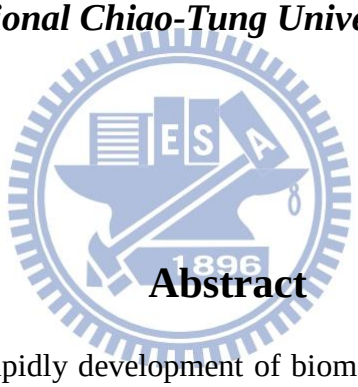

Abstract

Nowadays, due to the rapidly development of biomedical science and electronics, many System-on-Chips for biomedical application had been proposed to implant into human body. Cochlear implant is also one kind of medical application for the profound deafness. New type electrodes for cochlear implant had been proposed by our biomedical group, and these electrodes have to be driven by voltage. Thus, a stimulator can deliver voltage pulses to stimulate the auditory nerve in the cochlea is proposed.

According the research of our biomedical group, the stimulator should be capable of providing biphasic voltage pulses with adjustable amplitudes and adjustable pulse widths. The well-developed CMOS processes had been attractive to realize implantable device for biomedical application, so the cochlear implant is implemented in the 0.18-um 1.8-V/3.3-V CMOS process. For the purpose of integration with other circuit

blocks into a system-on-chip (SoC), the stimulator should also be implemented in the 0.18-um 1.8-V/3.3-V CMOS process. But the maximum output voltage of the stimulator can be as high as 7 V, so the dynamic bias technique and stacked MOS configuration are used to implement this stimulator in the low-voltage CMOS process, without causing the issues of electrical overstress and gate-oxide reliability during circuit operation. According the research of our biomedical group, to help deafness to have sufficient speech intelligibility, the stimulator should be able to deliver stimulus voltage to four different positions on the cochlea, so our stimulator has four output channels.

The cochlear implant can only be powered by wirelessly power transmission, and the power supplied by wirelessly power transmission is V_{DD} of 1.8 V. The maximum output voltage of the stimulator is 7 V, so the proposed stimulator also includes a positive high voltage generator, which can pumped V_{DD} (1.8 V) to V_{DDH} (8.4 V). Thus, the stimulator only needs one supply voltage of 1.8 V

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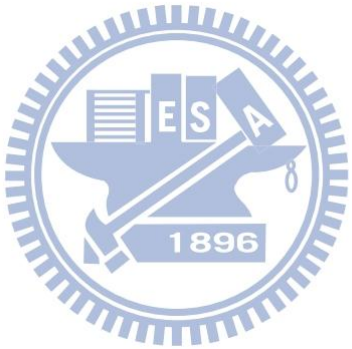

Acknowledgment

在這兩年中，很感謝柯明道老師的指導，讓我不僅僅學到如何做研究，還有處理事情的態度。也要感謝所有曾經在課堂上教授過我知識的教授，交大的教授都非常認真，使我在各堂課上都能夠獲益良多，打好基礎。使我能夠在這些基礎上順利完成我的研究。

感謝實驗室的同學們，曾建豪、范美蓮、張品歆、湯凱能，在學習的過程中一起成長與進步。還有要感謝實驗室的學長姐，林群祐學長、陸亭州學長、邱柏硯學長、黃雅君學姐、葉致廷學長、艾菲學長、竹立煒學長、蔡惠雯學姐、林倍如學姐、戴家岑學長、顧珊綺學姐、黃俊瑋學長、黃楀晴學姐，還有學弟們，黃義傑、廖顯峰、劉睿閎、楊子毅、鄭瑩學。還有要感謝幫忙我實驗的李家鳳醫師、周元昉教授，宋昱霖博士。最後要感謝父母對我從小到大無私地教養栽培、經濟支持。

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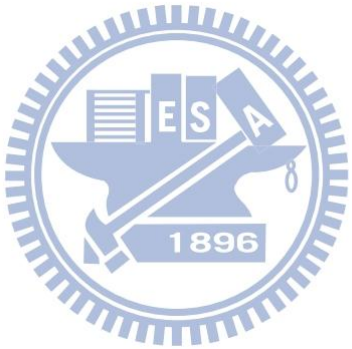

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Chapter 1
Introduction

1.1 Motivation

Because of the rapidly development of biomedical science and electronics, bioelectronics is more and more popular. Several applications such as biomedical implant device and resonance imaging are proposed, and they are helpful for patients and doctors in the surgery. According to the research of the neuroscience, some lost physical functions of human body can be restored by delivering electrical charge to corresponding nerve, this technique is called as neuromuscular electrical stimulation or functional electrical stimulation (FES) [1]. Due to the highly development of advanced integrated circuit process, complex systems can be integrated into a single chip. Combined FES and advanced integrated circuit process, many implant devices for medical application are proposed.

The cochlear implant is also one kind of implant device for medical application, and it is also the most successful commercial implant device. The cochlear implant has not only restored useful hearing of more than 120 000 deaf people, but also becomes a multibillion-dollar industry [2]. Hearing is initiated when oscillation in air pressure are converted into fluid pressure that travel down the cochlear duct and induce vibrations in the basilar and finally generate action potential on the auditory nerve in the cochlea [3]. The cause leads people to be deaf is that the medium between the sound and action potential generation on the auditory nerve of the cochlea is damaged, so the cochlear implant is based on the above theorem. When the sound is picked by the cochlear implant, the cochlear implant can deliver stimulus voltage or

stimulus current to the auditory nerve in the cochlea according to the amplitude and frequency of the picked sound to restore the hearing of deaf people. The electrodes of the traditional cochlear implant are pierced through the cochlea into the auditory nerve, and stimulus current are delivered to the auditory nerve through the implanted electrodes, but this way can induce meningitis and losing the residual hearing. According to the research of our biomedical group, two electrodes are pasted on the two sides of the bone of the cochlea, and biphasic stimulus voltage are delivered on the electrodes to form electrical field to stimulate the auditory nerve. By the above way, meningitis and losing the residual hearing can be avoided. According to the request of our biomedical group, a stimulator with voltage mode for cochlear implant is proposed in this thesis.

There are several challenges and issues should be considered in designing the stimulator for cochlear implant. Firstly, the impedance of the cochlea with implanted electrodes should be investigated, and then the architecture of the circuit can be decided to optimize the circuit performance. According to the request of our biomedical group for cochlear implant, the maximum voltage for stimulation is as high as 7 V. For SoC integration, the circuit with high operation voltage realized in the low-voltage process has the issues of gate-oxide overstress and hot-carrier effect [4]. Also the voltage level and pulse width of the stimulus voltage should be adjustable according to the frequency and amplitude of the picked sound. Furthermore the issue of power consumption should be taken into consideration, because the power through wireless is limited. In this thesis, a stimulator with four output channels for cochlear implant is proposed, and the issues of gate-oxide overstress, hot-carrier effect, and power consumption have been considered.

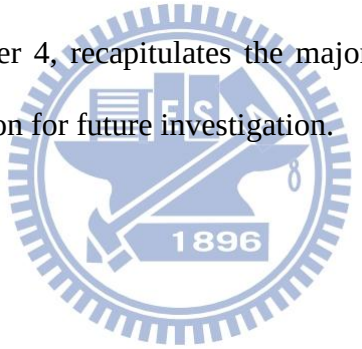
1.2 Thesis Organization

This first chapter, chapter 1 includes the motivation of this work and the thesis organization.

The chapter 2 of this thesis introduces some background knowledge of implant device, cochlear implant, and design considerations of implantable stimulator.

In the chapter 3, the design of the proposed stimulator and the impedance analysis will be introduced. Then the design of the high-voltage-tolerant bipolar biphasic stimulator with an on-chip high voltage generator for cochlear implant is proposed, which had been fabricated in TSMC 0.18-μm 1.8-V/3.3-V CMOS process for SoC integration.

The last chapter, chapter 4, recapitulates the major consideration of this thesis and concludes with suggestion for future investigation.



Chapter 2

Background of Implant Device, Cochlear Implant, and Design of Implantable Stimulator

2.1 Introduction of Functional Electrical Stimulation and Implant Device for Biomedical Application

2.1.1 Introduction of Functional Electrical Stimulation

The theorem of functional electrical stimulation (FES) is that some neurologically impaired individuals can be restored or replaced by providing electrical pulse to excite tissue or neurons. The stimulation electrodes can create a localized electrical field at neurons that are near the stimulating electrodes, and the cell of these neurons can be depolarized. If the depolarization reaches a critical threshold, then an action potential that propagates in both directions away from the site of stimulation can be produced by an influx of sodium ions from the extracellular space to the intracellular space. Finally, some lost function can be replaced or restored by generating an action potential on corresponding nerve [1].

Neuromuscular tissue is activated by electrical charge requires at least two electrodes to produce a current flow, and the waveform of electrical stimulation pulse is characterized by three parameters: amplitude, pulse width, and pulse frequency. To different position of neurons and different human bodies, the optimized parameters of amplitude, pulse width, and pulse frequency are different, so to achieve a desired function, FES system are usually designed to be worn by the user. Stimulus waveforms are generally either biphasic or monophasic in shape. A monophasic can

induce DC charge accumulation on the neuron, and the neuron can be injured by chronic DC charge accumulation. Thus, most FES systems adopt biphasic stimulus waveforms, the secondary pulse is used to balance the electrical charge produced by the first pulse, so the potential damaging electrochemical process can be avoided [1].

Today, neuroprostheses for restoring visual, hand function, ambulation, bladder and bowel control, and respiration are approved by food and drug administration (FDA). Numerous neuroprostheses for different kind of applications have reached the clinical testing stage of development. Some neuroprostheses have already been progressed to commercialization such as restoring hand function, visual, bladder andbowel control, and respiration. The experimental and commercial neuroprostheses such as the upper extremity neuroprosthesis, shown in Fig. 2.1 [1], and epiretinal prosthesis, shown in Fig. 2.2 [5].

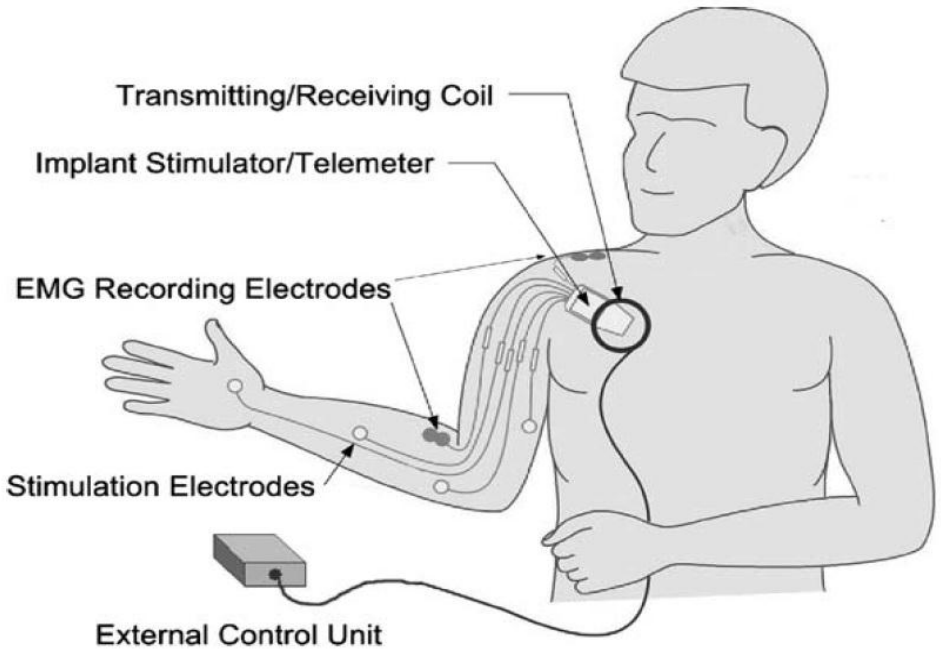


Fig. 2.1. Diagram of the 12-channel implanted upper extremity neuroprosthesis with myoelectric control capability [1].

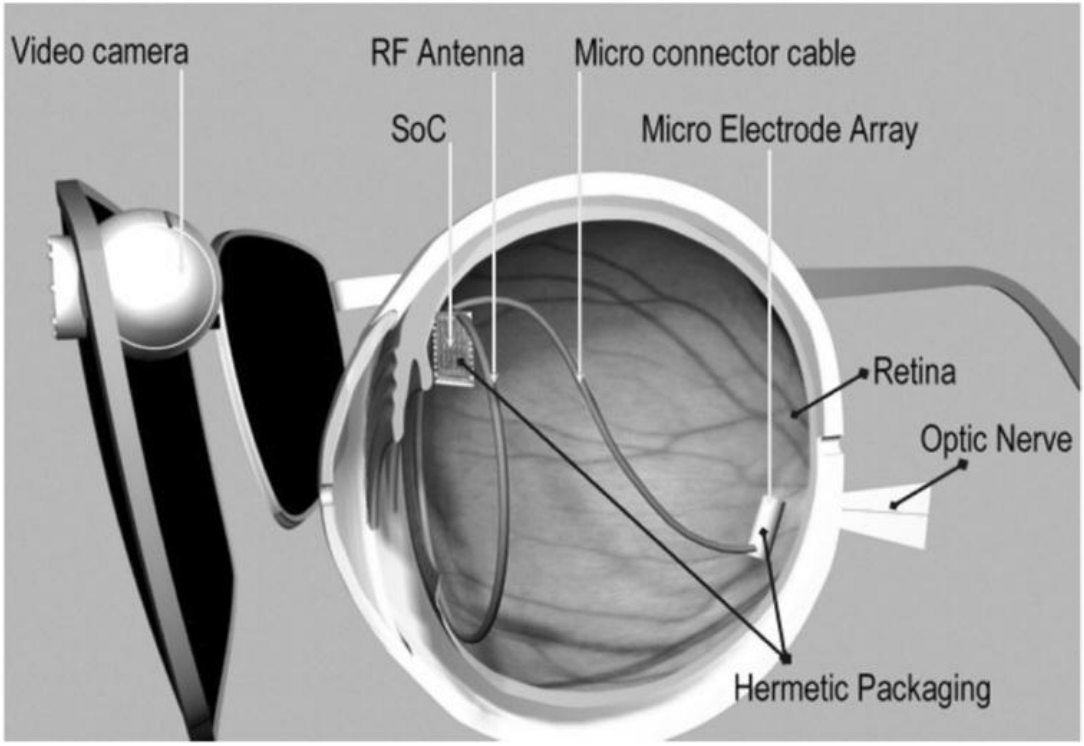


Fig. 2.2 Diagram of the 256-channel epiretinal prosthesis [5].

2.1.2 Implant Device for Biomedical Application

According to the discussion in previous section, some lost functions of human body can be restored by generating an action potential on nerves. Due to the rapidly development of the semiconductor process, complex systems and many circuit blocks can be realized in a single chip with small size. Base on the research of neuroscience and the development of the semiconductor process, systems for medical application can be integrated in a single chip with small size, and electrodes are implanted at the nerves of human body, then the chip can deliver electrical voltage or current to stimulate nerves for restoring lost function of human bodies.

In recent years, many system-on-chips (SoC) for medical application, such as retinal prosthesis [5]-[6], epileptic seizure controller [7]-[9], cardiac pacemaker [10]-[11], and vestibular prosthesis [12], had been proposed to implant into human

body. Usually systems for medical application include sensing part and output part, and according to the application, they can be divided into two types. One type is fully implanted such as epileptic seizure controller, shown in Fig. 2.3[13], and the architecture of the epileptic seizure controller is shown in Fig. 2.4 [8]. Because the occurrence of epileptic seizures is at the deep brain, so sensing part and output part are implemented in one chip, and sensing electrodes and stimulating electrodes are placed at the deep brain, shown in Fig. 2.5 [14]. Filters and analog-to-digit converter (ADC) convert voltage on the sensing electrodes to digit signals, and these digit signals are sent to digit signal processing (DSP), when DSP detects the epileptic seizures, then the stimulators will deliver stimulus current to nerves at the deep brain through stimulating electrodes for controlling epileptic seizures. Because the chip is implanted in the deep brain, thus power of implant device is wirelessly transmitted from outside. Another application is that the system is divided to external part and internal part, such as epiretinal prostheses, shown in Fig. 2.6 [15], and the architecture of epiretinal prostheses is shown in Fig. 2.7 [6]. The visual generation is at outside of the human body, so the sensing circuit is at external part. When a camera receives the image message, ADC will convert this image message to digit signals, and theses digit signals are processed and decoded by DSP, and they are wirelessly transmitted to internal part. When the internal part receives theses encoded digit signals, they will be decoded, and stimulator deliver stimulus current to stimulate visual nerves according to these decoded digit signal. Similarly, internal part of epiretinal prosthesis is inside the eyes, so the power is wireless transmitted form the external part.

Because the power of the internal part is wirelessly transmitted from external part, so power consumption is an important consideration when designing internal part. The relationship between the amplitude, frequency, and duration of stimulus voltage or stimulus current are a tradeoff. If duration is longer, then the needed

amplitude can be smaller; if duration is shorter, then the needed amplitude can be larger. So the best parameters of stimulus voltage or current are according to the research and experiment results of the biomedical group.

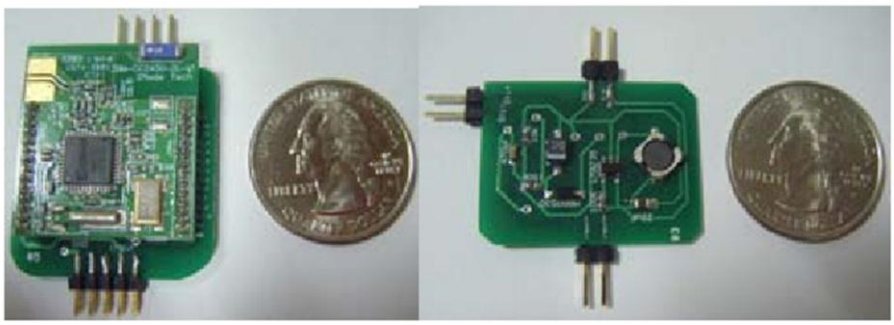


Fig. 2.3. The closed-loop epileptic seizure monitor and controller [13].

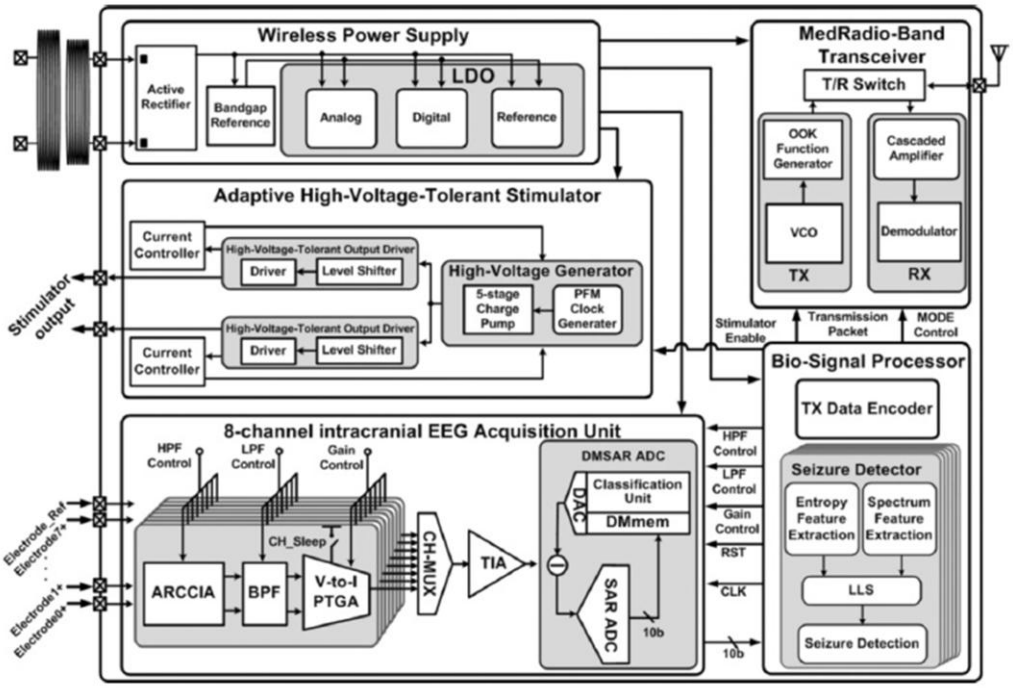


Fig. 2.4. Architecture of a fully 8-channel closed-loop epileptic seizure controller [8].

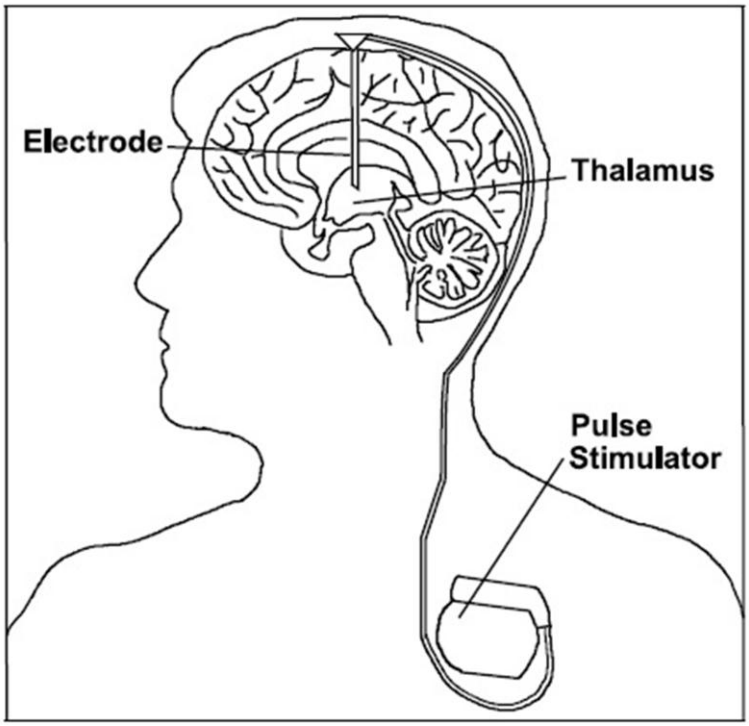


Fig. 2.5. Deep brain stimulation [14].

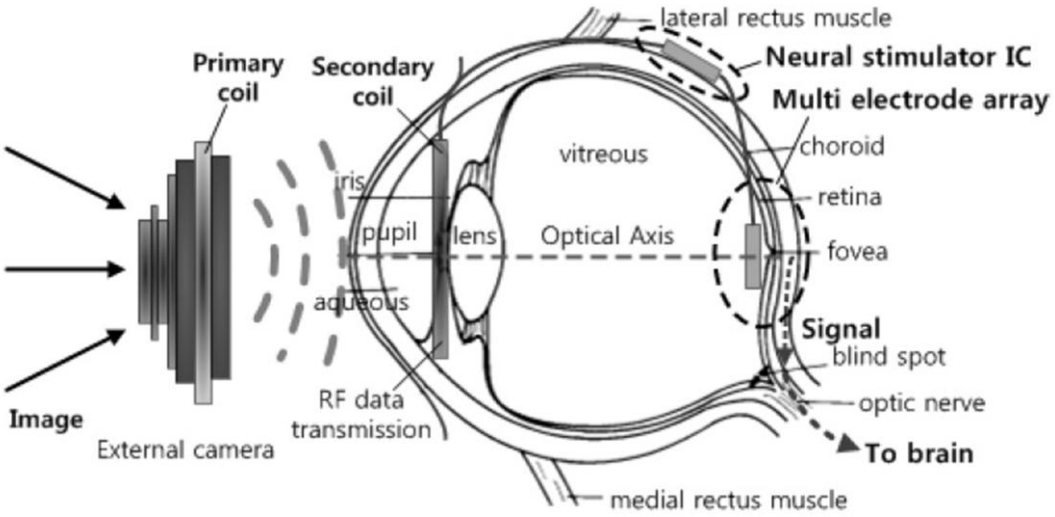


Fig. 2.6. Concept of epiretinal prostheses [15].

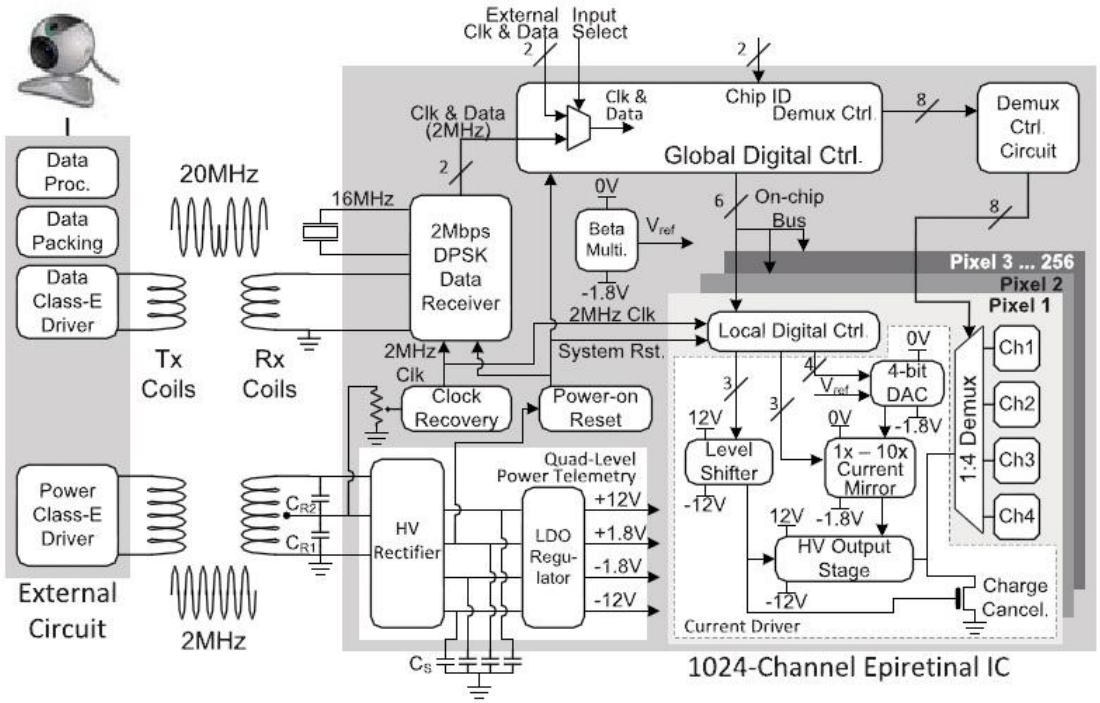


Fig. 2.7. Architecture of a 1024-channel epiretinal prostheses [8].

2.2 Introduction and Design Consideration of Cochlear Implant

Hearing is initiated when sound waves travels through air reach the tympanic membrane via the ear canal, sound waves can cause oscillations in air pressure, so the tympanic membrane can be vibrated by sound waves, and finally causing vibrations that move the three small bones of the middle ear [3], [16] This action produces a piston-like movement of the stapes, the third bone in the chain, and the footplate of the stapes is attached to a flexible membrane in the bony shell of the cochlea called the oval window [16]. Inward and outward movements of this membrane induce pressure oscillations in the cochlear fluids, which travel down the cochlear duct and induce vibrations in the basilar membrane [3], [16]. Motion of the basilar membrane is sensed by the sensory hair cells in the cochlea, when the basilar membrane moves at the location of a hair cell, such deflections in one direction increase the release of chemical transmitter substance at the base of hair cells [16]. The increases in chemical transmitter substance at the bases of the hair cells increase discharge activity in the immediately adjacent auditory neurons. Changes in neural activity thus reflect events at the basilar membrane [16]. These changes are transmitted to the brain via the auditory nerve, so the auditory sensation at the level of the brain cortex can be induced [3], [17]. The steps described previously are shown in Fig. 2.8(a) [16].

The hair cells are fragile structures compared to the other structures in the cochlea, and the hair cells are subjected to a wide variety of insults, including but not limited to genetic defects, infectious diseases (e.g., meningitis and rubella), overexposure to loud sounds, certain drugs (e.g., kanamycin, streptomycin, and cisplatin), and aging [16]. Compared to normal people, the hair cells of the cochlea of deafness are largely or completely absent, which serves the connection between the peripheral and central auditory systems [16]. The anatomical situation of the deafened

cochlea is shown in Fig. 2.8(b), it is obvious that compared to Fig. 2.8(a), the hair cells are absent [16].

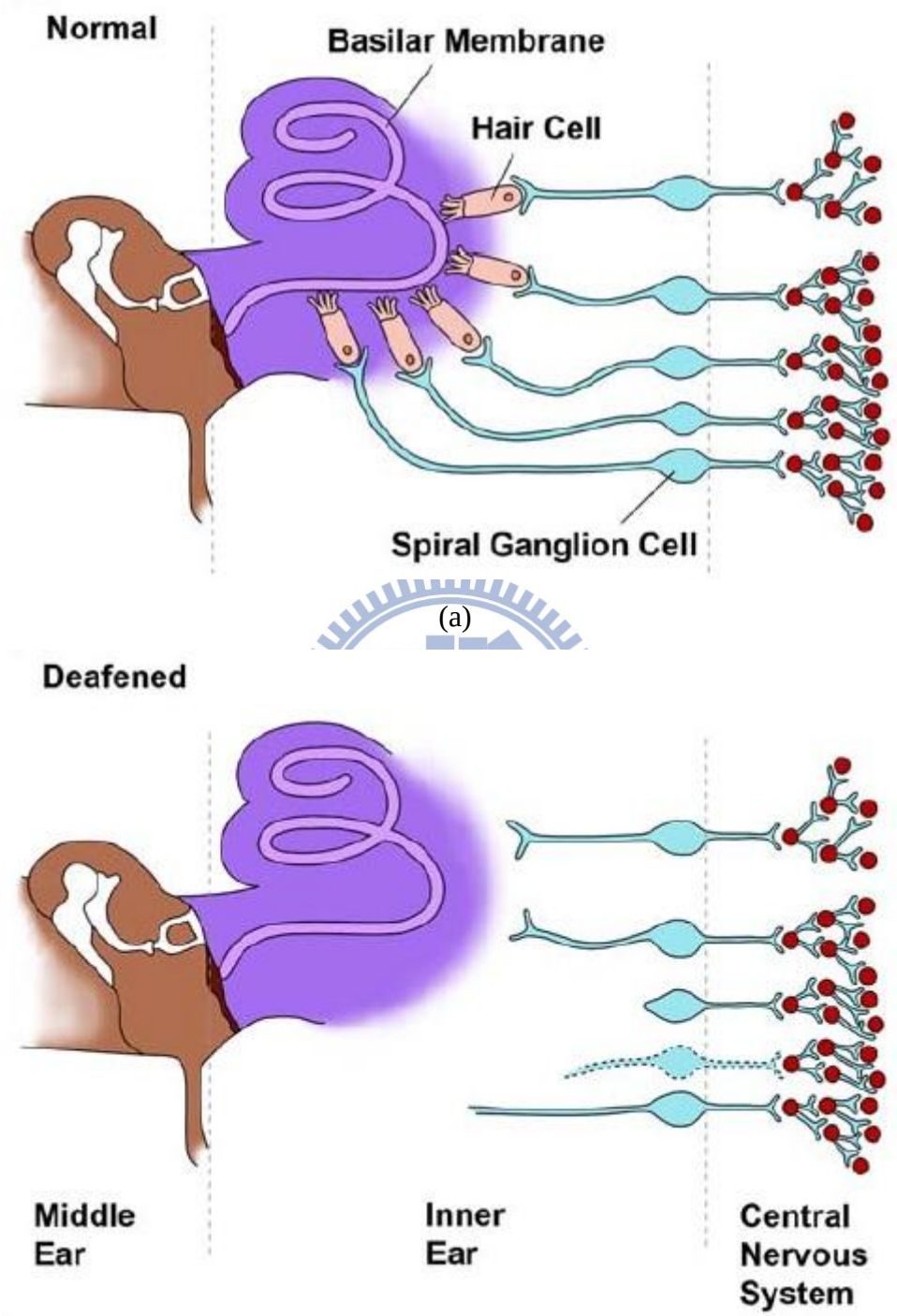


Fig. 2.8. Anatomical structures in (a) normal and (b) deafened ears. Note absence of sensory hair cells in (totally) deafened ear [16].

According to the pervious discussion, usually people are deaf because of the absence of the hair cells, and the auditory nerve are usually undamaged. Thus, the auditory sensation at the level of the brain cortex can be induce by generating action potentials on surviving nerves in the cochlea [17]-[18]. Traditionally, array of intracochlear electrodes is thin, long, and bendable [2], [19], as shown in Fig. 2.9 [2]. Array of intracochlear electrodes is inserted through a drilled opening made by the surgeon in the bony shell of the cochlea overlying the scala tympani and close to the base of the cochlea, so the auditory nerve can be direct stimulated by currents delivered through implanted electrodes placed in the scala tympani. The illustration of array of intracochlear electrodes placed in the scala tympani is shown in Fig. 2.10 [16]. The depth of insertion is limited by the decreasing lumen of the scala tympani from base to apex, the curvature if the cochlear spiral, and an uneven and unsmooth lumen [16].

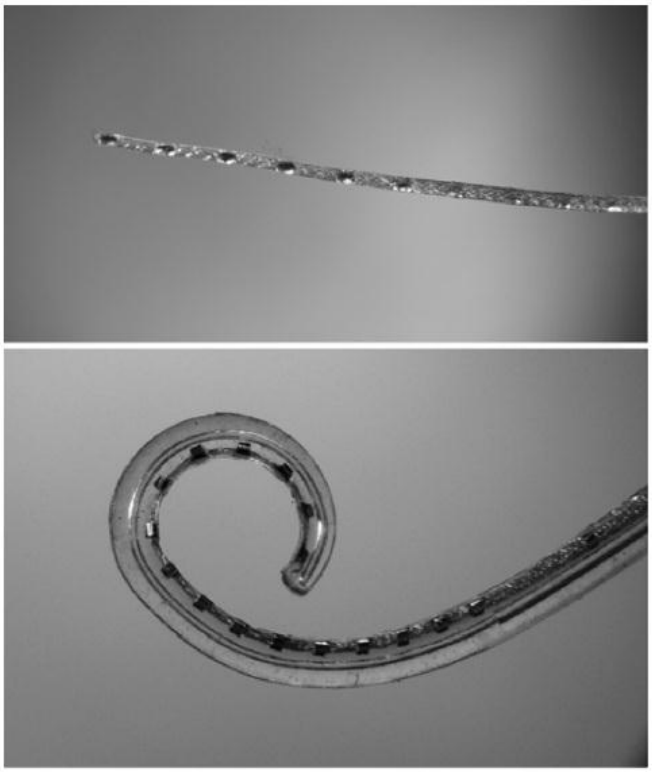


Fig. 2.9. The intracochlear electrode, it is obvious that the electrode is bendable [2].

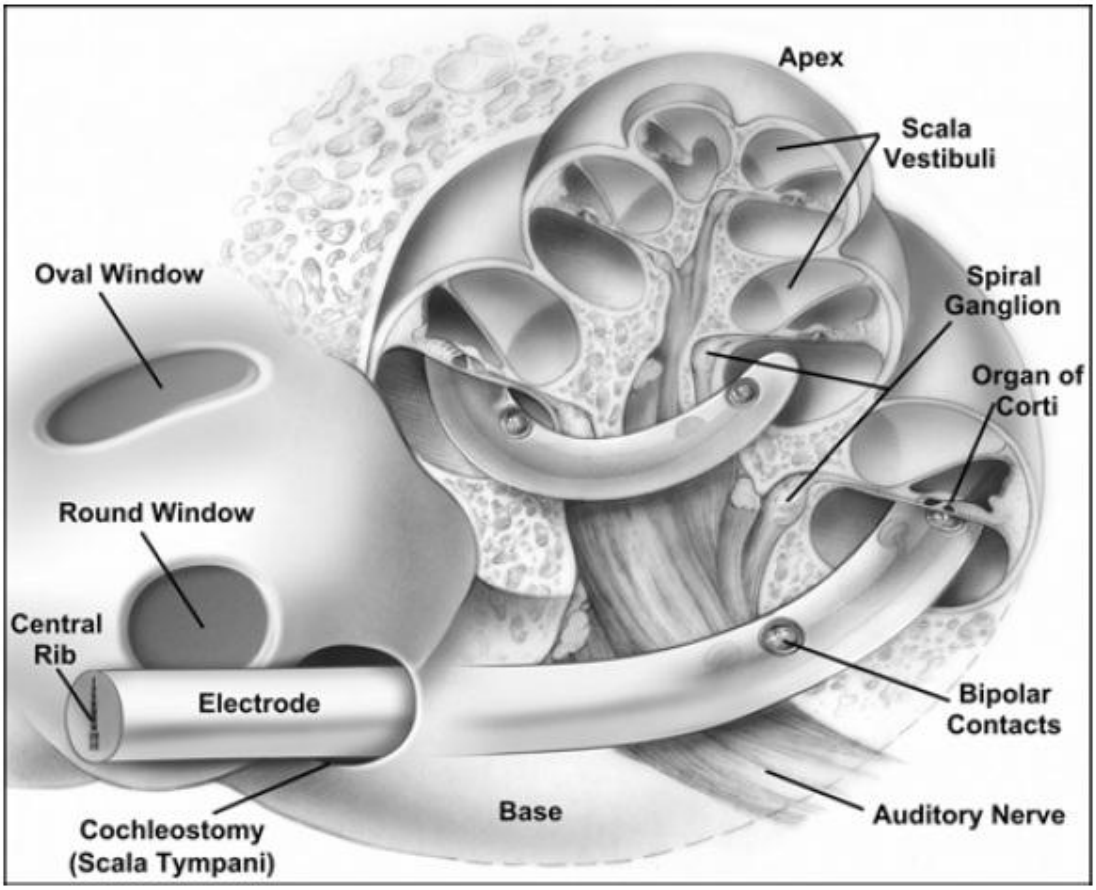


Fig. 2.10. Cutaway drawing of implanted cochlea [16].

The illustration and the architecture of the cochlear implant are shown in Fig. 2.11 [2]. The goal of a cochlear implant is using electrical stimulation safely to provide or restore functional hearing [2]. Cochlea implant can be divided to external part and implant part. The external part comprises of a microphone, filters, an analog-to-digit converter (ADC), a digit signal processor (DSP), a power amplifier (PA), and a transmitter. The internal part comprises of a power management unit, a decoder, a stimulator, and a back-telemetry. The external part is outside the human body, and the internal part is placed in the inner ear, the concept is shown in Fig. 2.12 [16]. The sound is picked by the microphone, filters and an ADC are used to convert the picked sound into a digit signal, and this digit signal processed and encoded by the DSP, and finally this signal is send to the internal part by the transmitter through the

transmission coil [2], [16], [20]. When the internal part received the encoded signal through the receiver coil, the encoded signal is demodulated by the demodulator and decoded by the decoder, and finally the stimulator deliver the stimulation pulses through the implanted electrode array to the auditory nerve in the cochlea [16], [2], [20]. Unlike external part can be powered by a battery, power for the internal part is transmitted wirelessly through PA, and the received ac power is rectified and regulated by the power management unit.

According the research of the other medical group, the auditory nerve is certainly can be stimulated by electrical stimulation, and the response can be recorded by electrically-evoked auditory brainstem responses (EABRs), as shown in Fig. 2.13 [21]. The relationship between the amplitude, the frequency, and the duration of stimulus current or stimulus voltage, and the size of electrodes is a tradeoff, so the best parameters should be decided by the experiments of the medical group, and the circuit design of the cochlear implant is according to the experiment results.

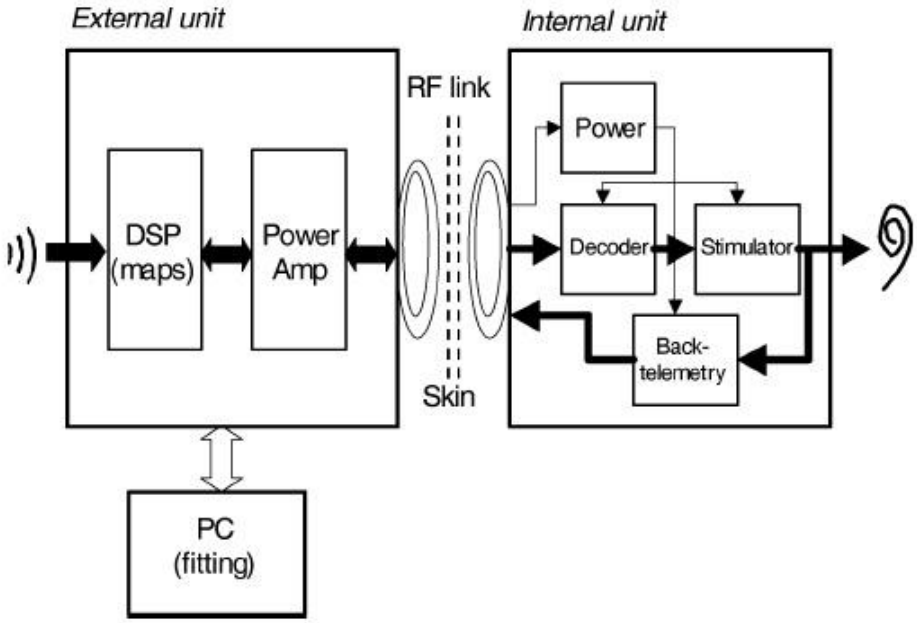


Fig. 2.11. Architecture and block diagram of a modern cochlear implant [2].

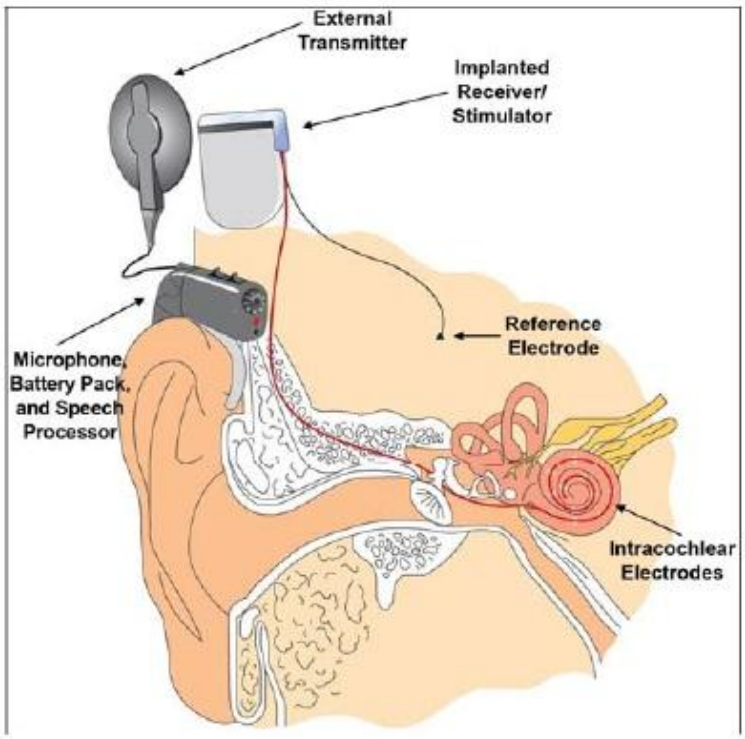


Fig. 2.12. The essential components of cochlear implant system with intracochlear electrodes [16].

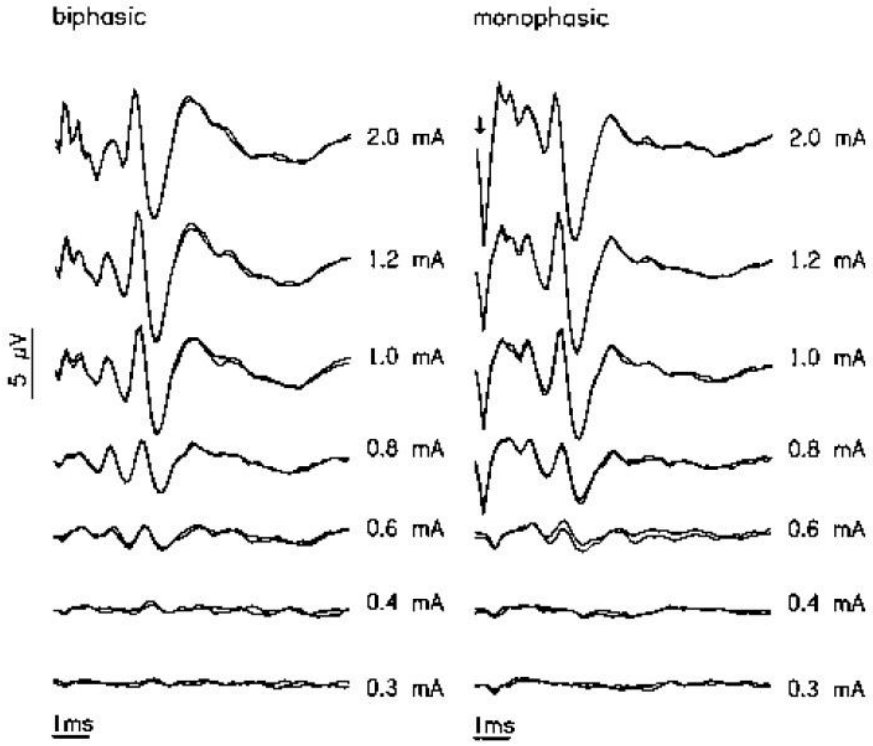


Fig. 2.13. Representative EABRs recorded from a mouse in response to a 50-μs per phase biphasic current pulse (left) and 50-μs per phase monophasic current [21].

2.3 Introduction and Design Consideration of Implantable Stimulator

As discussed in chapter 2.1, some lost function of human body can be restored by FES, and as discussed in chapter 2.2, many implant devices for medical application had been proposed. Thus a variety of implantable stimulators had been researched and presented in order to provide stimulus current or stimulus voltage to the tissues through implanted electrodes. While designing implantable stimulators, some considerations and challenging issues have to be taken into account such as safety, reliability, charge balance, and density of stimulus sites. And according to different applications, stimulators may have a single channel or multiple channels, monophasic or biphasic stimulation, monopolar or bipolar fashion, and constant-current mode or constant-voltage mode [22], [23].

The stimulation pulses may be monophasic or biphasic, early stimulation pulses are usually monophasic, but monophasic stimulation pulses can cause the residual charge accumulated in the tissues, and it can induce DC current, thus the tissues are damaged by the residual charge. Most stimulation pulses now are biphasic [23]-[24]. In biphasic stimulation, usually a cathodic phase followed by an anodic phase, and an interphase delay is between a cathodic phase and an anodic phase, as shown in Fig. 2.14 [23]-[24]. In the cathodic phase, the stimulus current is send to the tissues for generating action potentials on the tissues, so the tissues are stimulated. The succeeding anodic phase is used to cancel the residual charge accumulated in the cathodic phase on the tissues. The interphase delay is used to separate the two stimulation phase so that the physiological effect of the cathodic phase cannot be reversed by the anodic phase [23]-[24].

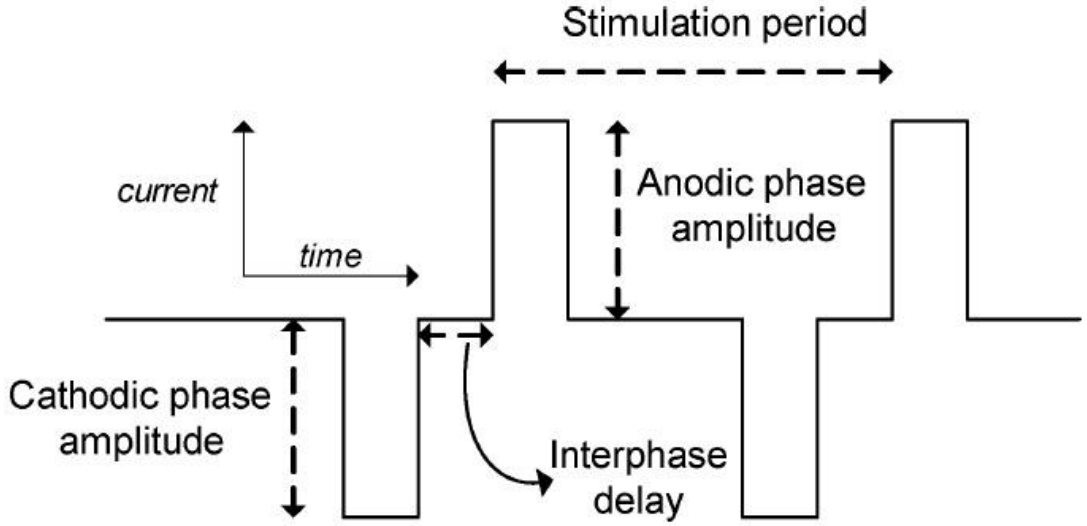
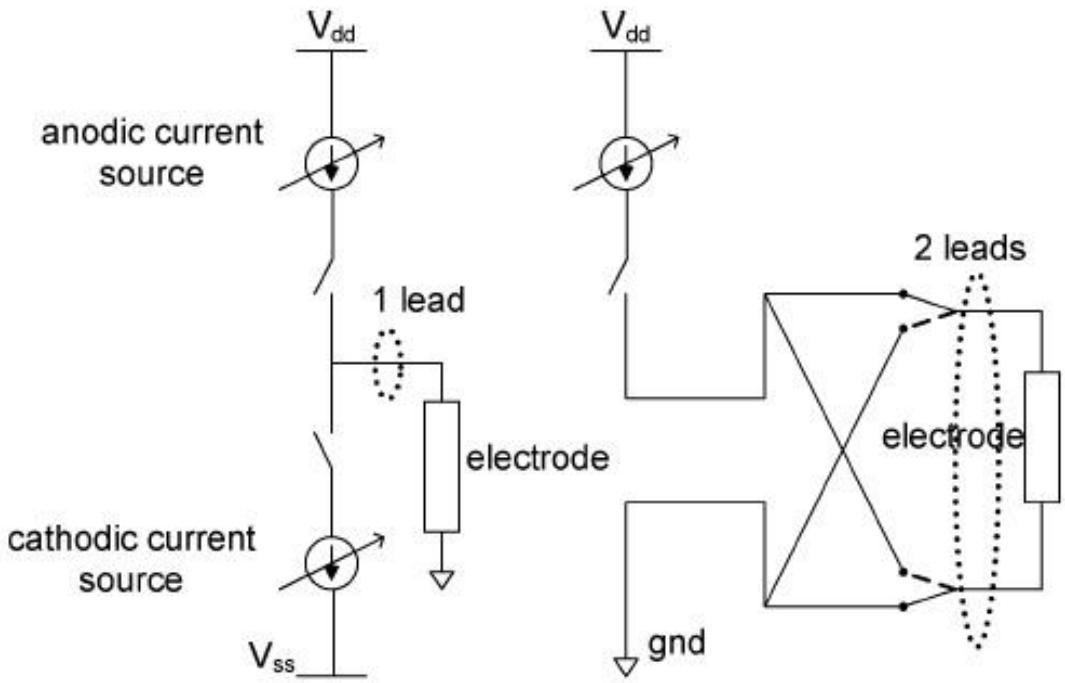


Fig. 2.14. Biphasic stimulation pulse [23].

In order to generate the biphasic stimulation pulses, there are two choices of chip-electrode configurations [23]. The first type is that only one interconnect lead per stimulation site is used, and a return electrode, common to all the stimulating electrodes, is connected to the ground potential [23]. In the first type, two supply voltages are required, one supply voltage is with a positive polarity, another supply voltage is with a negative polarity, as shown in Fig. 2.15(a) [23], [25]. The advantage of the first type is that the number of electrodes can be reduced, but the drawback of the first type is that it is hard to implement the circuits with negative polarity voltage in CMOS process. The first type is suitable for high-density stimulation sites such as epi-retinal prosthesis, as shown in Fig. 2.16 [5]. The second type is that two interconnect leads per stimulation are used, shown in Fig. 2.15(b) [23], so only one supply voltage is required since each stimulation site has a dedicated return path [23], [26]. The advantage of the second type is that only one supply voltage with a positive polarity is needed, but the drawback of the second type is that the numbers of electrodes are doubled. The second type is suitable for low-density stimulation sites such as epileptic seizure controller, as shown in Fig. 2.17 [27].



(a) (b)

Fig. 2.15. Electrode configuration. (a) One interface lead per site. (b) Two interface leads per site [23].

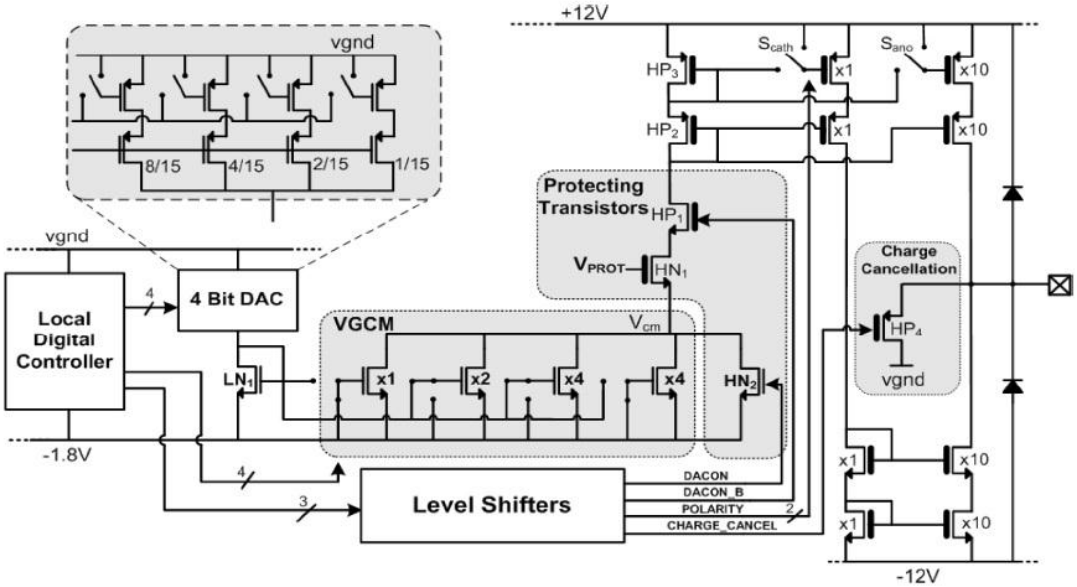


Fig. 2.16. A stimulator pixel of an integrated 256-channel epiretinal prosthesis, it needs only one interconnect lead per stimulation site [5].

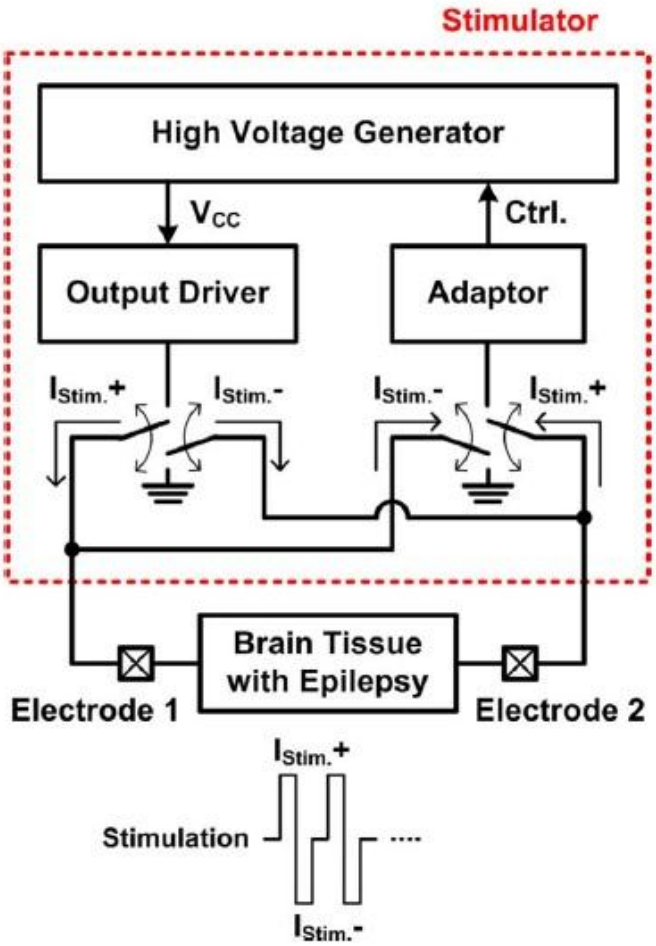


Fig. 2.17. A stimulator of an epileptic seizure controller, it needs two interconnect leads per stimulation site [27].

Studies shows that if the residual DC current is larger than 100 nA, the neural tissue may be damaged [21], so several techniques of the circuit design for reducing residual current is proposed. The circuit model of the measured impedance of the tissues with implanted electrodes is usually as Fig. 2.18, the R_S is about several tens of kΩ, and C_P is about several hundreds of nF [5]. Although the stimulation pulse is biphasic, but due to the mismatch between the amplitudes of the anodic and cathoidc current, there are still some residual charge in the tissues after every stimulation pulse. The DC current caused by the residual charge may be larger than 100 nA, so some techniques are proposed for reducing the DC current. The commonly used method is

to short all electrodes to ground after every biphasic stimulation pulses, but the time needed for the DC current is smaller than 100 nA is relative to the time constant of R_S and C_P. The time constant of R_S and C_P is usually too large, so there is no enough time to let the DC current is smaller than 100 nA between every stimulation pulse. The second method is to insert a large DC blocking capacitor (> 100 nF) between each electrode [28], so the DC current can be blocked [28], as shown in Fig. 2.19 [24], but large off-chip capacitor is not suitable for implant devices. Another method is using the circuit design techniques to reduce the mismatch between the amplitudes of the anodic and the cathodic current pulses such as [29]. In [29], a feedback current DAC calibration technique by sampling and holding a correction current is proposed to reduce the mismatch between the amplitudes of the cathodic and the anodic current pulses, as shown in Fig. 2.20, and this method can achieve ~90 nA of DC error.

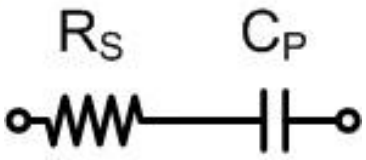


Fig. 2.18. The circuit model of the measured impedance of the visual nerve with implanted electrodes.

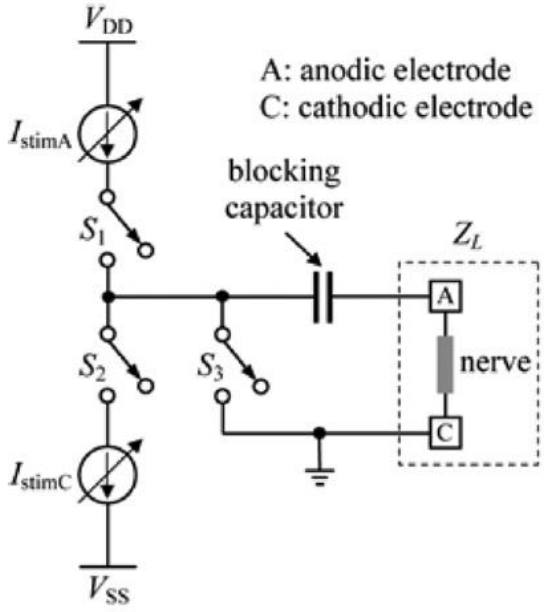


Fig. 2.19. A stimulator with a blocking capacitor to reduce the DC current [24].

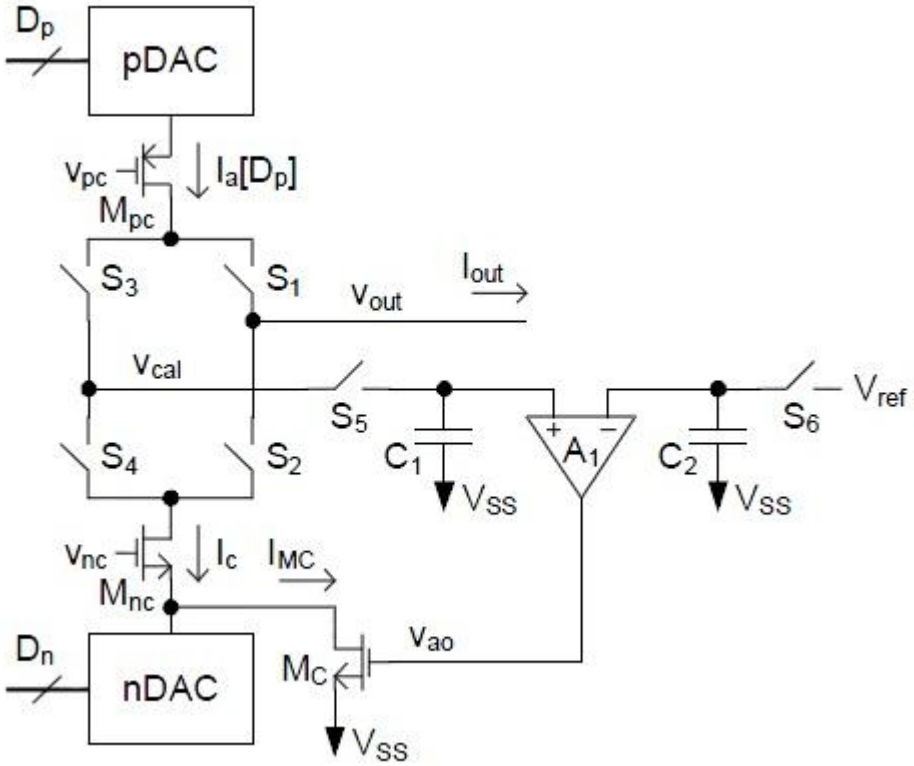


Fig. 2.20. A stimulator with a feedback current DAC calibration technique [29].

Chapter 3

Design of Bipolar Biphasic Stimulator for Cochlear Implant with High-Voltage-Tolerance

3.1 Introduction

The cochlear implant system is one kind of medical application for the profound deafness. The auditory sensation at the level of the brain cortex can be induced by generating action potentials on the surviving nerve in the cochlea [3], [17]. Base on this mechanism, cochlear implant is implanted into the inner ear to deliver electrical impulses to stimulate the surviving auditory nerve in the cochlea when sound is picked by the microphone of the cochlear implant.

Our cochlear implant system shown in Fig. 3.1 is divided to the external part and the internal part. The external part comprises of a microphone, a filter, an analog-to-digit converter (ADC), a digit signal processor (DSP), and a power amplifier (PA). The internal part comprises of a rectifier, a regulator, a demodulator, a back telemetry, a stimulator, and electrode arrays. Sound is picked up by the microphone, ADC converts sound into a digit signal, and this digit signal processed and encoded by DSP, and finally this signal is send to the internal part through the transmission coil. When the internal part received the encoded signal through the receiver coil, the encoded signal is demodulated by demodulator and decoded by the data decoder, and finally the stimulator delivers stimulation pulses through electrode arrays to the auditory nerve in the cochlea according to this signal. Unlike the external part can be powered by battery, power for the internal part is transmitted wirelessly

through PA, and the received ac power is rectified by the rectifier and regulated by the regulator into DC power.

Our cochlear implant project can be divided into several sub-projects, and the stimulator is developed by our research group. The stimulator of the cochlear implant system may have a single channel or multiple channels, monophasic or biphasic stimulation, monopolar or bipolar fashion, and current mode or voltage mode [22]-[23]. From the biomedical application in our cochlear implant project, a stimulator with four output channels stimulated in bipolar fashion, biphasic pulse, and voltage mode is requested. According to different amplitude of the picked sound by the microphone, the output of the each output channel should be able to provide adjustable stimulus voltage to the electrodes those are implanted into the cochlea.

The well-developed CMOS processes had been attractive to realize the implantable device for biomedical electronic applications. But the operation voltage of the stimulator is usually higher than the device normal operating voltage of a low-voltage CMOS process, so the stimulator was usually implemented in the high-voltage CMOS process [30]. According to the request of our biomedical project for cochlear implant, the required maximum stimulus voltage is as high as 7 V. For SoC integration purpose, the other circuits including data decoder, rectifier, regulator, demodulator in the implant SoC device are all designed and realized in the low-voltage CMOS process to reduce power consumption. So the stimulator combined with a high voltage generator implemented in the low-voltage CMOS process is needed [31].

Before the human psychoacoustic experiment, the animal experiment to verify the function of the stimulator should be performed in advance. Before the circuit design, the influence of the loading impedance to the stimulator should be

investigated first, and then the architecture if the circuit can be decided to optimize the circuit performance.

In this work, a stimulator for cochlear implant with high-voltage-tolerance is proposed. This stimulator consists of four output channels combined an on-chip high voltage generator is implemented in the 0.18-μm 1.8-V/3.3-V CMOS process. In this chapter, firstly the measured impedance data of the cochlea and impedance analysis will be presented. Secondly, the proposed stimulator is introduced. Finally, the measurement results are presented.

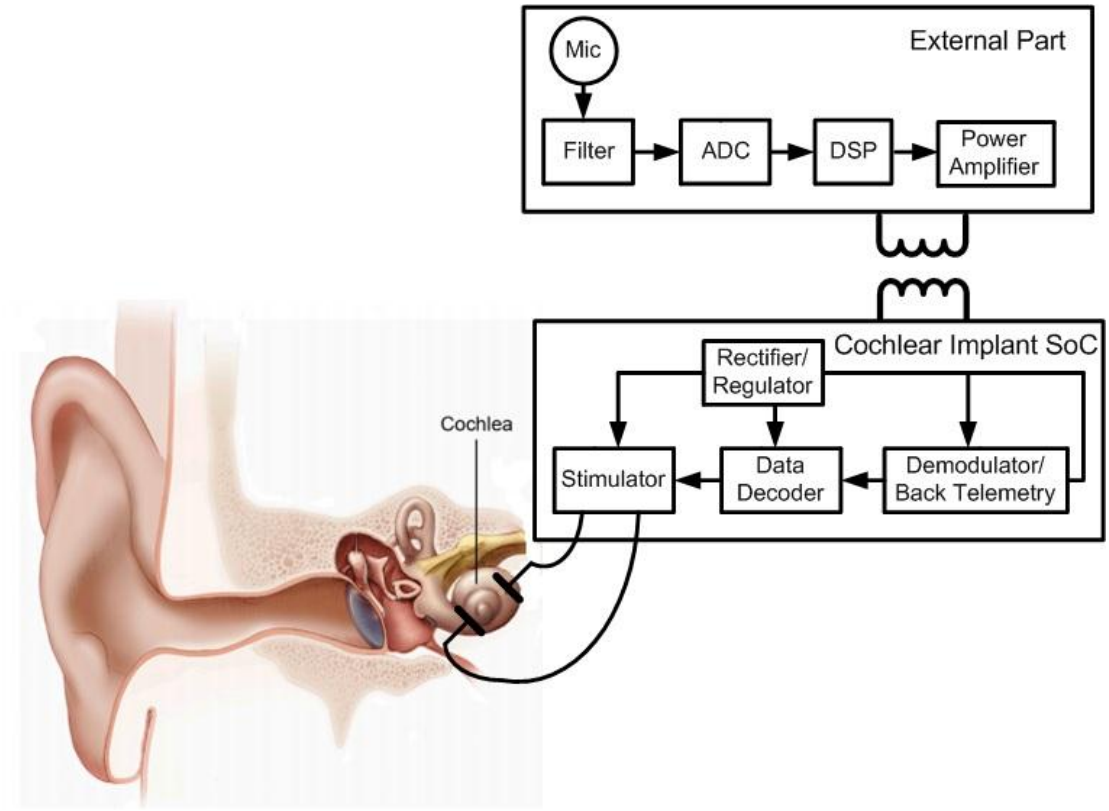
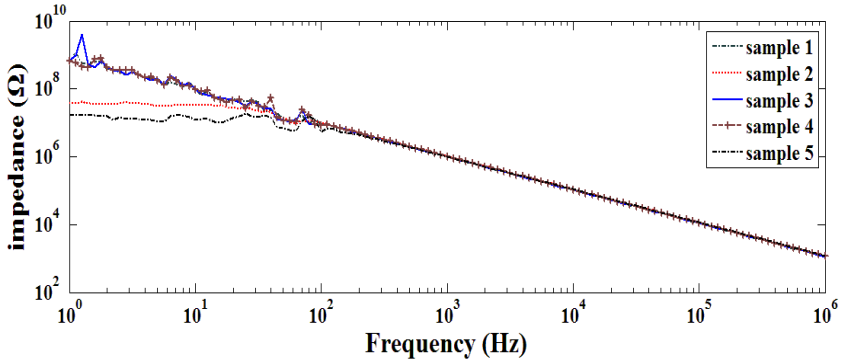
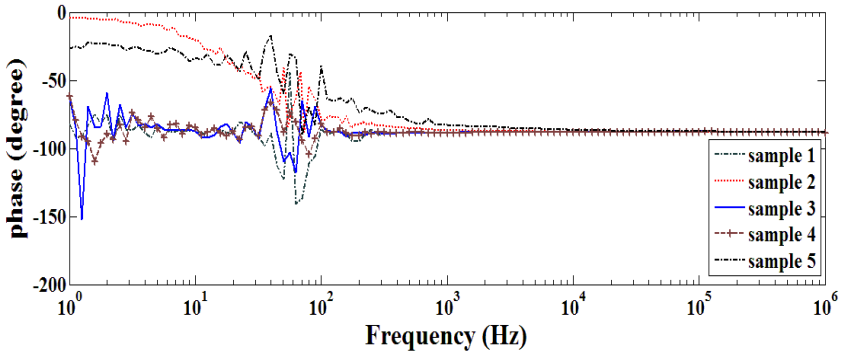


Fig. 3.1. Architecture of our cochlear implant, and block diagrams of the external part, and the implant part are shown.

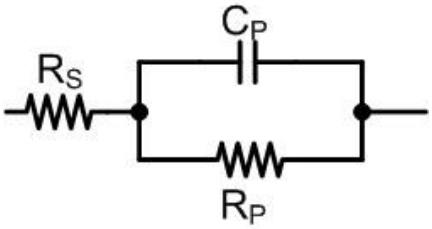
3.2 Impedance Analysis

Before the circuit design, the influence of the loading impedance to our stimulator should be investigated first, and then the architecture of the circuit can be decided and circuit performance can be optimized according the measured loading impedance. The stimulus voltage is sent through the implanted electrodes into the cochlea, so the loading impedance not only includes the impedance of the cochlea but also the impedance of the implanted electrodes. The impedance of the cochlea of guinea pig with the implanted electrodes was measured by the impedance analyzer (Solartron SI 1260), the frequency was swept form 1 Hz to 1 MHz, the measured results are shown in Fig. 3.2(a), and there are totally five measured impedance data. These five impedance data should be calculated to a circuit model for the convenience of the circuit design and circuit simulation. The circuit model shown in Fig. 3.2(b) is used to fit the measured impedance data, the fitted results are shown in Table 3.1. In these five fitted results, all the series resistors (R_S) are very small < 100 Ω, all the shunt resistors (R_P) are all very large > 10 MΩ, and all the shunt capacitors (C_P) are all very close to 150 pF. These five fitted results are close to a capacitor of 150 pF. These five measured data and a 150-pF capacitor are separately as the output load of the stimulator in the circuit simulation, and all the simulation results are almost the same. For the convenience of the circuit simulation and the circuit measurement, a 150-pF capacitor is as our loading impedance.





(a)



(b)

Fig. 3.2. There are five measured impedance data of the cochlea of guinea pig with implanted electrodes in (a), and (b) is the circuit model used to fit the measured data.

Table 3.1 The fitted results of the measured impedance data.

Data Number	R_S (Ω)	R_P (Ω)	C_P (pF)
Sample 1	68.5	$6.30\ 10^{9}$	160.2
Sample 2	75.5	$35.8\ 10^{6}$	147.7
Sample 3	54.9	$30.0\ 10^{15}$	157.3
Sample 4	71.0	$15.7\ 10^{6}$	159.4
Sample 5	71.5	$8.40\ 10^{9}$	155.3

3.3 Design of Bipolar Biphasic Stimulator for Cochlear Implant

3.3.1 Architecture and Block Diagrams of the Proposed Stimulator

The stimulator for our cochlear implant is stimulated in bipolar fashion and biphasic stimulation, the illustration of the stimulator is as shown in Fig. 3.3, and the waveform of the biphasic stimulus voltage is shown in Fig. 3.4. Because of the time constant composed of R_P and C_P in Table 3.1 is small, so charge balanced stimulation is achieved by let all electrodes connected to ground after every stimulation pulse. The maximum output voltage of the stimulator is as high as 7 V, so stacked MOS configuration and dynamic bias technique are used to realize the stimulator in the low-voltage CMOS process to avoid the issues of gate-oxide reliability and electrical overstress. According to the above considerations, the architecture of the proposed stimulator is shown in Fig. 3.5, the stimulator consists of four output channels, a voltage reference, and a high voltage generator. The proposed stimulator is implemented in TSMC 0.18-μm CMOS process, this process provides core device and I/O device, and tolerant voltage of core device and I/O device are 1.8 V + 10 % and 3.3 V + 10 % separately.

In the cochlear implant, only one supply voltage V_{DD} is provided for the simulator, so a high voltage generator is needed to boost V_{DD} (1.8 V) to V_{DDH} (8.4 V). The high voltage generator is classified to two structures: one is boost converter, and the other one is charge pump. Usually the power efficiency of the boost converter is higher than the charge pump, but the boost converter must need a large size off-chip inductor, and charge pump can be fully implemented in CMOS processes without off-chip components. In biomedical application, the size of the implant part is the smaller the better, so the number of off-chip components should be reduced. To reduce the number of off-chip components, charge pump based high voltage generator

is adopted. A precise and stable reference voltage is needed for stimulus drivers to reduce the mismatch between positive and negative stimulus voltage, also the high voltage generator needs a precise and stable reference voltage to regulate its output voltage. Thus a bandgap based voltage reference circuit is used to provide the desired reference voltage for four output channels and the high voltage generator.

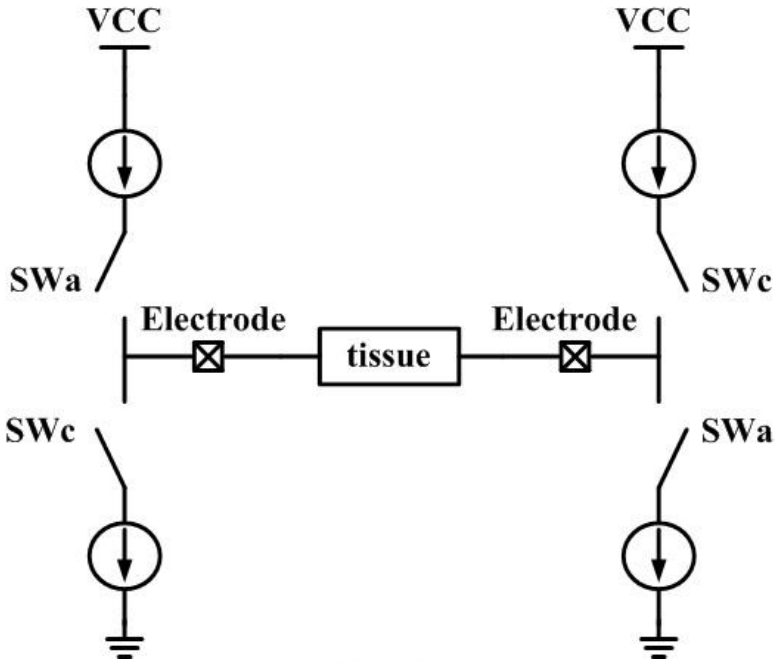
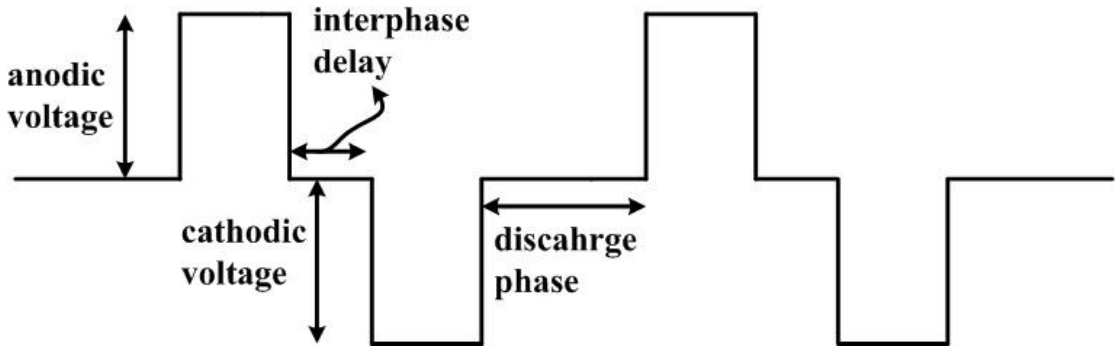


Fig. 3.3. The illustration of a stimulator with bipolar fashion and biphasic stimulation.



(b)

Fig. 3.4. The waveform of the biphasic stimulus voltage.

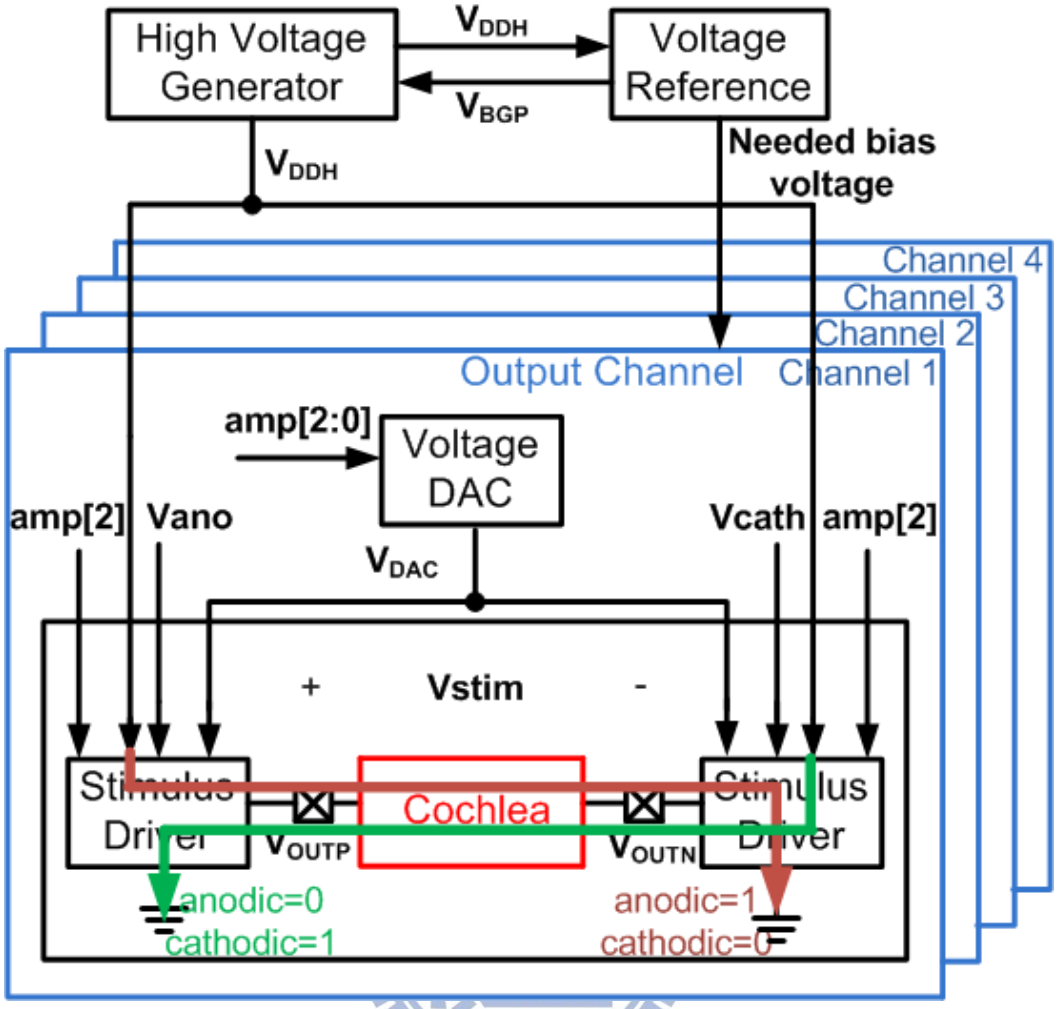


Fig. 3.5. The architecture and block diagrams of the proposed stimulator.

One output channel adopts two electrodes per stimulus site (V_{OUTP} and V_{OUTN}), and through the switch to generate biphasic stimulus voltage. The benefit is that negative voltage can be avoided to be used, so the chip area and design difficulty of the stimulator can be reduced. One output channel can deliver the stimulus voltage (Vstim) to the cochlea, where the Vstim is defined as $V_{OUTP} - V_{OUTN}$. In biomedical application, the amplitude and the pulse width should be adjustable according to the picked sound. The waveforms of one output channel is shown in Fig. 3.6, the polarity and pulse width are adjustable according to the control signals (Van / Vcath), and the amplitude is also adjustable according to the 3-bit signals (amp). After every biphasic stimulation pulse (in discharging phase), Vano and Vcath are at logic 0, and V_{OUTP} and

V_{OUTN} are shorted to ground to prevent from charge accumulation on the auditory nerve in the cochlea.

One output channel in the stimulator consists of a voltage digital-to-analog converter (voltage DAC) and two stimulus drivers. The left stimulus driver in Fig. 3.4 is the same as the right stimulus driver, the difference between them is that only the control signal “Vano” and output node “V_{OUTP}” are changed to “Vcath” and “V_{OUTN}”. The circuit block of the left stimulus driver of one output channel is shown in Fig. 3.7, it consists of a dynamic bias circuit, a high-voltage-tolerant amplifier, and an output stage. A 3-bit signal (amp) is used to control the amplitude of Vstim, and the Vano and Vcath signals are used to control the polarity and pulse width of Vstim. The pulse width of Vstim is as same as the duration of Vano or Vcath remains logic 1. When Vano is logic 1 and Vcath is logic 0, the left stimulus driver in Fig. 3.5 will deliver a voltage pulse at V_{OUTP} node; as well as the V_{OUTN} node will be connected to ground by the right stimulus driver, so the Vstim is with a positive polarity. When Vano is logic 0 and Vcath is logic 1, the right driver will deliver a voltage pulse at V_{OUTN} and V_{OUTP} will be shorted to ground, so the Vstim is with a negative polarity. Through the control of Vano and Vcath signals to reach the biphasic stimulation, the negative voltage source was not needed in this design.

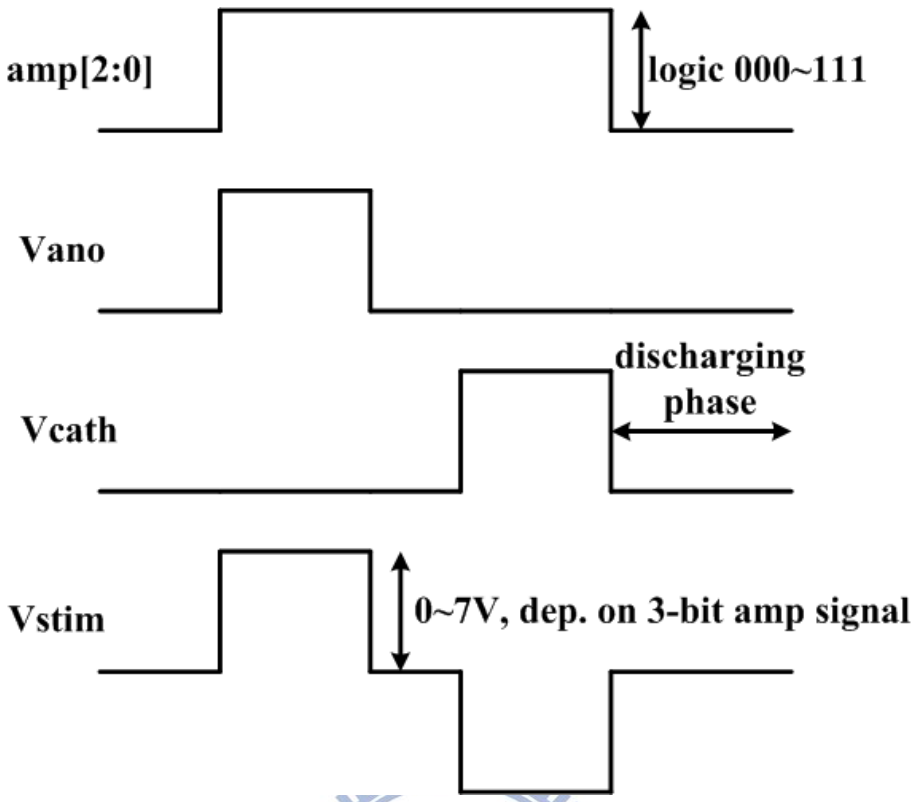


Fig. 3.6. The voltage waveform of one output channel.

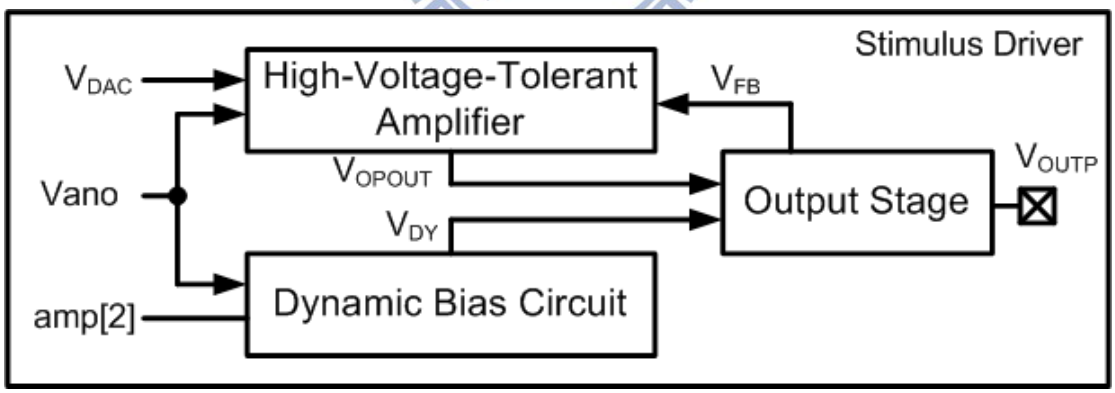


Fig. 3.7. Circuit blocks of the left stimulus driver of one output channel.

3.3.2 Voltage Reference

The proposed voltage reference circuit is composed of a bandgap reference, a high bias voltage generator, and a voltage DAC. The used bandgap reference circuit is adopted from [32], as shown in Fig. 3.8. A reference current I_{REF} is generated by the bandgap reference circuit, this reference current I_{REF} is inversely proportional to the resistor R_{BG2}, and this current is not sensitive to process variation, supply voltage, and temperature. The current I_{BGP} mirrored from M_2 and M_{BGP} is flowing through R_{BGP} to generate a reference voltage V_{BGP}. Because I_{BGP} is copied from I_{REF}, so the reference voltage V_{BGP} is only affected by the relative mismatch between R_{BG2} and R_{BGP}. Through a suitable layout drawing, the relative mismatch between R_{BG2} and R_{GBP} can be very small, thus V_{BGP} is not sensitive to process variation, supply voltage, and temperature. 3-bit Vtrim signal is used to control the resistor value of R_{BG2}, thus V_{BGP} can be adjusted by 3-bit Vtrim signal. V_{BGP} is used as the reference voltage for the high voltage generator to regulate its output voltage V_{DDH}.

The bandgap reference circuit has two operation points, one is normal operation point, and the other one is zero point. To prevent the bandgap reference circuit stays at zero point, so a start up circuit is needed, the used start up circuit is shown in Fig. 3.9.

Stimulus voltage of the stimulator should be adjustable according to the sound picked by the cochlear implant, so each output channel needs an adjustable reference voltage V_{DAC} to regulate its output voltage. The proposed voltage DAC circuit is shown in Fig. 3.10. The gate voltage of M_{ADC2}, M_{DAC1}, M_{DAC0}, and M_2 are at the connect point V_P, so gate-to-source voltages of these four transistor are the same. Thus I_{DAC} can be mirrored from the transistor M_2. The amplitude of V_{DAC} is decided by the amount of current I_{DAC} flowing through the resistor R_{DAC}. M_{DAC2}, M_{DAC1}, and M_{DAC0} are in different transistor size, so through 3-bit amp signal to control M_{S2}, M_{S1}, M_{S0} is conductive or not conductive can generate different current amount of I_{DAC}.

Thus the amplitude of V_{DAC} can be controlled by 3-bit amp signal, and four-channel V_{DAC} are sent to four output channels as the reference voltage for regulating the stimulus voltages separately. The relationship between 3-bit amp signal, V_{DAC}, and V_{OUTP} is shown in Table 3.2.

Because the maximum stimulus voltage of stimulus drivers is 7 V, so stimulus drivers is operated under high supply voltage V_{DDH} (8.4 V). Thus stimulus drivers need a high bias voltage generator to generate suitable high bias voltages for stimulus drivers for preventing the transistor in stimulus drivers from the issues of electrical overstress and gate-oxide reliability. The proposed high bias voltage generator is shown in Fig. 3.11. The current I_{BIAS} mirrored from M_2, M_{HP0}, M_{HN0}, M_{HN1}, and M_{HP1} flowing through R_{B3}, R_{B2}, R_{B1}, and R_{B0} to generate bias voltage (V_{B3}, V_{B2}, V_{B1}, and V_{B0}) for stimulus drivers. A series of diode-connected I/O PMOS M_{D0}~M_{D7} are used to prevent M_{HN1} from electrical overstress.

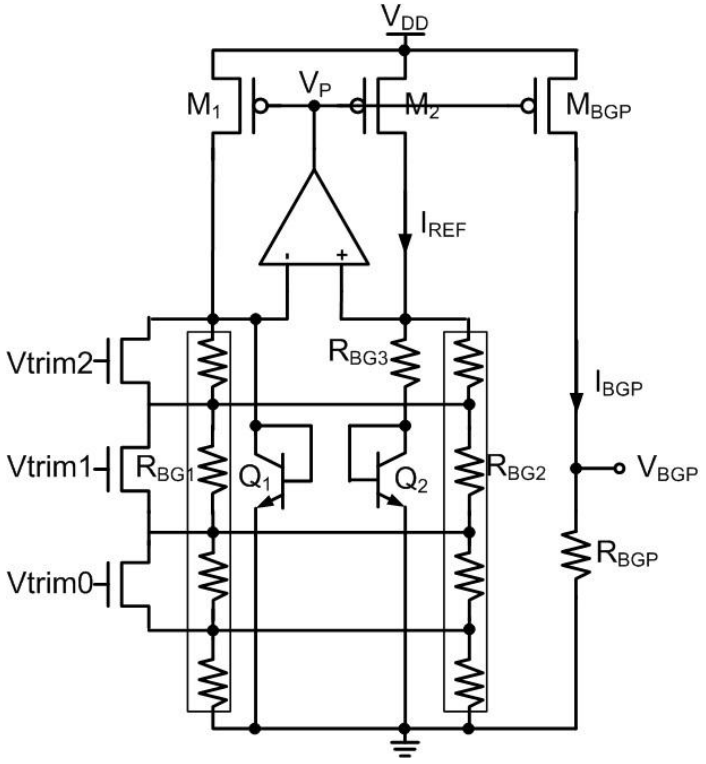


Fig. 3.8. The used bandgap reference circuit.

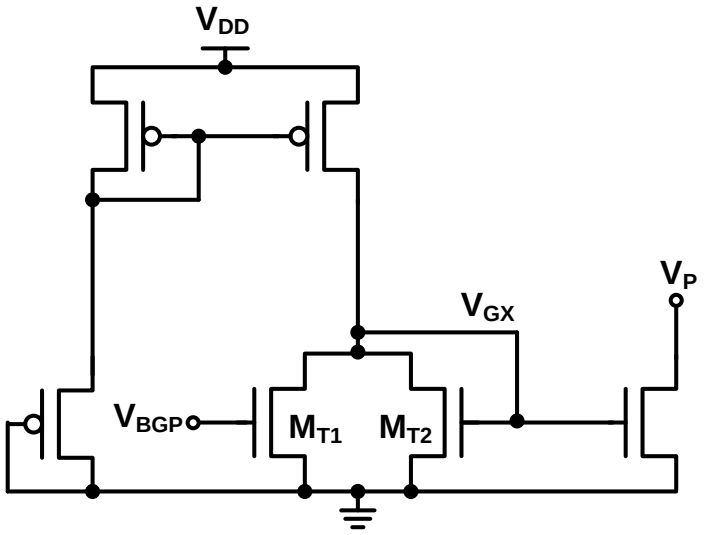


Fig. 3.9. The used start up circuit.

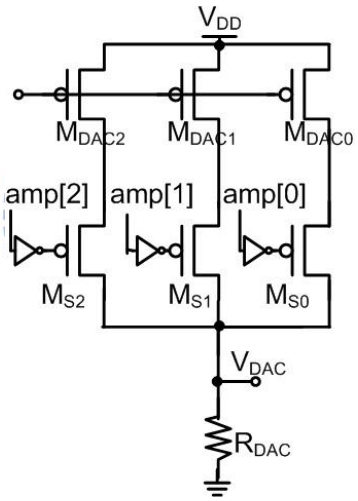


Fig. 3.10. The used voltage DAC.

Table 3.2 The relationship between 3-bit amp signal, V_{DAC} and V_{OTUP}.

amp[2:0]	000	001	010	011	100	101	110	111
V_{DAC} (V)	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7
V_{OUTP} (V)	0	1	2	3	4	5	6	7

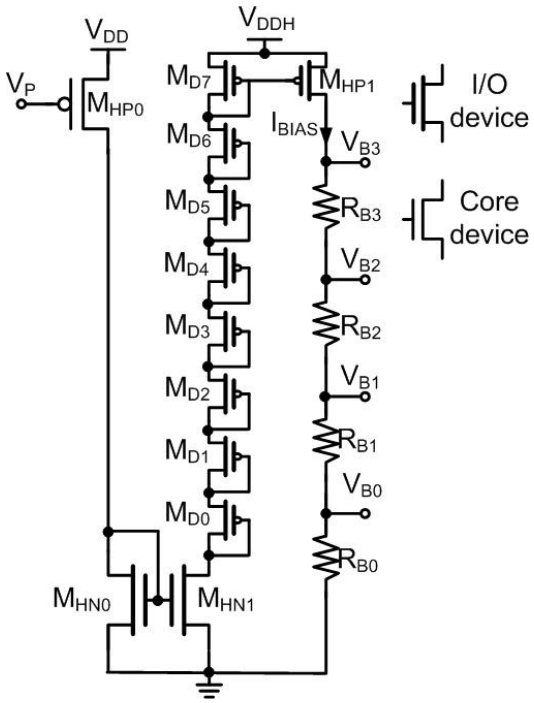


Fig. 3.11. The used high bias voltage generator.

3.3.3 The Stimulus Driver Circuit of One Output Channel

The circuit blocks of the left stimulus driver of one output channel is shown in Fig. 3.7, it consists of a high-voltage-tolerant amplifier, an output stage, and a dynamic bias circuit. Due to the maximum output voltage of the stimulus driver circuit is as high as 7 V, so the supply voltages of the stimulus driver circuit are V_{DD} (1.8 V) and V_{DDH} (8.4 V) separately. Because the stimulus driver circuit is operated under 8.4 V, so it should be noticed that gate-to-source, gate-to-drain, and drain-to-source voltage must be smaller than the tolerant voltage of the transistor, and the tolerant voltages of core device and I/O device are 1.8 + 10 % and 3.3 V + 10 % separately.

The proposed high-voltage-tolerant amplifier and output stage are shown in Fig. 3.12. If the loop gain of the feedback loop in the high-voltage-tolerant amplifier and output stage is high enough, then V_{ADC} and V_{FB} can be forced at almost the same voltage level by this negative feedback loop, but the feedback loop has the problem about the stability. So the analysis of poles and zeros at V_{OUTP} becomes important. The measured impedance data have been calculated to a circuit model, as discussed in chapter 3.2. The measured impedance and feedback resistors (R_1 and R_2 in Fig. 3.12) can generate one pole at V_{OUTP}, other poles and zeros are much higher than unity gain frequency, so they can be neglected. Thus, only one pole at ~1 kHz will be induced at V_{OUTP}.

When Vano signal is logic 1, the one output channel will deliver a voltage pulse at V_{OUTP}. The NMOS current path of the output stage and Mswitch of the high-voltage-tolerant amplifier will be turned off, so the high-tolerant amplifier is in normal operation, the negative feedback loop is built, thus the high-voltage-tolerant amplifier can force the voltage level of V_{FB} almost as same as V_{DAC}. The resistance of R_2 and R_1 are in 1:9 ratios, so the voltage level of V_{OUTP} is ten times of the voltage

level of V_{DAC}, and the relationship between V_{OUTP} and 3-bit amp signal is shown in table 3.2.

When one output channel delivers negative stimulus voltage or not in stimulation or in discharging phase (Vano is at logic 0), V_{OUTP} should be connected to ground and V_{OPOUT} should be connected to V_{DDH} to turn off the PMOS current path of the output stage.

When Vano is at logic 0, Mswitch will be turned on, and V_X will be shorted to V_{DD}. Thus, M_{R3}, M_{R4}, M_{R5}, M_{R6} are off, it means that $I(M_{R3}) = I(M_{R4}) = I(M_{R5}) = I(M_{R6}) = 0$, but the gate voltage of M_{R6} is biased by diode-connected MOS M_{L6}, and $I(M_{L6}) \neq 0$, so drain-to-source voltage of M_{R6} will be 0, V_{OPOUT} is therefore shorted to V_{DDH}.

In the high-voltage-tolerant amplifier, fixed gate bias voltages (V_{B0}, V_{B1}, V_{B2}, and V_{B3}) are used to prevent MOS in the high-voltage-tolerant amplifier from the issues of electrical overstress and gate-oxide reliability. In the output stage, the stimulus driver circuit can deliver different amplitude of voltage pulse at V_{OUTP}, according to 3-bit amp signal and Vano signal logic low or high. Because the change of the voltage level of V_{OUTP} is large, so dynamic bias technique is needed for preventing MOS in the output stage from electrical overstress and gate-oxide reliability, and the proposed dynamic bias circuit is shown in Fig. 3.13. V_{DY} is controlled by the signal Vano and amp[2], and according to different Vano and amp[2] V_{DY} may be 2.4 V or 4 V. When the stimulus driver circuit is in stimulation and V_{OUTP} is at low voltage level (< 4V), it means Vano is logic 1 and amp[2] is logic 0, so the dynamic bias circuit can bias the gate voltage of M_{P0} and M_{N0} at 2.8V, thus gate-to-source, gate-to-drain, and drain-to-source voltage of all MOS in the output stage are < 3.3V. When the stimulus driver circuit is in stimulation and V_{OUTP} is at high voltage level (> 4V), it means Vano is logic 1 and amp[2] is also logic 1, the

dynamic bias circuit can bias gate voltage of M_{P0} and M_{N0} at 4 V, so gate-to-source, gate-to-drain, and drain-to-source voltage of all MOS in the output stage is < 3.3V. When the stimulus diver circuit is negative stimulation or in discharging phase, V_{OUTP} is at almost 0 V, and the dynamic bias circuit can bias the gate voltage of M_{P0} and M_{N0} at 2.8V, if source voltages of MOS of the output stage is as same as their gate voltages ($V_{DP2} = V_{B3}$, $V_{DP1} = V_{DY}$, $V_{DN1} = V_{DY}$, and $V_{DN2} = V_{DD}$), then gate-to-source, gate-to-drain, and drain-to-source voltage of all MOS in the output stage is < 3.3V. But when the Vano signal is from logic 1 to logic 0, due to charge sharing, the source voltage of M_{P0} cannot be the same as its gate voltage V_{DY}. To solve this issue, V_{OUTP} should be connected to ground before V_{OPOUT} connected to V_{DDH}, so a delay circuit is inserter between the gate of Mswitch and the Vano signal for generating delay time.

When the change of the loading current at V_{DDH} is large, then the amplitude change of V_{DDH} can be large because of the on-chip capacitor cannot be large enough. To solve this problem, diode string in the high-voltage tolerant amplifier is used to prevent the output stage drawing large current from V_{DDH} immediately, although it may influence the slew rate, but the stimulation frequency is not very high, so it can be accepted.

One pole is generated at V_{OPOUT}, and the location of this pole is below the unity gain frequency, so there are two poles before the unity gain frequency, the phase margin may not be enough. Thus Rc and Cc in the high-voltage-tolerant amplifier are used to generate a zero to compensate the pole at V_{OPOUT}, and the phase margin can be large enough.

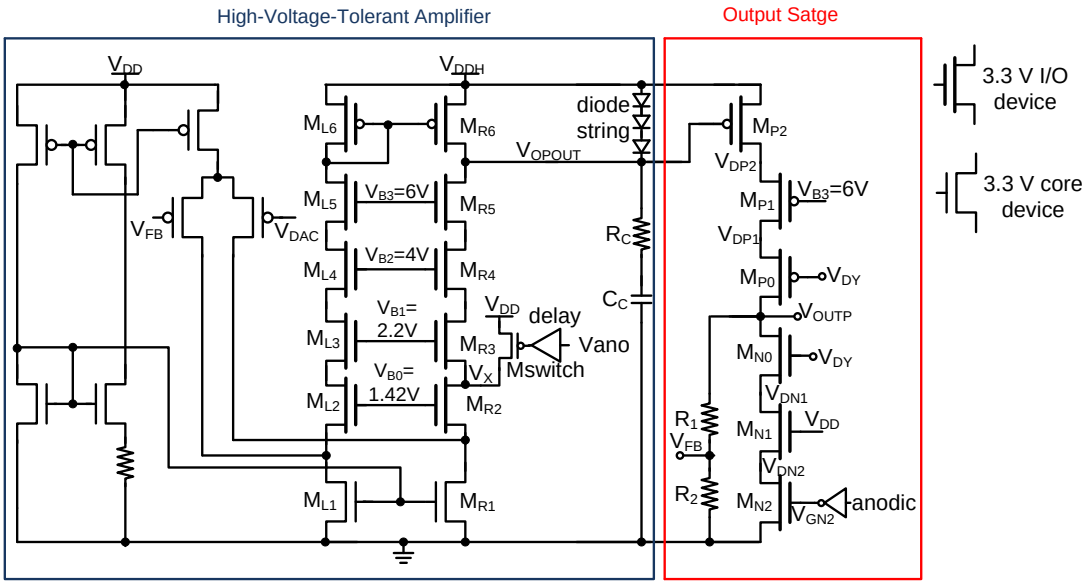


Fig. 3.12. The proposed high-voltage-tolerant amplifier and output stage in the stimulus driver.

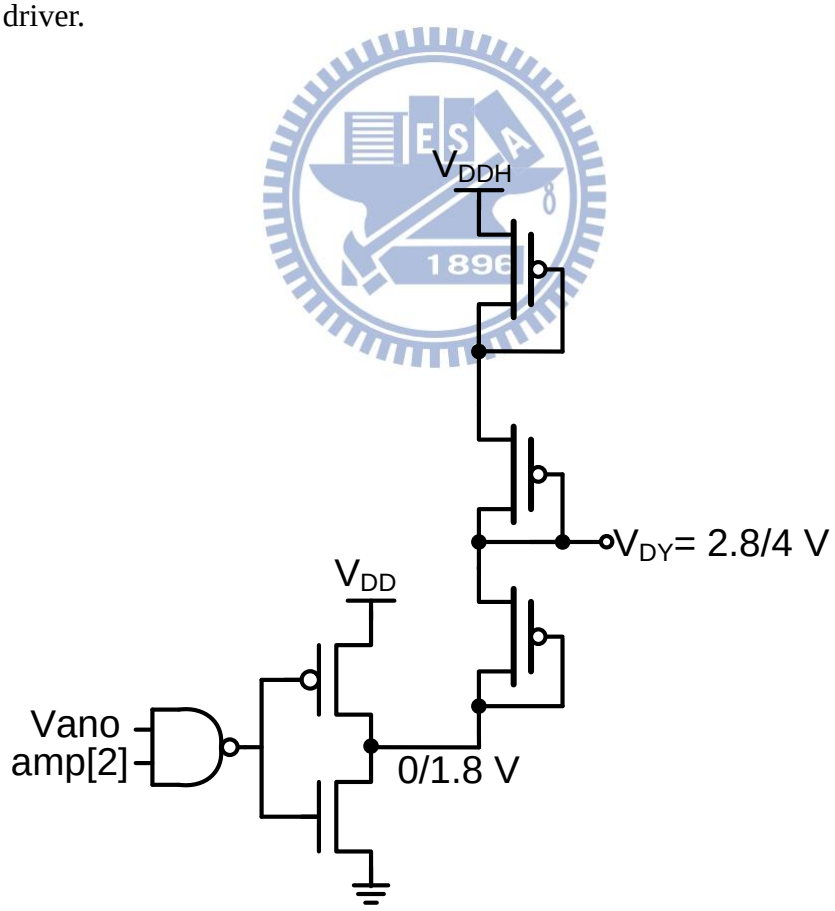


Fig. 3.13. The proposed dynamic bias circuit.

3.3.4 High Voltage Generator

Fig. 3.14 depicts the architecture of the high voltage generator, which is composed of a 5-stage charge pump, an amplifier, a voltage-controlled oscillator (VCO), a two-phase clock generator, a buffer, feedback resistors (R_{F1}, R_{F2}), and an output capacitor (C_L). The high voltage generator has two operation mode controlled by en signal. When the stimulator is in stimulation, the signal (en) will be logic 1, and the charge pump start to pump, finally the output voltage (V_{DDH}) from the high voltage generator will be regulated at voltage level 8.4 V. When the stimulator is not in stimulation, the signal (en) will be logic 0, VCO is turned off, and thus the voltage level of V_{DDH} is at almost 0 V. The power consumption of the stimulator not in stimulation can be reduced.

The used charge pump circuit is adopted from [33], it can output the high voltage level (> V_{DD}) without the issues of electrical overstress and gate-oxide reliability. Without any loading current, the output voltage level is as Eg. (3-1), N is the number of the pumping stage, C_P is pumping capacitance, and C_{par} is parasitic capacitance at each pumping node.

$$V_{out} = V_{DD} + N\frac{C_P}{C_P+C_{par}}V_{DD} \quad (3\text{-}1)$$

The desired output voltage level is at 8.4 V, and V_{DD} is 1.8 V, so at least 4 pumping stage is needed. But when loading current arises, the formula can be modified as Eg. (3-2), f is pumping frequency, and I_{LOAD} is loading current at output node.

$$V_{out} = V_{DD} + N\frac{C_P}{C_P+C_{par}}V_{DD} - 5\frac{I_{LOAD}}{f(c_P+C_{par})} \quad (3\text{-}2)$$

Usually the desired output voltage level is designed about 70 ~ 80 % of the maximum output voltage level, so 5-stage charge pump circuit is used in this high voltage generator, as shown in Fig. 3.15. Because the used charge pump circuit has

dual path, so it needs two pumping capacitors (C_P) per stage, thus a two-phase clock generator, shown in Fig. 3.16, is used to transform one-phase clock to non-overlap two-phase clock.

Under fixed pumping frequency, the voltage level of V_{DDH} can be varied with the change of the loading current from V_{DDH}, so the pulse frequency modulation (PFM) is adopted to regulate V_{DDH}. The amplifier used in high voltage generator, shown in Fig. 3.17, the output (vctrl) of this amplifier is adjusted by the voltage difference between V_{BGP} and V_{RF2}. The clock frequency (clkr) of VCO is controlled by vctrl, and the used VCO circuit is shown in Fig. 3.18. When V_{DDH} < 8.4 V, it means V_{RF2} < V_{BGP}, so the frequency of clkr will arise until V_{DDH} > 8.4 V; and when V_{DDH} > 8.4, it means V_{RF2} > V_{BGP}, so the frequency of clkr will decrease until V_{DDH} < 8.4. V_{DDH} can be regulated almost at the voltage level 8.4 V.

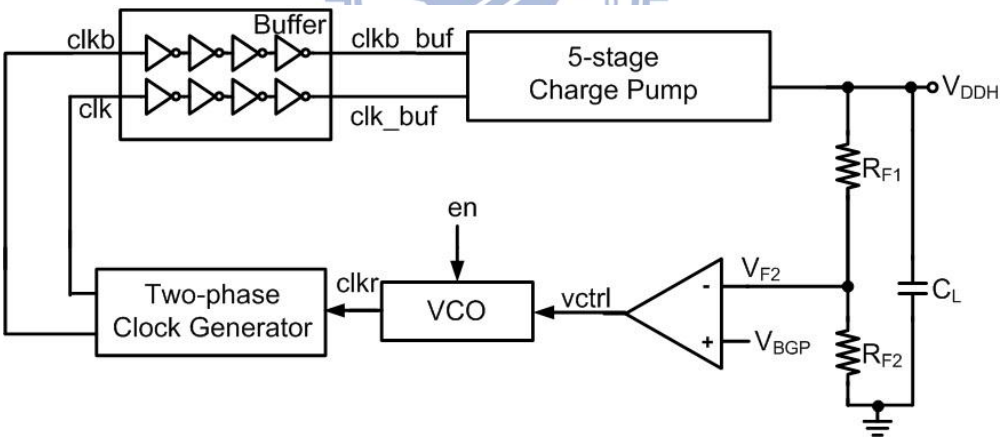


Fig. 3.14. The architecture of the proposed high voltage generator.

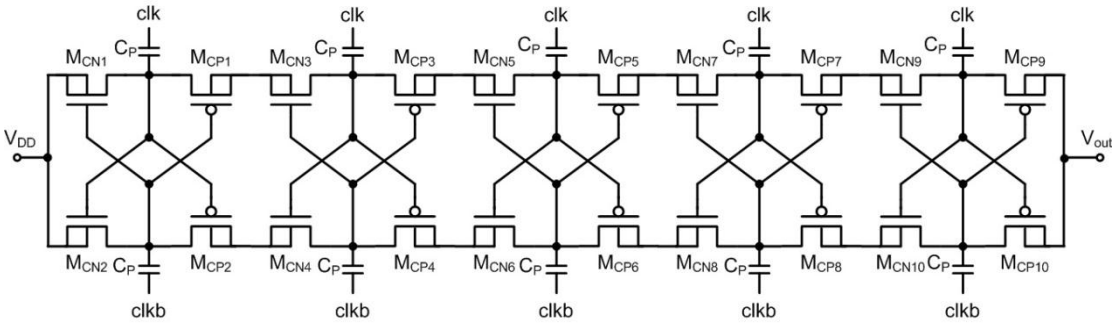


Fig. 3.15. The used 5-stage charge pump circuit.

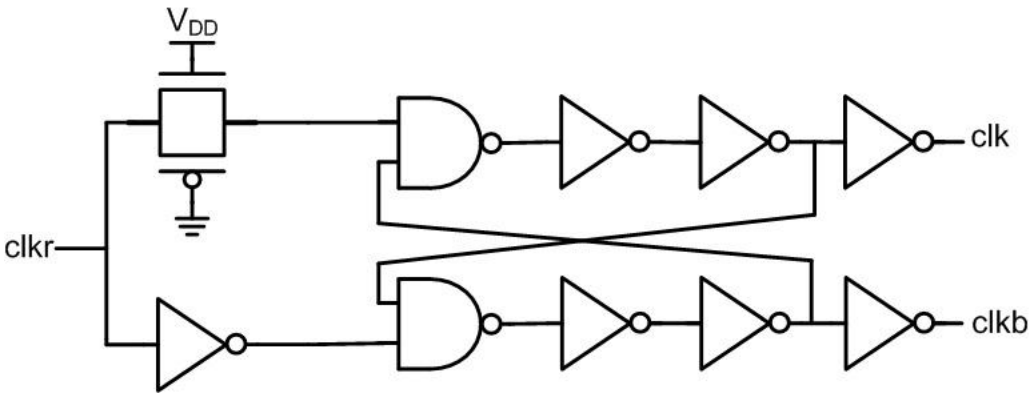


Fig. 3.16. Non-overlap two-phase clock generator.

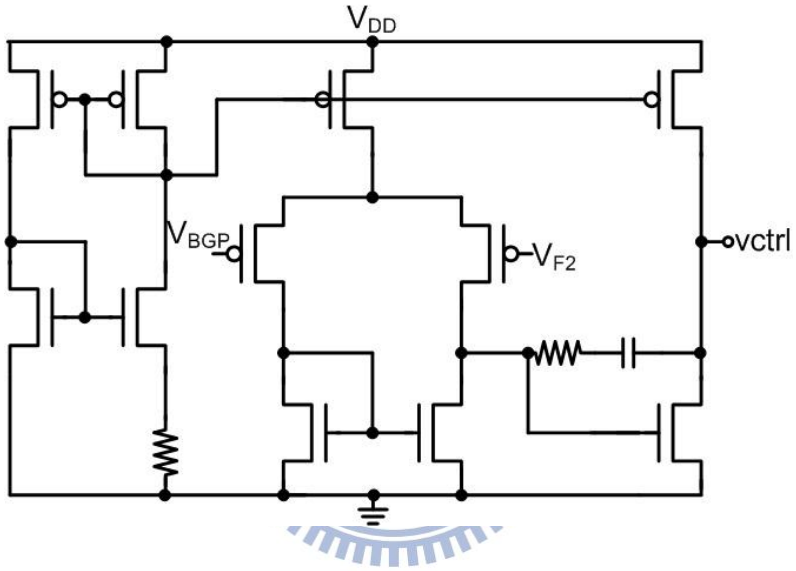


Fig. 3.17. Two-stage amplifier.

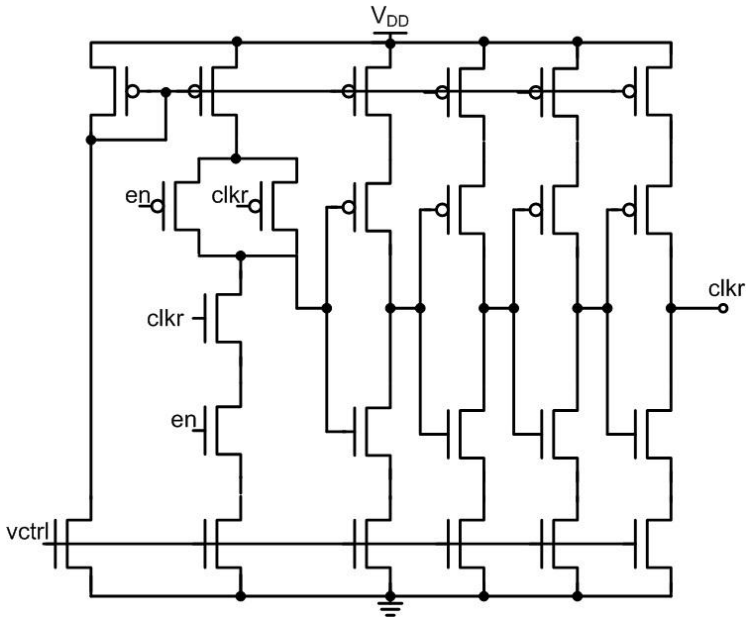


Fig. 3.18. The used voltage controlled oscillator.

3.4 Simulation and Measurement Results

3.4.1 Simulation Results

The proposed stimulator had been simulated in HSPICE with TSMC 0.18-μm 1.8-V/3.3-V CMOS process. Fig. 3.18 shows the simulated frequency response of the stimulus driver circuit, and the loading impedance at V_{OUTP} is a 150-pF capacitor. From the waveforms of the gain and phase, it can be observed that there are two poles and one zero below the frequency of 1 MHz. It is consistent with the description of the stimulus drive circuit in chapter 3.3.3, one pole is at V_{OUTP}, another pole is at V_{OPOUT}, and one zero is at V_{OPOUT} to compensate one pole for enhancing phase margin. It can also be observed that the phase margin is still positive before gain decreasing to 0 dB, so the whole loop of the stimulus driver circuit will be stable. The loop gain of the stimulus driver circuit is 57 dB, and the phase margin is 50 degrees.

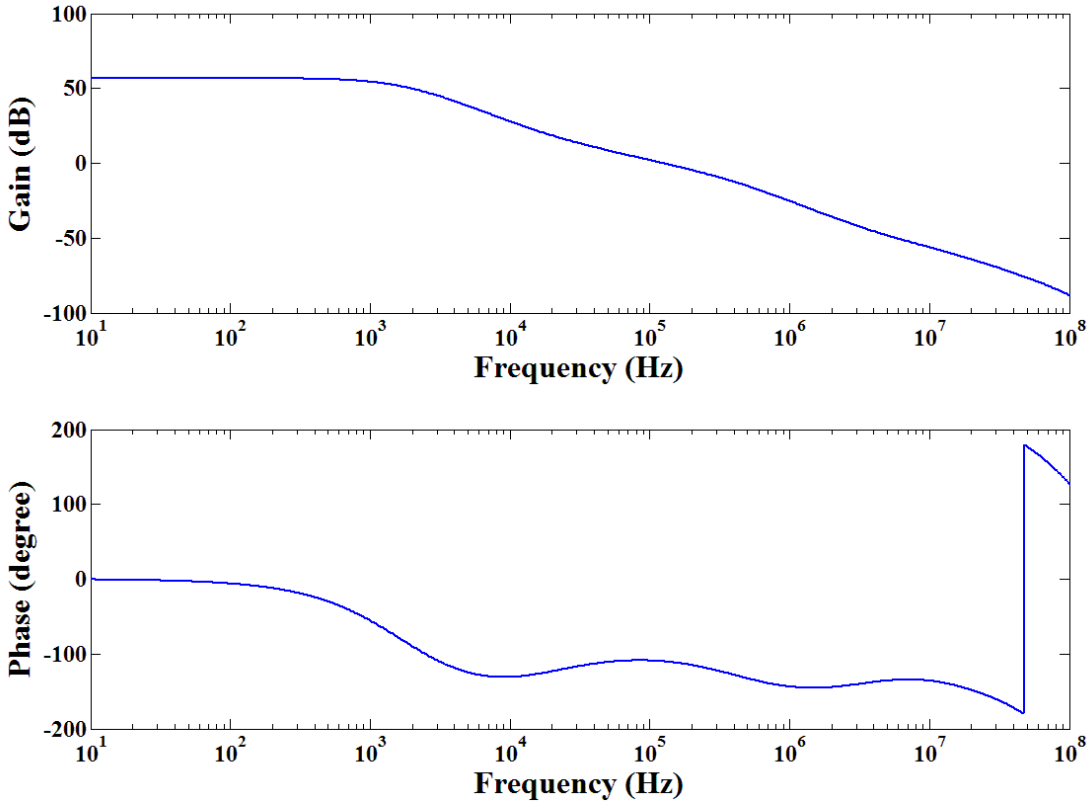


Fig. 3.19. Frequency response of the stimulus driver circuit.

The simulated waveforms of V_{DDH} and control signal (en) are shown in Fig. 3.20. During 0-2 µs, the stimulator is not in stimulation, the en signal is at logic low, so V_{DDH} is almost at 0 V for reducing the standby power consumption of the stimulator. During 2-10 µs, the stimulator is in stimulation, the en signal will be logic high, and V_{DDH} will be pumped to higher voltage level, and finally V_{DDH} will be regulated at 8.4 V. The maximum loading current of the proposed high voltage generator is 600 µA. Under the maximum loading current 600 µA, the power efficiency of the high voltage generator calculated according to [34] is ~ 52%.

Fig. 3.21 shows the waveform of Vstim of one output channel, the loading impedance between V_{OUTP} and V_{OUTN} is a 150-pF capacitor. During 1.1-1.9 ms, there are totally eight stimulation periods, 3-bit amp signal is from logic 000 to logic 111 in sequence in these eight stimulation periods. Every stimulation period is 100 µs, the pulse width of Vano and Vcath is 40 µs, and the interphase delay between Vano and Vcath is 10 µs. As shown in Fig. 3.21, the stimulus voltage Vstim is from biphasic 0 V to biphasic 7 V in sequence, so our stimulator can deliver adjustable stimulus voltage according to the controls signals Vano, Vcath, and 3-bit amp.

Fig. 3.22(a) and Fig. 3.22(b) show all the nodes in the output stage of the stimulus driver circuit. There are seven stimulation periods in the waveforms, each stimulation period is 100 µs, the pulse width of Vano and Vcath is 40 µs, and 3-bit amp signal is from logic 000 to logic 111. As shown Fig. 3.22(a) and Fig. 3.22(b), it is obvious that V_{OUTP} varies from 0 V to 7 V, and no matter V_{OTUP} at which voltage level, gate-to-source, gate-to-drain, and drain-to-source voltages of all the I/O transistors in the output stage are smaller than the tolerant voltage 3.3 V. So the proposed stimulator can deliver high stimulus voltage without electrical overstress and gate-oxide reliability.

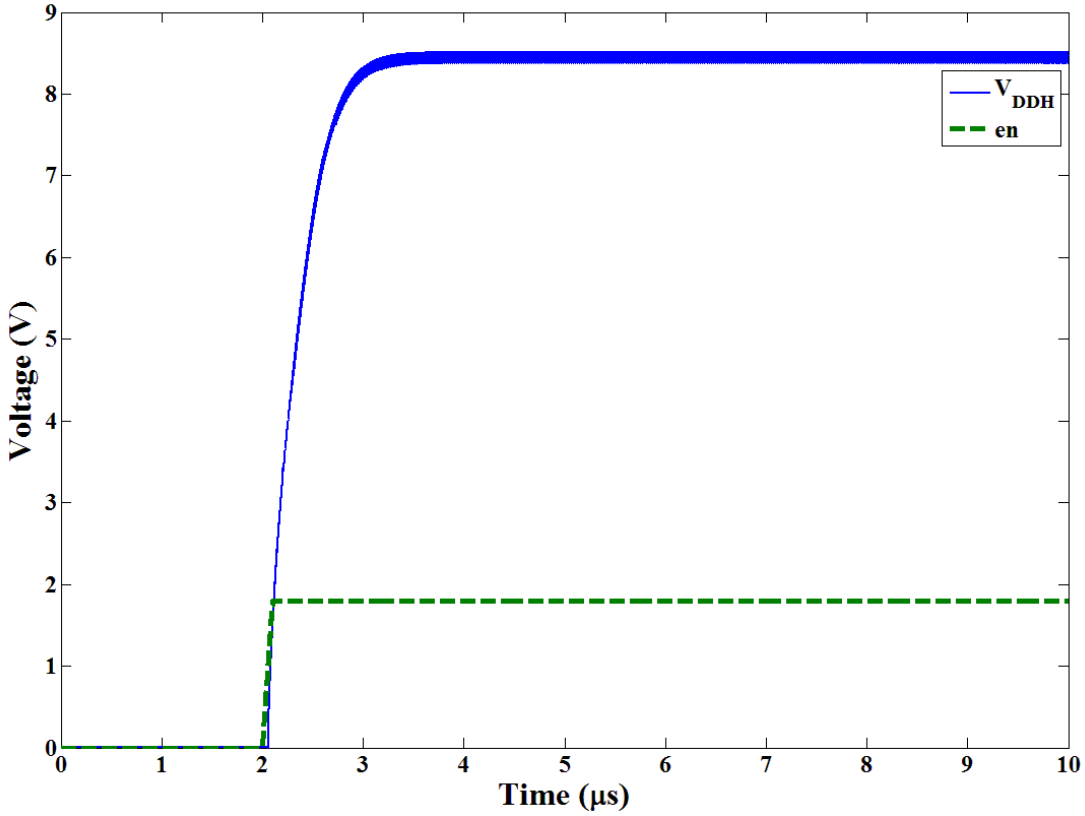


Fig. 3.20. Simulated voltage waveform of V_{DDH} and en.

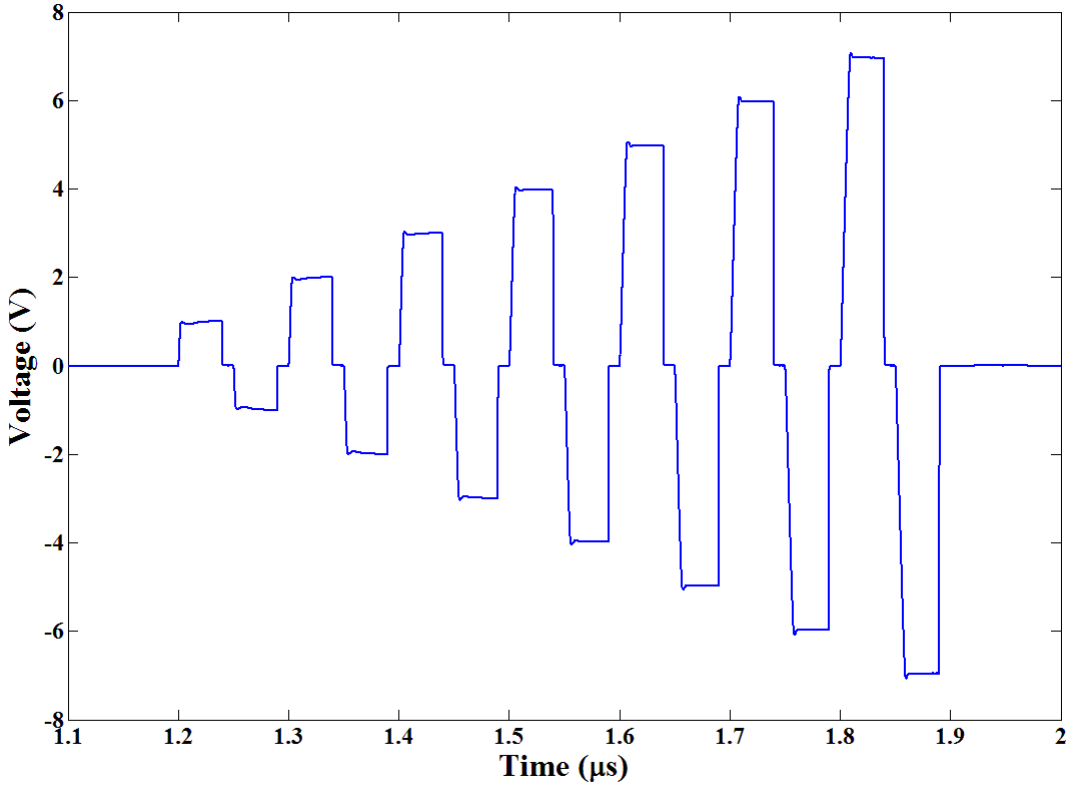
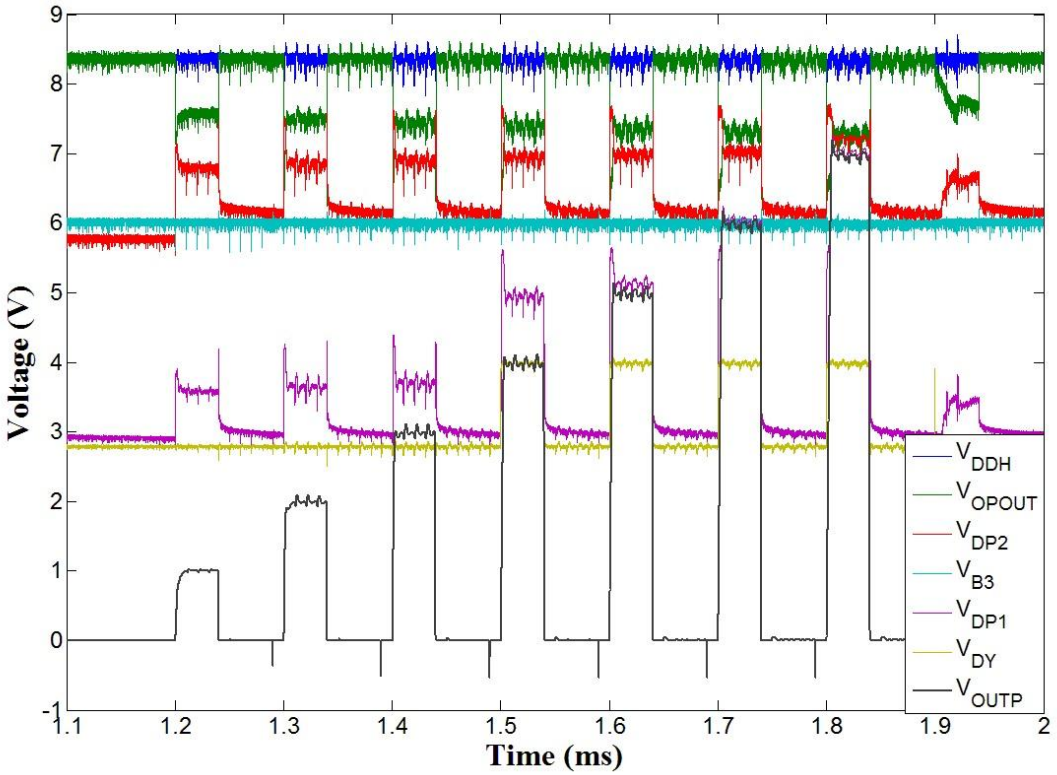
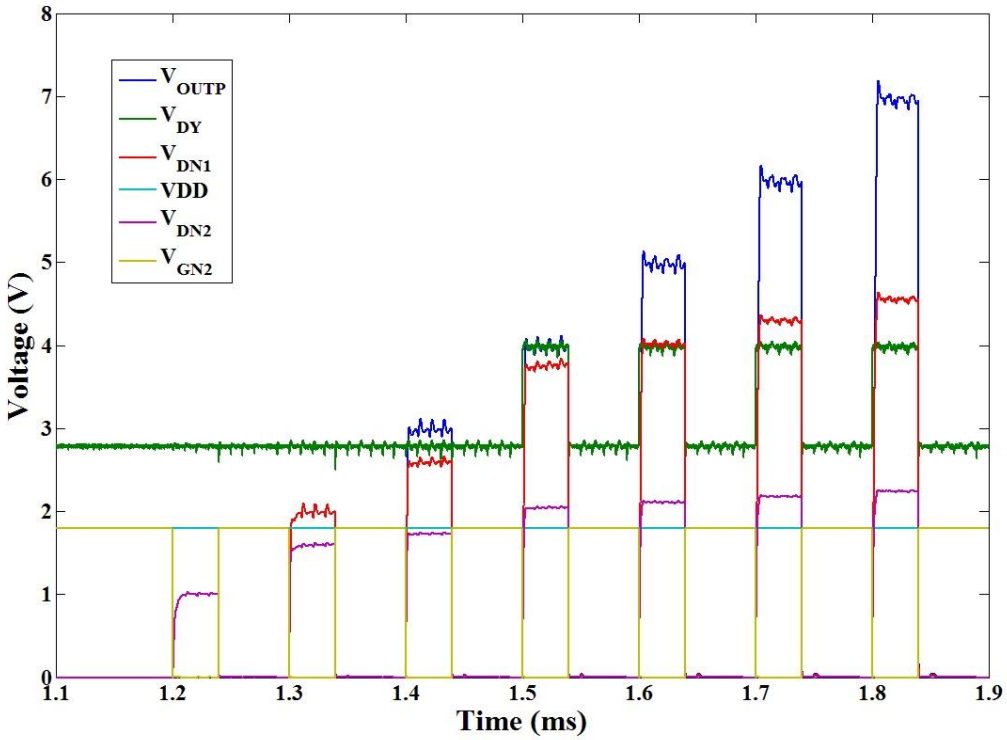


Fig.3.21. Simulated output waveform of one output channel.



(a)



(b)

Fig. 3.22. Simulated voltage waveform of the output stage of the stimulus driver circuit, all node voltages of PMOS and NMOS are separately shown in (a) and (b).

3.4.2 Measurement Results

The proposed high-voltage-tolerance stimulator for cochlear implant SoC had been fabricated in TSMC 0.18-μm 1.8-V/3.3-V CMOS process. The microphotograph of the fabricated chip is shown in Fig. 3.23, which includes four output channels (Ch1, Ch2, Ch3, and Ch4), a voltage reference, VDAC, and a high voltage generator, and total area is 1.167 × 1.648 mm^2. The chip had been assembled in package for measurement.

Fig. 3.24(a) show the measurement setup, Keithley 2410 is used to provide the fixed 1.8-V voltage V_{DD}, and it is also used to measure power consumption of the stimulator. Agilent 81110A is used to provide two non-overlap control signals Vano and Vcath. Agilent DSOX3034A is used to observe the waveforms of the stimulus voltage and V_{DDH}. The measurement environment is shown in 3.24(b).

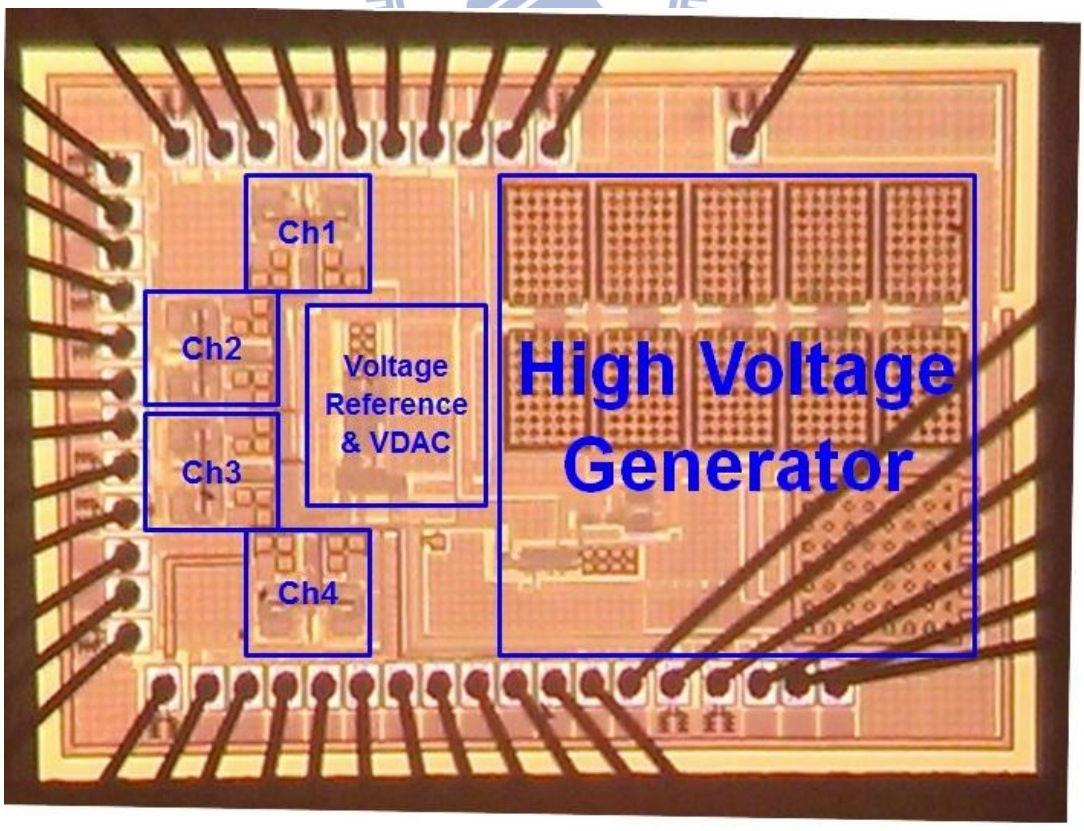
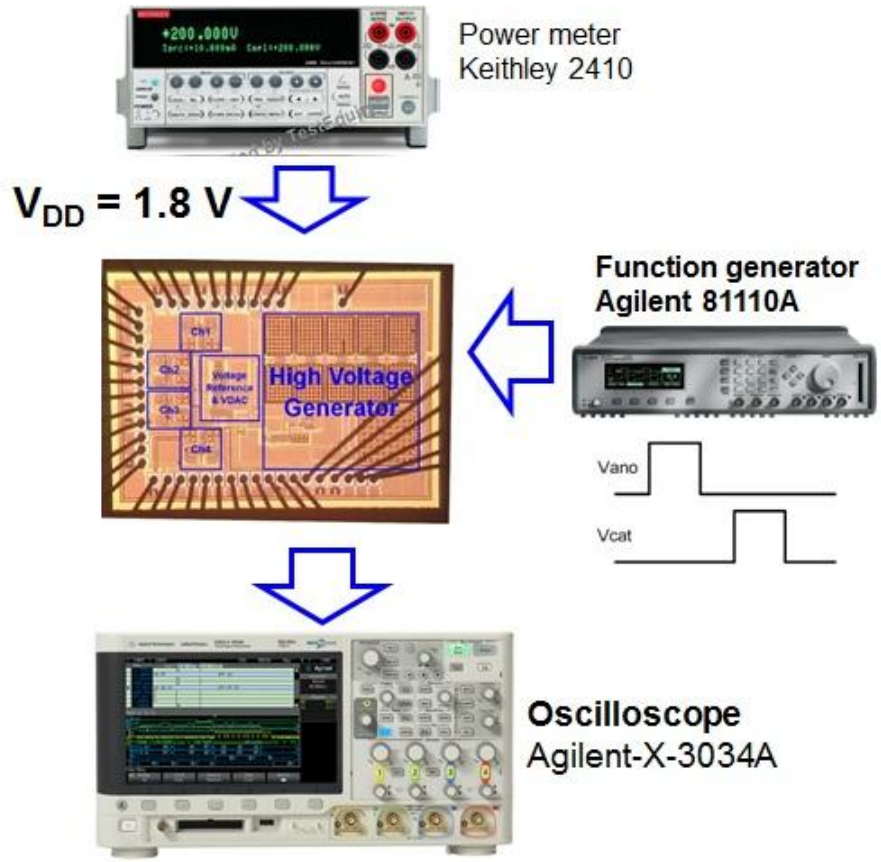


Fig. 3.23. The microphotograph of the fabricated stimulator chip.



(a)

(b)

Fig. 3.24. The measurement setup of the power meter, the function generator, the oscilloscope, and the chip is shown in (a). The measurement environment is shown in (b). The outputs of the stimulator are connected to test electrode-tissue equivalent circuit.

V_{DDH} is generated by the high voltage generator, and it is the needed high supply voltage for the stimulator. The waveform of V_{DDH} is measured in Fig. 3.25, and it can be observed that V_{DDH} can be regulated at 8.24 V. The power meter Keithley 2410 is used to measure power consumption of the high voltage generator, and the oscilloscope Agilent DSOX3034A is used to measure power consumption at output V_{DDH}. The power efficiency is calculated as Eg. (3-3), and the power efficiency under different loading current is shown in Fig. 3.26.

$$\text{Power Efficiency} = \frac{P_{OUT}}{P_{IN}} = \frac{V_{DDH} \times I_{LOAD}}{V_{DD} \times I_{IN}} \qquad (3\text{-}2)$$

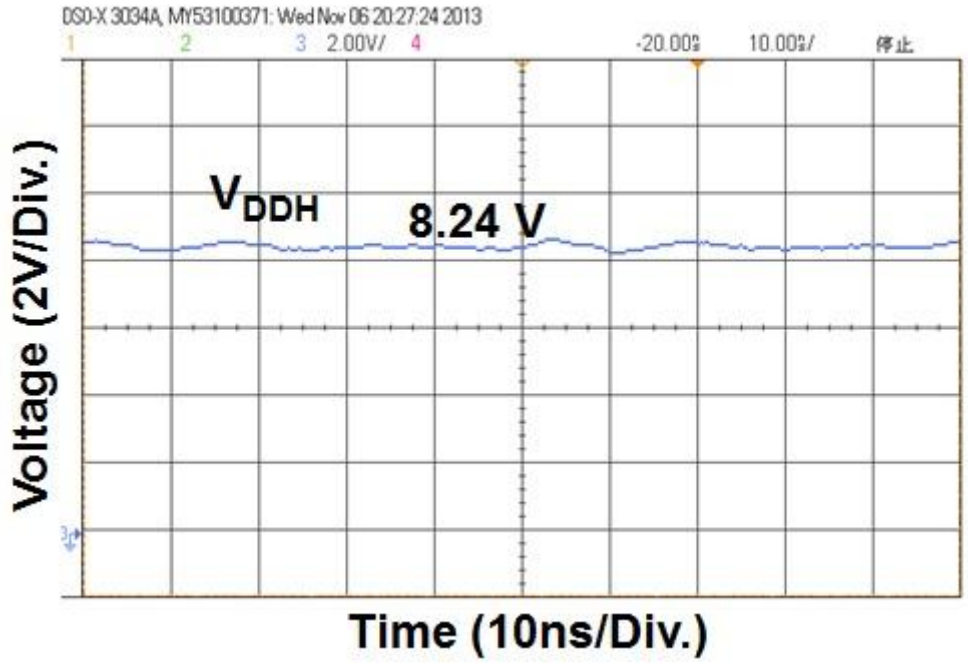


Fig. 3.25. The output voltage V_{DDH} of the proposed high voltage generator when the stimulator is in stimulation (control signal en is logic 1).

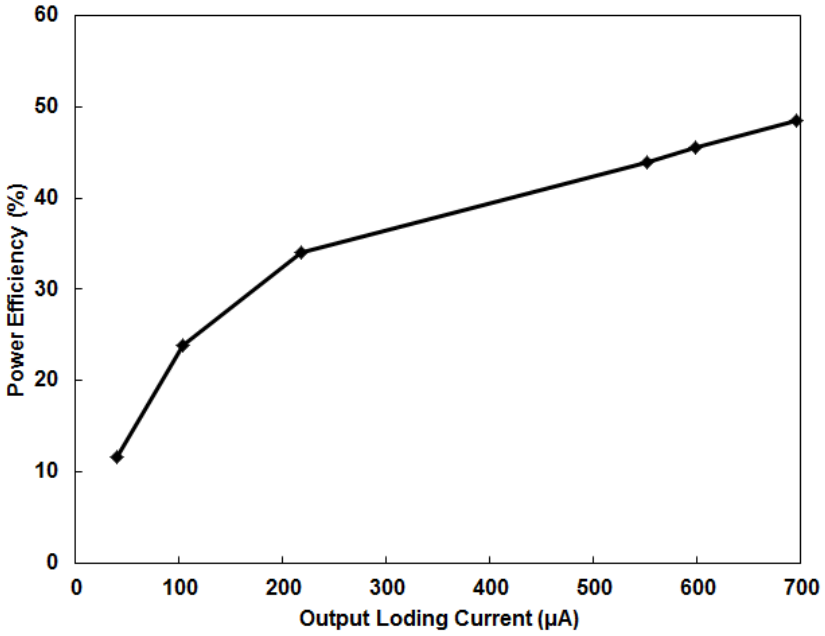


Fig. 3.26. The measured power efficiency under different loading current.

The whole stimulator has four output channels, so it can output four-channel stimulus voltages at four different positions of the cochlea at the same time. 3-bit amp signal, pulse width of Vano and Vcah are used to adjust the amplitude, polarity, and pulse width of the stimulus voltage (Vstim) on the loading impedance. So, the output from the proposed stimulator is adjustable, it can cover some range of the picked sound.

When the 3-bit amp signal is set to logic 111, the pulse width of Vano signal and Vcah signal is set to 1 ms, and the interphase delay between them is set to 0.25 ms. With such a control setting, the biphasic stimulus voltage waveform is measured in Fig. 3.27. When the 3-bit amp signal is set to logic 011, the pulse width of Vano signal and Vcath signal is set to 100 μs, and the interphase delay between them is set to 25 μs. Under such setting, the biphasic stimulus voltage waveform is shown in Fig. 3.28. As verified in Fig. 3.27 and Fig. 3.28, the pulse width and amplitude of biphasic stimulus voltage are adjustable. Fig. 3.29 shows this stimulator can deliver four channels of different stimulus voltages, simultaneously.

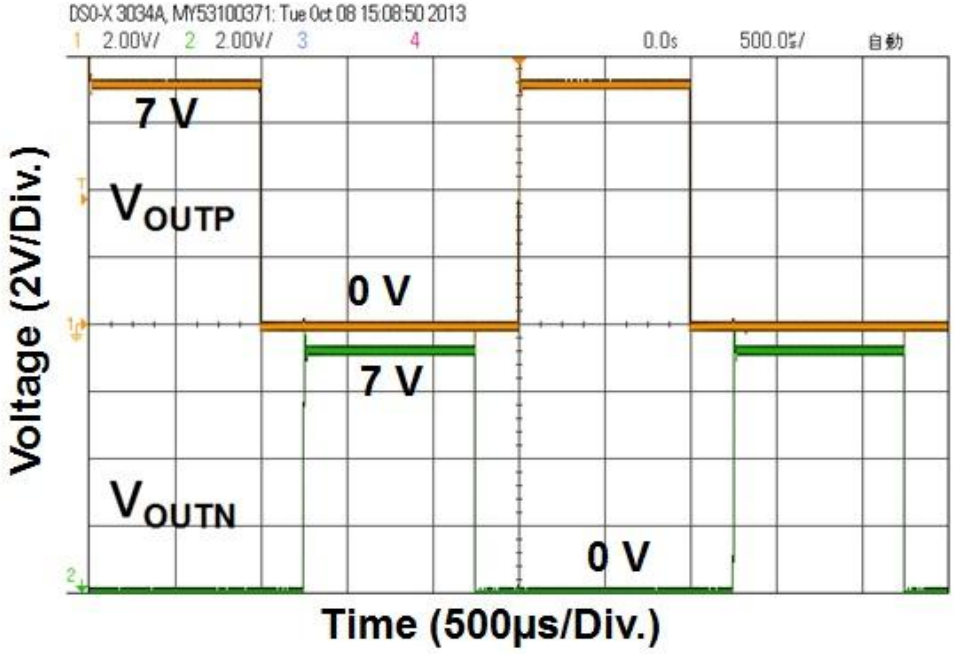


Fig. 3.27. When the 3-bit amp signal is set to logic 111, the stimulus voltage has the voltage magnitude of 7 V and pulse width controlled by Vano and Vcath is set to 1 ms.

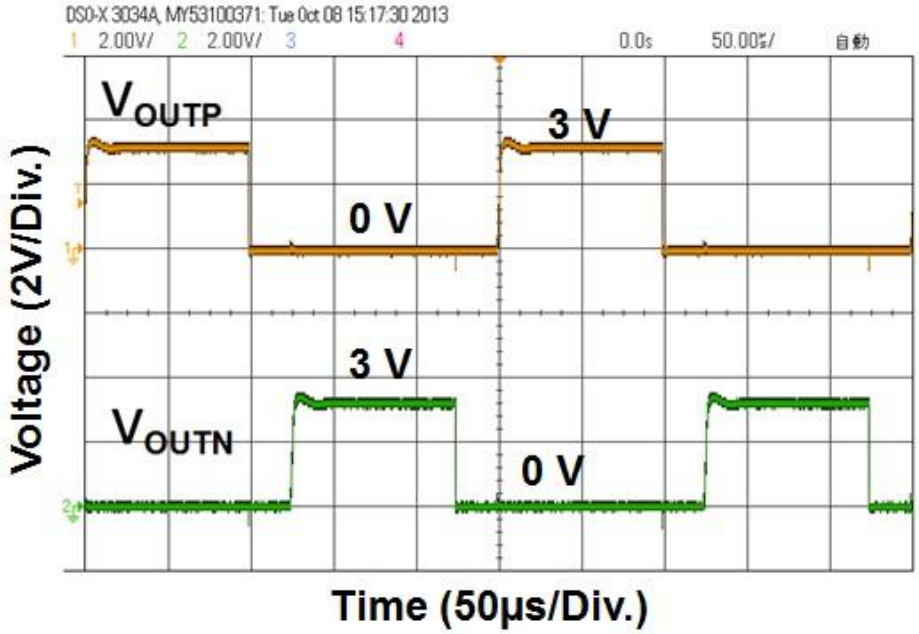


Fig. 3.28. When the 3-bit amp signal is set to logic 011, the stimulus voltage has the voltage magnitude of 3 V and pulse width controlled by Vano and Vcath is set to 100 µs.

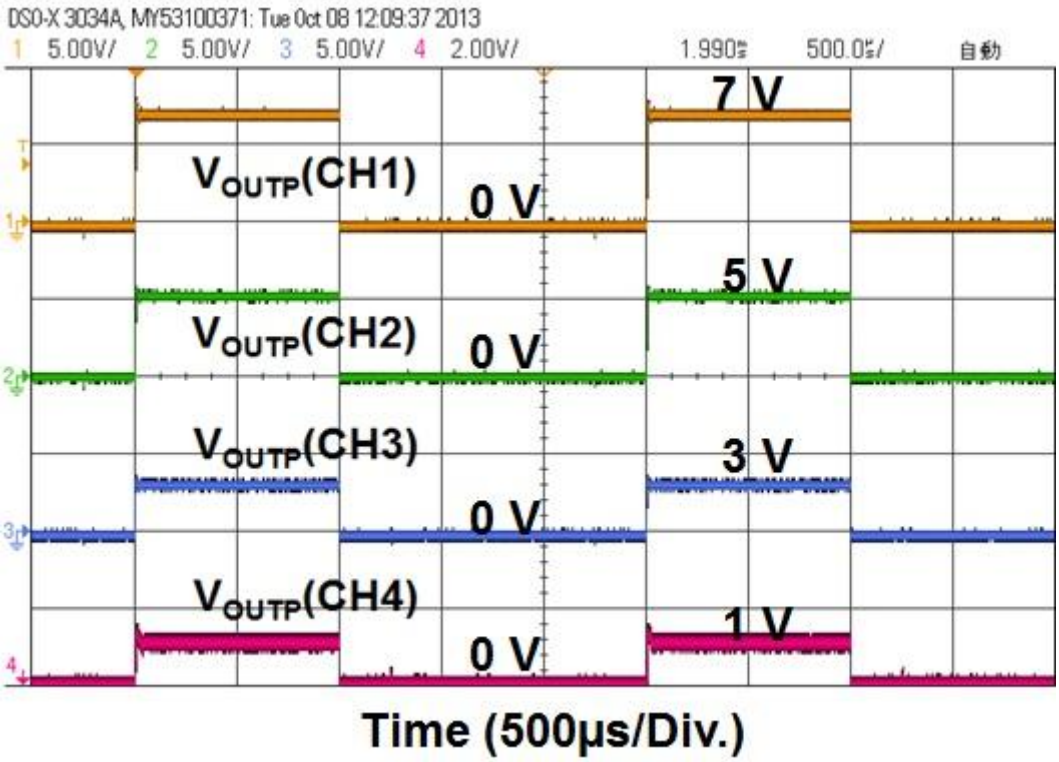


Fig. 3.28. The stimulator can simultaneously deliver four channels of different stimulus voltages, V_{OUTP} (7 V, 5 V, 3 V, and 1 V), under the pulse width of 1 ms.

The proposed design would provide the stimulus voltage at V_{OUTP} and V_{OUTN} of one output channel as shown in Fig. 3.5. The ideal stimulus voltage is shown in Table 3.2, and the voltage difference between the ideal stimulus voltage and the measurement results of stimulus voltage at V_{OUTP} and V_{OUTN} under 4 different chips and 3-bit amp signal is as shown in Fig. 3.30. The measurement results of the relative voltage mismatch between V_{OUTP} and V_{OUTN} of one output channel under different 4 chips and 3-bit amp signal is as shown in Fig. 3.31.

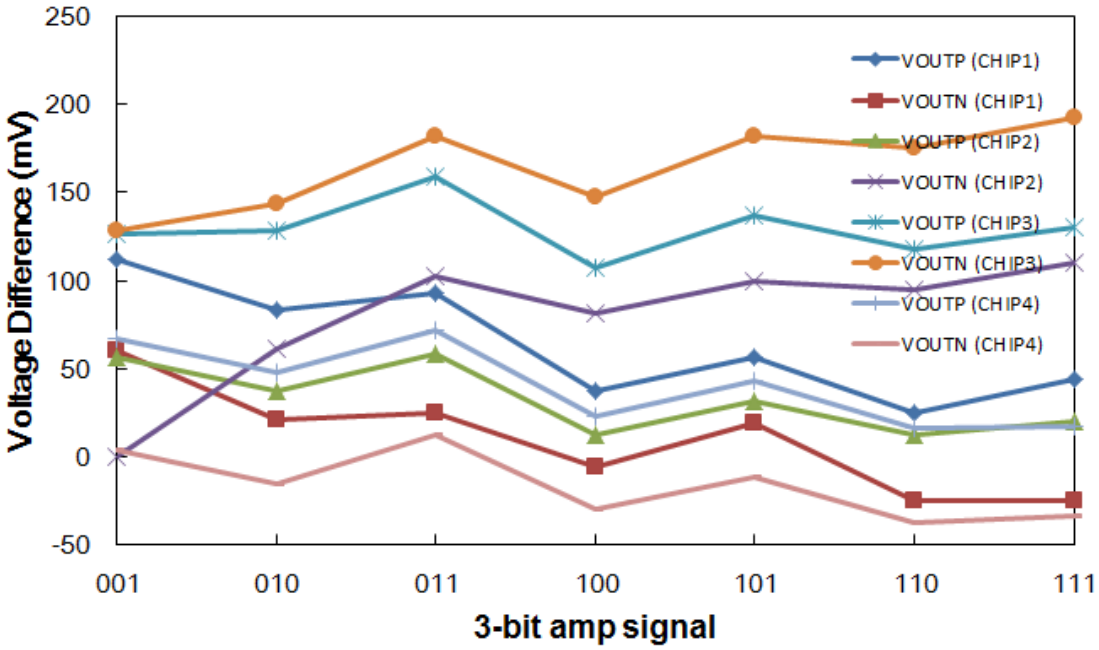


Fig. 3.30. The voltage difference between the ideal stimulus voltage and measured stimulus voltages under 4 different chips and 3-bit amp signals.

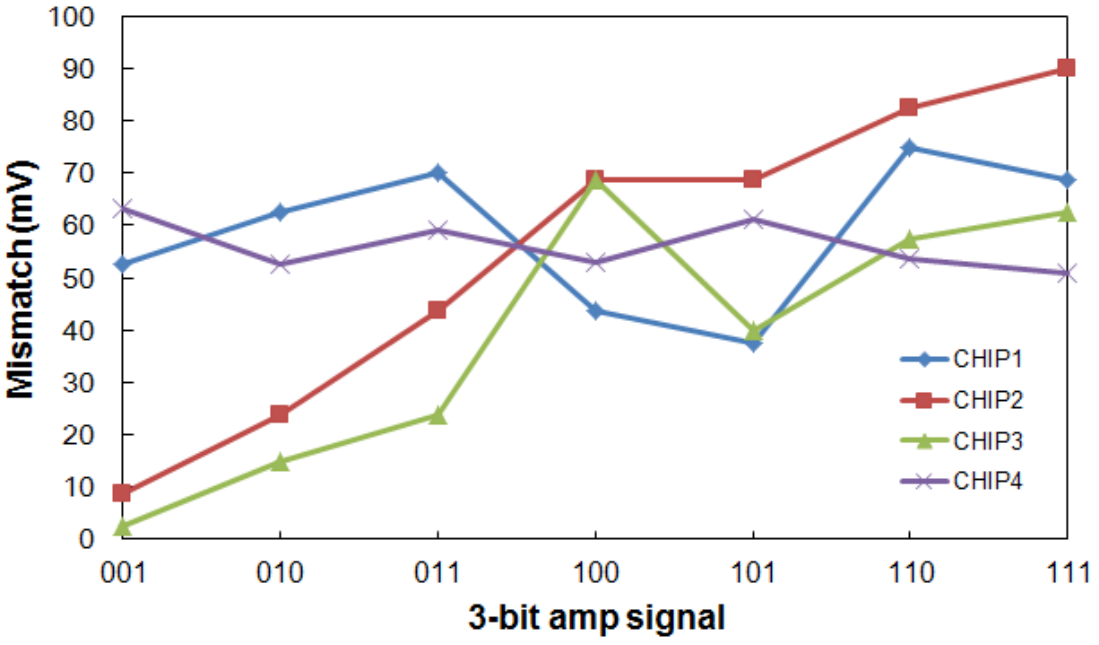


Fig. 3.31. The voltage mismatch between V_{OUTP} and V_{OTUN} of one output channel under 4 different chips and 3-bit amp signals.

The long-term measurement is used to verify the reliability of the stimulator chip. The stimulator continuously delivers four-channel stimulus voltages as shown in Fig. 3.28, and voltage level of each channel stimulus voltage is measured every day. The relationship between four-channel stimulus voltages and chip operation time is shown in Fig. 3.32, and initial measured voltage level of stimulus voltage is as reference voltage level, and long-term measured stimulus voltage level minus reference voltage level is as voltage variation. The relationship between voltage variation and chip operation time is shown in Fig. 3.33, and it can be observed that the trend of voltage variation of each output channel does not increase or decrease obviously, and voltage variations are always within 30 mV. Although everyday measured voltage level of stimulus voltage may change, but that is because the ripple of V_{DDH} can slightly influence stimulus voltages, and according to the opinion of biomedical group in this cochlear implant project, it is acceptable. So the reliability of our stimulator chip is verified in the long-term measurement.

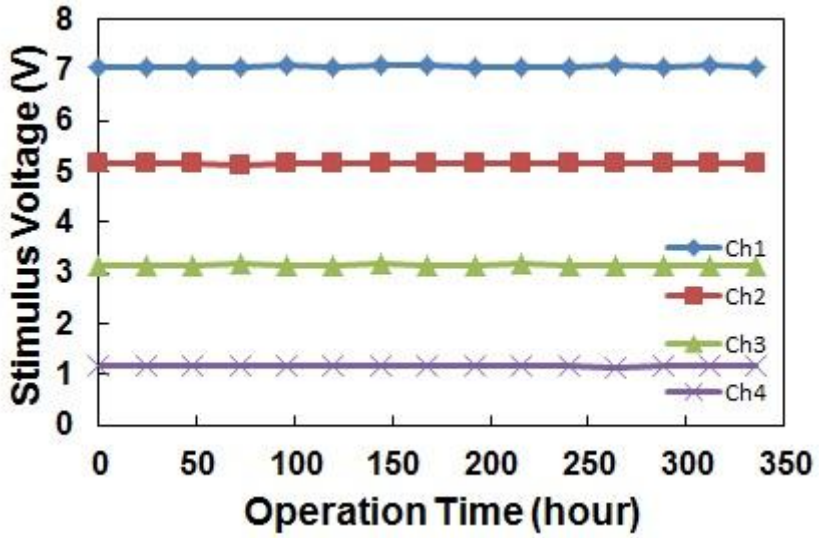


Fig. 3.32. Measured four-channel stimulus voltages under different chip operation time.

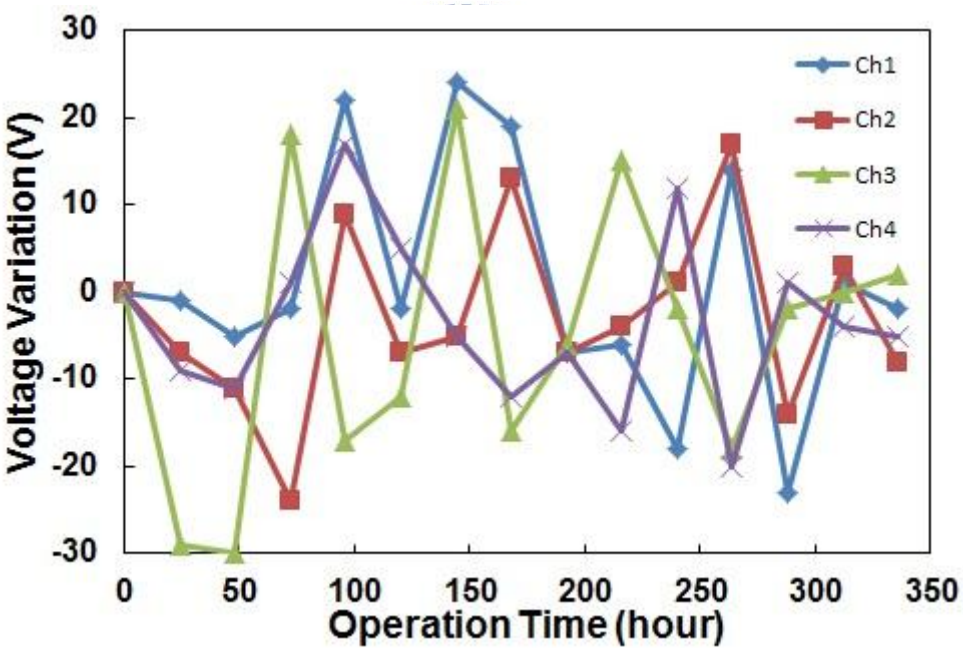


Fig. 3.33. Measured four-channel voltage variations under different chip operation time.

Table 3.3. Summary of the high voltage generator.

	Specification	Simulation	Measurement Results
V_{DD}	1.8 V	1.8 V	1.8 V
V_{DDH}	8.4 V	8.4 V	8.24 V
Imax	> 600 μA	800 μA	700 μA
Load Regulation	minimum	0.27 mV/μA	0.37 mV/μA
Power Efficiency	Maximum	53.0 %	45.5 %

Table 3.4. Summary of the stimulator.

	Specification	Simulation	Measurement Results
Power Supply V_{DD} (V)	1.8	1.8	1.8
V_{DDH} (V)	8.4	8.4	8.24 (CHIP1)
Output Stimulus Voltage Amplitude (V)	±1, ±2, ±3, ±4, ±5, ±6, ±7,	±1, ±2, ±3, ±4, ±5, ±6, ±7,	1.110,-1.060, 2.084,-2.021, 3.093,-3.055, 4.038,-3.990, 5.056, -5.019, 6.025,-5.975, 7.044,-6.975, (CHIP1)
Voltage Mismatch (V)	minimum	~0 depend on the process mismatch	< 90 mV
Standby Power (μW)	minimum	566	694.8
Power Consumption of Each Channel (±7 V, 1-ms pulse width)	minimum	345	270
Process	TSMC 0.18μm 1.8-V/3.3-V CMOS Process		

3.5 Summary

Design of a bipolar biphasic stimulator for cochlear implant with high-voltage-tolerant consideration is investigated and verified in this chapter. The proposed design had been fabricated in TSMC 0.18-μm 1.8-V/3.3-V CMOS process, because the maximum output voltage is as high as 7 V, so dynamic bias technique and stacked MOS configuration are proposed to avoid the issues of electrical overstress and gate-oxide reliability. This design consists of a high voltage generator, a voltage reference, and four output channels, the high voltage generator is used to pump low supply voltage V_{DD} (1.8 V) to higher supply voltage V_{DDH} (8.4 V), thus only one supply voltage is needed. The pulse width and amplitude of the biphasic stimulus voltage can be adjusted by Vano signal, Vcath signal, and 3-bit amp signal. Finally the functions of this stimulator design had been successfully verified in silicon chip, which can successfully deliver the required adjustable stimulus voltage to the output load.

Chapter 4
Conclusions and Future Works

4.1Conclusions

Our biomedical group in this cochlear implant project had proposed new type of electrodes, and based on these proposed electrodes, the auditory nerve in the cochlea has to be stimulated by stimulus voltages. But traditional stimulators for medical application usually deliver stimulus current, so for this cochlear implant, a stimulator with multi-channels, voltage mode, biphasic stimulation, and bipolar fashion is proposed by our group. Before designing the stimulator, impedance data of the cochlea with implanted electrodes are measured, and these impedance data have been analyzed and calculated into a circuit model for the convenience of simulation and measurement.

To be integrated into SoC with other sub-circuits of the cochlear implant, this work had been fabricated in TSMC 0.18-μm 1.8-V/3.3-V CMOS process, and the total chip area is 1.167 mm × 1.648 mm, and the cochlear implant is an implant device, so it can only be powered by wirelessly transmission from the external part, only one supply voltage of 1.8 V can be used in the cochlear implant. The proposed high-voltage-tolerant stimulator consists of four output channels, a voltage reference, and an on-chip high voltage generator. The stimulator has four output channels, so it can simultaneously deliver stimulus voltages to the auditory nerve at four different positions on the cochlea, and the on-chip high voltage generator can pump V_{DD} (1.8 V) to V_{DDH} (8.4 V). The maximum stimulus voltage is 7 V, but the tolerant voltage of the

transistor in this process is 3.3 V, so stacked MOS configuration and dynamic bias techniques are used to prevent the stimulator from the issues of gate-oxide reliability and electrical overstress. The functions of this stimulator design had been successfully verified in the silicon chip, which can successfully deliver the required adjustable stimulus voltage to the output load.

4.2 Future Works

4.2.1 Animal Experiment

Before the animal experiment, the auditory brainstem response (ABR) should be introduced firstly. Electrical activity in the brain can be recorded via electrodes placed on the scalp, and the ABR is an auditory evoked potential extracted from electrical activity in the brain. If the auditory nerve is stimulated by electrical pulse, then action potentials will start to convey from the auditory nerve to the brain, and wave I to wave V can be observed with action potentials conveying to ganglions at different positions.

The measurement setup of animal experiment is as shown in Fig. 4.1. The surgery was executed by the doctor, a pair of electrodes placed on the cochlea of a guinea pig, electrodes for recording electrical activity in the brain are placed on the scalp of the guinea pig, and ABR is extracted from electrical activity in the brain by computer. Electrodes on the cochlea of the guinea pig are connected to a function generator, and stimmulus voltages from the function generator are send to the cochlea via implanted electrodes to stimulate the auditory nerve. As shown in Fig. 4.1, the wave V can be observed in the ABR, so the auditory nerve can be successfully stimulated and successfully conveyed to the brain.

In the future, the function generator will be replaced by stimulator of our design, as shown in Fig. 4.2. Firstly, we have to make sure that the stimulator can successfully deliver biphasic stimulus voltage to the cochlea via implanted electrodes. And the ABR will be observed to make sure that the auditory nerve can be successfully by our stimulator.

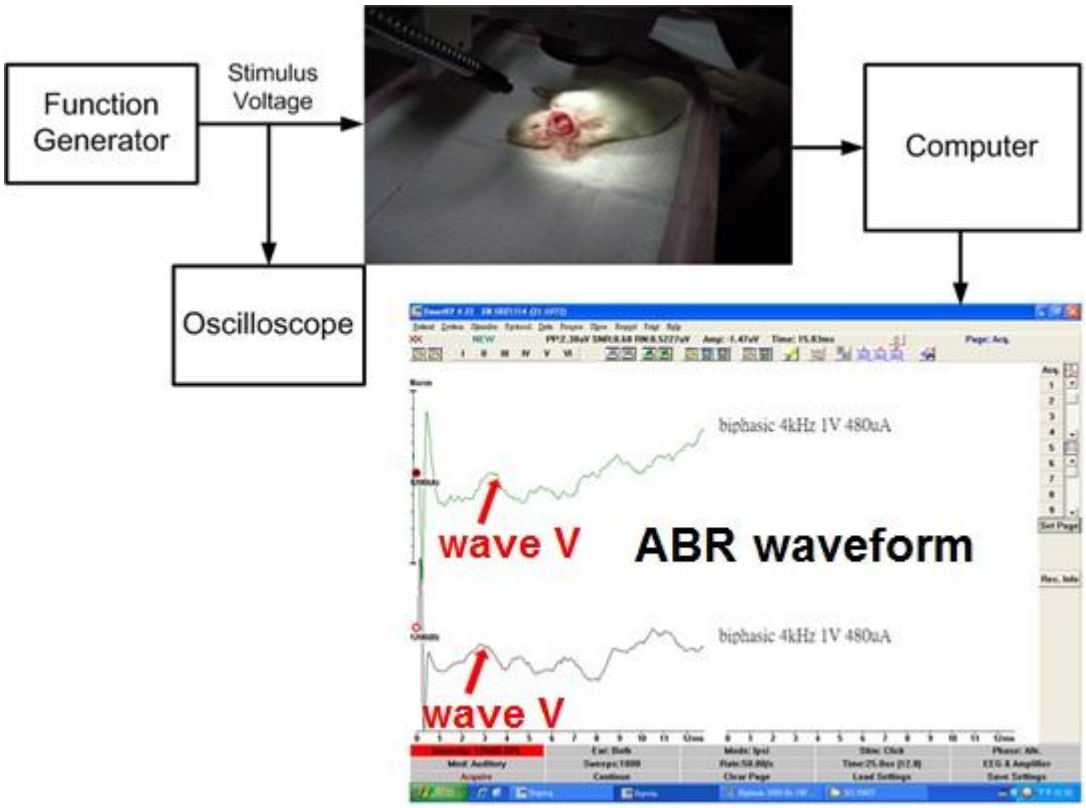


Fig. 4.1. The measurement setup of animal experiment, function generator is used to deliver stimulus voltage to cochlea via implanted electrodes, and auditory brainstem response can be extracted from electrical activity in the brain by the computer.

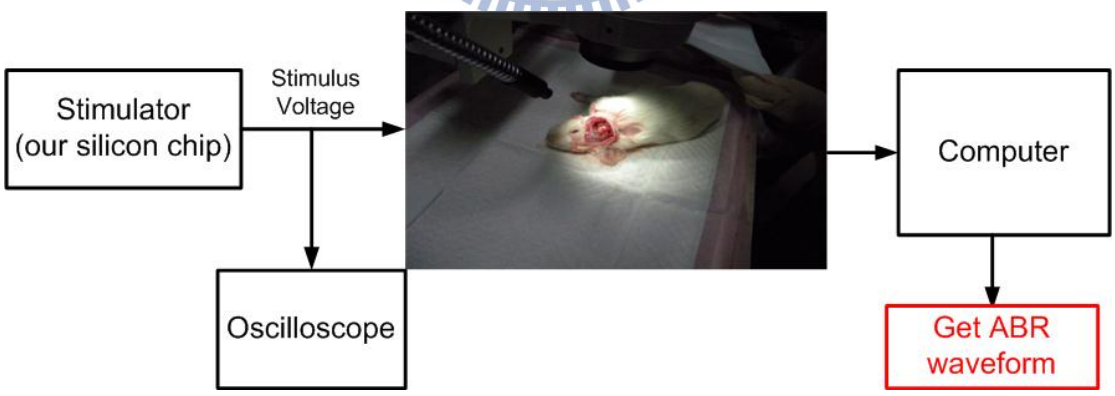


Fig. 4.2. The measurement setup of animal experiment, stimulator is used to deliver stimulus voltage to cochlea via implanted electrodes, and auditory brainstem response can be extracted from electrical activity in the brain by the computer.

4.2.2 SoC Integration of Implanted Part

The circuit blocks of our cochlear implant is shown in Fig. 4.3, and all the circuit blocks in the implanted part had been verified in silicon chips. To verify functions of SoC, all the circuit blocks in the implanted part should be integrated into a single chip. The single chip for the implanted part has a chip area of 2.07mm×2.03mm in TSMC 0.18-µm 1.8-V/3.3-V CMOS process, which had been taped out at 2013/12/18, and the chip layout is as shown in Fig. 4.4.

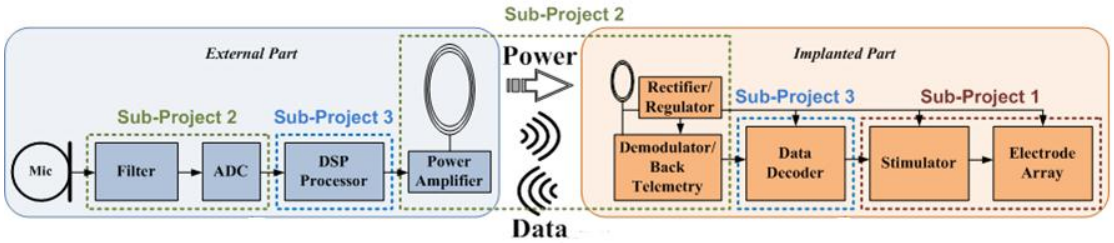


Fig. 4.3. Circuit blocks in the cochlear implant.

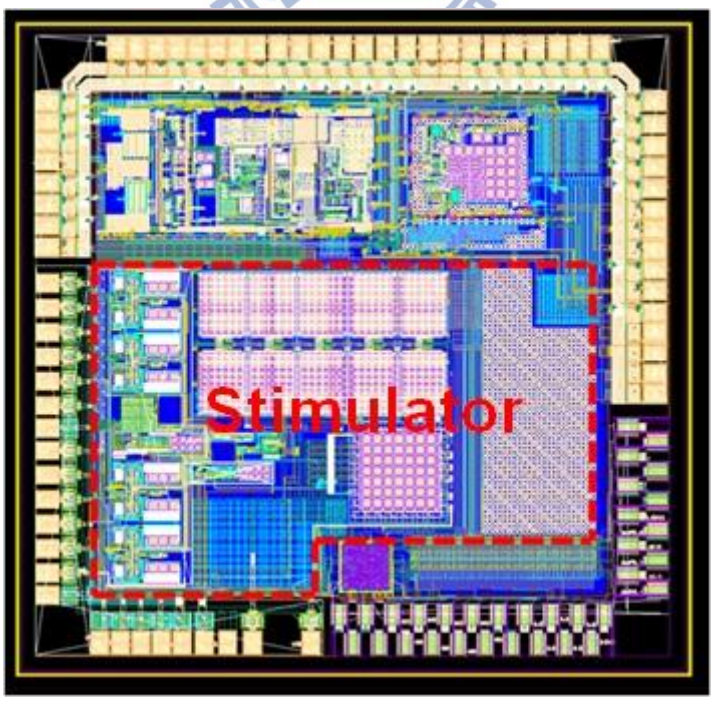


Fig. 4.4. Chip layout of the implanted part.

4.2.3 Dynamic Operating Voltage of Stimulator for Saving Power Consumption

The implantable device can only be powered by wirelessly transmission from the external part, so how to reduce power consumption becomes an important issue. Power consumption of the stimulator occupies most part of power consumption of the cochlear implant, so how to reduce power consumption of the stimulator becomes important. In original design, stimulus voltage of the stimulator is adjustable, amplitude of stimulus voltage is from 0 V to 7 V, and output voltage V_{DDH} of the on-chip high voltage generator is always at 8.4 V. But amplitude of stimulus voltage cannot always be at maximum amplitude 7 V, if V_{DDH} can be adjusted according to stimulus voltage, then the power consumption of implanted part can be significantly reduced.

Stimulus voltage of one output channel of the stimulator is controlled by 3-bit amp signal, Vano, and Vcath, and amplitude of V_{DDH} is regulated according to V_{BGP}. If V_{BGP} of voltage reference circuit can be adjusted by 3-bit amp signal, Vano, and Vcath, then V_{DDH} can be adjusted according to amplitude of stimulus voltage. The architecture of the stimulator with dynamic operating for saving power consumption is as shown in Fig. 4.5. Also, needed bias voltages from voltage reference circuit to output channels should be adjusted to the digit code, then the stimulator can prevent the stimulator from the issues of gate-oxide reliability and electrical overstress. The relationship between 3-bit amp signal and operating voltage is as shown in Fig. 4.6.

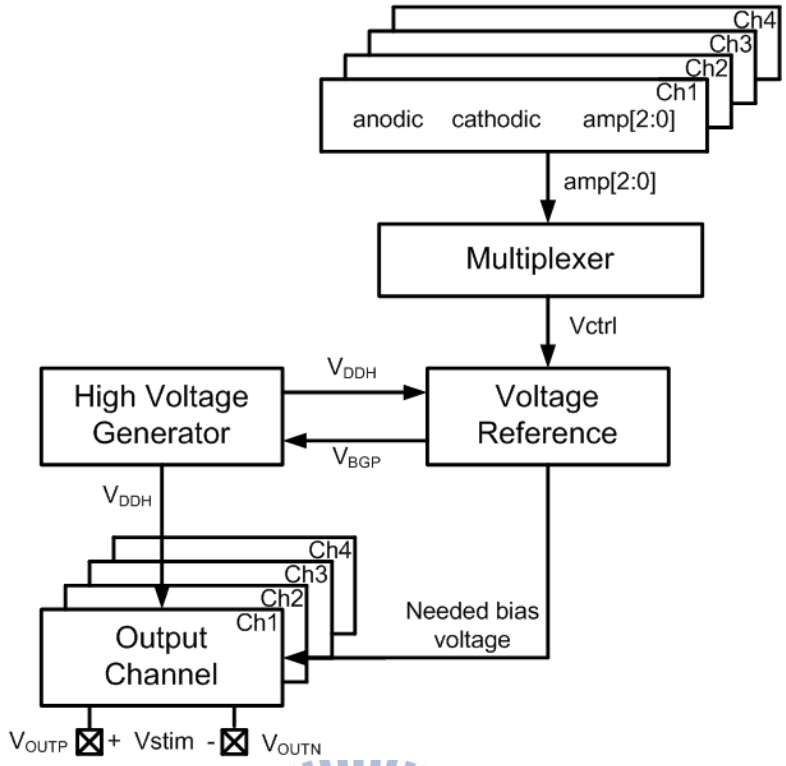


Fig. 4.5. The simulator with dynamic operating voltage for saving power.

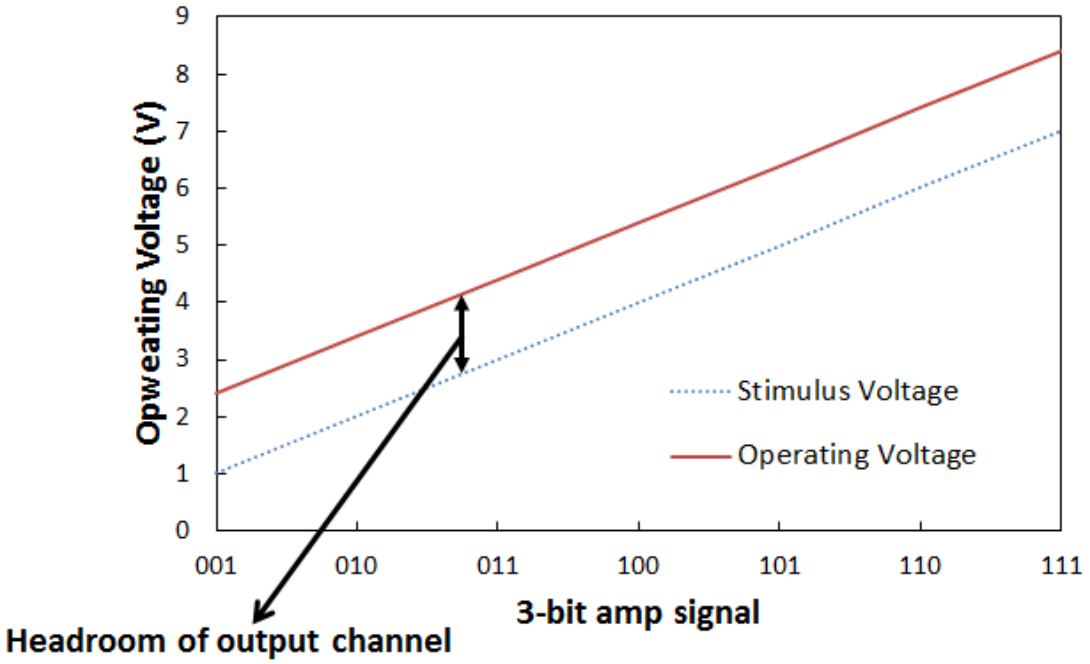


Fig.4.6. Output voltage of stimulator and required operating with different 3-bit amp signal.

4.2.4 Stimulator with Calibration Technique for Charge Balanced Stimulation

In FES, charge balanced stimulation is needed to prevent the tissue from harming. The proposed stimulator does not include the calibration circuit block, so the maximum relative mismatch between anodic and cathodic stimulus voltage is 90 mV, which is not tolerable. So the calibration circuit is needed, which is shown in Fig. 4.7. An amplifier is used to sense the voltage difference between V_{OUTP} and V_{OUTN}, and an output Vcal will be outputted from the amplifier according to the voltage difference. Also, an output Vshift will be outputted from level shifter according to Vcal, and this Vshift is added with V_{DAC} to change voltage level of V_{OUTP}. Finally, V_{OUTP} and V_{OUTN} will be almost at the same voltage level. Fig. 4.8 shows the mismatch of the stimulator with calibration and without calibration.

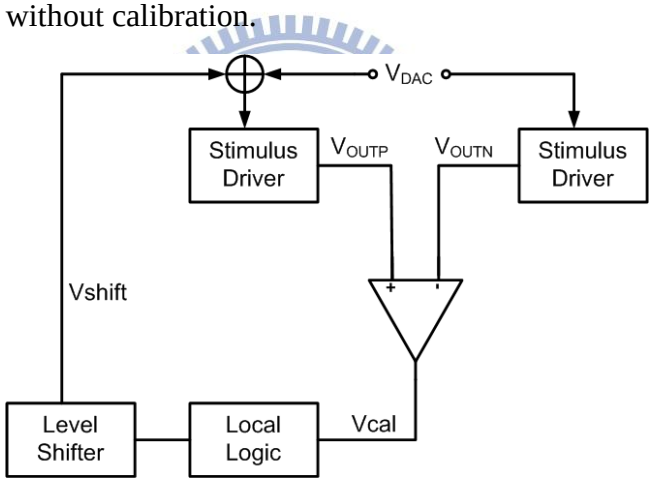


Fig. 4.7. The calibration method to match anodic and cathodic stimulus voltage.

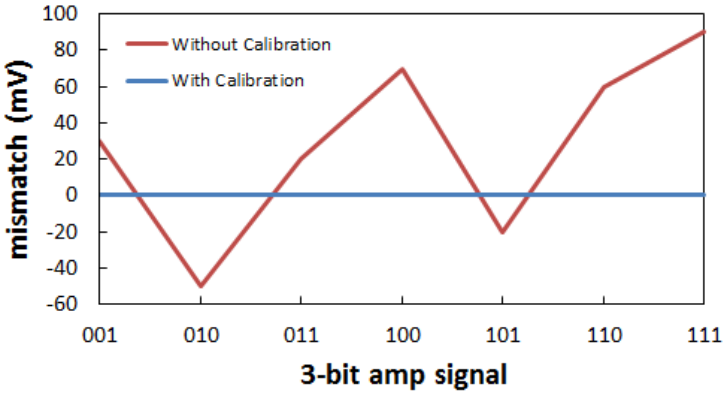


Fig. 4.8. The relative mismatch between anodic and cathodic stimulus voltage with calibration and without calibration.

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