國立交通大學

電子工程學系　電子研究所碩士班

碩　士　論　文

抑制癲癇發作之
十六通道雙向電流刺激器設計

Design of 16-Channel Biphasic Stimulus Driver to Suppress Epileptic Seizure in the Low Voltage Process

研 究 生：楊子毅　　(Tzu-Yi Yang)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國一○四年十月

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碩士論文

A Thesis
Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master of Science
in
Electronics Engineering
October 2015
Hsinchu, Taiwan

中華民國一○四年十月

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摘要

近年，電刺激技術已常用於醫療方面，如功能性電刺激 (Functional electrical stimulation)。透過電刺激的方式，刺激在患者異常的神經部位，可使患者恢復部分身體的機能。而隨著積體電路製程的發展，整合智慧型仿生系統於單晶片的目標已變得可行，結合微電子技術、醫學以及生物化學，可以製造應用於不同疾病醫療之生物晶片，例如癲癇晶片。

癲癇是種常見的神經疾病，發作源自於大腦某特定部位的異常的放電，進而引發其他部位的異常放電，而產生癲癇發作，使用電刺激抑制發作，最好的方法是刺激源頭位置，為了達成此目的，本研究團隊提出多通道的電刺激電路，當偵

測到發作源頭位置，給予正確的刺激位置，以降低癲癇的發作。

抑制癲癇的方式為輸出定電流刺激，而在人體規格的抑制電流大小需要高達1-3 mA，此外，電極以及人體組織阻抗會隨著電極擺放位置以及電極的大小而有所不同，考慮到負載適應性，輸出級需要用到近 12V 高電壓，為了承受輸出端的高壓，過去的刺激器電路都是使用高壓製程來實作，但為了將刺激器整合至智慧型仿生系統中，實現系統單晶片(SoC)，刺激器電路必須使用低壓製程來實作。

對植入性晶片而言，設計時的主要考量為安全性、可靠度與功率消耗。本研究團隊提出的具有 16 通道電流刺激器，使用自偏壓的電路技術，使其能以低壓製程元件來承受高壓，而電晶體不會面臨電性過壓的情形。藉由三位元的控制訊號可輸出 0.5, 1, 1.5, 2, 2.5, 3mA 的輸出電流。整體電路在 0.18μm 1.8V/3.3V 低電壓製程下實現。

Design of 16-Channel Biphasic Stimulus Driver to Suppress Epileptic Seizure in the Low Voltage Process

Student: Tzu-Yi Yang **Advisor: Prof. Ming-Dou Ker**

Department of Electronics Engineering & Institute of Electronics
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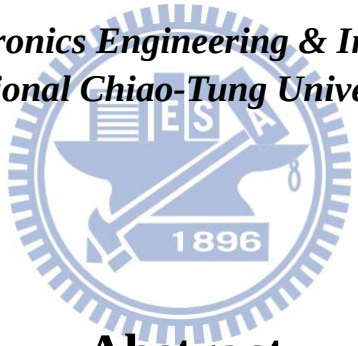


Abstract

Nowadays, the treatment of using electrical stimulation has been investigated and verified, such as functional electrical stimulation (FES). By stimulating abnormal nerve sites of the patients, they may restore some body functions. As the CMOS process developed, using an implantable device to provide stimulus current can be accomplished. The biomedical chip is made by the combination of microelectronics, medicine and biochemical such as epilepsy prosthetic system-on-chip (SoC).

Epilepsy is one of the most common neurological disorders. At epileptic seizure beginning, a particular part of the brain will begin abnormal discharge. Then, it will trigger some other part of the brain to discharge. By using electrical stimulation to suppress seizures, the best way is to stimulate source position. In order to achieve this object, we propose a multi-channel electrical stimulation circuit. When the circuit detects the epileptic seizure, it will stimulate the source position to reduce seizures.

The methodology to suppress epilepsy seizure is constant current stimulation, and the effective scale of stimulus current for human body is up to 0.5~3mA. In addition, the electrode-tissue impedance varies with the position and size of the electrodes in human body. Consider the loading adaptation, high voltage supply 12V is required in the output stage. Conventional works are fabricated in high-voltage process in order to sustain the high voltage at output of stimulus driver. To be integrated into biomimetic systems and to achieve SoC, this work needs to be implemented in low-voltage process.

The main considerations of designing an implantable device are safety, reliability, and power consumption. By using self-adaption technique and stacked transistors, the proposed multi-channel current stimulator, which consists of low voltage devices, is able to sustain high voltage (12V) without gate-oxide overstress. 3-bit amplitude signals are used to control the scale of stimulus current from 0.5mA to 3mA, with 0.5mA a step. The overall circuit has been fabricated by the 0.18μm 1.8V/3.3V CMOS process.

Acknowledgment

首先要感謝在碩士班這兩年柯明道老師的教導，感謝老師指導我們不管是在學術上的專業領域或是生活上一些做人處事的態度，扎實的訓練我們，使我們能在出社會前可以有很好的訓練。此外，也要感謝老師給我機會能參與癲癇計畫及人工電子耳計畫，在計畫中學習到很多，也參與到一些平常沒辦法接觸的經驗，如動物實驗與醫院手術的參觀，了解到電子以外的領域，並在這跨領域的合作學習到很多很多。

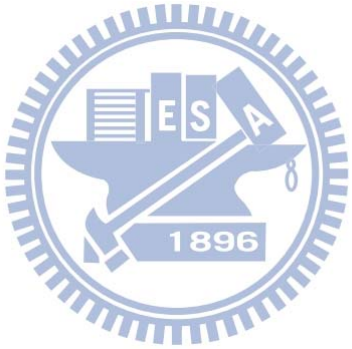
接著要感謝實驗室同屆的夥伴，黃義傑、廖顯峰、劉睿閎、鄭莞學，雖然大家研究的領域各不相同，大家還是都很熱情的起討論問題，互相學習，使我在碩士班的兩年學習得很愉快。再來要感謝實驗室的學長學姊，林群祐學長、蔡惠雯學姐、林倍如學姐、戴家岑學長、陳界廷學長、羅志聰學長、湯凱能學長、曾建豪學長、林冠宇學長、張品歆學姊、范美蓮學姊，在我有研究上遇到問題時，總是能給我重要的協助與幫助。還有感謝學弟妹們，吳柏翰、吳易翰、顏鼎洋、游力瑾、洪道一，能在實驗室的協助與幫忙。

接著要感謝在這計畫中給予我許多幫助的貴人，首先感謝吳重雨校長實驗室的錢信宏學長、鄭丞翔學長、林子涵、陳志鑫，李鎮宜教授團隊的蔡秉原學長、陳威宏，楊家驤教授團隊的吳易忠，花蓮慈濟醫院的李家鳳醫師及其助理陳臻，台灣大學周元昉教授團隊的吳宗殷，中山醫學大學附設醫院的辛裕隆醫師及智慧型仿生系統研究中心的黃健峻博士與陳煒明博士。

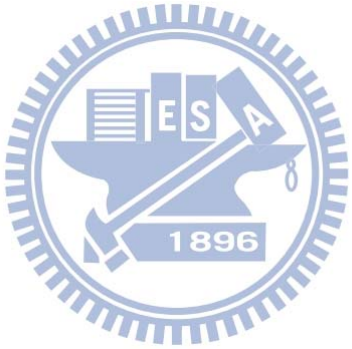
最後要感謝我的父母，從小到大無私的教養栽培與經濟支持，讓我能無憂無慮的順利成長、順利的畢業。

Contents

List of Tables



List of Figures



Chapter 1
Introduction

1.1 Motivation

As biomedical science and electronics rapidly developed, the new technology bioelectronics which combines with them is more and more popular. Nowadays, bioelectronics is an important technology in enhancing the quality of life, especially for those who are suffering from physiological difficulties. Several applications such as the resonance imaging (MRI), electroencephalography (EEG), electrocorticography (ECoG) and biomedical implant device are proposed and these are helpful to patients and doctors in the surgery. According to the research of the neuroscience, some lose physical functions can restore by functional electrical stimulation (FES). Novel biomimetic microelectronic systems such as the stimulation system through FES will enable treatment of some disease. For example, cochlear implants for treating profound hearing loss [1], retinal prostheses for treating blindness [2], spinal cord stimulators for blocking chronic pain [b], deep brain stimulators for treating parkinson's disease. Furthermore, epilepsy is also one of diseases investigated to be treated by therapeutic electrical stimulation.

Epilepsy is a neurological disorders caused by excessive abnormal discharge in the brain, and causes constant seizures. Seizures are the symptoms of epilepsy. It causes patients fainted, falling to the ground, making the muscles stiffen or jerking out of control. Nowadays, more than 60 million people suffer from epilepsy all over the word. As medical science progressed, therapies of epileptic seizure include pharmacologic treatment and surgical treatment. Pharmacologic treatment is always

applied in the first place. For patients who do not respond to the medicament, the surgical treatment will be used. However, the surgical treatment is non-reversible treatment and has high risks that might cause physical functions loss. Therefore, the new therapeutic option is announced. Through EEG technology which is analyzed in time or frequency domains [3], the probable disordered position which is seizure-onset zone can be found and the source of abnormal discharge tissue position can be predicted before seizure. It also has been demonstrated that the abnormal discharge signal that causes epilepsy can be suppressed by FES when detecting the abnormal brain wave [4]. In addition, accurately determining the location of the source abnormal tissue by multi-channel stimulator can have more high efficiency to suppress seizures.

Compared with the non-reversible surgical treatment, the advantages of electrical stimulation treatment are flexible, recoverable and do not injure the brain tissue. Although FES is a much better treatment for epileptic, there are several challenges in designing the stimulus driver. Due to different kinds of sizes, locations, and electrode material, the equivalent impedance of electrode and tissue will vary in a wide range. Moreover, the effective stimulus current to suppress epileptic seizures is up to 3mA. The series resistance of equivalent impedance (R_S) is always 2~3kΩ, so the stimulus driver need to provide high voltage (more than 9V) to output. Moreover, not like the epileptic system of rats, the electrodes which are used to record brain signal and stimulate are at different place, but the epileptic system of human uses the same electrodes. The stimulus driver need to deliver very small brain signal to signal acquisition circuit and stimulate constant current by high voltage. To be integrated into biomimetic systems and to achieve SoC, this work needs to be implemented in low-voltage process. The problems of gate-oxide overstress, hot-carrier effect, and other reliability issues will be considered [5]. In this thesis, the proposed stimulus

driver is designed consider with both reliability and safety issue. The 16-channel stimulus driver with high-voltage-tolerant structure with detect-mode and stimulate-mode functions is investigated in this work.

1.2 Thesis Organization

The first chapter, chapter 1, includes the motivation of this work and the thesis organization.

Chapter 2 of this thesis introduces some background knowledge of epilepsy, epileptic seizures treatment, implantable prosthesis of epileptic SoC and stimulus driver.

In chapter 3, design of 16-channel high-voltage-tolerance stimulus driver to suppress epileptic seizure is proposed. The proposed stimulus driver has been fabricated in the UMC 0.18μm 1.8V/3.3V process.

In chapter 4, to consider the stimulus driver need to deliver brain signal and stimulate biphasic current by high voltage, the stimulus driver based on the proposed circuit on chapter 3 is added detect-mode function. The proposed stimulus driver will be fabricated in the TSMC 0.18μm 1.8V/3.3V process.

The last chapter, chapter 5, recapitulates the major consideration of this thesis and concludes with suggestions for future investigation.

Chapter 2

Background of Epilepsy, Stimulus Driver and Epileptic SoC Development

2.1 Overview of Epilepsy and Epileptic Treatment

Epilepsy is a chronic disorder characterized by recurrent self-limited seizures with excessive discharges throughout localized or generalized groups of neurons in the brain recurrent seizures if frequent interfere with the patients' ability to perform day-to-day activities. Fig. 2.1.1 shows the electrodes on cerebral cortex and waveforms of ECoG during the epilepsy seizure [6]. For an example to illustrate, Fig. 2.1.2 shows the process of the epilepsy seizure. At epileptic seizure beginning, the electrodes 25 and 26 record the abnormal discharge signal which is consist by a low frequency and different with other electrodes. At this time, the patient feels nothing then the abnormal discharge will deliver to neighbor region and induce a big area abnormal discharge like the right part of Fig. 2.1.2. All the electrodes record the excessive electrical discharge signal and these make the epileptic seizures.

According to a Brodmann area which is shown in Fig. 2.1.3, it is a region of the cerebral cortex in the human. Many of the areas Brodmann defined based solely on their neuronal organization have since been correlated closely to diverse cortical functions. For example, Brodmann areas 4 are primary motor cortex which manage the function of human motion, and Brodmann areas 1,2,3 are primary somatosensory cortex which manage the function of human sense.

If the abnormal discharge delivers to primary motor cortex, the patients will make the muscles stiffen or jerk out of control. In other way, if the abnormal

discharge delivers to primary somatosensory cortex, the patients will feel numb on face or hand. The common two ways to treat the epilepsy are pharmacologic treatment and surgical treatment.

Pharmacologic treatment is the priority way to suppress epileptic seizure. Due to the diversification of epilepsy, there are more than 20 types of medications, and each is developed for specific type of epileptic seizure. According to patients' age, types of epilepsy, syndromes, and intensity of seizure, doctors will choose suitable medications (antiepileptic drugs or AED) for treatment [7]. Depakine is one of the general AED. The mechanism of action is to inhibit GABA transaminase, which is an enzyme that metabolizes GABA. Then, it increases levels of GABA, which is an inhibitory neurotransmitter, and reduces abnormal discharge of nervous system (Fig. 2.1.4).

However judicious use of antiepileptic medications allows about 65-70% of epileptic patients to be seizure-free. It means that about 25-30% of epileptic patients can't be cured by classical antiepileptic drugs. This type of drug-resistant epilepsy is called "intractable epilepsy". The surgery treatment will be used. The method of surgery treatment is to directly cut out the disorder region which is usually called seizure-onset zone. But not everywhere in the brain can be cut out, the region like primary motor cortex or primary somatosensory cortex is important place which makes doctors carefully consider. If doctors cut the primary motor cortex, after surgery the patients may become paralyzed or feel muscles stiff. For this reason, surgery treatment has some necessary steps to be followed as Fig. 2.1.5. First, doctors will use electroencephalography (EEG) which is typically a non-invasive method to record electrical activity of the brain along the scalp to find the probable place of epilepsy. Second, the electrocorticography (ECoG) which is the practice of using electrodes placed directly on the exposed surface of the brain to record electrical

activity from the cerebral cortex will be used to record clearer brain signal and find more accurate position of seizure-onset zone. Third, the doctor will do brain mapping to find where are the safe regions can be cut. During brain mapping, doctors will stimulate each electrode on the cerebral cortex. According to the response of patient, doctors can find what region on the cortex such as primary motor cortex and primary sensory cortex. If the seizure-onset zone is not on the important region, doctors will do resection surgery.

However, the seizure-onset zone of every patient is not always at safe region. The advanced therapeutic option is announced. By automatic detection of the epileptic seizures in ECoG [8] and using FES to suppress, the closed-loop neural prosthetic system on the chip can be achieved. At next section, the neural prosthetic SoC will be detailed illustrated.

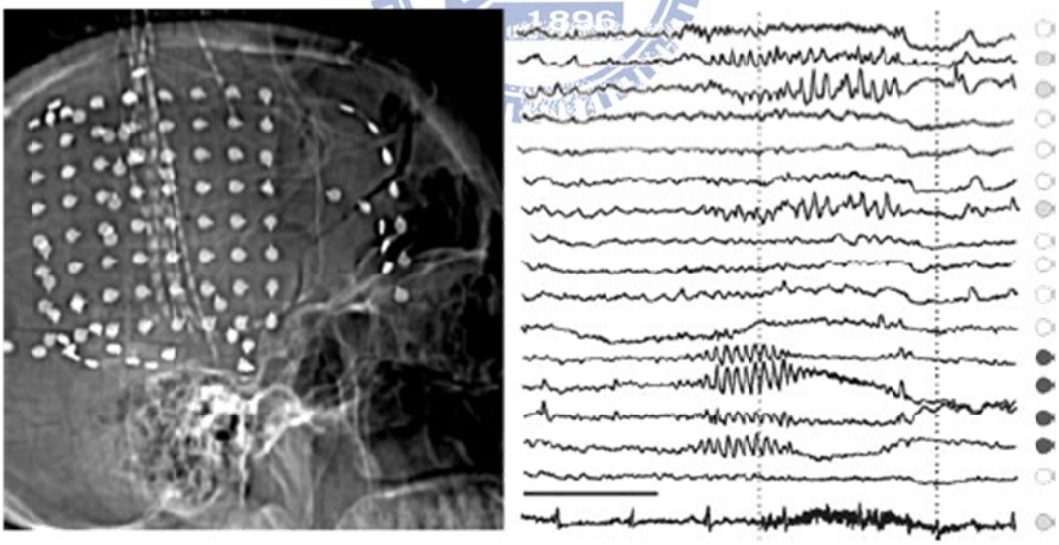


Fig. 2.1.1 Pictures of an electrode array for recording of the brain activity [6].

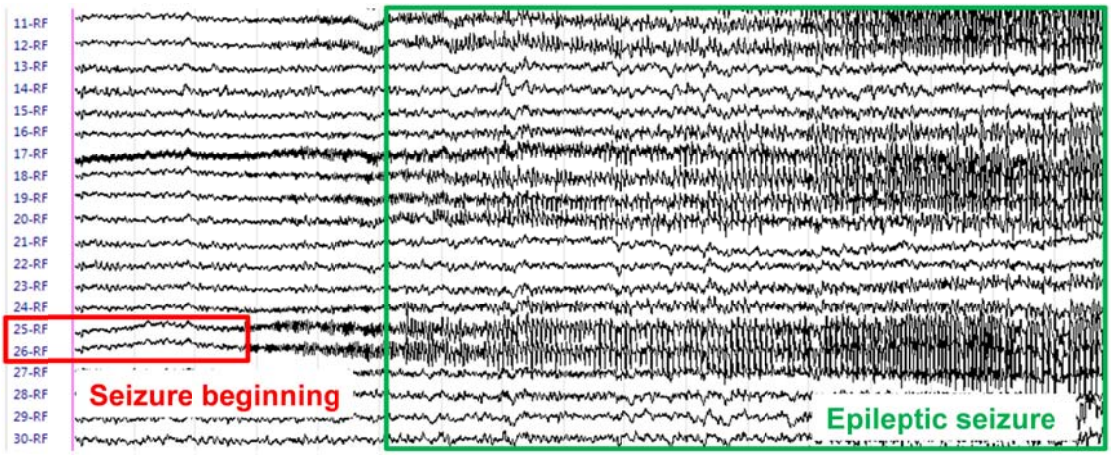


Fig. 2.1.2 The ECoG signals of an epileptic patient.

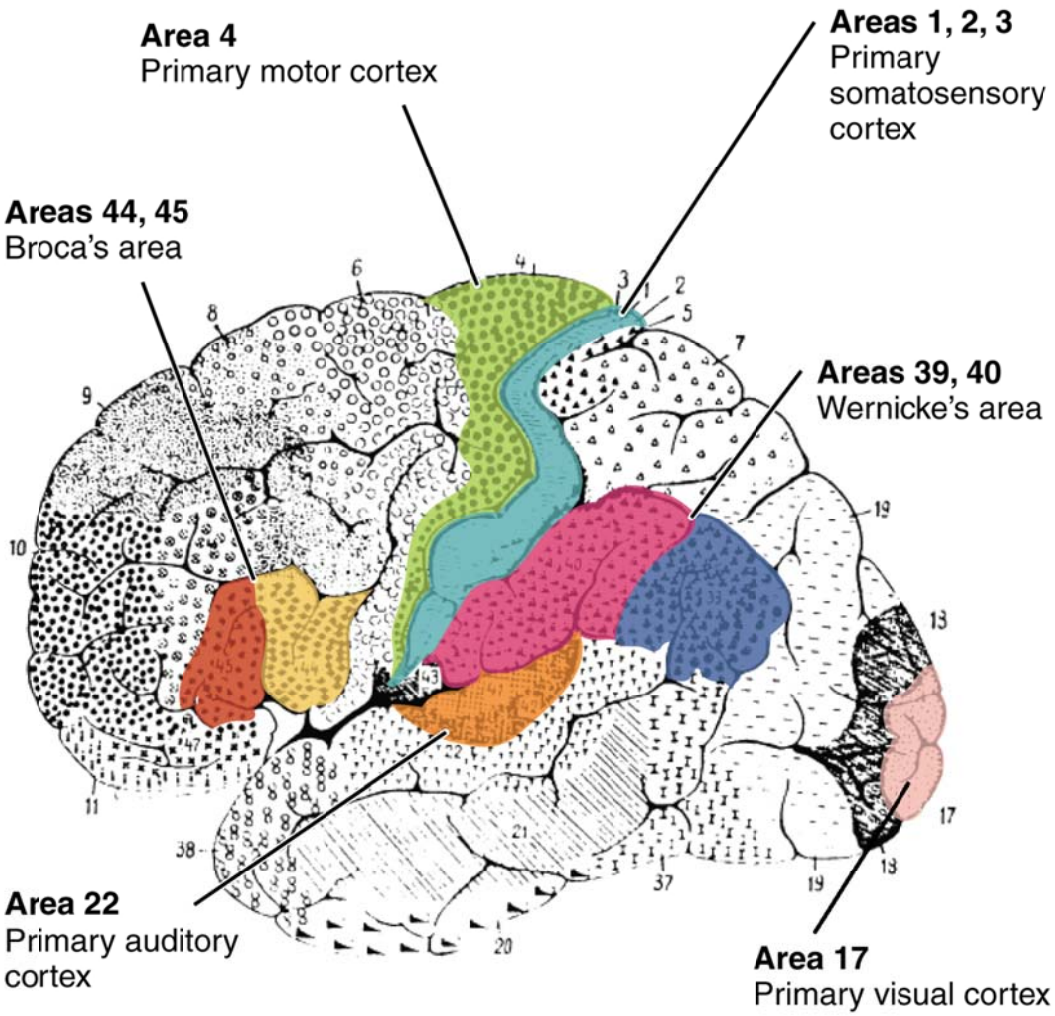


Fig. 2.1.3 Brodmann area.

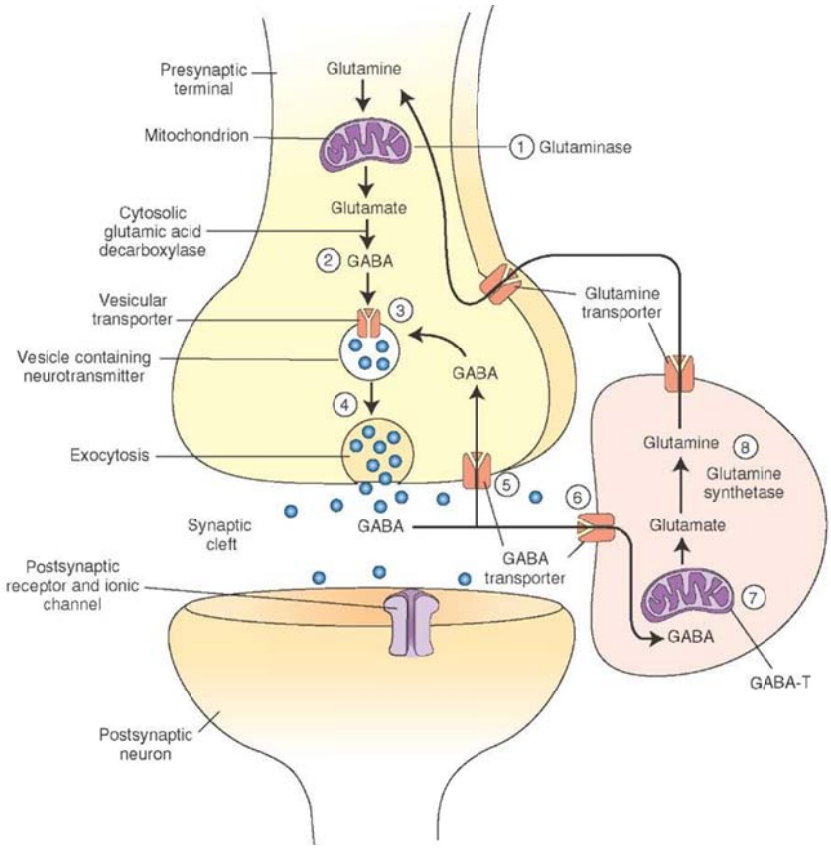


Fig. 2.1.4 Mechanism of action of Depakine, which is one of the AED.

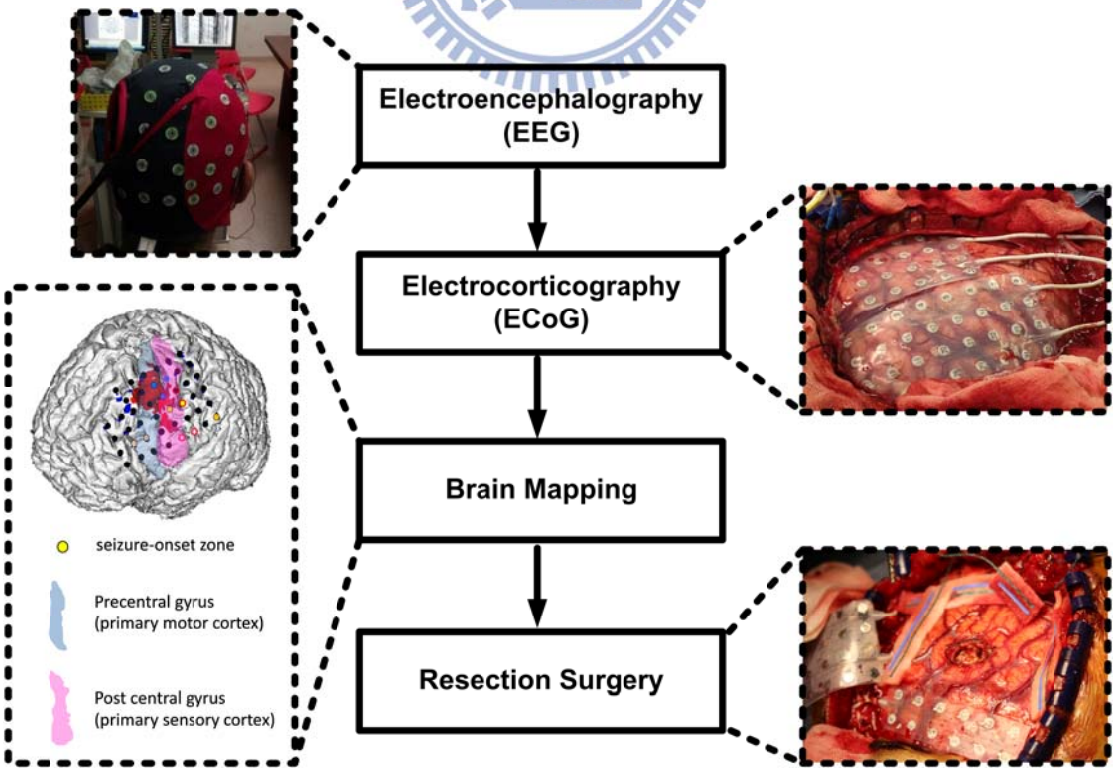


Fig. 2.1.5 The steps of surgery treatment.

2.2 Closed-Loop Neural Prosthetic SoC for Suppressing Epileptic Seizure, and Design of Implantable Stimulus Driver

2.2.1 Introduction of Functional Electrical Stimulation (FES)

Functional electrical stimulation (FES) is a technique that uses electrical current applied in programmable patterns through electrical stimulators and electrodes to excitable tissue to supple or replace function that is lost in neurologically impaired individuals. In addition to the chronic applications for restoration of function, electrical stimulation has also been used for many therapeutic applications [9].

The waveform of electrical stimulation pulse is characterized by three parameters: amplitude, pulse width, and pulse frequency. To different position of neurons and different human bodies, each of the parameters may be different. Stimulus waveforms are generally either biphasic or monophasic in shape. A monophasic can induce DC charge accumulation on the neuron, and the neuron can be injured by chronic DC charge accumulation. Thus, most FES systems adopt biphasic stimulus waveforms shown in Fig. 2.2.1. The cathodic current usually starts first to elicit a desired neural response, while the anodic current, following the cathodic current, cancels charge across stimulating electrode pair. The interphase delay separates the currents so that the anodic current does not reverse the physiological effect of the cathodic current.

Nowadays, several applications used functional electrical stimulation (FES) has successful achievements, such a cochlear prosthesis for hearing loss, shown in Fig.2.2.2 [10], and retinal prosthesis for blindness, shown in Fig. 2.2.3 [11][12].

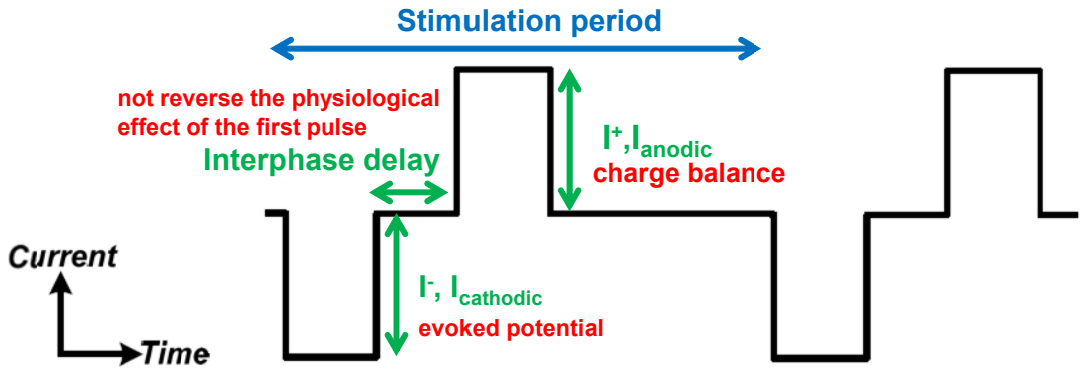


Fig. 2.2.1 Biphasic stimulation pulse.

Fig. 2.2.2 The implanted system of cochlear prosthesis [10].

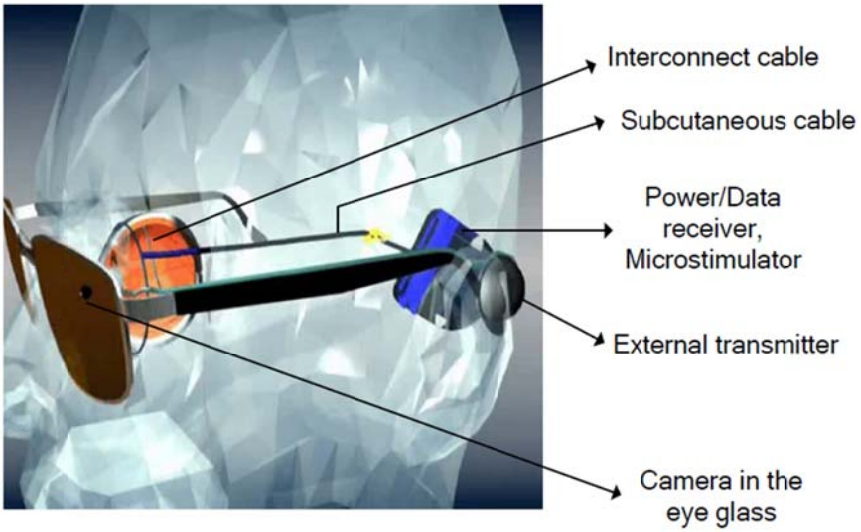


Fig. 2.2.3 The implanted system of retinal prosthesis [12].

2.2.2 Closed-Loop Neural Prosthetic SoC for Suppressing Epileptic Seizure

Fig. 2.2.4 shows the block diagram of the closed-loop neural-prosthetic SoC for suppressing epileptic seizures [13]. The system consists of external chip and implanted chip. The system has a signal acquisition unit (SAQ), a bio-singal processor (BSP), an electrical stimulator, a wireless transceiver/receiver system (Tx/Rx), and a power system.

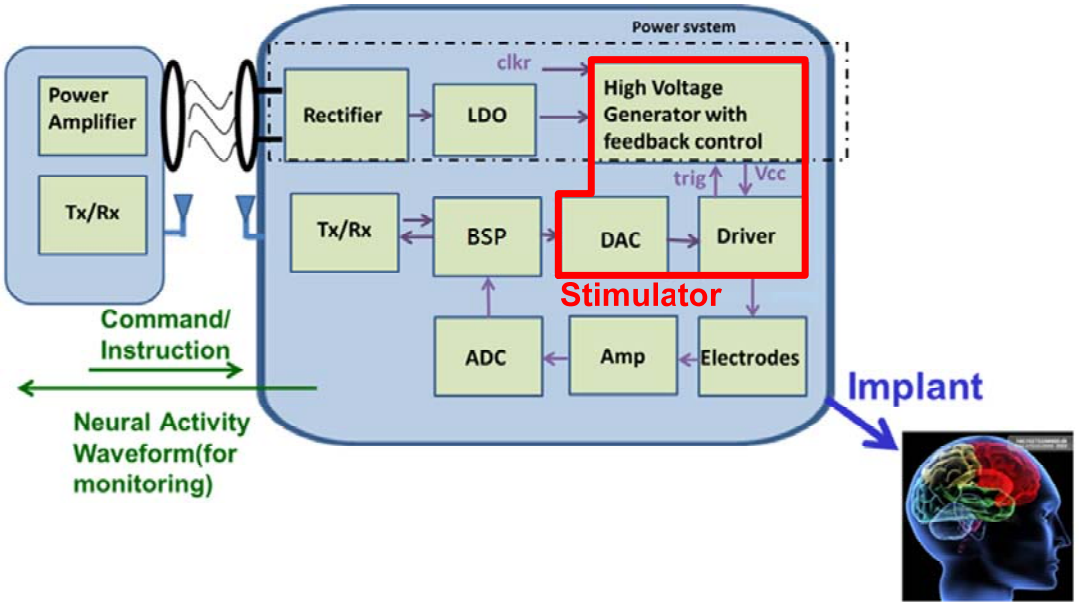


Fig. 2.2.4 The block diagram of an implantable system for epileptic treatment.

In the implanted chip, the SAQ is used to amplify the brain signal from electrode on the cerebral cortex (ECoG) and through analog to digital converter (ADC) converts signal to digital signal for BSP to analyze. The ECoG is calculated by specific algorithms through time or frequency domains to predict when epileptic seizure will happen and the position of seizure-onset zone. Then, the BSP controls stimulator by programmable patterns through functional electrical stimulation to suppress the abnormal brain activities.

The recorded ECoG signals can be transmitted by Tx/Rx to monitor system. Data transmission is encoded through a reliable cyclic redundancy check (CRC). If the data

transmission is not pass the CRC, the system will pass the data to ensure the accuracy of data.

The power system consists of power amplifier, rectifier, regulator, and high voltage generator. The power amplifier through the primary coil transmits the power in the external part. In the implanted part, the rectifier converts the AC to DC from secondary coil and low dropout regulator (LDO) converts the output voltage of rectifier to a stable voltage source which supplies to the circuit of implanted part. When the BSP detects the epileptic seizure, the high voltage generator will use the output voltage which is supplied by LDO to generator a high voltage for stimulator.
In addition, the wireless system uses only one coil, so the data of ECoG is added on the power signal to deliver. The wireless system can be transmitted of the industrial scientific medical band (ISM) which is 13.56MHz.

Fig. 2.2.5 is an example for epileptic SoC which is treatment for rats and is presented in 2014 [14]. A fast seizure detection response time of 0.8s and high accuracy of above 92% are achieved using the proposed portable embedded device. The system provides biphasic current (30uA) to suppress and has the advantages of low cost, compact size, low power and real-time detection.

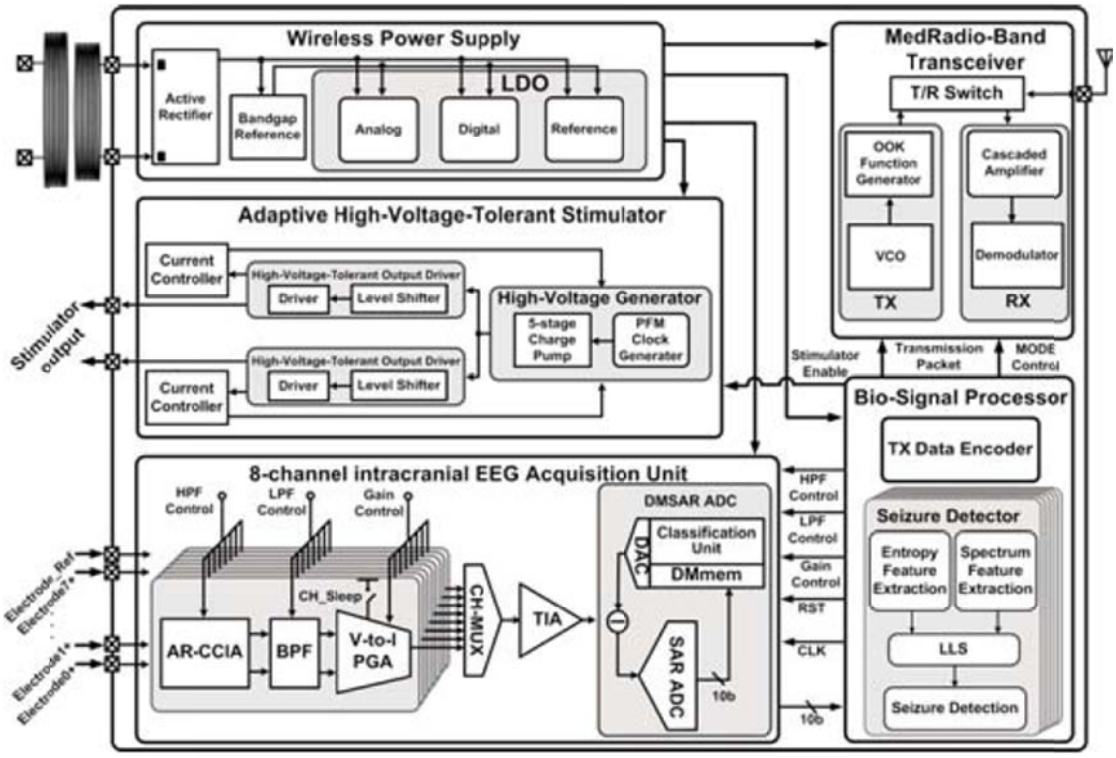


Fig. 2.2.5 Architecture of the epileptic seizure SoC [14].

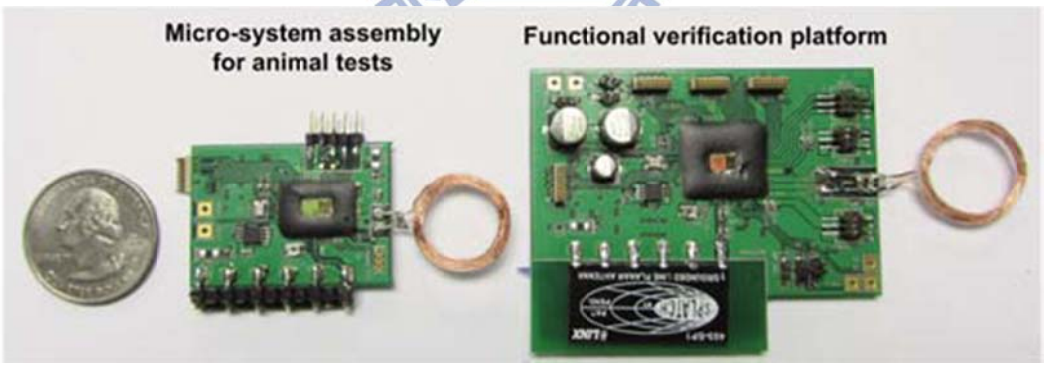
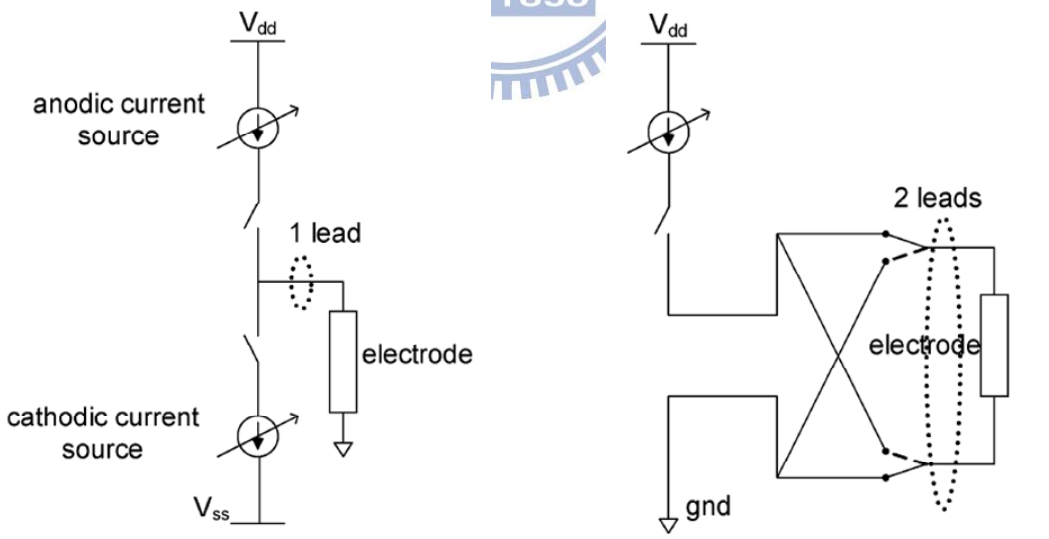


Fig. 2.2.6 Another example of the closed-loop epileptic seizure monitor and controller [15].

2.2.3 Design of Implantable Stimulus Driver

As the development of electrotherapy, a variety of implantable stimulus drivers have been researched and presented. In order to deliver the biphasic current pulses, there two choices of chip-electrode interface for each stimulation site: (1) one interface lead per site (monopolar stimulation) and (2) two interface leads per site (bipolar stimulation) [16]. Fig. 2.2.7(a) shows the schematic of one interface lead per site, when the monopolar stimulation is used, two supply voltages are required to provide the cathodic and anodic stimulus currents. A return electrode, common to all the stimulating electrodes, is connected to the ground potential in this case. Fig. 2.2.7(b) shows the schematic of two interface leads per site, when the bipolar stimulation is used, only one supply voltage is required because each stimulation site has a dedicated return path. The anodic and cathodic stimulus currents are provided by reversing the current paths by switches.



(a) One Interface lead per site (Monopolar Stimulation)

(b) Two Interface leads per site (Bipolar Stimulation)

Fig. 2.2.7 Different stimulation method affects the components in the stimulus driver.

Fig. 2.2.8 is an example of monopolar stimulation [17]. This work is used for the retinal prosthesis devices. The stimulus driver is proposed in the 0.35μm high voltage CMOS process. The positive high voltage +5V and negative high voltage -5V are required to generate cathodic and anodic stimulus currents. To consider the current mismatch problem, this work describes a compact negative-feedback self-calibration scheme to minimize the current amplitude mismatch between the anodic and the cathodic pulses for achieving the charge balance. The device can provide 1mA stimulus current in less than 0.3μA current mismatch by self-calibration technique.

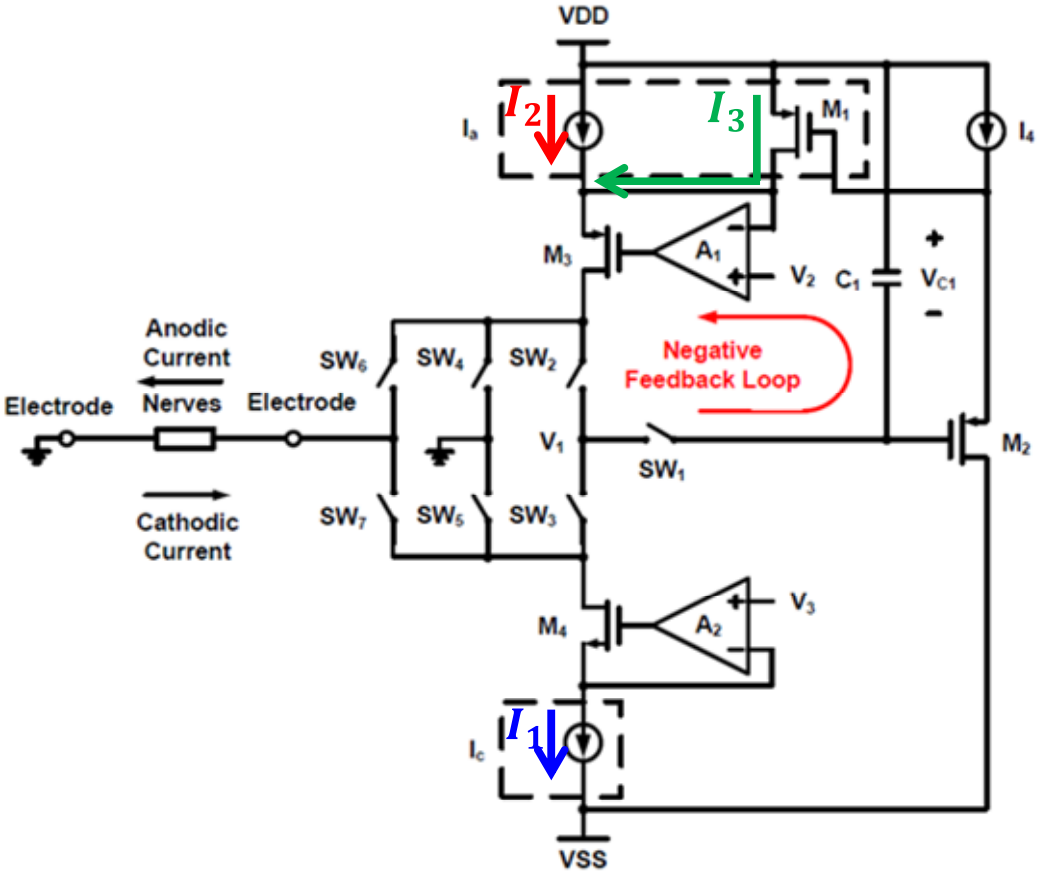
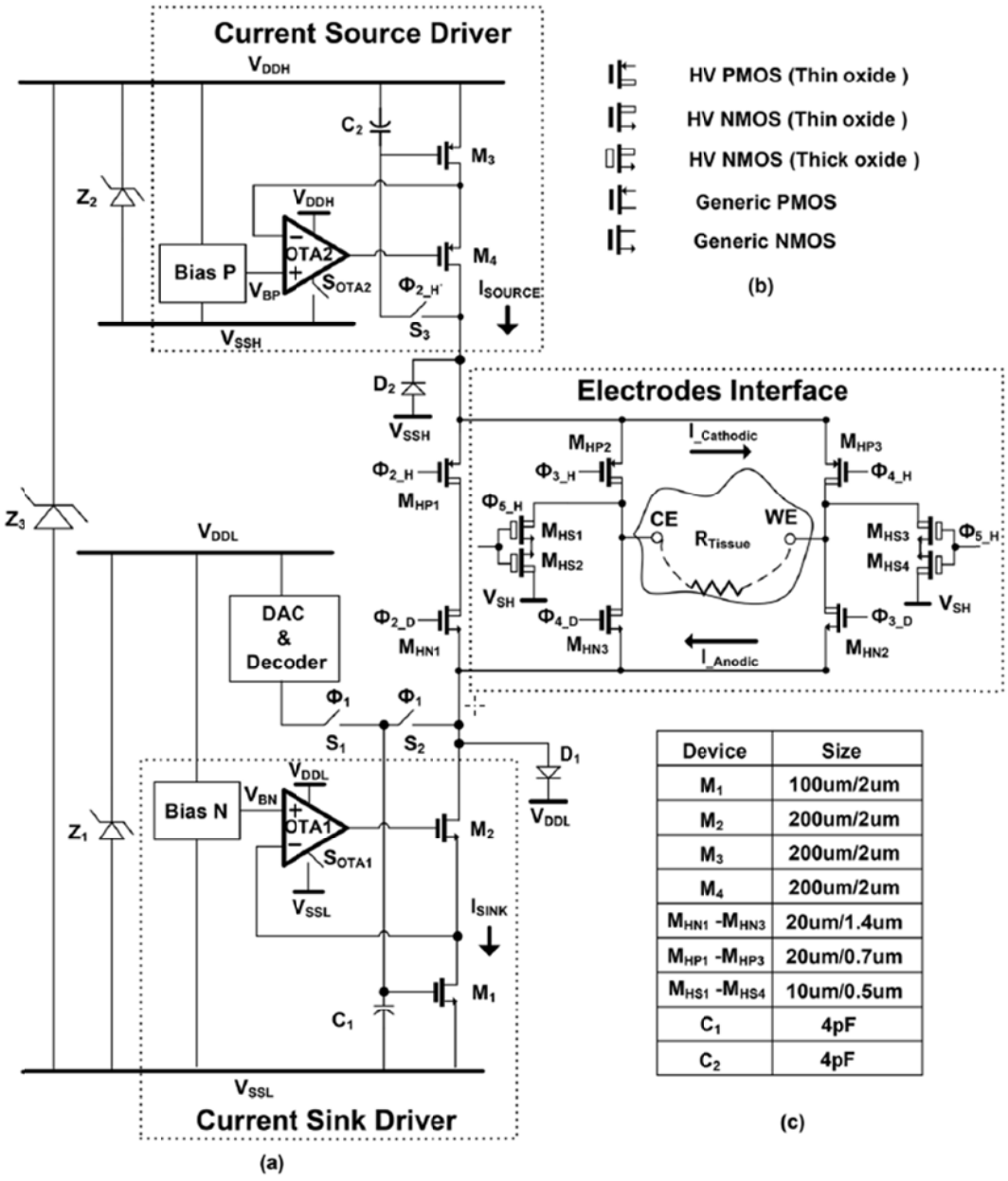


Fig. 2.2.8 Biphasic stimulator with one interface lead per site.

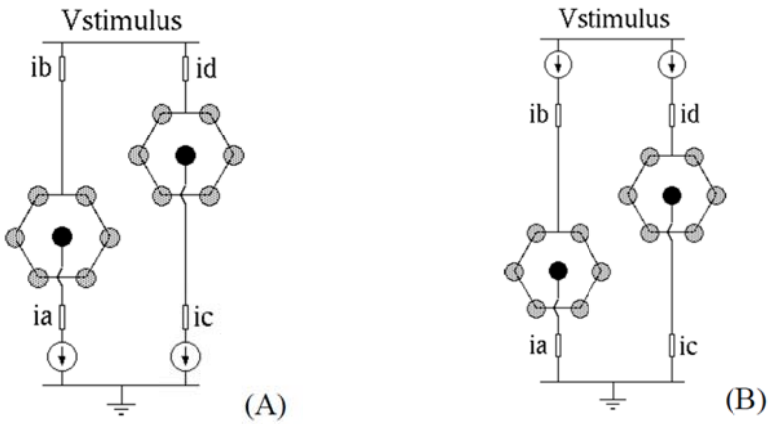
Fig. 2.2.9 is an example of bipolar stimulation [18]. This work is also applied in retinal prosthesis devices. By using the 0.35μm high voltage CMOS process, the device operates at 15V high supply voltage and controls transistors M_{HP2}, M_{HP3}, M_{HN2}, and M_{HN3} as switches and uses dynamic current mirror to sample current source and current sink through capacitance C_1 and C_2. The device can generate 1mA biphasic stimulus current in less than 3μA current mismatch.



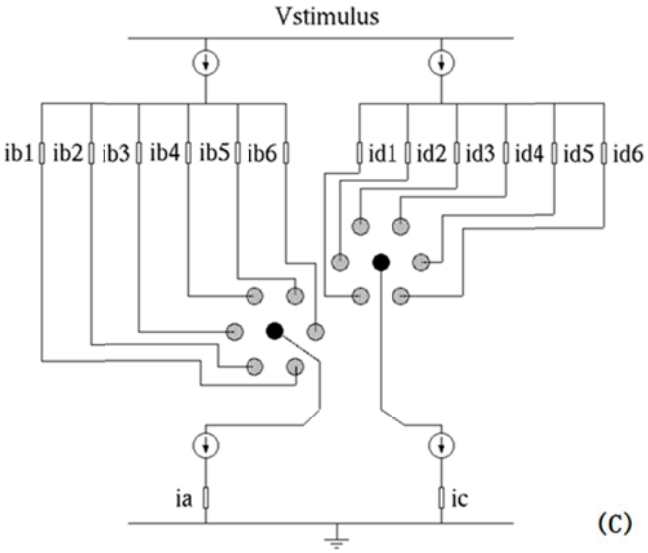
Device	Size
M_1	100um/2um
M_2	200um/2um
M_3	200um/2um
M_4	200um/2um
M_{HN1} -M_{HN3}	20um/1.4um
M_{HP1} -M_{HP3}	20um/0.7um
M_{HS1} -M_{HS4}	10um/0.5um
C_1	4pF
C_2	4pF

Fig. 2.2.9 Biphasic stimulator with two interface leads per site.

In two interface leads per site, the construction of the stimulus driver can be discussed by three methods: (a) current source only, (b) current sink only, and (c) the combination of a balanced current source and current sink (Fig. 2.2.10). [19] has tested in retinal prosthesis devices and demonstrated that the combination of current source and current sink has better direction and control of the current flow in multi-channel simultaneously stimulating.



(A) Active electrode connected to a current sink and guard electrodes connected to Vstimulus. (B) Active electrode connected to circuit ground and guard electrodes connected to a current source. (i_a, i_b, i_c, and i_d are the currents measured in each electrode.)



(C) Active electrode connected to a current sink and guard electrodes connected to a current source. (i_a, $i_{b[1-6]}$, i_c, and $i_{d[1-6]}$ are the currents measured in each electrode.)

Fig. 2.2.10 Three constructions of the stimulus driver in two interface leads per site.

Chapter 3

Design of 16-Channel High-Voltage-Tolerance Biphasic Stimulus Driver to Suppress Epileptic Seizure in the Low Voltage Process

3.1 Introduction

In this chapter, the illustration is separated into three parts. First, to consider the device is used to suppress epileptic seizure on human body, the impedance of the platinum electrodes on the cerebral cortex of human body is analyzed. According to the result of impedance analysis and some architecture tradeoffs, the specifications of stimulus driver will be proposed. Second, the 16-channel high-voltage-tolerance stimulus driver is proposed. Third, the detailed circuit simulation and measurement results of proposed design will be presented.

3.2 Design Considerations of stimulus driver

3.2.1 Impedance Analysis

According to the [20][21], the electrode-tissue impedance can be modeled by Fig. 3.2.1. In this simple model, R_S is the solution spreading resistance, which is determined by the resistivity of the fluid (set by ionic species in solution). C_{dl} is the double-layer capacitance, which is created by the accumulation of tightly adsorbed ions at the electrode surface and more loosely attracted ions in a diffusion layer behind it. R_f is the Faradaic resistance, which is decided by diffusion of reactive species to the electrode

for charge-transfer reactions. The resistance R_f is indicated as a time-varying variable resistor because its value varies based on the dynamics of redox charge-transfer reactions occurring at the electrode. To illustrate Faradaic charge transfer and capacitive redistribution of charge, Fig. 3.2.2 shows (a) physical representation and (b) two-element electrical circuit model for mechanisms of charge transfer at the interface to explain.

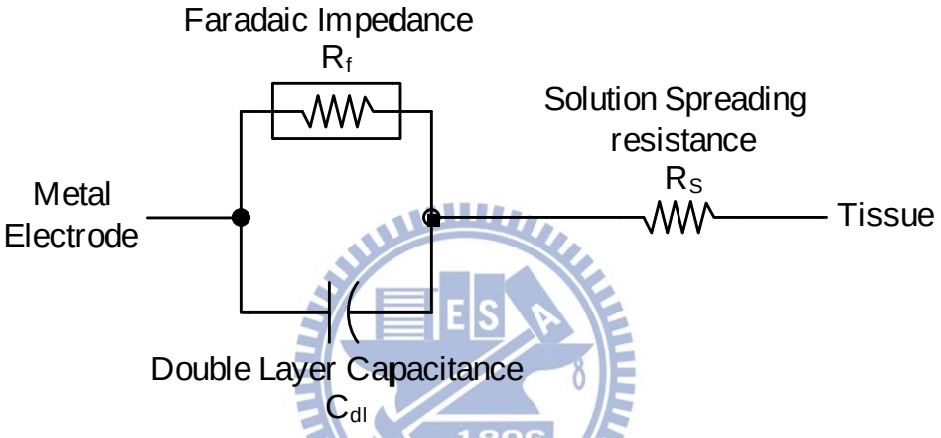


Fig. 3.2.1 The equivalent impedance of electrode-tissue.

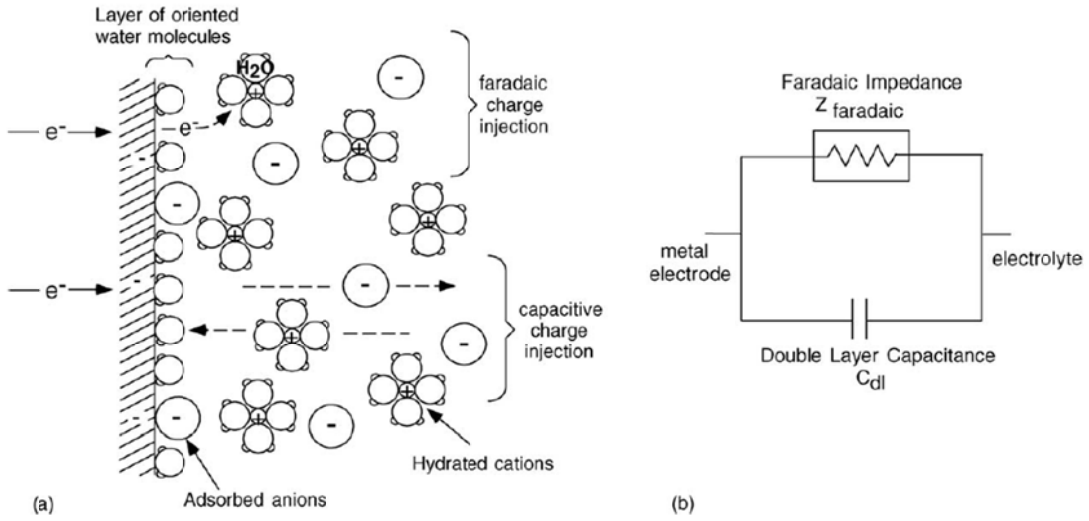


Fig. 3.2.2 The electrode/electrolyte interface.

Fig. 3.2.3 shows the resection of cerebral cortex. In this case, the area of cerebral cortex is probable 1×1.5 cm^2 and the electrode is used by AD-TECH IS04R-SP10X-000 which is platinum material (charge density limit 100~150μC/cm^2) and has 2.3mm diameters of contact area to meaure the equivalent impedance (Fig. 3.2.4). The impedance analyzer sweeps frequency from 1 to 10^5 Hz and the sets ac amplitude 1V (Fig. 3.2.5). The result of the analysis is shown Fig. 3.2.6. The R_S is 2.78kΩ, C_{dl} is 319nF, and R_f is 56.2kΩ.

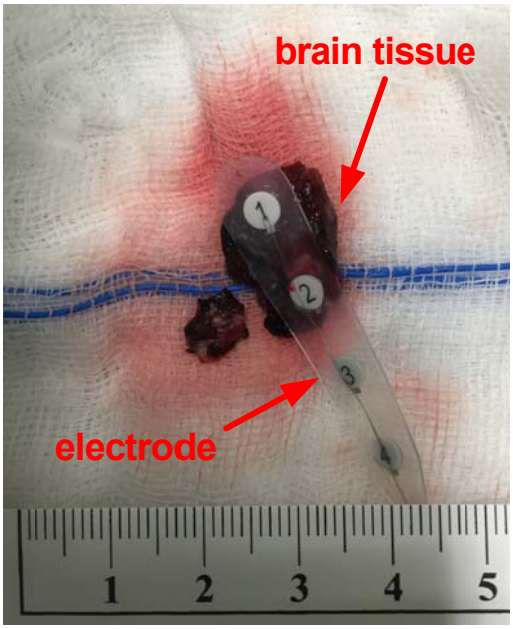


Fig. 3.2.3 The resection of cerebral cortex.

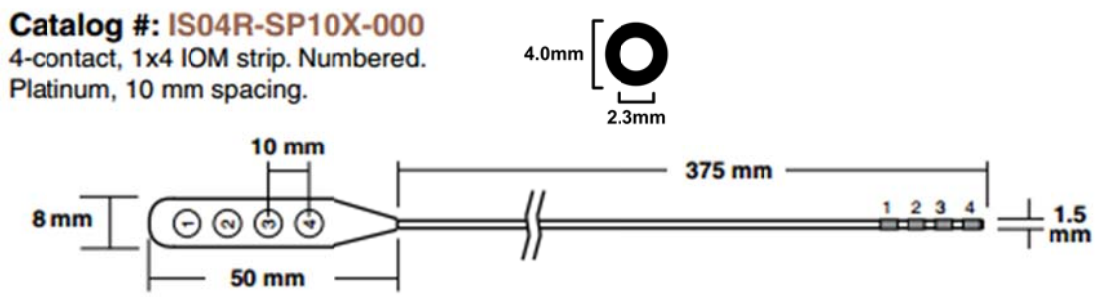


Fig. 3.2.4 AD-TECH IS04R-SP10X-000 electrode.

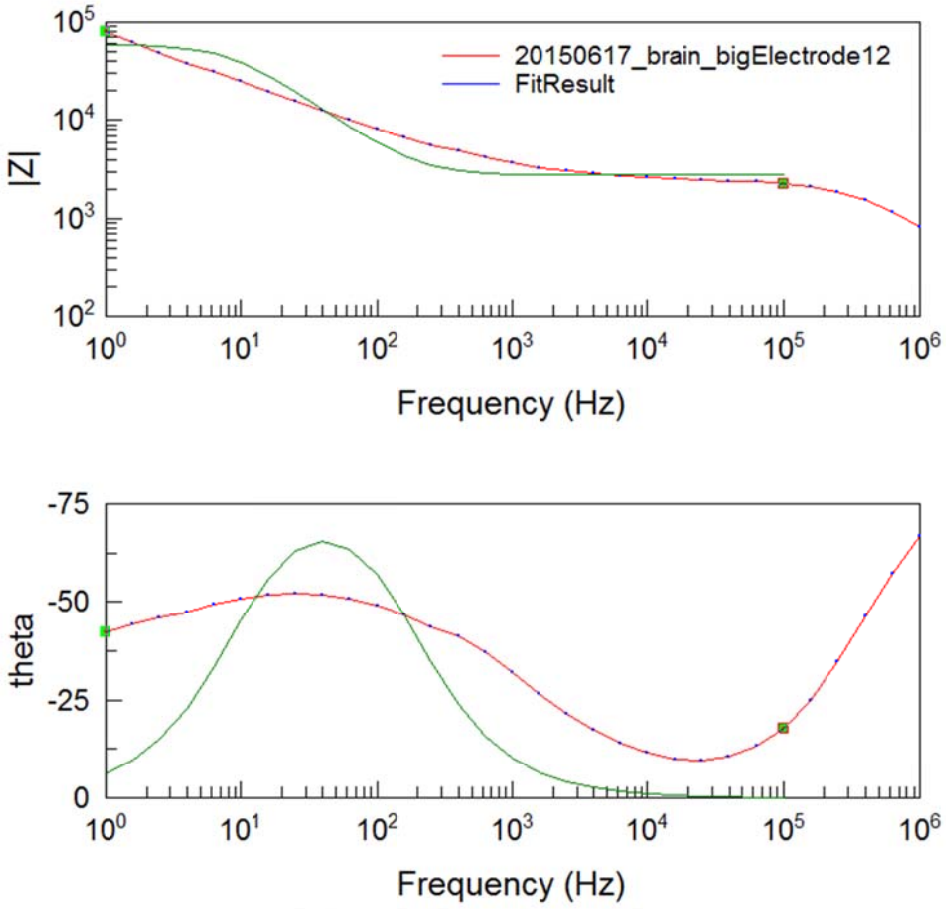


Fig. 3.2.5 The result of impedance analyzer.

Element	Value	Error	Error%
Rs	2780	236.83	8.5191
C	3.1941E-7	4.219E-08	13.209
Rp	56161	7817	13.919

Fig. 3.2.6 The analysis of impedance data.

3.2.2 Specifications of Stimulus Driver

This work is to improve effective suppressing epileptic seizure. The accurately determining the location of the source abnormal tissue by using 16-channel stimulator is proposed. To be integrated into biomimetic systems and to achieve SoC, this work selects 0.18μm 1.8V/3.3V process to achieve. However, because of R_S of the

equivalent impedance is about 3kΩ and following the demand of doctors that stimulus current is up to 3 mA which can make valid stimulation, the high voltage supply needs more than 9V. In this case, we set the high voltage which supports to 12V and do not use negative supply voltage which is difficult to generator in the chip. The bipolar stimulation (two leads per site) is used. Though the proposed 16-channel is used, but only one pair of electrodes can stimulate. So, the construction of only current source is used. According to [22], the tissue damage does not occur in chronic stimulation of cochlear implants, where charge imbalance (residual DC current) is kept below 100nA, so we prefer the residual DC current will be under 100nA. Finally, the power dissipation in an implanted stimulator will provide the thermal rise. 1 or 2°C above the normal retinal temperature could lead to the retinal damage [23] so the standby power must be less than tens of mW and it is believed that the thermal rise will not cause tissue damage.

Table 3.1
Specifications of stimulator.

Process	**0.18μm 1.8V/3.3V process**
Electrode Configuration	**Bipolar (two leads per site) (Only current source)**
Supply Voltage	**1.8V & 12V**
Stimulus Current Amplitude	**0.5mA ~ 3mA (tunable)**
Output Resistance Load	**1kΩ ~ 3kΩ**
Channel Number	**16 channels**
Cathodic / Anodic Current Mismatch	**<100nA (residual DC current)**
Power Consumption	**<20mW**

3.3 Design of 16-Channel High-Voltage-Tolerance Stimulus Driver

3.3.1 Architecture

The proposed 16-channel high-voltage-tolerance stimulator schematic is showed at Fig. 3.3.1. The stimulator controls stimulus driver to make biphasic stimulus current in three phases. In first phase, when the switches $SW_{\Phi 1a,b}$ are turned on and $SW_{\Phi 2a,b}$ are turned off, the driver can induce a cathodic current. In second phase, when switches $SW_{\Phi 2a,b}$ are turned on and $SW_{\Phi 1a,b}$ are turned off, the driver can induce a anodic current. In third phase, when switch $SW_{\Phi 2a}$ and $SW_{\Phi 1b}$ are turned on, the driver can induce a discharge current to discharge residual charge which is made by current mismatch on electrode. Fig. 3.3.2 shows the control signal and current level of 3-bit amplitude. The control pins ANO, CAT and DISCHARGE control the output waveform and AMP[2:0] decides the stimulus current amplitude.

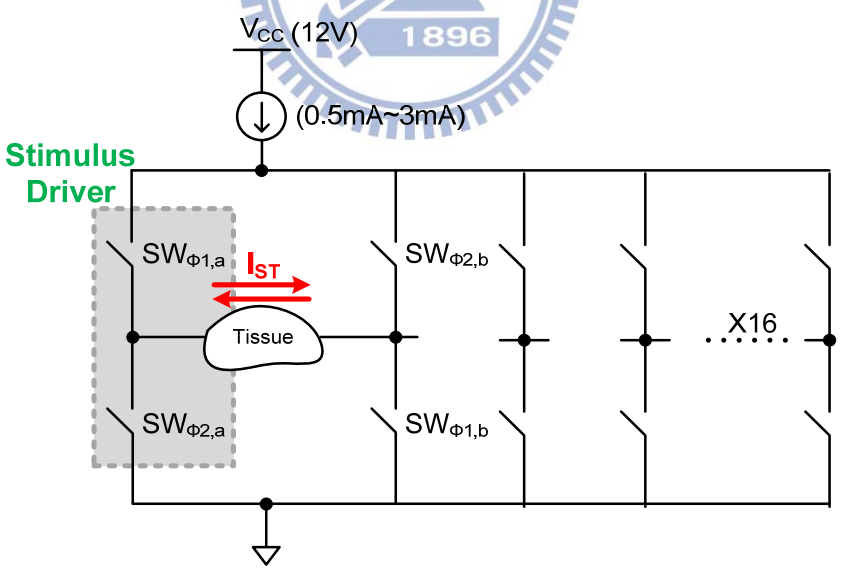
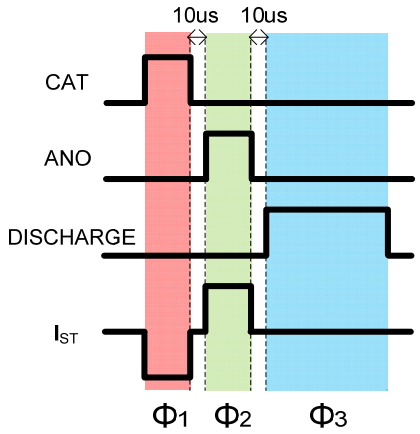


Fig. 3.3.1 16-channel high-voltage-tolerance stimulator schematic.



Amplitude signal AMP[2:0]	Stimulus current (Ist)
001	0.5mA
010	1.0mA
011	1.5mA
100	2.0mA
101	2.5mA
110	3.0mA

Fig. 3.3.2 Control signals and output waveform.

The block diagram of the stimulator which is shown in Fig. 3.3.3 consists of 16 stimulus units (level-shift (high-side), level-shift (low-side), and stimulus driver), reference voltage generator, DAC, decoder, and high voltage generator. However, the high voltage generator does not realize in this work.

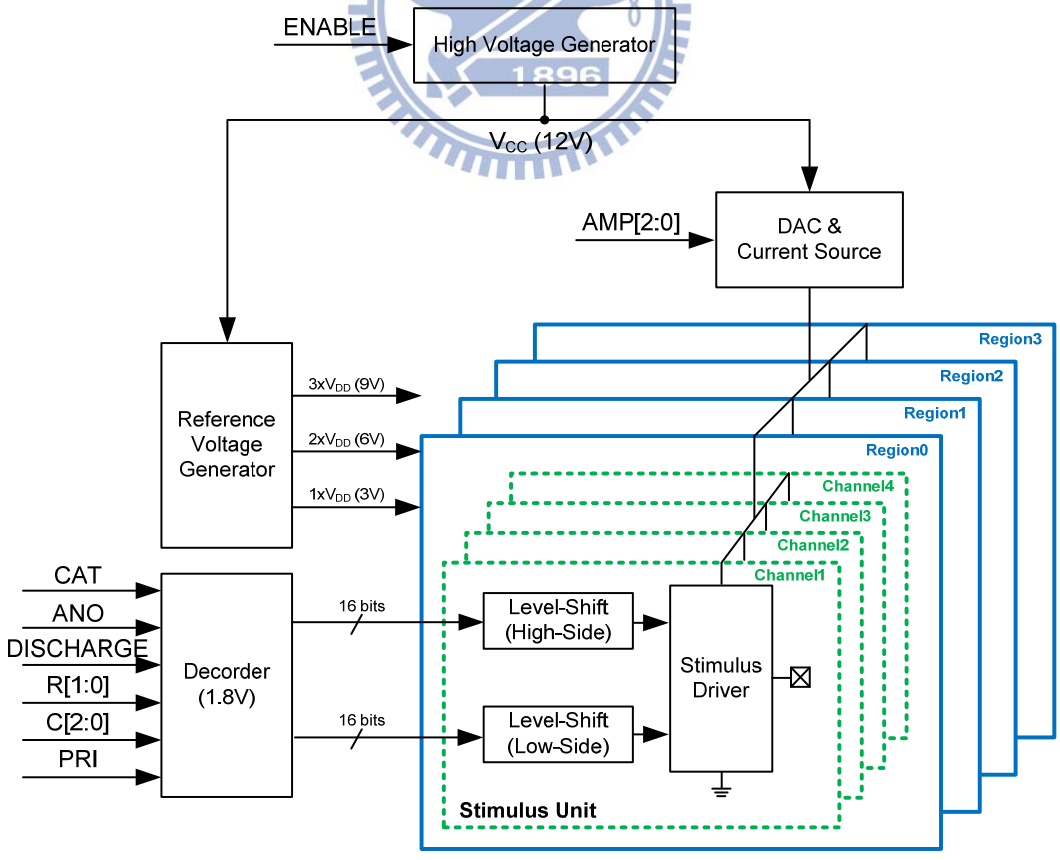


Fig. 3.3.3 16-channel high-voltage-tolerance stimulator block diagram.

The proposed 16-channel stimulator is fixed on 4x4 electrode array (Fig. 3.3.4). Only one pair of drivers can be chosen to stimulate current. Through control pins (R[1:0], C[2:0] and PRI) we can decide which pair of drivers stimulates. The control pins R[1:0] decide which region of four quadrants. The control pins C[2:0] decide which pair in one quadrant. For example, if we choose C[2:0]=4, that means we choose channel A and channel C. The control pin PRI decides the current direction.

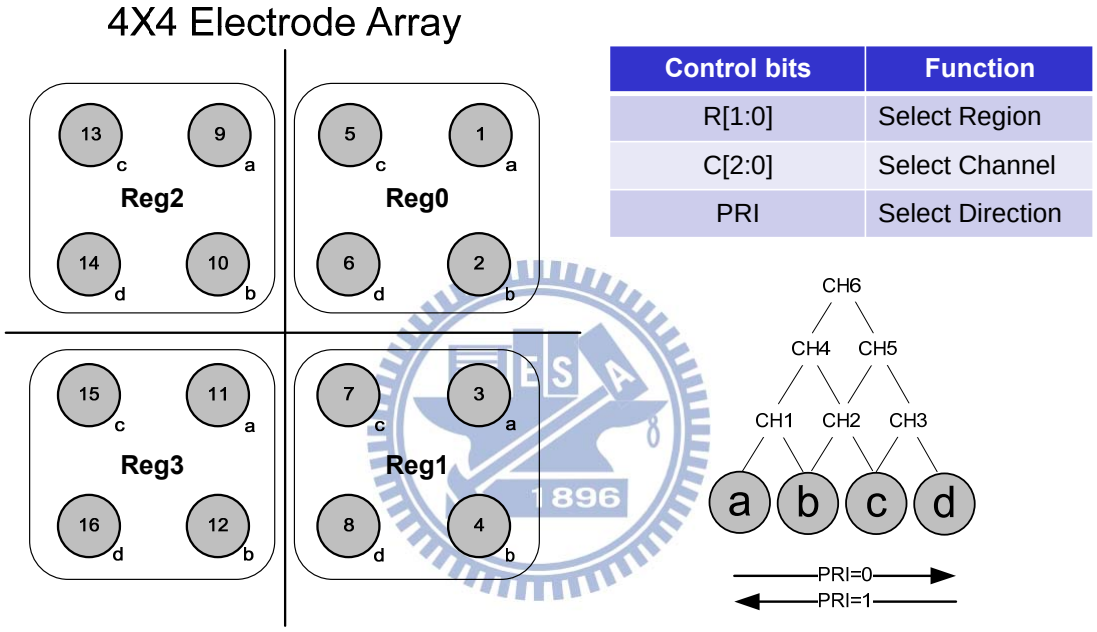


Fig. 3.3.4 4x4 electrode array.

3.3.2 Voltage Limiting Technique

The maximum voltage of the 0.18μm standard CMOS process I/O devices is 3.3V. To prevent the devices from junction breakdown or gate oxide breakdown, we need ensure any two points voltage of all devices smaller than this value (3.3V). Fig. 3.3.5 shows the concept of the voltage limiting technique. The main idea is to control the source voltage of a transistor by giving a suitable gate voltage. Taking transistor Mn for an example, if there is no current (Fig. 3.3.5 (a)) through Mn, the source voltage of Mn will be charged up by leakage current until it is equal to its gate voltage. Otherwise, if

there is a current flowing (Fig. 3.3.5 (b)) through Mn, the aspect ratio of the transistor is designed to be large enough so that the V_{GS} of Mn are slightly larger than the threshold voltage (V_{th}). The drain voltage of Mn is controlled by the source voltage of the transistor cascaded above. The body node of every transistor is connected to its own source node to prevent large voltage leading gate oxide breakdown so that the deep N-well layer is used to isolate the P-well region of each stacked NMOS from the common P-substrate. The structure of PMOS works in a similar way. Following this technique, when the gate voltages of all transistors are carefully determined, the transistors will not overstress in high voltage condition and have more reliability.

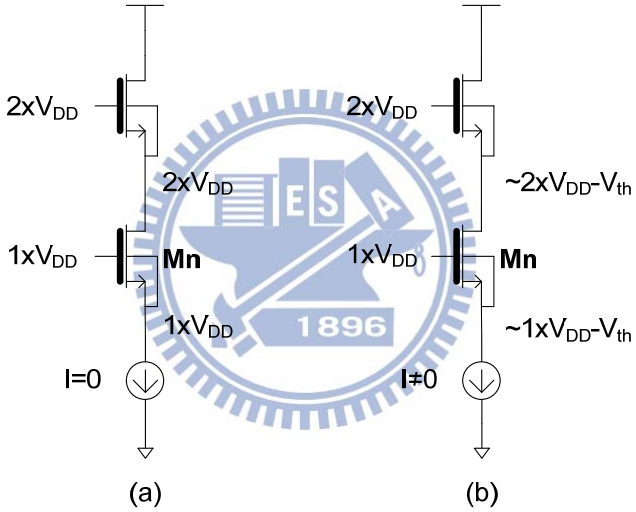


Fig. 3.3.5 Voltage limiting technique [24].

3.3.3 Stimulus Driver

The stimulus driver which is designed to tolerate $4xV_{DD}$ high voltage is modified by [25]-[28]. Fig. 3.3.7 shows the schematic of stimulus driver which needs $1xV_{DD}$, $2xV_{DD}$, and $3xV_{DD}$ bias. The driver is constructed from two parts, a self-adaption bias circuit (M_9~M_{14}) and stacked transistors (M_1~M_8) using voltage limiting technique. To prevent transistors overstressed problem during transient state, the protective diode D_1~D_6 is added. All the transistors in driver are 3.3V I/O devices. This driver can detect

the voltage of node OUT and use self-adaption bias circuit to dynamically adjust the suitable bias for stacked transistors to prevent overstressed problem.

To simply illustrate the complexity of driver operation, we set the driver circuit like a $4xV_{DD}$ high voltage-tolerant inverter (Fig. 3.3.6). However, the driver need connect a current source above the driver in reality (Fig. 3.3.7). When transistor M_8 is turned on and transistor M_1 is turned off, the high voltage ($4xV_{DD}$) delivers to node OUT. V_{n4}, V_{n5} and V_{n6} will increase to $4xV_{DD}$, and transistors M_{11} and M_{12} will turn on. V_{n8} and V_{n9} will increase to $3xV_{DD}$. When V_{n8} increase to $3xV_{DD}$, transistor M_{14} will turn off and transistor M_{13} will turn on. $2xV_{DD}$ will deliver to V_{n7}. Because transistor M_1 is turned off, the I_{ds} of M_1~M_4 is zero and the V_{gs} of M_1~M_4 is zero. V_{n3} will equal V_{n8} which is $3xV_{DD}$. The same result about V_{n2}=$2xV_{DD}$ and V_{n1}=$1xV_{DD}$. Finally, all the transistors in driver will not be overstressed. In a similar way, when transistor M_8 is turned off and transistor M_1 is turned on, the low voltage (0) delivers to node OUT.

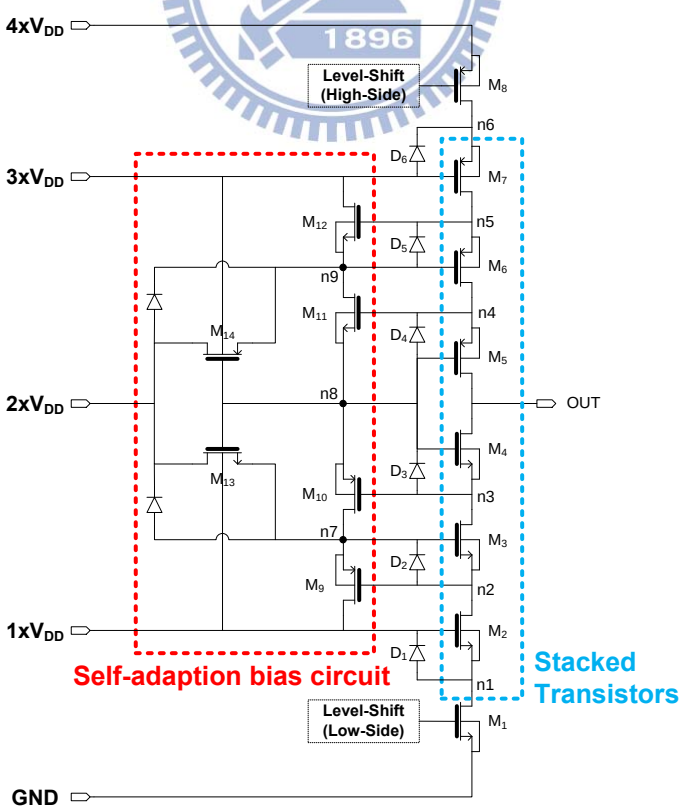


Fig. 3.3.6 $4xV_{DD}$ high voltage-tolerant inverter.

It is the same operation to accurately analyze in reality when we set a current source above the driver and a resistor as a load connecting node OUT (Fig. 3.3.8). Let the transistor M_8 be turned on and transistor M_1 be turned off, the current is delivered by transistors M_5~M_8 to resistor. To consider transient state, current source is set from small level to large level. Because of different current level, the voltage of node OUT will be set to a specific voltage. In the following, we will separate four voltage conditions at node OUT (~0, $1xV_{DD}$, $2xV_{DD}$, $3xV_{DD}$) to illustrate the voltage of all nodes in driver.

In the previous state, the quiescent voltage at the nodes n1 to n9 is 0, 0, 0, $1xV_{DD}$, $2xV_{DD}$, $3xV_{DD}$, $1xV_{DD}$, $1xV_{DD}$, $2xV_{DD}$ respectively and V_{OUT} is 0.

Firstly, when current source is a very small level, it makes V_{OUT} be almost zero. The voltage at the nodes n1 to n9 is ~0, ~0, ~0, $1xV_{DD}+V_{th}$, $2xV_{DD}+V_{th}$, $3xV_{DD}+V_{th}$, $1xV_{DD}$, $1xV_{DD}$, $2xV_{DD}$ respectively.

Secondly, when current source increases current, it makes V_{OUT} be $1xV_{DD}$. The voltage at the nodes n1 to n9 is ~$1xV_{DD}$, $1xV_{DD}$, $1xV_{DD}$, $1xV_{DD}+2V_{th}$, $2xV_{DD}+V_{th}$, $3xV_{DD}+V_{th}$, $1xV_{DD}+V_{th}$, $1xV_{DD}+V_{th}$, $2xV_{DD}$ respectively.

Thirdly, when current source increases current, it makes V_{OUT} be $2xV_{DD}$. The voltage at the nodes n1 to n9 is ~$1xV_{DD}$, ~$2xV_{DD}$, $2xV_{DD}$, $2xV_{DD}+2V_{th}$, $2xV_{DD}+3V_{th}$, $3xV_{DD}+V_{th}$, $2xV_{DD}$, $2xV_{DD}+V_{th}$, $2xV_{DD}+2V_{th}$ respectively.

Fourthly, when current source increases current, it makes V_{OUT} be $3xV_{DD}$. The voltage at the nodes n1 to n9 is ~$1xV_{DD}$, ~$2xV_{DD}$, ~$3xV_{DD}$, $3xV_{DD}+V_{th}$, $3xV_{DD}+V_{th}$, $3xV_{DD}+V_{th}$, $2xV_{DD}$, $3xV_{DD}$, $3xV_{DD}$ respectively.

When current increases, it makes V_{n4} and V_{n5} increase. As a result, it makes transistors M_{11} and M_{12} be turned on, then V_{n9} and V_{n8} increases. When V_{n8} increases, it makes transistor M_{14} be turned off and M_{13} be turned on. The Self-adaption bias circuit will track output voltage to decide the voltage at nodes n7, n8, and n9. As mentioned in

section of voltage limiting technique illustrates, when V_{n7}~V_{n9} is decided, the voltage at nodes n1 to n6 can be decided. Finally, all transistors in driver will not be overstressed when the voltage at out node is from 0 to $4xV_{DD}$.

The same concept can also illustrate that when transistors both M_8 and M_1 are turned off, the wide range voltage source (0~$4xV_{DD}$) put at output node. All the transistors in driver will not be overstressed either.

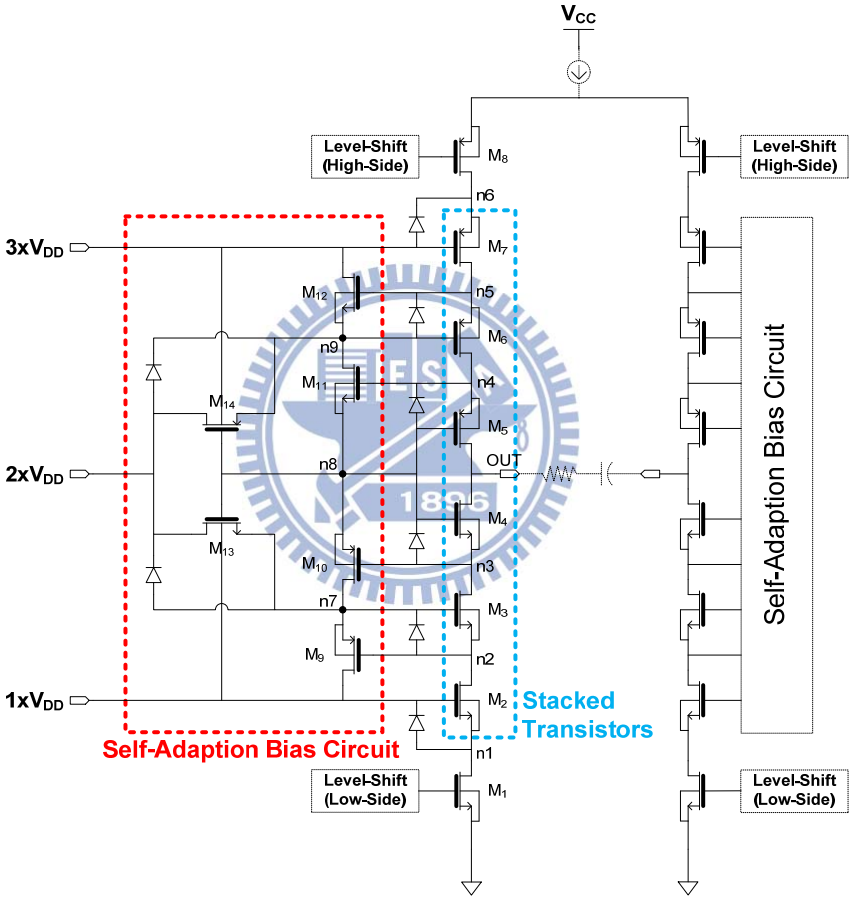


Fig. 3.3.7 High-voltage-tolerant stimulus driver.

3.3.4 Reference Voltage Generator

Fig. 3.3.8 shows the schematic of the reference voltage generator which divides Vcc into 3 levels ($1xV_{DD}$, $2xV_{DD}$, and $3xV_{DD}$) to provide the required reference voltages for the stimulus unit. All the transistors in bias circuit are 3.3V I/O devices.

Transistors M_{BN1}~M_{BN4}, M_{P1}~M_{P4}, and resistors R_1~R_3 perform the function of the voltage divider. Transistors M_{P1}~M_{P3} and M_{N1}~M_{N3} perform the function of the push pull output stage. The dimension of transistors and the resistance of the resistors are set to the same, so V_{nb1}, V_{nb2}, V_{nb3} will be $1xV_{DD}$, $2xV_{DD}$, $3xV_{DD}$. The gate voltage of M_{BP1} (V_{p1}) is $1xV_{DD}$-V_{THP} and the gate voltage of M_{BN2} (V_{n1}) is $1xV_{DD}$+V_{THN}. Thus, V_{bbn1} decided by transistors M_{P1} and M_{N1} is $1xV_{DD}$. For the same principle, V_{bbn2} is $2xV_{DD}$ and V_{bbn3} is $3xV_{DD}$. The transistors M_{P0} and M_{N0} is used for resisting process variation.

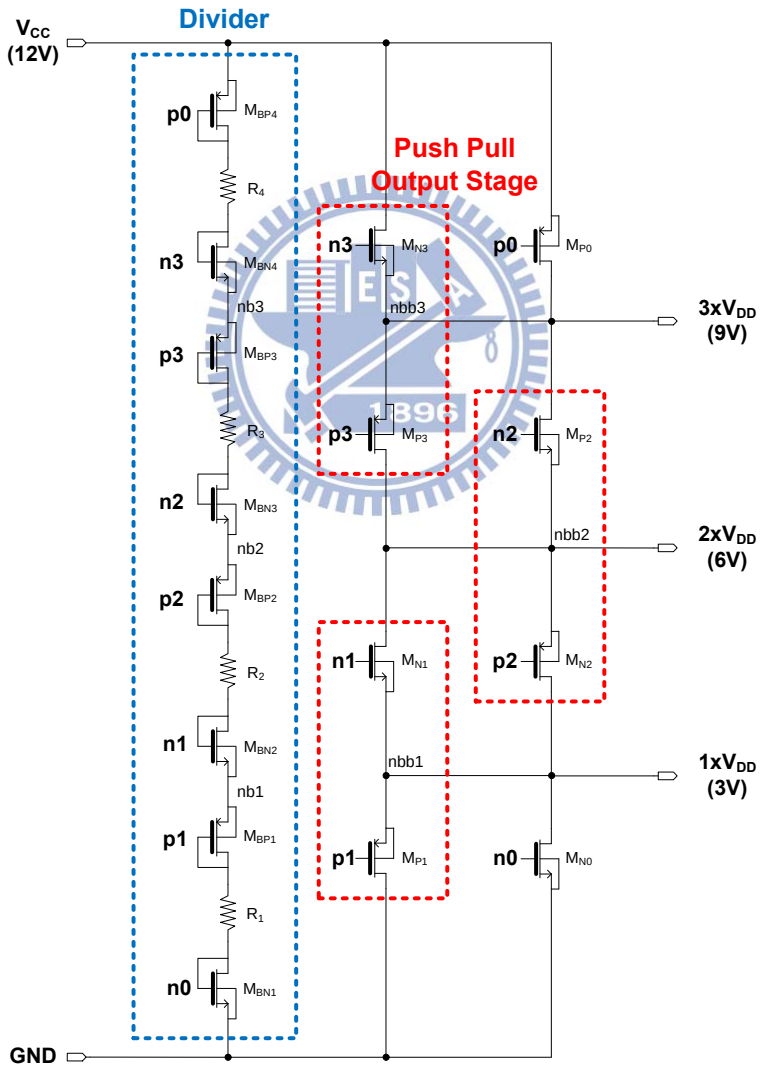


Fig. 3.3.8 Reference voltage generator.

3.3.5 Level-Shift

As discussed in section 3.3.3, the transistors M_1 and M_8 of the driver in Fig. 3.3.7 need to use level-shift to control it open and close. Thus, the Level-Shift (Low-Side) (Fig. 3.3.9) and Level-Shift (High-Side) (Fig.3.3.10) are proposed.

Level-Shift (Low-Side) is a common level shift circuit. The key point of design concept is that the size of transistors M_1 and M_3 must be larger than M_2 and M_4, so that V_{n2} will be pulled down to low voltage enough when input control signal is low (0V) to high (1.8V). Through the cross coupled pair, the positive feedback will let M_4 will be turned on and M_2 will be turn off when V_{n2} begins to be lower. Finally, the V_{n2} will have a full swing and the output can transit 0V to 3V. For the same principle, the input control signal is high (1.8V) to low (0V), the output will be 3V to 0V.

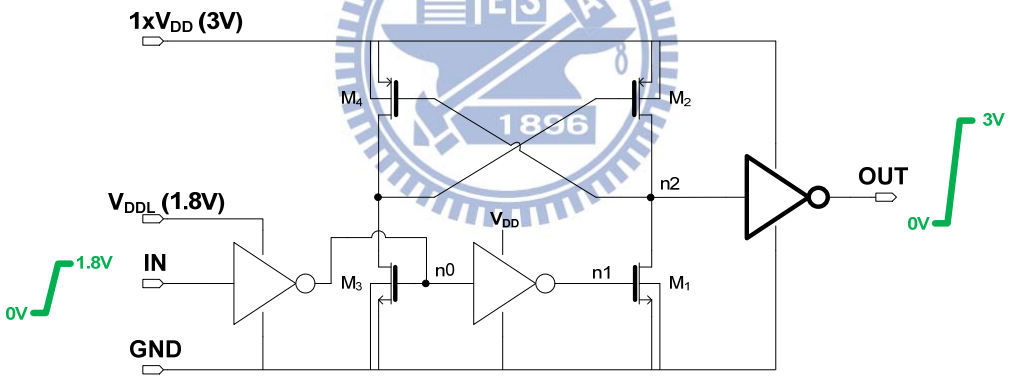


Fig. 3.3.9 Level-Shift (Low-Side).

Level-Shift (High-Side) can produce control signals which is operated in the range of $3xV_{DD}$ (9V) to Vcc (12V). To avoid overstressed issue, the Level-Shift (High-Side) consists of voltage limiting transistors. For an example to illustrate the circuit operate, when input control signal is low (0V) to high (1.8V), V_{na1} is pulled down to 0. Because of the gate voltage of M_{A2} and M_{A3} is $1xV_{DD}$, V_{na2} will be 0 and V_{na3} will be discharged to $1xV_{DD}$. Following this procedure, the V_{na1} to V_{na7} is 0, 0, $1xV_{DD}$, $1xV_{DD}$, $2xV_{DD}$,

$2xV_{DD}$, $3xV_{DD}$. In the other side, V_{n0} is 0 and there is no current at this path. Because of the gate voltage of M_{B2} is $1xV_{DD}$, V_{nb1} will be charged to $1xV_{DD}$. Following this procedure, the V_{nb1} to V_{nb7} is $1xV_{DD}$, $2xV_{DD}$, $2xV_{DD}$, $3xV_{DD}$, $3xV_{DD}$, $4xV_{DD}$, $4xV_{DD}$. Finally, the output will be 12V to 9V. For the same principle, the input control signal is high (1.8V) to low (0V), the output will be 9V to 12V. The same key point of design concept with Level-Shift (Low-Side), the size of M_{A1} to M_{A7} and M_{B1} to M_{B7} must be larger than M_{A8} and M_{B8} to let circuit normal operate.

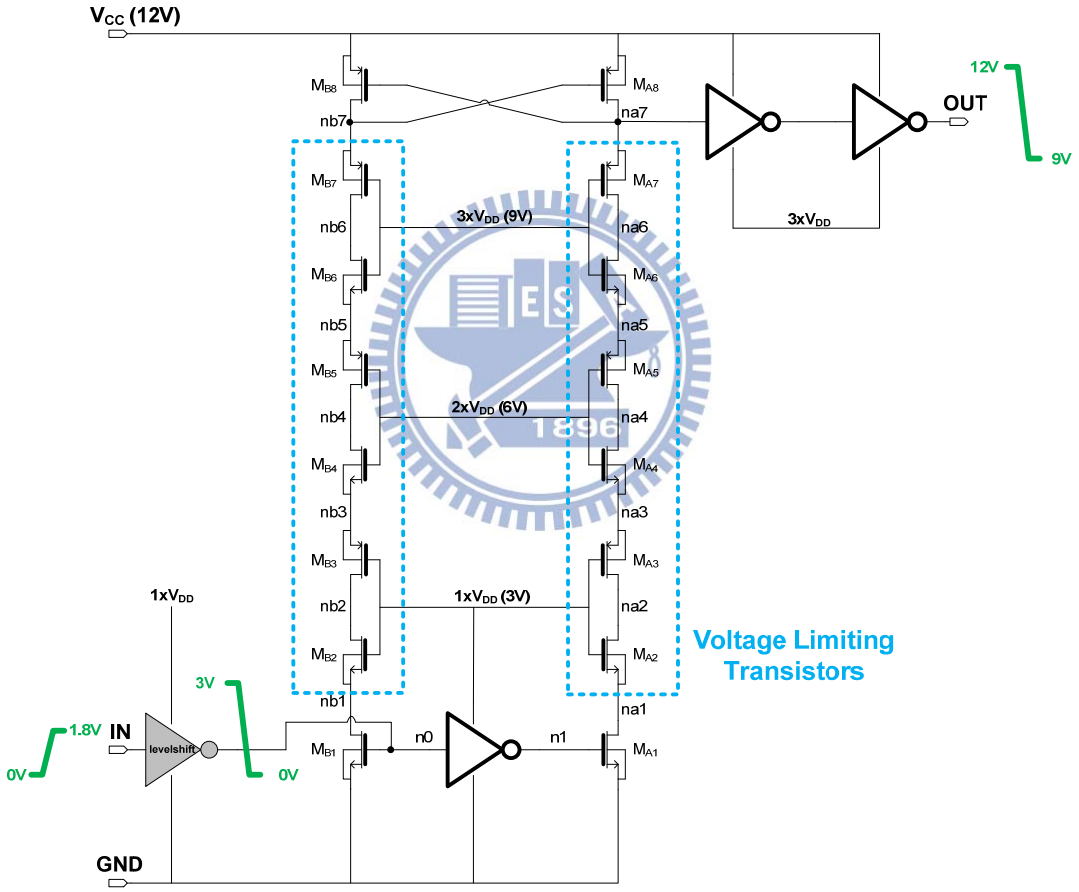


Fig. 3.3.10 Level-Shift (High-Side).

3.3.6 DAC & Current Source

Fig. 3.3.11 shows the schematic of DAC & current source. 5μA current is generated by the reference current source which has 3-bit trimming control pins to adjust current inaccuracy by process variation. 3-bit amplitude signals control the DAC to generate 5 to 30μA current (5μA per step). Then, the DAC current is multiplied by 100 times to the output (I_{OUT}) by current mirror. The voltage limiting transistors are used to avoid overstressed issue.

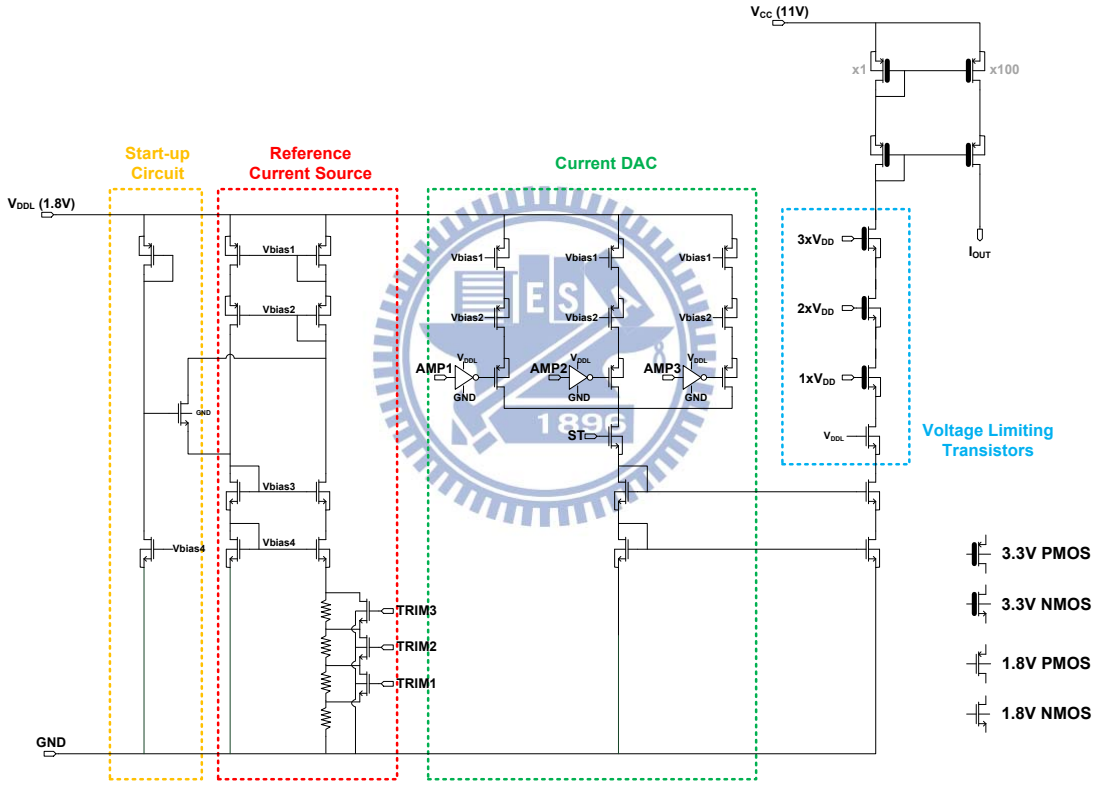


Fig. 3.3.11 DAC & Current source.

3.4 Simulation and Measurement Results

3.4.1 Simulation Results

The proposed stimulator had been simulated in HSPICE with UMC 0.18μm 1.8V/3.3V CMOS process. Fig. 3.4.1 shows the simulation result of the biphasic stimulus current (I_{ST}) at different amplitude and the 3.3V I/O devices overstressed test shows the gate-to-source, gate-to-drain, and drain-to-source voltages of all the transistors in stimulus driver. The simulation result observes that the driver is not overstressed in steady state but has maximum voltage of V_{DS5} which is 3.7V in transient state.

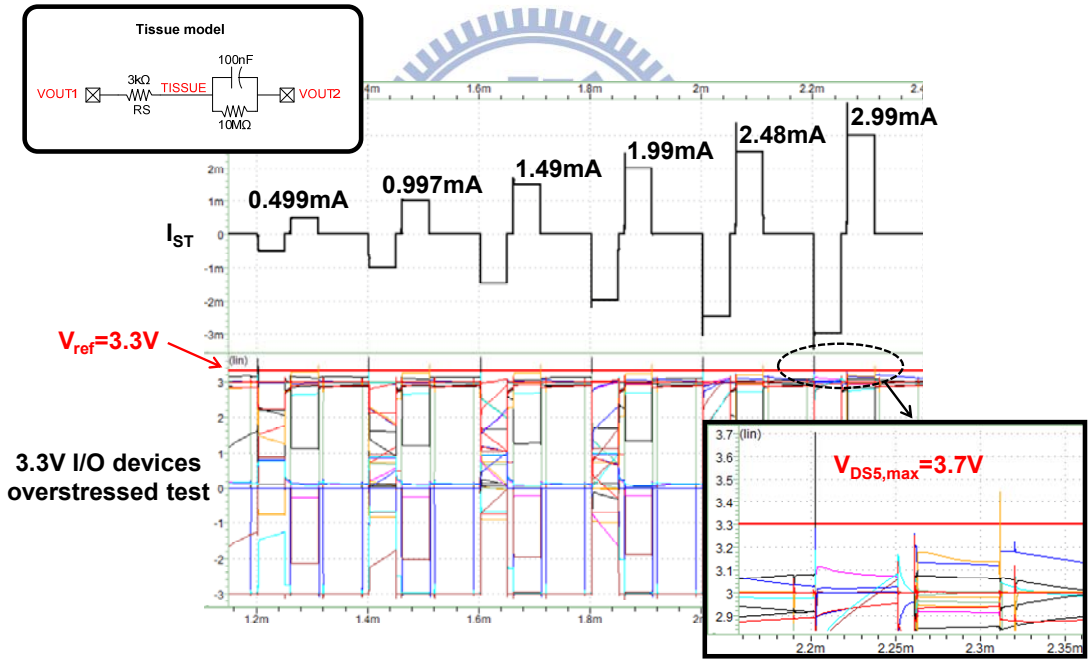
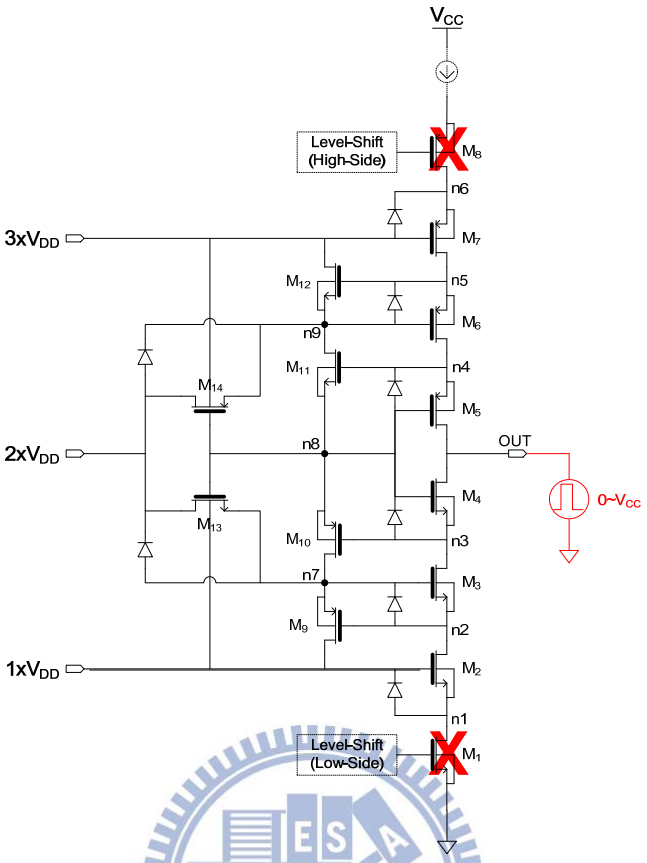
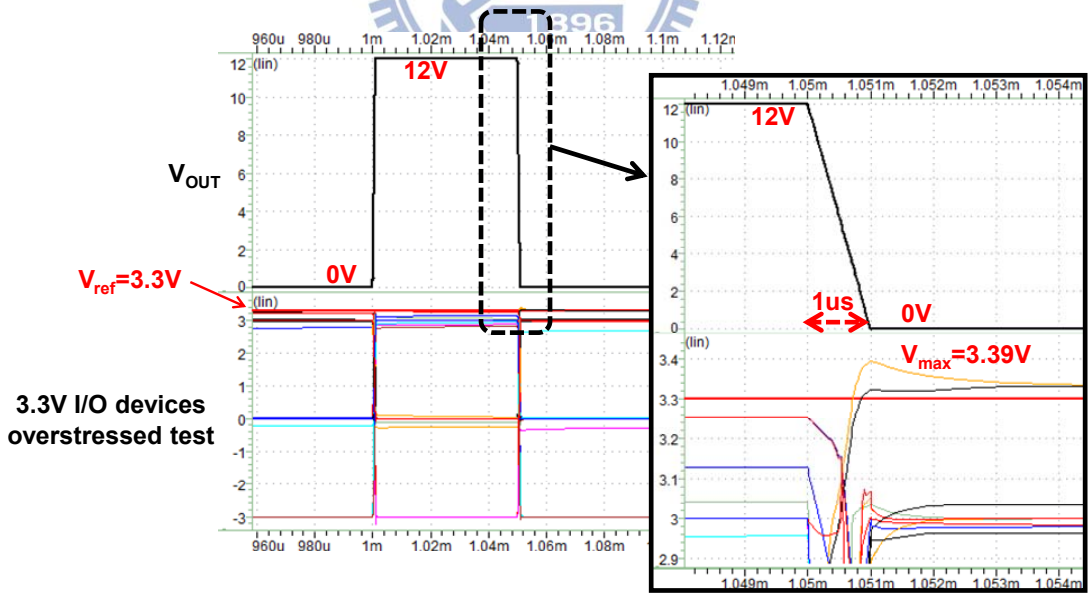


Fig. 3.4.1 The simulation result of all scale stimulus current.

To verify the stimulus driver will not have overstressed problem when another pair of drivers stimulates the tissue, Fig. 3.4.2 shows the simulation result of the stimulus driver by putting a ramp signal at output. When the ramp signal falls down from 12V to 0 V in 1μs, all the transistors in driver will not be overstressed.



(a) Turn off the switches M_1 and M_8, and put a 0V~12V ramp signal at output.



(b) The simulation result of 3.3V I/O device overstressed test.

Fig. 3.4.2 The simulation result of stimulus driver by putting a ramp signal at output.

Finally, Fig. 3.4.3 shows the simulation result of stimulus driver at power on state. All the transistors in the driver will not be overstressed and can normal be started.

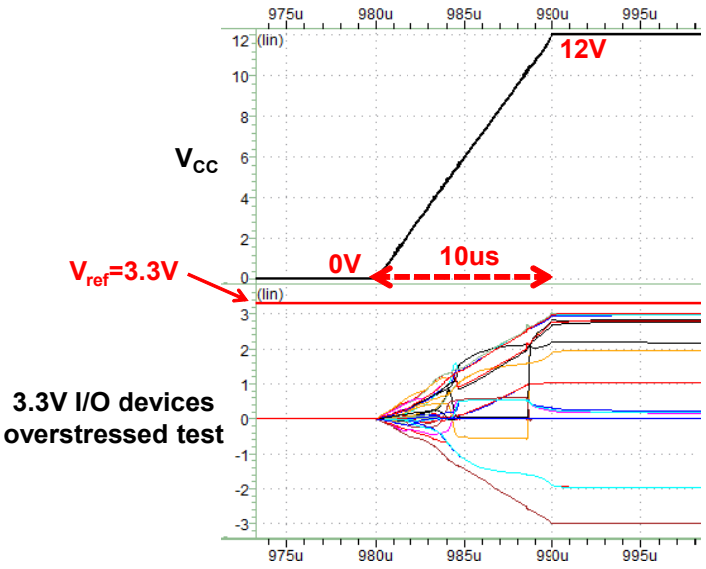


Fig. 3.4.3 The simulation result of stimulus driver at power on state.

3.4.2 Measurement Results

The proposed high-voltage-tolerance stimulus driver had been fabricated in UMC 0.18μm 1.8V/3.3V CMOS process. The microphotograph of the fabricated chip which includes 16 stimulus units, a reference voltage generator, DAC, and decoder is shown in Fig. 3.4.4. The total area is 1852 × 999.98 μm^2. The chip had been bonded on the PCB for measurement.

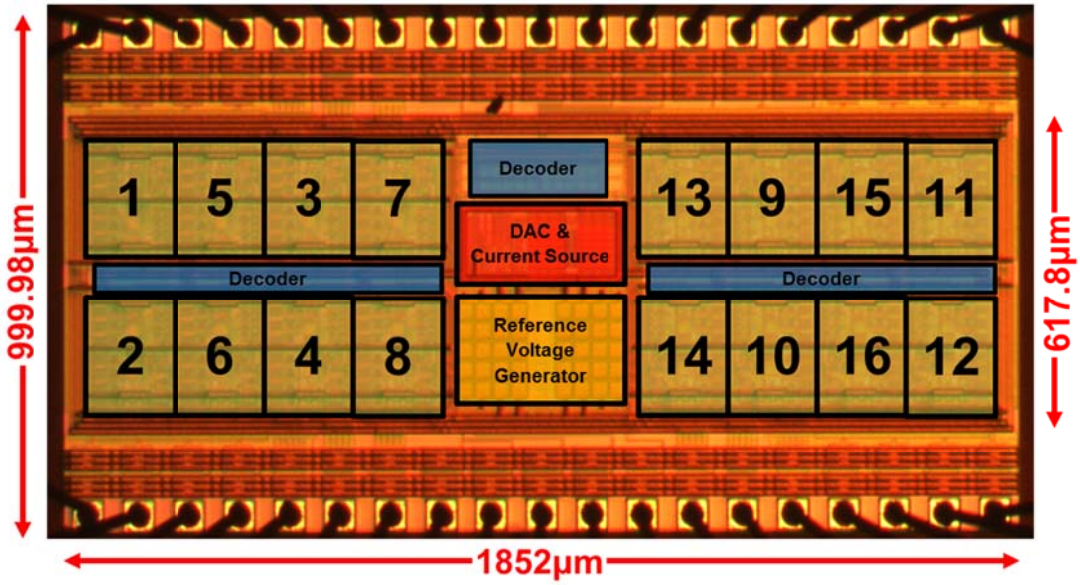
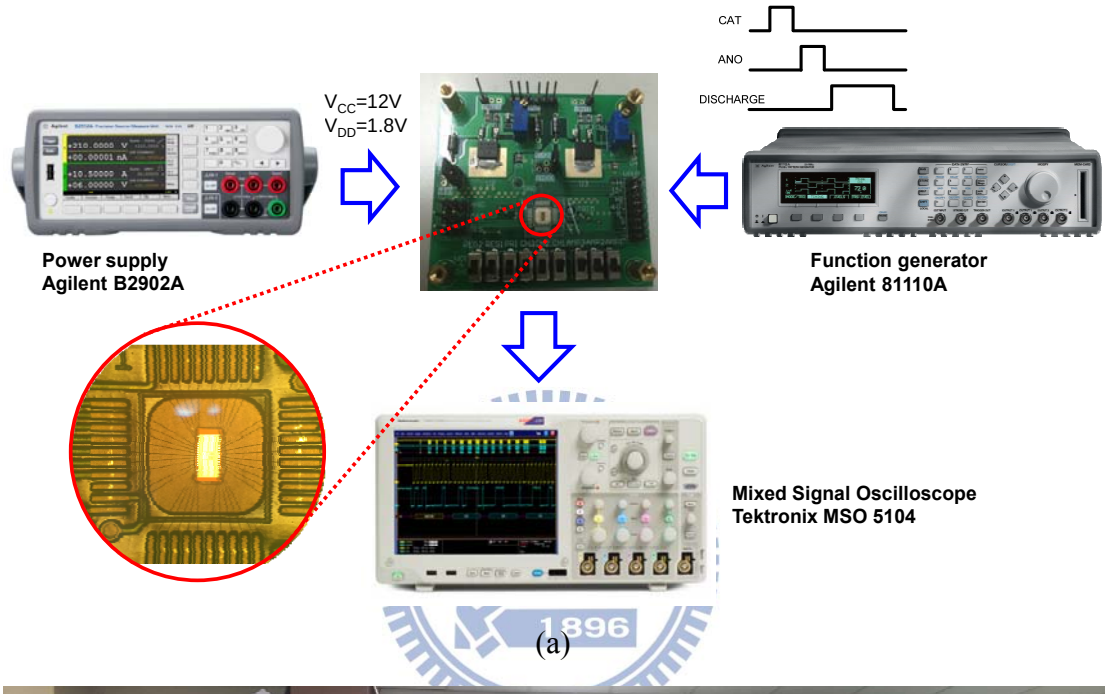
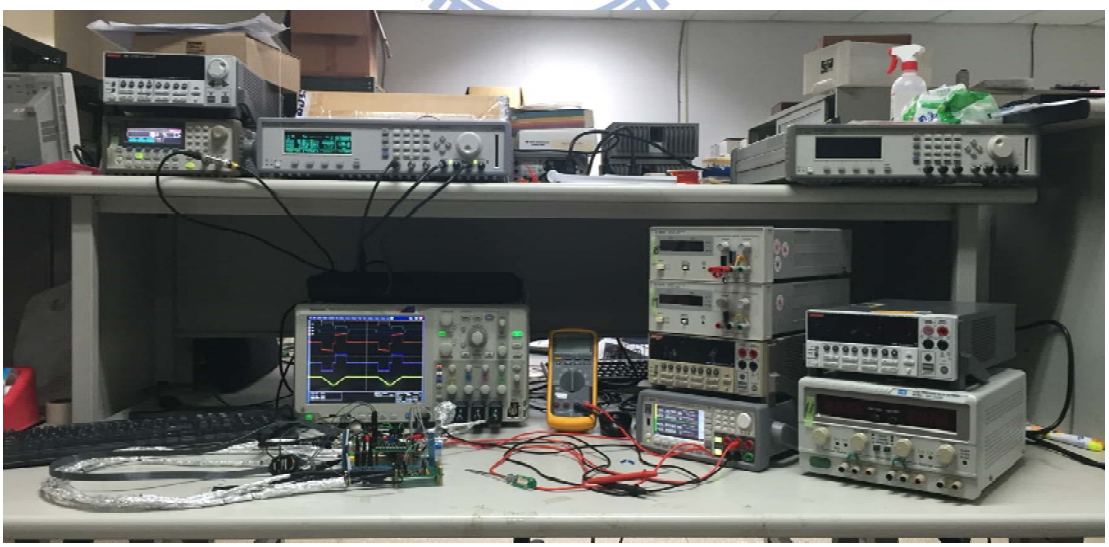


Fig. 3.4.4 The microphotograph of the fabricated stimulator chip.

Fig. 3.4.5(a) shows the measurement setup. Agilent B2902A is used to provide the fixed voltage 1.8V (V_{DD}) and 12V (V_{CC}) and it is also used to measure power consumption of the stimulator. Agilent 8110A is used to provide control signals CAT, ANO, and DISCHARGE. Tektronix MSO 5104 is used to observe the waveforms of the stimulation. The measurement environment is shown in Fig. 3.4.5(b).



(a)



(b)

Fig. 3.4.5 The measurement setup of the source meter, the function generator, the oscilloscope, and the chip is shown in (a). The measurement environment is shown in (b). The outputs of the stimulator are connected to test electrode-tissue equivalent circuit.

The tissue model R_S, C_{dl}, and R_f value are 3kΩ, 100nF, and 10MΩ. When the 3-bit amplitude signal is set to logic 010 (1mA), the pulse width of CAT signal and ANO signal are set to 50μs, the interphase delay between them is set to 10μs, and DISCHARGE signal is set to120μs, the biphasic stimulus waveform is measured in Fig. 3.4.6.

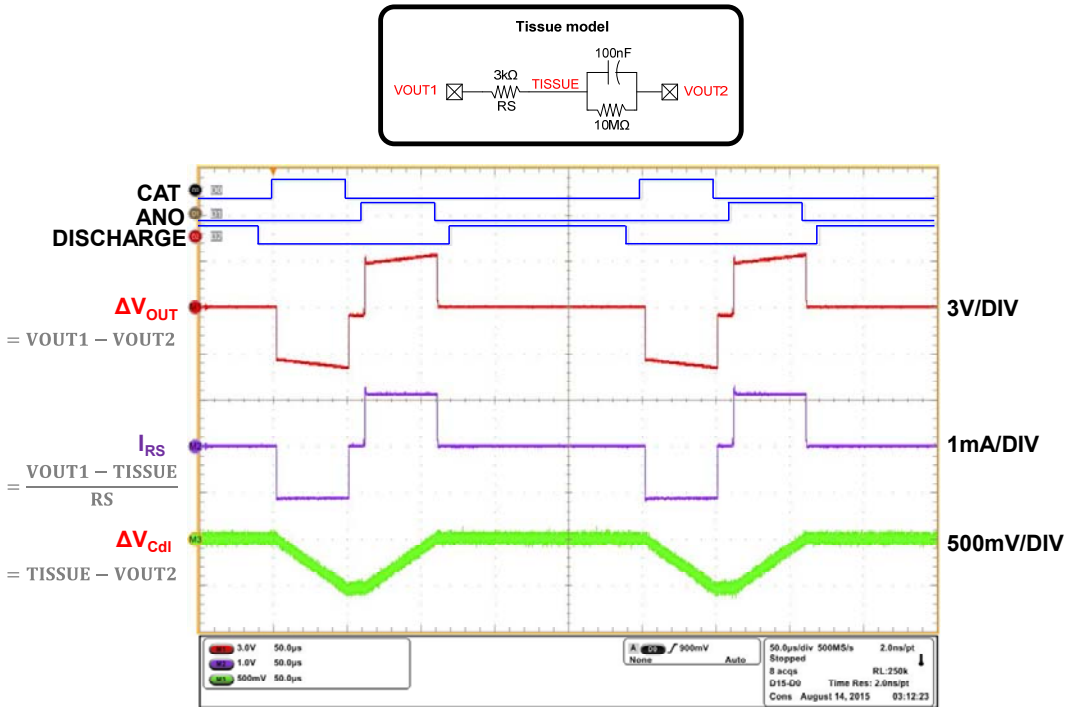


Fig. 3.4.6 The measurement result of stimulation.

To measure the stimulus current, we set only 1kΩ resistance at output. Fig. 3.4.7 shows the result of the stimulus current. Fig. 3.4.8 shows the line graph of cathodic current and anodic current. The current is 20% more than the specifications but still remain linear.

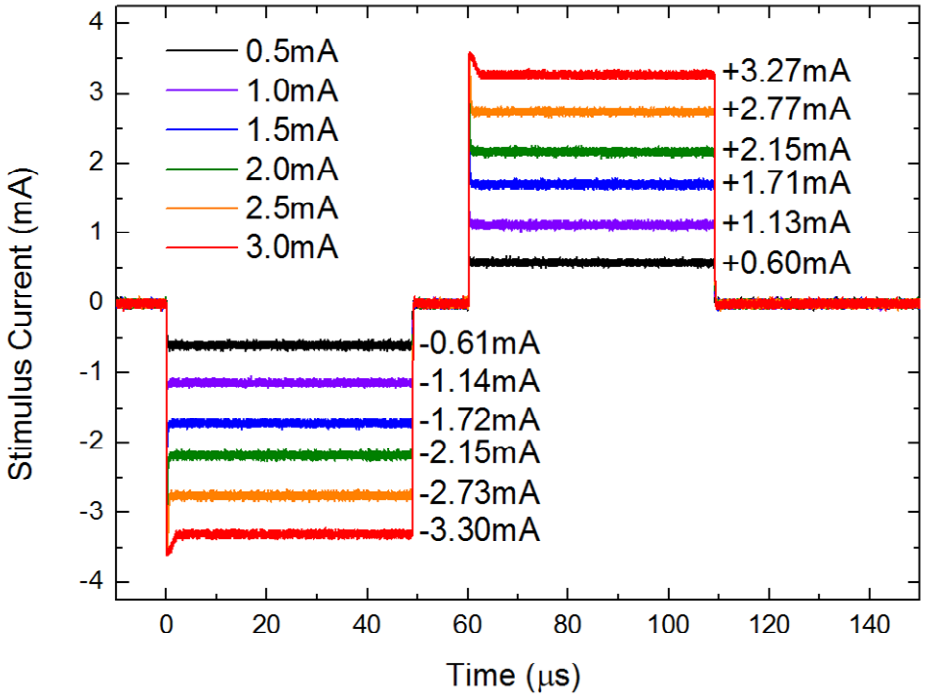


Fig. 3.4.7 The measurement result of all current levels.

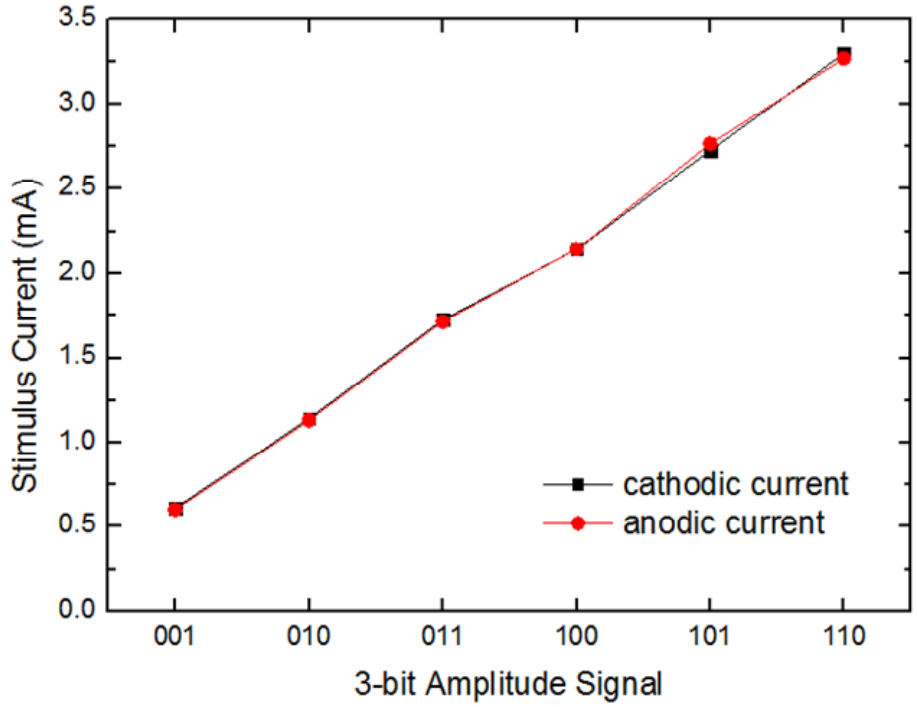


Fig. 3.4.8 The measurement result of comparing current and anodic current.

The precision of the current balance is obtained by measuring the residual voltage integrated on the 100nF Teflon capacitor at the end of the biphasic pulse. Fig. 3.4.9 shows the result of charge error. The tissue model is set by only R_S (1kΩ) and C_{dl} (100nF). To solve the dpi problem of oscilloscope, we set 10 continuous biphasic stimulations to observe the residual voltage on the capacitor. The 3-bit amplitude signal is set to logic 110 (3mA) and the pulse width of CAT signal and ANO signal are set to 100μs ($T_{stimulus}$). The ΔV_{ERROR} is 260mA, then the current mismatch is calculated as Eg. (3-1) and Eg. (3-2). The current mismatch under different region and different channel is shown in Fig. 3.4.10 and it is under 0.88% in all the condition.

$$\Delta V_{ERROR} = \frac{|I_{cat} - I_{ano}| \times T_{stimulus}}{C_{dl}} \quad (3\text{-}1)$$

$$\text{Current Mismatch} = \frac{|I_{cat} - I_{ano}|}{I_{cat}} \times 100\% \quad (3\text{-}2)$$

In order the calculate the residual DC current with discharge signal, first, Eq. (3-3) is used to illustrate the charge on C_{dl} during discharge phase.

$$q(t) = q(0) \times e^{-\frac{t}{RC}} \quad (3\text{-}3)$$

q(t) is the residual charge after discharge t second, q(0) is the residual charge before discharge, and RC is time constant. In this case, the time constant is 1kΩ×100nF=100μs and the discharge time is 500μs-(50μs+50μs+30μs)=370μs (assume the stimulus period is 500μs, the pulse width of stimulus time is 50μs, interphase delay is 10μs, the discharge control signal is given after 10μs, and the discharge control signal is turned off before 10μs by next pulse of stimulus beginning), so the allowed residual charge is reduced at least $e^{-3.7} \approx 1/40$. Then the residual dc current with discharge signal which can be calculated by Eq. (3-4) is 68nA.

$$\text{Residual DC Current} = \frac{I_{cat} \times \text{Current Mismatch} \times T_{stimulus}}{40 \times \text{period}} \quad (3\text{-}4)$$

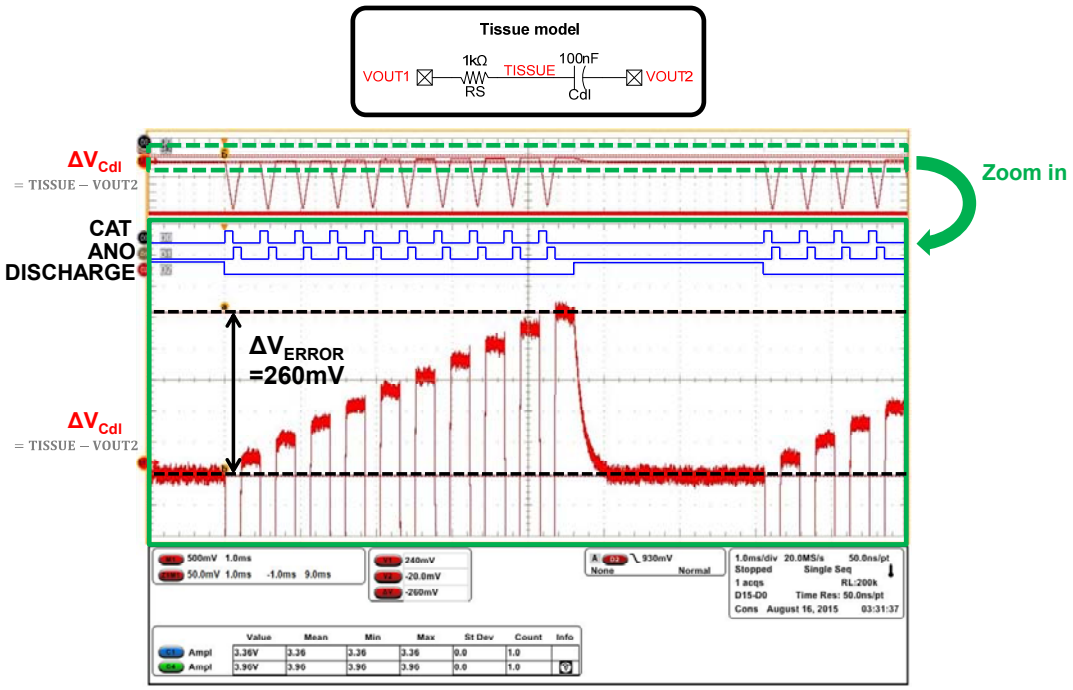
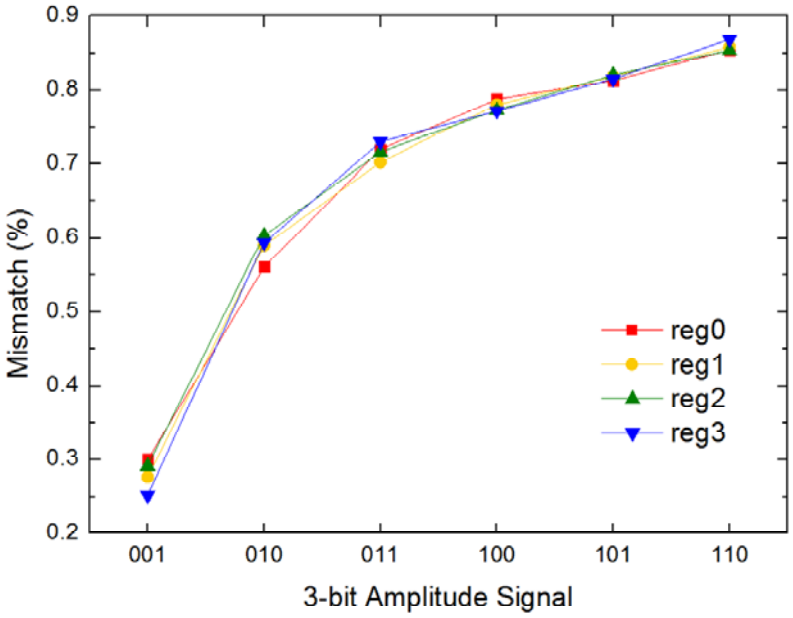
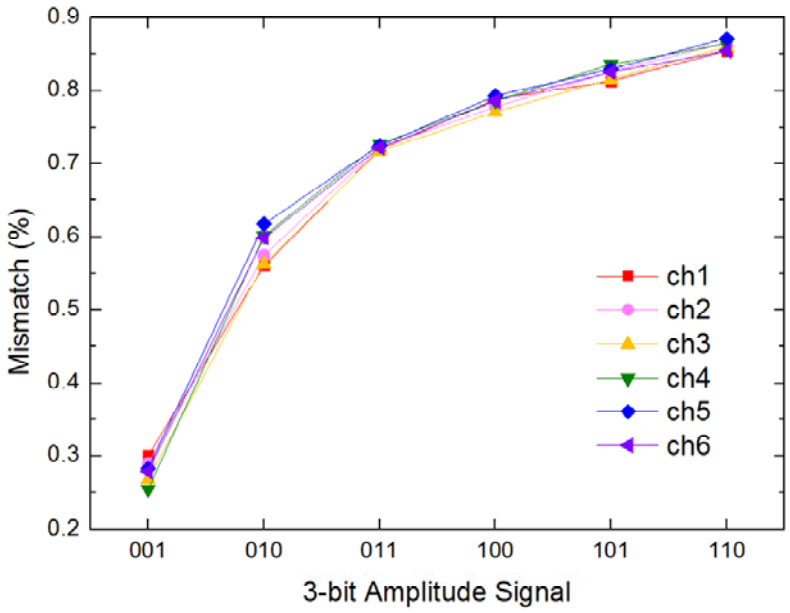


Fig. 3.4.9 The measurement result of mismatch error voltage on C_{dl}.



(a) Current mismatch (different region @ch=001)



(a) Current mismatch (different channel @reg=00)

Fig. 3.4.10 The measurement result of current mismatch.

To verify the function of multi-channel stimulation, the tissue model is set as Fig. 3.4.11 and the oscilloscope can observe the stimulus current change by adjust the 2-bit region control signal from 00 to 01.

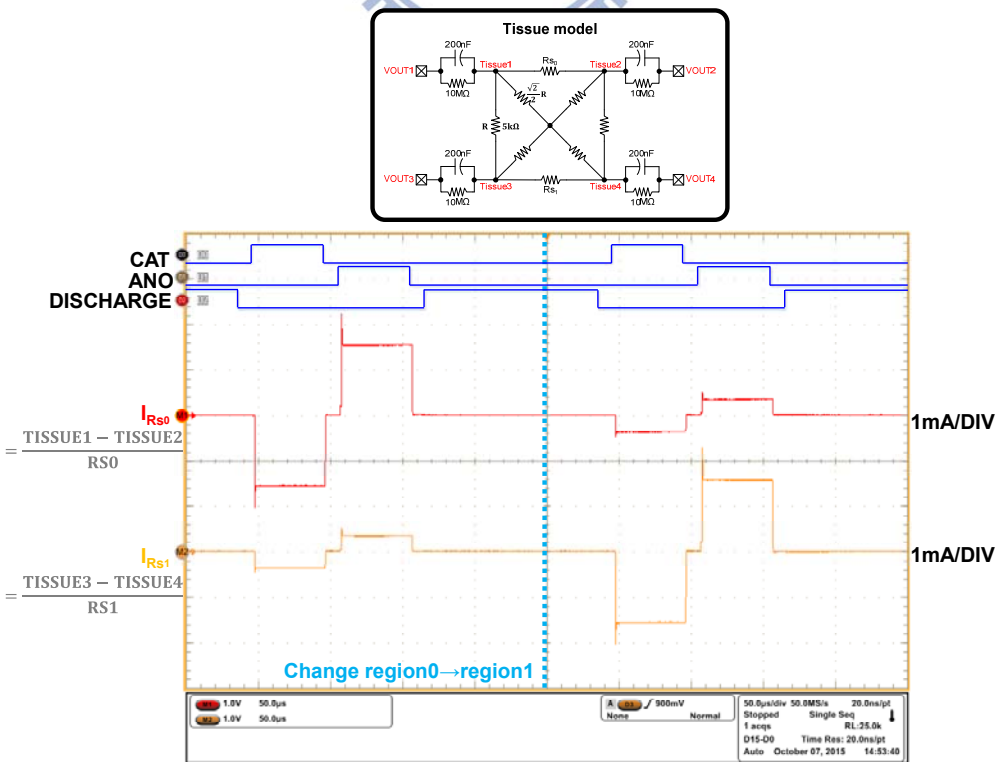


Fig. 3.4.11 The measurement result of changing region.

Fig. 3.4.12 shows the function of priority control signal. We can observe when the priority adjust from 0 to 1, the I_{RS} will change the direction of stimulus current for first cathode current to first anode current.

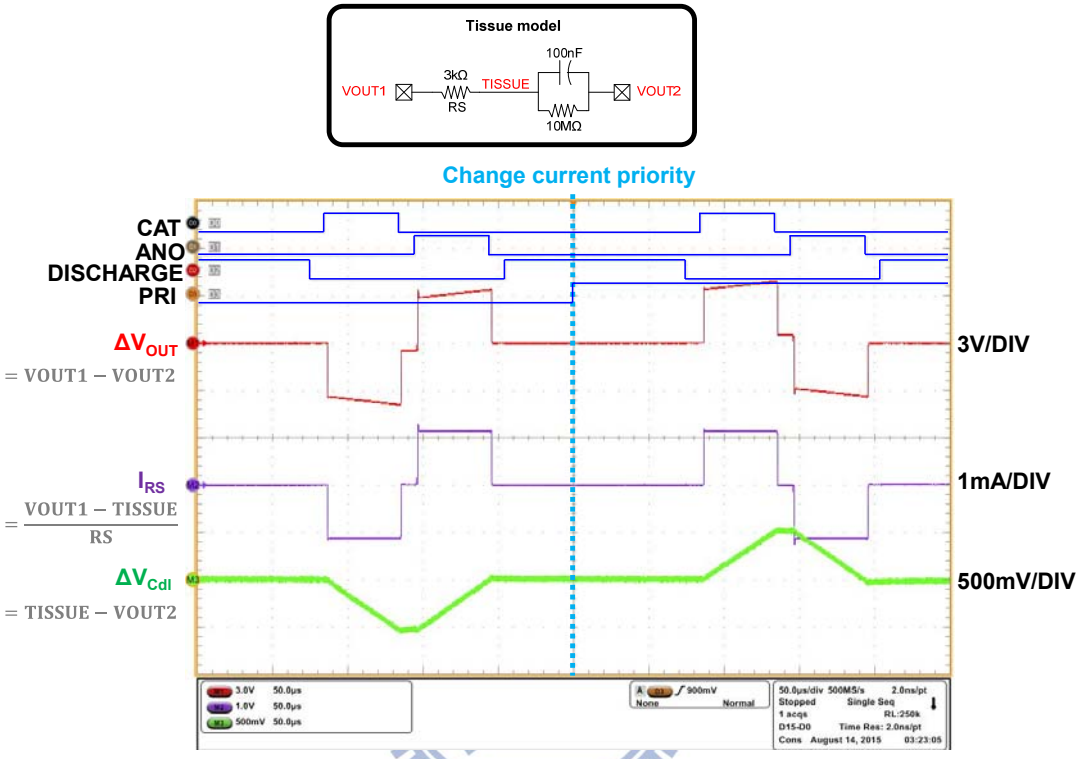


Fig. 3.4.12 The measurement result of changing priority.

3.5 Summary

The summary of the stimulator is shown in the Table 3.2. The measurement results approach the simulation results and conform to the specifications. In the measurement results, the cathodic/anodic matching is under 0.88%. The residual dc current is smaller than 70nA and the power consumption is 36.33uW (1.8V) and 10.02mW (12V) when the pulse width, period, and amplitude are set to 50μs, 500μs, and 3mA. The standby power is 23.7uW.

Table 3.2

Summary of high-voltage-tolerance stimulator measurement results.

	Spec.	Pre-layout simulation	Post-layout simulation	Measurement
V_{DD} (V)	1.8V			
V_{CC} (V)	12V			
Stimulus Current Amplitude (mA)	±0.5, ±1.0, ±1.5, ±2.0, ±2.5, ±3.0,	±0.50, ±1.00, ±1.51, ±2.00, ±2.50, ±3.01,	±0.50, ±0.99, ±1.49, ±1.99, ±2.49, ±2.99,	+0.60, -0.61, +1.13, -1.17, +1.71, -1.72, +2.15, -2.15, +2.77, -2.73, +3.27, -3.30,
Cathodic / Anodic Matching	minimum	0.52%	0.70%	≤0.88%
Residual DC Current Error (nA) (@biphasic, cat.=50us, ano.=50us, inter.=10us, dis.=370us period=500us, amp.=3mA)	<100nA	39nA	52.5nA	≤70nA
Power Consumption (W) (@biphasic, cat.=50us, ano.=50us, inter.=10us, period=500us, amp.=3mA) VDD=1.8V VCC=12V	minimum	29.51uW 8.73mW	29.43uW 8.65mW	36.33uW 10.02mW
Standby Power (W)	minimum	18.54uW	18.34uW	23.7uW
Process	UMC 0.18μm 1.8V/3.3V CMOS process			

Chapter 4

Design of 16-Channel Biphasic Stimulus Driver to Suppress Epileptic Seizure on Human Body in the Low Voltage Process

4.1 Introduction

In the circuit design of epileptic treatment for rats [14], the signal acquisition and stimulation are at different locations of cortex (Fig. 4.1.1 [29]). Different with rats, because of the path of signal acquisition and stimulation through the same electrode in human body, the stimulus driver on chapter 3 must be modified to add detect-mode function. Based on the proposed 16-channel high-voltage-tolerance stimulus driver which is already demonstrated without gate-oxide overstress, hot-carrier effect, and other reliability issues, the design of 16-channel biphasic stimulus driver with both detect-mode and stimulate-mode functions is proposed in this chapter.

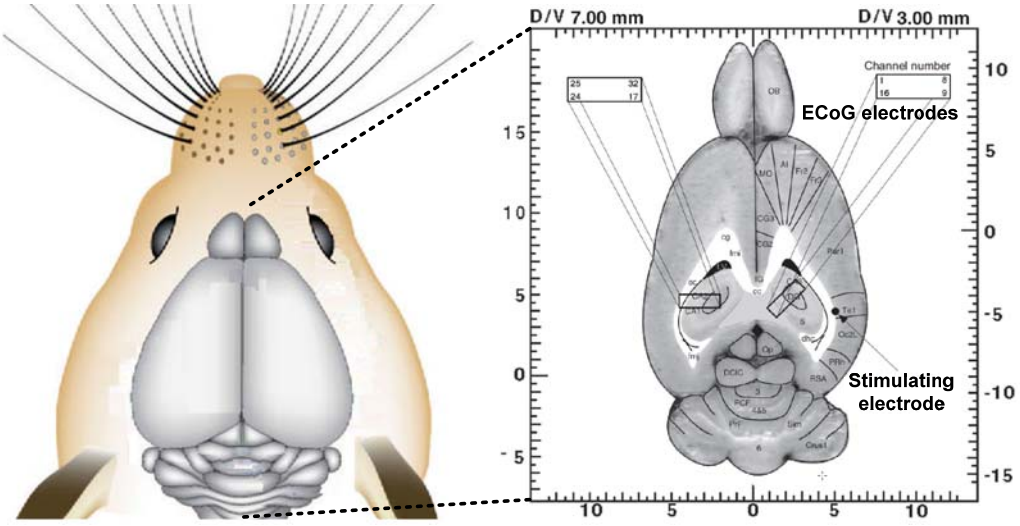


Fig. 4.1.1 The cortex of rats and the position of ECoG electrodes and stimulating electrode.

4.2 Design of 16-channel biphasic stimulus driver on SoC

4.2.1 Architecture

The modified stimulus driver is designed by two structures: driver ($SW_{\Phi 1a,b}$ and $SW_{\Phi 2a,b}$) and detect-switch (SW_{acq}). Fig. 4.2.1 shows a pair of drivers (2 channels) to illustrate how the stimulator works.

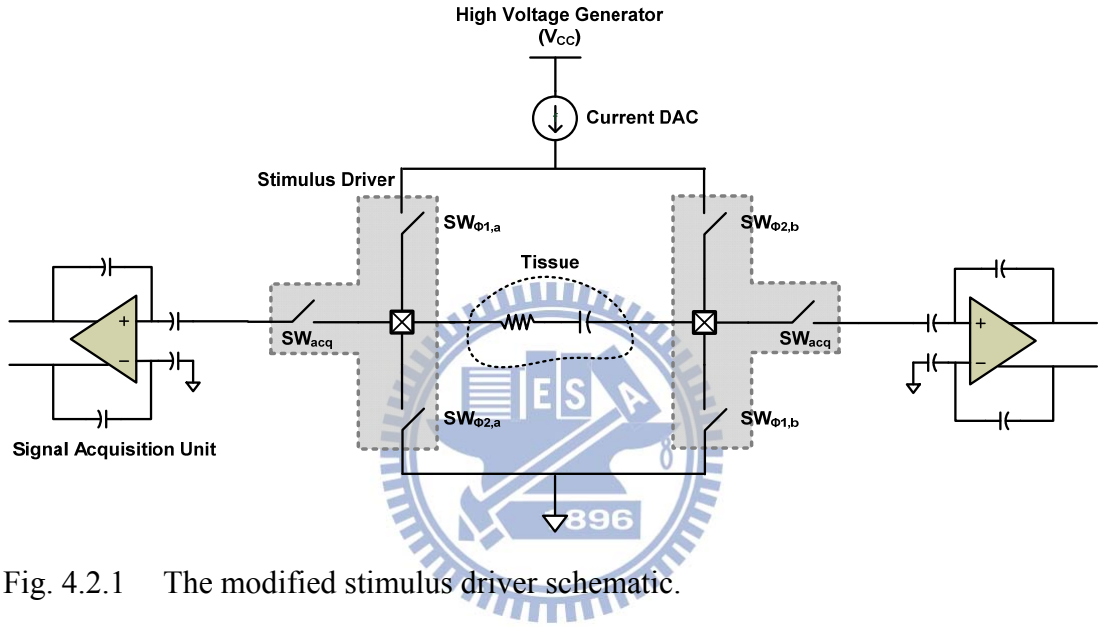


Fig. 4.2.1 The modified stimulus driver schematic.

The modified stimulus driver operates in two modes: detect-mode and stimulate-mode. In detect-mode (Fig. 4.2.2), the switch SW_{acq} is turned on and the switches $SW_{\Phi 1a,b}$ and $SW_{\Phi 2a,b}$ are turned off. The high voltage generator is at off state. The brain signal can deliver to signal acquisition unit.

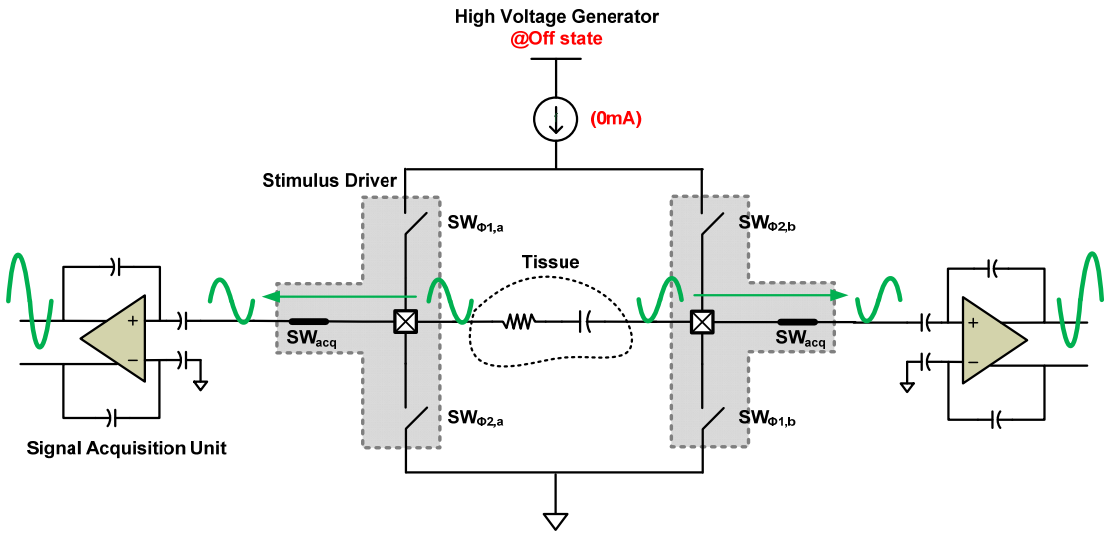


Fig. 4.2.2 The modified stimulus driver schematic. (operating at detect-mode)

In stimulate-mode (Fig. 4.2.3), the switch SW_{acq} is turned off. The operation of driver is the same with high-voltage-tolerance stimulator in section 3.3.1. The stimulus current is generated in three phases. Through controlling the switches $SW_{\Phi 1a,b}$ and $SW_{\Phi 2a,b}$, the cathodic, anodic, and discharge current can be generated.

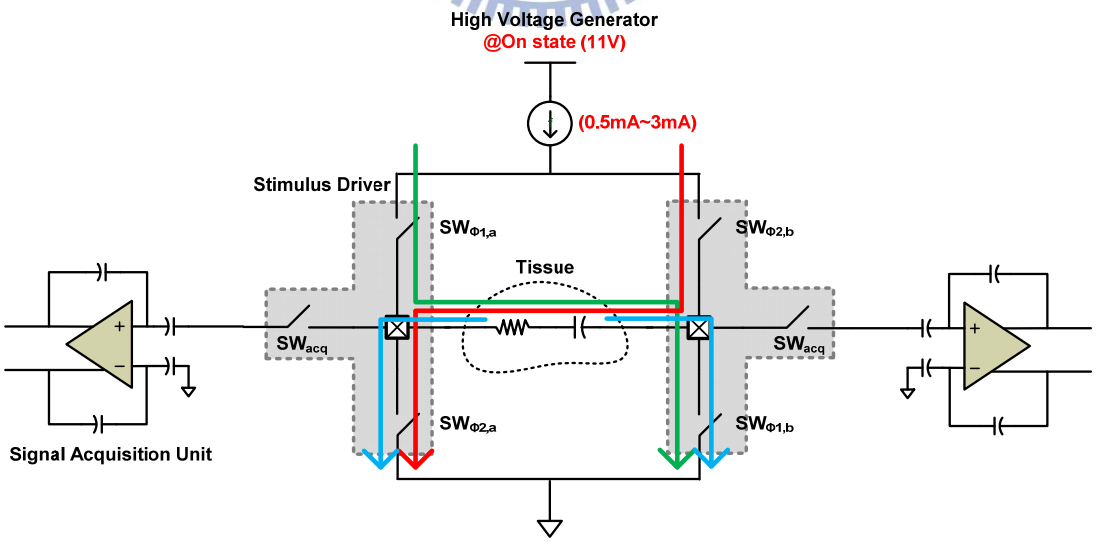


Fig. 4.2.3 The modified stimulus driver schematic. (operating at stimulate-mode)

The detail architecture of the stimulator which is shown in Fig. 4.2.4 consists of 16 stimulus units (stimulus driver, level-shift (high-side), and level-shift (low-side)), reference voltage generator, DAC, quick-discharge circuit, control signal circuit, LDO, level-shift (detect-mode), decoder and high voltage generator. In this case, the high voltage generator uses cross-couple charge pump and provides 11V to stimulator. However, the high voltage generator does not present in this work.

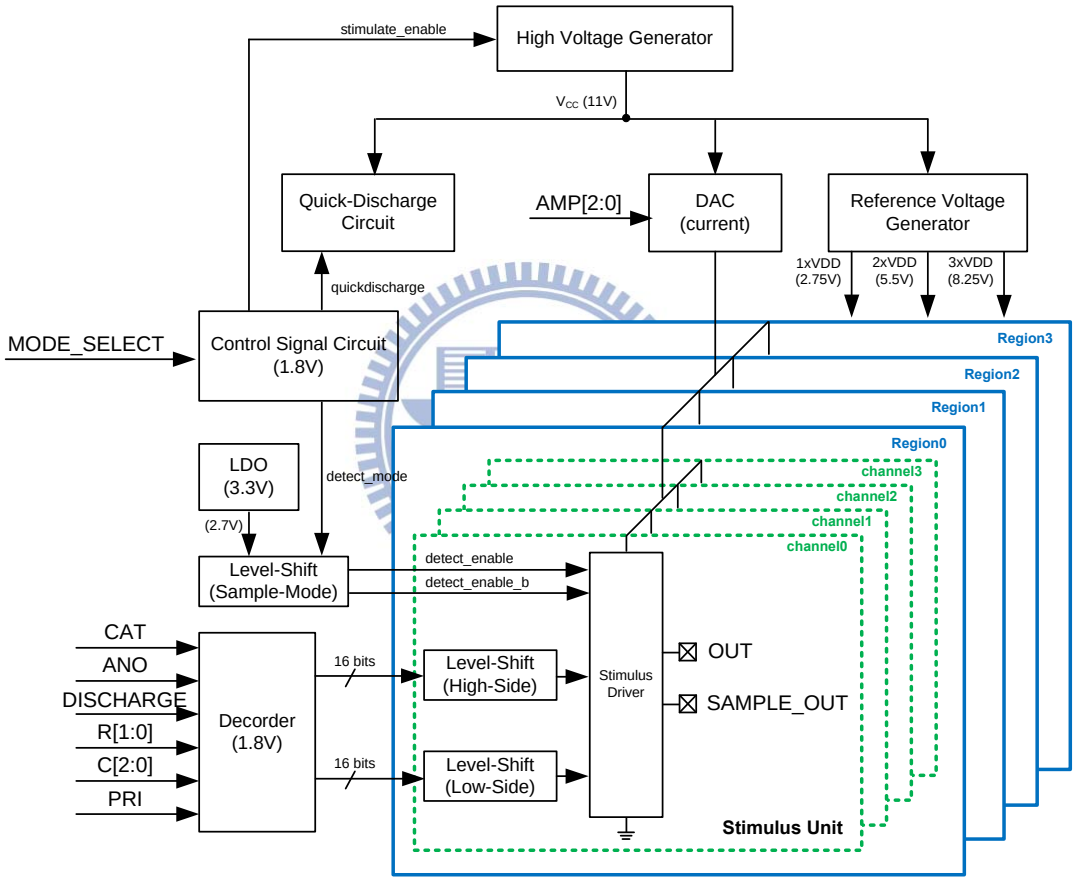


Fig. 4.2.4 16-channel biphasic stimulator block diagram.

4.2.2 Stimulus Driver

In the beginning, we mentioned that the path of signal acquisition and stimulation through the same electrode in human body. The stimulus driver based on this function is proposed as Fig. 4.2.5 and all the transistors in driver are 3.3V I/O devices. The stimulus driver is consisted of detect-switch (Fig. 4.2.6) and driver (Fig. 4.2.8) and operates in two modes: detect-mode and stimulate-mode.

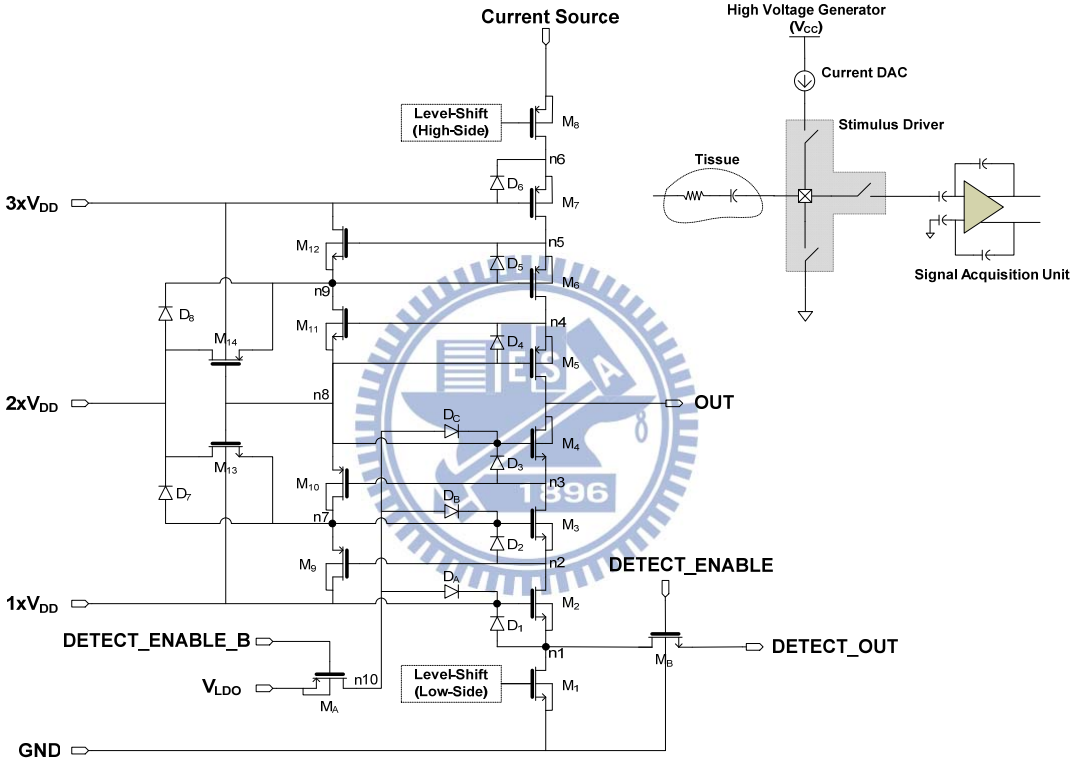


Fig. 4.2.5 Stimulus driver with detect-mode and stimulate-mode functions.

In the detect-mode, the brain signal through stimulus driver delivers to signal acquisition unit. The driver turns on the detect-switch as Fig. 4.2.6 and the high voltage generator is off state. The control pin DETECT_ENABLE is set to 2.7V and DETECT_EBABLE_B is set to 0V. The 2.7V generated by V_{LDO} through transistor M_A, diodes D_A, D_B, D_C delivers to the gate of M_2~M_3 (V_{n8}, V_{n7}, $1xV_{DD}$). When V_{n8} is charged to 2.7V, the transistor M_5 is turned off. Finally, the brain signal can deliver

through by transistors $M_{2\sim4}$, M_B from node OUT to node DETECT_OUT. To avoid leakage current in this path, the circuit needs other circuit to cooperate as Fig. 4.2.7.

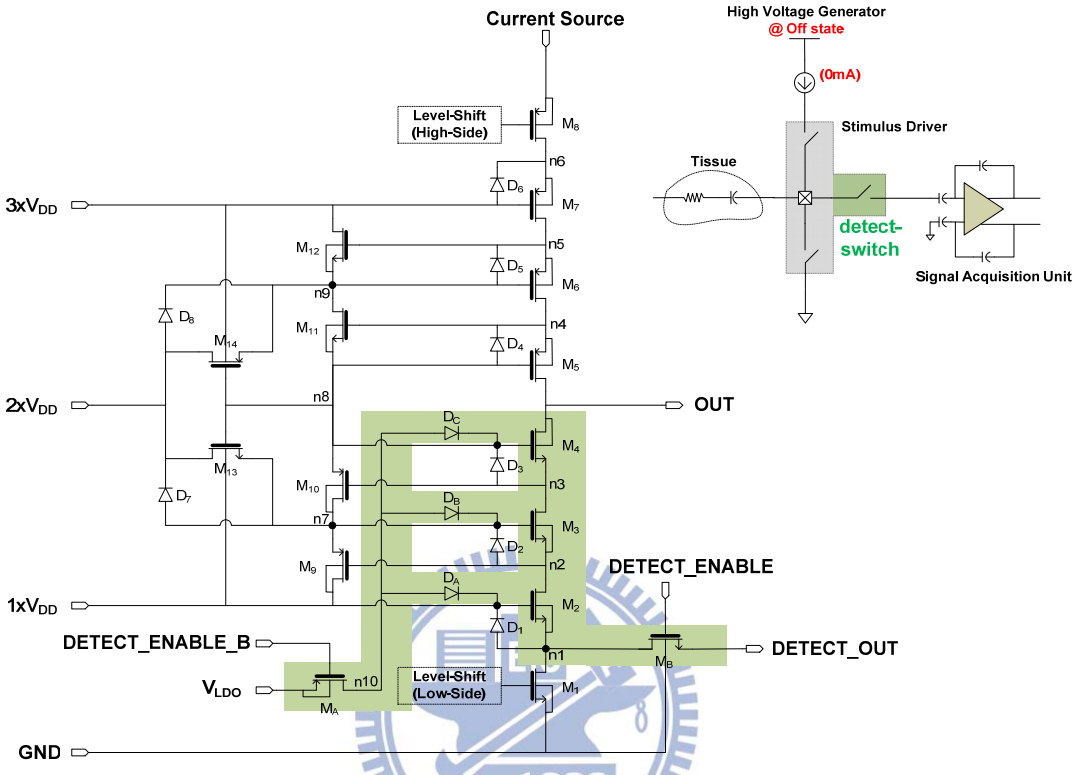


Fig. 4.2.6 Stimulus driver. (operating at detect-mode)

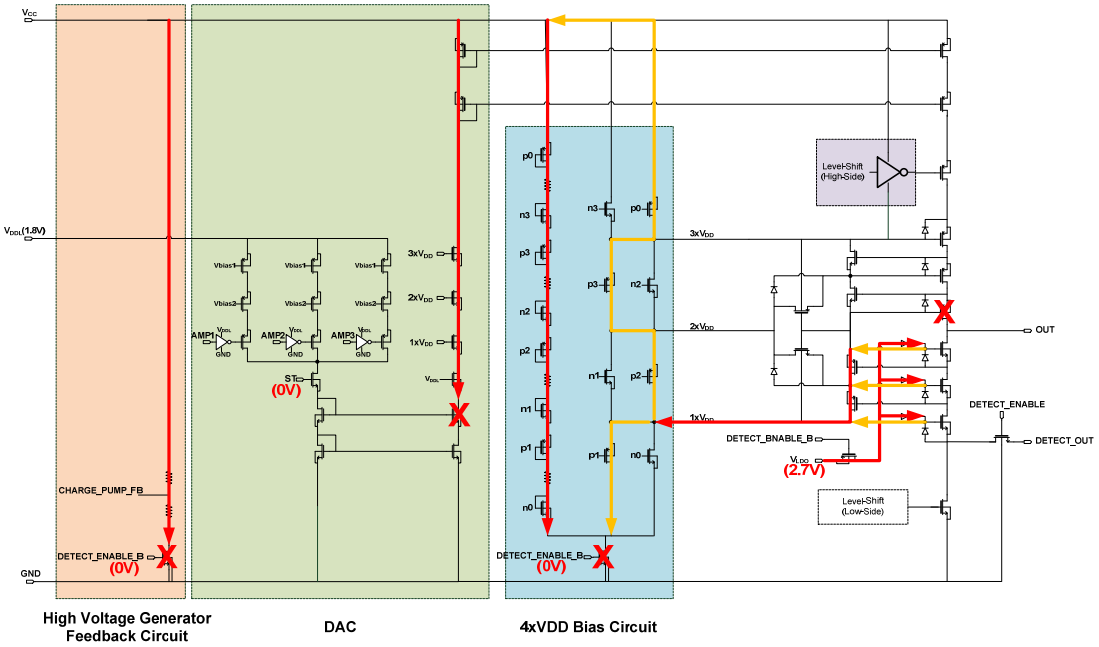


Fig. 4.2.7 Design to avoid leakage current path at detect-mode.

In the stimulate-mode, the stimulus driver needs to stimulate a constant current to tissue. In our measurement, the tissue resistor R_s is always about 3k ohm. When the stimulus current is 3mA, a high voltage 9V will be at output node. To be integrated into biomimetic systems and to achieve SoC, this work needs to be implemented in low-voltage process. The operation of modified stimulus driver in the stimulate-mode (Fig. 4.2.8) is the same in the concept of section 3.3.3. It can deliver low to high voltage to output node and ensure that all transistors will not be overstressed. The diodes D_A, D_B, D_C as off-state switch protect transistor M_A which will not be overstress in stimulate-mode. In this case, the diodes maximum reverse voltage is $3xV_{DD}$.

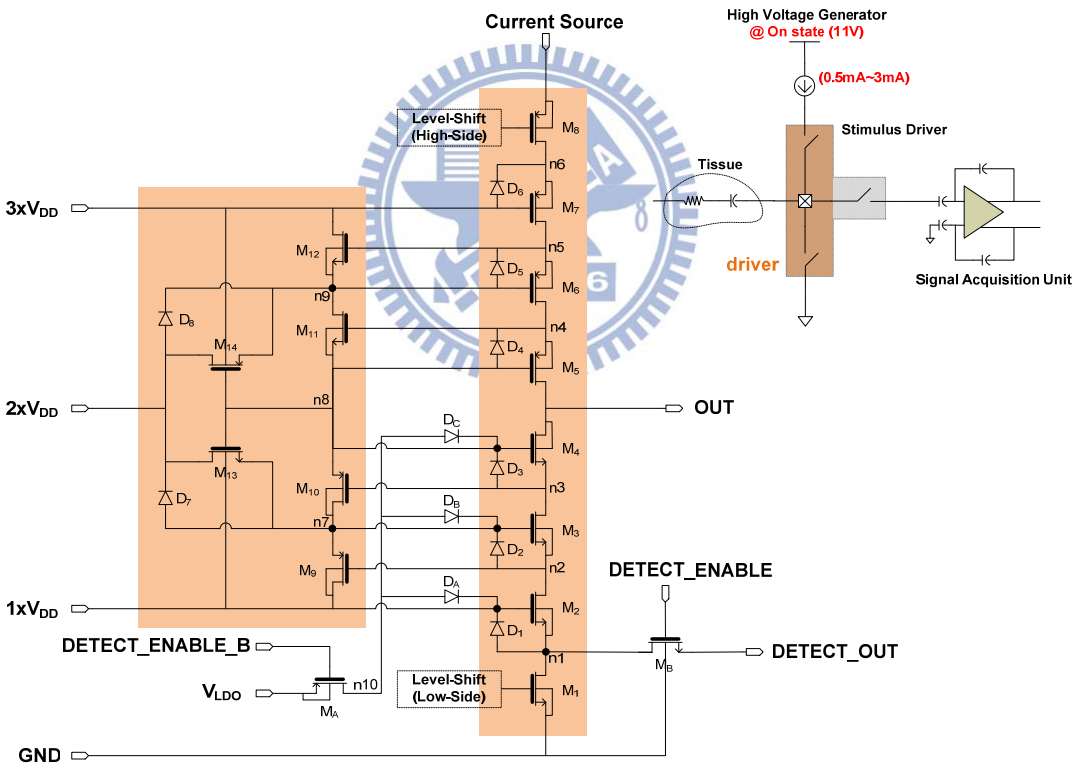


Fig. 4.2.8 Stimulus driver. (operating at stimulate-mode)

4.2.3 Voltage Reference Circuit

The bandgap voltage reference is used to generate the reference voltage of the LDO and quick-discharge circuit. Fig. 4.2.9 shows the implemented bandgap reference voltage circuit based on the architecture in [30]-[32]. The bandgap has high PSR through feedforward ripple cancellation. The basic idea is to feed the supply noise directly into the feedback loop and replicate ripples at the gate of the current mirror. By this way, it would reduce the drain current variation from the current mirror and allow the reference node to be less sensitive to the supply noise.

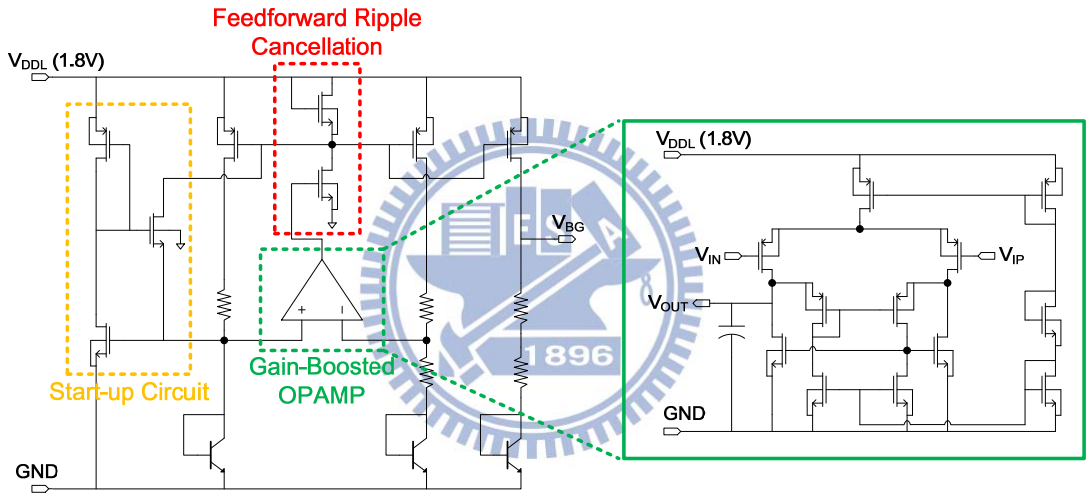


Fig. 4.2.9 Bandgap voltage reference.

4.2.4 Low Dropout Regulator

Because the brain signal is very small and sensitive, the low dropout regulator (LDO) is used to supply the clear bias as control signals for switches to stimulus driver at detect-mode. The proposed LDO is capacitance-free architecture shown in Fig. 4.2.10. All the transistors in the LDO are 3.3V I/O devices and the LDO can regulate 3.3V to 2.7V.

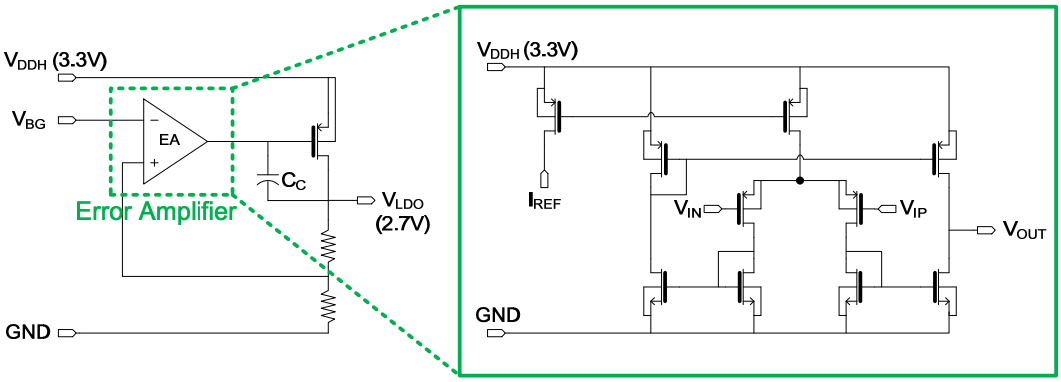


Fig. 4.2.10 Low Dropout Regulator.

4.2.5 Quick-Discharge Circuit

Fig. 4.2.11 shows the quick-discharge circuit which is used to discharge Vcc made by high voltage generator at initial stage of the detect-mode. To consider the overstressed problem, the circuit separate two discharge paths to discharge current. Firstly, the discharge current through I_{slave} which is limited by R_{limit} is very small. Secondly, when Va decreases under V_{BG}, the transistor M_1 will be turned on and the large discharge current through I_{master} will quickly discharge Vcc.

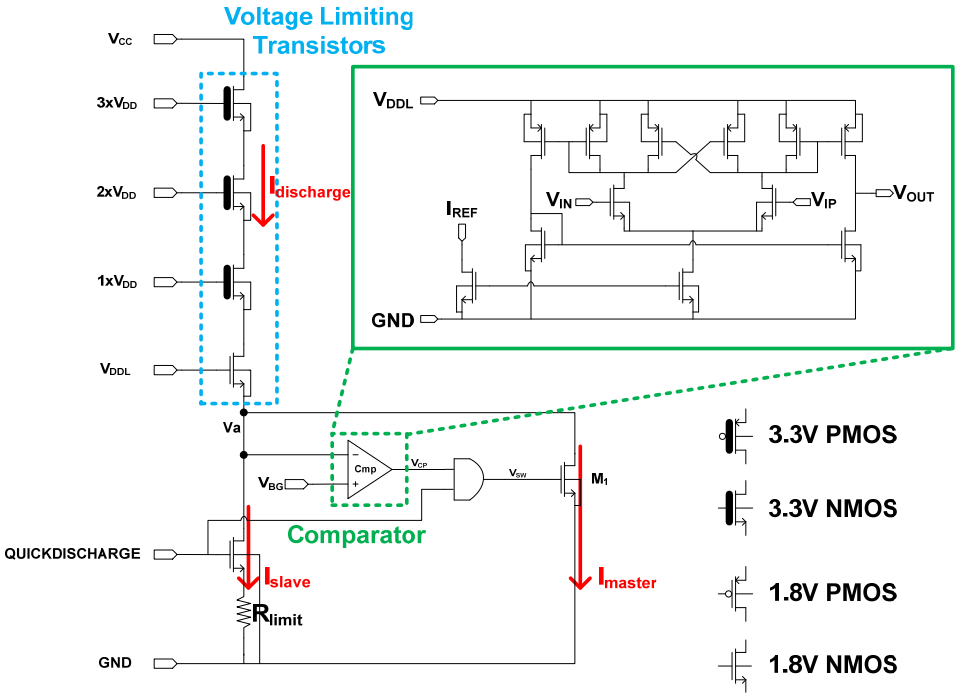


Fig. 4.2.11 Quick-Discharge Circuit.

4.3 Simulation Results

The modified stimulator had been simulated in HSPICE with TSMC 0.18μm 1.8V/3.3V CMOS process. Fig. 4.3.1 shows the layout photo of the 16-channel biphasic stimulator. The post-layout simulation results will be presented in the following.

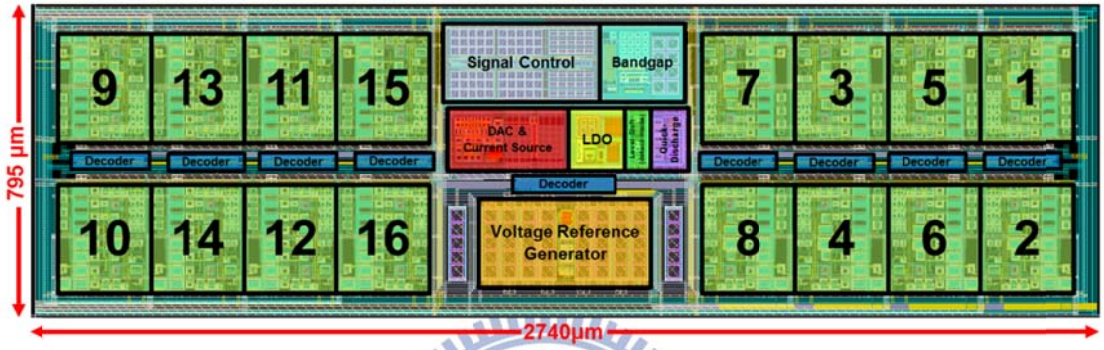
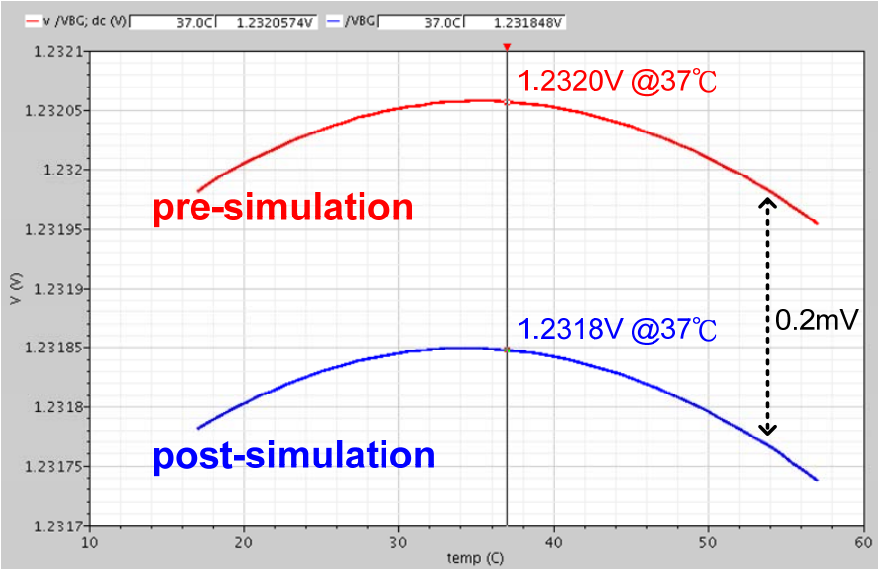
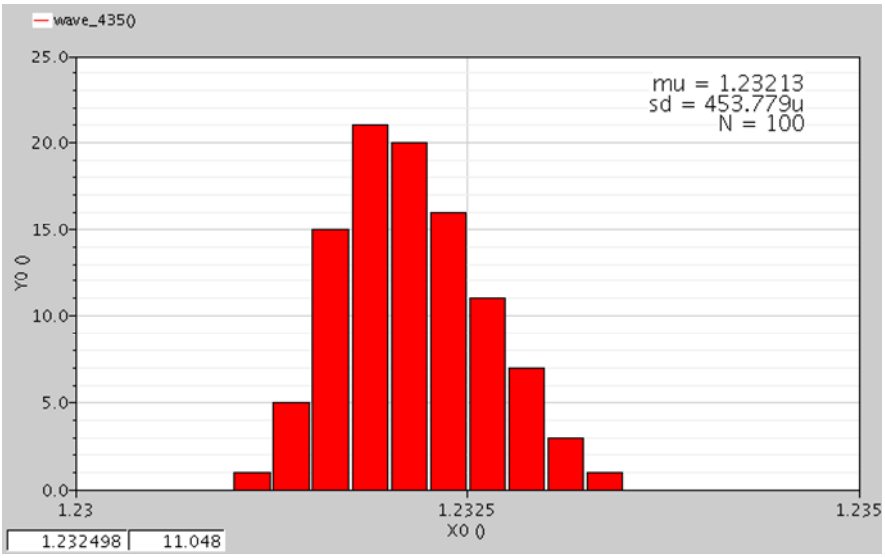


Fig. 4.3.1 The layout photo of the 16-channel biphasic stimulator.

Fig. 4.3.2 shows the results of bandgap reference circuit. In Fig. 4.3.2(a), the reference voltage is 1.2318V at 37°C by post-layout simulation result. The pre-layout simulation and post-layout simulation have different voltage which is 0.2mV. Fig. 4.3.2(b) shows the MONTE CARLO analysis and the result is presented the voltage is about 1.232V in different process corners and process mismatch.



(a) The results of pre-layout and post-layout simulations during different temperature.



(B) The results of post-layout simulation of MONTE CARLO analysis.

Fig. 4.3.2 The simulation result of bandgap voltage reference.

Fig. 4.3.3 shows the simulation result of quick-dischrge circuit. When control signal $V_{QUICKDISCHARGE}$ is 1.8V, the quick-discharge circuit will begin discharge the high voltage (V_{CC}) which is generated by charge pump by limited current 134uA. If V_{CC} decreases to the particular voltage, the comparator makes control signal V_{SW} be 1.8V and lets the larger discharge current 2.42mA quickly decrease V_{CC}. Through this protocol, all the transistors will not be overstressed.

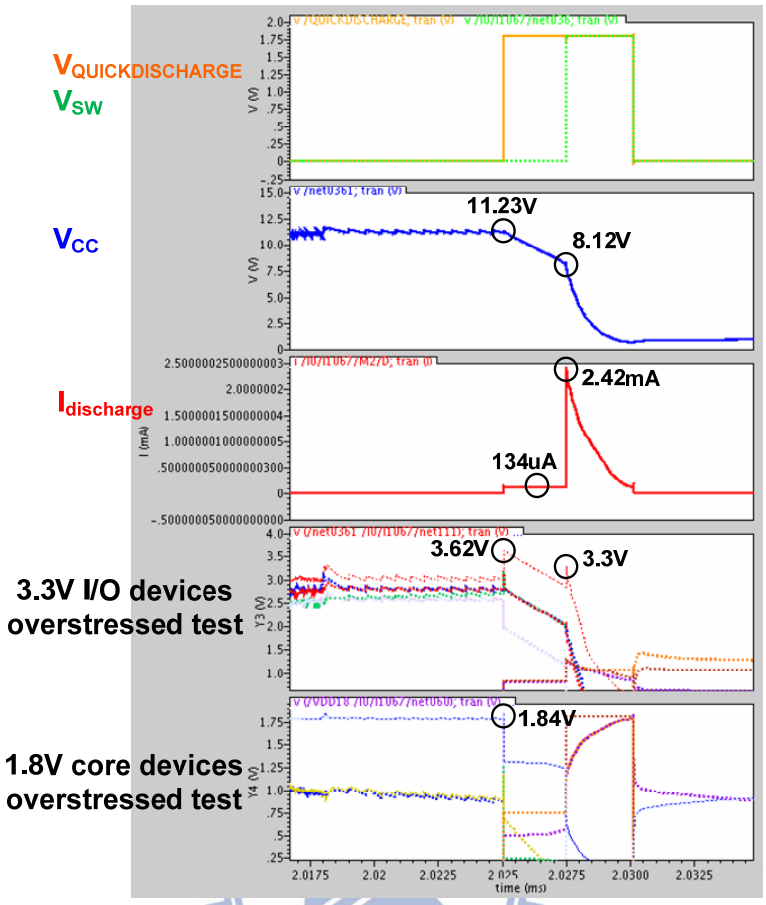


Fig. 4.3.3 The simulation result of quick-discharge circuit.

Fig. 4.3.4 shows the simulation result of stimulator during changing detect-mode to stimulate-mode. When control signal V_{mode_select} is zero, the stimulator operates in detect-mode and V_{detect_out} can successfully deliver the brain signal which is simulated by sine wave which frequency is 1kHz and amplitude is 1mV. When control signal $V_{mode\text{-}select}$ is 1.8V, the stimulator operates in stimulate-mode. In this phase, the charge pump begins to generate 11V and the stimulator delivers biphasic current to tissue. Moreover, Fig. 4.3.5 shows the simulation result of all scale stimulus current which is control by changing 3-bit amplitude signals.

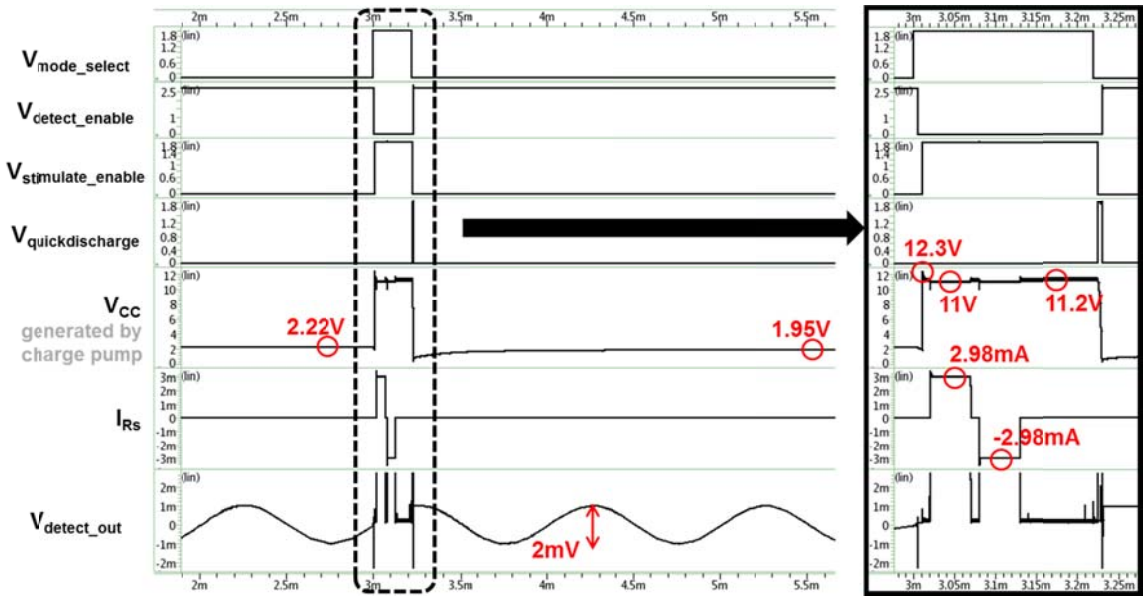


Fig. 4.3.4 The simulation result of stimulator during changing detect-mode to stimulate-mode.

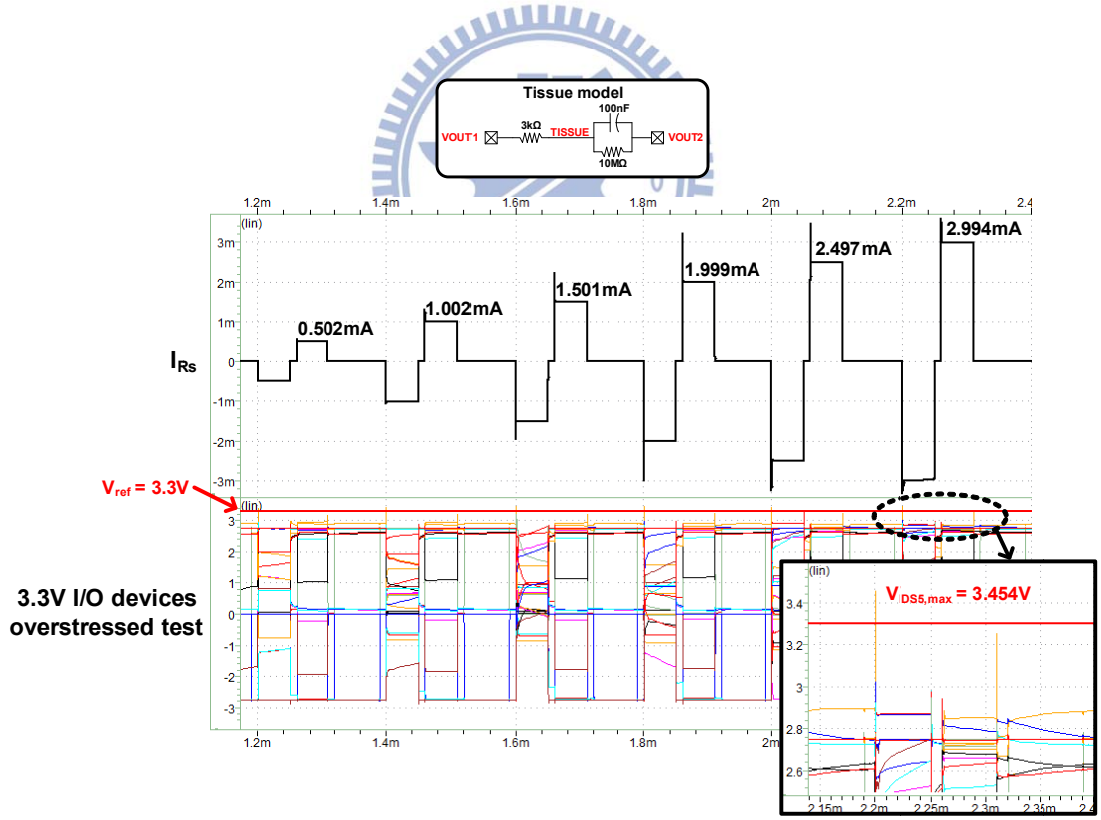


Fig. 4.3.5 The simulation result of all scale stimulus current.

4.4 Summary

The summary of the stimulator is shown in the Table 4.1. The simulation results conform to the specifications. In the simulation results, the cathodic/anodic matching is 0.317% in post-layout simulation. The residual dc current is 23.78nA and the power consumption is 93.75uW (1.8V), 86.08uW (3.3V), and 7.3mW (11V) when the pulse width, period, and amplitude are set to 50μs, 500μs, and 3mA. The standby power (in detect-mode) is 82.9uW (1.8V) and 86.3uW (3.3V).

Table 4.1
Summary of 16-channel biphasic stimulator measurement results

		Spec.	Pre-layout simulation	Post-layout simulation
V_{DDL} / V_{DDH} (V)		1.8V / 3.3V		
Vcc (V)		11V		
Stimulus Current Amplitude (mA)		±0.5, ±1.0, ±1.5, ±2.0, ±2.5, ±3.0,	±0.502, ±1.002, ±1.507, ±2.008, ±2.497, ±2.999,	±0.502, ±1.002, ±1.501, ±1.999, ±2.497, ±2.994,
Cathodic / Anodic Matching		Minimum	0.406%	0.317%
Residual DC Current Error (nA) (@biphasic, cat.=50us, ano.=50us, inter.=10us, dis.=370us period=500us, amp.=3mA)		<100nA	30.45nA	23.78nA
Power Consumption(W) (@stimulate-mode, biphasic, cat.=50us, ano.=50us, inter.=10us, dis.=370us, period=500us, amp.=3mA)	V_{DDL}=1.8V V_{DDH}=3.3V V_{CC}=11V	Minimum	96.17uW 85.38uW 7.4mW	93.75uW 86.08uW 7.3mW
Standby Power (W) (@detect-mode)	V_{DDL}=1.8V V_{DDH}=3.3V	Minimum	85uW 85.3uW	82.9uW 86.3uW
Process		TSMC 0.18μm 1.8V/3.3V CMOS process		

Chapter 5

Conclusions and Future Works

5.1 Conclusions

The advanced treatment for suppressing epileptic seizure by using multi-channel biphasic stimulator is proposed. The advantage of using electrical stimulation has two reasons. First, it is non-reversible surgical treatment, so the patients will not have the injury problems of the important area of cerebral cortex such as the primary motor cortex. Second, the multi-channel technique has more accurate prediction for seizure-onset zone and makes more effective stimulation for suppressing epileptic seizure.

In this work, the design of 16-channel high-voltage-tolerance stimulator had been fabricated in UMC 0.18μm 1.8V/3.3V CMOS process and is investigated and verified. The high-voltage-tolerance stimulus driver through self-adaption bias circuit and stacked transistors can operate with 12V high voltage and successfully deliver biphasic current to tissue. The residual dc current is smaller than 66nA under the safe dc error current 100nA, so this device might not cause injuries to the tissue during the stimulation.

After demonstrating by 16-channel high-voltage-tolerance stimulator, the 16-channel biphasic stimulator with detect-mode and stimulate-mode functions is proposed. Because the acquisition of brain signals and stimulation use the same electrodes in human body, the circuit must be consider the gate-oxide overstress, hot-carrier effect, and other reliability issues during changing detect-mode and stimulate-mode. The simulation results present that the proposed circuit can fit this

condition. The device will be taped out in TSMC 0.18μm 1.8V/3.3V CMOS process and integrated in epileptic SoC. The SoC layout photo is shown in Fig. 5.5.1.

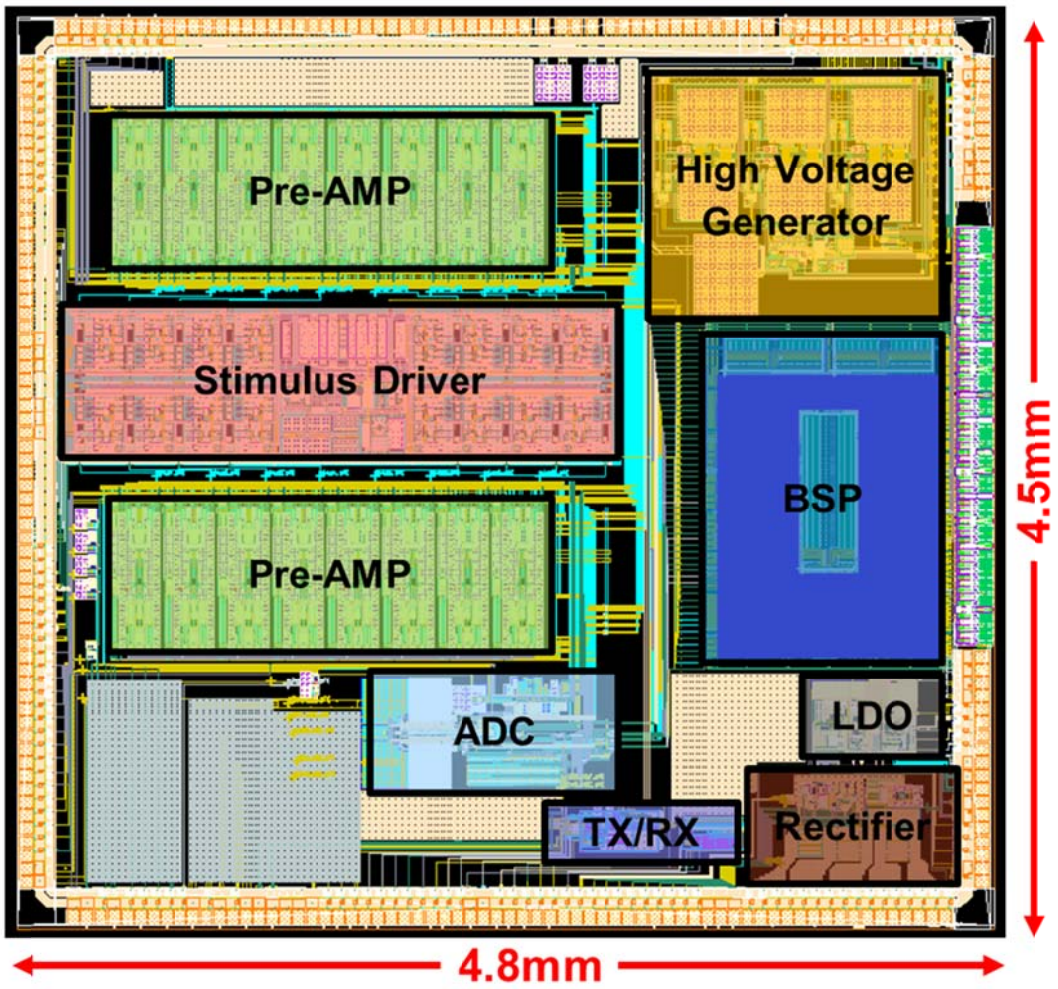


Fig. 5.1.1 The layout photo of the epileptic SoC.

5.2 Future Works

5.2.1 Electrode Monitoring Circuit

The electrode monitoring circuit (EMC) [33] can immediately measure the electrode output voltage during stimulation and it has two advantages. First, the electrode monitoring circuit can be used to control the high voltage generator. When the electrode output voltage is smaller than V_{CC} and it means that the V_{CC} is high enough to generate to stimulus current for the impedance of tissue, high voltage generator can decrease the V_{CC} to reduce the power consumption by using the dynamic high-voltage control signal [34]. Second, by using the impedance analyzer, the tissue impedance can be calculated. Through ascertaining the abnormal of impedance such as (open or short), the enable signal can control stimulus driver to stop the stimulation and prevent the tissue damage.

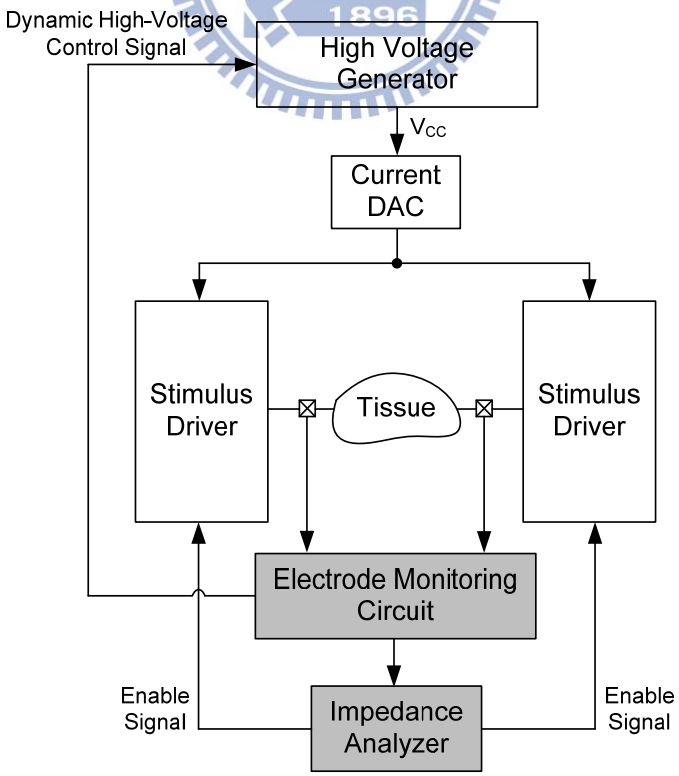


Fig. 5.2.1 Architecture of electrode monitoring system.

5.2.2 DC Blocking Capacitance

Adding the DC blocking capacitance at the output of stimulus driver can ensure the fail-safe condition because the capacitance will block the dc current to prevent tissue damage when the circuit component fails as a short or open circuit. Fig. 5.2.2 shows the architecture of the monopolar biphasic stimulation (a), bipolar biphasic stimulation (b), and monopolar monophasic stimulation (c) by using dc blocking capacitance. Unfortunately, the value of the capacitance is usually micro-scale level and it is impossible to achieve on chip, so the volume of stimulus system is depended on the number of discrete capacitances (Fig. 5.2.3). To achieve full on-chip system, the high-frequency current-switching technique (HFCS) is used to reduce the dc blocking capacitance to pico-scale level. Fig. 5.2.4 shows the proposed stimulus driver based on monopolar monophasic stimulation [35][36].

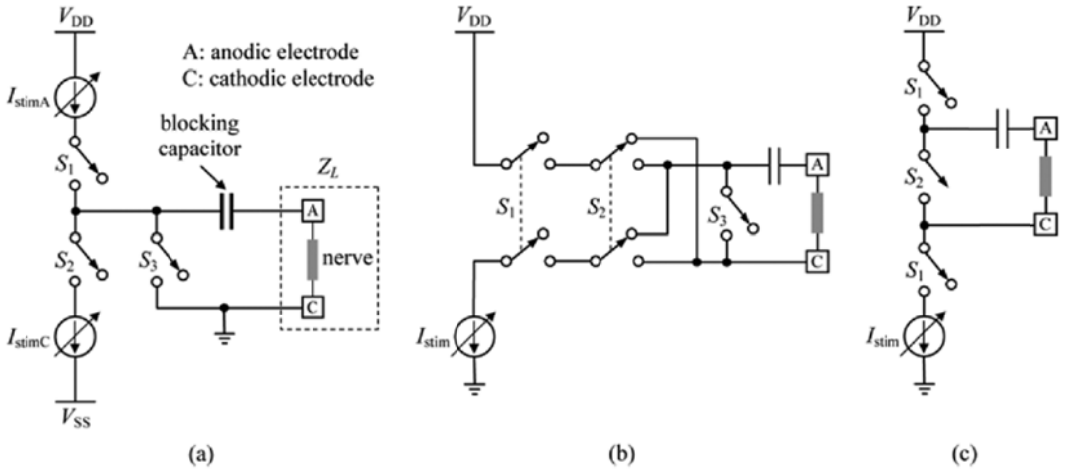


Fig. 5.2.2 Conventional stimulator output stage configurations for two-electrode setup. (a) Dual supplies with active cathodic and active anodic phases. (b) Singe supply with active cathodic and active anodic phases. (c) Single supply with active cathodic phase and passive anodic phase.

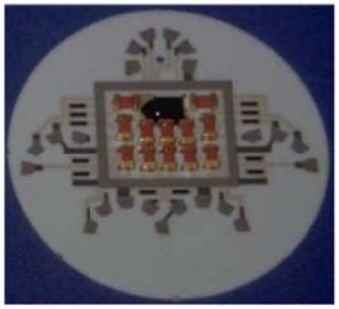


Fig. 5.2.3 The stimulus system. (The discrete off-chip capacitors (orange devices) dictate the implant volume.)

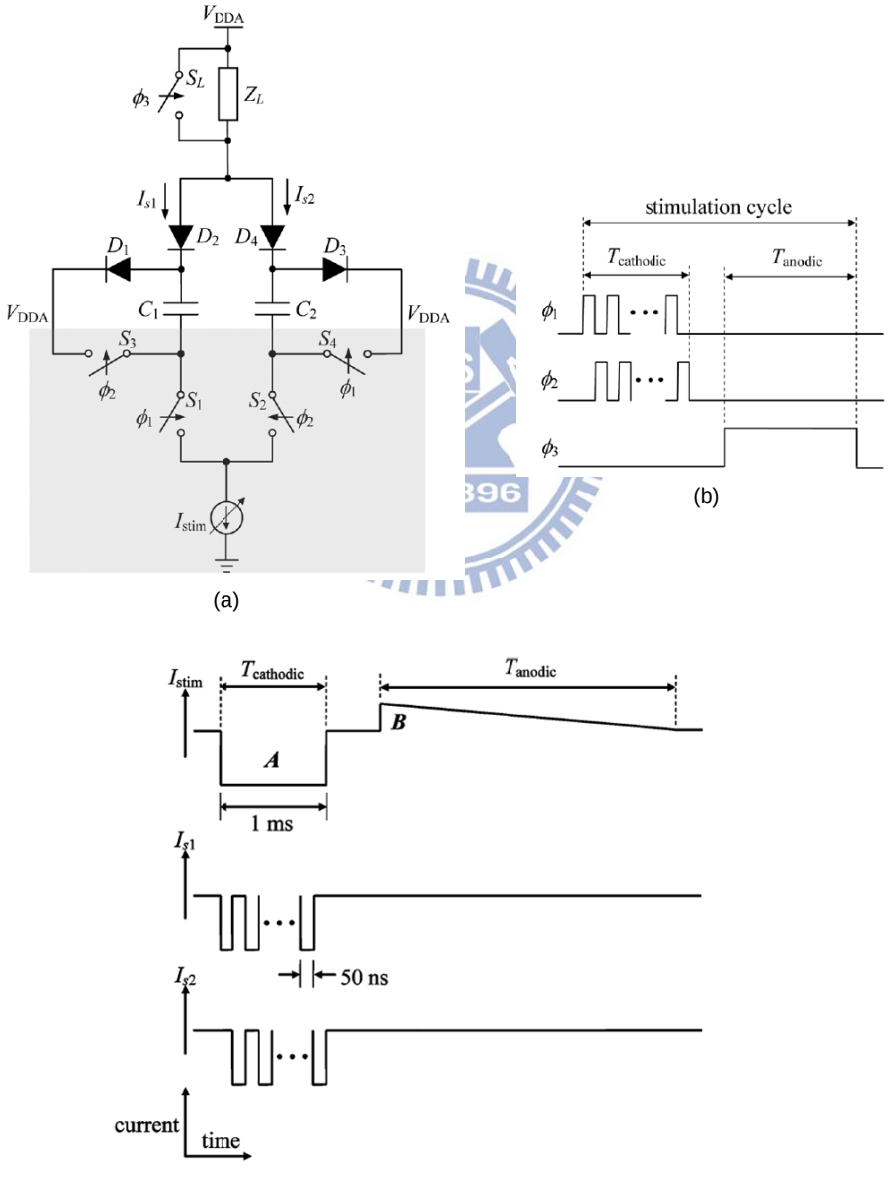


Fig. 5.2.4 (a) HFCS technique stimulus driver. (b) Timing waveforms. (c) The results of stimulation.

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