國立交通大學

電子研究所

碩 士 論 文

應用於900–1800MHz GSM規格的

高功率CMOS T/R開關之靜電放電防護設計

ESD Protection Design of

900–1800MHz High-Power CMOS T/R Switch

for GSM Cellular Applications

研 究 生：洪道一　　(Tao-Yi Hung)

指導教授：柯明道教授　(Prof. Ming-Dou Ker)

中 華 民 國 一〇六 年 九 月

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摘要

近年來，隨著矽製程的演進，射頻積體電路 (radio-frequency integrated circuits, RFICs) 已經可以在一般的 CMOS 製程中實現，如此以來，不但可以降低製造成本，也可以提升與其他射頻電路區塊的整合性。而隨著電晶體尺寸微縮，雖然達到了提升邏輯閘的運算速度以及降低電源功率消耗的目的，但來自靜電放電 (electrostatic discharge, ESD) 的威脅，卻不會因為製程的先進而降低，因此靜電放電防護設計是在積體電路的可靠度中是一個不可忽略的問題。在射頻積體電路中，靜電放電防護設計除了要能夠達到一定的工業規格之外，也不能影響到射頻電路中敏感的射頻效能參數及正常的電路操作。因此，必須以非常嚴格的標準來設計 ESD 防護元件以期將其所帶來的寄生效應對高速射頻訊號的影響降至最低。

本論文分為兩大部分，第一部分為針對應用於手機通訊中的高功率 T/R 開關 (transmit/receive switch, T/R switch) 電路架構所設計的 ESD 靜電放電設計。在高功率 T/R 開關的堆疊 (multi-stacked) 架構中，由於射頻訊號大振幅與高頻率，會使得一般傳統的靜電放電防護設計將正常的射頻訊號誤判為靜電，將正常的射頻訊號排放到地而造成失真。本論文所提出新的靜電放電防護設計並不使用額外的電流疏通路徑，而是利用辨識射頻訊號和 ESD 的行為差異，可以在靜電來臨時開啟自身電晶體的方式來將電流導入到地。此設計已在 0.18 微米 CMOS 製程中實現，相較於未加入靜電放電防護設計的原始電路，能夠達到良好的靜電防護效果。ESD 的耐受度及 T/R 開關射頻電路的參數特性將在論文中完整的討論。

第二部分為應用在典型 T/R 開關中的靜電放電防護元件，利用原本就存在於傳統靜電放電防護電路之中的二極體 (diode) 以及金氧半電晶體 (MOS transistor) 之間的寄生路徑，透過電路佈局技巧組合出一個嵌入式矽控整流器 (embedded silicon-controlled rectifier) 並實現於 90 奈米 CMOS 製程中。此外，藉由電源與地之間的靜電放電箝制電路 (power-rail ESD clamp circuit) 的偵測電路提供觸發訊號將嵌入式矽控整流器在靜電來臨時開啟，成功地降低導通電阻 (Ron) 並提高 T/R switch 對 PS-mode ESD 的耐受度。

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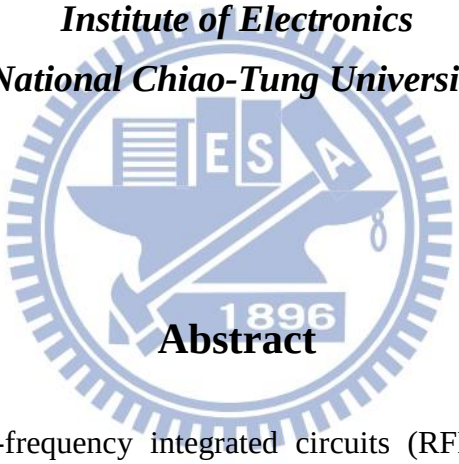

Abstract

In recent years, radio-frequency integrated circuits (RFICs) have been successfully implemented in CMOS process thanks to the fast development of CMOS technologies. In this way, the RFICs can be integrated in a system on chip (SOC) for mass production with lower cost of IC manufacturing. As the transistors scale down rapidly, the oxide thickness becomes thinner and provide faster logic operations with lower energy consumption. However, the threat from electrostatic discharge (ESD) phenomenon was not alleviated as technology advances. In RFICs, the ESD protection circuit must provide enough ESD robustness without disturbing the normal circuit operations. Thus, the ESD protection design must be strictly conducted in order to minimize the parasitic effect of the ESD devices lest it should degrade the performance of the high-speed RF signal.

There are two major parts in this thesis. The first part of the thesis targets on the T/R switch which is applied for cellular device. In a high-power T/R switch, traditional ESD protection method cannot be used since the large amplitude and high frequency of the RF signal will mis-trigger the traditional ESD protection design. As a consequence, in this work, there is no additional discharging path employed to discharge the ESD current. Instead, by identifying the behavior of the ESD transients and the normal RF signal, the transistors in the proposed ESD protection design can trigger the inherent transistors of the T/R switch in the PS-mode zapping event and discharge the ESD current. The proposed ESD protection design for high-power T/R switch has been fabricated in a 0.18-μm CMOS process and achieved good ESD levels. RF performance and ESD characteristics are measured and analyzed in the thesis.

The second part focuses on an ESD protection device for typical T/R switch applications. By using the diodes and MOS transistors which are already designed in the T/R switch with conventional ESD protection, embedded silicon-controlled rectifiers (embedded SCR) are implemented in a 90-nm CMOS process by layout skill. The proposed ESD protection with embedded SCRs and power-rail ESD clamp triggered can enhance the PS-mode ESD robustness of the T/R switch successfully.

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洪 道 一

丁酉年 誌於 新竹交大

Table Captions

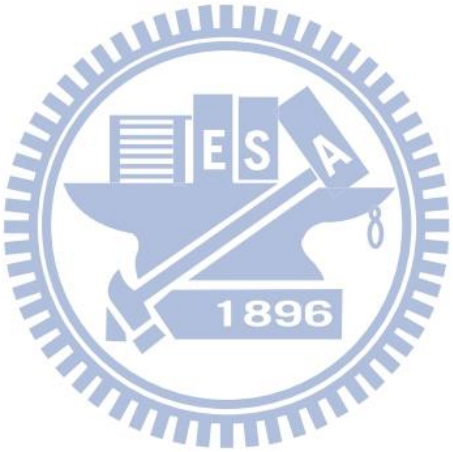


Figure Captions

Chapter 1
Introduction

1.1 Motivation

In recent years, RF transceivers are widely designed in a CMOS system on chip (SoC) for lower manufacturing cost and mass production [1]. The RF transmit/receive front-end circuit plays an important role between antenna and mixer, including low noise amplifier (LNA), power amplifier (PA), and transmit/receive switch (T/R switch), as shown in Fig. 1.1 [2]-[5]. On the other hand, owing to the fast development of CMOS process technologies, MOS transistors have been scaled down rapidly, and therefore provide faster logic performance and lower energy consumption. However, even though the oxide thickness becomes thinner, the threat from ESD phenomenon was not alleviated as technology advances. To solve this issue, ESD protection circuits such as conventional dual diodes and power-rail clamp circuit must be taken into considerations and co-designed in the RF transmit/receive front-end circuit without severe RF performance degradation [6].

In order to provide enough ESD level, the dimensions of the ESD devices are usually selected as large as possible. However, the parasitic capacitance of the ESD device may become larger as well. The additional parasitic capacitance contributed by the ESD device will affect the impedance matching network of the LNA or PA. As for T/R switch, significant degradation of the insertion loss and power handling capability will be observed. This can be seen as a trade-offs between RF performance and ESD robustness. As a consequence, low-capacitance and area-efficient ESD devices co-design with specific circuits are challenges for IC designers.

Moreover, in a RF transceiver SoC chip, T/R switch, LNA, and PA are implemented together in a same chip. Due to the position between antenna and the transceiver circuits, the ANT node of T/R switch is very sensitive to the ESD stress during module assembly. Therefore, ESD protection design on T/R switch can be a more efficient and effective way than former ESD design on either LNA or PA [7], [8]. With proper ESD protection circuit on T/R switch, the ESD current from antenna node can be discharged to VDD or ground before it rush into LNA or PA [9]-[11].

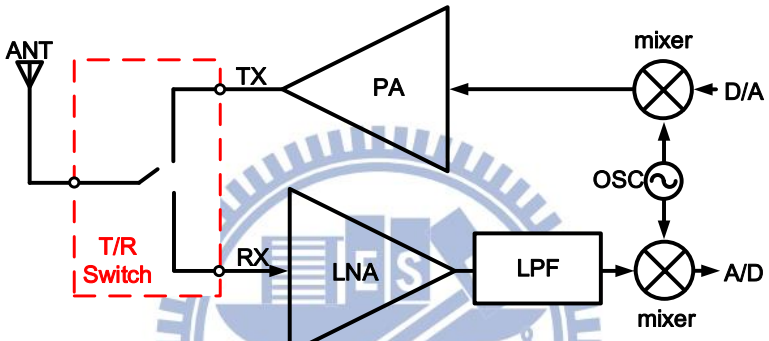


Fig. 1.1. RF transceiver front-end circuit with T/R switch.

In practice, high-power T/R switch architecture is set in GSM/WCDMA cellular phone with time-division duplexing (TDD) system. Fig. 1.2 shows the spectrum of the RF wireless communication applications worldwide. In standard IEEE 802.11 WLAN (wireless local area network) specifications, the maximum power transmitted from TX branch to ANT node is about 30dBm. The power in watts and maximum voltage V_{peak} can be calculated as

$$\text{Pwatt} = 10^{\frac{30\ dBm}{10}} \times 0.001 = 1\ \text{W} \quad (1.1)$$

$$\text{Vpeak} = \sqrt{2 \times Pwatt \times Z_0} = 10\ \text{V} \quad (1.2)$$

where Z_0 equal to 50 ohm, which represents the required matching impedance for the maximum power transfer efficiency.

From (1.2), the voltage amplitude swing on TX branch can reach about $\pm$10V. As a consequence, multi-stack FETs architecture T/R switch [12] is used to achieve high power-

handling capability. Nevertheless, with the large amplitude and fast transient of the transmitting signal on TX branch, the conventional RC detection mechanism may fail to distinguish the RF signal and ESD stress. The conventional power-rail clamp ESD circuit will be mis-triggerred. Moreover, the DC bias of ANT, TX, and RX are usually in the same voltage level. The VDD node and VSS node are not included in the high-power T/R switch. Power-rail ESD clamp circuit cannot be inserted in the high-power T/R switch circuit, either. Therefore, a new ESD protection design customized for high-power T/R switch is in need.

In the first part of the thesis, ESD protection design targeted to high-power T/R switch is presented. The ESD current are detected and discharged without additional ESD path. By identifying the different behavior between RF signals and ESD stress, the high-power T/R switch with proposed ESD protection design discharge the positive-to-VSS ESD on ANT node by the RX branch of the T/R switch itself. Motivations, circuit designs and experimental results are discussed. The proposed ESD protection design successfully enhances the ESD robustness significantly without RF performance degradation in normal circuit operations.

The second part of the thesis focus on the conventional T/R switch with embedded SCRs and power-rail ESD clamp circuit are implemented in 90-nm CMOS process. The embedded SCRs are formed by conventional ESD diode and the shunt MOS transistors of T/R switch together, without additional layout area. With this approach, the experimental results and failure analysis have shown that the proposed design can not only obtain higher failure current (It_2) in transmission line pulse (TLP) system testing and but also introduce lower parasitic capacitance compared with the conventional dual-diode method in the same chip layout area coverage.

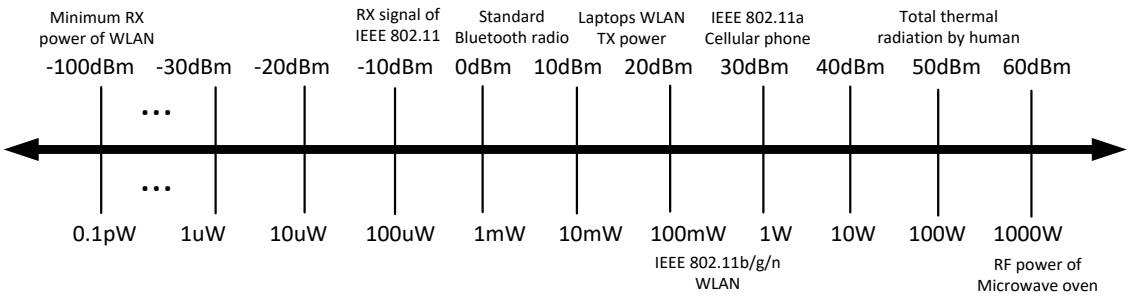


Fig. 1.2. Spectrum of RF wireless application.

1.2 Thesis Organization

Chapter 1 states the motivation of this work and the current issues in RF T/R switch.

Chapter 2 summarizes the background of the research. Brief considerations of T/R switch, including insertion loss, power handling capability, and isolation are introduced. RF circuit simulations, layout skills and measurement are discussed, too. At the end of this chapter, conventional ESD protection circuit for RFICs and the current obstacles are shown.

Chapter 3 exhibits the ESD protection design for high-power T/R switch. A new ESD detection circuit combined with high-power T/R switch is implemented in 0.18-μm CMOS process. Design concepts, ESD zapping simulations before tape-out are performed. After chips were fabricated, TLP and HBM testing are performed to examine whether the proposed design has properly operated as expected. RF performances are measured also to confirm the ESD detection circuit does not affect the normal circuit operations. Failure analysis by SEM is applied to observe the different failure mechanism in PS-mode and NS-mode. Trade-offs between ESD robustness and RF performances are discussed before this chapter ends.

Chapter 4 features conventional T/R switch with embedded silicon-controlled rectifiers for its ESD protection design, where the SCR devices are embedded in the ESD diodes and the transistors of T/R switch by layout skill. Silicon chip verified in a 90-nm CMOS process has been measured by TLP and HBM ESD test to confirm its efficiency for ESD protection. The parasitic capacitance on the ESD devices was also measured. Failure analysis by SEM was performed to find the burned-out site on the T/R switch with the proposed design. From the SEM pictures, the embedded SCRs in the proposed design are actually triggered on to discharge the ESD current.

Chapter 5 concludes the analyses and experiences of the thesis. Optimizations and suggestions on ESD protection for high-power T/R switch are narrated, for the testkeys and notices in future work.

Chapter 2

Basics of T/R Switch and ESD Protection

2.1 General Considerations of T/R Switch Design

2.1.1 S-parameters

In giga-hertz frequency network, the wavelength of the traveling signal can be much shorter than the circuit metal path. That is, the amplitude and phase of the waveform which is displayed on the oscilloscope is not the exact real-time waveform. The distortion effect makes the traditional analog measurement method cannot be applied for RF circuit. Thus, the concept of incident power waves, reflected power waves and impedance matching are a more suitable way to describe the electrical behavior in high-frequency networks. In microwave engineering, scattering parameters (S-parameters) are used to describe the electrical behavior of the two-port network or n-port network [13], [14].

A two-port network is drawn in Fig. 2.1. In the network, S-parameters are defined by signal power of incident waves and reflected waves. The S-parameters matrix:

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \tag{2.1}$$

which can also be noted as

$$\begin{cases} V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \\ V_2^- = S_{21}V_1^+ + S_{22}V_2^+ \end{cases} \tag{2.2}$$

where V_1^+ and V_2^+ represent the incident waves of each port; V_1^- and V_2^- represent the reflected waves of each port, respectively.

Each term of the scattering matrix can be defined as

$$S_{11} = \left.\frac{V_1^-}{V_1^+}\right|_{V_2^+=0} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{2.3}$$

$$S_{12} = \left.\frac{V_1^-}{V_2^+}\right|_{V_1^+=0} \tag{2.4}$$

$$S_{21} = \left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0} \tag{2.5}$$

$$S_{22} = \left.\frac{V_2^-}{V_2^+}\right|_{V_1^+=0} = \frac{Z_{out} - Z_0}{Z_{out} + Z_0} \tag{2.6}$$

S_{11} is the power ratio of the reflected and the incident waves at input port, and it is also known as the input return loss or reflection coefficient, Γ. S_{12} is the power ratio of the reflected wave at output port to incident wave at input port, it is called the reversed gain of the network. S_{21} represents the power ratio of reflected wave at output port to incident wave at input port, it is known as the forward gain of the network. S_{22} is the power ratio of the reflected wave and the incident wave at output port, which is called the output return loss.

In RF measurement, S_{11} and S_{22} represent the accuracy of the input matching and output matching. The typical value of the S_{11} and S_{22} is below -10dB. S_{21} represents the gain or insertion loss of the circuit. For a low noise amplifier circuit, the typical value of S_{21} is about 10 dB. At last, S_{12} represents the reverse isolation of the circuit.

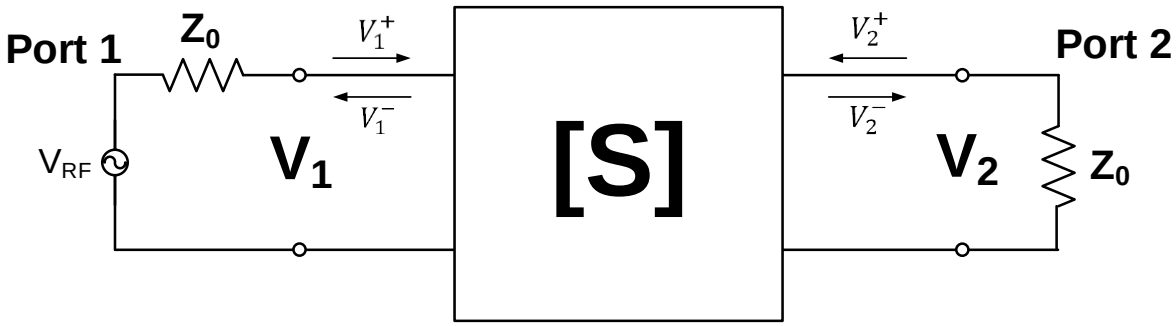


Fig. 2.1. A two-port network describe with S-parameters.

2.1.2 Insertion Loss

The schematics of a conventional single-pole-double-throw (SPDT) T/R switch, as shown in Fig. 2.2, is the most commonly used topology worldwide [15]. By applying the control signal of logic 1 to V_{TX} (0 to V_{RX}), the T/R switch can be operated in the transmit mode (TX mode). On the contrary, with the control signal of logic 0 to V_{TX} (1 to V_{RX}), it is operated in the receive mode (RX mode).

Insertion loss (IL) is one of the most important specifications in T/R switch, which is mainly determined by the turn-on resistance (Ron) of the MOS transistors M1 and M2. Thus, the dimensions ratio, W/L, has to be large enough to make Ron as small as possible. However, with the increase in ratio of the transistors, the parasitic capacitances become larger as well.

Fig. 2.3 shows the cross-section view of the NMOS transistors in T/R switch. The resistive body-floating technique [16] and deep N-well doping in CMOS triple-well process [17] have been proved to enhance the RF performance of T/R switch including insertion loss and power handling capability. The schematic of a single NMOS transistor is illustrated in Fig. 2.4. The insertion loss of a single NMOS transistor is analyzed using S-parameters below.

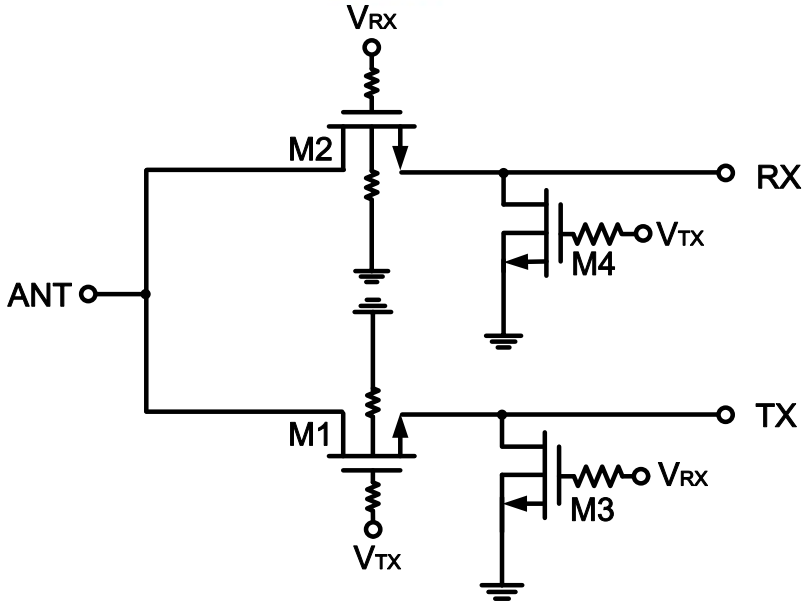


Fig. 2.2. Conventional T/R switch without ESD protection.

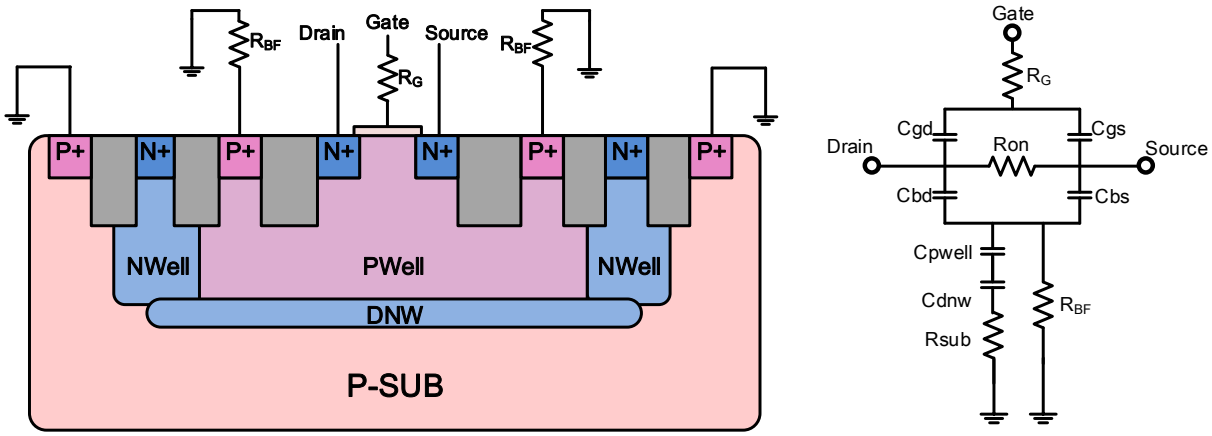


Fig. 2.3. Cross-section view and equivalent circuit of the NMOS in T/R switch.

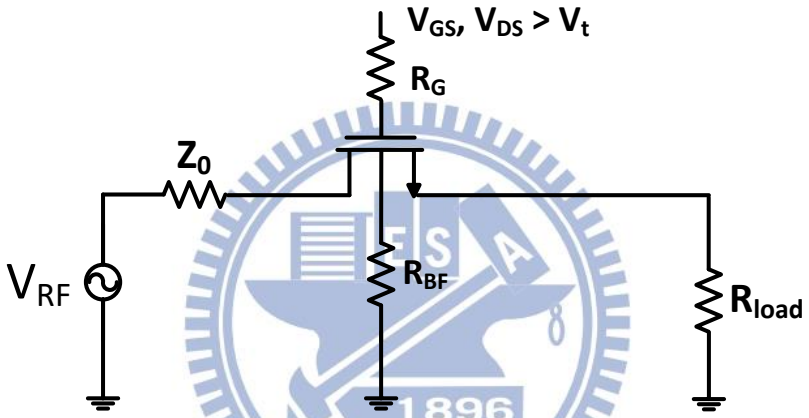


Fig. 2.4. Schematic of a single NMOS transistor.

The insertion loss can be expressed as

$$\mathrm{IL} = \frac{1}{|S_{21}|^2} \tag{2.7}$$

where the magnitude of S_{21} is the power ratio of the power delivered by the load and the power available from the source:

$$|S_{21}|^2 = \frac{P_{load}}{P_{available}} \tag{2.8}$$

the insertion loss can be derived as

$$\mathrm{IL} = \frac{P_{available}}{P_{load}} = \frac{P_{load} + P_{Ron} + P_{loss,sub}}{P_{load}} \tag{2.9}$$

By (2.9), the power dissipated on R_{on} and R_{sub} increase the insertion loss of the T/R switch.

In higher frequencies, the parasitic effect of the capacitance must be taken into consideration. The capacitance C_{bd}, C_{PWELL} and C_{DNW} in Fig. 2.3 will be a low impedance path to ground. Therefore, a large p-substrate resistance, R_{sub}, and R_{BF} (10kohm) for resistive body-floating technique are implemented to reduce the signal loss. It can be seem as AC open to avoid the current leakage of high-frequency RF signal to ground. By these methods, the IL of the T/R switch can be minimized in a standard triple well CMOS process.

2.1.3 Power Handling Capability

For large signal behaviors, S parameters are not sufficient enough to describe the electrical characteristics. Linearity of a RF system is introduced to depict the relationship between output power and input power. As the power of the input signal increases, intermodulation distortion and harmonics make the power of the output signal saturate gradually. The characteristics line between output power and input power will no longer be linear. Besides, the large voltage swing stressed on the gate dielectric oxide and the unwanted turn-on of the source/drain-body diodes will also degrade the linearity of the circuit. The performance of linearity is limited by the specific process that will cause reliability issues of the RF system.

The power gain of the T/R switch is also known as the insertion loss in TX mode. As the power signal from PA becomes larger, the power gain of the T/R switch will be compressed eventually. The linearity is usually measured by the 1-dB power gain compression point (P_{1dB}) of the circuit. At the P_{1dB} compression point, the power gain is 1dB lower than the constant power gain. Fig. 2.5 sketches the plot of power gain versus input power (in dBm). IP_{1dB} represents the input power (in dBm) when power gain (in dB) degrades 1dB. Similarly, in Fig. 2.6, the plot of output power versus input power is illustrated, the linear relationship between output power and input power can be more intuitively observed. OP_{1dB} and IP_{1dB} represents output power (in dBm) and input power (in dBm) respectively.

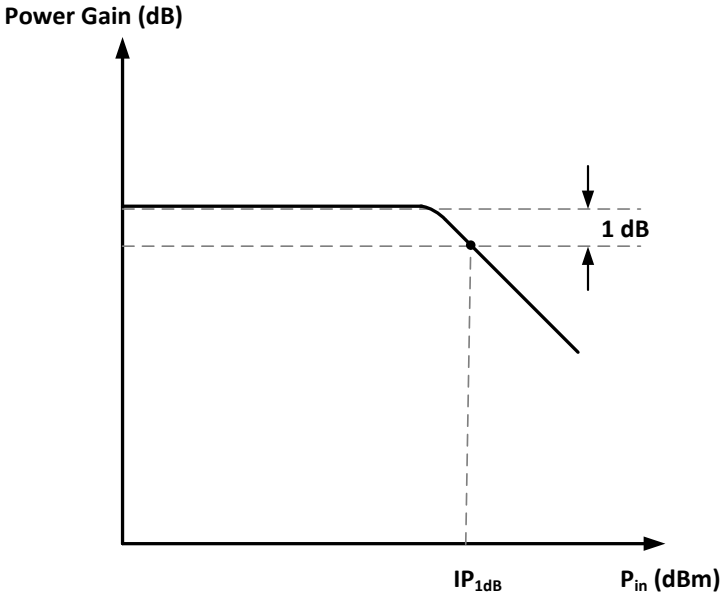


Fig. 2.5. The plot of power gain versus input power.

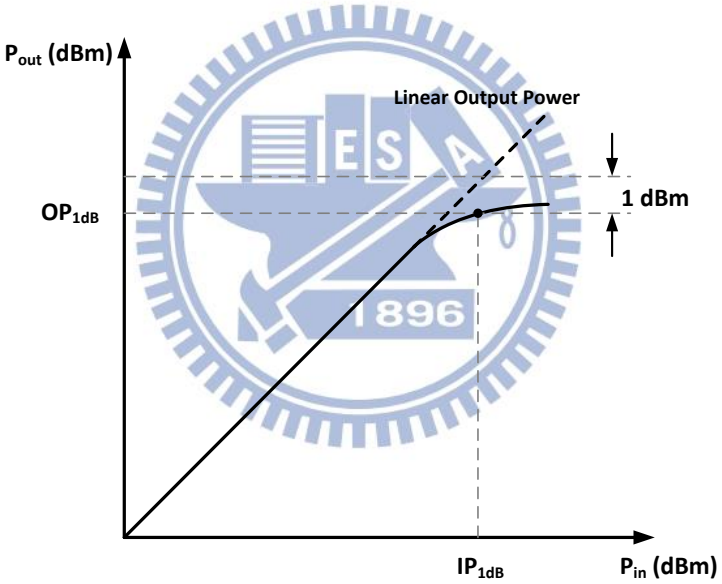


Fig. 2.6. The plot of output power versus input power.

In a SPDT series-shunt T/R switch, both on-state transistors and off-state transistors affect the power handling capability of the switch. For Fig. 2.7, take T/R switch operates in transmit mode as an example. The negative voltage peaks of RF signals are clamped by the parasitic drain/source-body junction diodes of on-state transistors M1. To solve the issue, resistive body-floating technique and large bulk resistance R_{sub} are employed to reduce the voltage drop on the junction diodes. The AC voltage swing can be divided through C_{bs} (C_{bd}), C_{Pwell_DNW}, C_{DNW_Psub}, and R_{sub} [18].

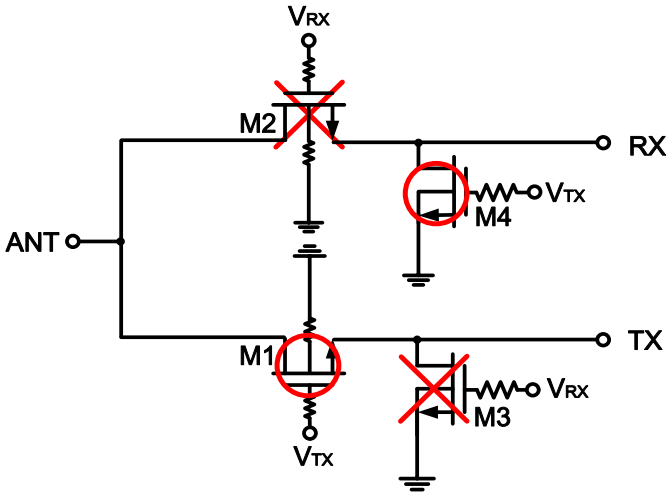


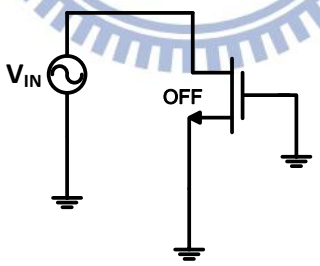
Fig. 2.7. T/R switch operates in transmit mode.

For the off-state transistors M2 and M3, large gate resistor (10kohm) is employed to prevent the V_{GS} and V_{GD} from exceeding the threshold voltage and the oxide breakdown voltage. By applying the large gate resistor, the gate terminal can be seen as AC-floating. The AC voltage swing thus can be divided into the C_{GS} and C_{GD}.

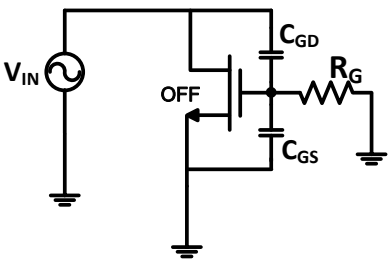
The maximum V_{IN} of off-state transistors without gate resistance can be derived as

$$|V_{IN} - V_G| = |V_{IN}| < V_t \tag{2.10}$$

$$|V_{IN}|_{max} \cong V_t \tag{2.11}$$



(a)



(b)

Fig. 2.8. Off-state transistors (a) without gate resistor and (b) with gate resistor.

On the other hand, with the help of large gate resistance, the maximum V_{IN} of the off-state transistors with gate resistor can be estimated as

$$|V_{IN} - V_G| = \frac{|V_{IN}|}{2} < V_t \tag{2.12}$$

$$|V_{IN}|_{max} \cong 2V_t \tag{2.13}$$

The large gate resistor can not only avoid unwanted channel formation of the off-state transistors but also prevent the oxide overstress for reliable operations.

Apart from the AC-floating technique that can enhance the linearity of T/R switch, stacked transistors are further used to strengthen the power handling capability. As illustrated in Fig. 2.9, the off-transistors arms that is in shunt to the signal path are constructed by stacked NMOS transistors. With the help of the large resistor at the gate terminal, the large RF transient can be blocked from the DC power supply and divided into the C_{GS} and C_{GD} of each transistors. However, the stacked transistors architecture enhance the linearity of the T/R switch by sacrifice the insertion loss of the RX. The specific T/R switch which is targeted to high-power applications are commonly employed for GSM or WCDMA communication systems which operates in 0.9GHz and 1.8GHz. The schematic of high-power T/R switch without ESD protection circuit is sketched in Fig. 2.10. It includes ANT, TX, RX, GND port and two voltage signal, V_{TX} and $V_{RX,}$ which control the circuit operations.

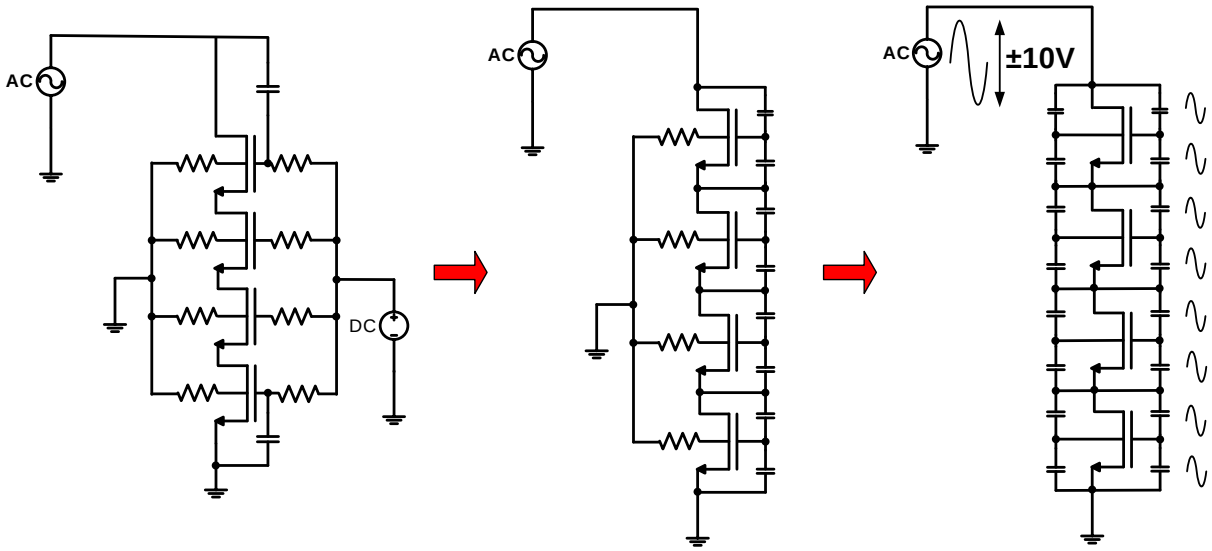


Fig. 2.9. Stacked transistors for AC voltage dividing.

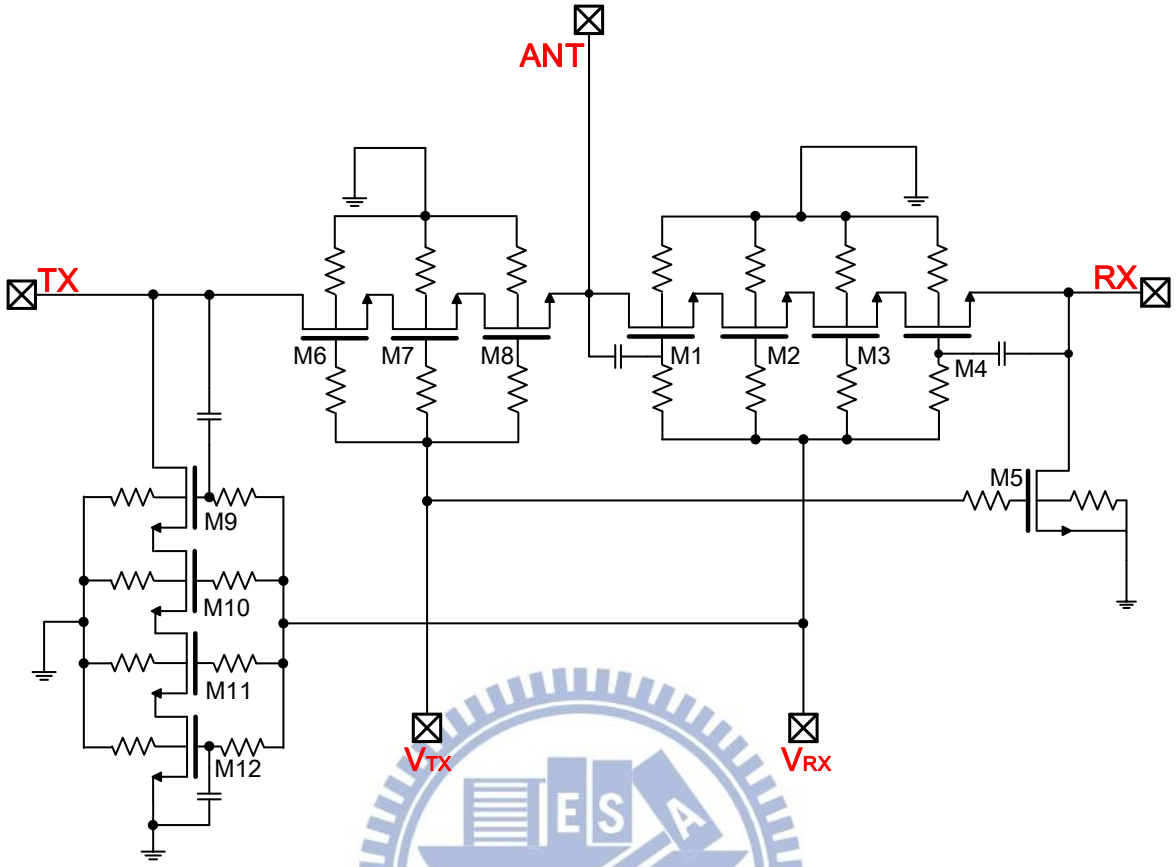


Fig. 2.10. High-power T/R switch without ESD protection circuit.

2.1.4 Isolation

The isolation of the switch depicts the signal power leaks to the uninterested port. For example, while T/R switch operates in transmit mode, the signal leaks to the RX port instead of ANT port. A T/R switch using series-shunt topology is applied to resolve the leakage issue. The shunt arm of the T/R switch serves as a low impedance path for undesired signal discharge to the ground. In addition, the dimension of the shunt transistors can be used to adjust the impedance matching for input return loss. Typically, the isolation of the T/R switch is larger than 30dB in both TX and RX operation modes.

2.2 RF Simulations and Layout Considerations

2.2.1 Pre-Simulation and Post-Simulation

In integrated circuit design industry, function verification by EDA (electronic design automation) simulation tools with specific process models are necessary to ensure that the circuit meets the required specifications before tape-out.

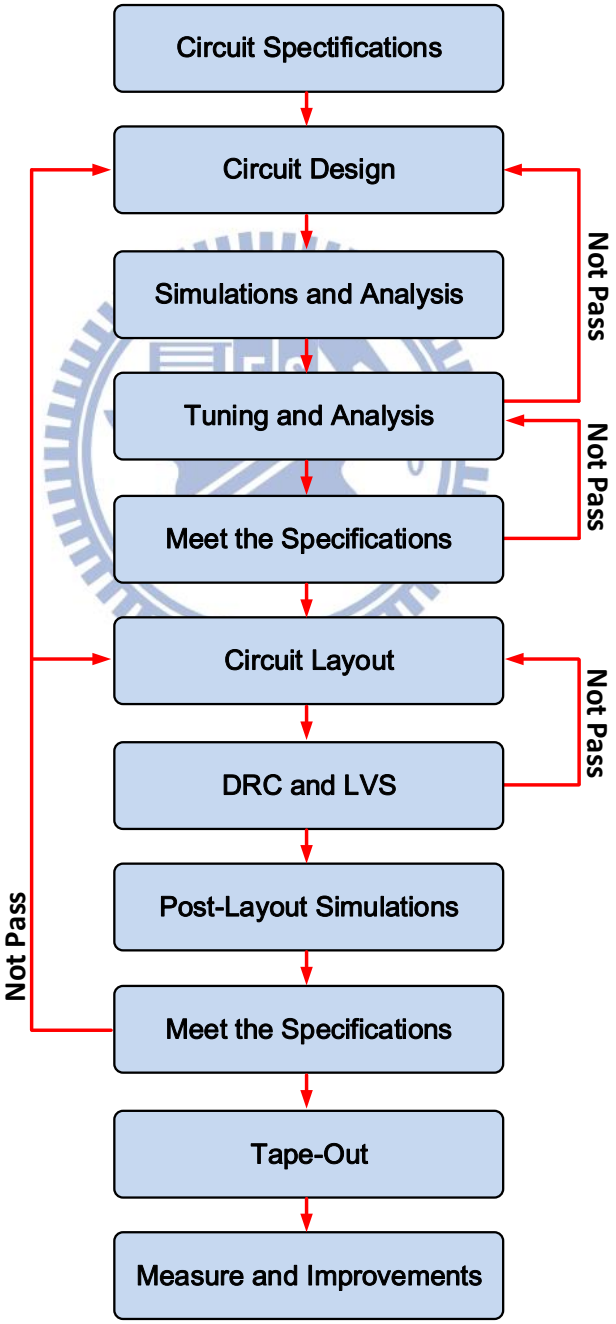


Fig. 2.11. Flow chart of analog IC design.

IC design flow chart is illustrated in Fig. 2.11. Circuit simulations simulated by Cadence Spectre are at the upstream of the design flow. As a consequence, if the designer does not simulate the project appropriately, the performance of the fabricated circuit will be unpredictable. For the simulation before doing circuit layout is called pre-layout simulation. Pre-layout simulations depict the preliminary circuit performance without the non-ideal parasitic effects of the metal connections. After the circuit layout is generated, post-layout simulations are performed to extract the parasitic RC which is introduced by the metal connections and the devices. Since the post-layout simulation is a more practical description of the circuit, layout must be modified as long as the performance does not meet the specifications.

Unlike the traditional analog circuit simulations, the inductive effect on the metal cannot be neglected for high-speed RFICs. Thus, the simulation procedures for RFICs are more complicated and lengthy than the traditional analog circuits. In recent years, the IC industry has dedicated to enhancing the accuracy of the simulations for RFICs. For foundry end, parameterized devices (P-Cell) such as RFNMOS and RFPMOS including simulation models and layout are given to designers to minimize the gap between the pre-layout and post-layout simulations. For designers, additional EDA simulation tools such as HFSS are programmed, with the help of the electromagnetic simulations (EM) performed by HFSS, complete parasitic R-L-C effects can be extracted from the 3D layout structure.

In this thesis, the post-layout simulation of a RF circuits is done by EM simulation of HFSS (high frequency structure simulator), the 3D software can simulate the S-parameters of every terminal of the metal connections. The EM simulation flow is sketched in Fig. 2.12. First, the model parameters of the specific process is defined. Next, a simplified layout (merges of layers or vias) is exported from Cadence Virtuoso. The reason that the layout has to be simplified is because of the convergence problem during the iterations, the most time-consuming step of the simulations. At last, the RF circuits are simulated in Spectre again with the extracted S-parameters of the metal connections from HFSS.

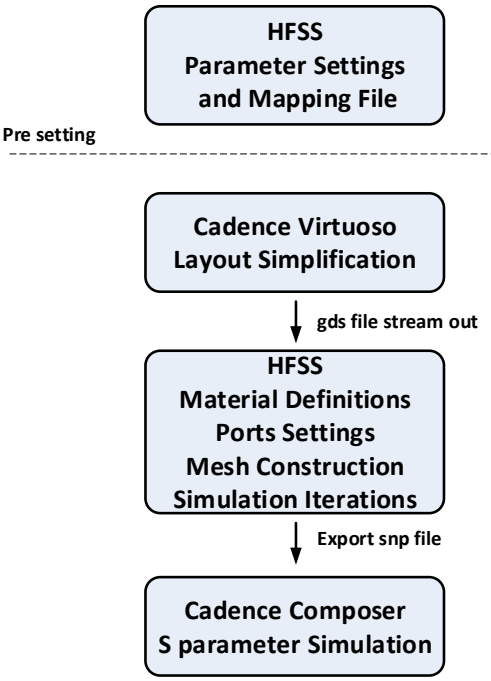
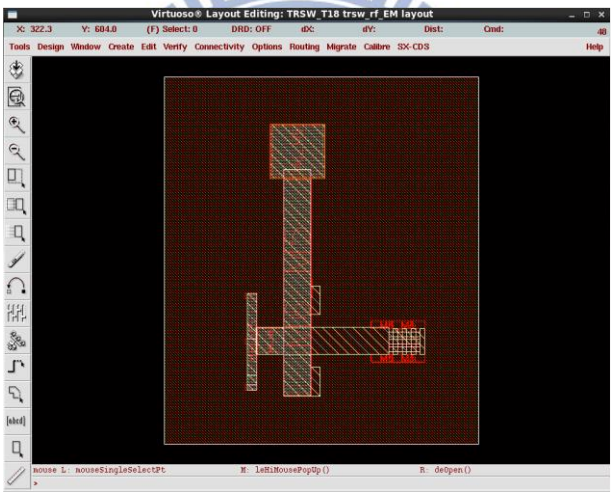
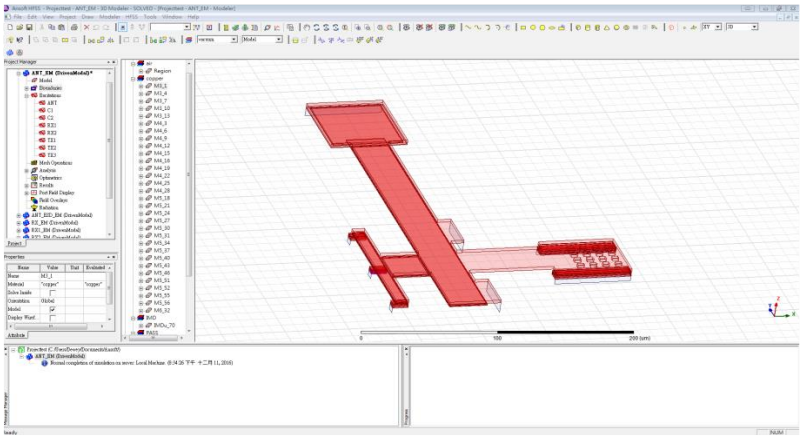


Fig. 2.12. Design flow of electromagnetic simulation.



(a)



(b)

Fig. 2.13. Layout view in (a) Cadence Virtuoso (b) HFSS.

For realistic practice, Fig. 2.13(a) and Fig. 2.13(b) show the same layout in Cadence Virtuoso and HFSS, respectively. Different from the 2D flat layout in Cadence Virtuoso, HFSS constructs a concrete 3D model to simulate the electrical behavior of the metal line.

2.2.2 Layout Considerations and RF Measurement

Considering of the parasitic effects, the layout of either analog or digital integrated circuits affects the function performance significantly. In RF circuit's layout, some basic skills are noted in the following paragraph.

The most important of all is the efficiency of the signal delivering. The top metal (M6 in 180-nm process) is the thickest deposition layer. As a consequence, the sheet resistance of the top metal line is the smallest. With the lower Ron, top metal M6 is preferred to be the path for RF signal passing. In addition, since the distance (altitude) between top metal M6 and the silicon ground surface is the farthest compare to metal M1 to M5, the parasitic capacitance between signal path and ground will be the smallest, too. On the other hand, grounded metal layers overlapping with signal path is prohibited. By the way, if there are two signal paths, they should not cross over from each other for electromagnetic interference (EMI) conditions.

To ensure the devices in a RF system operate correctly, a stable DC power has to be provided. The de-coupling capacitance must be set around in the layout area as well. For RF active circuits such as LNA or PA, the circuits will oscillate and appear unwanted tones if de-coupling capacitance were not inserted properly in the layout. The de-coupling capacitance serves as a reservoir of energy to stable the DC bias. It can also be seen as a low impedance path for AC signal not to affect the DC bias.

At last, the dummy pattern (Fig. 2.14 and Fig. 2.15) of RF layout is not just to pass the density rule check (DRC) of the process. All the dummy patterns have to be connected together and neatly grounded. In this way, unwanted interference or harmonics can be suppressed.

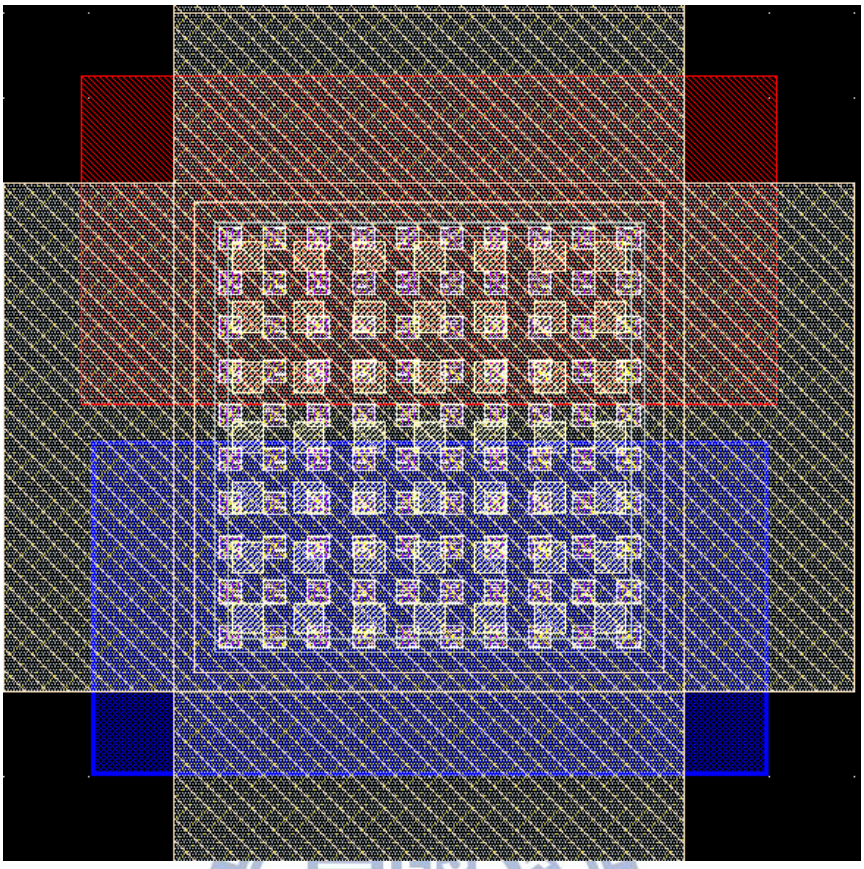


Fig. 2.14. Layout example of dummy cell for 0.18-μm process (6 metal layers).

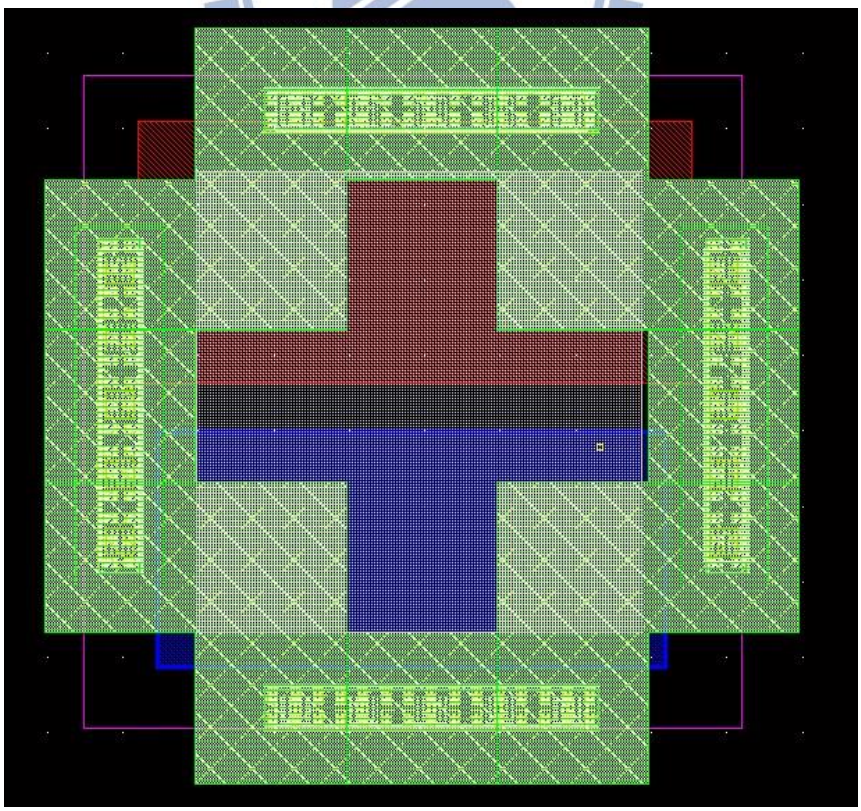


Fig. 2.15. Layout example of dummy cell for 90-nm process (9 metal layers).

When it comes to the on-wafer measuring of the RFICs, the layouts of the PADs for RF single-ended (GSG) have to be drawn customized. As mentioned before, top metal M6 is employed for signal path. The RF PADs for signal are constructed only by M5 and M6 with via connected, in order to minimize the parasitic capacitance of the PADs. It is different from the I/O library provided by the foundry, which is fulfilled with all the metal layers (M1 to M6) and ESD protection devices.

The dimension of a single RF PAD is drawn in 60um*60um, slightly larger than the minimum allowance 50um*50um of CIC (Chip Implement Center, Hsinchu) 20-GHz on-wafer measurement rule. The PAD pitch distance between two RF PADs is 100um (PAD's center to PAD's center). Layout rules of PADs in illustrated in Fig. 2.16. If the PAD patterns on the layout does not meet the rules, the on-wafer measurement will not be allowed in CIC. Furthermore, the pin's orders of the DC PADs are not the same as the RF PADs. The order of the DC PADs goes on P-G-P (pad-ground-pad), rather than the order of the RF PADs is G-S-G (ground-signal-ground). The stated rules must be strictly followed or the RF probes provided by CIC cannot be used.

The designers can also do the RF measurement on printed circuit board (PCB), as long as the parasitic inductance of the bonding wire is taken into design considerations in advanced.

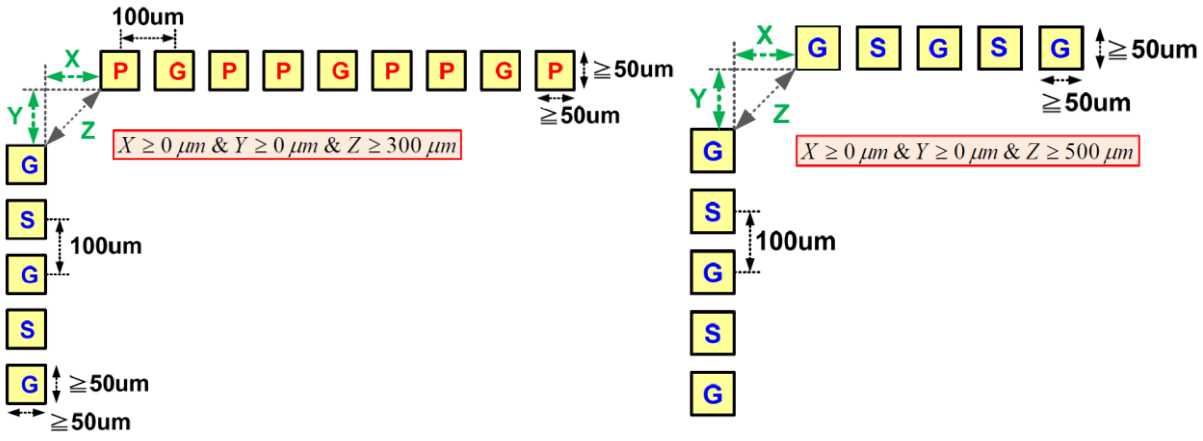


Fig. 2.16. Layout rules for (a) RF pads and DC pads and (b) RF pads and RF pads of 20-GHz on-wafer measurement in CIC (2016.10).

2.3 Conventional ESD Protection Design

2.3.1 Architecture of Conventional Whole-Chip ESD Protection Design

The architecture of whole-chip ESD protection design is illustrated in Fig. 2.17. In order to prevent the ESD current rushes into the sensitive inner circuits, the on-chip ESD protection design is employed. In Fig. 2.17, ESD protection devices are inserted between I/O PAD and VDD (VSS). The chosen ESD protection devices can deal with the ESD stress that directly zaps on the I/O pins. Besides the ESD protection devices at the I/O forefront, power-rail ESD clamp circuit is set between the power lines also. The power-rail ESD clamp circuit is used to suppress the fluctuations on the power line. With the ESD protection devices and the power-rail ESD clamp circuit, the conventional protection architecture can construct a complete ESD protection design for integrated circuits in all aspects.

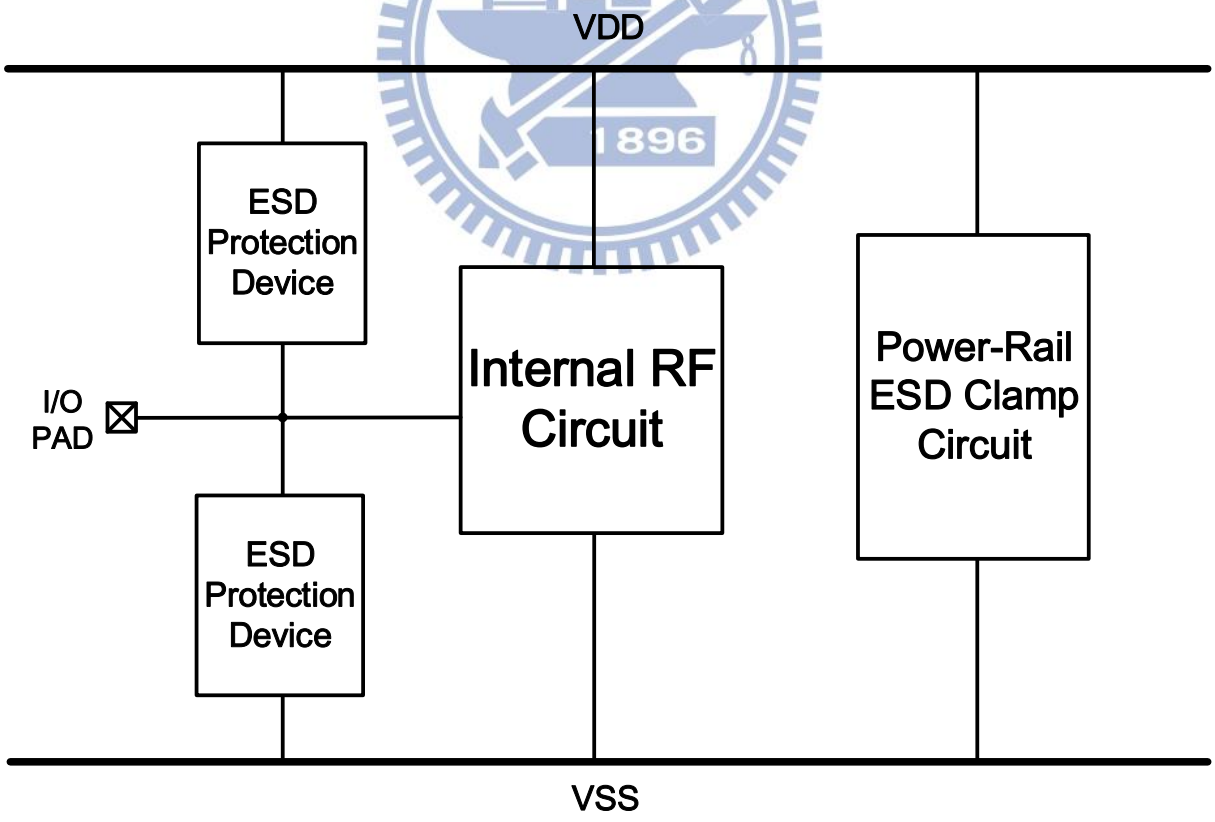


Fig. 2.17. Architecture of whole-chip ESD protection.

2.3.2 Power-Rail ESD Clamp Circuit and I/O ESD Clamp Circuit

In IC industry, a qualified integrated circuit product before mass manufacture has to go through a series of tests, including the ESD tests for reliable operations. There are several testing standards of ESD: Human body model (HBM), machine model (MM), charge device model (CDM), field induced model (FIM), etc. Among the mentioned models, the HBM ESD test which simulates the ESD strikes from the human living around, is commonly used for the fragile integrated circuits. Fig. 2.18 shows the equivalent circuit of HBM ESD test. In phase 1, the charge is stored in the capacitance. Then the charge will be injected into the device under test (DUT) in phase 2.

Besides the ESD testing standards, there are four testing modes that need to be stressed on the interested pins. The four testing modes for HBM test are positive-to-VDD (PD), positive-to-VSS (PS), negative-to-VDD (ND), and negative-to-VSS (NS). The ESD protection design has to meet the all specifications in every testing modes. Typically, the goal of ESD robustness on HBM testing has to pass 2-kV. The ESD design using the conventional architecture which is mentioned in the previous section with appropriate ESD protection devices can easily meet the product's requirements.

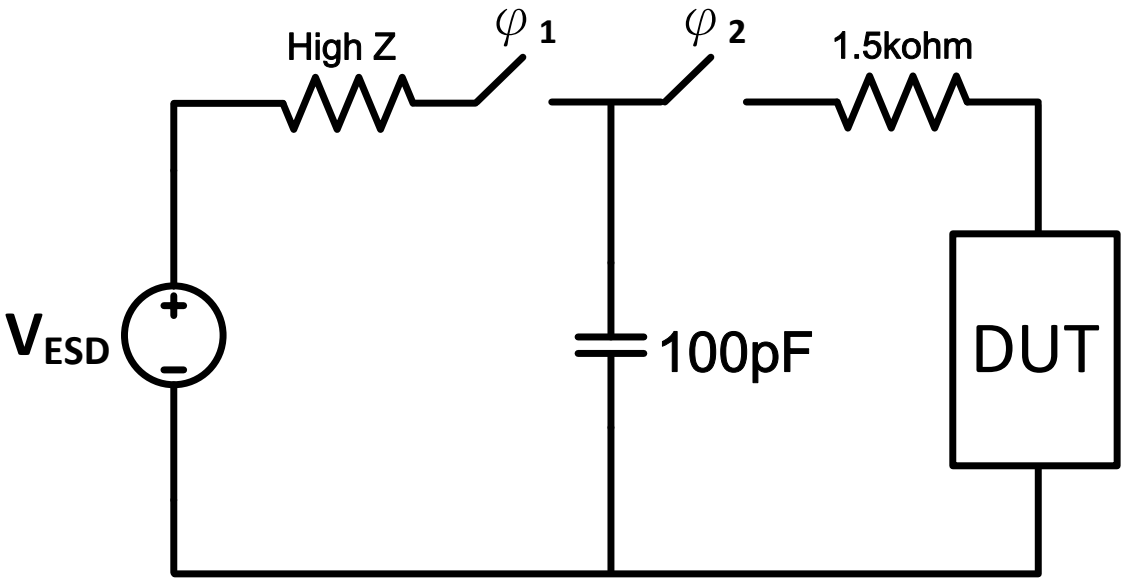


Fig. 2.18. Equivalent circuit of human body model ESD test.

Fig. 2.19 sketches the schematic of conventional whole-chip ESD protection design for T/R switch. The two ESD diodes D1 and D2 serve as the I/O ESD clamp circuits. The diode D1 and D2 will be forward-biased during the PD and NS-mode ESD event, while reversed-biased in normal circuit operations. The diodes are good ESD protection devices that do not occupy large silicon layout area. In addition, the power-rail ESD clamp circuit are set between the power line and the ground which is composed of an ESD transient detection circuit and a large transistors M_{ESD} to discharge the current. Resistor R1, capacitor C1, transistor Mp1, and Mn1 form an ESD detection circuit to control the operation of the M_{ESD}. In normal circuit operations, the input of the invertor will be charged to VDD, the voltage at the gate of M_{ESD} will be zero. The RC time constant is set to 100-ns, for the duration of an ESD stress. The RC delays can ensure the PMOS Mp1 keeps in on-state during the event to charge the gate of the M_{ESD}. For PS-mode zapping, the ESD discharging current will go through the ESD diode D1 and be delivered to the power-rail clamp circuit (red arrow in Fig. 2.19). And for ND mode ESD, the negative stress are passed to the VSS node and coupled through C1 to the gate of Mp1. Mp1 turns on and charges the gate of M_{ESD} to discharge the current (brown arrow in Fig. 2.19).

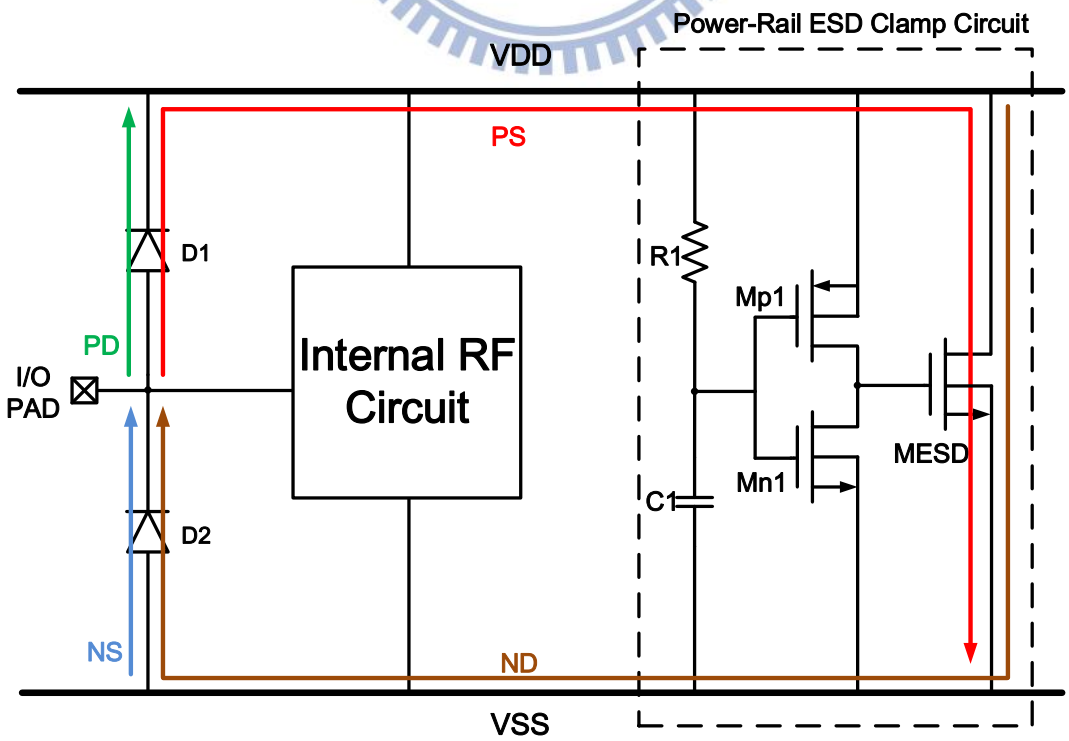


Fig. 2.19. Conventional whole-chip ESD protection circuit.

2.4 ESD Protection Design for RFICs

2.4.1 Conventional RF ESD Protection Design Methods

For integrated circuits that operates in lower frequencies, the parasitic capacitance caused by ESD protection device affects the circuits' performance slightly. The dimension of the ESD devices can be chosen flexibly to meet the specific specifications. However, unlike the traditional analog circuits, parasitic capacitance occupies in a more important position and is always a great consideration for RF circuit systems. The unwanted parasitic capacitance not only degrade the signal transfer efficiency but also the change the impedance matching of the system. As a result, the categories and dimensions of ESD protection devices which are employed for RF circuit systems have to be strictly determined and co-designed with the system. Fig. 2.20 sketches the general issue of ESD protection design for RF circuits. The parasitic capacitance C_{ESD} introduced by the ESD protection device serves as a low impedance path for RF signal to ground. As a consequence, the trade-offs between the RF performance and the ESD robustness are significant challenges for circuit designers [19].

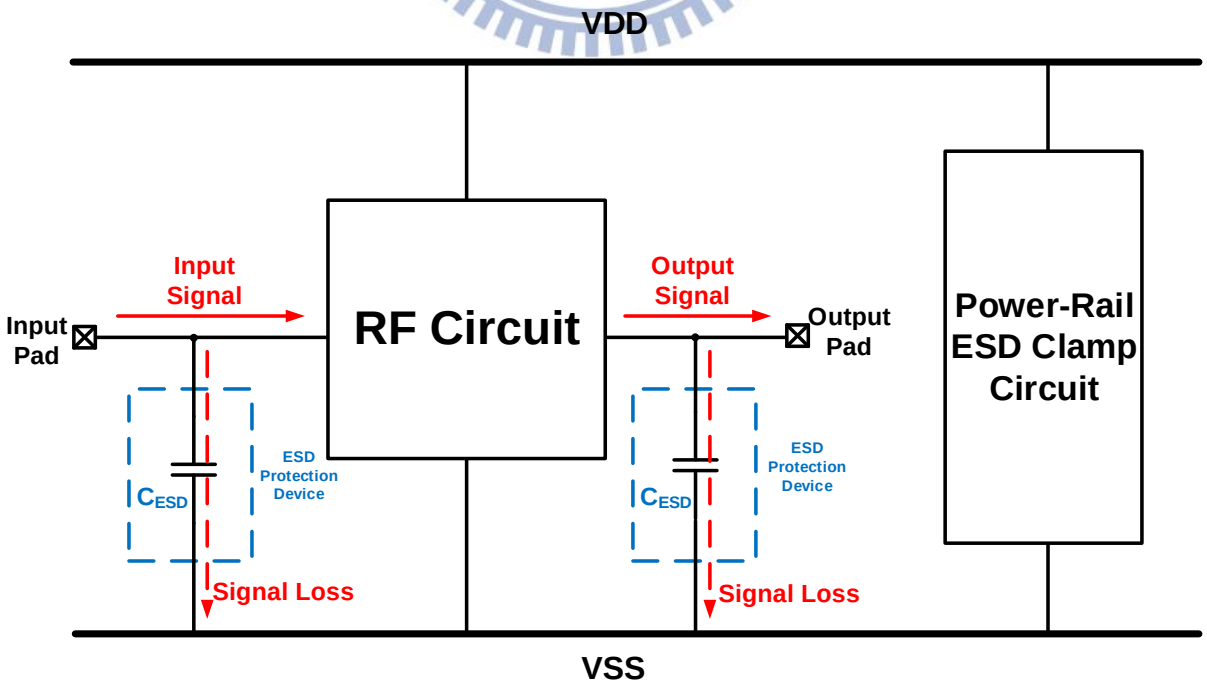


Fig. 2.20. Signal loss caused by the ESD protection device in RF circuit system.

Several circuit techniques are investigated to minimize the impact of on ESD protection device or co-design with the RF integrated circuits. The methods using stacked diodes, parallel LC, series LC, T-coil, and distributed diodes array will be introduced in the following.

(i) ESD protection design with stacked diodes

Stacked diodes method is the most intuitive way to reduce the parasitic capacitance. Fig. 2.21 shows the ESD protection design with stacked diodes architecture. The parasitic capacitance of stacked ESD diodes can be seen as capacitances in series. The original $2C_{ESD}$ will be divided into $2C_{ESD}/n$ if the I/O clamp circuits consist of stacked diodes with the number of n. Moreover, by using the polysilicon diode (P-I-N diode over the STI structure) which can be realized in standard CMOS process without additional masks, the substrate noise coupling effect can be eliminated [20]. However, the trade-off of the stacked diodes method is that the Ron of the discharging path will multiply by n and thus degrade the ESD robustness.

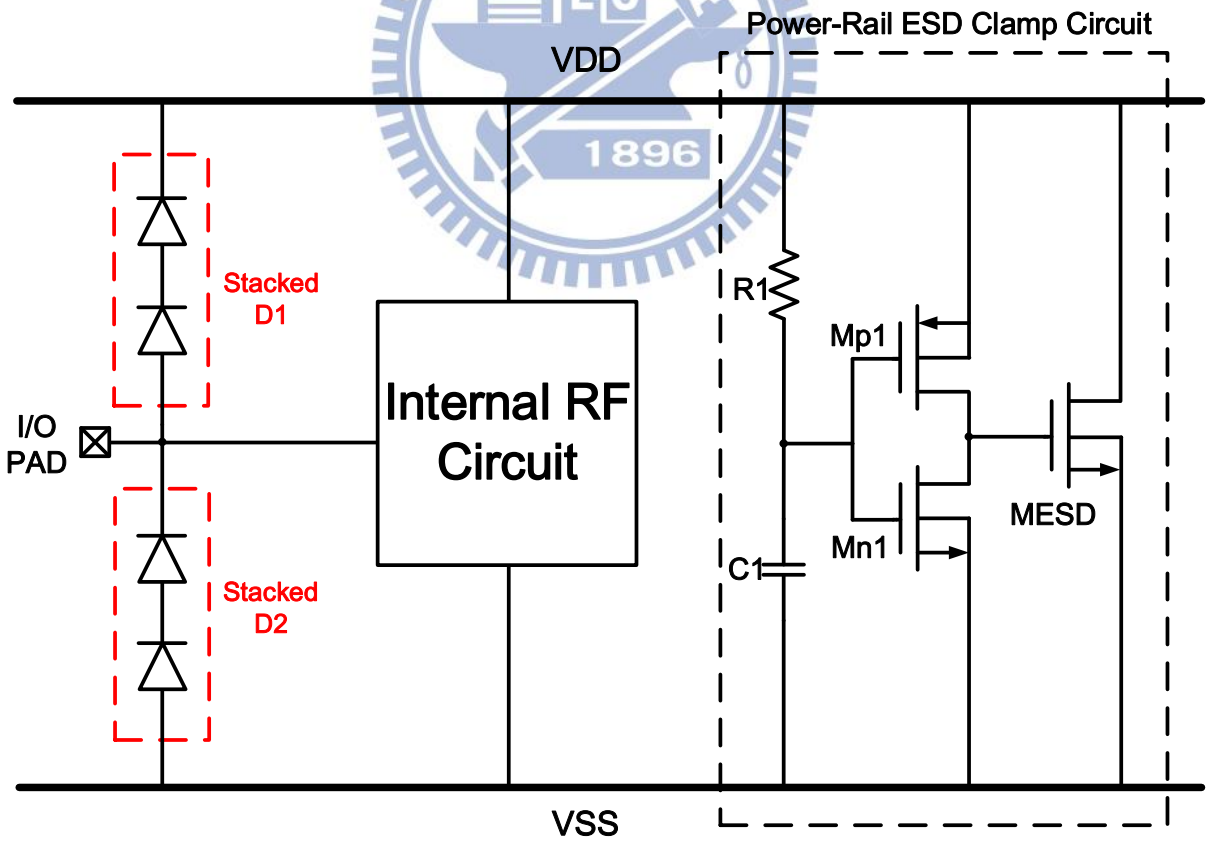


Fig. 2.21. ESD protection design with stacked diodes architecture.

(ii) ESD protection design with LC-tank

The parallel LC architecture is employed to isolate the capacitance of the ESD device, as illustrated in Fig. 2.22. The LC-tank is composed by an inductor and a capacitor in parallel which is inserted between the power line and the signal path. The LC-tank can be a variable impedance according to the operation frequency. When the circuit operates in the resonant frequency

$$\omega_0 = \frac{1}{\sqrt{L_{ESD}C_P}} = \frac{1}{\sqrt{L_{ESD}C_N}} \quad (rad/s) \tag{2.14}$$

the parallel LC-tank can be seen as a large impedance which isolates the parasitic capacitance of the ESD device from the signal path [21]. The signal with the interested frequency has little loss while operating at the resonant frequency. On the other hand, the inductor can be neglected in standby DC situation and the ESD conditions with lower frequencies relatively. Thus, the scheme can be simplified to the original I/O ESD clamp circuit.

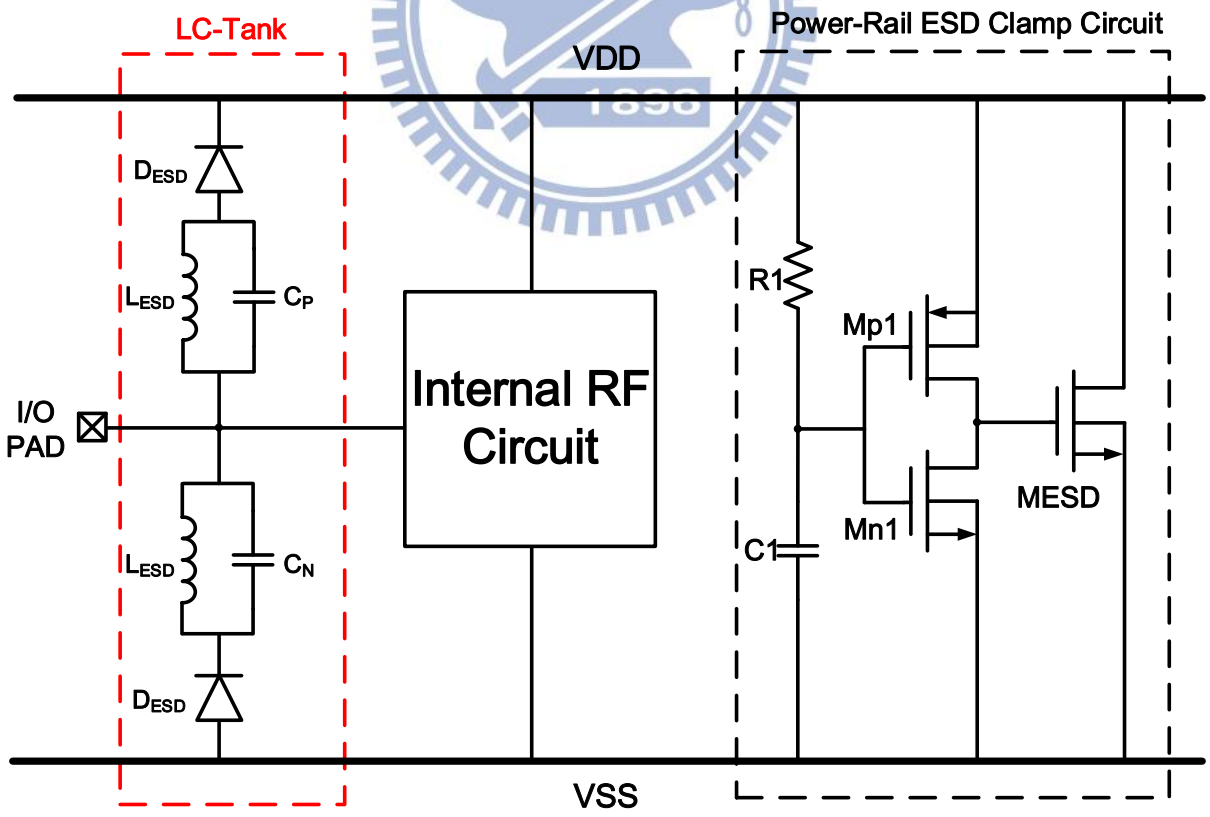


Fig. 2.22. ESD protection design with LC-tanks architecture.

(iii) ESD protection design with series LC

Another ESD protection method using the LC combination is the LC in series [22]. The ESD protection design with series LC architecture is drawn in Fig. 2.23. Different from the previous LC-tank technique, the impedance of the LC-series will be zero and serve as a low impedance path under the resonant frequency, ω_0. The general purpose of the LC series architecture design is focused on the broadband applications. The operating frequency of the applications is much higher than the LC-series resonant frequency. Under the adequate frequencies, the inductor L_{ESD} becomes a large impedance that block the parasitic capacitance of the ESD device away. In the standby DC and ESD conditions, the scheme is also reduced to the original I/O ESD clamp circuit. Furthermore, research has shown that the capacitance elimination of the ESD device can also be done by the series LC architecture [23].

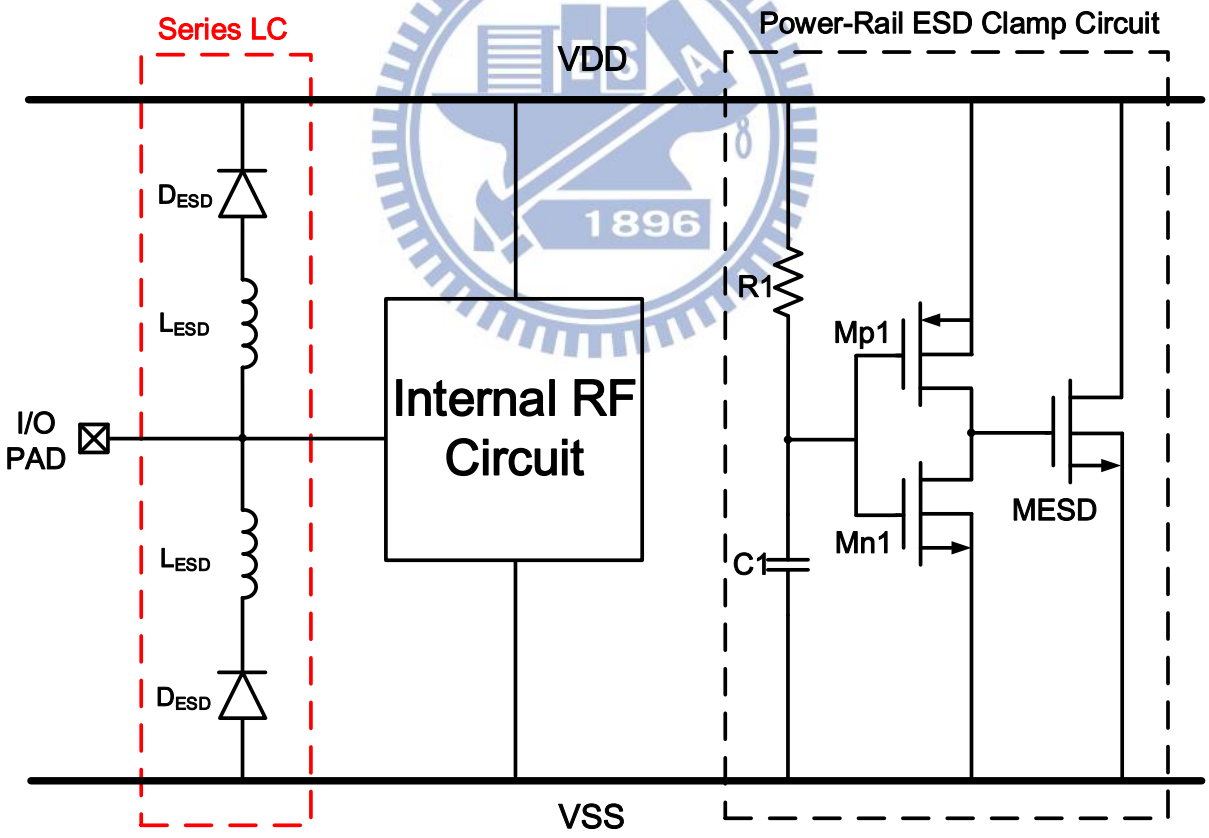


Fig. 2.23. ESD protection design with series LC architecture.

(iv) ESD protection design with T-coil

The T-coil network (Fig. 2.24) consists of two coupled inductors L_{ESD} having a coupling coefficient of k and a bridge capacitor C_B. With proper design, the T-coil circuit displays a purely resistive input impedance equals to the termination resistor R_T, i.e., $Z_{in} = R_T$ [24]. The condition holds for all frequencies for broadband ESD design once the relationship satisfied:

$$L_{ESD} = \frac{C_L R_T^2}{4}\left(1 + \frac{1}{4\zeta^2}\right) \tag{2.15}$$

$$C_B = \frac{C_L}{16\zeta^2} \tag{2.16}$$

$$\mathrm{k} = \frac{4\zeta^2 - 1}{4\zeta^2 + 1} \tag{2.17}$$

where C_L indicates the loading capacitance of the ESD diodes and the next stage, ζ is the damping factor of the network. The factor ζ and k are chosen to target a desired transfer function response.

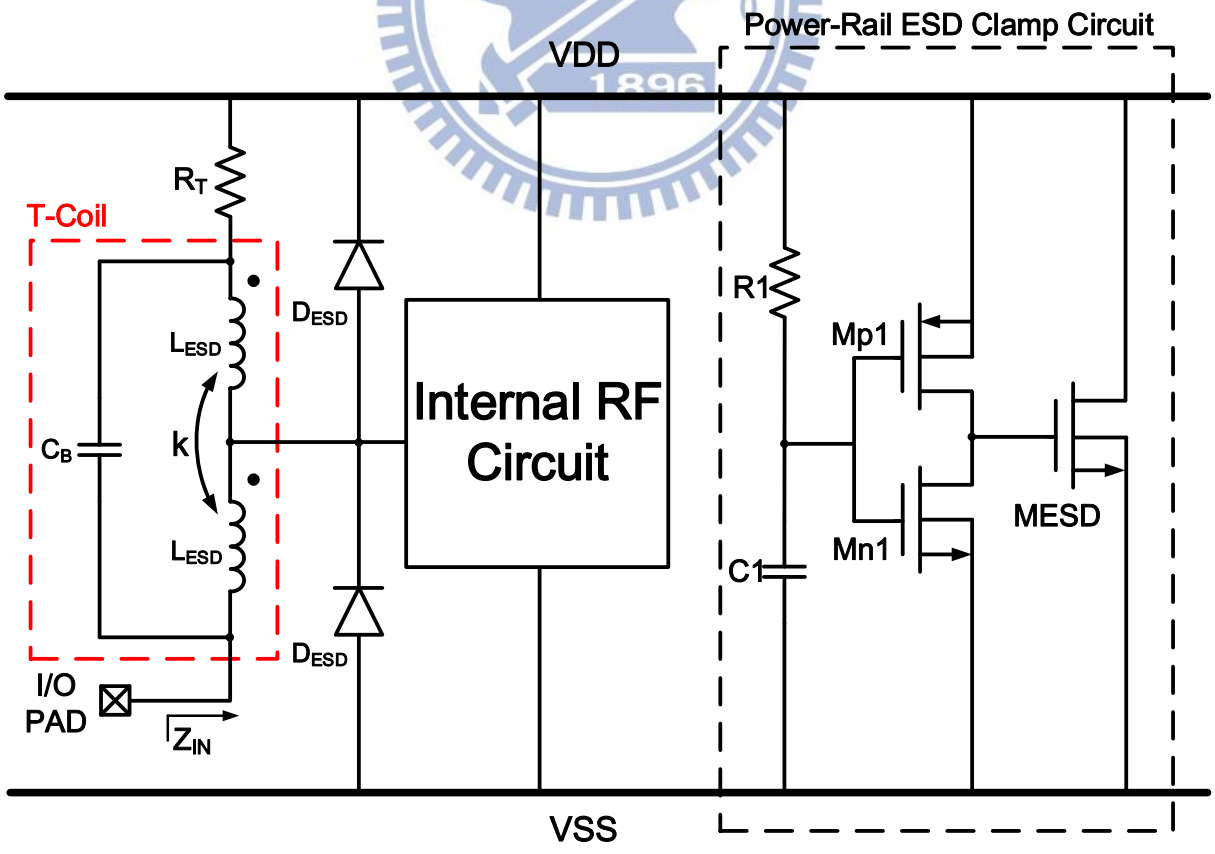


Fig. 2.24. ESD protection design with T-coil architecture.

(v) ESD protection design with distributed array

The concept of distributed array has been employed for distributed amplifier in microwave engineering to obtain wider bandwidth. Considering of the ESD design that suits for large bandwidth applications, the distributed concept for ESD protection are developed to absorb the capacitance introduced by the ESD device by artificial transmission line [25]. The effort of the distributed array can be understood by observing the smith chart which is overlapped by both impedance and admittance circle. The parallel capacitance will make the impedance point turn clockwise alone the admittance smith circle, then the series inductance will make it turn clockwise alone the impedance circle. As a consequence, the impedance point can be adjusted and return to the original characteristic 50 ohm point theoretically.

Furthermore, decreasing-size distributed ESD protection scheme has better ESD robustness than the equal-size distributed protection scheme [26]. As illustrated in Fig. 2.25, the ESD diode closest to the I/O pad will be the dominant protection device that discharge the ESD current.

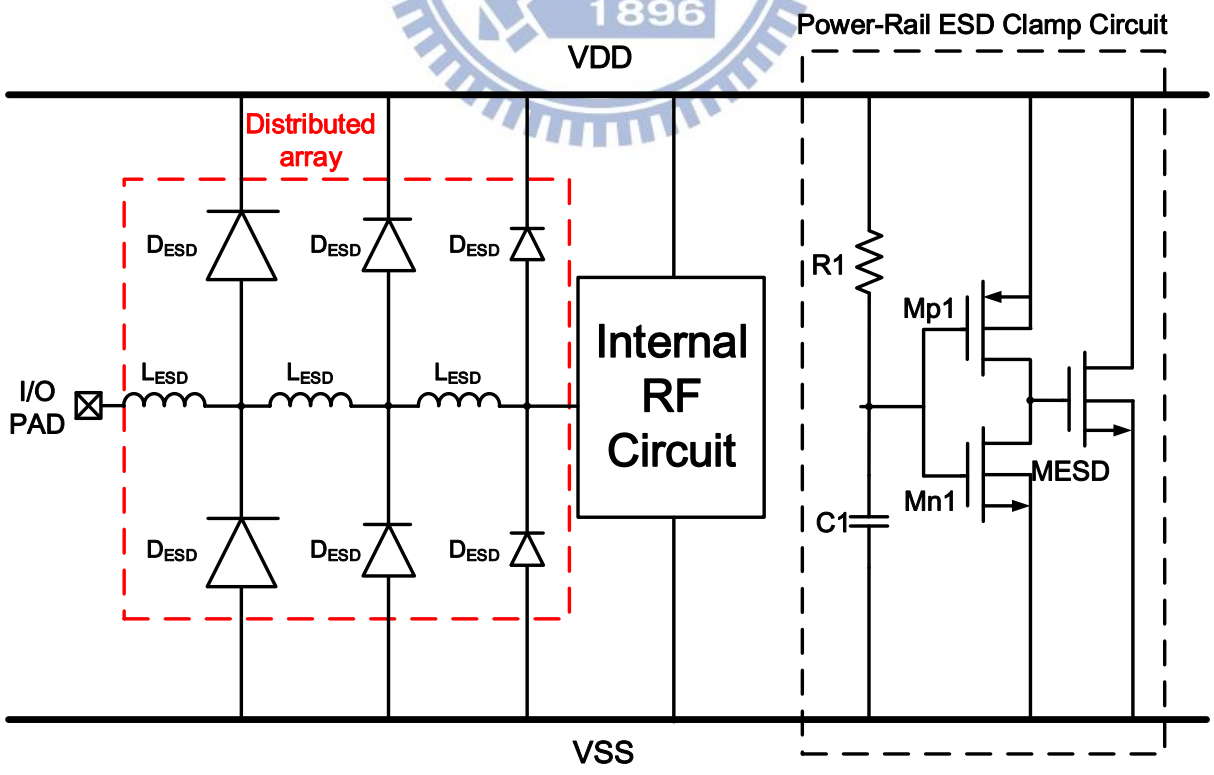


Fig. 2.25. ESD protection design with decreasing-size distributed array architecture.

2.4.2 Issues of ESD Protection Design on T/R Switch

In the conventional T/R switch with traditional ESD protection design in Fig. 2.19, the ESD robustness on PS-mode and ND-mode is usually worse than PD-mode and NS-mode. It is because the discharging path of the PS and ND-mode are longer than the PD and NS-mode and therefore the turn-on resistance of PS and ND-mode are larger than PD and NS-mode. A larger turn-on resistance R_{on} will result in higher clamping voltage on the interested pins under the same discharging current. As for PS-mode and ND-mode, since a simple conventional T/R switch is constructed by four n-type MOS transistors, the reversed body-diode of the NMOS can be an assistant discharge path for ND-mode. On the other hand, PS-mode ESD condition not only has the longest discharging path but also does not benefit from the body-diode of the NMOS. As a consequence, the ESD robustness on PS-mode is the most critical case among the four testing modes for conventional T/R switch. The conventional T/R switch requires specialized ESD protection design to focus on the PS-mode ESD event.

Now considering about the T/R switch implemented in the commercial cellular phones, the architecture of the T/R switch has to be modified to handle the high-power application's purpose. The traditional ESD protection method (Fig. 2.19) are reviewed again whether it is sufficient enough to face the ESD threat. Unfortunately, the large AC voltage swing on the transmit branch derived from (1.2) makes the conventional ESD protection design useless because the large RF signal will be delivered to the VDD and VSS node through the ESD diodes. Next, the rising time of RF signal is faster than the ESD transient and therefore the RC power-rail ESD clamp will be mis-triggered. Besides the large AC voltage swing, the existence of the body-floating resistance (R_{BF}) which is used to suppress the insertion loss in the high-power T/R switch, prevents the front-end parasitic path for ESD current discharging. ESD protection designs based on silicon layout skills are not available. For the reasons above, ESD protection circuit design for high-power T/R switch is a difficult challenge with reliability concerns.

2.4.3 Conventional Silicon-Controlled Rectifier for ESD Protection

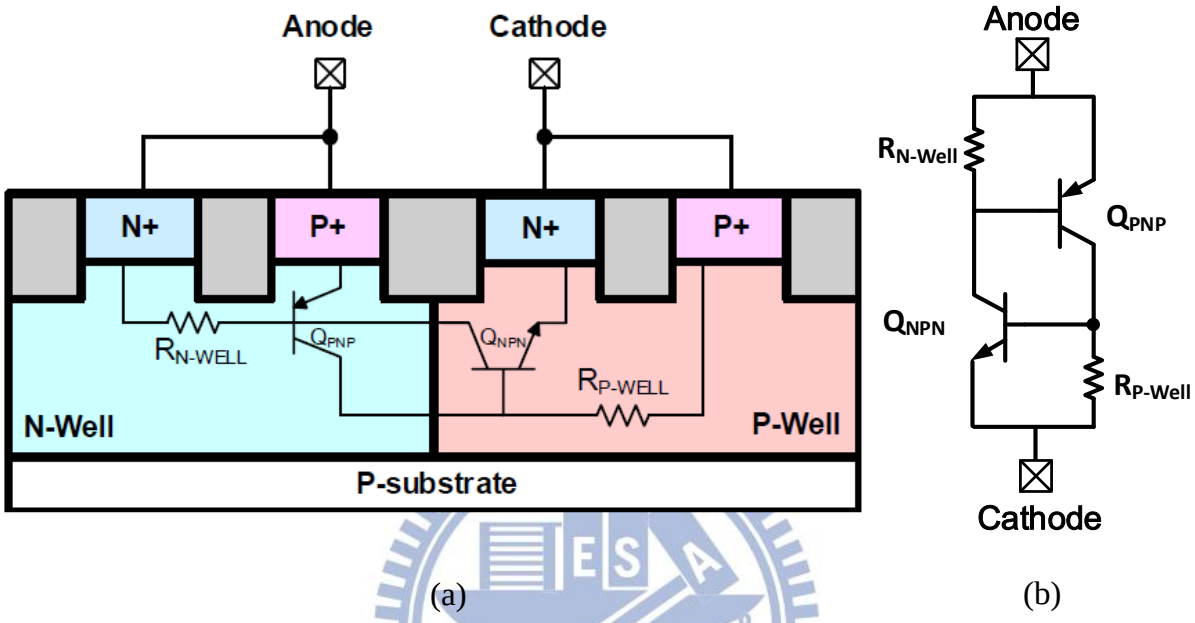
A silicon-controlled rectifier (SCR) has been a suitable ESD protection device in RF ICs due to its low parasitic capacitance and high ESD robustness [27]. A basic SCR device is constructed by P-N-P-N path in front-end of line. As illustrated in Fig. 2.26(a), the P-N-P-N structure can be seen as capacitors in series and introduce less capacitance than the traditional ESD diodes. The equivalent circuit of a SCR device is sketched in Fig. 2.26(b), which consists of vertical bipolar junction transistor Q_{PNP} and lateral bipolar junction transistor Q_{NPN}.

The trigger voltage of the SCR device is determined by N-P breakdown voltage of the specific process. When positive ESD stress on the anode node exceeds the avalanche breakdown voltage between N-Well and P-Well, a large number of holes and electrons pairs generated in the depletion region will be swept to both sides by electric field and cause voltage drops on the resistor $R_{P\text{-}Well}$ and $R_{N\text{-}Well}$. The bipolar junction transistor Q_{NPN} (Q_{PNP}) will be turned on once the voltage potential in the P-Well (N-Well) exceeds the turn-on voltage of the BJT. More and more current conducted by the BJTs increases the voltage drop on the resistance of the well, turns on BJTs better, and thus forms a positive feedback system for ESD current discharging. As for negative ESD stress, the simple P-Well to N-Well diode path will be forward biased to discharge the current. Fig. 2.27 shows the TLP I-V curve of a typical SCR device, where the unique snap-back phenomenon can be observed at the triggering point (V_{t1}, I_{t1}).

However, in spite of the high ESD robustness and low capacitance, the turn-on voltage of the SCR is usually much higher than the oxide breakdown voltage of the transistors in the specific fabrication process. The inner circuit will be damaged before the SCR start to pull down the ESD stress. Therefore, an appropriate triggering method is need to ensure that the V_{t1} to be smaller than the oxide breakdown voltage. With a suitable triggering design, the SCR can be turned on quickly to sustain high ESD level in a small device dimension.

The latch-up issue is another concern for SCR device. Once the SCR device is mis-triggered on by noise or ripples during the normal circuit operations, the SCR device will lower

the voltage at the specific point and cause a large current leakage. In addition to the inevitable function error, the worst situation is to burn the whole IC. Fortunately, with the aids of process advances (later than 90-nm CMOS process), the supply voltage of the core IC has been lower to 1V. The opportunity of the SCR's latch-up condition is reduced.



(a) (b)

Fig. 2.26. (a) Cross-section view and (b) equivalent circuit of SCR device.

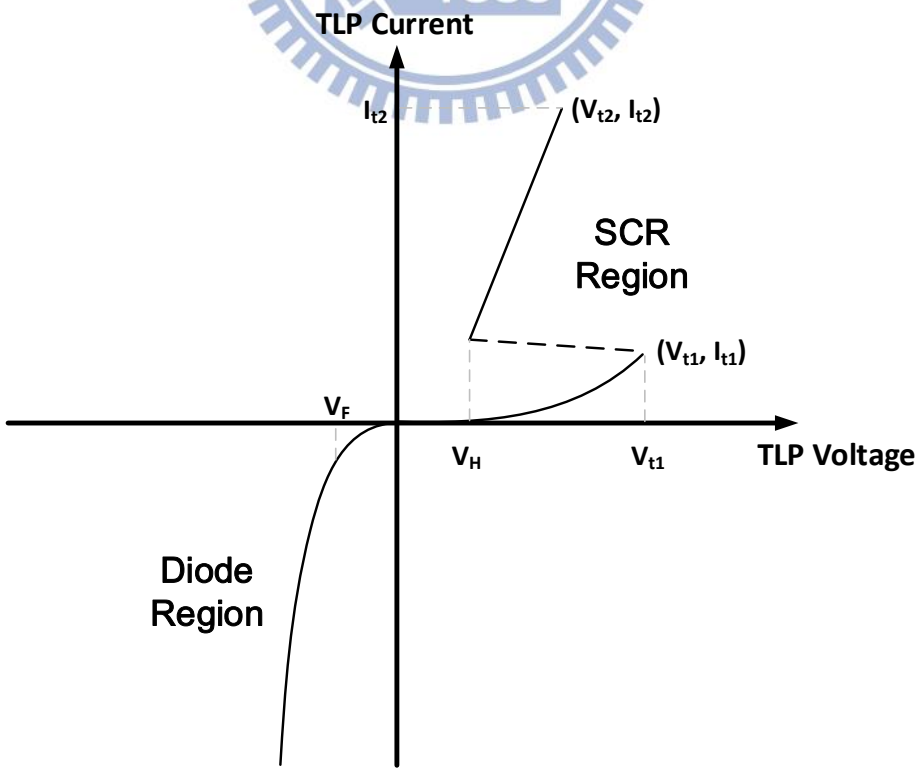


Fig. 2.27. TLP characteristics of SCR device.

Chapter 3

ESD Protection Design for High-Power T/R Switch

3.1 Circuit Design of High-Power T/R Switch

Recently, the RF circuit blocks such as low-noise amplifiers (LNAs), mixers, voltage-controlled oscillators (VCOs) have been integrated in a single SOC for lower cost, high integration capability, and high yield [1]. However, reliability issues occur on the CMOS IC when the operating power increases. As a consequence, gallium arsenide (GaAs) technology or silicon-on-insulator (SOI) technology implemented for power amplifiers and antenna switches is still in the trend. Researchers have made lots of attempts to overcome the reliability obstacles in high-power CMOS switches: adaptive voltage distribution method [12], resistive body-floating technique [16], LC-tuned substrate technique [29]. For the realistic applications in the GSM/WCDMA mobile communication market, stacked-transistors architecture are an intuitive method utilized to meet the specifications of the linearity requirements to about 30dBm [11].

In this work, the high-power T/R switch using the series-shunt topology with stacked transistors architecture and is implemented in a 0.18-μm standard CMOS process. The schematic of the high-power T/R switch is illustrated in Fig. 3.1. There are 6 terminals in the schematic, including ANT, TX, RX, $V_{TX,}$ V_{RX}, and GND. By given the controlling voltage signal V_{TX} and V_{RX}, the operation mode of the circuit can be determined. In the circuit schematic, M1 ~ M4 and M6 ~ M8 are the series transistors of RX branch and TX branch, respectively. Similarly, M5 and M9 ~ M12 are the shunt transistors of RX branch and TX branch, respectively. The number of the stacked transistors is determined by specifications of power handling capability. Considering of the voltage stress in transmit mode circuit operations, M1

~ M4 and M9 ~ M12 are in off-state and stacked in series to sustain the high AC voltage swing. However, the stacked M1 ~ M4 will increase the insertion loss in RX branch since the turn-on resistance is multiplied by the number of the stacked transistors. The trade-off of the series-shunt T/R switch with stacked transistors architecture can obtain higher power compression point in transmit mode by sacrifice the insertion loss of the receive mode.

In order to endure the high power in TX branch, the dimension of the transistors M6 ~ M8 are chosen as large device to handle the large AC current. The W/L ratio of M6 ~ M8 is 1500/0.35 (μm), which is the largest dimension ratio in the T/R switch. The transistors in RX branch, M1 ~ M4, the W/L ratio is 1000/0.35 (μm) to obtain a lower Ron for lower insertion loss. The W/L ratio of the shunt transistors M5 and M9 ~ M12 are 500/0.35 (μm) to enhance the isolation of the T/R switch. As introduced in section 2.1.3, the 10kohm large resistance is employed at the gate and body to ease the voltage stress on the gate oxide and therefore enhance the power handling capability. The capacitor C1 ~ C4 with 0.5pF are called feed-forward capacitor to prevent unequally distributed voltage swing on the C_{GS} and C_{GD} of the stacked transistors in the off-state.

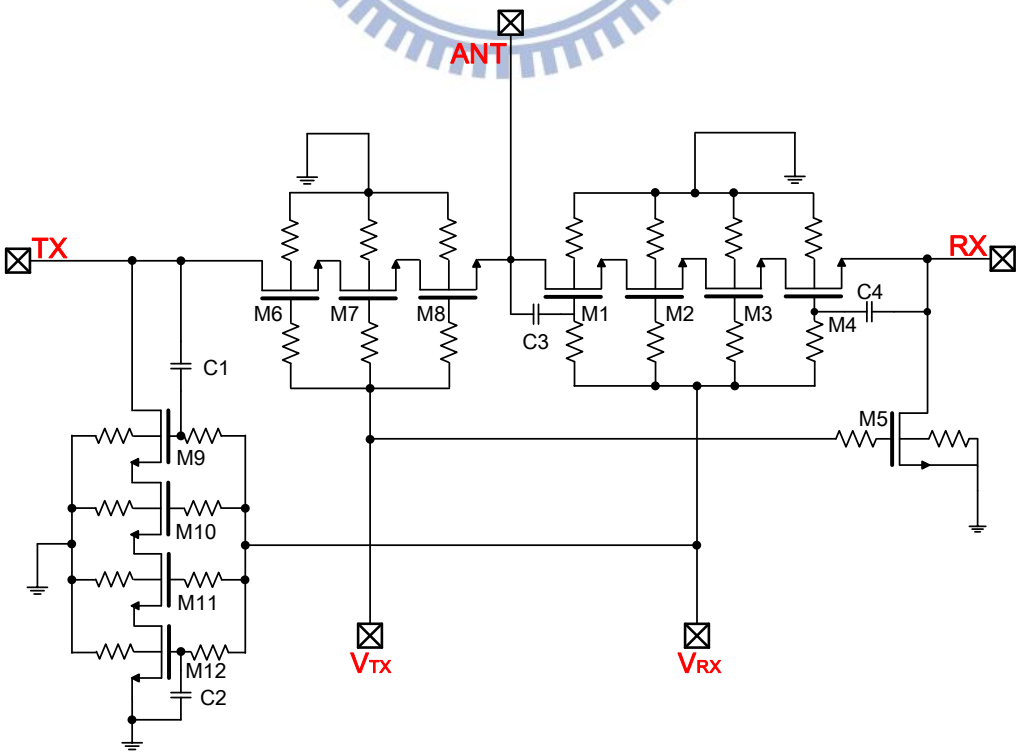


Fig. 3.1. Circuit schematic of a high-power T/R switch.

3.2 Proposed ESD Protection Design for High-Power T/R Switch

ESD is an inevitable threat for the using of cellphone in our daily life. The frictions and rubbings will induce positive or negative charges and rush into the RF transceiver front-end module by antenna. Thus, the high-power T/R switch requires ESD protection circuits to discharge the ESD current before the unwanted charges damage the inner circuit. The prior study [11] installed the ESD protection circuits on the RX port of the T/R switch (Fig. 3.2) rather than ANT port and claimed that the design can sustain high ESD robustness up to 8.5kV. The ESD design in [11] cleverly avoided the mis-triggering risks of the ESD protection devices during the transmit mode since the RX branch was in off-state to isolate the ESD diodes from the transmit path. However, though the large voltage signal from PA will be clamped if the ESD stacked diodes are installed in the antennal (ANT) port, it is not a sufficient reason to move the ESD protection circuit away from the ANT port to RX port. The ESD protection devices on RX port are inadequate to protect the transistors of the T/R switch circuit since the ESD stress is right zapping on the ANT port. The uncertain state of the transistors cannot guarantee the ESD current can be completely delivered to the ESD devices on the RX port. This strategy misses the original intention of ESD protection design.

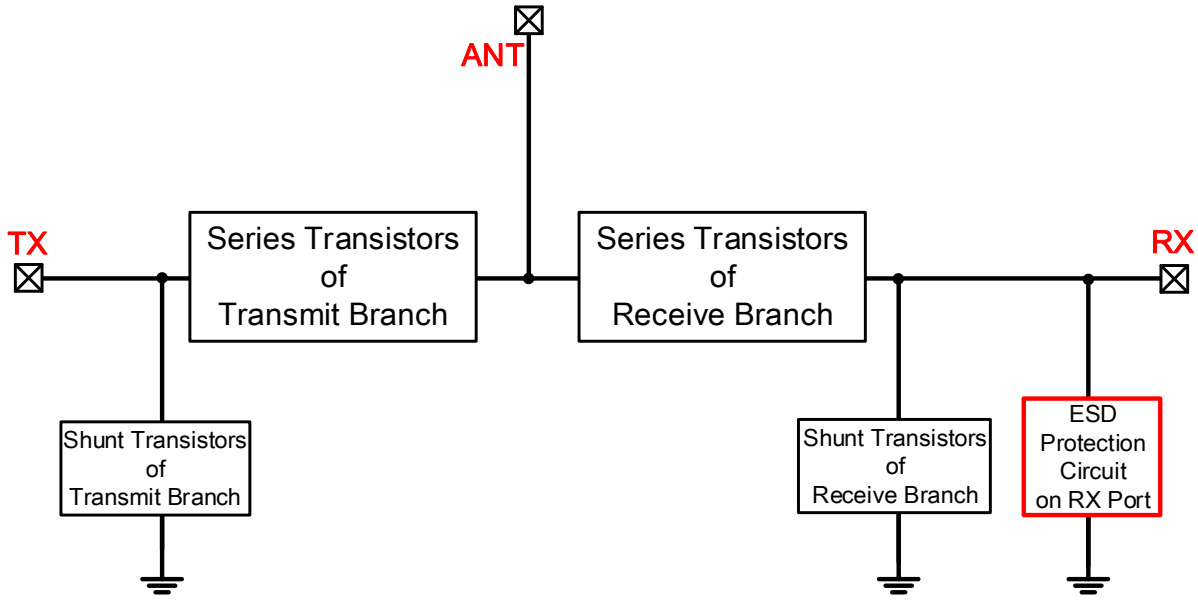


Fig. 3.2. The schematic of ESD protection design for high-power T/R switch on RX port.

In the previous paragraph, the ESD protection design for high-power T/R switch with stacked transistors architecture on ANT port by using additional ESD discharge path such as ESD diodes seems to be a difficult challenge for circuit designers because of the high-power signal from PA is an ESD-like transient that will mis-trigger on the ESD protection device. What's worse is, as depicted in section 2.4.2, the existence of the 10kohm body-floating resistance prohibit the parasitic discharge path in the silicon front-end of line. In summary, whether the traditional ESD protection method of adding extra ESD protection device or embedded discharging path by layout skills, they are not suitable ESD protection strategies for high-power T/R switch. With the realistic perspective given above, the ESD protection designers are forced to develop a more effective solution for high-power T/R switch.

In this work, the proposed ESD protection design makes a preliminary attempt to deal with the PS-mode ESD threat on the ANT port. The schematic of the proposed ESD protection design is drawn in Fig. 3.3. A transient detection circuit is located at the ANT port. The main purpose of the ESD transient detection circuit is to distinguish between ESD transient in ESD events and the RF signal in normal circuit operations. With a proper transient detection circuit, the ESD current are discharge to ground by the inherent RX transistors of T/R switch itself.

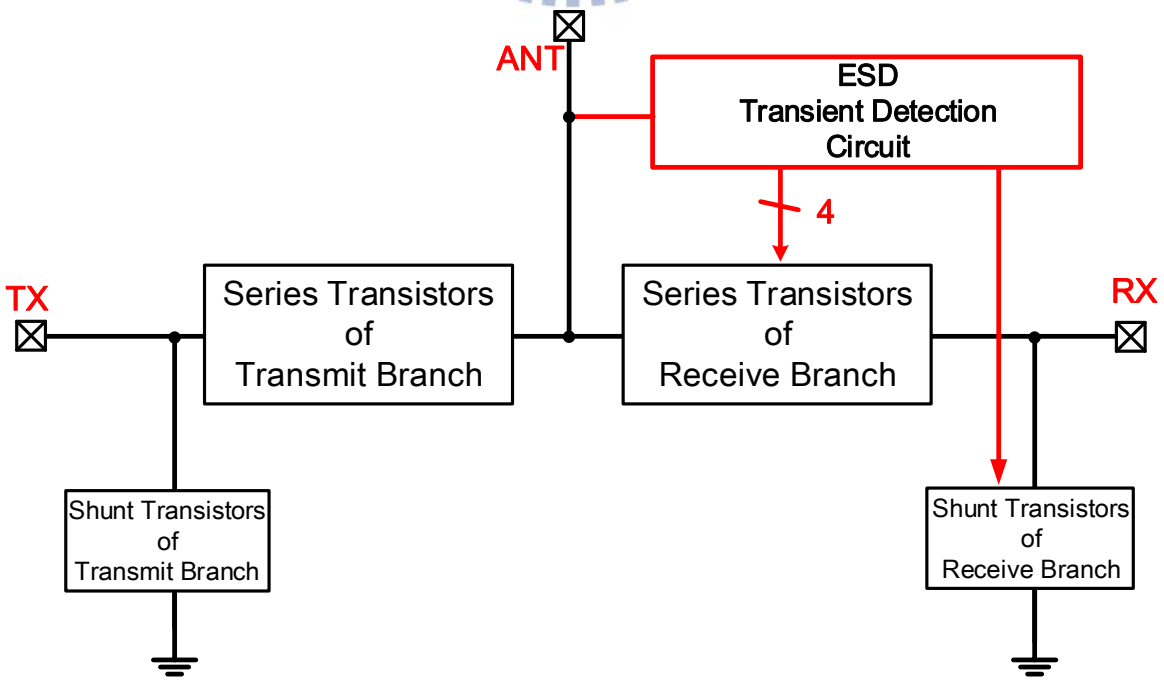
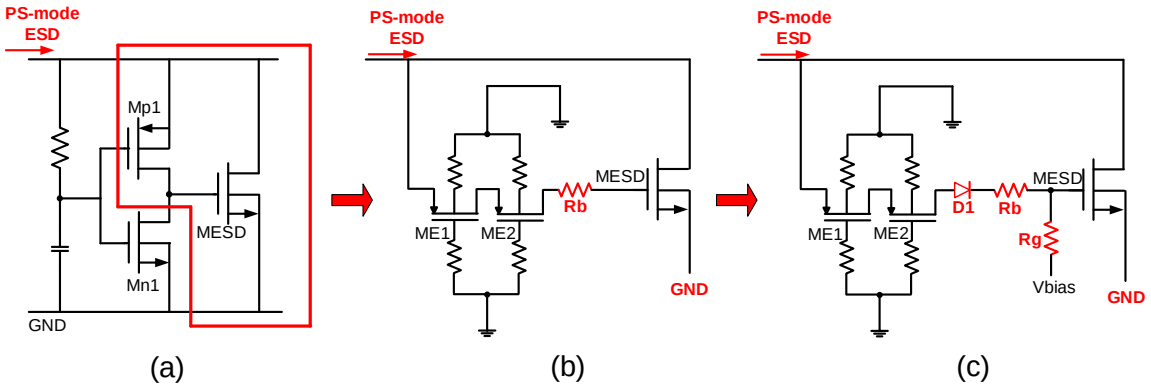


Fig. 3.3. The schematic of the proposed ESD protection circuit design.

The idea of the ESD transient detection circuit was inspired from the traditional ESD power-rail clamp circuit. The evolution of the design is depicted in Fig. 3.4. In the RC-invertor clamp circuit, the large transistor M_{ESD} is turned on by the transistor Mp1, which charges the gate of M_{ESD} during the ESD events. The RC element in the power-rail clamp circuit are used to identify the ESD transient from the normal circuit power-on conditions. Besides, a low standby leakage current is one of the features of the power-rail ESD clamp circuit. However, the high-power T/R switch circuit acts like a tunable signal delivering path for transmit/receive mode, the connection to the VDD node does not exist. Thus, only the PMOS Mp1 and large M_{ESD} in the power-rail clamp circuit are needed. The traditional power-rail clamp circuit can be simplified to the red frame in Fig. 3.4(a). Next, in order to endure the large AC voltage swing from PA, the PMOS are stacked and equipped with gate resistor and body-floating resistors, just like the transistors in the T/R switch circuit. Moreover, a blocking resistors R_b with 10kohm is employed to block the normal RF signal. Since the frequency (GHz) of the RF signal is much faster than the ESD transient (MHz), the blocking resistor R_b can block the RF signal (considered as AC floating) whereas the slower DC-like ESD transient can pass through it and charge the transistors in the RX branch (M_{ESD} is an analogy of RX transistors). The schematic is shown in Fig. 3.4(b). At last, in Fig. 3.4(c), a diode D1 is inserted between the gate of the M_{ESD} and the detection circuit to ensure the bias of the transistors in normal circuit operations.



(a) (b) (c)

Fig. 3.4. The evolution of the ESD transient detection circuit from (a) power-rail clamp circuit, (b) stacked PMOS and resistor R_b to distinguish the RF signal and ESD transient, and (c) diode D1 and resistor R_g to ensure the normal DC voltage bias of the RX transistors.

The whole circuit of the proposed ESD protection design schematic is shown in Fig. 3.5. In this thesis, this protection scheme is named “type 1” ESD protection design for high-power T/R switch. The dimension ratio W/L of the PMOS transistors ME1, ME2, and ME3 is 300/0.35 (μm). The turn-on resistance Ron of ME1 ~ ME3 will affect the trigger time of the RX transistors to discharge the ESD current. Besides, the number of the stacked “ME” transistors influence the power compression point, too. Considering if there is only one “ME” transistor, the large voltage swing will not only affect the gate voltage of M1 ~ M5 more easily but also cause oxide breakdown reliability and therefore degrade the efficiency in the transmit mode. Finally, diodes are utilized to make sure the proposed ESD protection design does not affect the normal circuit operations. As shown in Fig. 3.6 and Fig. 3.7, the diode D_1 and diode strings can clamp the DC voltage bias on the gate of M1~M12 in the T/R switch circuit.

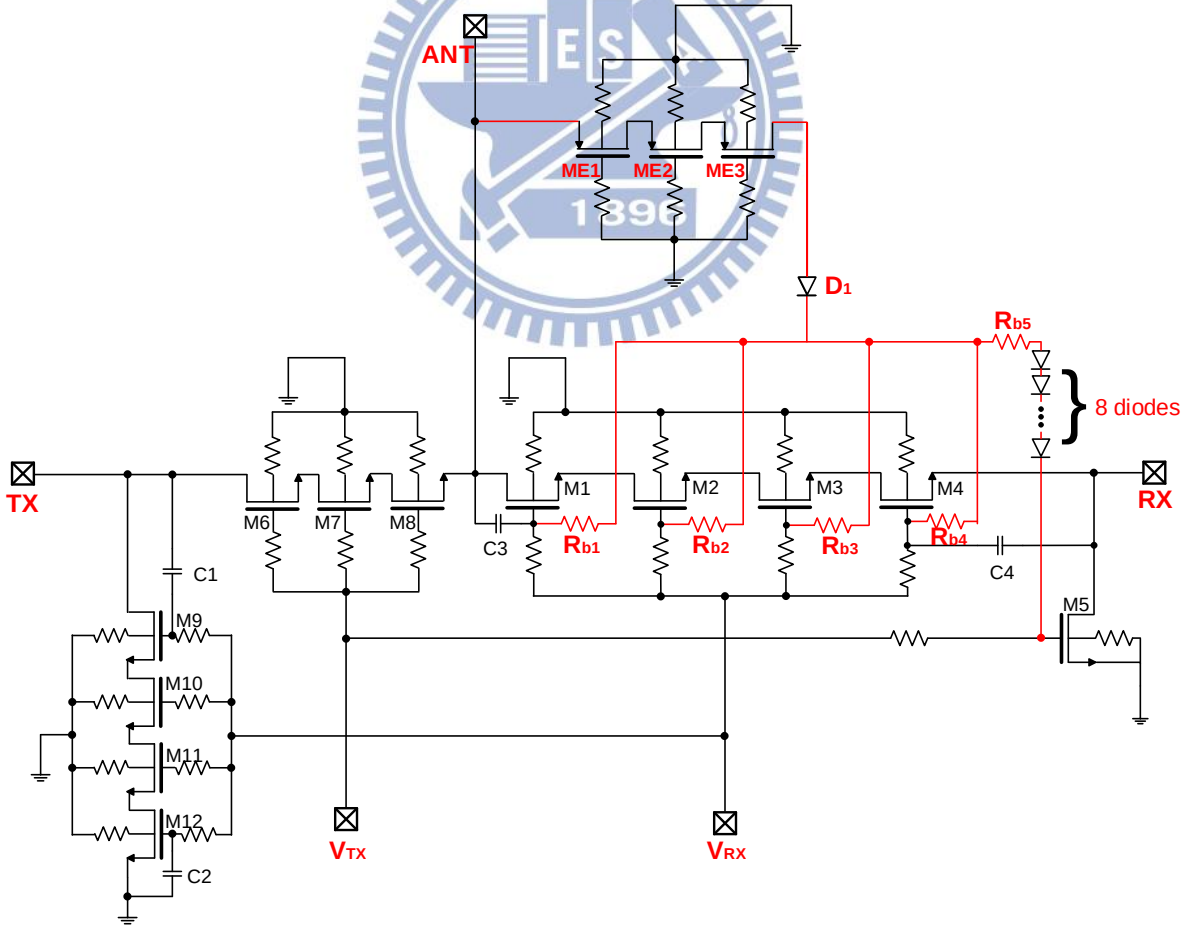


Fig. 3.5. Type 1 circuit realization schematic of the proposed ESD protection design for high-power T/R switch.

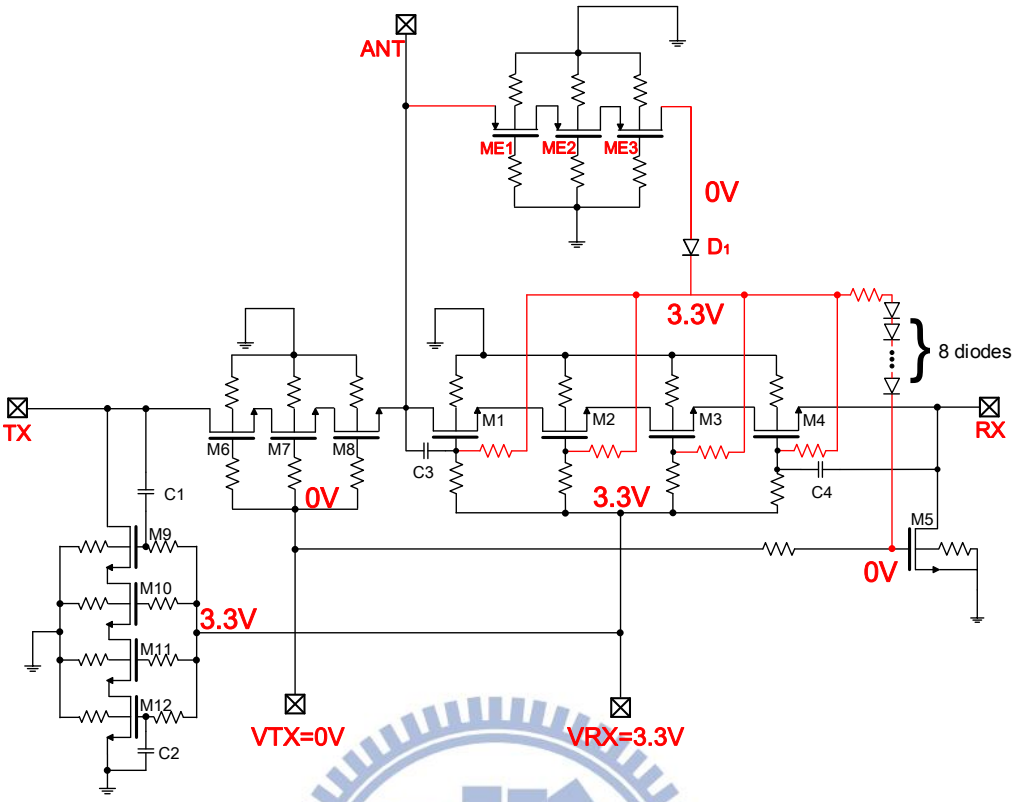


Fig. 3.6. DC voltage distribution in type 1 ESD protection design for high-power T/R switch operates in receive mode, where V_{RX}=3.3V and V_{TX}=0V.

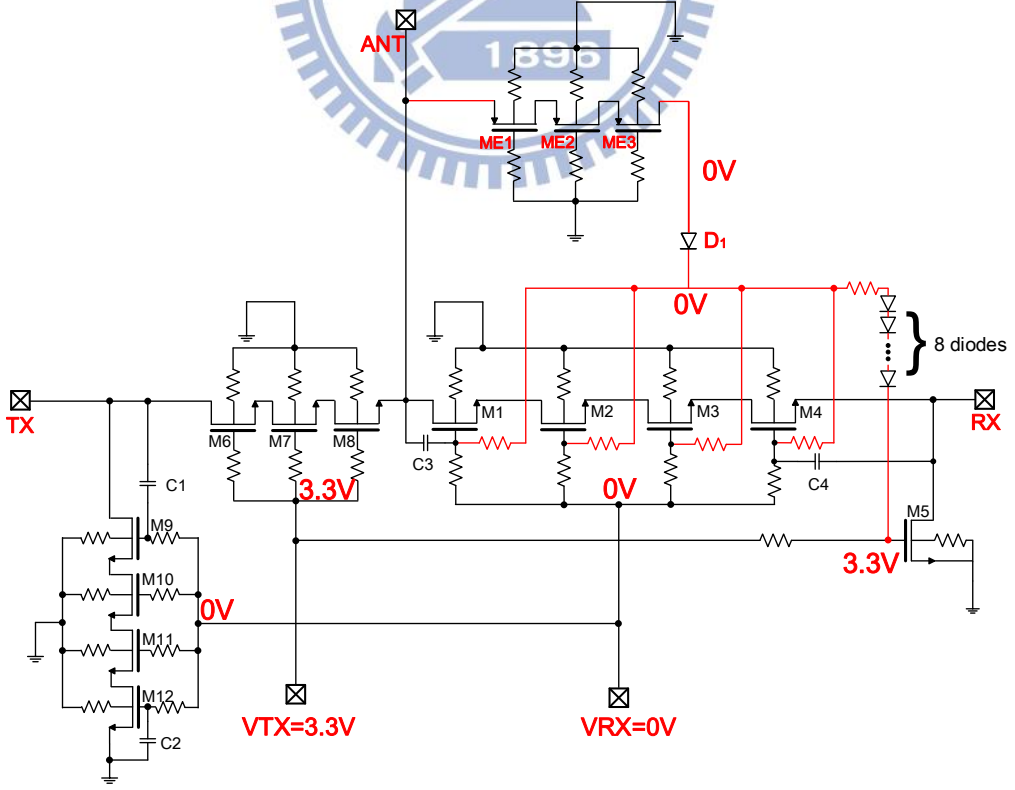


Fig. 3.7. DC voltage distribution in type 1 ESD protection design for high-power T/R switch operates in transmit mode, where V_{RX}=0V and V_{TX}=3.3V.

For the NS-mode ESD events on the ANT port, the discharging paths of the proposed design are from the parasitic BJTs of the stacked-transistors of both RX and TX branch. As illustrated in Fig. 3.8 (the N+ diffusion in NWell is floated and omitted in the figure), the base of a single BJT is connected to the 10kohm body-floating resistor. The parasitic BJTs will be turned on to discharge the current during the NS-mode ESD events.

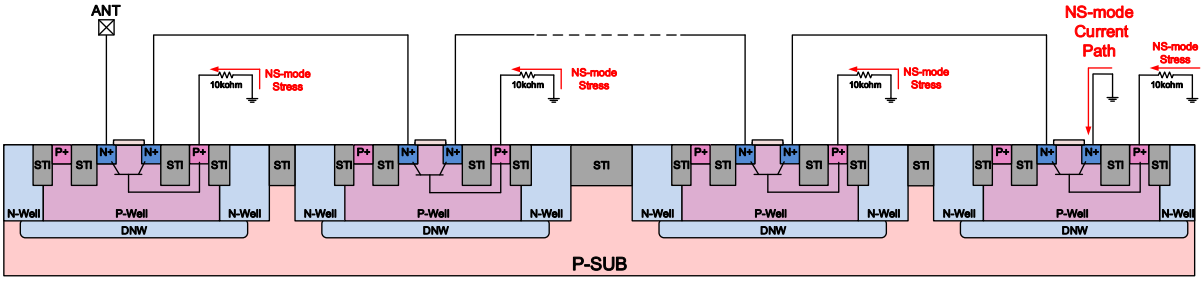


Fig. 3.8. Cross-section view of the stacked-transistors showing the parasitic BJTs of NS-mode discharging path in the type 1 ESD protection design.

In the high-power T/R switch with body-floating technique, the body of the transistor is separated from the source and connected with a large resistor to the ground. In type 1 proposed ESD protection design, since the ESD stress is delivered from drain to source rapidly after the M1 ~ M5 are triggered in PS zapping mode, the body voltage of the transistors cannot keep on with the source. The voltage difference between source and body will increase the threshold voltage V_{th} of the NMOS transistors due to the body effect. The risen of the V_{th} can be understood by the fundamental semiconductor physics equation:

$$V_{th} = V_{t0} + \gamma\left(\sqrt{V_{SB} + 2\varphi_f} - \sqrt{2\varphi_f}\right) \tag{4.1}$$

where the V_{t0} represents the threshold voltage for zero substrate bias, γ is the body-effect parameter, and φ_f means the Fermi level of the p-type substrate.

The increasing V_{th} is not a good thing for type 1 ESD protection design, because the transistors M1 ~ M5 requires a larger gate voltage to turn on to discharge the ESD current. Fig. 3.9 depicts the type 2 ESD protection design. With body and source connected to each other, the rising of the threshold voltage can be eliminated. The PS-mode ESD robustness of the type

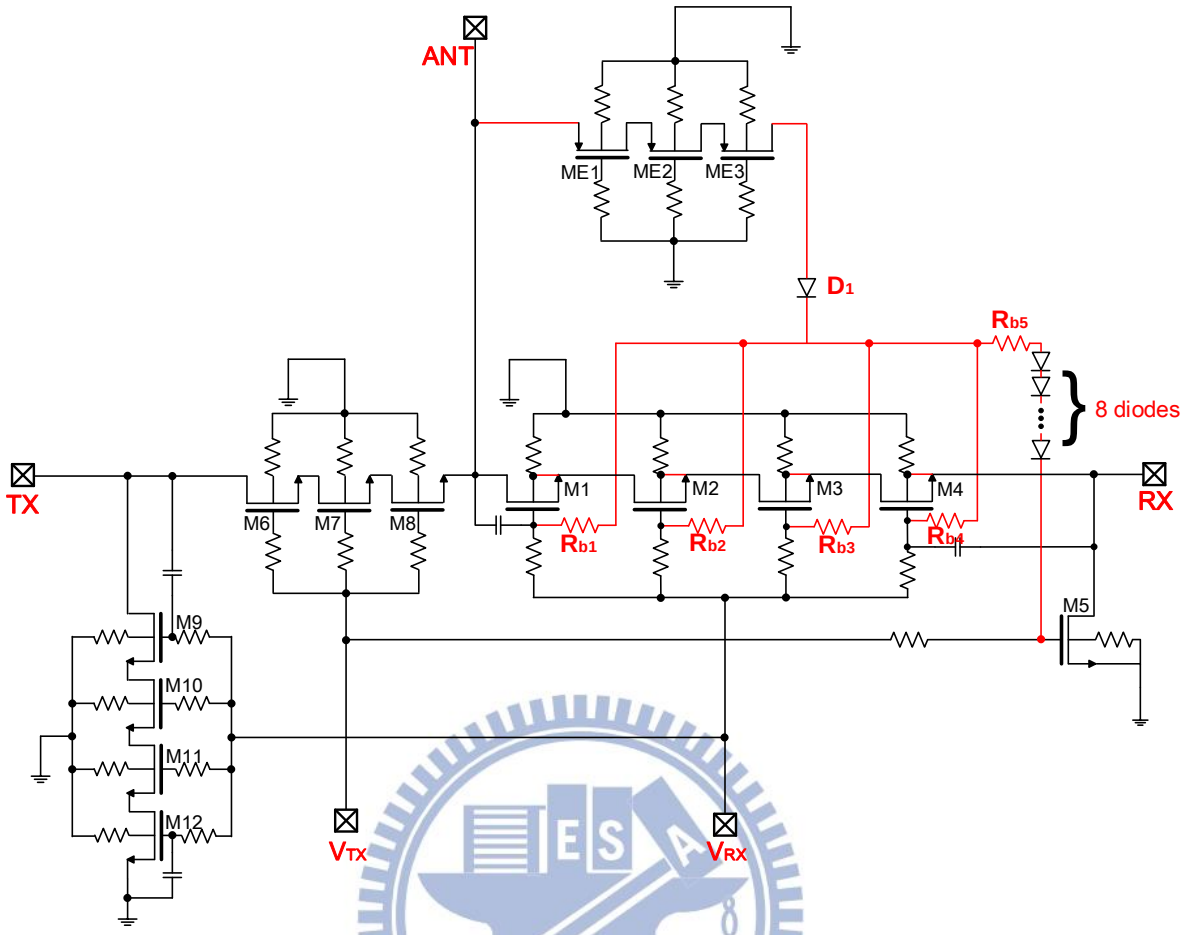


Fig. 3.9. Circuit realization schematic of the proposed type 2 ESD protection design for high-power T/R switch.

2 ESD protection design will be better than the type 1 ESD protection design for the transistors in type 2 ESD protection design do not suffer from the body effect. However, the drawback is the insertion loss and linearity performance in transmit mode is degraded for the RF signal leaks to RX port more easily with the aids of the body-source connection.

The cross-section view of the NS-mode discharging path of type 2 ESD protection design is sketched in Fig. 3.10. A parasitic diode strings are formed naturally with the connection of the reverse body-diodes in the n-type transistors. The parasitic diodes of the RX transistors will be smoother discharging path compare to the BJT path in TX. Therefore, the NS-mode ESD robustness will be higher than the type 1 ESD protection design, too.

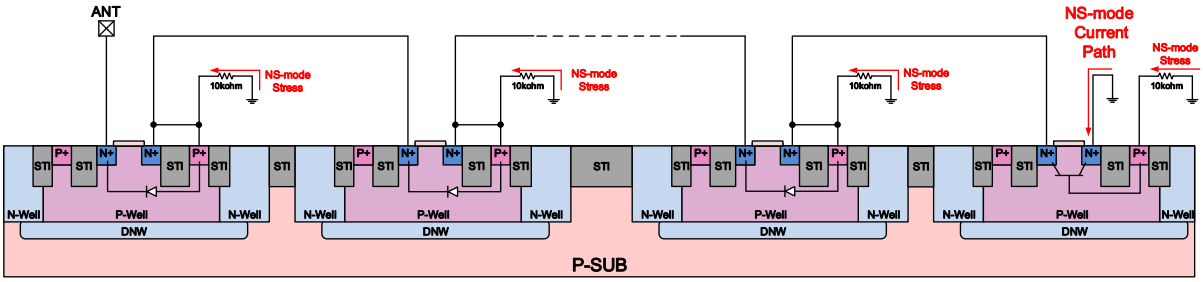


Fig. 3.10. Cross-section view of the stacked-transistors showing the parasitic diodes of NS-mode discharging path in the type 2 ESD protection design.

After the description of PS-mode and NS-mode, now the ESD events of positive-to-VDD (PD-mode) and negative-to-VDD (ND-mode) are concerned. As introduced in section 2.4.2, the ANT node of the high-power T/R switch are not connected to the VDD node by diode because not only the large PA signal will be clamped but also the additional diode will results in the degradation of the RF performance. Hence, in a simple high-power T/R switch circuit, there is no direct connection to the VDD node. However, the PD-mode and ND-mode testings are still necessary to be done for ESD robustness of an IC in all aspects.

The PD-mode and ND-mode discharging paths for a high-power T/R switch integrated in a RF SoC (System on Chip) is illustrated in Fig. 3.11. The discharging paths of the PD-mode and ND-mode ESD tests on the ANT port are marked in the red line and blue line in Fig. 3.11, respectively. A power-rail ESD clamp circuit is a common ESD protection circuit which is installed in an IC product. Besides, with a proper design, a traditional RC-invertor power clamp circuit can achieve the ESD level of ±8kV easily. As a consequence, the weakest point of the PD-mode and ND-mode discharging paths are still at the ANT-to-VSS path in the high-power T/R switch. In other words, the ESD robustness of high-power T/R switch under PS-mode and NS-mode determine the ESD levels of PD-mode and ND-mode. The proposed ESD protection design kills two birds with one stone to enhance the comprehensive ESD robustness. The measured DCIV curves and RF performance of the proposed ESD protection design after PS-mode and NS-mode ESD stress are arranged in section 3.3.

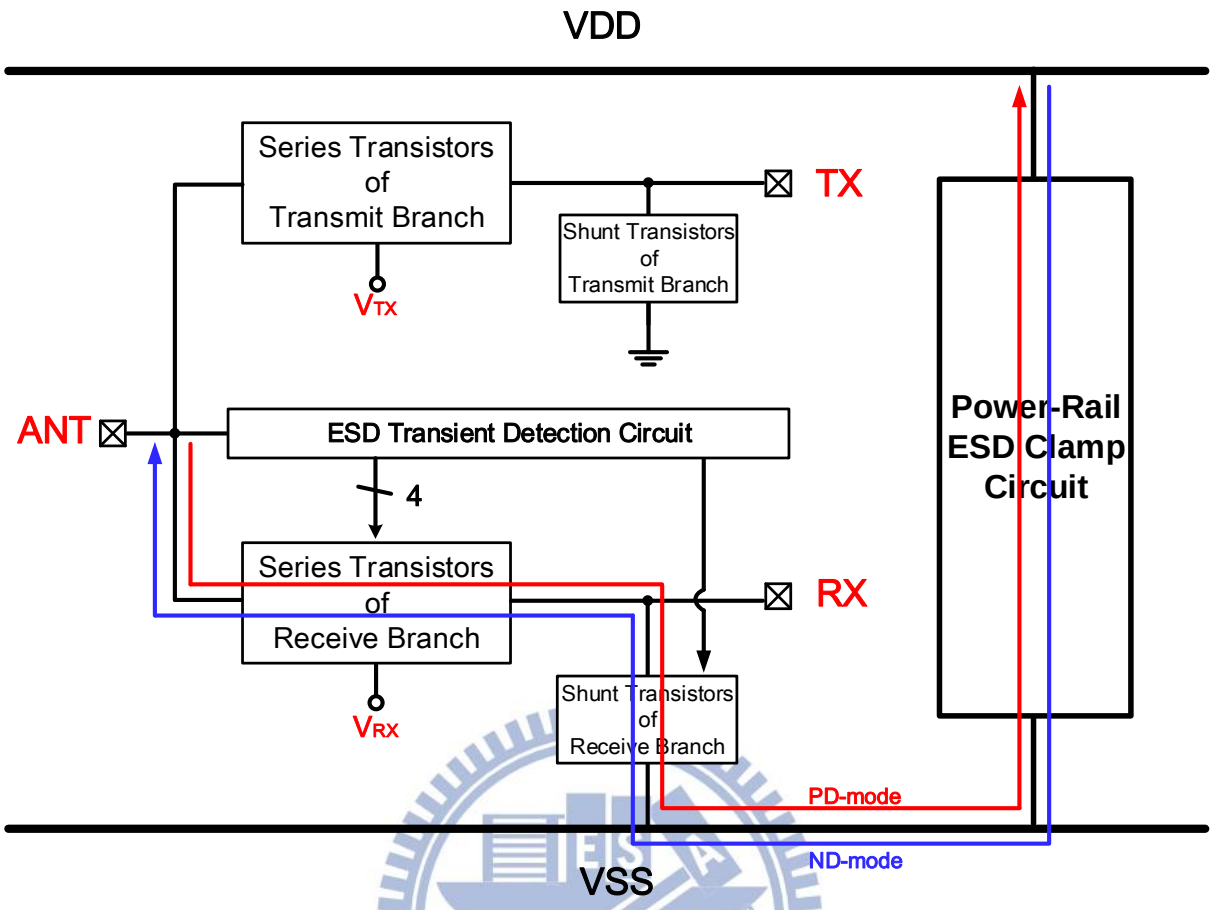


Fig. 3.11. The discharging path under PD-mode and ND-mode ESD stress.

ESD simulations of the type 1 ESD protection design and type 2 ESD protection design are done in the Spectre to check the RX transistors are turned on during the PS-mode ESD stress. The simulation setups are drawn in Fig. 3.12 and Fig. 3.13, which show the equivalent HBM and TLP stimulator for ESD zapping events on the ANT port. Simulation results of HBM 2kV and TLP 50V pulse are shown in Fig. 3.14 and Fig. 3.15, respectively. In Fig. 3.14, both type 1 and type 2 ESD protection design can pass the 2kV HBM test stress on ANT port and discharge the ESD current about 1.3A. However, in Fig. 3.14(a) and Fig. 3.15(a), type 2 ESD protection design owns a lower clamping voltage under the same zapping conditions. A lower clamping voltage indicates the ESD robustness of type 2 ESD protection design is better than the type 1 ESD protection design.

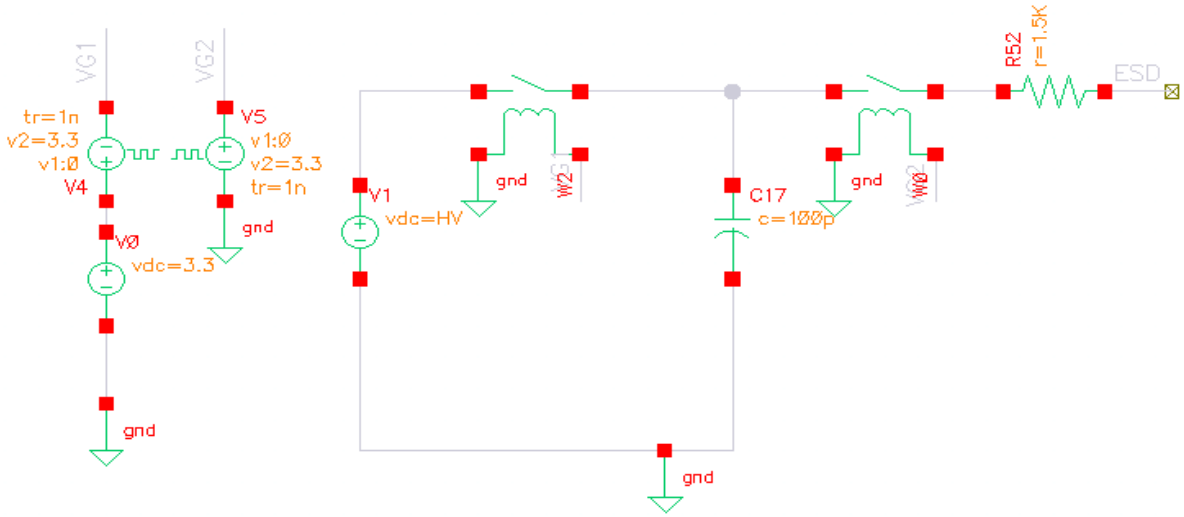


Fig. 3.12. A HBM stimulator setup for circuit simulation in Spectre.

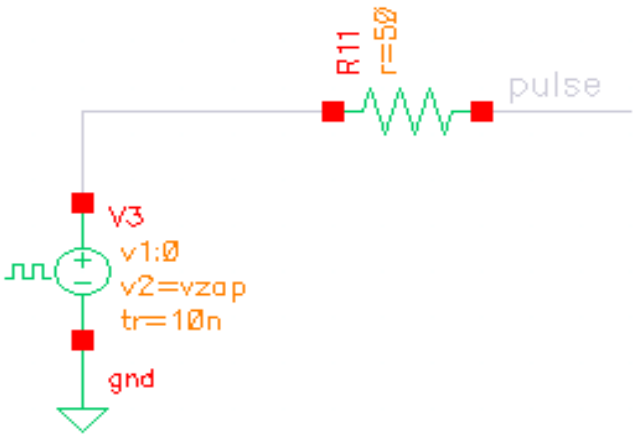
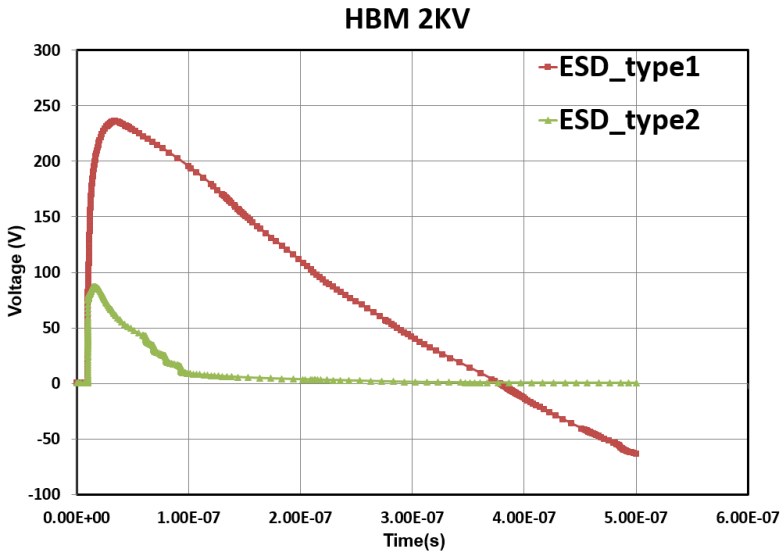
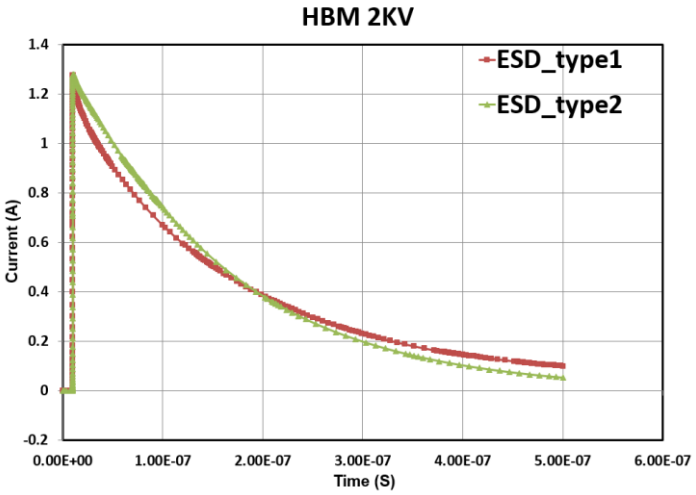


Fig. 3.13. A TLP stimulator setup for circuit simulation in Spectre.

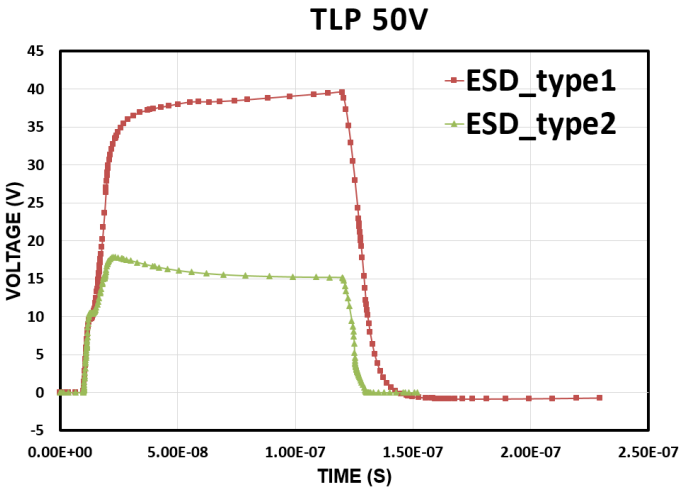


(a)

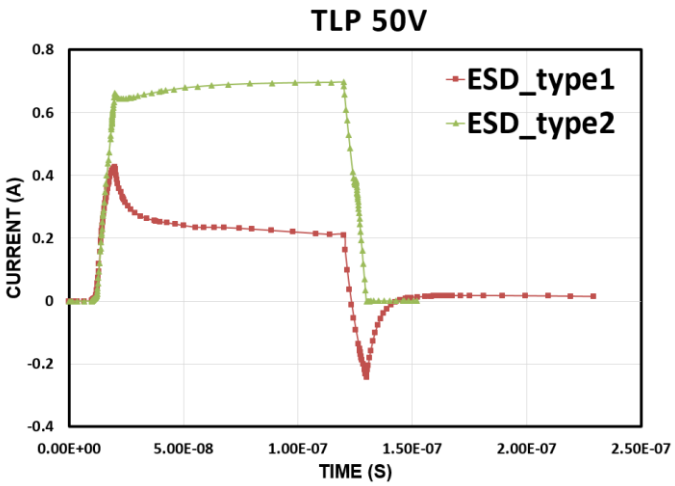


(b)

Fig. 3.14. Transient simulations of HBM 2kV testing results of (a) voltage and (b) current on ANT node of the high-power T/R switch with different ESD protection designs.



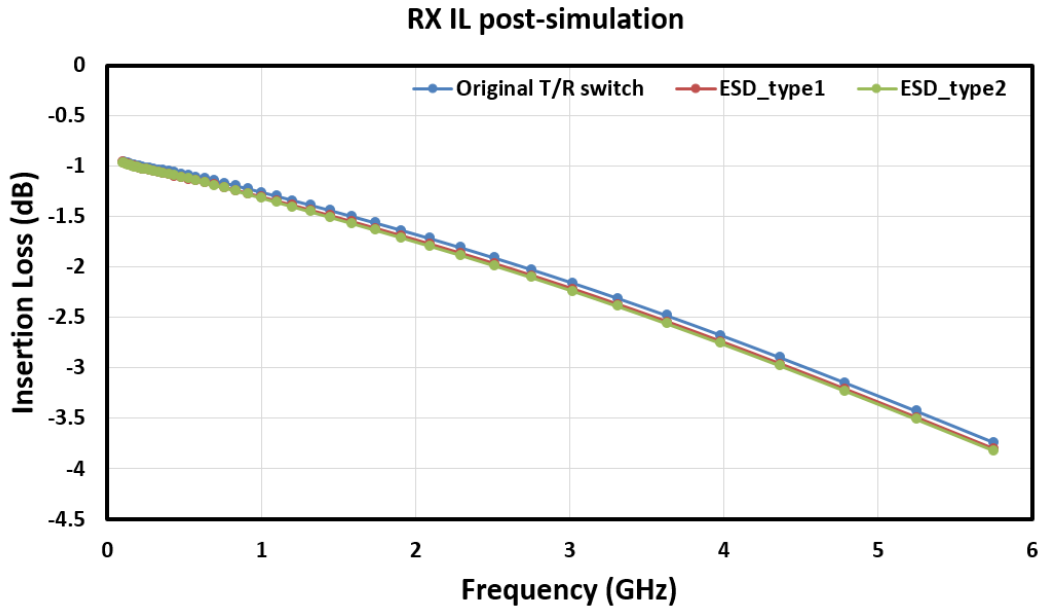
(a)



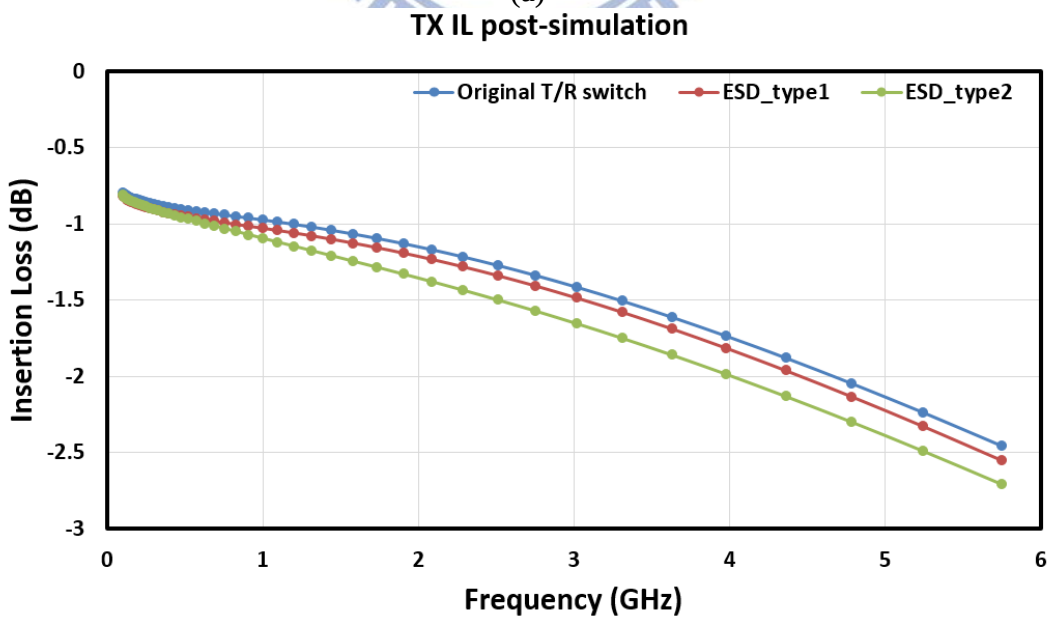
(b)

Fig. 3.15. Transient simulations of TLP 50V testing results of (a) voltage and (b) current on ANT node of the high-power T/R switch with different ESD protection designs.

The target frequency of the T/R switch is at 0.9GHz and 1.8GHz for GSM roaming agreement. The post-simulation of insertion loss in the original high-power T/R switch with type 1 and type 2 ESD protection design is presented in Fig. 3.16. In receive mode, the ESD protection slightly affect the insertion loss of the T/R switch. However, the insertion loss are degraded in transmit mode, especially in the type 2 ESD protection design. Table 3.1 summarized the simulation of S parameters and ESD stressing conditions.



(a)



(b)

Fig. 3.16. Comparison of insertion loss in (a) receive mode (b) transmit mode of high-power T/R switch with different ESD protection designs after post-simulations.

Table 3.1

Simulation results of high-power T/R switch with ESD protection designs.

Simulation Results @1.8GHz in RX/TX	Insertion Loss (dB)	Return Loss (dB)	Isolation (dB)	HBM 2kV Clamping Voltage (V)	TLP 50V Clamping Voltage (V)
Original T/R Switch	1.09/1.56	13.45/18.75	32.51/54.94		
T/R Switch with Type 1 ESD Design	1.16/1.61	13.69/18.3	32.57/54.46	235.7	40
T/R Switch with Type 2 ESD Design	1.29/1.63	13.73/18.43	32.53/52.79	91.25	18

Noise is also a concern in a RF transceiver circuit. Noise can be classified into three categories: shot noise, flicker noise, and thermal noise in analog integrated circuit. The shot noise is known as white noise, which is associated with a direct current flow and is present in diodes, MOS transistors, and bipolar junction transistors. The white noise is a purely random signal and unavoidable in communication systems. As for flicker noise, the spectrum of flicker noise has a $1/f$ frequency dependence and can be ignored in high frequencies operations. At last, the thermal noise always exists in resistors and is proportional to it.

Since the proposed ESD protection designs are equipped with several resistors, the noise source is from the thermal noise of the resistors. The substrate of the ESD designs will be noisy. The noise figure of the type 1 and type 2 ESD protection designs are worse than the original high-power T/R switch. Fig. 3.17 and Fig. 3.18 shows the simulated noise figure (NF) in RX and TX mode, respectively. For high-power T/R switch with type 2 ESD protection design, since the connection between body and source, the substrate noise can couple to the traveling signal in the channel more easily than type 1 ESD protection design. In general, the NF of the T/R switch with ESD protection designs are acceptable in the antenna switch modules.

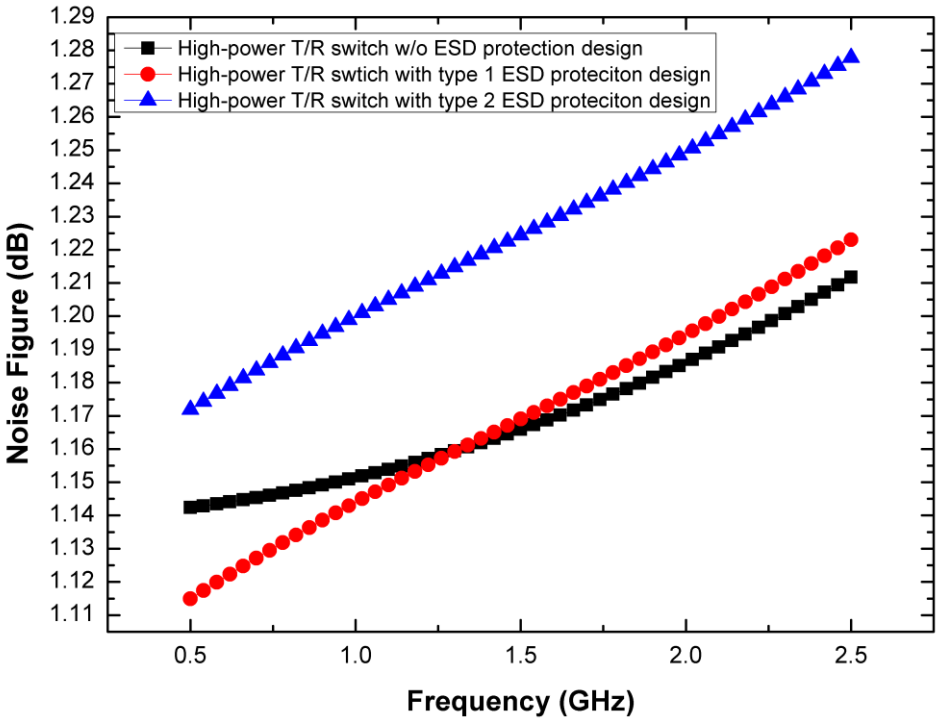


Fig. 3.17. The simulated noise figure in receive mode.

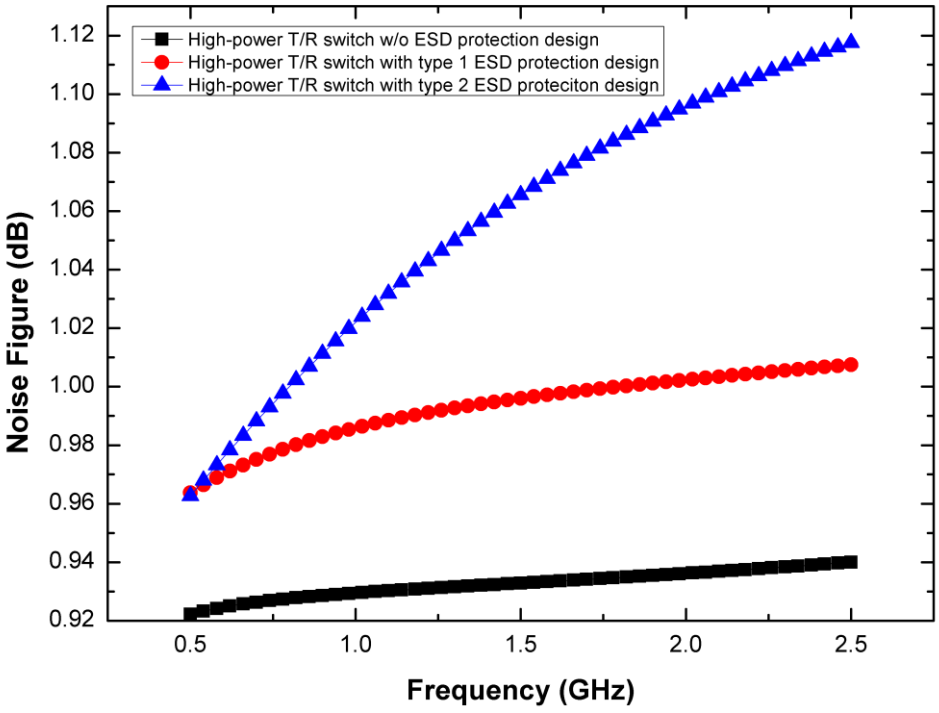
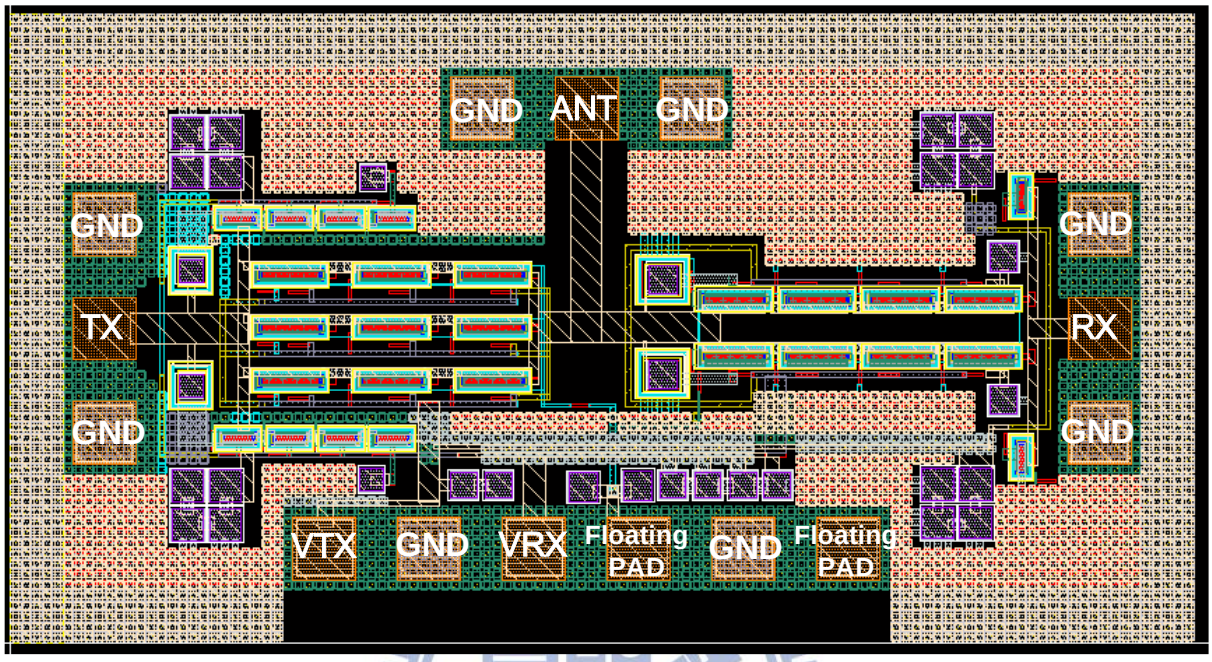
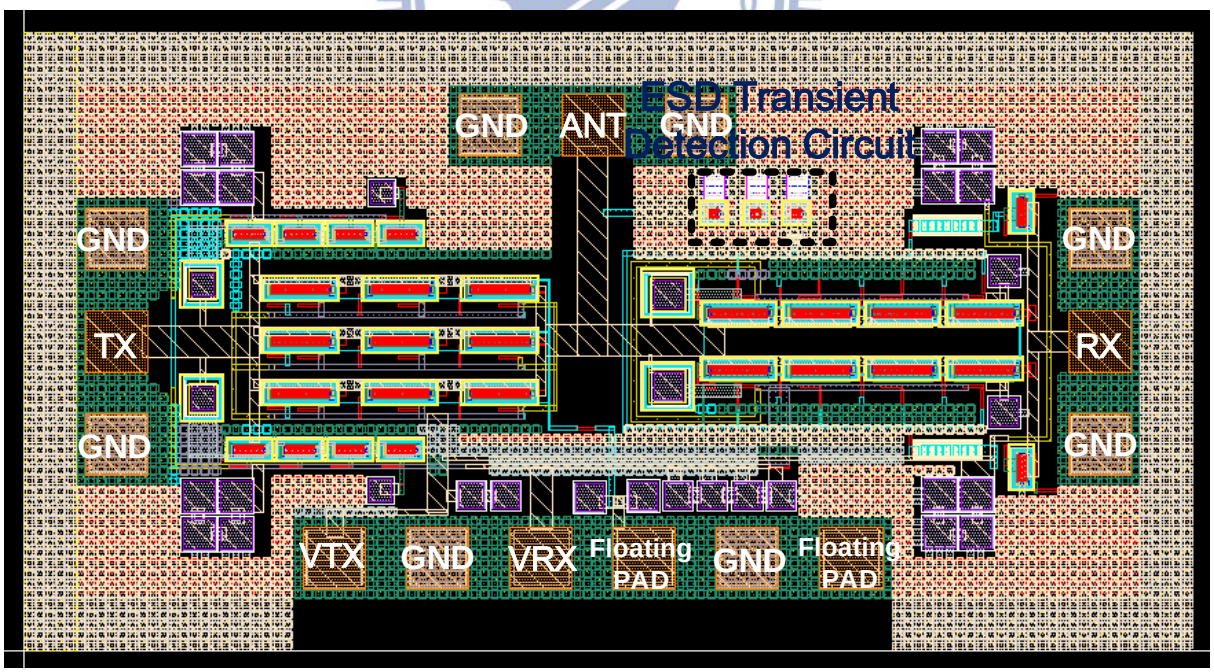


Fig. 3.18. The simulated noise figure in transmit mode.

The layout view of high-power T/R switch is shown in Fig. 3.19(a). The dimension of a single chip is size of 0.5mm*1mm. The type 1 ESD protection design is shown in Fig. 3.19(b), with ESD transient protection circuit located at the bottom-right of the ANT pad.



(a)



(b)

Fig. 3.19. Layout view of (a) high-power T/R switch and (b) high-power T/R switch with type 1 ESD protection design.

3.3 Experimental Results of High-Power T/R Switch with Proposed ESD Protection Designs

To verify the ESD efficiency of the proposed ESD design, HBM testing, TLP testing, and relative RF parameters of high-power T/R switch are measured and presented in this section. HBM ESD and TLP are tested using ETS Model-910 electrostatic discharge ESD stimulator (Fig. 3.20) and HED-T5000 (Fig. 3.21), respectively. The ETS Model-910 stimulator are equipped with 100pF and 1.5kohms, which is as same as the HBM equivalent circuit in Fig. 2.18. The RF parameters are measured in 20G on wafer probe station in CIC, Hsinchu. A photo of the fabricated chip is shown in Fig. 3.22, with total area of 1.5mm*1mm. Fig. 3.23 exhibits the photo of the high-power T/R switch under Cascade Infinity GSG probes.

Since the power of the signal generator (Agilent E8247C) can only reach about 20dBm, which is not sufficient for the P_{1dB} measurement of the high-power T/R switch. Thus, a 5W power amplifier (Mini Circuits ZHL-5W-422+) is employed to boost the input power of the T/R switch. Fig. 3.24 demonstrates the measurement environment of P_{1dB}.

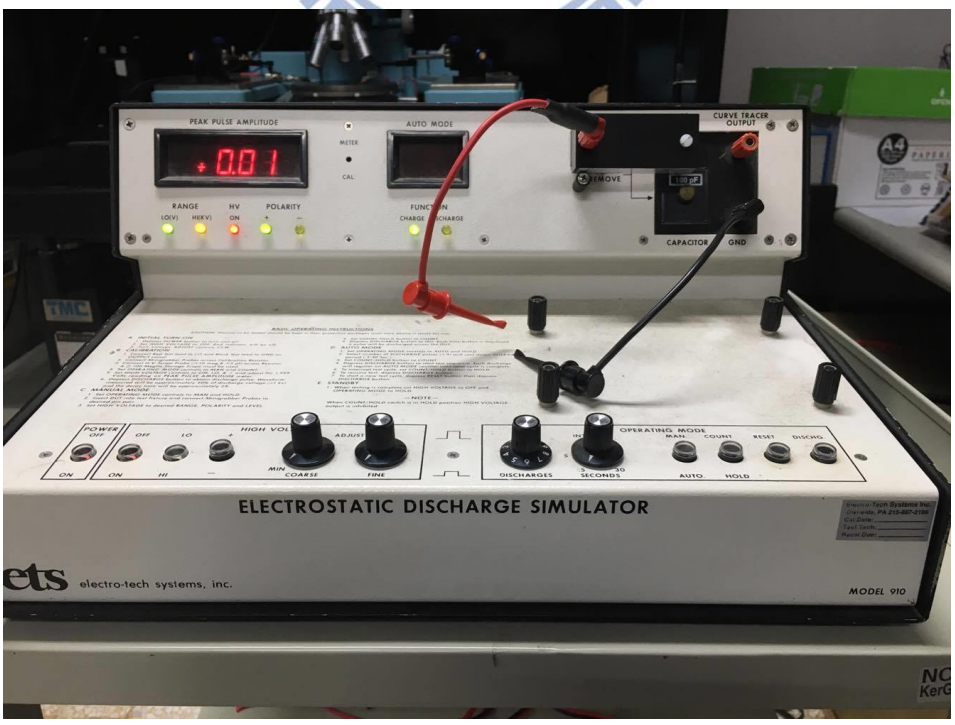


Fig. 3.20. ETS Model-910 ESD simulator.

Fig. 3.21. HED-5000 transmission line pulses system.

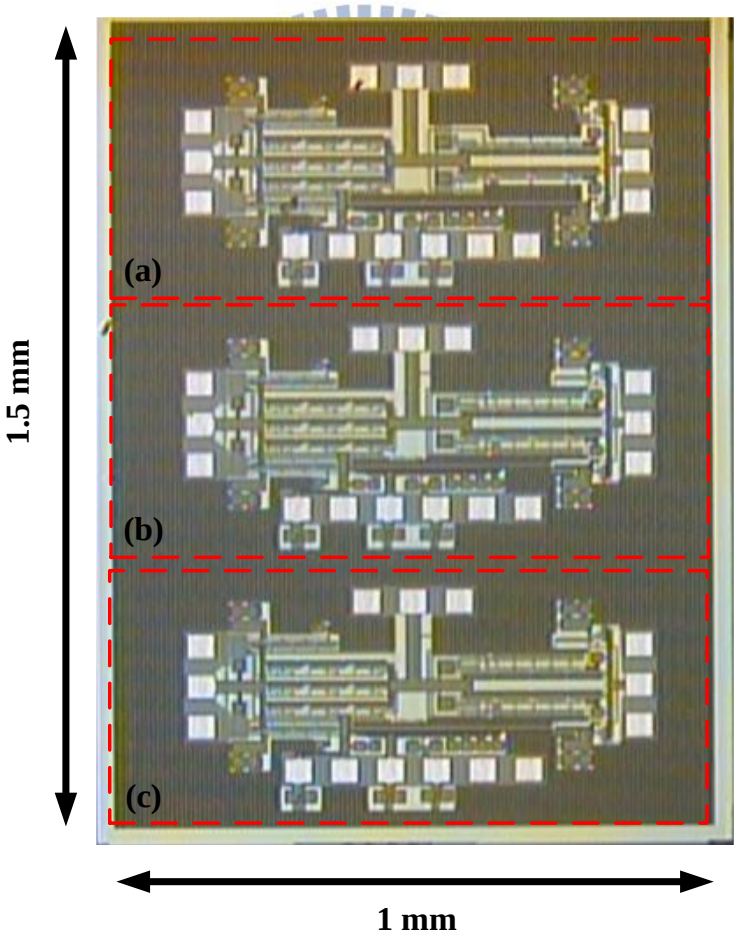


Fig. 3.22. Chip photo of (a) high-power T/R switch, (b) high-power T/R switch with type 1 ESD protection design, and (c) high-power T/R switch with type 2 ESD protection design.

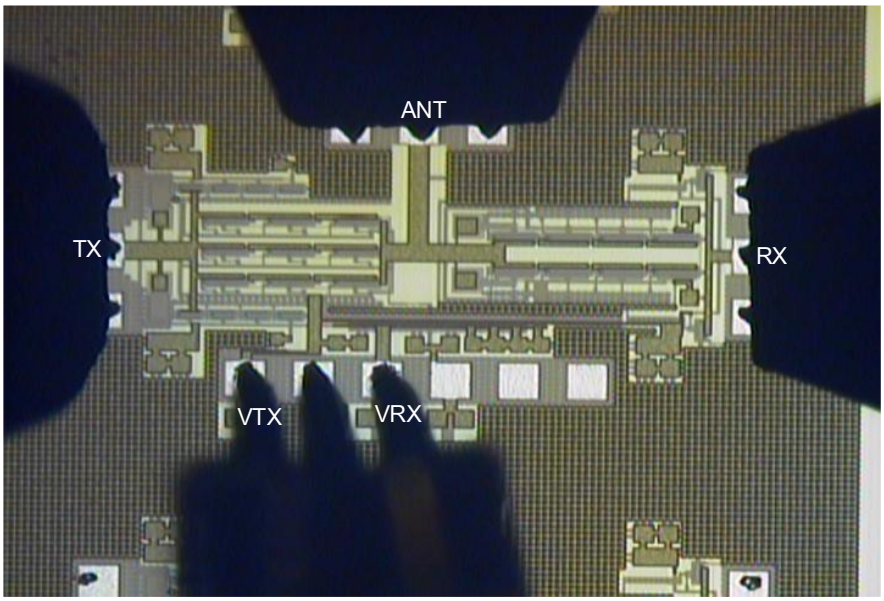


Fig. 3.23. High-power T/R switch with type 1 ESD protection design under 20GHz measurement using Infinity GSG probes.

Fig. 3.24. Measurement environment of P_{1dB}.

3.3.1 ESD Levels Measured with ESD HBM Tester and TLP System

Measured HBM ESD levels of ANT node of the high-power T/R switch are arranged in Table 3.2. The failure criteria is judged by the 10% shifts of the full-scale DCIV curve from -3.3V to 3.3V. The DCIV curve are checked in both positive and negative DC bias, in order not to miss any symptoms of the damaged spot. The anode and cathode of the DCIV measurement is at ANT port and GND, respectively.

Fig. 3.25 shows the DCIV curves of the high-power T/R switch without ESD protection design after 0.2kV PS-mode HBM stress. Fig. 3.26 is a closer look at 0V to 1.8V of Fig. 3.25. The PS-mode HBM level of the high-power T/R switch without ESD protection design is only 0.1kV. Fig. 3.27 presents the DCIV curves of high-power T/R switch with type 1 ESD protection after 4.25kV PS-mode HBM stress. Fig. 3.28 is a zoom-in of Fig. 3.27 at -3.3V to -0.6V. Fig. 3.29 shows the enlarged part at -0.3V to 0.6V of Fig. 3.27. The high-power T/R switch with type 1 ESD protection design can reach HBM level of 3.75kV. Fig. 3.30 shows the DCIV curves of high-power T/R switch with type 2 ESD protection design after 5kV PS-mode HBM stress. Fig. 3.31 shows the enlarged graph at -3.3V to -0.6V of Fig. 3.30. Fig. 3.32 shows the enlarged graph at 0V to 0.9V of Fig. 3.30. The ESD robustness of high-power T/R switch with type 2 ESD protection design can achieve 4.5kV.

In Fig. 3.33, the DCIV curves of high-power T/R switch without ESD protection design after 6kV NS-mode HBM stress are exhibited. Fig. 3.34 shows the enlarged part at 0V to 2.1V of Fig. 3.33. Fig. 3.35 shows DCIV curves of the high-power T/R switch with type 1 ESD protection design after 6kV NS-mode HBM stress. Enlarged view at 0V to 0.9V of Fig. 3.35 is shown in Fig. 3.36. Fig. 3.37 shows DCIV curves of the high-power T/R switch with type 2 ESD protection design after 7kV NS-mode HBM stress. The curves from -1V to 3.3V in Fig. 3.37 are overlapped perfectly. Since the positive DCIV curves still remain the same, it can conclude that the ESD robustness of the circuit will be misjudged if the unilateral DCIV curves is measured only. The NS-mode of the type 2 ESD protection design is better than the type 1

ESD protection design. It is speculated that the body to source connection in the type 2 ESD protection design makes the NMOS transistors in RX branch act like p-n diodes in NS-mode direction and thus strengthens the robustness of NS-mode ESD stressing.

The TLP characteristics of the type 1 and type 2 ESD protection design are shown in Fig. 3.38. The leakage current of both the high-power T/R switch with type 1 and type 2 ESD protection is about ~20nA when 0.5V apply on the ANT node. The failure current I_{t2} of type 1 and type 2 ESD protection design is 2A and 2.5A, respectively. In addition, the trigger voltage of the type 1 ESD protection design is lower than the type 2 ESD protection design, too. The type 2 ESD protection design can discharge the ESD current to ground earlier than the type 1 ESD protection design. Overall, the robustness of type 2 ESD protection design is better than the type 1 ESD protection design.

The measured V-t and I-t curves of type 1 and type 2 ESD protection design before failure point are shown in Fig. 3.39(a) and Fig. 3.39(b). The high voltage pulse can be pulled down immediately to avoid the breakdown issues of the high-power T/R switch.

Table 3.2

Measured HBM ESD levels of high-power T/R switch by ETS HBM simulator.

HBM tests on ANT node	PS-mode	NS-mode
High-power T/R switch w/o ESD protection design	0.1kV	5kV
High-power T/R switch with type 1 ESD protection design	3.75kV	5kV
High-power T/R switch with type 2 ESD protection design	4.5kV	6kV

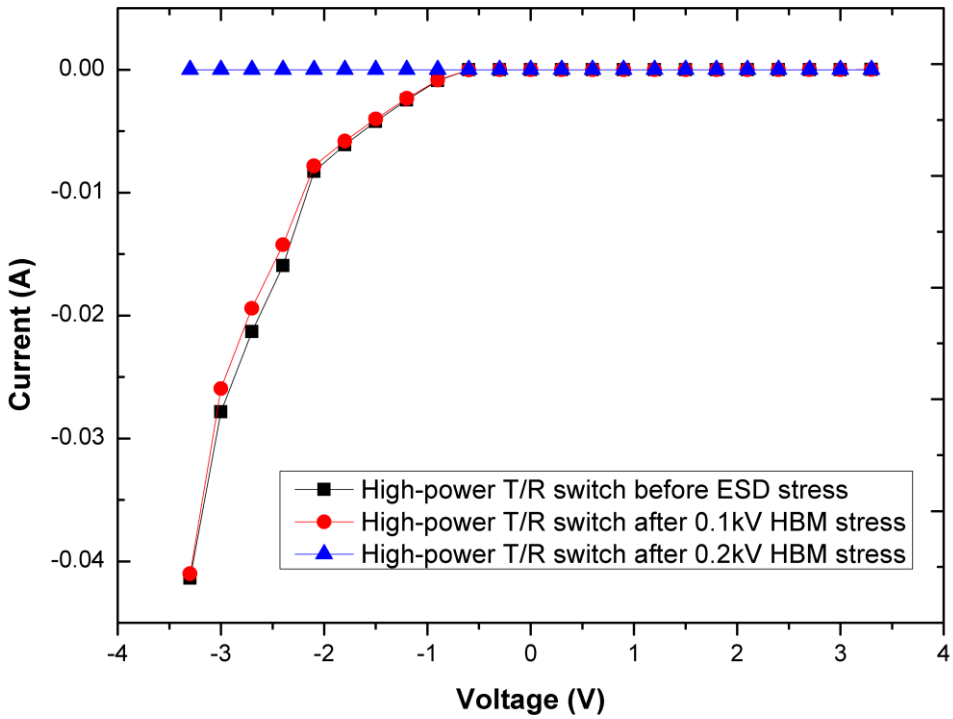


Fig. 3.25. DCIV curves of high-power T/R switch after 0.2kV PS-mode HBM stress.

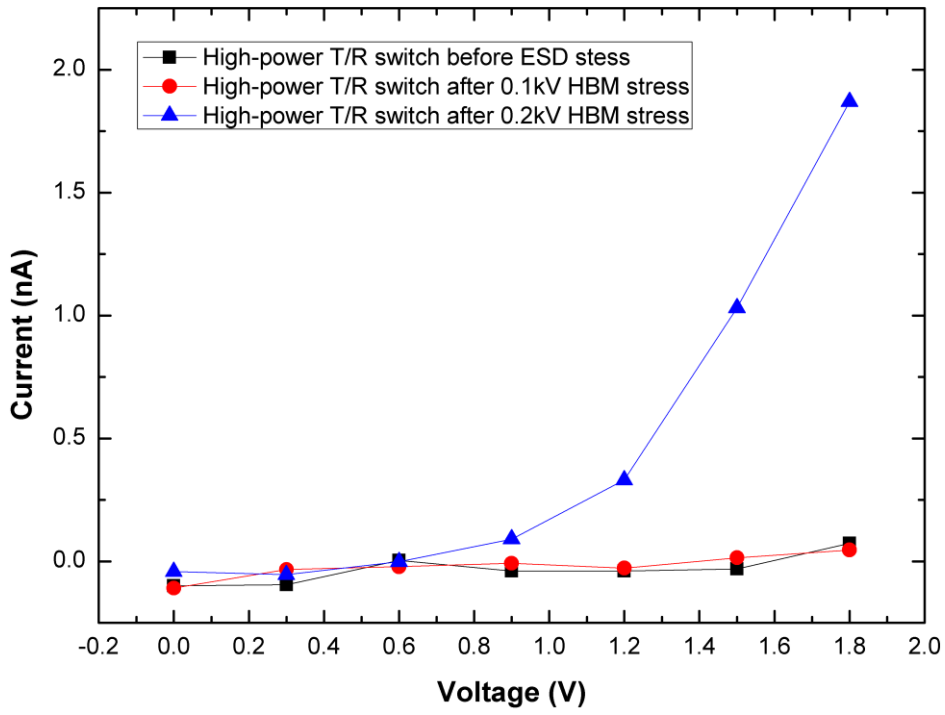


Fig. 3.26. Enlarged graph of 0V to 1.8V from Fig. 3.25.

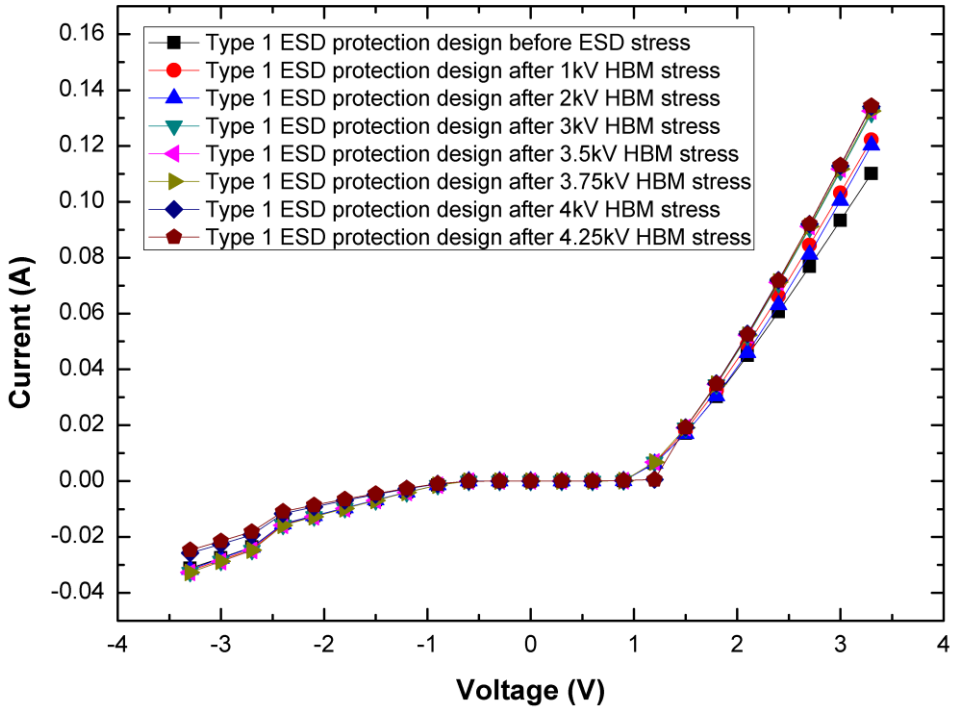


Fig. 3.27. DCIV curves of type 1 ESD protection design after 4.25kV PS-mode HBM stress.

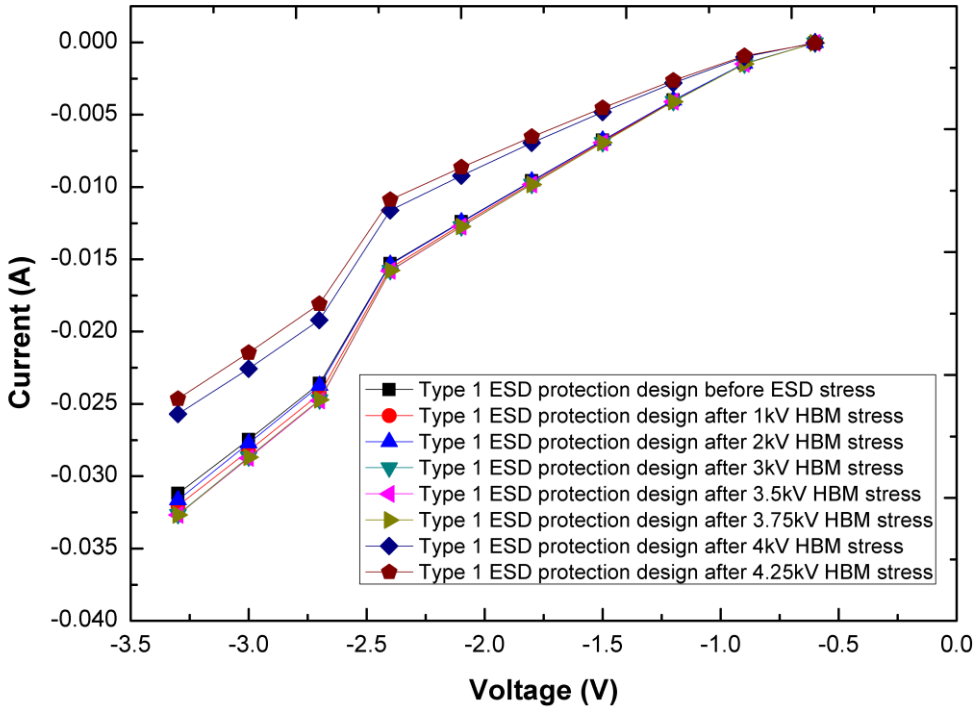


Fig. 3.28. Enlarged graph of -3.3V to -0.6V from Fig. 3.27.

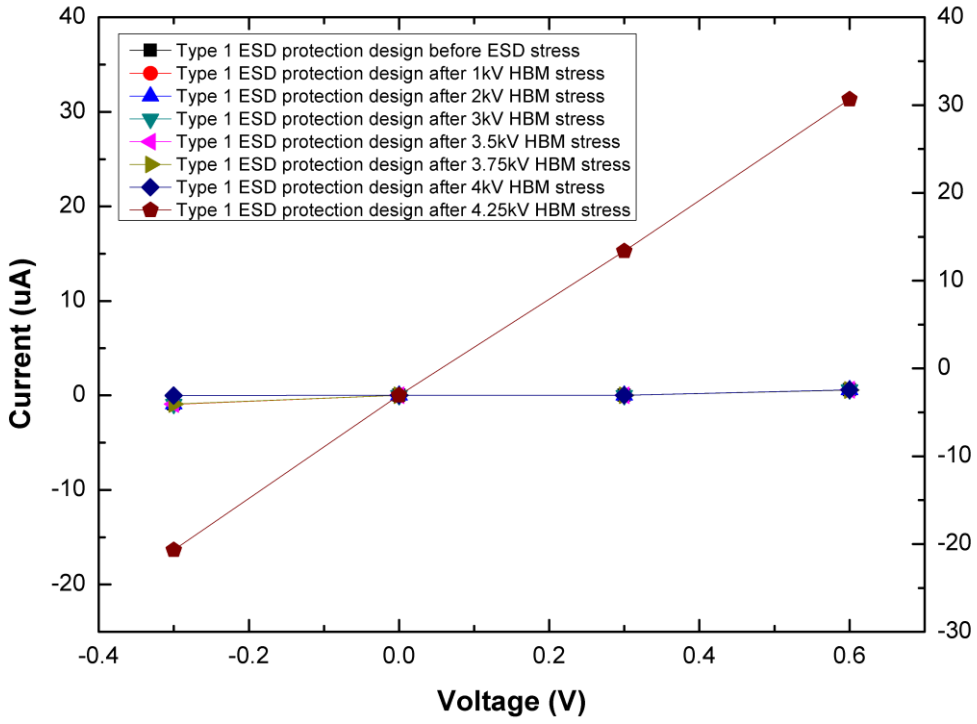


Fig. 3.29. Enlarged graph of -0.3V to 0.6V from Fig. 3.27.

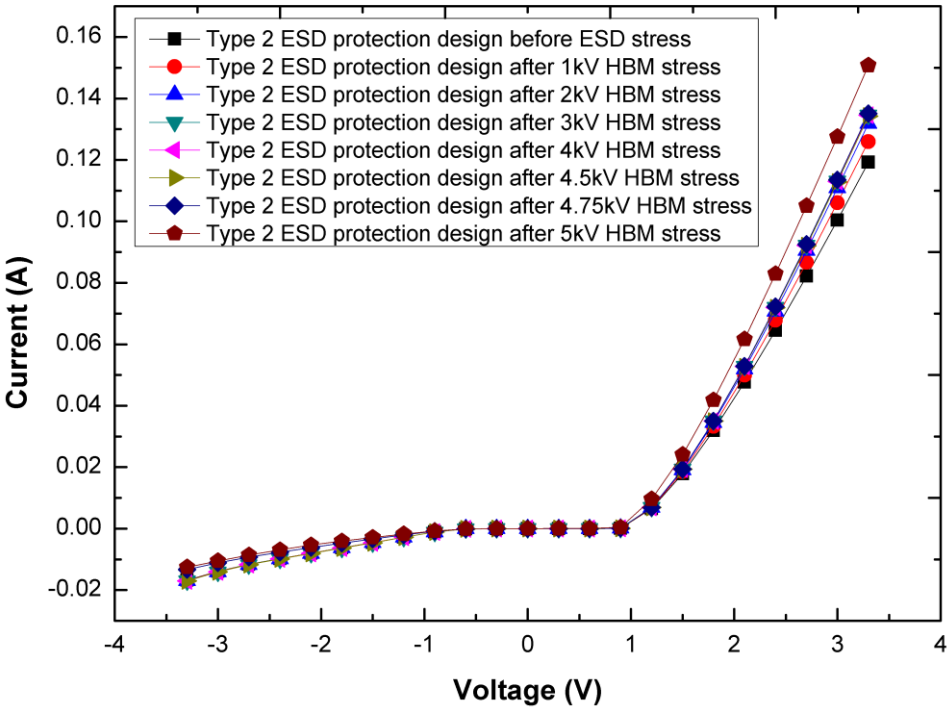


Fig. 3.30. DCIV curves of type 2 ESD protection design after 5kV PS-mode HBM stress.

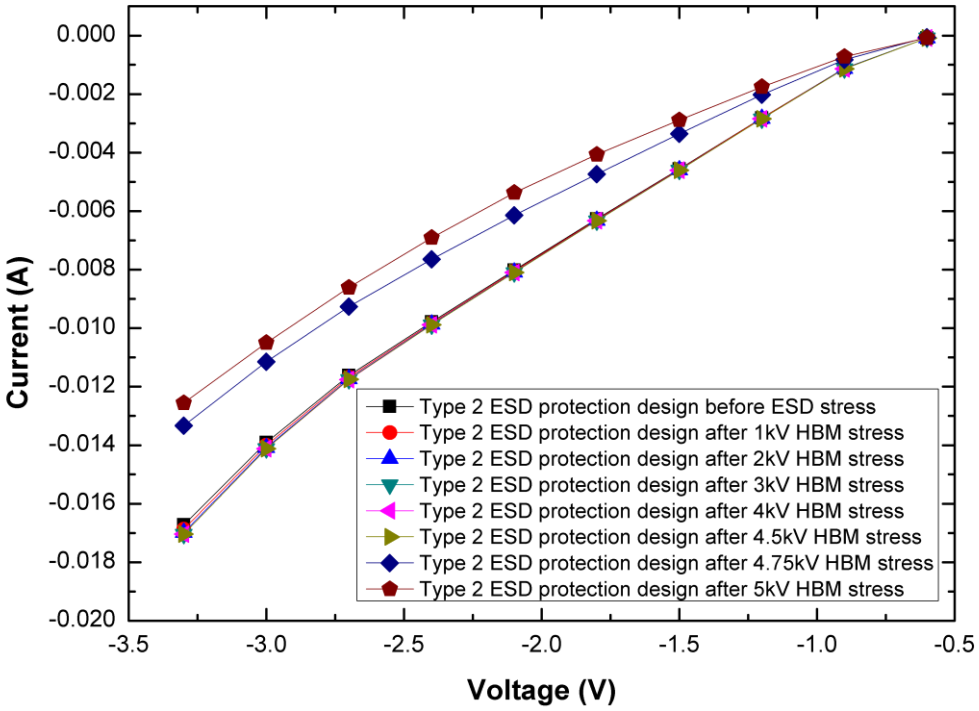


Fig. 3.31. Enlarged graph of -3.3V to -0.6V from Fig. 3.30.

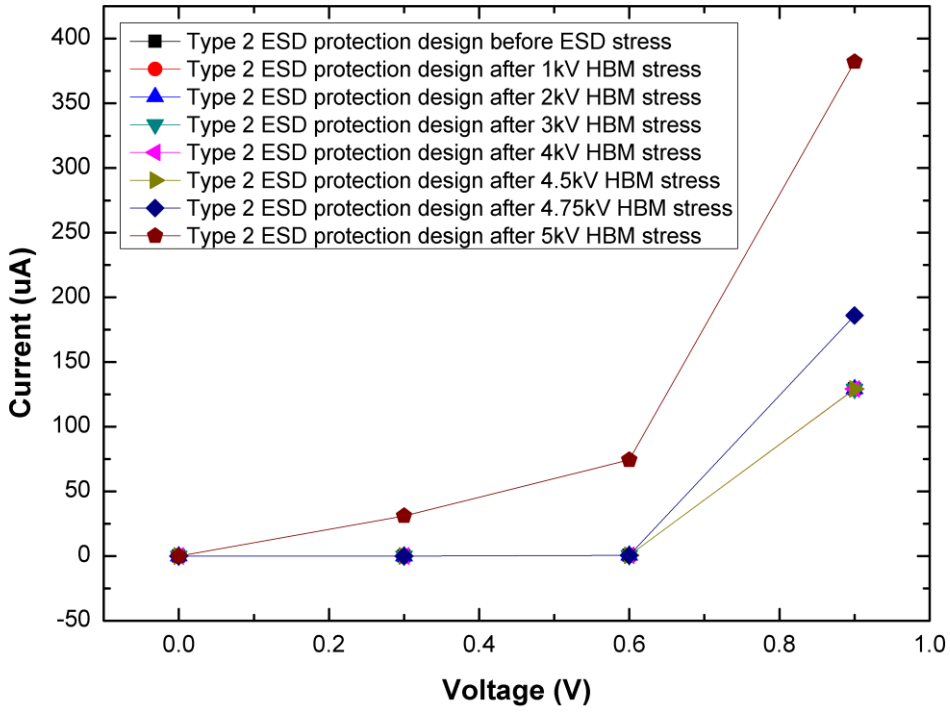


Fig. 3.32. Enlarged graph of 0V to 0.9V from Fig. 3.30.

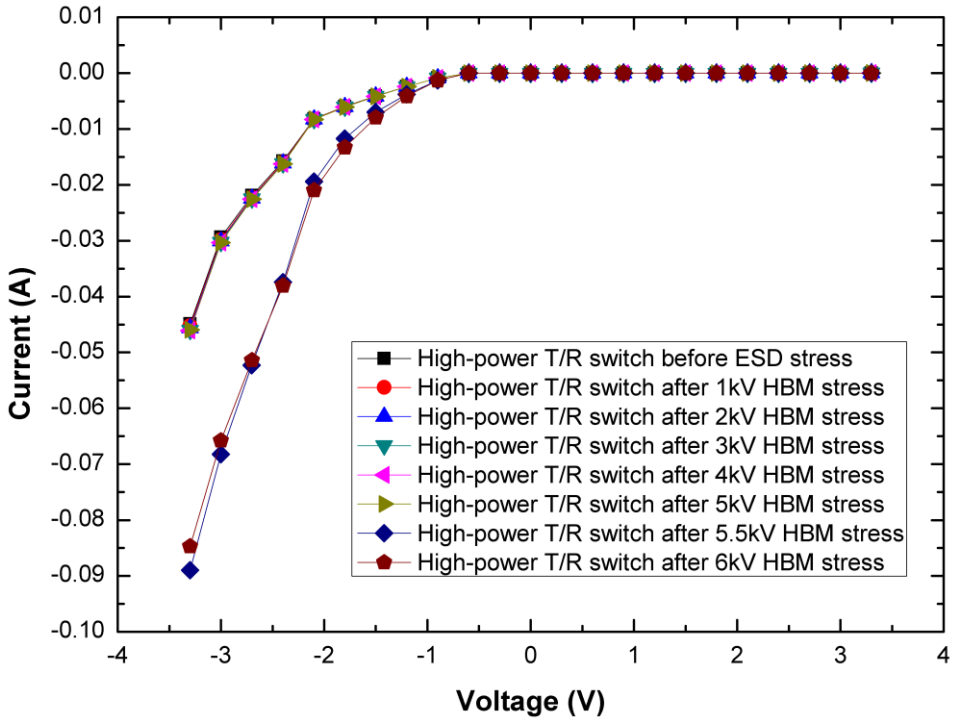


Fig. 3.33. DCIV curves of high-power T/R switch after 6kV NS-mode HBM stress.

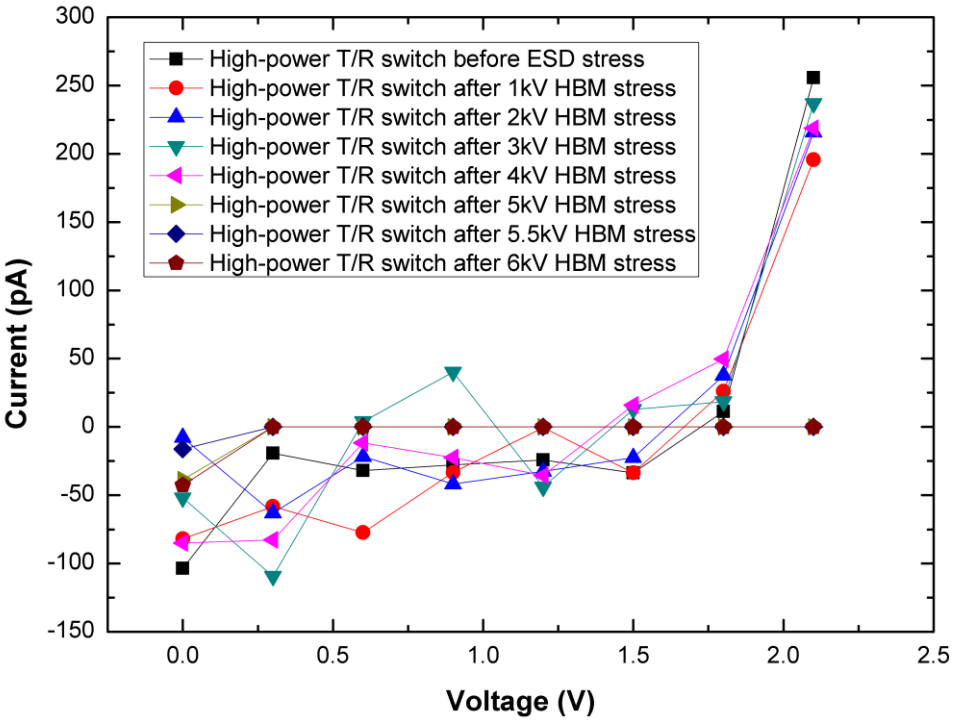


Fig. 3.34. Enlarged graph of 0V to 2.1V from Fig. 3.33.

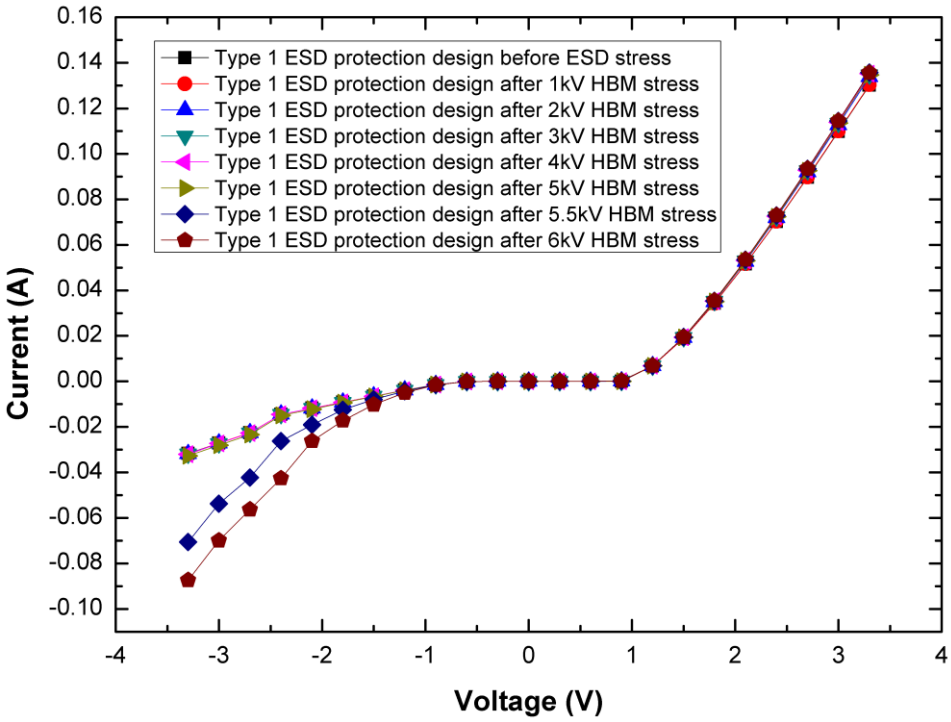


Fig. 3.35. DCIV curves of type 1 ESD protection design after 6kV NS-mode HBM stress.

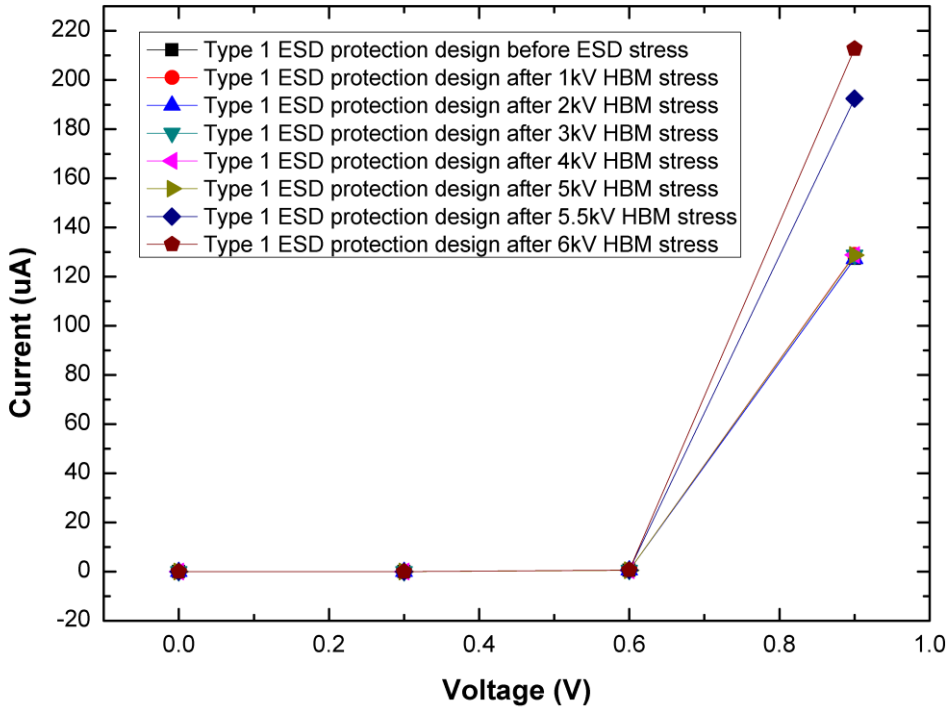


Fig. 3.36. Enlarged graph of 0V to 0.9V from Fig. 3.35.

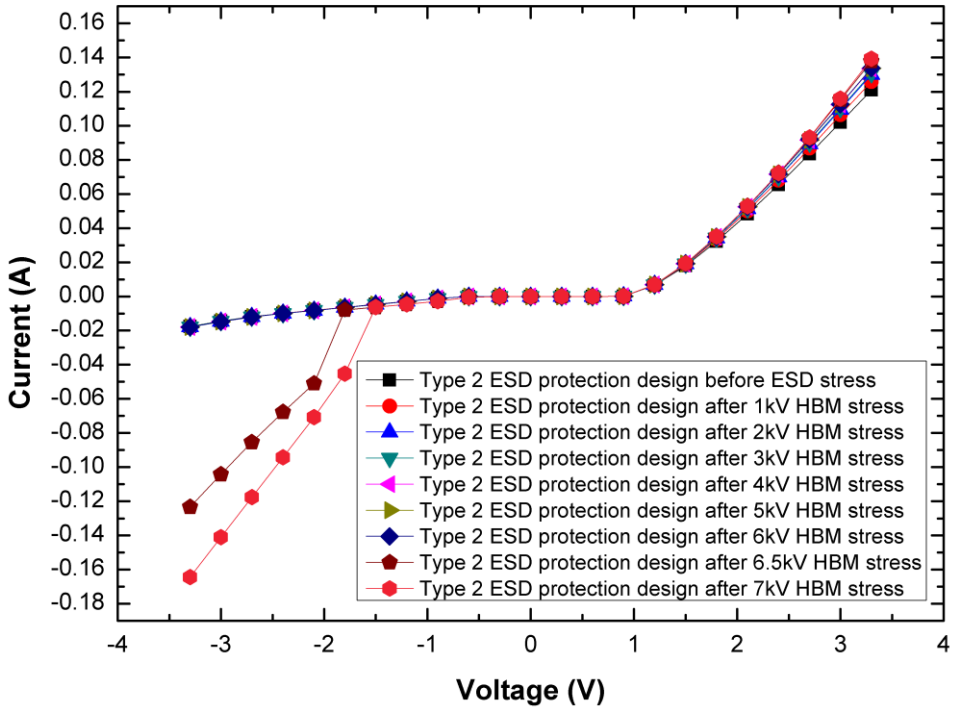


Fig. 3.37. DCIV curves of type 2 ESD protection design after 7kV NS-mode HBM stress.

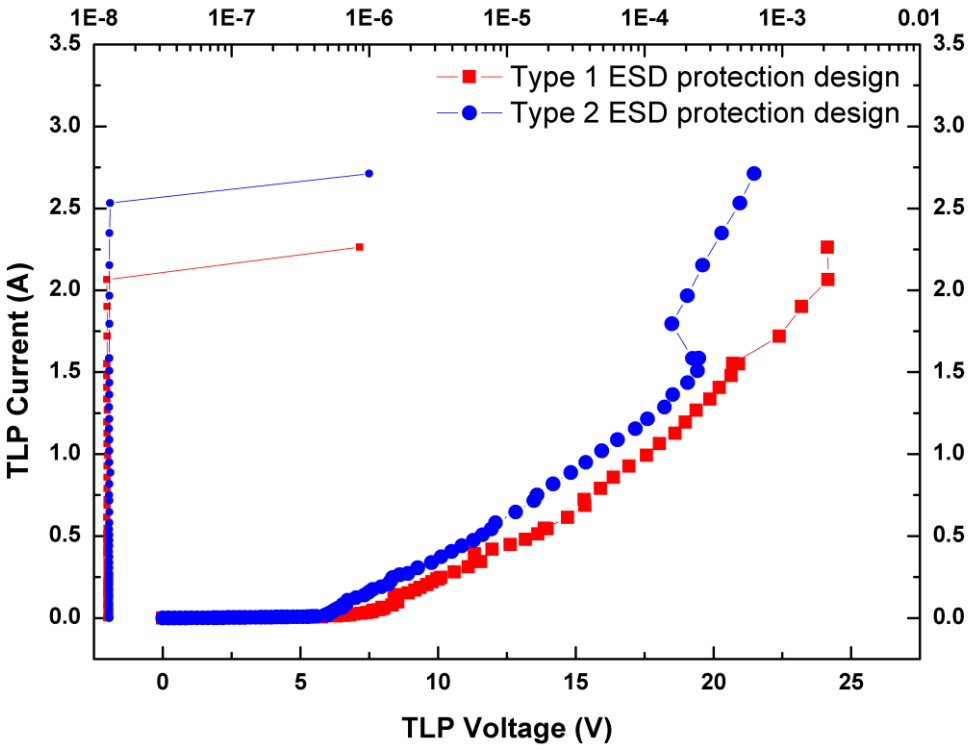
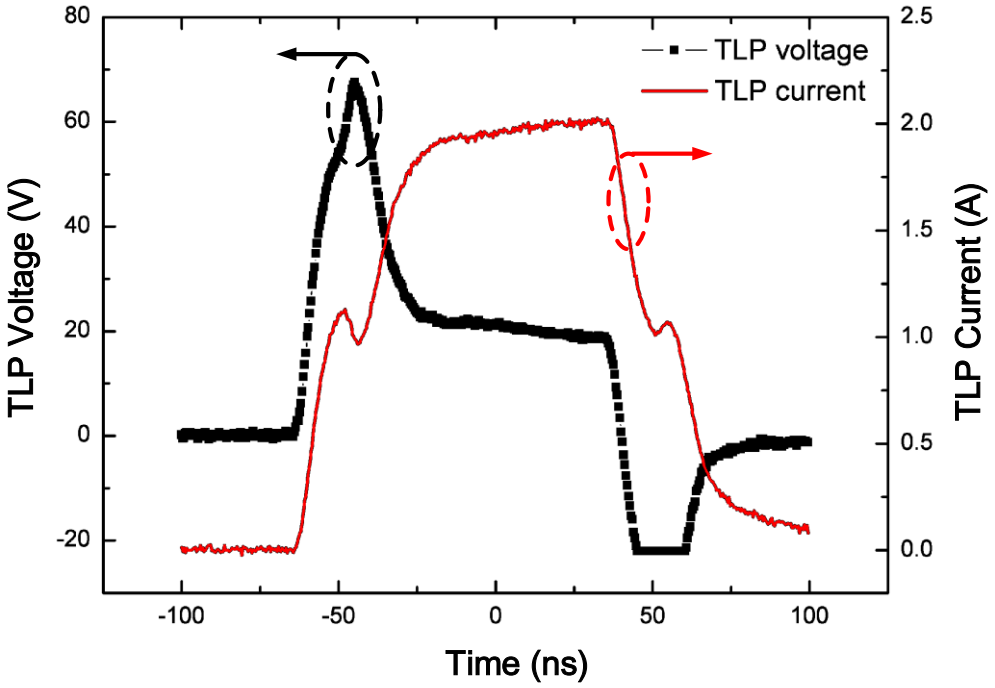
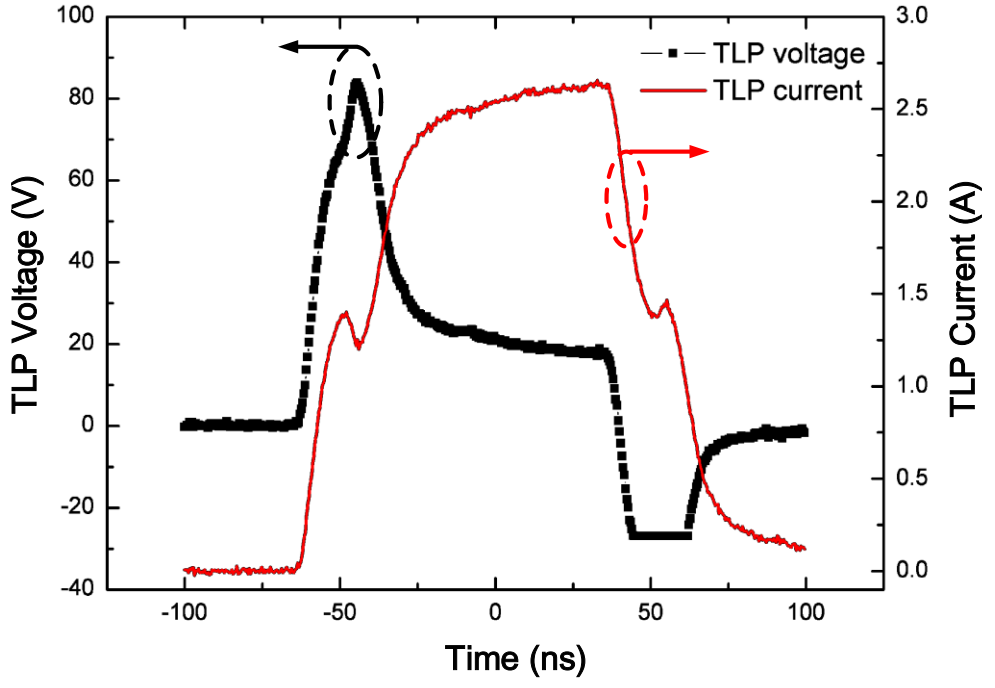


Fig. 3.38. Measured TLP characteristics of type 1 and type 2 ESD protection design.



(a)



(b)

Fig. 3.39. The measured point V-t and I-t curves before failure of (a) high-power T/R switch with type 1 ESD protection design and (b) high-power T/R switch with type 2 ESD protection design.

3.3.2 Comparison of RF Performances Before ESD Stress

The interested frequency of GSM is at 0.9GHz and 1.8GHz. The measured input return loss, insertion loss, isolation, and P_{1dB} are summarized and listed in Table 3.3 and Table 3.4.

The RX mode insertion loss of the high-power T/R switch without ESD protection design is 1.98dB at 0.9GHz and 2.83dB at 1.8GHz. On the other hand, the TX mode insertion loss is 1.81dB at 0.9GHz and 2.58dB at 1.8GHz. As for type 1 and type 2 high-power T/R switch with ESD protection designs, the insertion loss degrades about 0.2dB ~ 0.5dB. Fig. 3.40 and Fig. 3.41 show the insertion loss in RX mode and TX mode, respectively. The measured insertion loss is worse than post-layout simulation. It is considered that the N-Well of the p-cell are not connected to the VDD node, and thus the parameters of RFNMOS are changed.

Fig. 3.42 and Fig 3.43 show the 1dB input compression point P_{1dB} of the T/R switches. The high-power T/R switch without ESD protection design can reach 25.6dBm under 0.9GHz measurement and 28.6dBm under 1.8GHz measurement, respectively. The P_{1dB} at 1.8GHz is higher than the one at 0.9GHz. It is because in higher frequencies, the gate resistance of the off-state transistors can block the RF signal more effectively so that the DC bias of the off-state transistors will be less affected. However, the P_{1dB} at 1.8GHz of the type 1 and type 2 high-power T/R switch with ESD protection design is only 23.4dBm and 22.7dBm, respectively.

The RX mode and TX mode input return loss of the T/R switches are shown in Fig. 3.44 and Fig. 3.45. The both return loss in RX and TX of the proposed ESD protection designs are not far from the original high-power T/R switch.

At last, the isolation of RX mode and TX mode of the switches is shown in Fig. 3.46 and Fig. 3.47. The isolation of the type 1 ESD protection design is not degraded by the ESD detection circuit. However, the TX mode isolation of the type 2 ESD protection design is worse than the original T/R switch since the transmitting signal are more likely to leak to the RX node due to the source-body connection of the RX transistors.

Table 3.3

RF parameters of the high-power T/R switches measured at 0.9GHz.

Measurements at 0.9GHz (TX/RX)	Return Loss (dB)	Insertion Loss (dB)	Isolation (dB)	P_{1dB} (dBm)
High-power T/R switch without ESD protection design	12.78/12.88	1.81/1.98	51.42/37.86	25.6
High-power T/R switch with type 1 ESD protection design	12.37/12.97	1.86/2.33	51.51/39.52	22.5
High-power T/R switch with type 2 ESD protection design	12.18/12.53	1.84/2.42	47.32/38.99	21.5

Table 3.4

RF parameters of the high-power T/R switches measured at 1.8GHz.

Measurements at 1.8GHz (TX/RX)	Return Loss (dB)	Insertion Loss (dB)	Isolation (dB)	P_{1dB} (dBm)
High-power T/R switch without ESD protection design	9.00/9.53	2.58/2.83	44.73/31.00	28.6
High-power T/R switch with type 1 ESD protection design	9.16/9.90	2.66/3.16	44.82/33.40	23.4
High-power T/R switch with type 2 ESD protection design	8.85/9.51	2.69/3.20	41.67/32.83	22.7

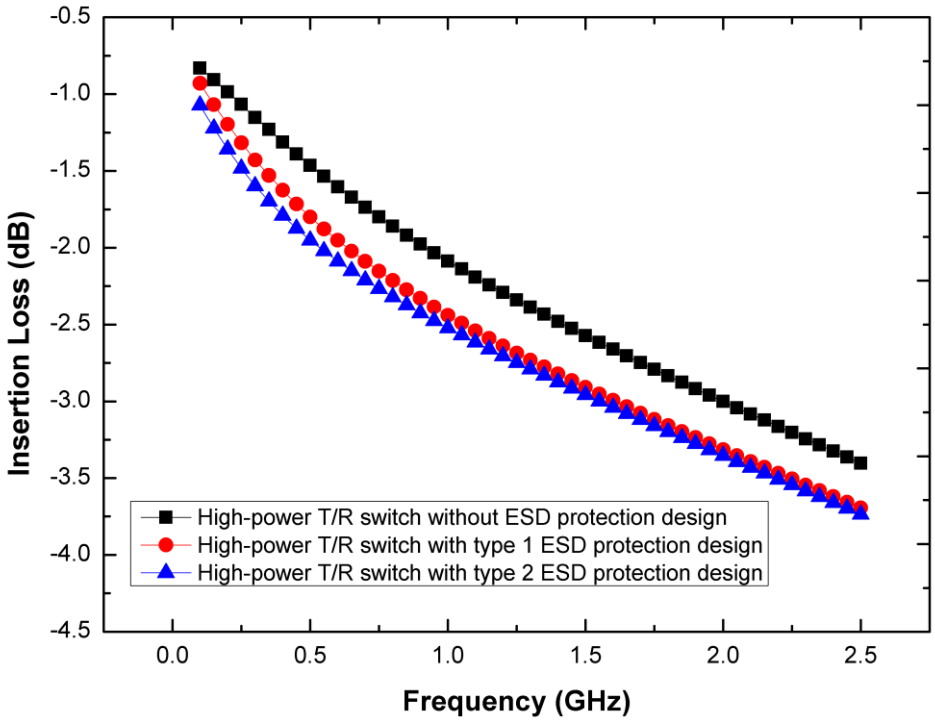


Fig. 3.40. Insertion loss in RX mode of high-power T/R switches.

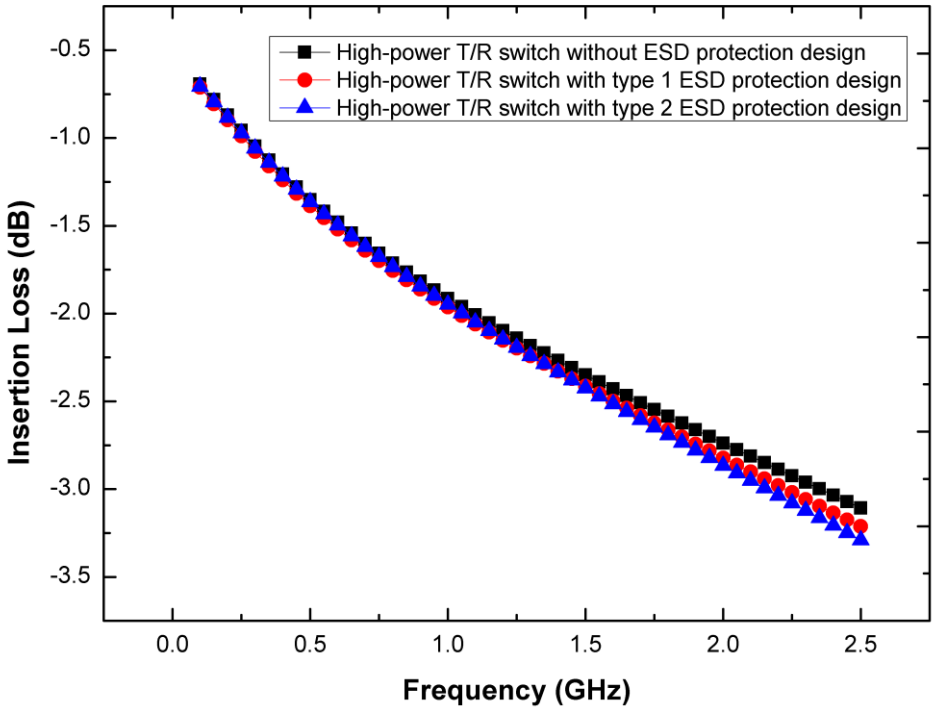


Fig. 3.41. Insertion loss in TX mode of high-power T/R switches.

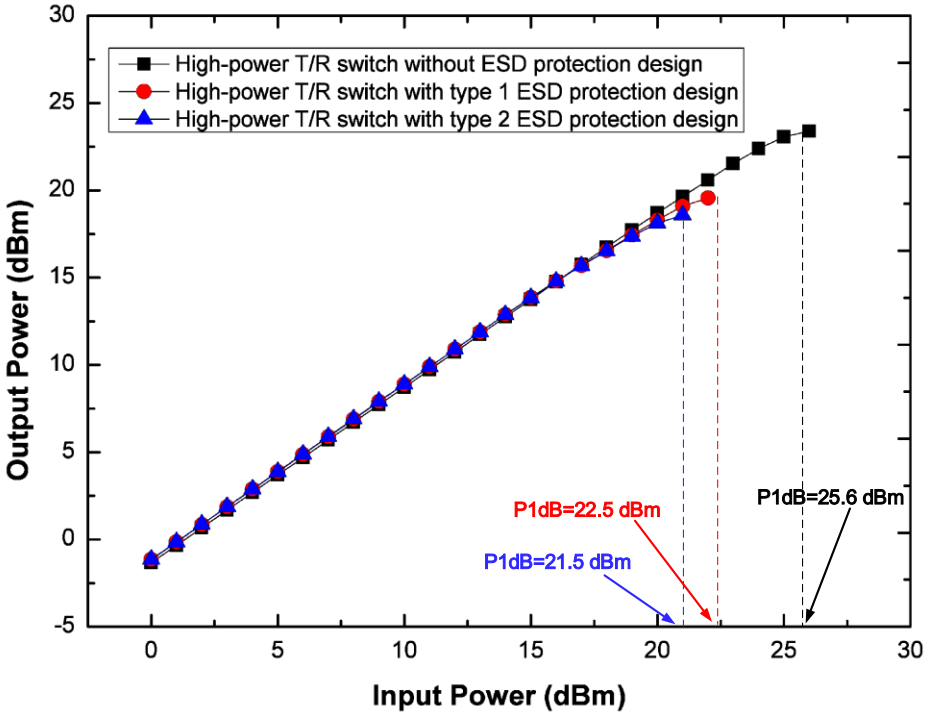


Fig. 3.42. P_{1dB} of high-power T/R switches at 0.9GHz.

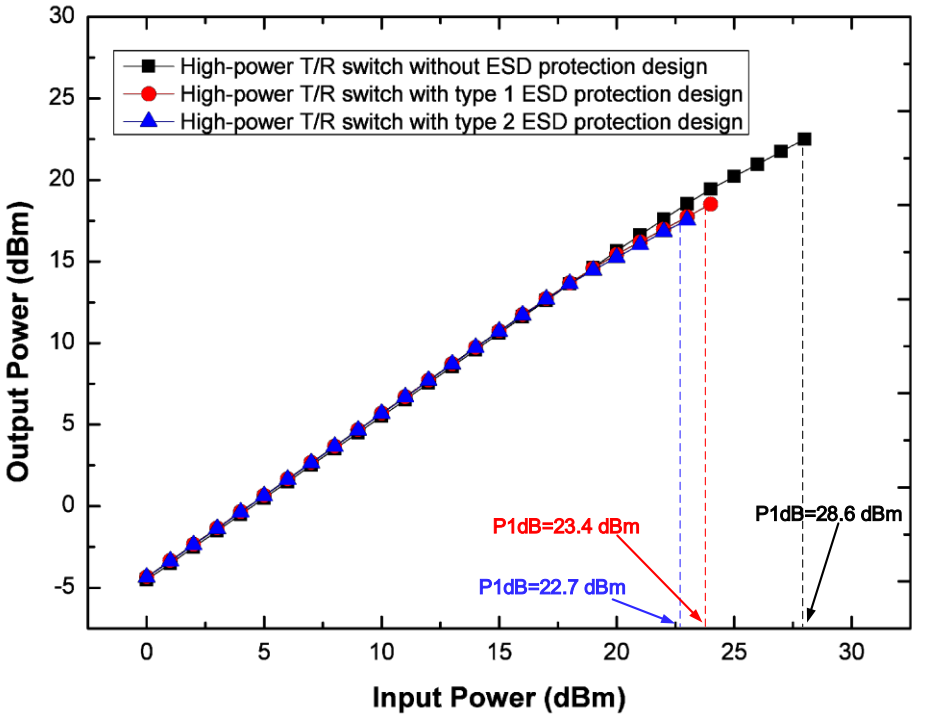


Fig. 3.43. P_{1dB} of high-power T/R switches at 1.8GHz.

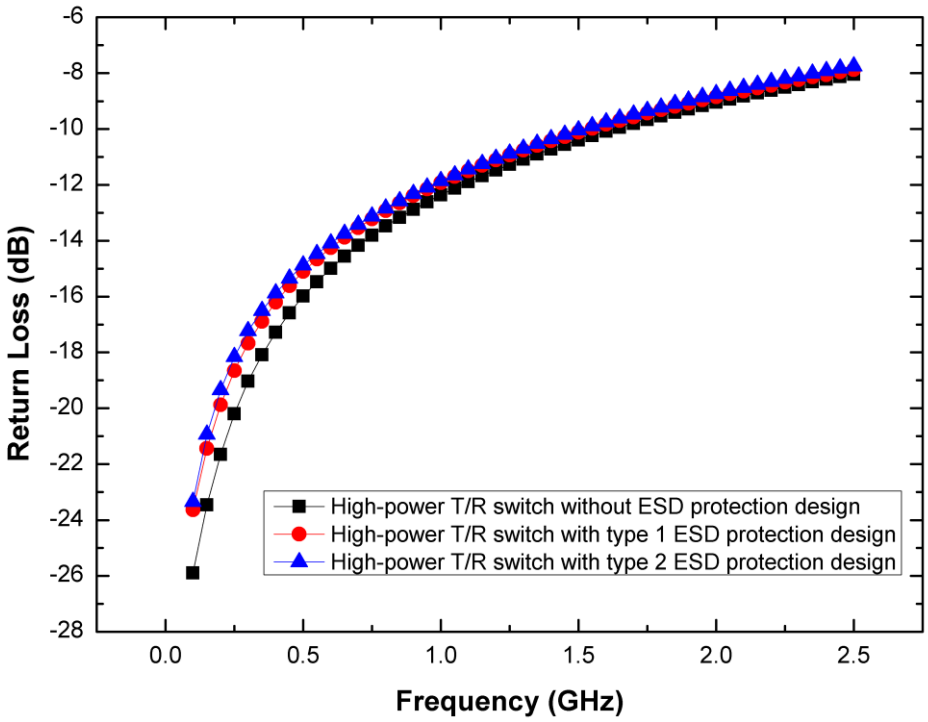


Fig. 3.44. Return loss in RX mode of high-power T/R switches.

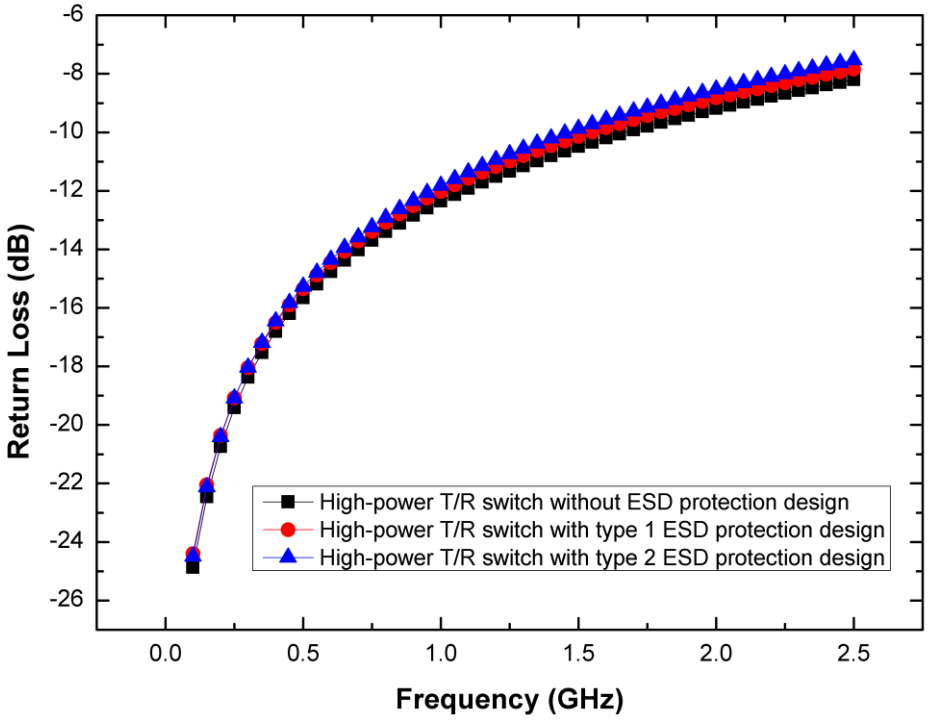


Fig. 3.45. Return loss in TX mode of high-power T/R switches.

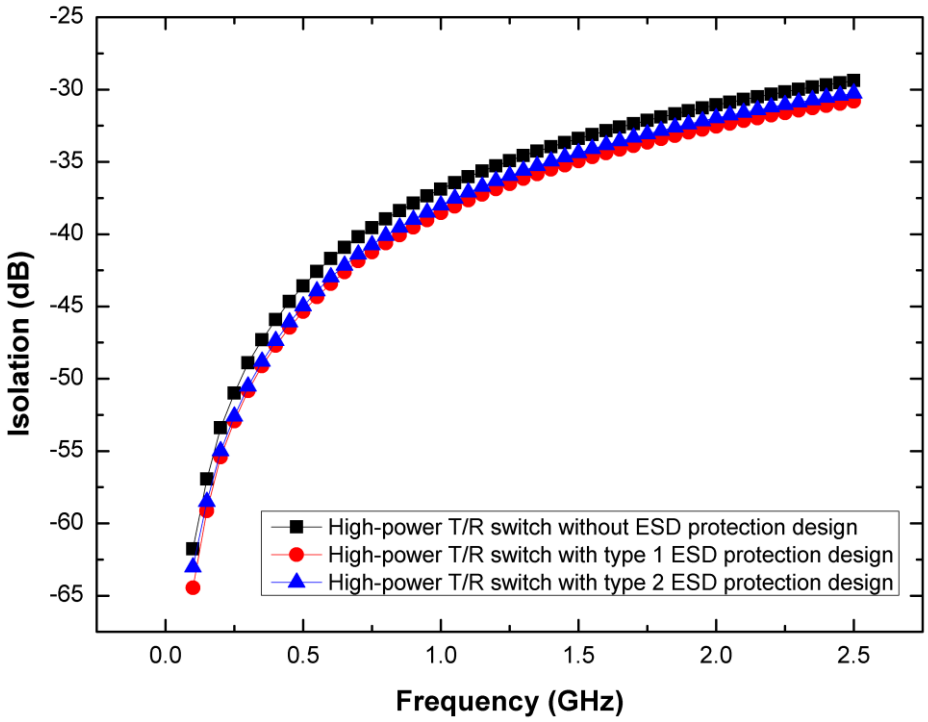


Fig. 3.46. Isolation in RX mode of high-power T/R switches.

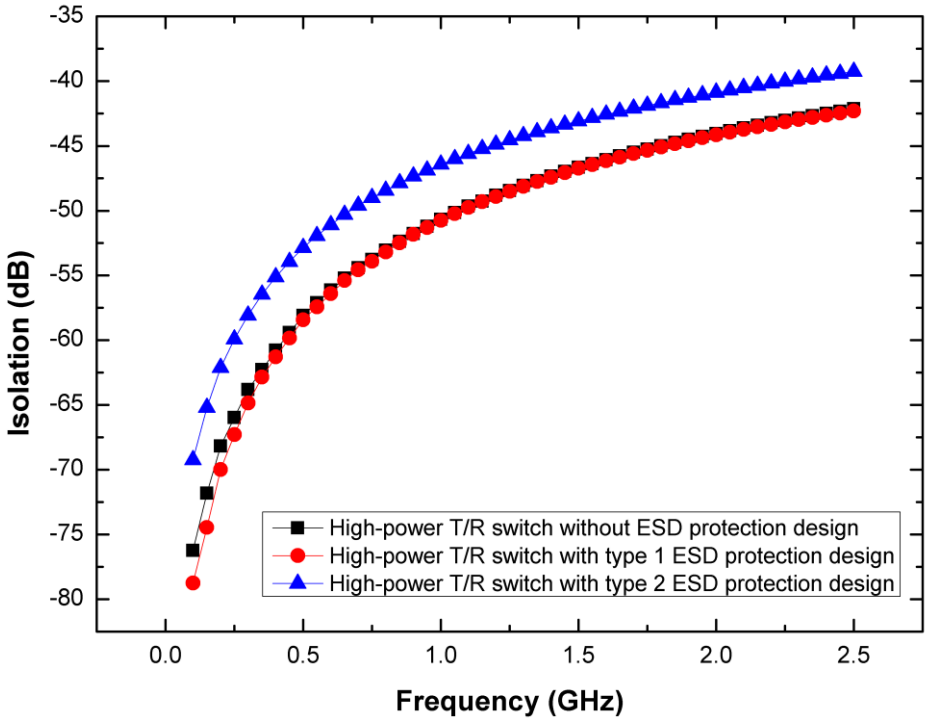


Fig. 3.47. Isolation in TX mode of high-power T/R switches.

3.3.3 Comparison of RF Performances After ESD Stress

Since the high-power T/R switch are surrounded by 10kohm resistors, the scale of the leakage current at the damaged point in comparison to the standby DC current of the resistors may be too low to be detected. Therefore, RF parameters are measured again after the HBM ESD stressing on the ANT node to ensure the high-power T/R switch can still operate regularly.

The RX and TX insertion loss of the high-power T/R switch without ESD protection are shown in Fig. 3.48 and Fig. 3.49. In Fig. 3.48, RX insertion loss after 0.5kV PS-mode HBM stress is degraded significantly. On the other hand, TX insertion loss is still remain the same. It indicates that the damage spot is located at the RX branch of the circuit.

Fig. 3.50 and Fig. 3.51 demonstrate the insertion loss of high-power T/R switch with type 1 ESD protection design. The RX insertion loss after 4kV PS-mode HBM stress is out of shape whereas the TX insertion does not affect by the ESD stress. The HBM level of the type 1 ESD protection design can sustain 3.5kV stress. With no degradation in the TX insertion loss, the damage part of the type 1 ESD protection design can be recognized at the RX branch, too.

In Fig. 3.52, the high-power T/R switch with type 2 ESD protection design can survive from the 4.5kV PS-mode HBM stress. However, in Fig. 3.53, no significant degradation on the insertion loss of TX, too. Type 2 ESD protection design provides the highest ESD robustness of all the T/R switches design.

Fig. 3.54 and Fig. 3.55 show the measured P_{1dB} of the high-power T/R switch after 4kV PS-mode HBM stress. Fig. 3.56 and Fig. 3.57 show the measured P_{1dB} of the high-power T/R switch with type 1 ESD protection design after 4kV PS-mode HBM stress. Fig. 3.58 and Fig. 3.59 show the measured P_{1dB} of the high-power T/R switch with type 2 ESD protection design after 4kV PS-mode HBM stress. The linearity of the T/R switches remain unchanged after the PS-mode HBM 4kV stress.

Finally, Fig. 3.60 and Fig. 3.61 show the insertion loss of RX and TX after NS-mode HBM 4kV stress on ANT node.

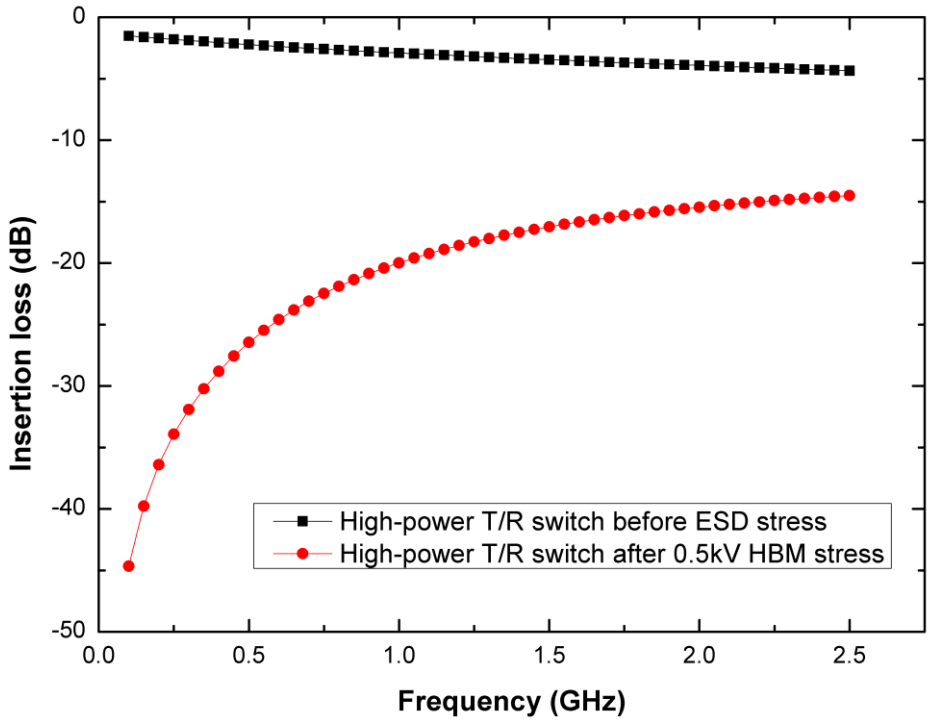


Fig. 3.48. RX IL of high-power T/R switch after 0.5kV PS-mode HBM stress.

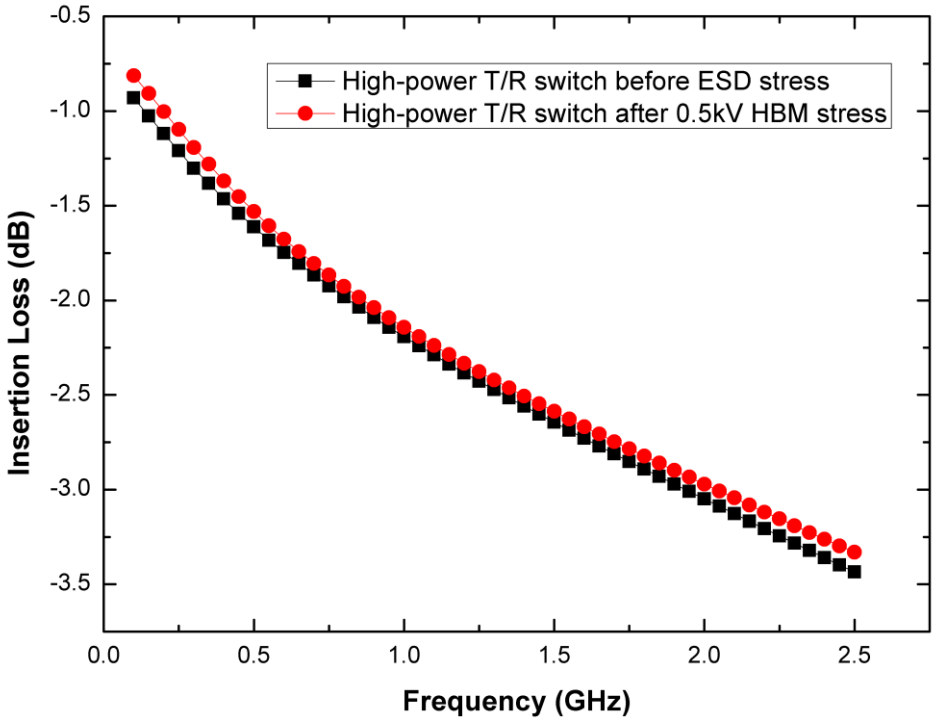


Fig. 3.49. TX IL of high-power T/R switch after 0.5kV PS-mode HBM stress.

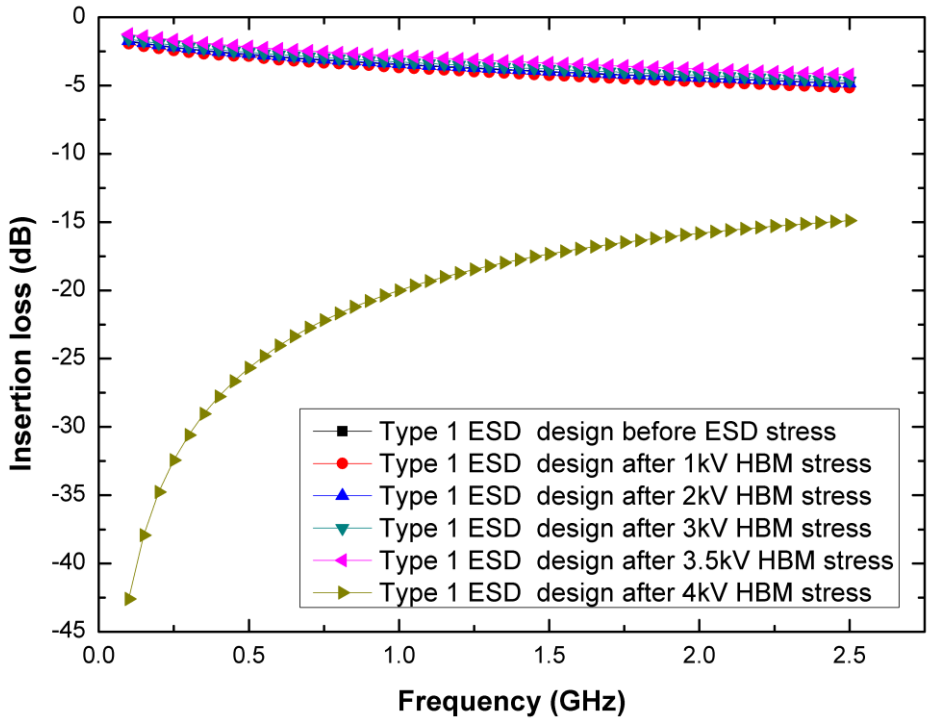


Fig. 3.50. RX IL of type 1 ESD protection design after 4kV PS-mode HBM stress.

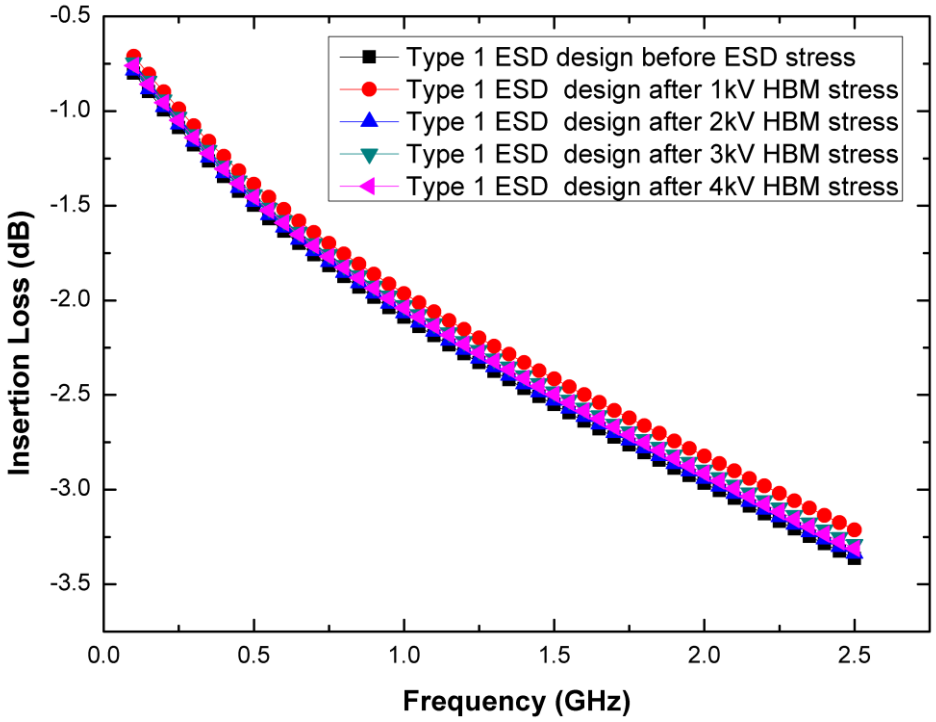


Fig. 3.51. TX IL of type 1 ESD protection design after 4kV PS-mode HBM stress.

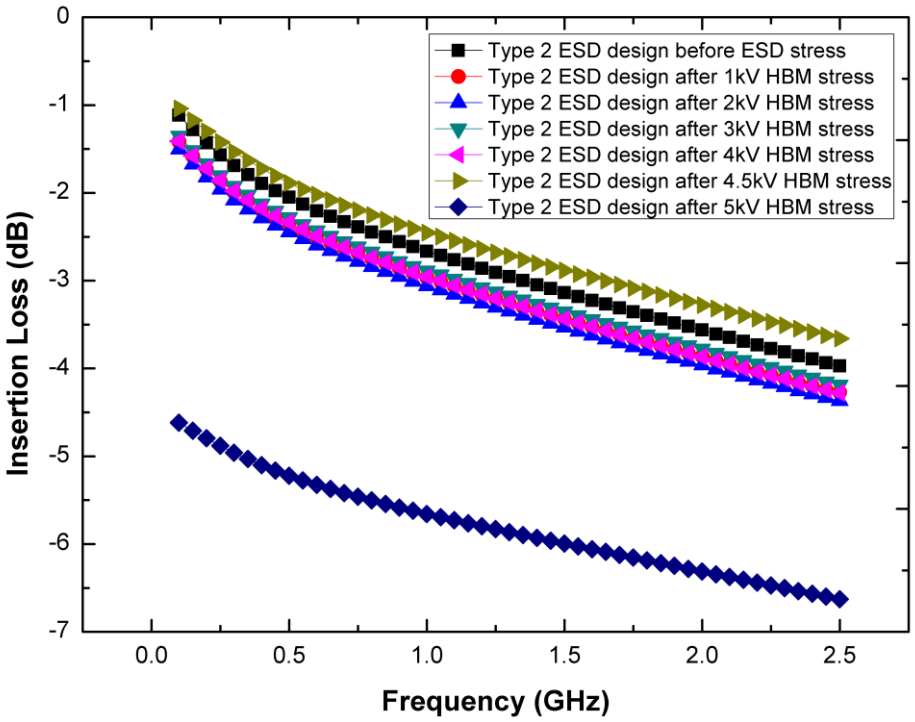


Fig. 3.52. RX IL of type 2 ESD protection design after 5kV PS-mode HBM stress.

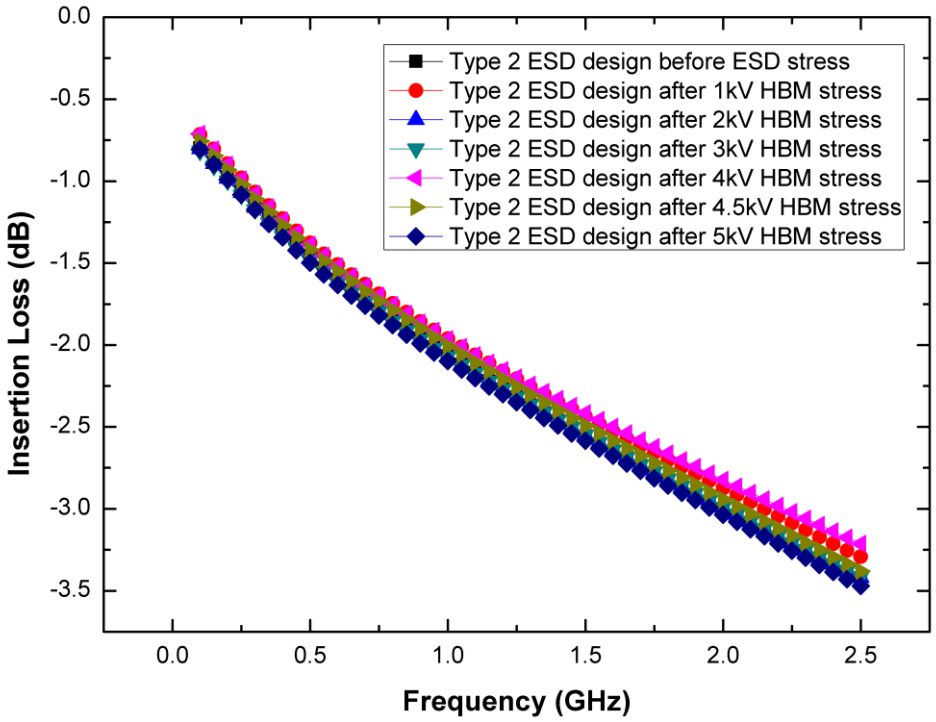


Fig. 3.53. TX IL of type 2 ESD protection design after 5kV PS-mode HBM stress.

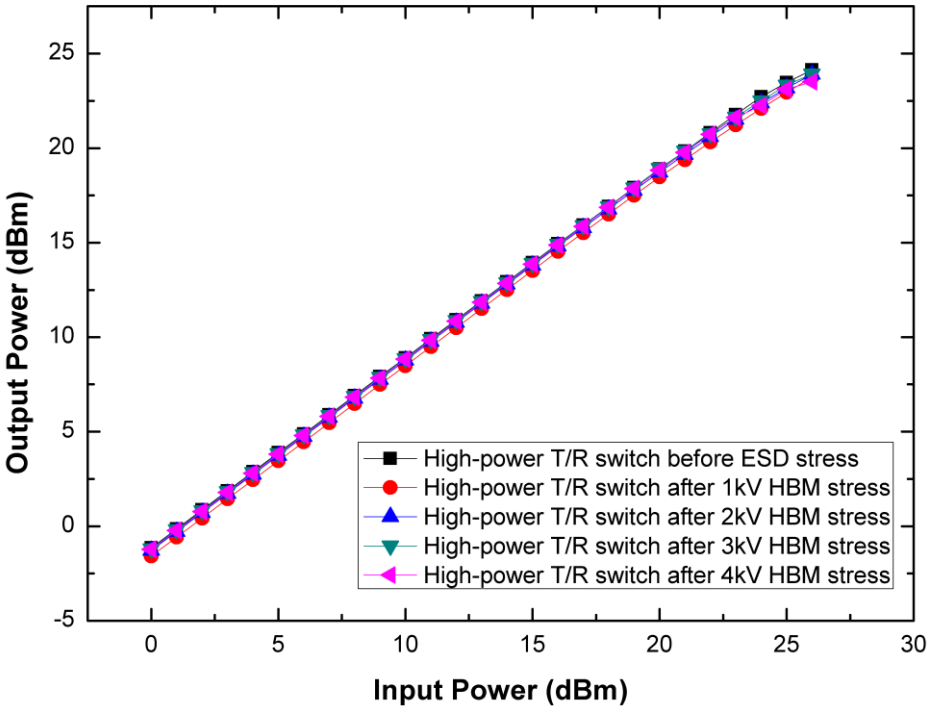


Fig. 3.54. P_{1dB} of high-power T/R switch at 0.9GHz after 4kV PS-mode HBM stress.

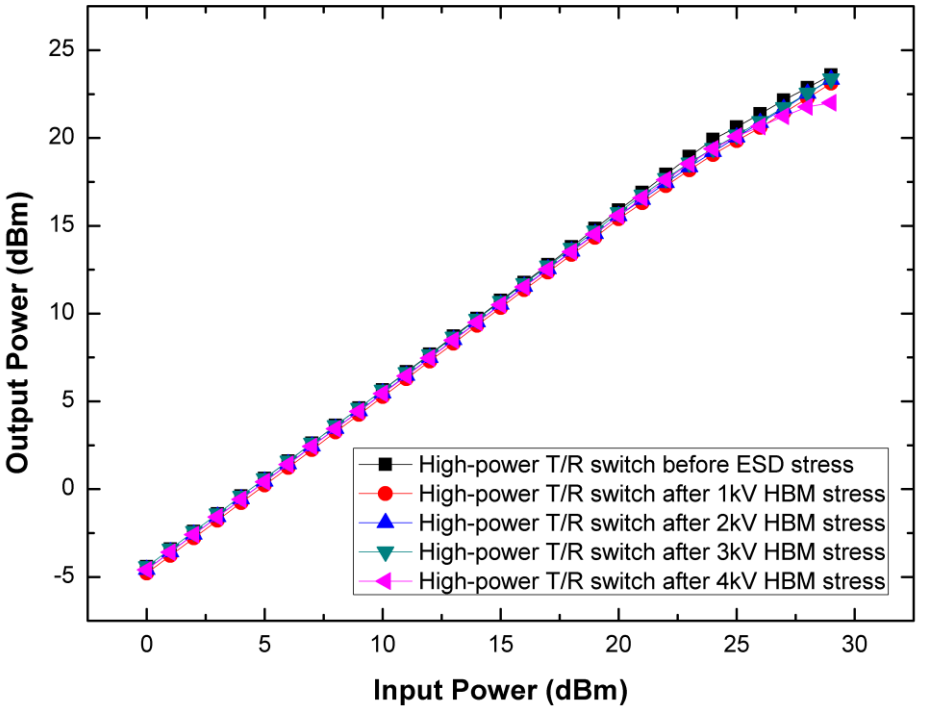


Fig. 3.55. P_{1dB} of high-power T/R switch at 1.8GHz after 4kV PS-mode HBM stress.

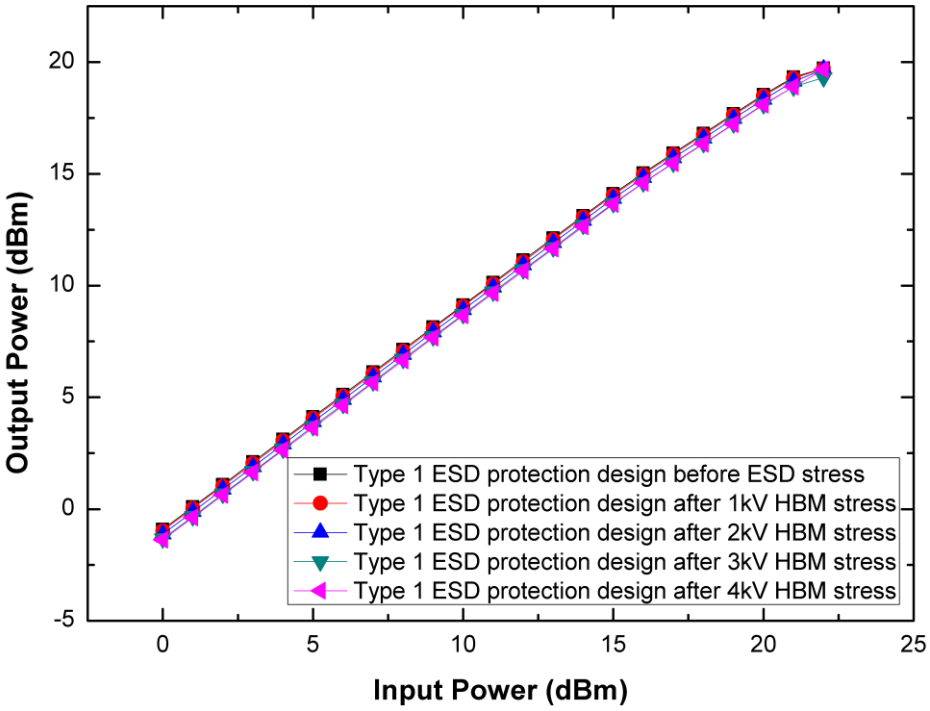


Fig. 3.56. P_{1dB} of type 1 ESD protection design at 0.9GHz after 4kV PS-mode HBM stress.

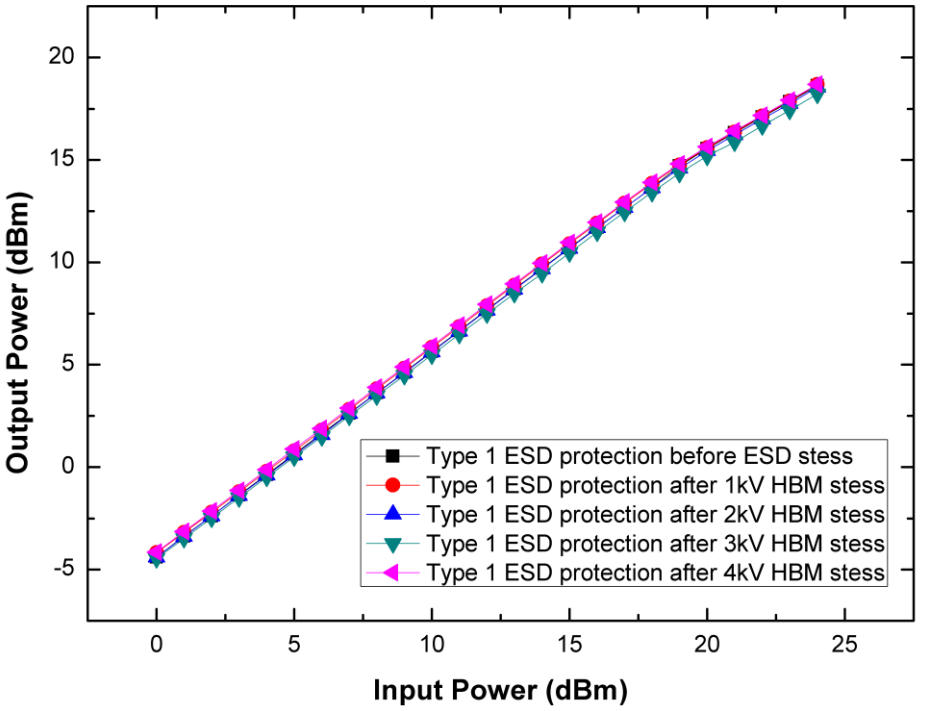


Fig. 3.57. P_{1dB} of type 1 ESD protection design at 1.8GHz after 4kV PS-mode HBM stress.

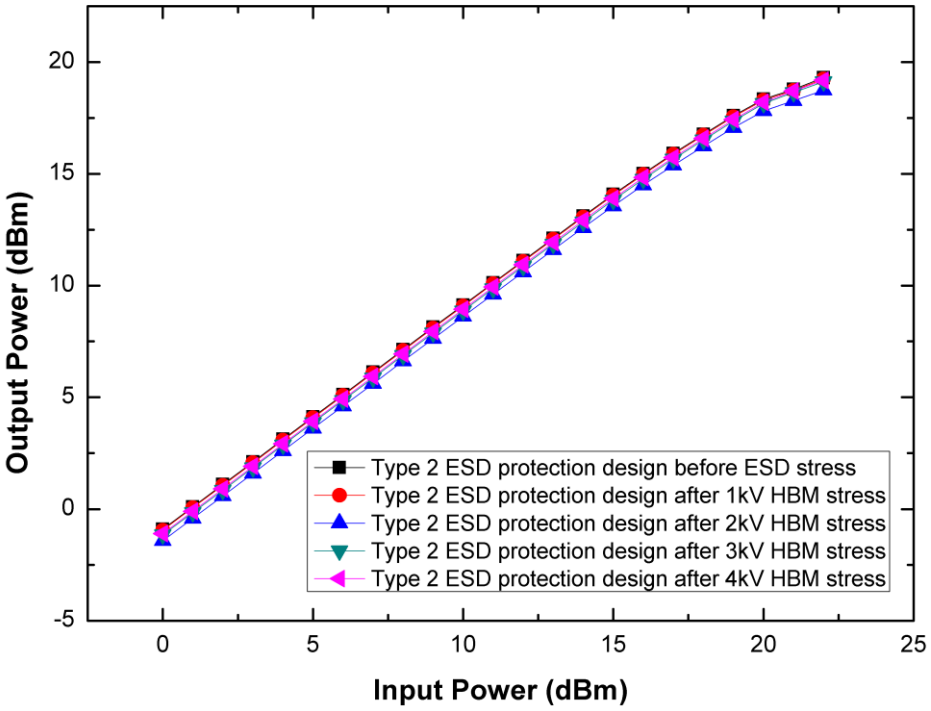


Fig. 3.58. P_{1dB} of type 2 ESD protection design at 0.9GHz after 4kV PS-mode HBM stress.

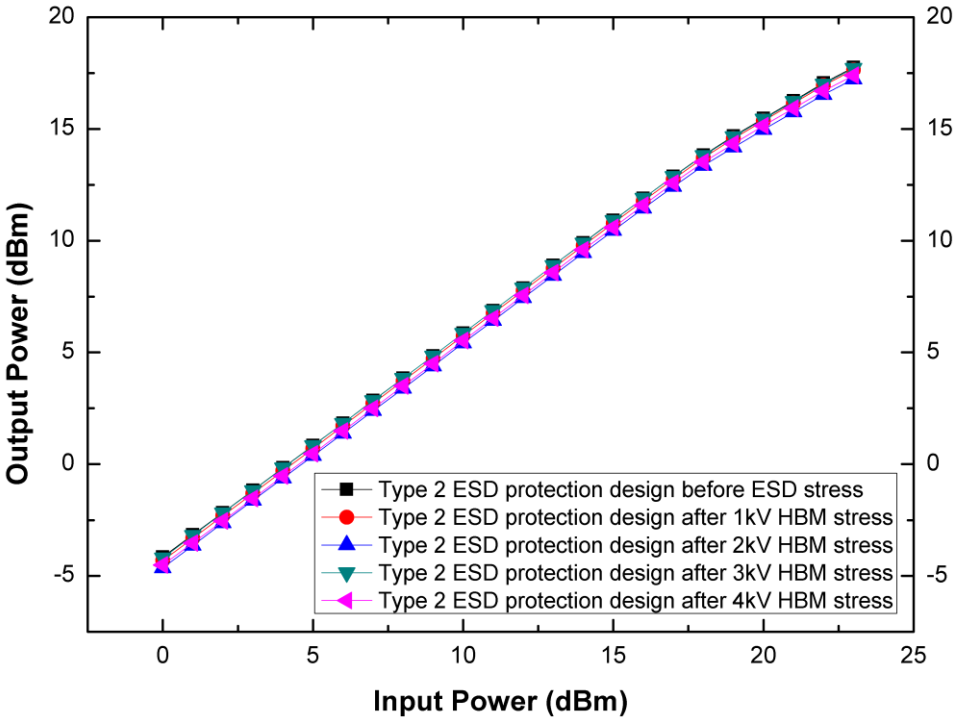


Fig. 3.59. P_{1dB} of type 2 ESD protection design at 1.8GHz after 4kV PS-mode HBM stress.

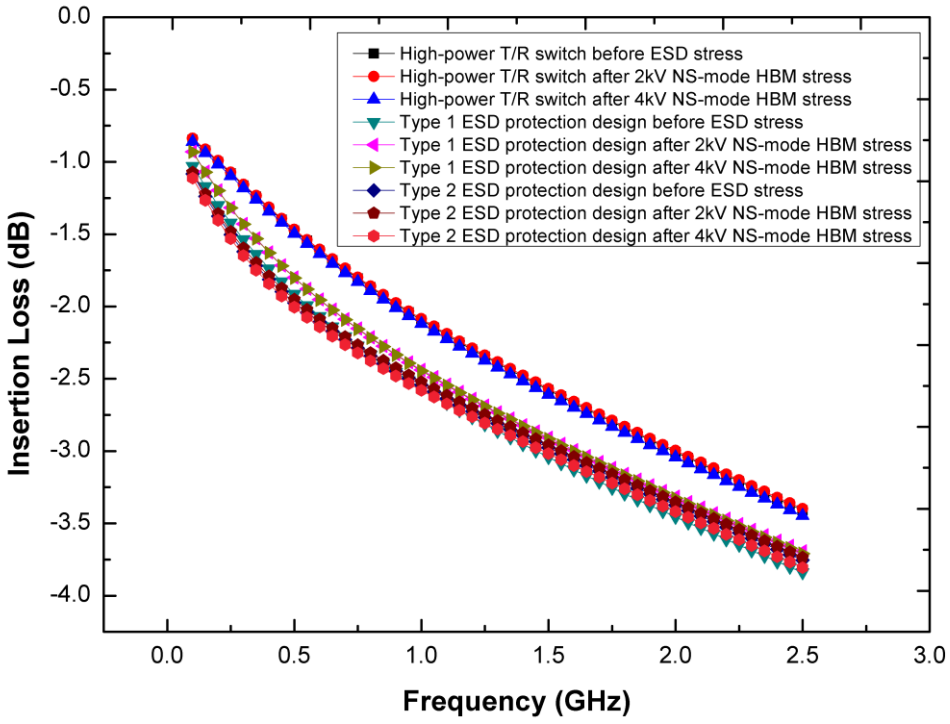


Fig. 3.60. RX insertion loss of T/R switches after 4kV NS-mode HBM stress.

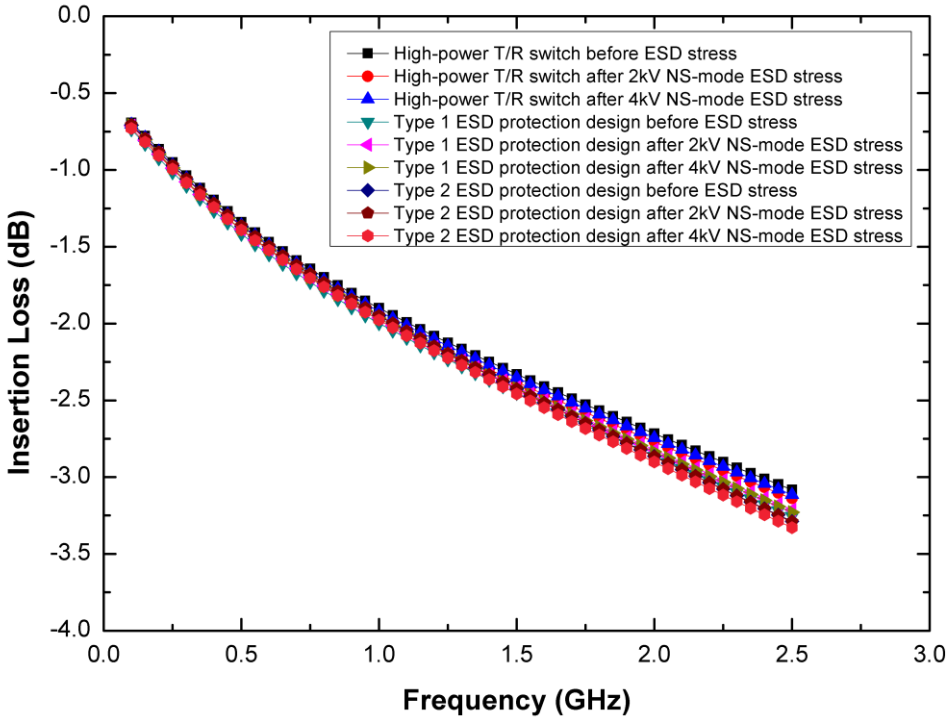


Fig. 3.61. TX insertion loss of T/R switches after 4kV NS-mode HBM stress.

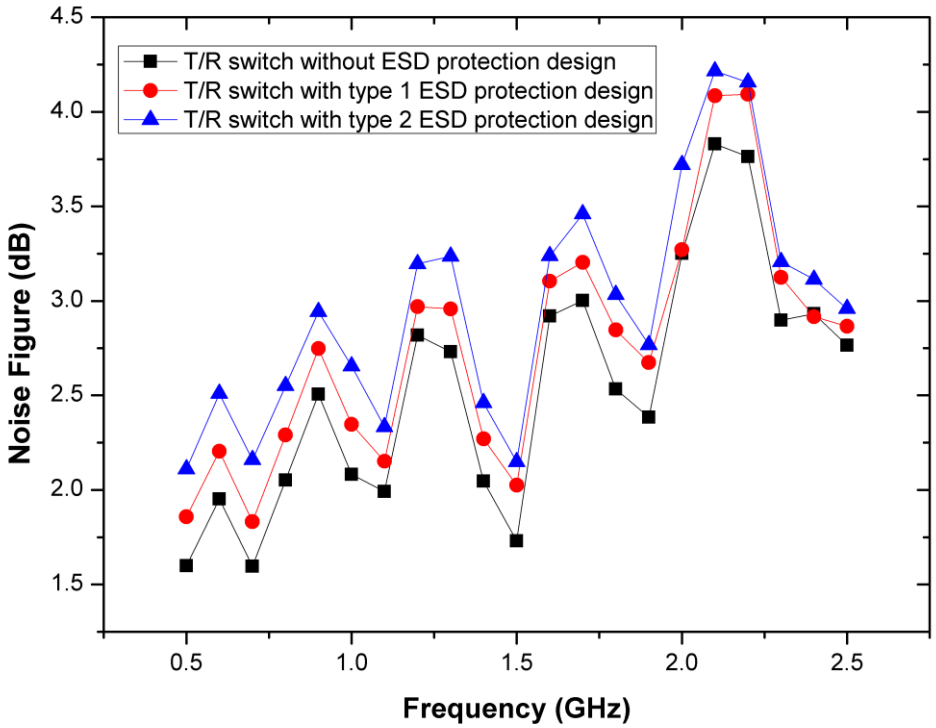


Fig. 3. 62. Measured noise figure of the T/R switches.

Fig. 3.62 shows the measured noise figure by N8975A noise figure analyzer in CIC. Since the T/R switch is a purely lossy signal path which does not have power gain, the deviation of the measured noise figure becomes larger than other RF circuit such as LNA, which has signal gain intrinsically. However, as a matter of fact, the measured noise figure in type 1 and type 2 ESD design are increased about 0.25dB and 0.5dB.

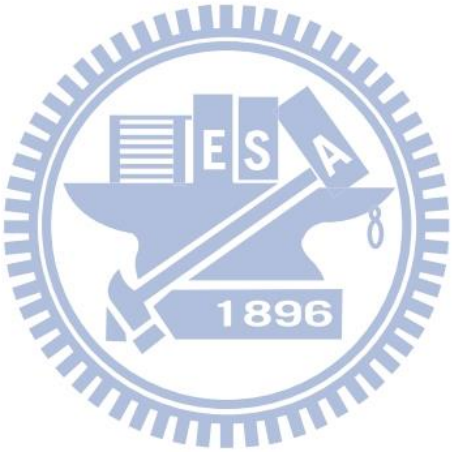
Among all of the presented graphs above, an interesting thing is that the degradation trend of insertion loss in Fig. 3.52 is different than Fig. 3.48 and Fig. 3.50, it indicates that the damaged part of the type 2 ESD protection design is different than original T/R switch and the type 1 ESD protection design.

Table 3.5 summarizes the HBM levels of the T/R switches. Judging from both the DCIV curves and the RF performance, the type 1 and type 2 ESD protection design can ensure the T/R switch operates normally after 3.5kV and 4.5kV PS-mode HBM stress, respectively.

Table 3.5

Comparison of HBM levels judged by DCIV curves and RF performance.

HBM tests on ANT node	Judged by DCIV curves		Judged by RF performance	
	PS-mode	NS-mode	PS-mode	NS-mode
High-power T/R switch w/o ESD protection design	0.1kV	5kV	< 0.5kV	> 4kV
High-power T/R switch with type 1 ESD protection design	3.75kV	5kV	3.5kV	> 4kV
High-power T/R switch with type 2 ESD protection design	4.5kV	6kV	4.5kV	> 4kV



3.3.4 Failure Analysis and Discussion

The failure analysis is conducted to find out the damaged spots of the high-power T/R switch after HBM stresses. The SEM photo of the three T/R switches after total delayer procedures is shown in Fig. 3.63. For the high-power T/R switch without ESD protection design after 0.5kV PS-mode HBM stress, the damaged spot is located at the first transistor of the RX branch, as shown in Fig. 3.64.

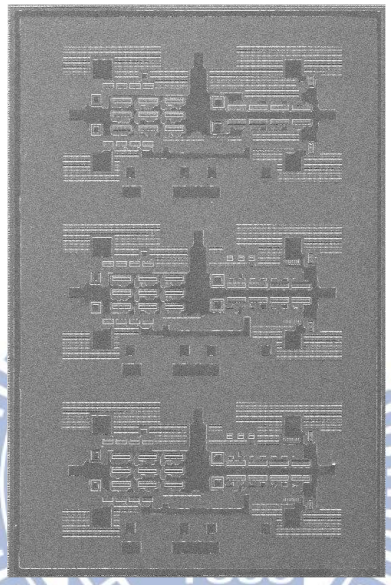


Fig. 3.63. SEM photo of the T/R switches.

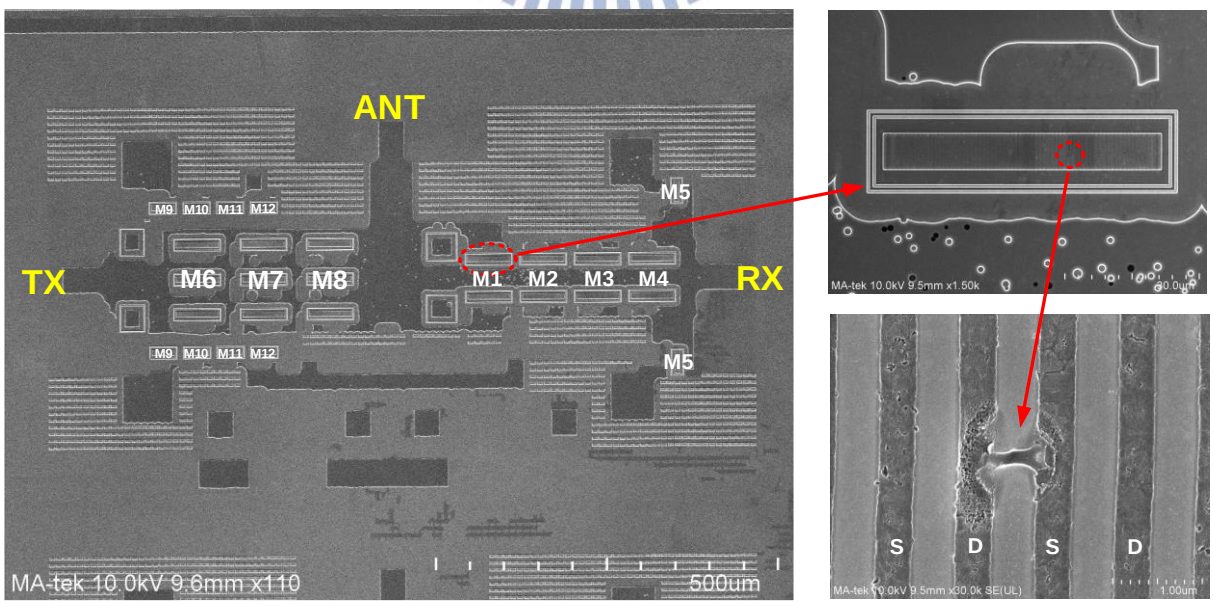


Fig. 3.64. SEM photos showing the high-power T/R switch without ESD protection design after 0.5kV PS-mode HBM stress.

In Fig. 3.65, the damaged part of the high-power T/R switch with type 1 ESD protection design after 4kV PS-mode HBM stress is founded at the first transistor of the RX branch, too. However, the failure point of the type 2 ESD protection design is located at the RX shunt transistors, as shown in Fig. 3.66. The PS-mode ESD are passed to the last (and the weakest) transistors in the discharging path with the help of the body-source connected RX transistors. The damage on the drain of the transistors are more severe than the source in PS-mode HBM.

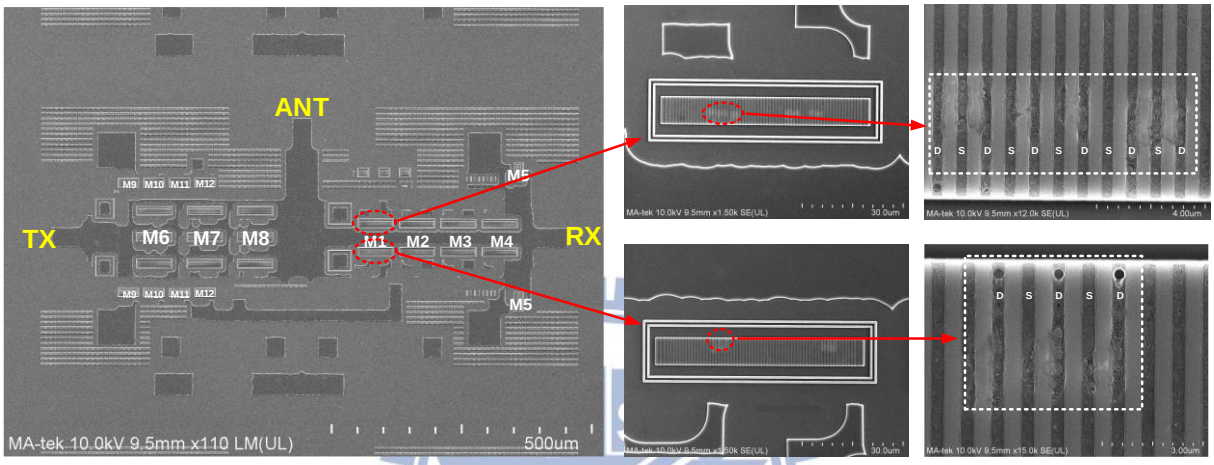


Fig. 3.65. SEM photos showing the high-power T/R switch with type 1 ESD protection design after 4kV PS-mode HBM stress.

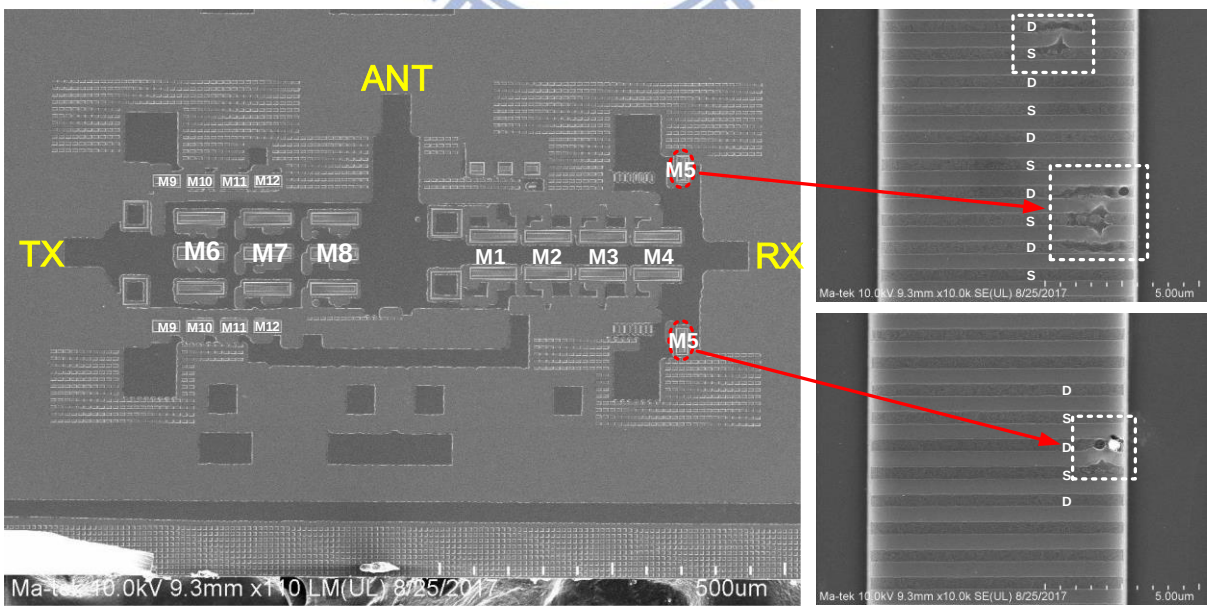


Fig. 3.66. SEM photos showing the high-power T/R switch with type 2 ESD protection design after 5kV PS-mode HBM stress.

For NS-mode ESD failure analysis, Fig. 3.67, Fig. 3.68, and Fig. 3.69 show the SEM photos after NS-mode HBM stressing. The damaged spot of the T/R switch without ESD protection design and the T/R switch with type 1 ESD protection design are located at the shunt transistors of the TX branch which are nearest to the ground, as shown in Fig. 3.67 and Fig. 3.68. The discharging path of the NS-mode ESD are the parasitic BJTs in series. The TX parasitic BJTs are weaker than the RX parasitic BJTs since the discharging path (Ron) on TX is longer (larger) than RX. The white spots discovered on the source of the transistors indicate that the contact are melted into the substrate and were not wash off after the total delayer procedures.

On the other hand, Fig. 3.69 shows a different location of the T/R switch with type 2 ESD protection design after 7kV NS-mode HBM stress. The burning site are located at the shunt transistors of RX branch. This indicates that the reverse body diodes in the RX branch are the preferred discharging path for the NS-mode stressing. With the help of the source-body connection, the NS-mode ESD robustness of the high-power T/R switch with type 2 ESD protection design is higher than the high-power T/R switch with type 1 ESD protection design.

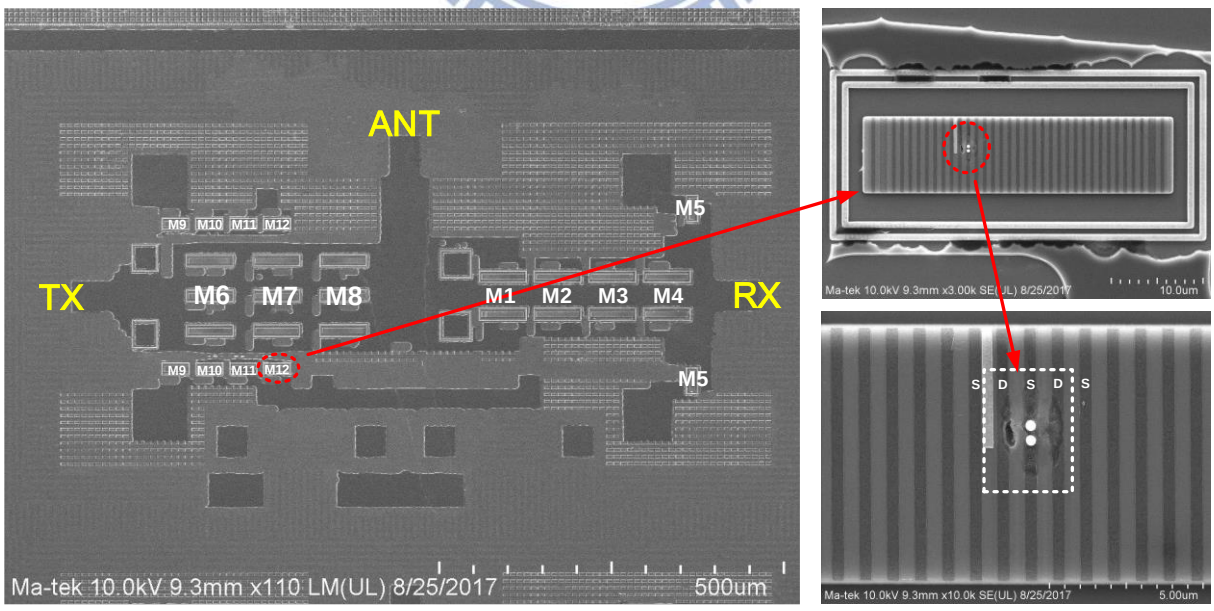


Fig. 3.67. SEM photos showing the high-power T/R switch without ESD protection design after 6kV NS-mode HBM stress.

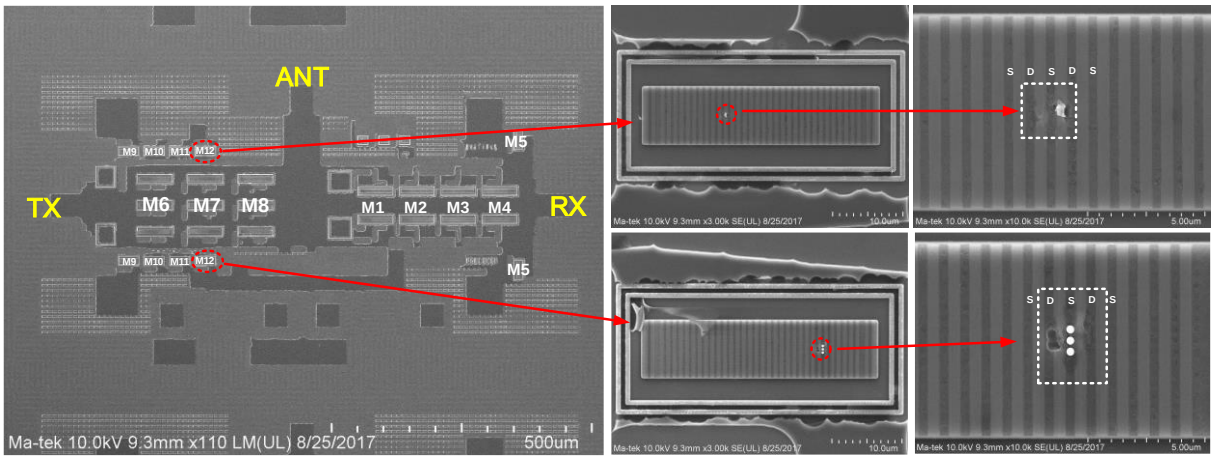


Fig. 3.68. SEM photos showing the high-power T/R switch with type 1 ESD protection design after 6kV NS-mode HBM stress.

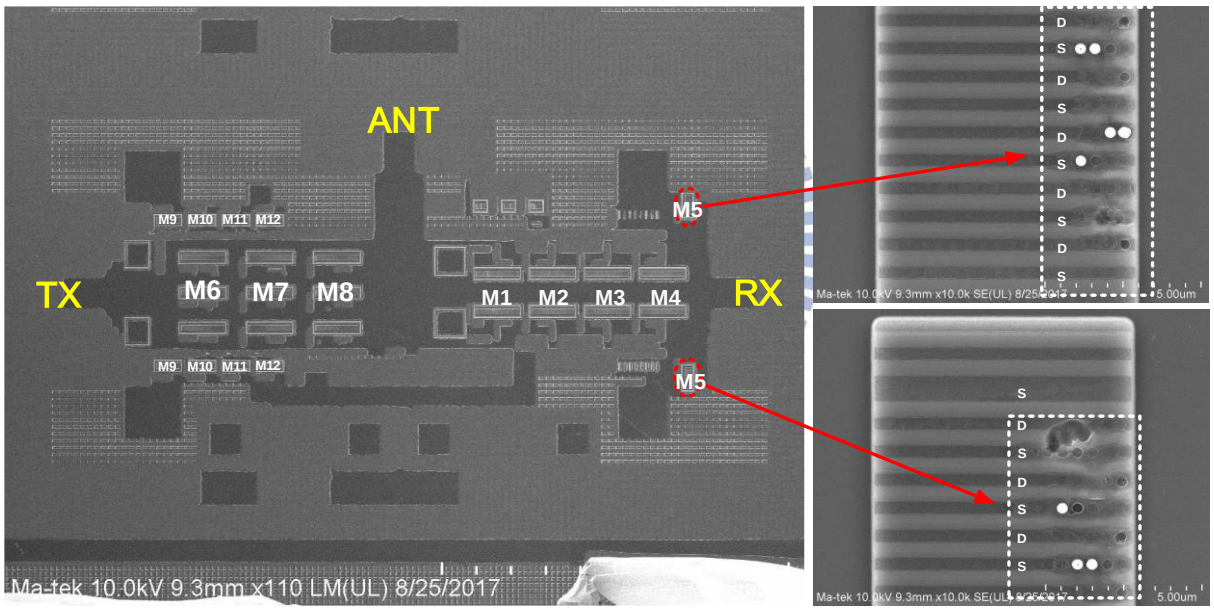


Fig. 3.69. SEM photos showing the high-power T/R switch with type 2 ESD protection design after 7kV NS-mode HBM stress.

3.3.5 The Effect of the Substrate Resistance

The high-power T/R switch with the same architecture had been implemented in a previous tape-out shuttle. In the previous design, the dummy pattern are extended vertically into the p-substrate of the silicon with M1-Diffusion contacts. Since the dummy pattern in the RF layout are grounded perfectly, the silicon substrate will be connected to ground, too. It results in an extreme low substrate resistance R_{sub}. With R_{sub} which approach to zero, the RF signal will leak to ground through the low impedance path of C_{PWELL} and C_{DNW} which are depicted in Fig. 2.3. The RF performance of the T/R switch is therefore degraded.

Fig. 3.70 and Fig. 3.71 show the comparison of measured RX insertion loss and TX insertion loss of the high-power T/R switch in different tape-out shuttles, respectively. Similarly, Fig. 3.72 and Fig. 3.73 show the difference of the P_{1dB} of the high-power T/R switch in 0.9GHz and 1.8GHz, respectively. The RF performance of the high-power T/R switch with Rsub=0 is worse than the one with substrate floating.

The comparison of measured HBM levels are listed in Table 3.6. The PS-mode HBM level of the T/R switches with R_{sub}=0 are 0.1kV, 4kV, and 5kV, respectively. The PS-mode HBM levels of the T/R switches with R_{sub}=0 are about the same compare to the substrate floating ones. As for the NS-mode HBM testings, the T/R switches with R_{sub}=0 can all achieve the level of 8kV. With R_{sub}=0, SCRs can be easily formed in the nearest transistors to the ANT, M1 and M8, to discharge the NS-mode ESD current, as shown in Fig. 3.74. The parasitic transistors is embedded in the drain of M1 and source of M8. Fig. 3.75(a) and Fig. 3.75(b) illustrate the cross-section view of M8 and M1, respectively. SEM photo of the high-power T/R switch with R_{sub}=0 after total delayer procedures is shown in Fig. 3.76. The damaged spots are discovered on M1 and M8 after NS-mode 9A TLP pulses stress on the ANT port. Fig. 3.77 shows the enlarged graph of Fig. 3.76 on M8, where the source of M8 is damaged more severe than the drain. On the other hands, the drain of the M1 is more severe than the source (Fig. 3.78). The failure analysis demonstrate the existence of the parasitic SCRs under the NS-mode ESD conditions.

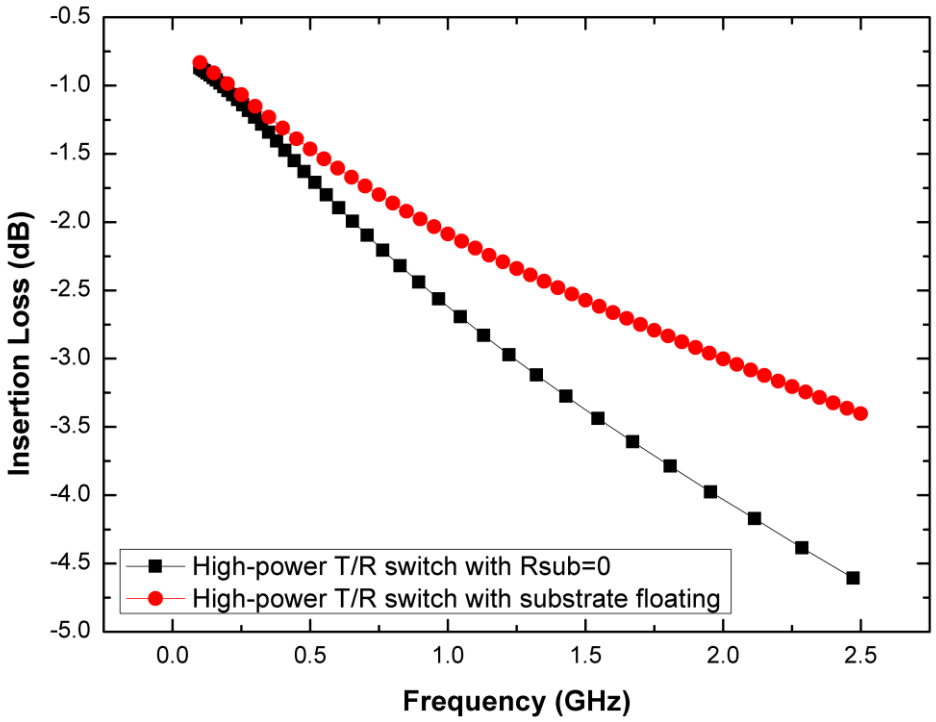


Fig. 3.70. RX insertion loss of high-power T/R switch with Rsub=0 and substrate floating.

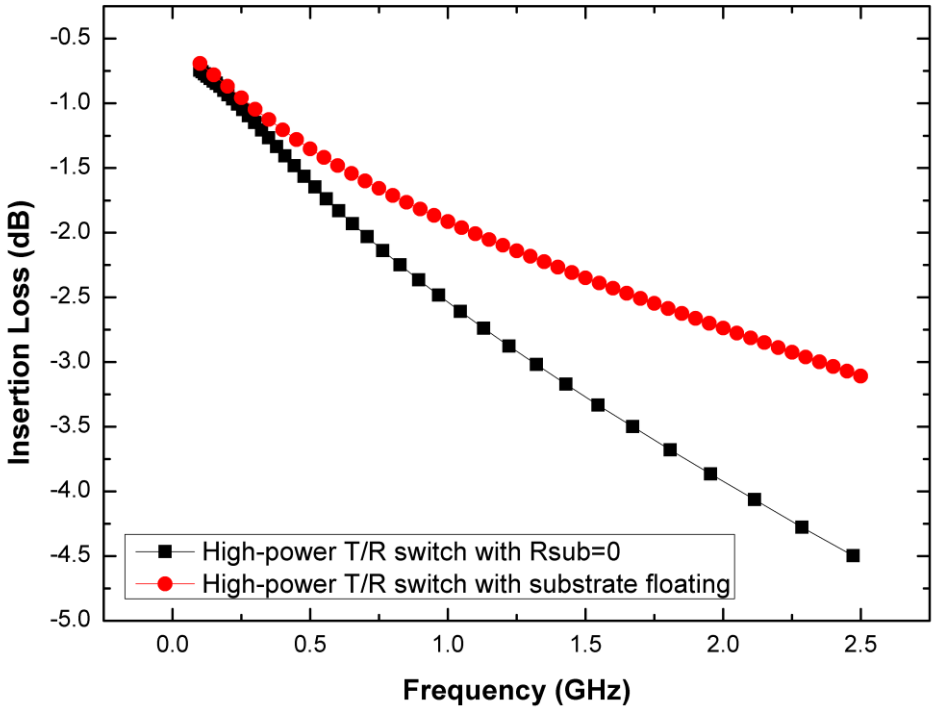


Fig. 3.71. TX insertion loss of high-power T/R switch with Rsub=0 and substrate floating.

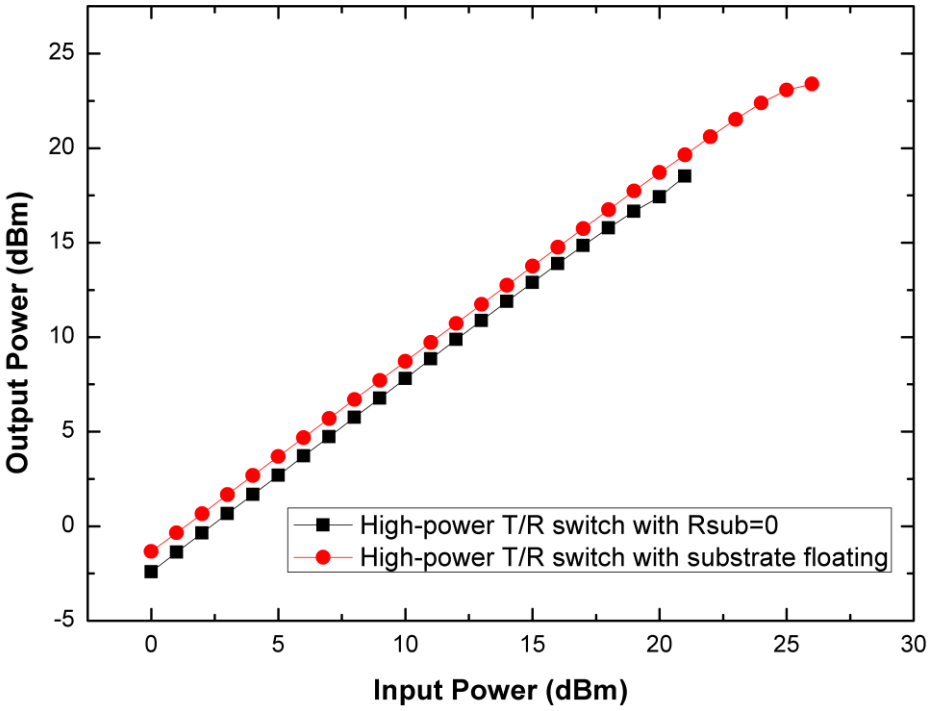


Fig. 3.72. P_{1dB} of high-power T/R switch with Rsub=0 and substrate floating at 0.9GHz.

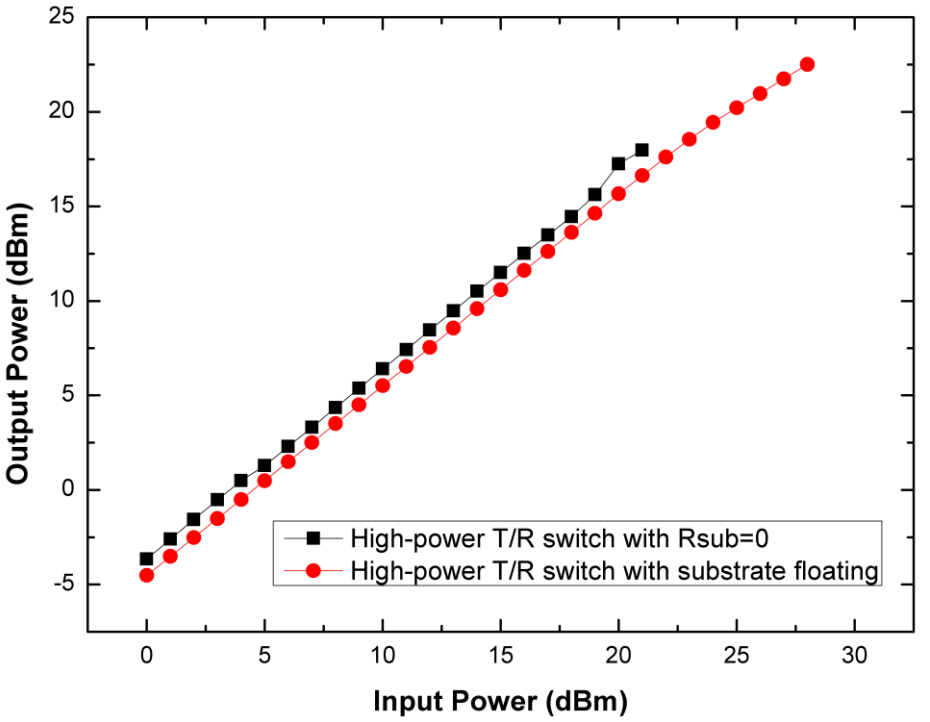


Fig. 3.73. P_{1dB} of high-power T/R switch with Rsub=0 and substrate floating at 1.8GHz.

Table 3.6

Comparison of HBM levels between R_{sub}=0 and substrate floating.

Measured HBM level	PS-mode		NS-mode	
	Rsub=0	Substrate floating	Rsub=0	Substrate floating
High-power T/R switch without ESD protection design	0.1kV	0.1kV	8kV	5kV
High-power T/R switch with type 1 ESD protection design	4kV	3.5kV	8kV	5kV
High-power T/R switch with type 2 ESD protection design	5kV	4.5kV	8kV	6kV

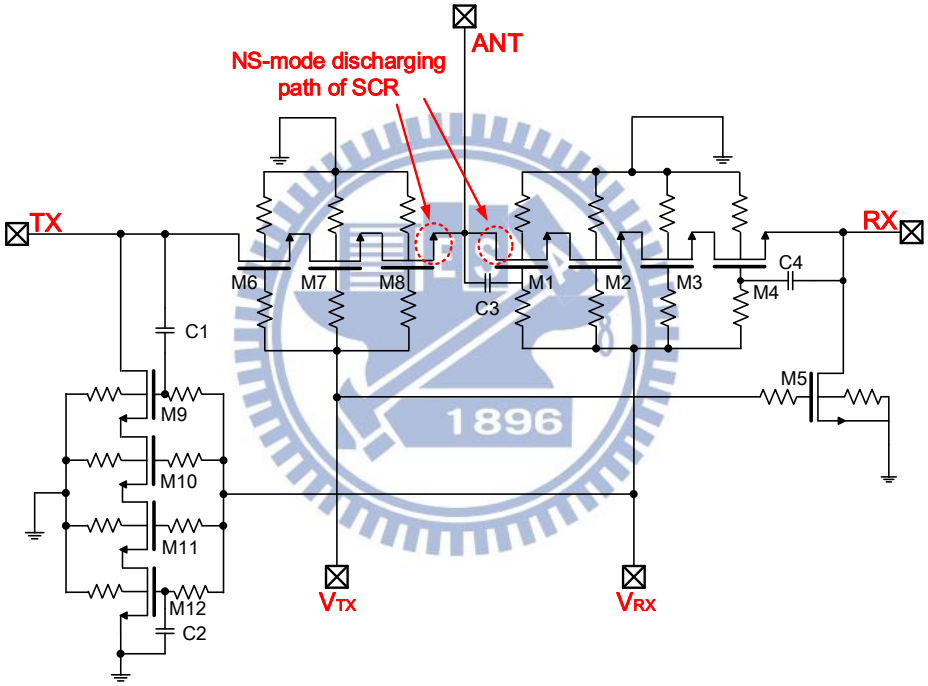


Fig. 3.74. The parasitic SCR path to discharge the NS-mode ESD is located at the source of the M8 and drain of M1, which is nearest to the ANT node.

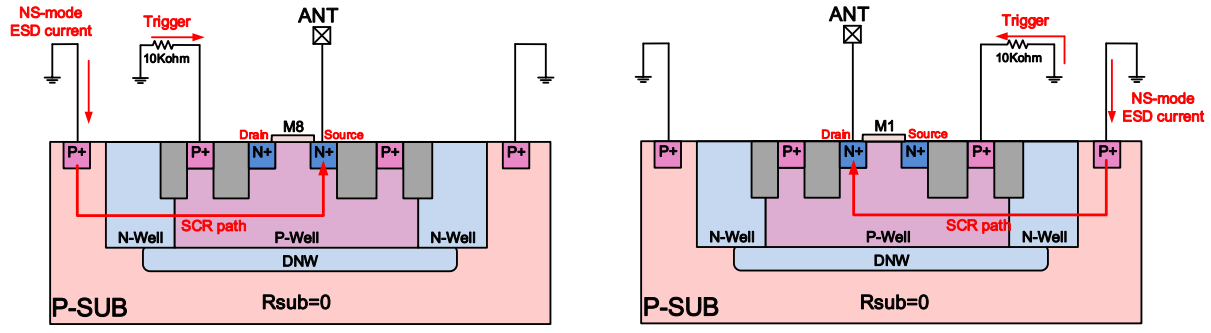


Fig. 3.75. The cross-section view of SCR path in NS-mode direction on (a) M8 and (b) M1.

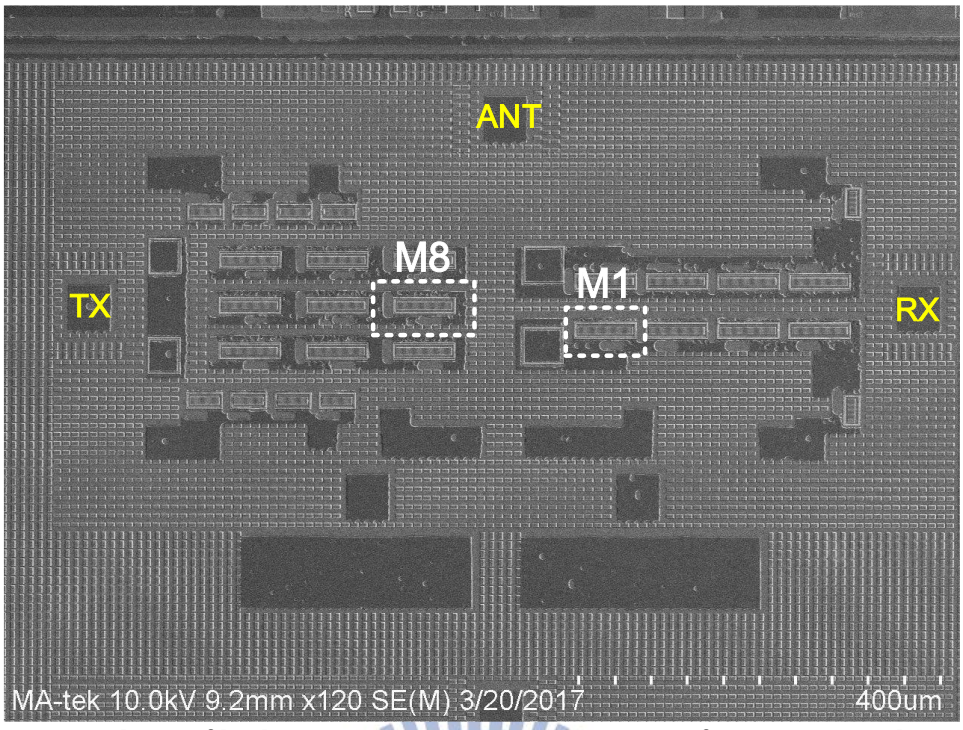


Fig. 3.76. SEM photo of high-power T/R switch with R_{sub}=0 after 9A NS-mode TLP stress.

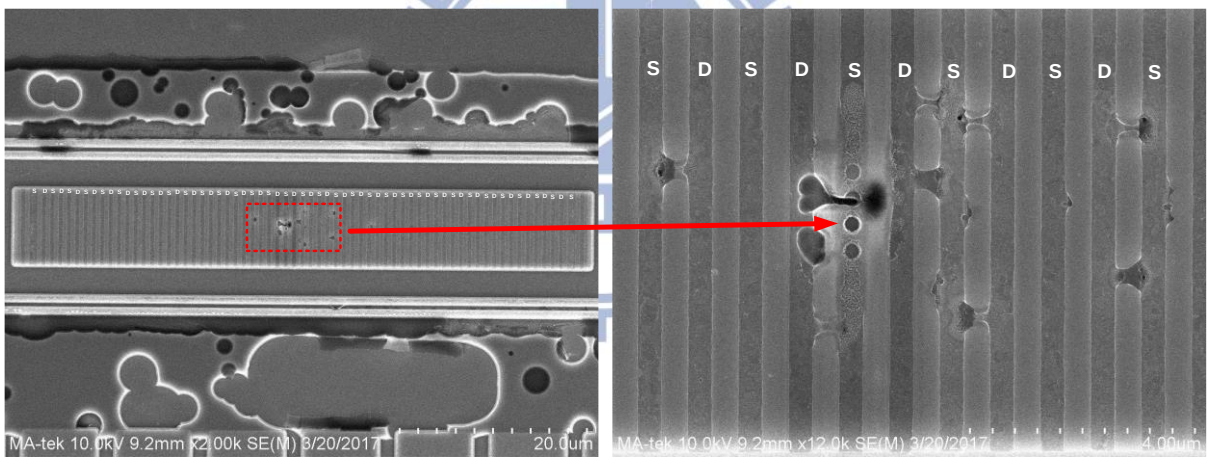


Fig. 3.77. Enlarged part of M8 in Fig. 3.76 to observe the damage spot in the source of M8.

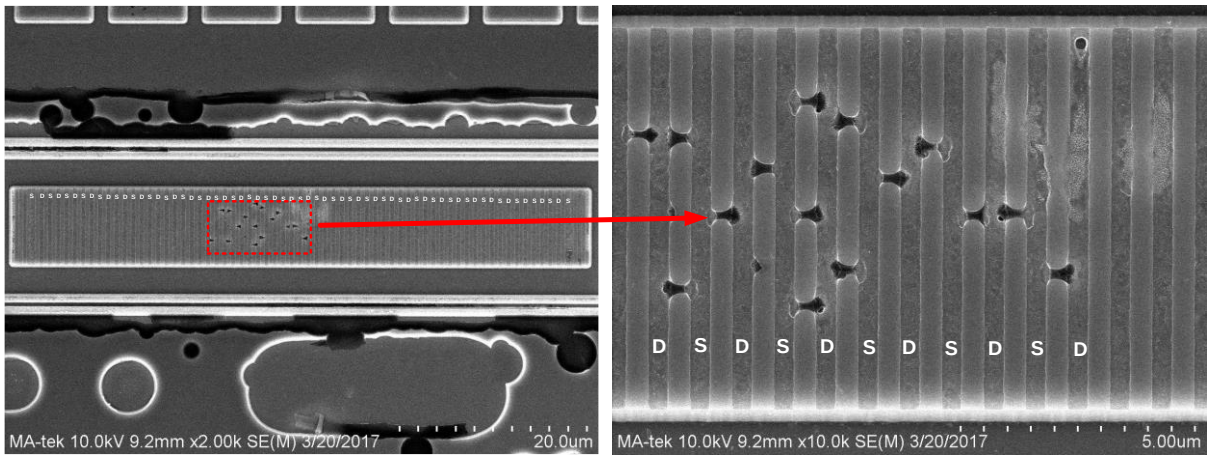


Fig. 3.78. Enlarged part of M1 in Fig. 3.76 to observe the damage in the drain of M1.

3.4 Summary

The high-power T/R switch with proposed type 1 and type 2 ESD protection design are fabricated in a 0.18-μm CMOS process. The DCIV curves after different HBM levels zapping and RF performances before ESD stress are measured. The type 1 and type 2 ESD protection design can discharge the ESD current without any additional discharge path and enhance the PS-mode HBM robustness from 0.1kV to 3.5kV and 4.5kV, respectively. Besides, the NS-mode HBM levels of the T/R switch without ESD protection design, with type 1 ESD protection design, and type 2 ESD protection design are 5kV, 5kV, and 6kV, respectively.

The RX and TX insertion loss of the high-power T/R switch without ESD protection design is 1.81dB, 1.98dB at 0.9GHz and 2.58dB, 2.83dB at 1.8GHz. The P_{1dB} of the high-power T/R switch without ESD protection design is 25.6dBm at 0.9GHz and 28.6dBm at 1.8GHz. In comparison, the insertion loss of the T/R switches with proposed ESD protection design are degraded only 0.1dB ~ 0.4dB in the interested frequencies. However, the P_{1dB} of the T/R switches with proposed ESD protection design are degraded 3dBm ~ 5dBm in the interested frequencies.

After the RF and ESD measurements, the failure analysis is conducted. The damaged spots vary in different ESD testing modes and ESD protection designs. For T/R switch without ESD protection design and T/R switch with type 1 ESD protection design, the failure part in PS-mode and NS-mode are located at the first series transistors of RX branch and the last shunt transistors in TX branch. However, the failure part of the T/R switch with type 2 ESD protection design are located at the shunt transistors of RX branch, in both PS-mode and NS-mode.

At last, the substrate resistance is also a parameter that affect both ESD robustness and RF performance. With R_{sub}=0, the T/R switches own the highest ESD robustness, however, the RF performance is poor; with substrate floating, the RF performance are better, and the ESD robustness can still meet the specifications.

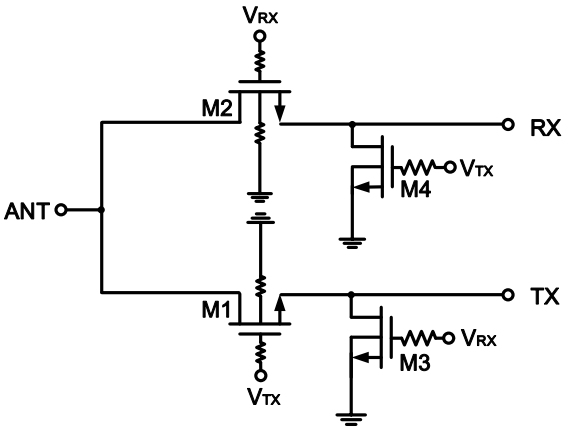
Chapter 4

ESD Protection Design for Conventional T/R Switch

4.1 Circuit Design of Conventional T/R Switch

The schematic of conventional T/R switch is drawn in Fig. 4.1. The series-shunt architecture T/R switch are employed to be the protected circuit. Different from the prior art [10], which the ESD current can be discharged by the original body-diodes in NMOS and PMOS because the body-floating resistance R_{BF} is not included in the circuits. In Fig. 4.1, the body-floating resistance is connected between P-Well and the ground. In giga-hertz operations, the body-floating resistance is regarded as open circuit for RF signal and therefore reduces the insertion loss and substrate noise.

In this design, to minimize the insertion loss, the dimension of the transistors M1 and M2 in series branch is 200/0.1 (μm). M3 and M4 in shunt branch is 12/0.1 (μm) in order to tune the real part of the impedance to 50 ohm for matching purpose to the next circuit block. The gate resistance and body-floating resistance are both 10kohm. The test chip is tapped out in a 90-nm CMOS process.



Transistor	Dimensions (μm)
M1, M2	200/0.1
M3, M4	12/0.1

Fig. 4.1. Schematic and device parameters of conventional T/R switch.

4.2 Traditional ESD Protection Design for Conventional T/R Switch

Since the ESD stress will strike into the IC from antenna, the four ESD testing modes are zapping on the antenna port to ensure the reliability of the product. To discharge the ESD current immediately during the ESD events, ESD protection for T/R switch is installed on the antenna port (ANT) of the circuit is an effective and efficient way to deal with the ESD threat. The Conventional dual-diode ESD protection design for T/R switch which consists of two ESD diodes D1 and D2 and a power-rail ESD clamp circuit is drawn in Fig. 4.2.

In positive-to-VDD (PD) and negative-to-VSS (NS) testing mode, the ESD current is discharged through the forward biased diode D1 and D2. As for positive-to-VSS (PS) and negative-to-VDD (ND) mode, the ESD current will be discharged from the combination of diode and the power-rail ESD clamp circuit. The operation mechanism of the power-rail ESD clamp circuit has been described in section 2.3.2. With the proper RC time constant 100-ns, the RC-invertor detection circuit can distinguish the ESD stress and turn on the M_{ESD} right away.

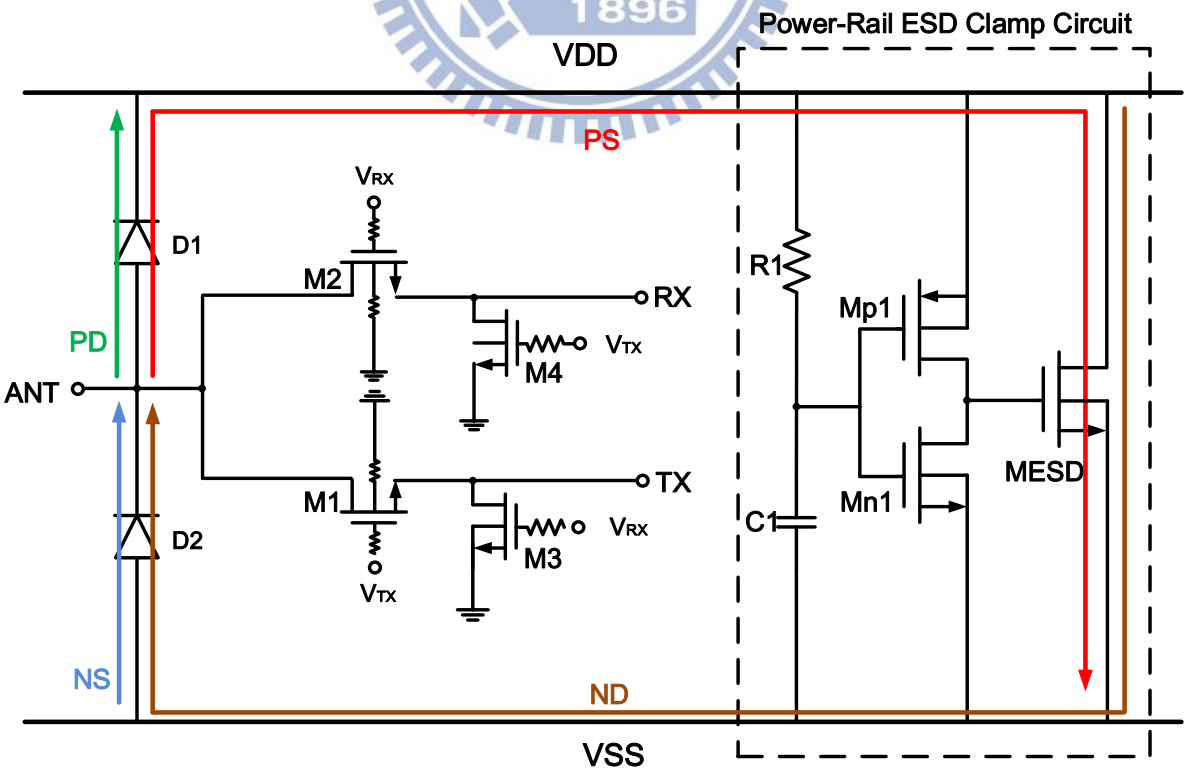


Fig. 4.2. Conventional T/R switch with traditional dual-diode ESD protection circuit.

The silicon implementation of the conventional ESD protection design is fabricated in a 90-nm 1P9M CMOS process. The silicon layout view of the T/R switch with conventional ESD protection design is illustrated in Fig. 4.3. Using the common centroid layout method, the series transistor M1, M2 are placed in the center and shunt transistors M3, M4 are set in the corner. The ESD diodes are inserted between the series and shunt transistors. The dimension of each single ESD diode D1 and D2 is 14μm*1μm, with junction area 28μm^2 in total. Finally, the dimension W/L ratio of the transistors Mp1, Mn1, and M_{ESD} in the power-rail ESD clamp circuit is 300/0.35 (μm), 100/0.35 (μm) and 3000/0.35 (μm), respectively. The layout of the power-rail ESD clamp circuit is drawn with the recommended ESD rules given from the foundry.

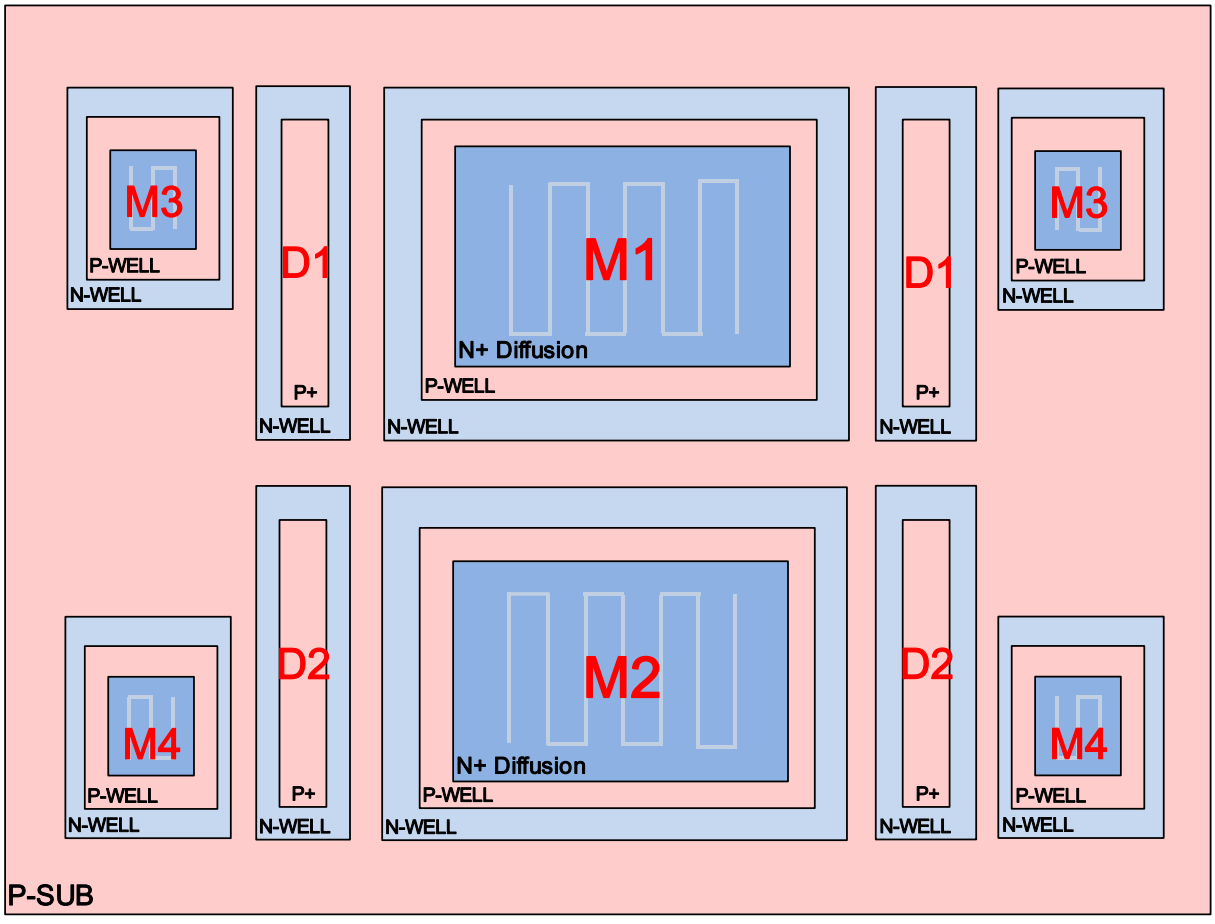


Fig. 4.3. Layout top view of the conventional dual-diode ESD protection for T/R switch with ESD diode D1 and D2.

4.3 Proposed ESD Protection Design for Conventional T/R Switch

The weak point of the conventional ESD protection design for T/R switch is described in section 2.4.2. Positive-to-VSS (PS) ESD testing event is the worst case of all the testing modes due to the all-NMOS structure of the T/R switch. Thus, the T/R switch circuit needs customized ESD strategy to enhance the ESD reliability of PS-mode.

In order to strengthen the robustness on PS-mode, the proposed ESD protection design utilized four silicon-controlled rectifiers (SCR1 ~ SCR4) as ESD protection devices which are constructed by the ESD diode D1 and the shunt transistors M3 and M4. Since the SCRs are formed naturally by the originally existing devices in the conventional ESD protection design, they are regarded as "embedded SCRs" in the silicon. Similar to the ESD dual-diodes, the embedded SCRs are installed next to the antenna port. In this way, the embedded SCRs can discharge the ESD current as soon as possible during the PS-mode ESD event. Fig. 4.4 shows the schematic of the proposed ESD protection design for T/R switch with embedded SCRs.

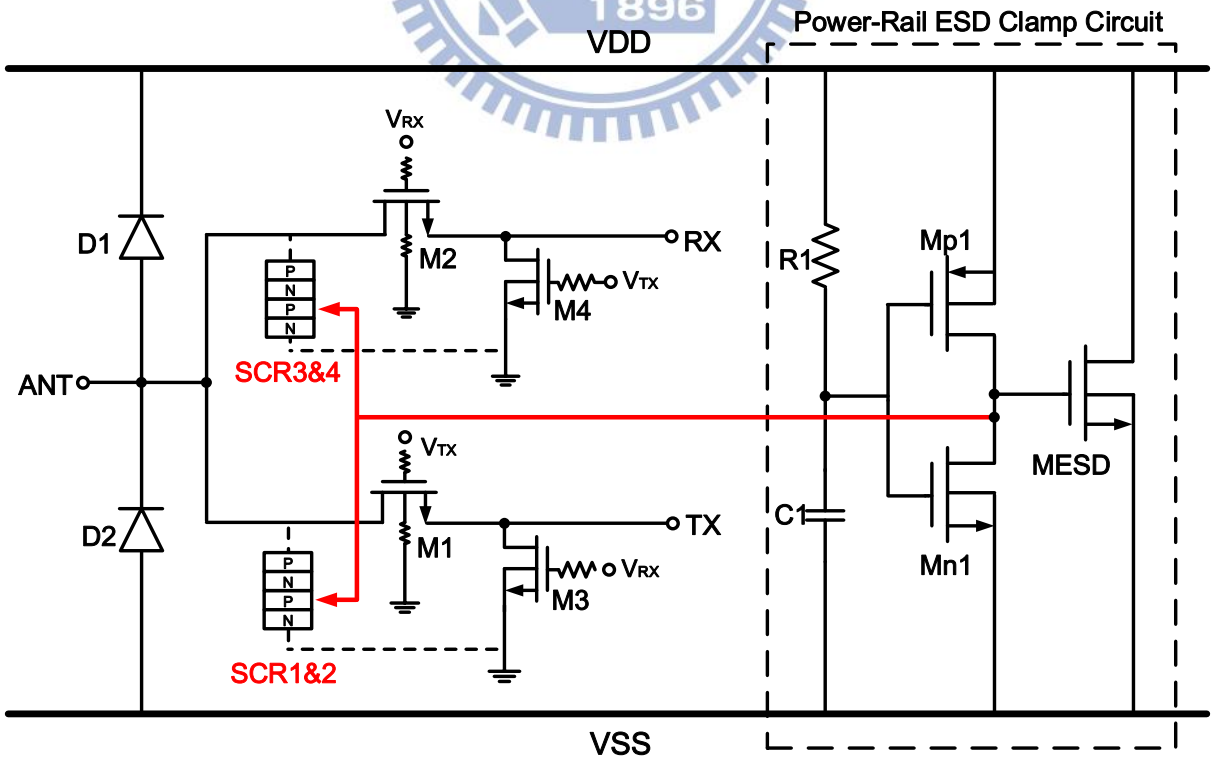


Fig. 4.4. Proposed ESD protection design for T/R switch with embedded SCRs.

As introduced in section 2.4.3, the turn-on voltage of a silicon-controlled rectifier without triggering is determined by the junction breakdown voltage between NW/PW and is usually higher than the oxide breakdown voltage of the inner circuit. The embedded SCRs need proper trigger method to lower the turn-on the ESD device rapidly. In the proposed design, the embedded SCRs are triggered by the power-rail ESD clamp circuit. The triggering mechanism is sketched as the red arrow in Fig. 4.5. When PS-mode ESD strikes on the ANT node, the ESD transient will wake the RC-invertor detection circuit and charge the gate of M_{ESD} to logic high. In this work, by connecting the gate of the M_{ESD} and the P-Well of the shunt transistors M3 and M4, the power-rail ESD clamp can rise the voltage potential simultaneously in the PS-mode ESD event. With the voltage potential rising in the P-Well, the bipolar junction transistor Q_{NPN} will be activated once the voltage drop on the $R_{P\text{-}Well}$ exceeds the turn-on voltage of the Q_{NPN} and start the positive feedback to discharge the ESD current. As a result, the ESD current in PS-mode can be discharged not only by the M_{ESD} but also the additional path of embedded SCRs.

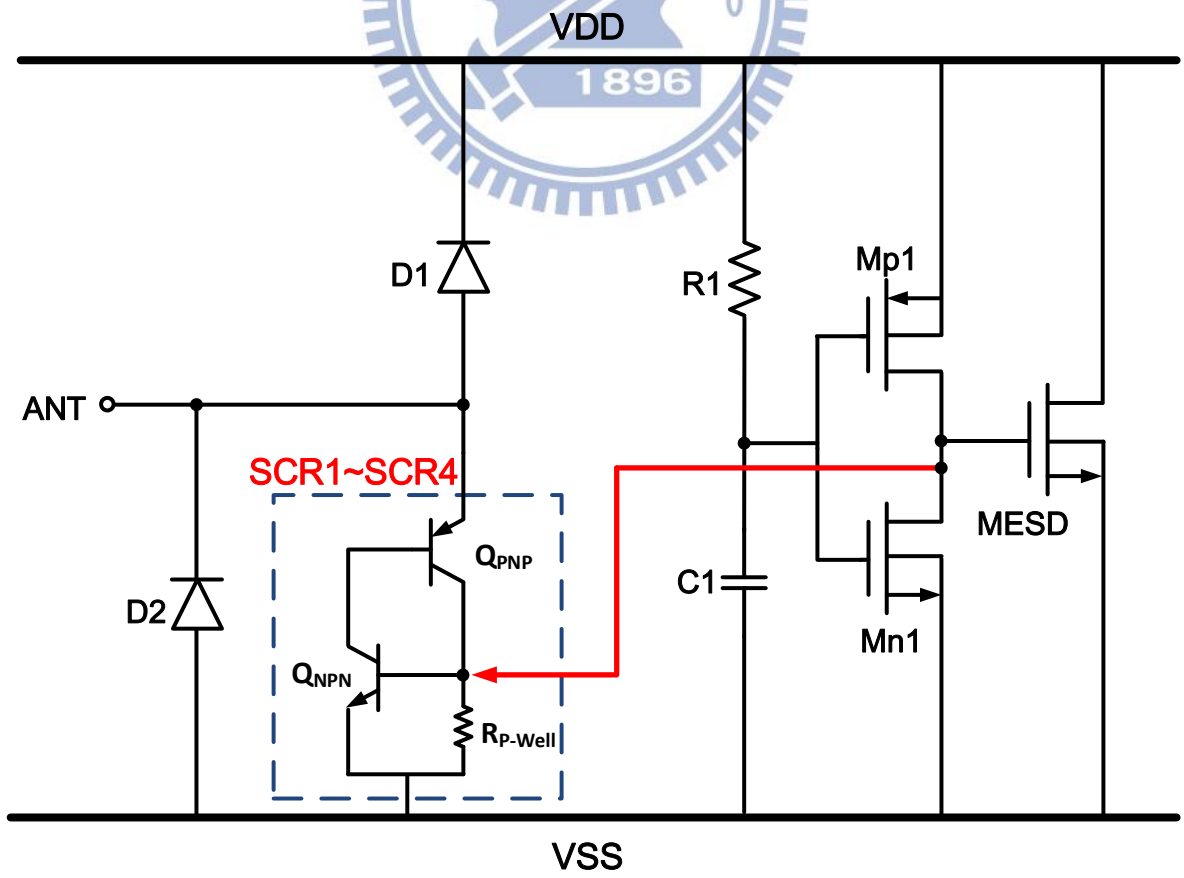


Fig. 4.5. The equivalent triggering mechanism of the proposed ESD protection design.

The silicon layout view is illustrated in Fig. 4.6. The location of the transistors M1~M4 is implemented as same as the conventional ESD protection design with common centroid method. The ESD diode D1 is divided into four parts and combined with the shunt transistors M3, M4. By this layout skill, the four embedded SCRs can be constructed by the parasitic path in the silicon front-end of line intrinsically. The proposed ESD protection design forms an additional discharging path for PS-mode ESD current without any extra layout device.

For the purpose of comparing to the conventional ESD protection design, the dimension of a single diode D1 is 7μm*1μm. Total junction area of the diode D1 is 28μm^2, which is equal to the conventional ESD protection design in section 4.2. On the other hand, the ESD diode D2 is hanged outside the Fig. 4.6, with 28μm^2 junction area in total. The power-rail ESD clamp in the proposed ESD protection design is same as the conventional ESD protection design, too.

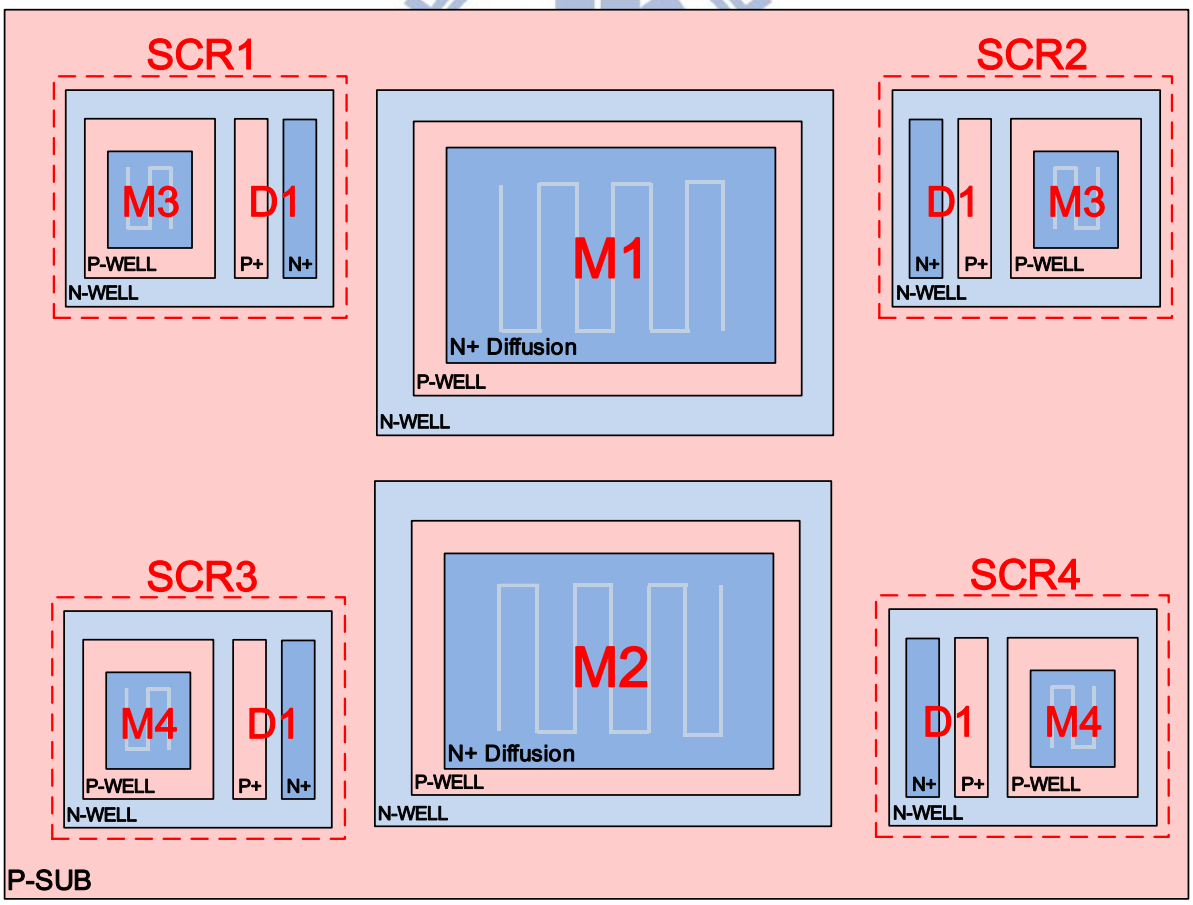
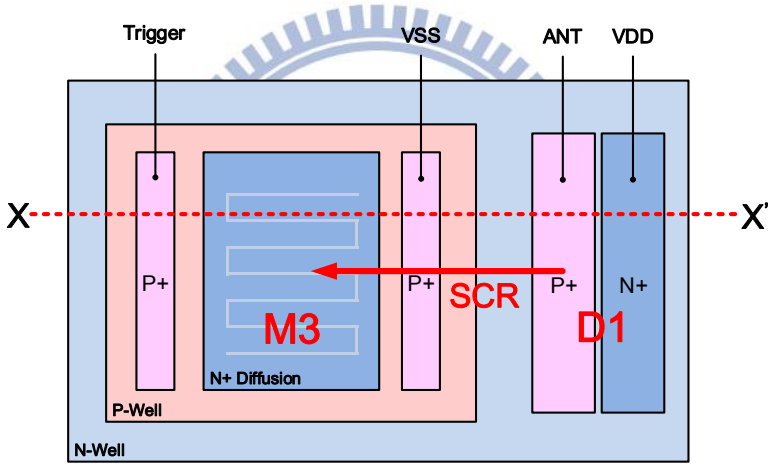
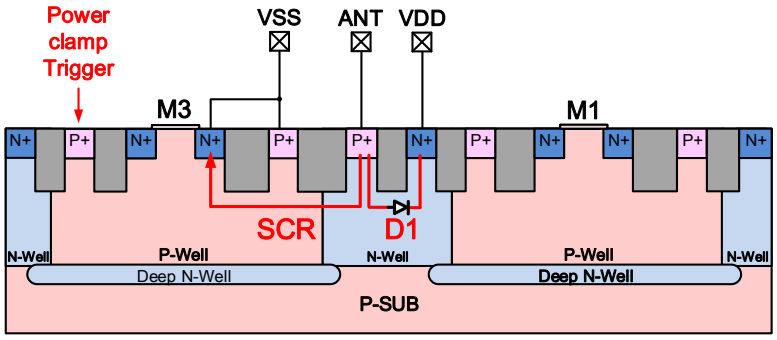


Fig. 4.6. Layout top view of the proposed ESD protection design for T/R switch with embedded SCRs (SCR1~SCR4) and diode D1.

A closer look at a single embedded SCR (constructed by D1 and M3 for example) from Fig. 4.6 is sketched in Fig. 4.7(a) and Fig. 4.7(b). The P-N-P-N path goes from the P+ diffusion of the diode D1, N-Well, P-Well, and the N+ diffusion of the transistor M3 in order. As we can see, the embedded SCR shares the same P+ diffusion area with the ESD diode D1. The fewer ESD device layouts, the less parasitic capacitance. The proposed ESD design can enhance the PS-mode robustness of the T/R switch with little RF degradation. In normal circuit operations, the triggering signal will be zero, so the body of the shunt NMOS M3 (M4) is grounded properly. Under the PS-mode ESD event, the triggering signal from the power-rail ESD clamp circuit will be injected into the P-Well of the shunt transistors M3 (M4) and trigger on the embedded SCRs.



(a)



(b)

Fig. 4.7. (a) Realization of the embedded SCR with the P+ anode of D1 and the N+ source of M3. (b) Cross-section view on X-X' line of Fig. 4.7(a) to show the path of SCR and diode D1.

4.4 Experimental Results of Conventional T/R Switch with Proposed ESD Protection Design

The testing chip is fabricated in a 90-nm CMOS process, with the area of 6 mm^2. Fig. 4.8 shows the whole chip photograph, which is taken at CIC, Hsinchu. The four circuit blocks in this shuttle includes T/R switch without ESD protection circuits, traditional dual-diodes ESD protection for T/R switch, proposed embedded SCRs ESD protection for T/R switch, and testkeys of the ESD devices. Besides the T/R switch, a low-noise amplifier serves as the inner circuit which is connected to the RX node of the T/R switch.

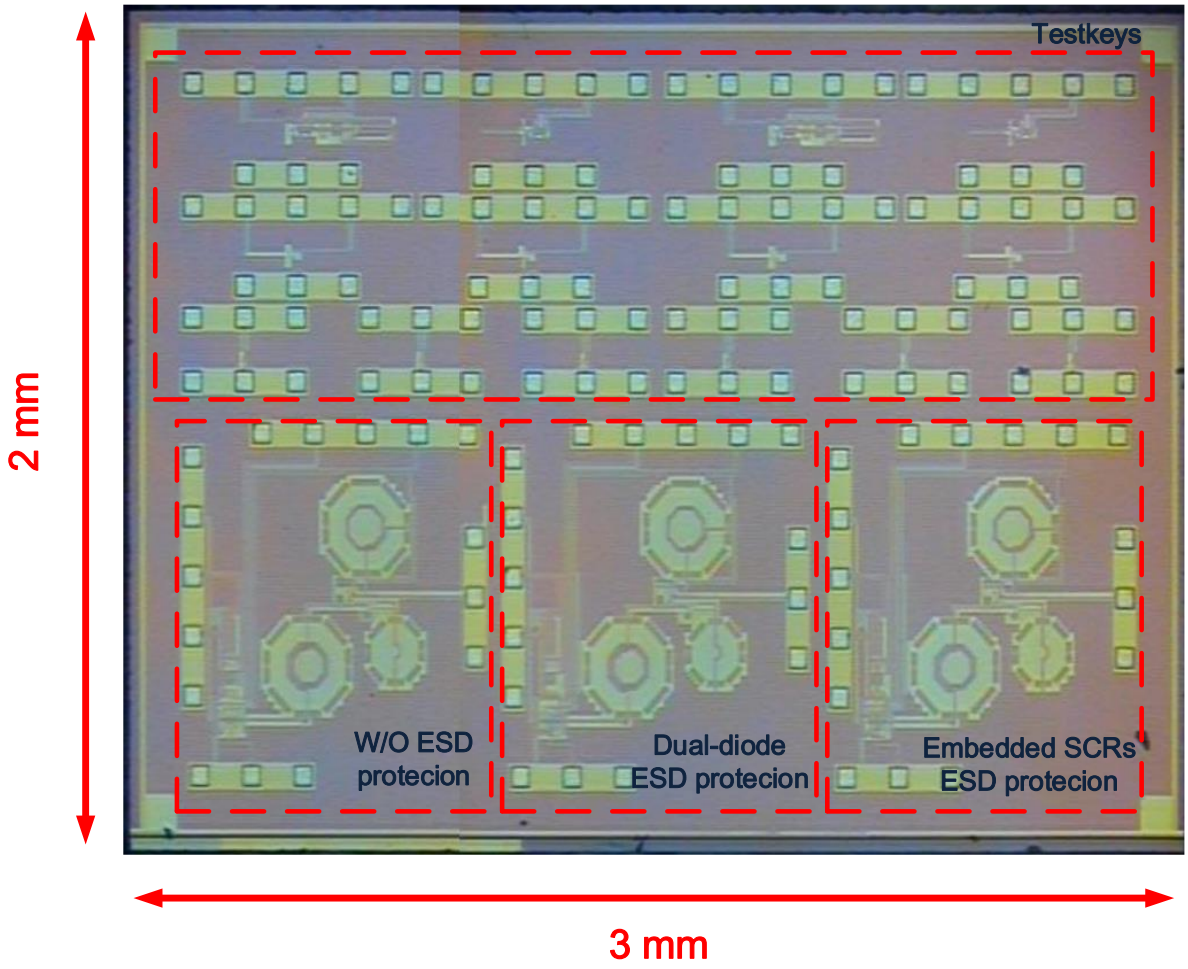


Fig. 4.8. The chip photo of T/R switch without ESD protection, T/R switch with traditional dual-diodes ESD protection, T/R switch with embedded SCRs ESD protection, and testkeys.

4.4.1 ESD Levels Measured with ESD HBM Tester and TLP System

The human-body model level is a commonly used ESD testing that represents the robustness of the certain circuits. In this thesis, the HBM tests are zapped on the interested pin of the IC by using the HCE-5000 ESD tester (Fig. 4.9(a)), including the four ESD conditions: PS-mode, PD-mode, NS-mode, and ND-mode. The result of HBM tests is arranged in Table 4.1. Besides the HBM tester, the transmission line pulse (TLP) system, HED-T5000 (Fig. 4.9(b)), which can generated high voltage and high current simultaneously is employed to analyze the characteristics of the ESD device.

(a) (b)

Fig. 4.9. (a) ESD tester for human-body model and (b) TLP system.

Table 4.1

Measured HBM ESD levels by HBM tester.

	PS (kV)	PD (kV)	NS (kV)	ND (kV)
Without ESD Protection Design	0.5	0.5	0.5	0.5
Conventional ESD Protection Design	2.3	2.4	2.7	2.8
Proposed ESD Protection Design	2.4	2.4	1.7	1.7

Table 4.2

Measured failure current (It2) by TLP systems.

	PS (A)	PD (A)	NS (A)	ND (A)
Conventional ESD Protection Design	1.24	1.23	1.46	1.6
Proposed ESD Protection Design	1.63	1.2	0.89	1.22

From the experiment result in table 4.1 and table 4.2, the ESD robustness on PS-mode of proposed ESD design is 2.4kV better than the conventional ESD protection design of 2.3kV. The failure current I_{t2} in PS-mode of the proposed ESD protection design is 1.63A, which is higher than the conventional ESD protection design of 1.24A, too.

Fig. 4.10 shows the TLP characteristics of PS-mode on the two ESD protection designs. The turn-on resistance Ron of the conventional and proposed ESD protection design is 5.5 ohm and 3.5ohm, respectively. A lower Ron indicates the proposed ESD protection design can achieve a higher ESD robustness than conventional ESD protection design.

An enlarged TLP I-V curve of Fig. 4.10 is shown in Fig. 4.11. In this graph, the unique snapback phenomenon of silicon-controlled rectifier can be observed. The snapback phenomenon states the evidence that the SCR device is turned on properly in the PS-mode ESD event. The embedded SCR had been triggered on at 1.7V as expected to discharge the ESD current. And with the additional discharging path of the embedded SCRs, the Ron are pulled down successfully.

The reason that ESD robustness of NS mode and ND mode in the proposed ESD protection design are worse than the conventional ESD protection design can be seen in the layout view in Fig. 4.12. The metal line which connects the anode of the ESD diode D2 and the ground are too thin to discharge the large amount of ESD current. The mistake of the metal connection makes the proposed ESD protection on both NS and ND mode into failure earlier than expected.

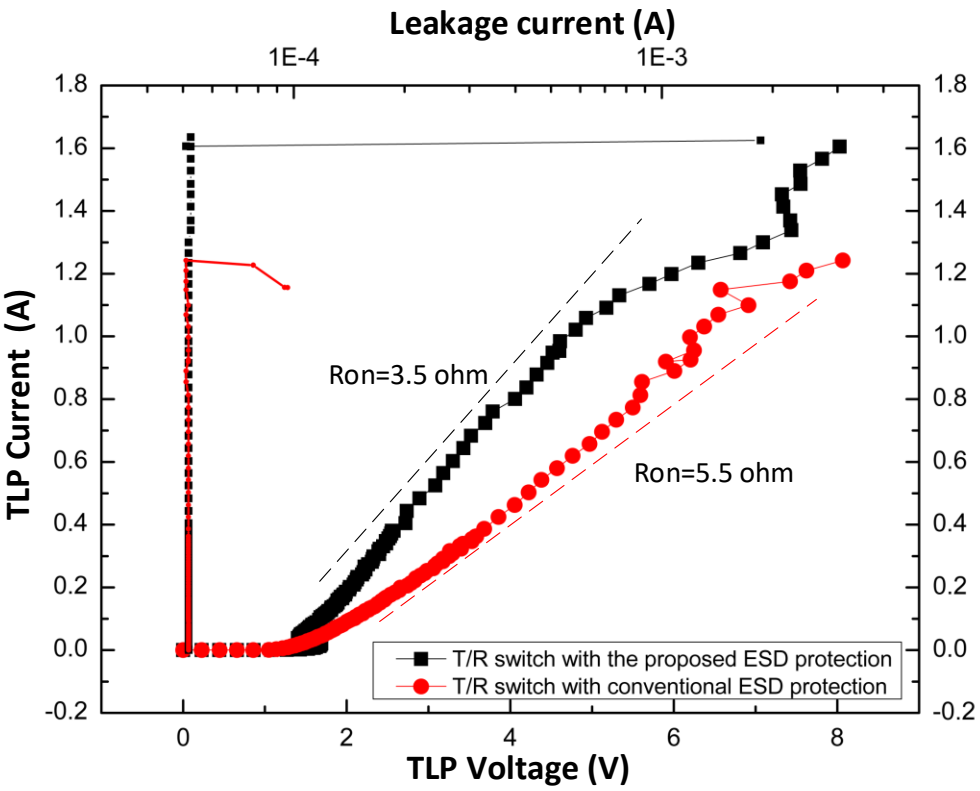


Fig. 4.10. TLP- measured I-V characteristics of the T/R switch on PS-mode with different ESD protection designs.

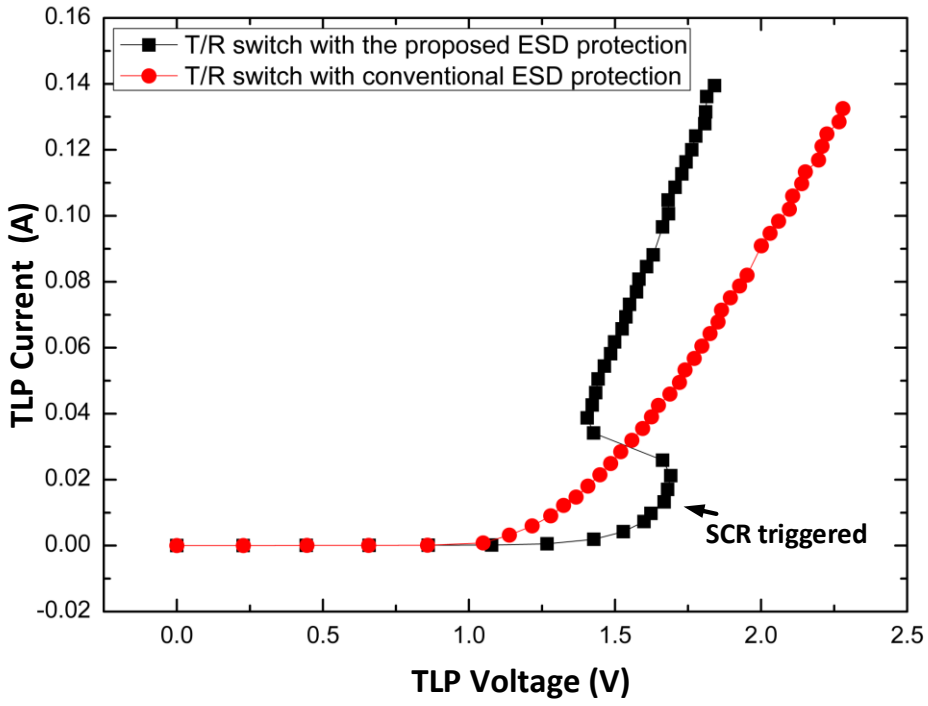


Fig. 4.11. Enlarged TLP I-V curves from Fig. 4.10 to show the snapback phenomenon on the embedded SCRs.

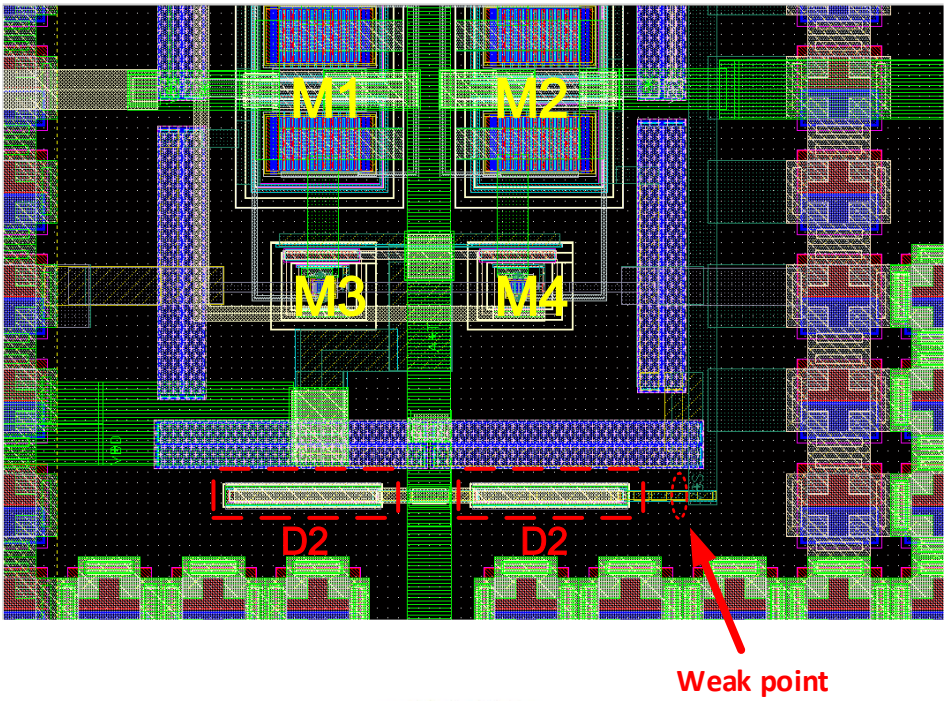


Fig. 4.12. The weak point in the layout of the proposed ESD protection design to explain the lower NS and ND mode ESD levels than the conventional ESD protection design.

4.4.2 Extracted Parasitic Capacitance after De-embedding Method

Fig. 4.13 illustrates the concept of de-embedding method to extract the parasitic capacitance of the device under test. The parasitic capacitance of the ESD protection device is a severe issue in high-speed I/O and RFICs. When it comes to measure the parasitic capacitance of the ESD protection device, the de-embedding method [28] is applied in order to excluding the parasitic effect of the PADs. By measuring the scattering parameters matrix [S] of the DUT with PADs, and the PADs under short, open, load, and through (SOLT) calibrations, [S'], the accurate capacitance of the DUT can be calculated by EDA software. In Fig. 4.14, the parasitic capacitance of the stand-alone single diode and embedded SCR (normalized to its layout area) are extracted at wide RF frequency bands. The parasitic capacitance per μm^2 of the conventional diode and embedded SCR are 2.92fF and 0.59fF, respectively. The p-n-p-n structure of SCR intrinsically contributes less capacitance than the conventional p-n diode does. With smaller capacitance, the RF performance degraded by the embedded SCR can be minimized.

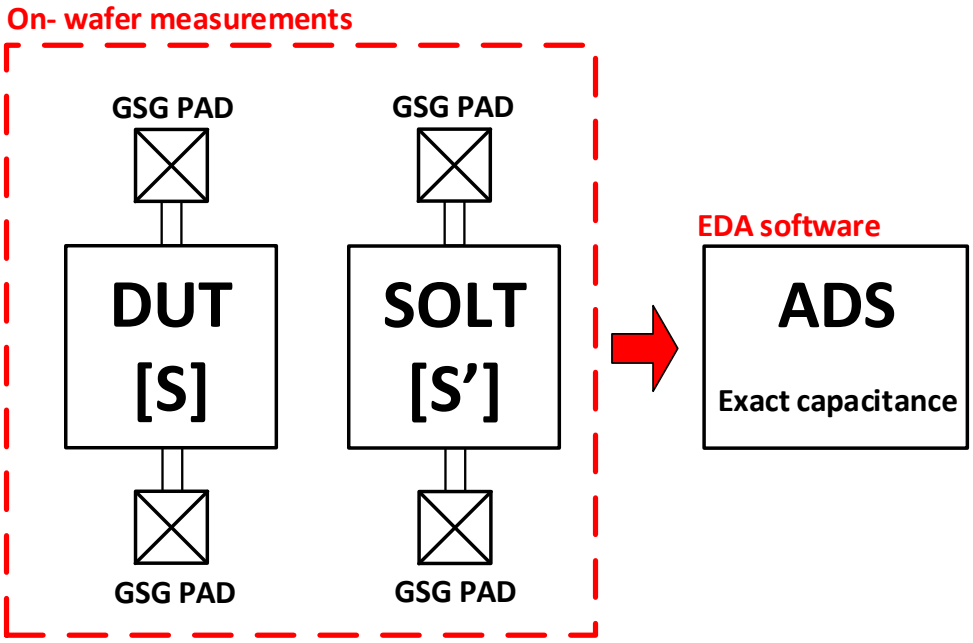


Fig. 4.13. Scattering matrixes are measured under different conditions and calculated in EDA tool to exclude the effect of the pads.

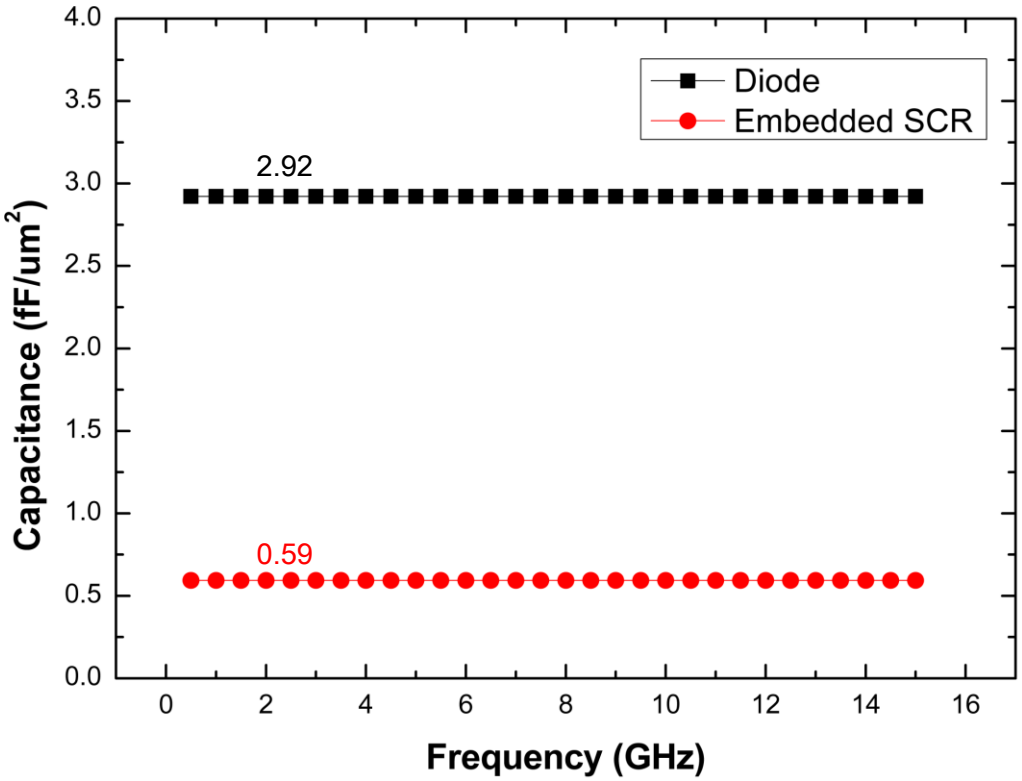


Fig. 4.14. Normalized parasitic capacitance of the stand-alone diode and embedded SCR.

4.4.3 Failure Analysis and Discussion

To demonstrate the proposed ESD protection is more suitable than the conventional ESD protection design on PS-mode ESD strikes, failure analyses (FA) are done by the scanning electron microscope (SEM) to show the front-end of line (FEOL) situation after the PS-mode ESD tests. The SEM photo of whole silicon chip after total-delayer procedure to remove the metal layers in back-end of line (BEOL) is shown in Fig. 4.15.

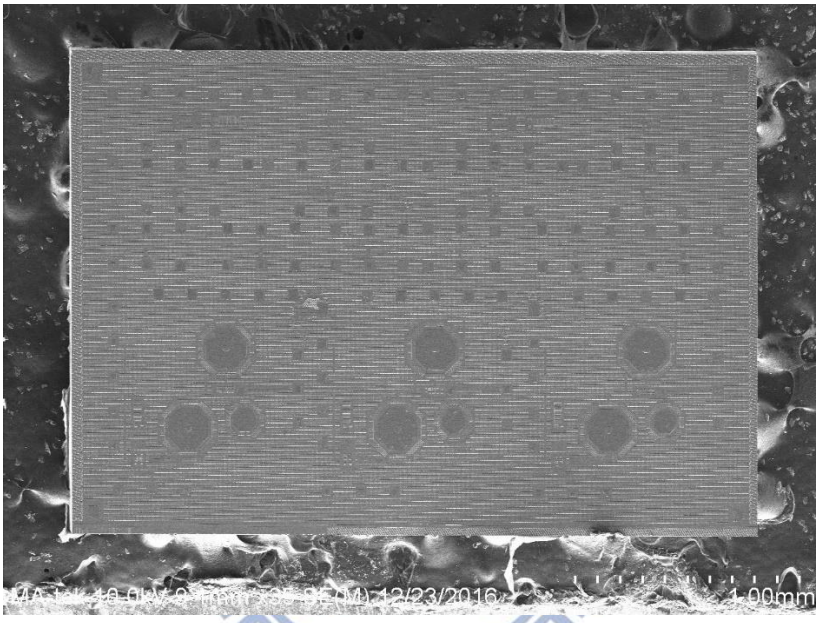
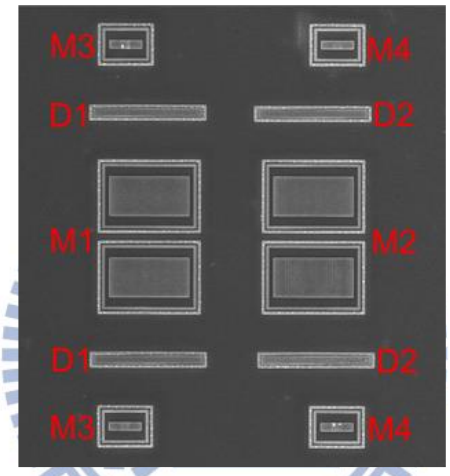


Fig. 4.15. SEM photo after the total-delayer procedure.

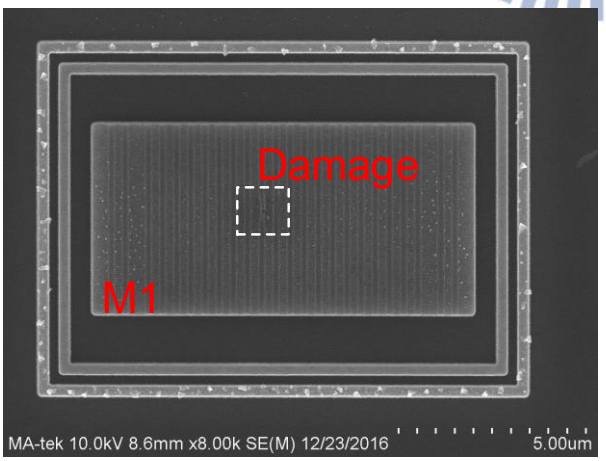
Scanning electron microscope photos of the conventional ESD protection circuit after PS-mode 2.3kV HBM testing on ANT node are shown in Fig. 4.16(a). The failure location is found at the transistors M1 and M2, as shown in Fig. 4.16(b) and Fig. 4.16(c). Transistors M1 and M2 are damaged, but ESD damage was not on the diodes D1 or D2. This indicates that the conventional ESD dual diodes are not sufficient enough to protect the T/R switch under the PS-mode ESD event because the transistors are broken before the ESD protection devices.

Fig. 4.17(a) shows the SEM photos of the proposed ESD protection design after PS-mode 2.4kV HBM stress. The failure sites are located at the embedded SCRs and the transistors M1 and M2 are not damaged at all, which is different from that with the conventional ESD protection design. Damaged spots on SCR1 ~ SCR4 are shown in Fig. 4.17(b) ~ Fig. 4.17(e),

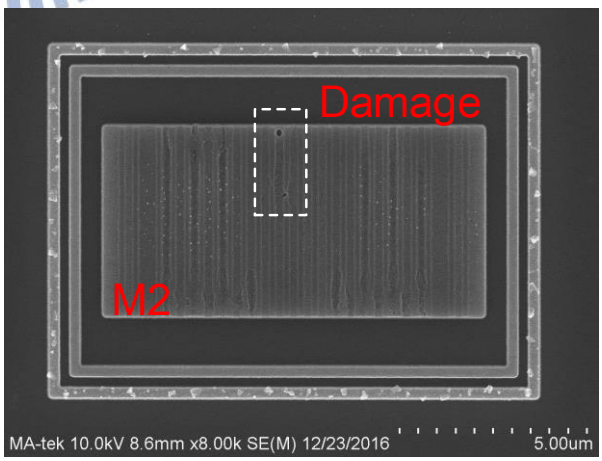
respectively. Fig. 4.18(a) ~ Fig. 4.18(e) present the each embedded SCRs after TLP PS-mode tests, the damage is located only at the embedded SCRs, too. The significant burned-out marks indicate the ESD current flow which is discharged from ANT node to VSS by all of the embedded SCRs. Those embedded SCRs are simultaneously triggered on by the driver in the power-rail ESD clamp circuit when ESD event is detected. In this work, the embedded SCRs are found to be the first elements damaged in the proposed ESD protection design under the PS-mode ESD stress. It means that the inner circuits can be really protected by the proposed ESD protection design with embedded SCRs.



(a)

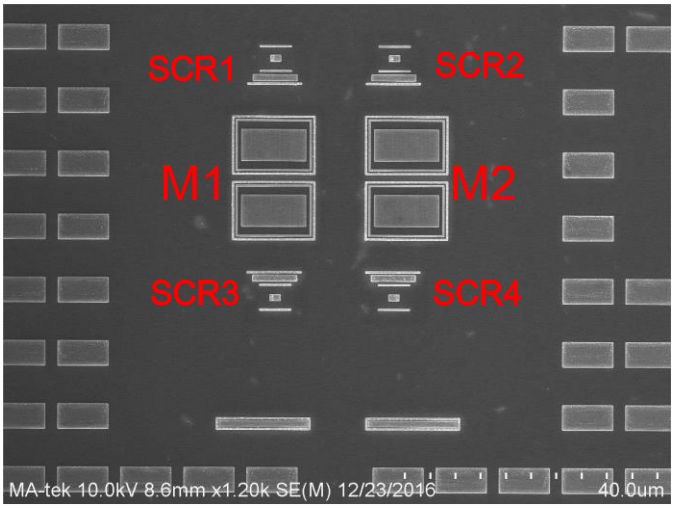


(b)

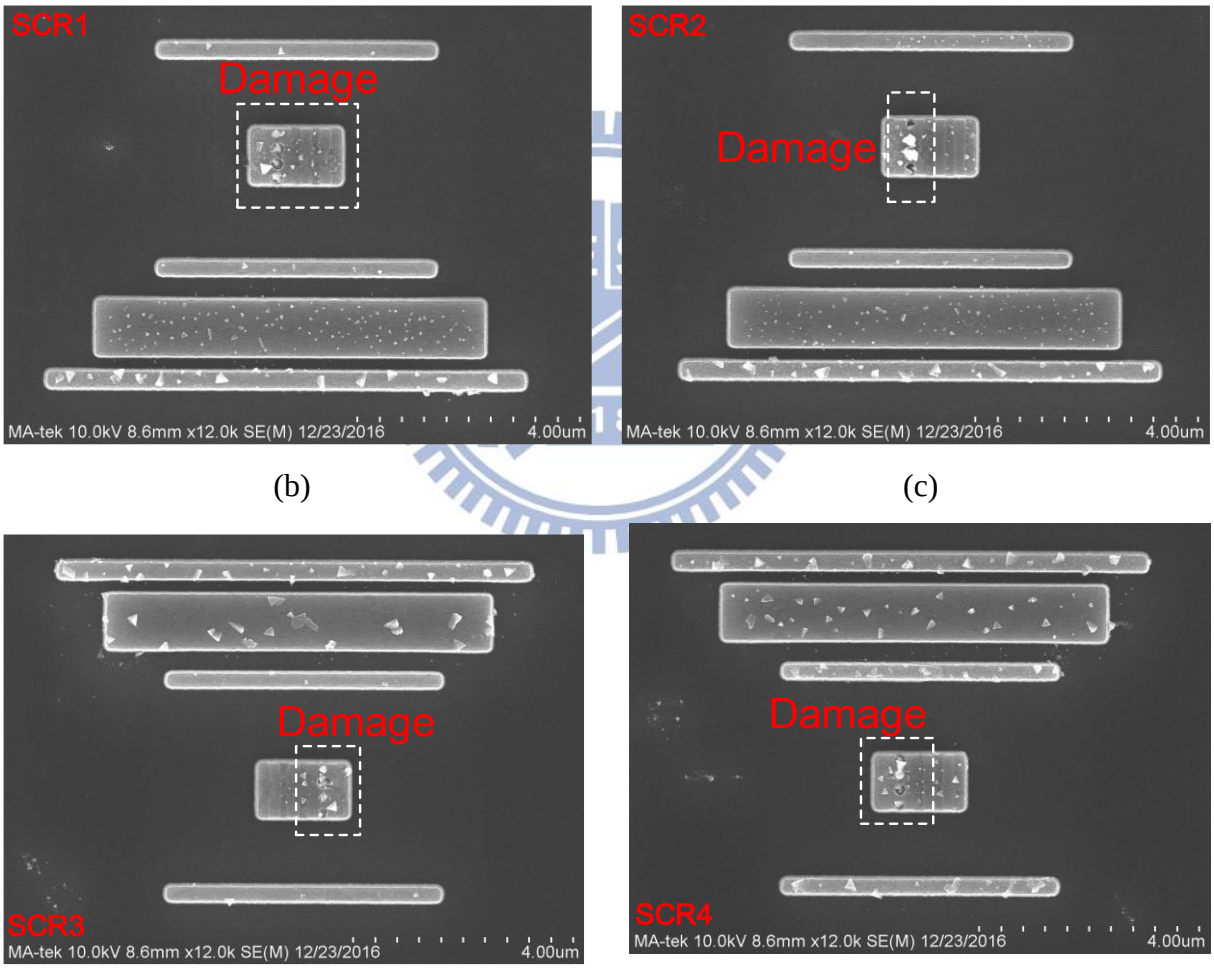


(c)

Fig. 4.16. (a) SEM photos of conventional ESD protection for T/R switch after 2.3kV HBM PS-mode ESD test. Enlarged photos on (b) M1 and (c) M2 from Fig. 4.16(a).



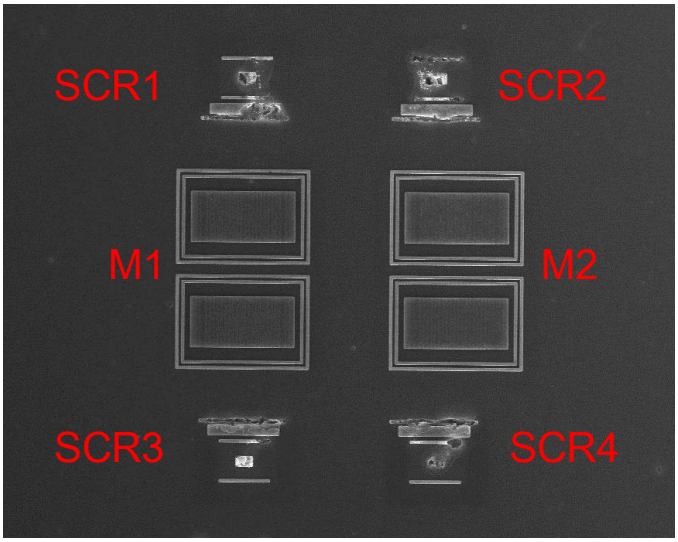
(a)



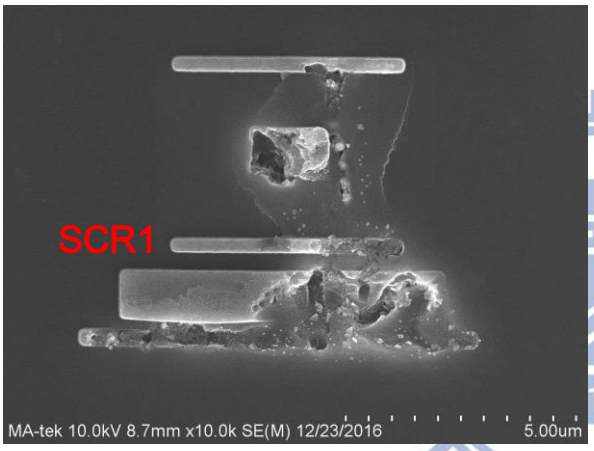
(b) (c)

(d) (e)

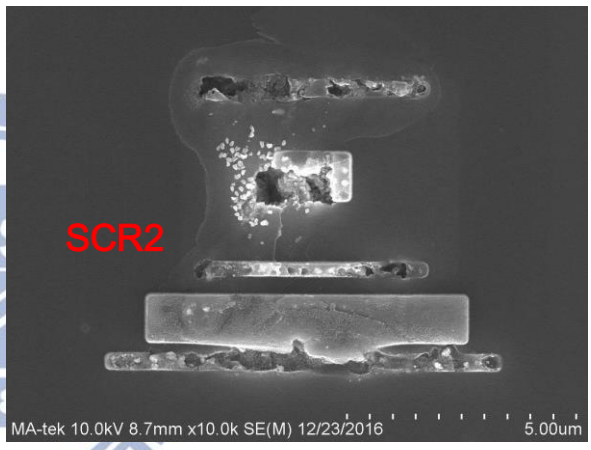
Fig. 4.17. (a) SEM photos of proposed ESD protection design for T/R switch after HBM 2.4kV PS-mode ESD test. Enlarged SEM photos from Fig. 4.17(a) to see the damage on (b) SCR1, (c) SCR2, (d) SCR3, and (e) SCR4.



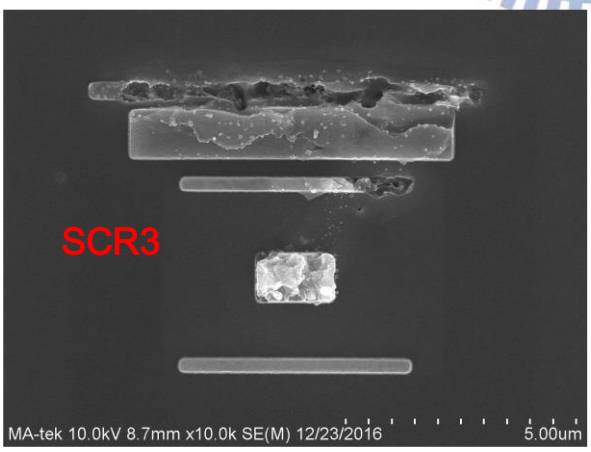
(a)



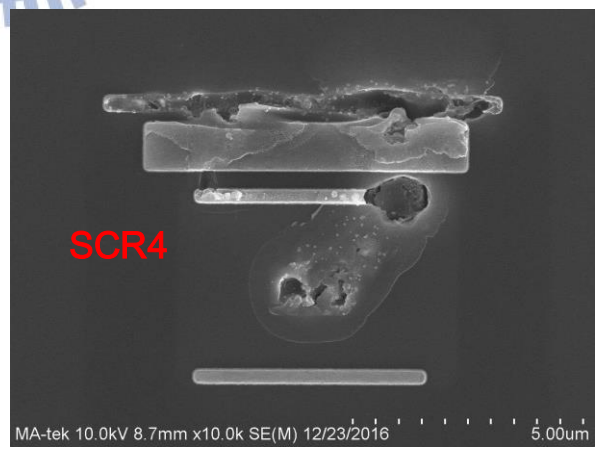
(b)



(c)



(d)



(e)

Fig. 4.18. (a) SEM photos of proposed ESD protection design for T/R switch after 1.6A of TLP ESD stress on PS-mode. Enlarged SEM photos from Fig. 4.18(a) to see the damage on (b) SCR1, (c) SCR2, (d) SCR3, and (e) SCR4.

4.5 Summary

The PS-mode ESD characteristics are arranged in Table 4.3. The total parasitic capacitance of the proposed ESD protection design seen at ANT port is slightly larger than the conventional ESD protection design because of the embedded SCR path. However, the Ron of the proposed ESD design is much better than the conventional design and the product of the Ron and C_{total} is smaller, too. The proposed ESD protection design does not utilize any additional ESD protection layout but can enhance the ESD robustness in PS-mode by embedded SCRs which are formed by the layout skills. The proposed ESD protection design can achieve the failure current I_{t2} to about 1.6A and HBM level 2.4kV, which is higher than the 1.2A and HBM level 2.3kV of the conventional ESD protection design. After the de-embedding methods were applied, the embedded SCR contributed less capacitance than the conventional diode. At last, the failure analyses have shown that the conventional ESD protection design is not sufficient for the T/R switch circuit. The proposed ESD protection design targeting to the PS-mode can be a suitable protection to deal with the weakest point on PS-mode of conventional T/R switch.

Table 4.3

Comparison of ESD characteristics on PS-mode.

	Conventional ESD Protection Design	Proposed ESD Protection Design
It_2 (A)	1.24	1.63
HBM (kV)	2.3	2.4
Ron (Ω)	5.5	3.5
Normalized Capacitance of diode/SCR (fF/um^2)	2.92	0.59
Total parasitic capacitance seen at ANT port (fF)	163.52	180.04
Ron*C_{total} (Ω*fF)	899.36	630.14
FOM (mA/fF)	7.58	9.05

Chapter 5
Conclusions and Future Work

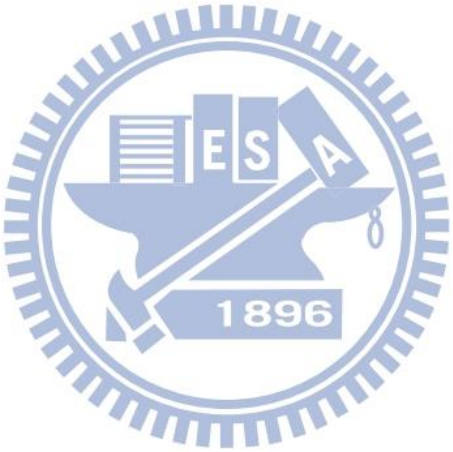
5.1 Conclusions

In this thesis, issues of ESD protection designs in RFIC are introduced, especially the obstacles which is encountered in the T/R switch circuit. The insertion loss and the linearity are two major concerns of the T/R switch. The ESD protection design which introduces less capacitance will be appreciated.

In the first part of the thesis, the challenges of ESD protection design for high-power T/R switch is presented. Unlike the conventional T/R switch, the large AC voltage swing of the transmit signal will mis-trigger the traditional ESD device. The proposed type 1 and type 2 ESD protection design employ an ESD transient detection circuit to distinguish the ESD transients and the RF signal. The ESD transient detection circuit can turn on the transistors in RX branch to discharge the current when the PS-mode ESD strikes. From the experimental results, the PS-mode HBM ESD robustness of the high-power T/R switch with type 1 and type 2 ESD protection design can achieve 3.75kV and 4.5kV, with a slightly insertion loss degradation of 0.2dB ~ 0.5dB. In addition, the NS-mode HBM levels for the T/R switches are better than the PS-mode. Although the power handling capability of the high-power T/R switch can reach 28.6dBm, after the ESD protection designs are installed, the P_{1dB} are degraded 3dBm ~ 5dBm. The ESD protection designs still have room for improvement which focus on the linearity performance of the T/R switch.

In the second part of the thesis, the PS-mode ESD threat is demonstrated to be the weakest point among the four ESD testing modes. The traditional ESD protection design are not

sufficient enough for PS-mode ESD attacks. The proposed ESD protection design utilized an area-efficient SCR device is embedded in the conventional series-shunt T/R switch to deal with the PS-mode ESD event. The test chip is fabricated in a 90-nm CMOS process. With layout skills, the additional embedded SCRs are formed in the parasitic path of the shunt transistors and diode D1 which are already existing in the traditional whole-chip ESD protection scheme. Experimental results show that the HBM robustness of the ESD protection design with embedded SCR for conventional T/R switch is improved from 2.3kV to 2.4kV and the failure current I_{t2} is enhanced from 1.2A to 1.6A. In addition, after the de-embedding method, the measured parasitic capacitance of the embedded SCR is less than the traditional ESD diode. The embedded SCR is a suitable ESD protection method for conventional T/R switch.



5.2 Future Work

5.2.1 Improvement of the Power Handling Capability of the T/R switch

According to the experimental results in this thesis, the P_{1dB} of the high-power T/R switch with ESD protection design is degraded. It indicates that the ESD transient detection circuit of the design are not strong enough the block the large AC signal of TX away from the discharging path of RX, as shown in Fig. 5.1. The leakage power will affect the transient detection circuit to turn on the off-state RX transistors and cause the power of the transmit signal to degrade. Stand in the perspective of optimization, since the HBM robustness has already meet the specifications of 2kV, the dimension of the ESD transient detection circuit can be smaller. With a smaller size of the transistor, the Ron will be increased. The ESD transient detection circuit can block the RF signal more effectively. Similarly, increase the number of the stacked transistors of the transient detection circuit can do the same effect, too. However, the optimizations need testkeys to verify their ESD robustness and the RF performance.

On the other hand, the ESD discharging path is selected on the RX branch because the RX branch owns a shorter discharging path compare to the TX branch in the proposed ESD protection design. However, the experimental results have shown that the ESD robustness of the design is good enough for 2kV HBM. Another point of view is to install the ESD transient detection circuit on the TX branch of the T/R switch. The schematic is sketched in Fig. 5.2. In this way, the transmitting signal from TX shall not leak to the RX port.

Finally, the composition of the ESD transient detection circuit can be selected as different devices, such as inductor. An inductor can be a resistive element that block the RF signal away in high-frequencies, whereas the ESD transients can be seen as DC pulses and pass through it.

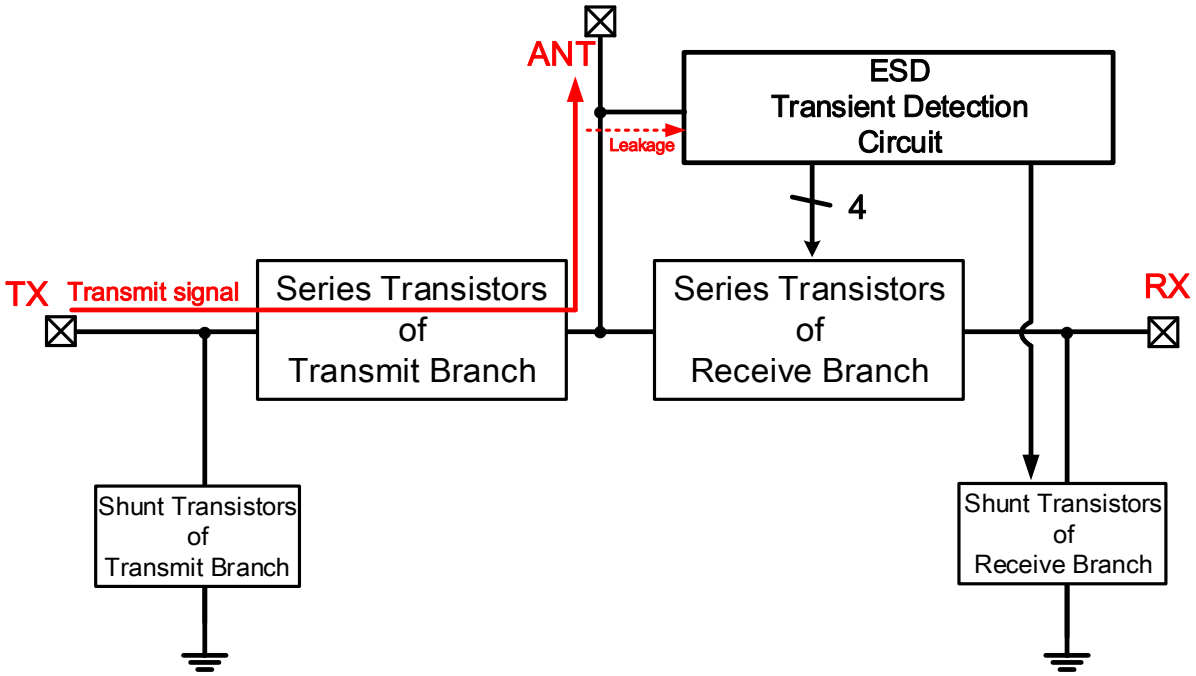


Fig. 5.1. The power leaks to ESD transient detection circuit and cause the degradation of P_{1dB}.

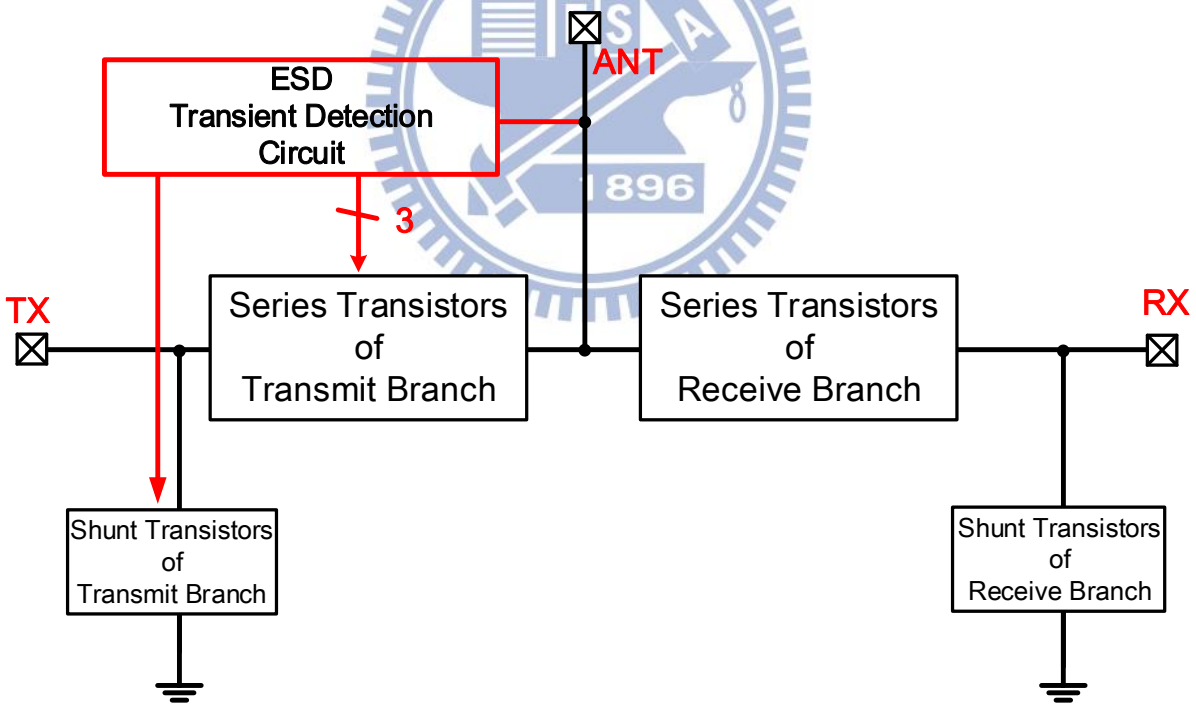
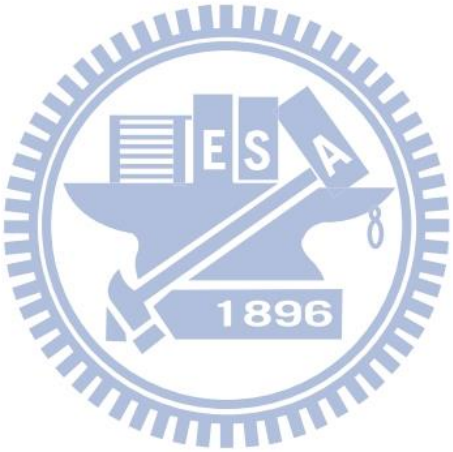


Fig. 5.2. High-power T/R switch with ESD transient detection circuit installed in TX branch.

5.2.2 *ESD Protection Design for Different T/R Switches*

The proposed type 1 ESD protection design for a single-pole double-throw high-power T/R switch is presented in the thesis. The insertion loss, return loss, and isolation are slightly affected by the ESD detection circuit. The proposed ESD protection design can be utilized to T/R switches which operate in extremely high frequencies, since the demanded power handling capability is not as high as the applications of GSM and WCDMA. Several T/R switches in 50–70GHz [30], 60GHz [31], 50–94GHz [32] have been implemented in CMOS process to control the millimeter-wave (MMW) signals for higher data rate in wireless communications. However, to the best of the author's knowledge, ESD protection design co-designed with the T/R switches in extremely high frequency has not been reported.



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