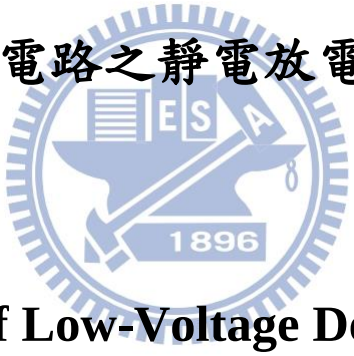
# 國立交通大學

電子工程學系　電子研究所碩士班

碩　士　論　文

## 使用低壓元件堆疊來達成
## 高壓積體電路之靜電放電防護設計



## Stacks of Low-Voltage Devices for
## ESD Protection in High-Voltage Applications

研 究 生：湯凱能　　(Kai-Neng Tang)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國一〇三年九月

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碩士論文

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中華民國一〇三年九月

# 使用低壓元件堆疊來達成
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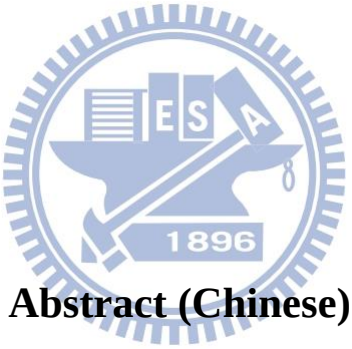

## Abstract (Chinese)

在現今的電子產品中，許多積體電路都是使用高壓相關製程的，例如各式平板的驅動 IC，電源管理 IC，車用 IC 等。在高壓製程中，高壓電晶體往往具有比較複雜的結構，來撐高崩潰電壓，增加可操作的電壓區間，這也使得靜電放電保護的設計，更加有挑戰性。

在高壓的靜電放電防護設計中，常會使用橫向擴散電晶體(lateral diffused MOS, LDMOS)，也就是常見的高壓電晶體，與低壓電晶體相比，在同樣的布局大小下，通常高壓靜電保護元件的靜電耐受度表現較差，所以使用高壓保護元件，都要撐大元件大小，並且注意均勻導通度，以達到要求的靜電耐受能力。

在高壓靜電放電防護設計中，持有電壓(holding voltage)是一個重要的考量，當在靜

電保護元件的持有電壓低於供給的電壓時，在應用上有可能會發生閂鎖效應(latchup)，在一些雜訊很多的環境中，這一點更是重要的考量。

相對於高壓靜電保護元件，低壓的靜電保護元件，往往都是充分驗證，而且有許多可行的方法增進其靜電耐受度，導通速度，導通均勻度。低壓的靜電保護元件，在單位面積下，靜電耐受能力很好。使用堆疊方法使整體的導通與持有電壓往上疊加，使它滿足高壓積體電路的需求，在面積與靜電耐受度的考量下，尋找最佳的方法。

在此篇論文中，實驗並驗證堆疊結構，並討論他們的問題以及改善方法，以及在不同形狀堆疊的情形。探討在堆疊中，擺放不同的元件，使其導通速度增加的方法。

# Stacks of Low-Voltage Devices for ESD Protection in High-Voltage Applications

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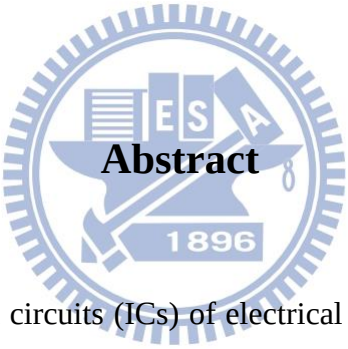

## Abstract

Nowadays, many integrated circuits (ICs) of electrical products are fabricated in a high-voltage process. For example, driver ICs for various display panels, power management ICs and automotive ICs are commonly fabricated in a HV process. In a high-voltage process, HV transistors are born with complicated structure for the increase of the operating range and breakdown voltage, and that makes electrostatic discharge (ESD) protection design more difficult and challenging.

In ESD protection design for HV applications, it is common to use lateral diffused MOS (LDMOS) as an ESD protection device. LDMOS is a general HV MOS, and its ESD robustness is worse than a low-voltage device's. It has to enlarge LDMOS, and be aware of uniformity for ESD protection.

In ESD protection design for HV applications, holding voltage of a device is an important

factor. When holding voltage of a device is lower than supply voltage, it is possible that latchup occurs in applications. In some noisy environment, this factor should be paid more attention.

Low-voltage devices are proved for good ESD robustness per area, and the devices can be enhanced by many methods. Stacking makes the devices' trigger voltage and holding voltage increase so that the devices meet the conditions for HV applications. For area and ESD robustness concerns, stacking can be one of the best ways.

In this thesis, stacks for ESD protection are implemented and verified, and it is discussed for the problems and improvement. Stacked configuration in different shapes is also examined. Increasing turn-on speed by replacing with other devices will be discussed.

# Acknowledgements

首先要感謝柯明道老師，在碩士班這兩年的教導，老師的反應很快，也很快掌握現今發展重點。在碩士班的一路上，老師一直在教導我們如何做研究，感謝老師的指導。與老師討論的過程，老師每次都能快速且精準地指出問題，並討論可能的解答，進而產生出很多不同的想法，真的很感謝老師！

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湯凱能

103 年 9 月於竹塹交大

# Contents

# List of Tables



# List of Figures

# Chapter 1
# Introduction

In this chapter, the motivation of this thesis is depicted first. The chapter shows the advantage of stacking in high-voltage (HV) applications. Electrostatic discharge (ESD) protection scheme reveals the typical arrangement for integrated circuits (ICs). It also introduces the concerns of ESD protection design and testing methods. Finally, thesis organization is included in the end of this chapter.

## 1.1 Motivation

Nowadays, more and more HV applications are flourished in commercial ICs such as power management ICs and display driver ICs. With development of HV technology, ESD protection in HV area should be provided for the need. However, ESD protection in HV area still faces some problems.

High-voltage pins of ICs should have special ESD protection devices for their high operation voltage. Modifying typical HV MOSFETs is a choice for ESD protection. However, high-voltage devices such as lateral diffused MOS (LDMOS) are usually inherent weak at ESD robustness because of non-uniform turn-on phenomenon [1]-[3]. It will take time to improve ESD robustness of high-voltage devices and make optimization by lots of splits. It is suggested that ICs should require 2kV in human body model (HBM) and 200V in machine model (MM) [3], [4].

High-voltage pins are sensitive to latchup issues. ESD protection devices and isolation rings should be designed carefully for latchup immunity. ESD protection devices can be totally latchup-free by increasing holding voltage over supply voltage. This is another problem of some high-voltage devices for ESD protection. Modified n-channel LDMOS or HV silicon-

controlled-rectifier (HVSCR) suffer this latent latchup problem due to their low holding voltage. Some papers indicate that some techniques can be adopted to enhance holding voltage [6]-[ 10], and stacking is one solid way for this issue.

Stacking low-voltage devices is an excellent solution for latchup immunity and ESD robustness. Low-voltage devices for ESD protection have excellent ESD robustness, and can be completed by less masks. It is a good solution to stack low-voltage devices up for latchup immunity, and that way takes less time to survey parameters of devices.

## 1.2 An ESD Protection Scheme in High-Voltage Integrated Circuits

ESD event will happen at fabrication, transportation, package and assembly processes. Accumulated charges discharge from human body or machine to ground through ICs. If no protection devices in ICs, ICs may burn out and losing their functionality. ESD protection is essential for ICs, and arbitrary two pins of the IC should have a path to dissipate ESD energy to avoid damage. Fig. 1.1 is a typical whole-chip ESD protection scheme. Each I/O pin would have two ESD protection devices to construct two paths to power line and ground line respectively, and power-rail clamp would provide an ESD path from VDD to ground.

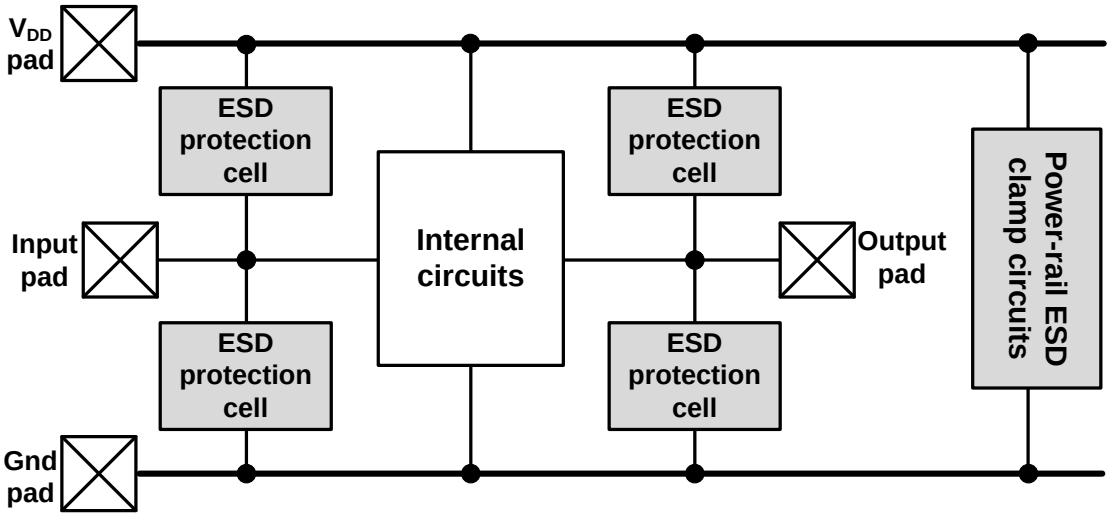



Fig. 1.1 A typical whole-chip ESD protection scheme

The thesis focuses on one ESD protection device, and the device can be an ESD protection cell or a power-rail clamp. Fig. 1.2 introduces ESD protection window. Supply voltage and internal breakdown voltage divide this plot into three parts, and ESD protection design should fit trigger voltage ($V_{t1}$) and holding voltage ($V_h$) of ESD cells into the middle part of this figure.

An ESD event will make damage in internal circuits if internal circuits have breakdown first, so ESD protection devices' trigger voltage should be smaller than the breakdown voltage of internal circuits. If trigger voltage is below supply voltage, that will influence normal operation.

ESD devices may be induced by some transient noise, and the voltage will be clamped at the holding voltage. If holding voltage is bigger than supply voltage, the circuits will return to normal operation after noise. If holding voltage is smaller than supply voltage, the circuits may lose their functionality and the voltage is stuck with a current flow through the IC. For latchup-free design, the holding voltage should be bigger than the supply voltage.

Besides adjusting trigger and holding voltage into the middle part, second breakdown current ($I_{t2}$) and on-resistance ($R_{on}$) are also important. Low on-resistance and high second breakdown current ensure high ESD robustness. The middle part of Fig. 1.2 is an ESD protection window, and the I-V curves of ESD protection devices should fit into the window.

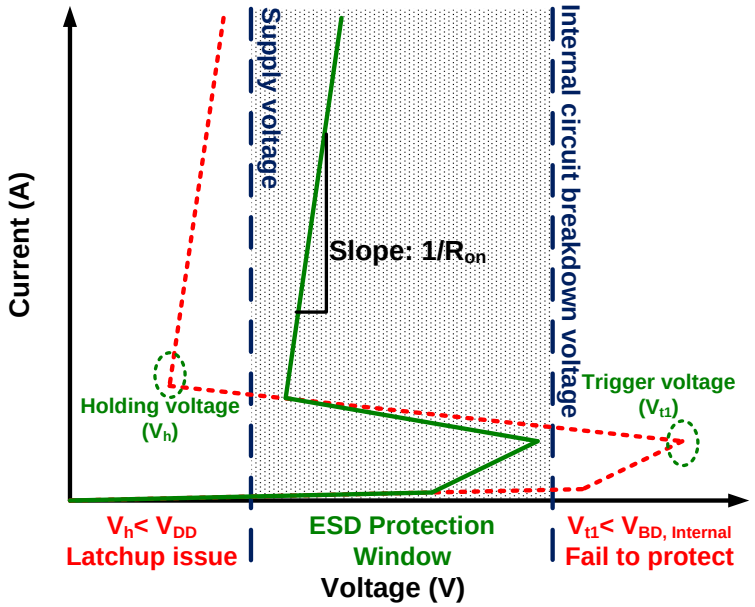



Fig. 1.2 An ESD protection window

In high-voltage technology, supply voltage and internal breakdown voltage are both higher. An ESD protection window are moved to a high-voltage zone, and adjusting holding voltage is more difficult for latchup-free design.

## 1.3 Measurement Methods

ESD robustness can be tested in several ways. It is generally required 2kV in human body model (HBM) and 200V in machine mode (MM). Transmission line pulse (TLP) system will help us to find the characteristics of ESD protection devices.

Charges will be accumulated in human bodies, machines and ICs. When one pin contacts with the object with charges and another pin is connected to ground, the discharging paths are constructed. According to different objects with charges, different testing standards are developed. The equivalent models of HBM and MM are illustrated in Fig. 1.3.

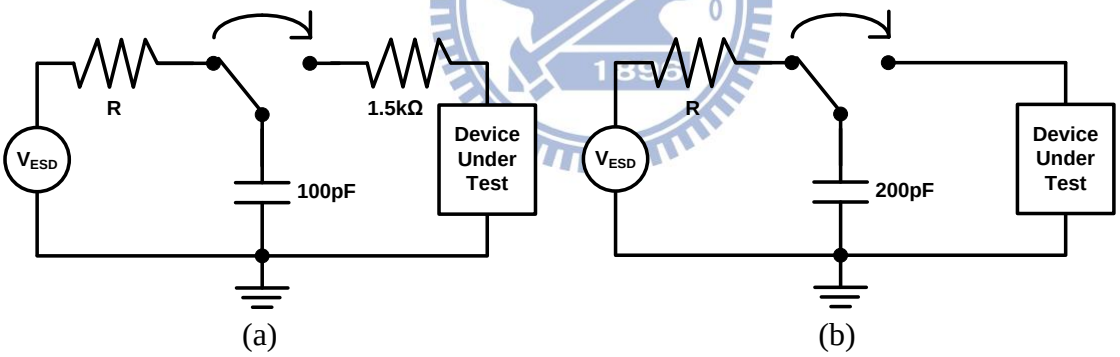



Fig. 1.3 Equivalent circuits of (a) HBM and (b) MM

TLP measurement is a good way to analysis the properties of ESD protection devices [11 ]. TLP system sends pulses sequentially with more and more power. The incident pulse is superposed with the reflective pulse, and it can be observed by an oscilloscope to know the voltage difference across the device and its current. By averaging the stable part of each pulse, it can be constructed an I-V curve. With the I-V data, trigger voltage ($V_{t1}$), holding voltage ($V_h$), second breakdown current ($I_{t2}$) and on-resistance (Ron) can be acquired. It is common to use

pulses with 100-ns duration. The dissipation of energy also concentrates in first 100 ns in HBM. Higher $I_{t2}$ usually means a higher level in HBM.

Tek370 is a dc curve tracer. It can output sinusoidal waves with a power limit. The I-V curve can show snapback and the holding voltage of the device in a dc condition. The holding voltage measured by a dc curve tracer is more convincing because latchup is an event in a dc condition.

The equipment and connection of transient-induced latchup test (TLU) is shown in the following Fig. 1.4 [12]. The device is supplied by the power supply, and then the transient pulse will inject into the device to turn on the device. After transient noise injection, the device may clamp the power supply to lower value with large current or keep normal in original setting with no current.

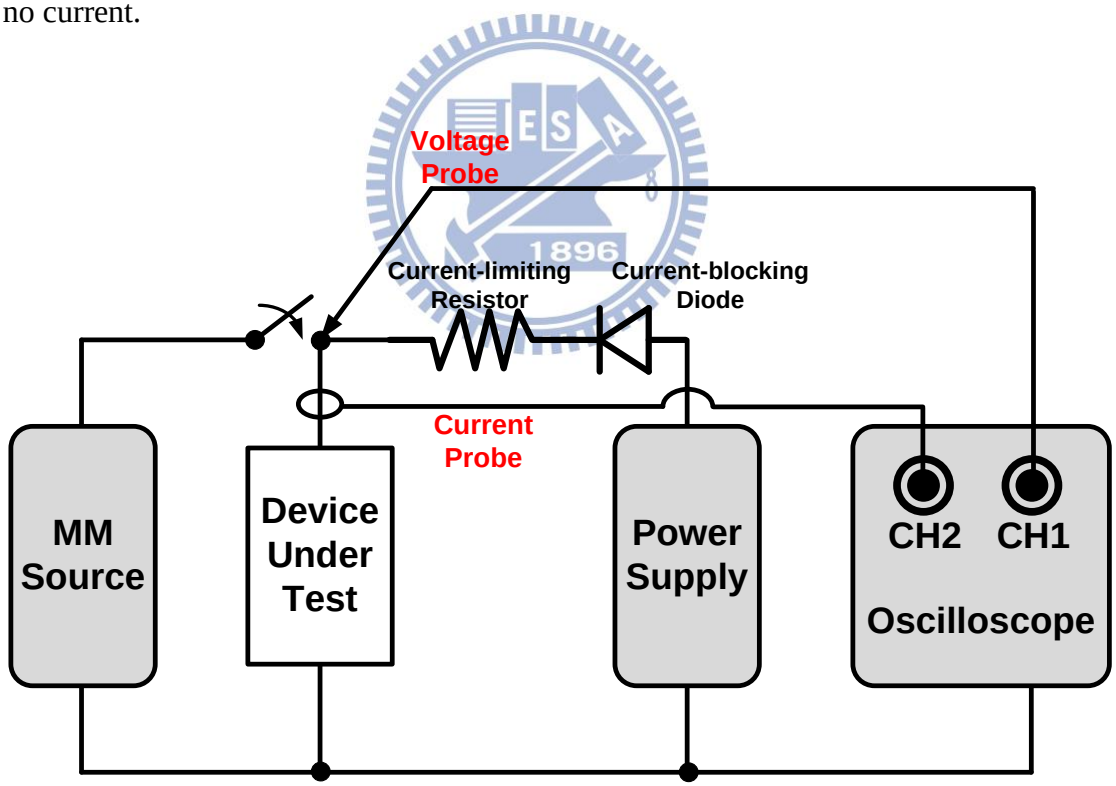



Fig. 1.4 A setup of transient-induced latchup test

## 1.4 Thesis Organization

This thesis focuses on stacks of low-voltage devices for high ESD level and latchup immunity. In chapter 1, it introduces research motivation, measurement methods and a typical protection scheme. It describes prior arts, and some problems of stacking in chapter 2. Chapter 3 shows realization of stacking and the methods of improvement for ESD robustness. In chapter 4, a new idea is proposed to improve stacks of low-voltage NMOS's turn-on speed and latchup immunity. In the last chapter, conclusions and future work are discussed.

# Chapter 2

# Prior Arts and Discussion

Stacking is a way to reach high holding and high ESD robustness. Some study had revealed some properties about stacking. This chapter will introduce prior arts and have some discussion.

## 2.1 Stacked-Field-Oxide Structure [13]

A field-oxide device (FOD) was fabricated in a 0.25-μm 40V CMOS process, and two cascaded FODs were proposed to latchup-free design. A single FOD's cross-section view is showed in Fig. 2.1(a), and stacked-field-oxide structure is shown in Fig. 2.1(b). The equivalent circuits are displayed in Fig. 2.2. This device is like a HV bipolar. The PWELL is surrounded by NWELL and N-buried layer. In this paper, single FOD can reach that trigger voltage is about 20V and holding voltage is about 16V, and the trigger and holding voltage of two cascaded FODs are twice bigger than single FOD's. The second breakdown current ($I_{t2}$) of two cascaded FODs is almost the same as single FOD's $I_{t2}$. $I_{t2}$ of stacked-field-oxide structure can be improved by enlarging total width. The base nodes of a FOD showed can be injected current to reduce trigger voltage and turn-on speed, and it is also verified in this paper.

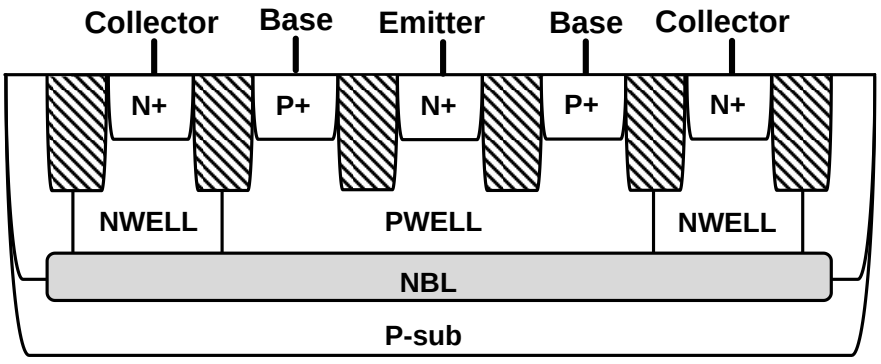



Fig. 2.1 A cross-section view of single field-oxide device

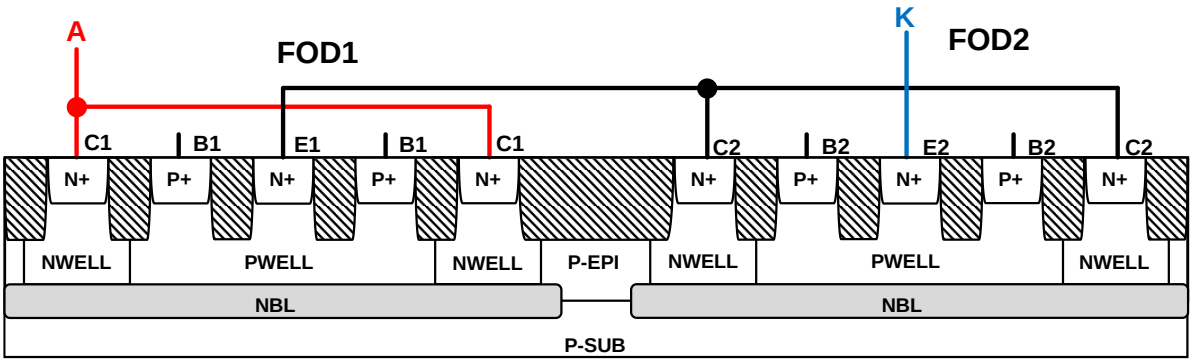



Fig. 2.2 A cross-section view of stacked-field-oxide structure

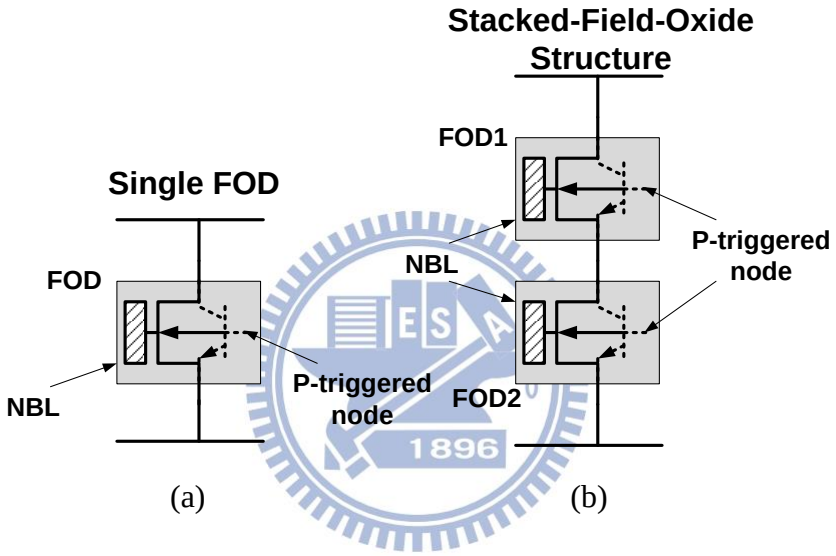



Fig. 2.3 Equivalent circuits of (a) a single FOD and (b) stacked-field-oxide structure

## 2.2 SCR-LDMOS Stacking [14]

This structure was fabricated in a 0.35-μm 30V/5V BCD process. The parasitic silicon-controlled rectifier can reach high $I_{t2}$ and strong ESD robustness. Embedding SCRs in lateral diffused MOS is a good way to enhance the ESD level, but the path of SCR often causes low holding voltage. Holding voltage can increase by stacking for latchup immunity, and trigger voltage won't increase much with ring-resistance-triggered technique.

Fig. 2.4(a) shows the top view of this device. The blue one is a metal line, and there is a piece of P+ ring not connected to metal. That piece of P+ ring forms the resistance used for ring-resistance-triggered technique. Fig. 2.4(b) and Fig. 2.5 are cross-section view and an

equivalent circuit, respectively.

In Fig. 2.4(b) and Fig. 2.5, the first device in the stack is normal SCR-LDMOS, and the P+ ring surrounding the first device are tied to the cathode of the first device. The second device are connected to the first device's cathode. The P+ ring of the second device is not fully covered and connected by the metal line, and that piece of P+ diffusion region forms an equivalent resistor used in ring-resistance-triggered technique. The cathode of the second device is the cathode of the whole stack.

With ring-resistance-triggered technique, stacking can make holding voltage be multiple value and the stack can have almost the same trigger voltage. After the voltage difference across the stack exceeds one SCR-LDMOS's breakdown voltage, the current begins to increases due to the path from the first SCR-LDMOS to the ring-resistor. After the current exceeds the initial trigger current of the first SCR-LDMOS, the first block changes into small resistor equivalently. The voltage difference is almost across on the second device after the first parasitic SCR turns on, and that forces the second device to turn on.

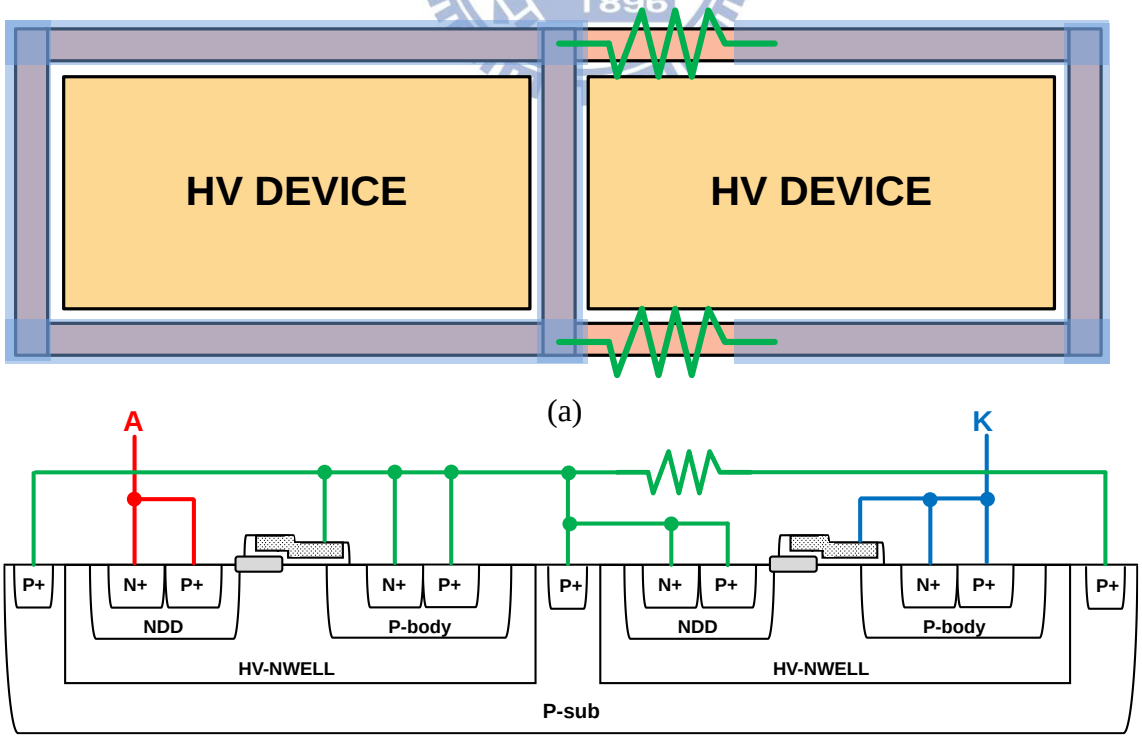



Fig. 2.4 SCR-LDMOS stacking's (a) top view and (b) cross-section view

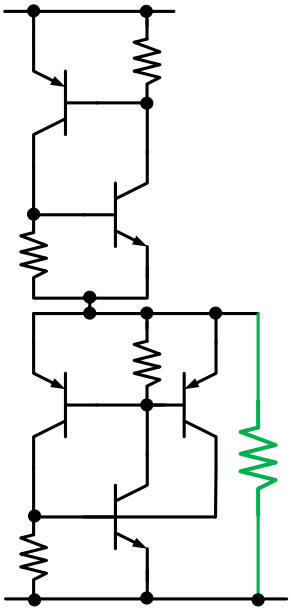


Fig. 2.5 The equivalent circuits of SCR-LDMOS stacking

## 2.3 Discussion

The LV NMOS might suffer non-uniform turn-on problems, and turn-on uniformity could also affect the ESD robustness of stacks [15].The LV PMOS was reported that the leakage current was large when the voltage difference close to its breakdown voltage [16]. The current was caused by gate-induced drain leakage. The leakage current could also occur at the stacking applications, and that would limit stacks of PMOS's uses.

The HV device could be derived different holding voltage by different measurement. The holding voltage of HV MOS measured by TLP is higher than the holding voltage measured by dc curve tracer due to self-heating effect [17], [18].

This thesis focuses on stacks of low-voltage devices for ESD protection. The following experiment will pay attention on stacked NMOS's turn-on uniformity, stacked PMOS's leakage current and the holding voltage of stacked devices.

# Chapter 3

# Stacks of Low-Voltage Devices

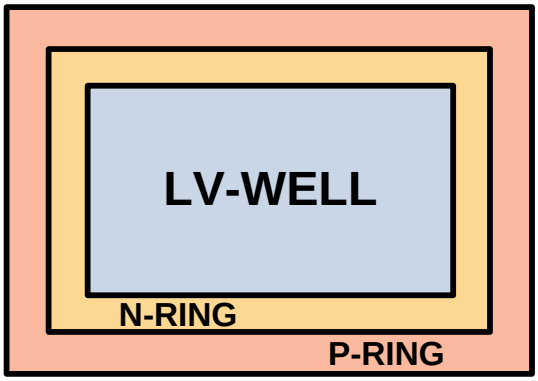
PMOS is a non-snapback device, and it has higher holding voltage than NMOS's holding voltage. For the latchup-free purpose, stacked PMOS is a good choice because of its high holding voltage. Although NMOS has a snapback property and lower holding voltage, NMOS has better ESD robustness per area. In this chapter, stacked NMOS and stacked PMOS are both fabricated and examined.

## 3.1 Low-Voltage Devices in High-Voltage Environments

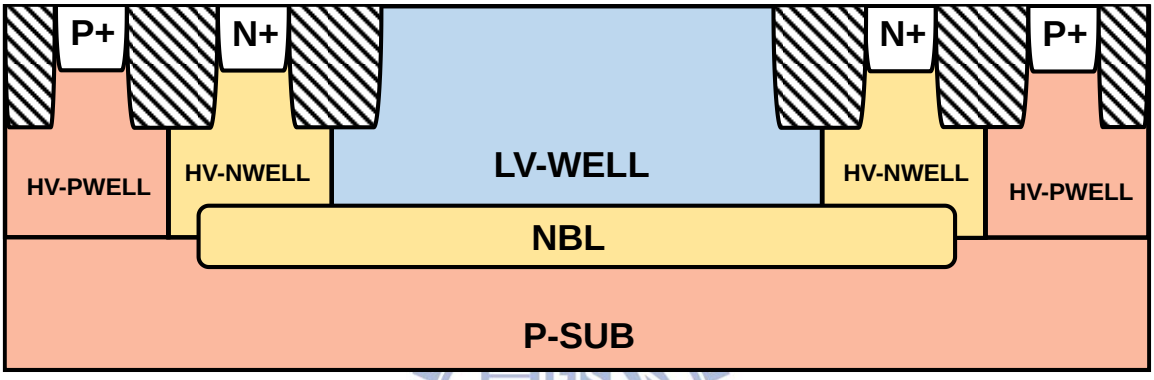
### *3.1.1 Isolation Rings*

Low-voltage devices should be surrounded by isolation ring for the stacking purpose. Without isolation rings, breakdown voltage will be limited by low-voltage layers. P-SUB is usually connected to the lowest potential, and PWELL is tied to P-SUB's potential without isolation rings. Stacks of NMOS without isolation rings have breakdown at N+/PWELL junction, and stacks of PMOS without isolation rings have breakdown at NWELL/PWELL junction. Those high doping junction's breakdown voltage is too low for the stacking purpose.

It has to isolate low-voltage wells by inserting low-doping wells, and these low-doping are high-voltage wells. Isolation rings are composed by a HV-NWELL ring and a HV-PWELL ring. Fig. 3.1(a) and Fig. 3.1(b) show the top view and the cross-section view respectively. The HV-PWELL ring is usually tied to the lowest potential point, and the HV-NWELL ring is tied to relative high potential point. The breakdown voltage of the HV-NWELL/HV-PWELL junction is much higher than the NWELL/PWELL junction's breakdown voltage. HV-NWELL and HVPWELL should keep certain width to avoid punch-through effects.




(a)

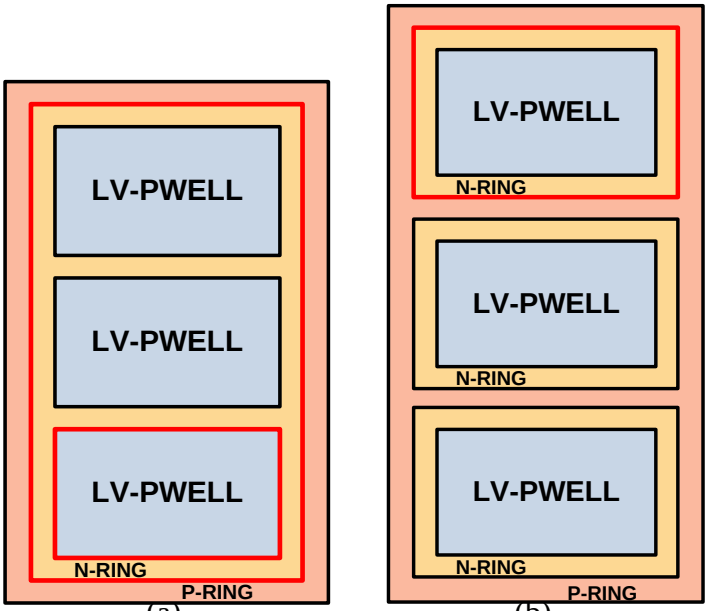



(b)

Fig. 3.1 (a) Top view and (b) cross-section view of LV devices in HV environments

### *3.1.2 Stacking Types*

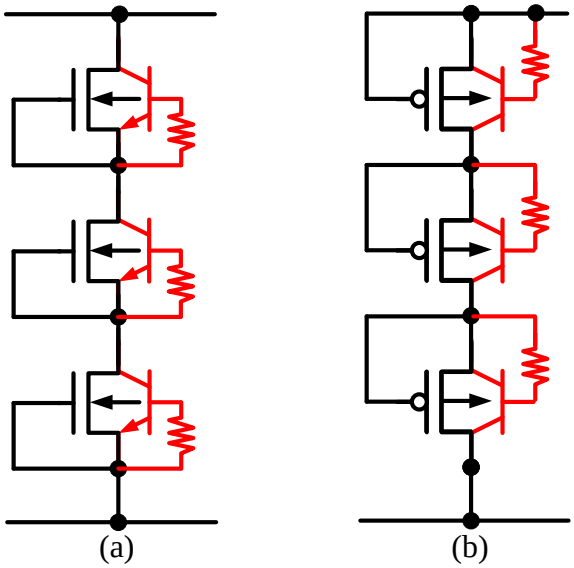
There are two stacking types illustrated in Fig. 3.2. In stacking type 1, the largest reversed voltage difference happens at HV-NWELL/PWELL and HV-NWELL/HV-PWELL junctions. In stacking type 2, only the HV-NWELL/ HV-PWELL junction suffers the largest voltage difference. Using stacking type 1 takes smaller area, but the breakdown voltage of the HV-NWELL/PWELL junction would limit the stacking number. It is adopted stacking type 2 here to reach much higher holding voltage and more stacking numbers.




(a) (b)

Fig. 3.2 (a) Stacking type1 and (b) stacking type 2 in HV environments

The following Fig. 3.3 shows the equivalent circuits of stacked NMOS and stacked PMOS. It can be observed from the figure that the gate of each unit in stacked NMOS is connected to a local low potential point and the gate of PMOS is connected to a local high potential point. The configuration is adopted in this thesis



(a) (b)

Fig. 3.3 Equivalent circuits of (a) a stack of NMOS and (b) a stack of PMOS

## 3.2 Stacks of Low-Voltage NMOS

### *3.2.1 Test Devices*

The test devices were all fabricated in a VIS 0.25-μm Bipolar-CMOS-DMOS (BCD) process. All devices' total width is 360μm. In this process, 5-V NMOS had lightly-doped drain (LDD) structure. Stacking number was from 1 to 10 in this test. The stacked units were introduced in Fig. 3.4. NMOS, NMOS with ESDN and NMOS with SST were implemented with silicide blocking on drain sides [19].

ESDN-implant is an N-type high-doping implantation, and the doping profile covers the range of LDD-implant and the depth is deeper. With the peak of LDD, it is possible that ESD current will flow through the peak and crowd in the peak and the surface. ESD level will be degraded due to this path through the peak of LDD. ESDN-implant covers the peak of LDD and makes junction deeper, and using ESDN implant not only removes the dangerous path but also enhances the current capability. NMOS with ESDN-implant is shown in Fig. 3.4(b). The paper indicates turn-on uniformity can be improved by self-substrate-triggered technique [20]. The cross-section view and an equivalent circuit of NMOS with SST is shown in Fig. 3.5. The central parasitic NPN has the biggest base resistor, and the central two fingers' channel length is smaller. It is expected that the central parasitic NPN will turn on first, and using its current to trigger other fingers to reach better turn-on uniformity.

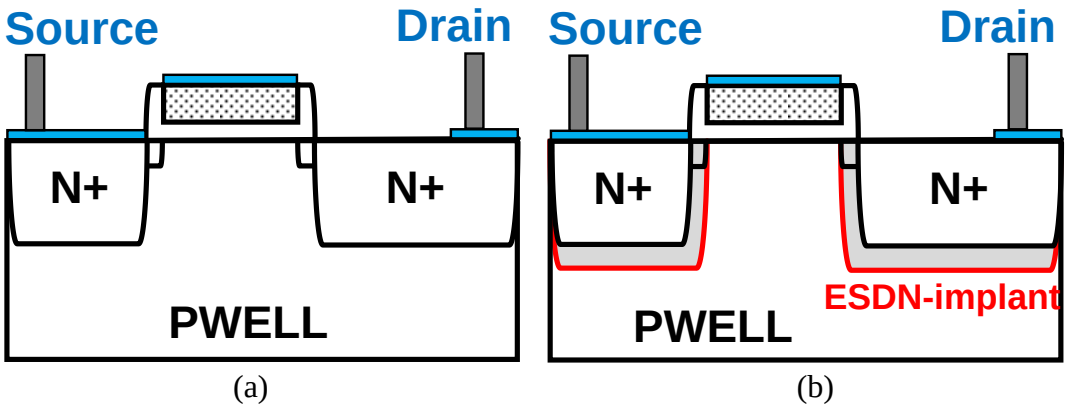
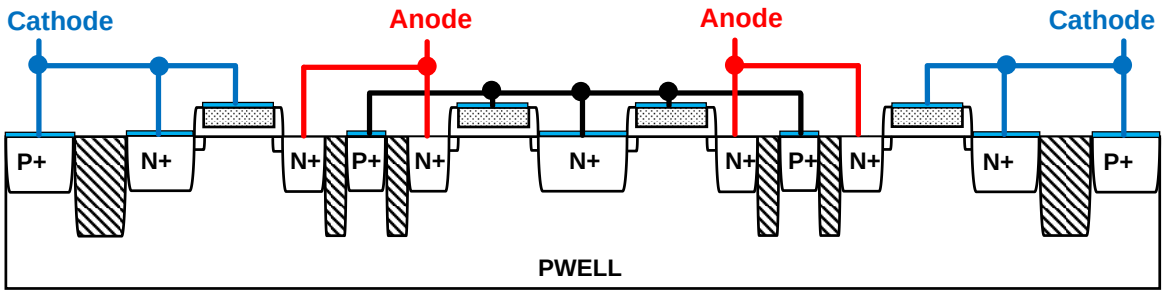
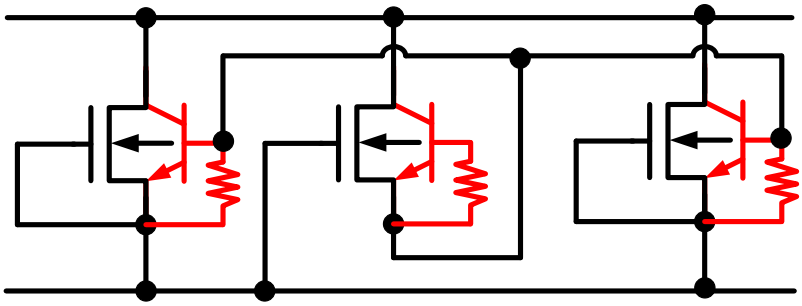



Fig. 3.4 The cross-section view of (a) NMOS and (b) NMOS with ESDN-implant




(a)



(b)

Fig. 3.5 (a) The cross-section view and (b) the equivalent circuit of NMOS with SST

### *3.2.2 Experiment Results*

All devices were fabricated in a VIS 0.25-μm BCD process. In Fig. 3.6(a), the TLP I-V curves show in the plot. It proved that stacking number can be up to ten without losing $I_{t2}$. Trigger and holding voltage are multiplied by the stacking number. With increasing stacking number, on-resistance of the stack increases. Fig. 3.6(b) shows I-V curves measured by the dc curve tracer, Tek370. The values of holding voltage measured by these two equipment is no obvious difference. Stacks of low-voltage NMOS are confirmed no obvious self-heating effect, and don't suffer overestimating by TLP measurement. In Fig. 3.6(b) there is no Tek370 I-V curves of NMOS x8, NMOS x9 and NMOS x10, because the turn-on current is so large to burn the devices out by dc curve tracer.

Table 3.1 illustrates the trigger voltage of 10 units can reach about 100 volts, and its holding voltage can require about 60 volts. More stacking numbers, bigger difference between the holding voltage and the trigger voltage. Bigger difference makes the curve hard to fit into

the ESD protection window. It can adopt some trigger circuits to improve this problem. Stacked NMOS can acquire good ESD robustness, and survive 6kV in HBM.

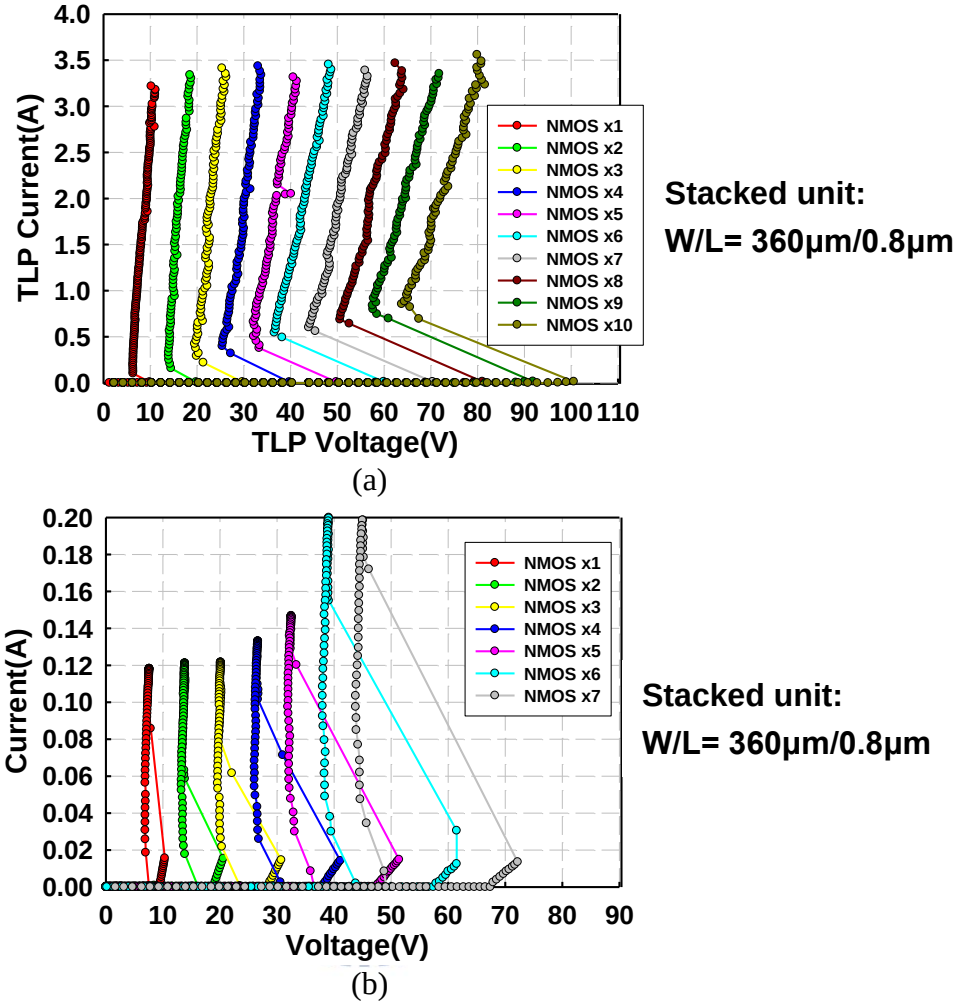



Fig. 3.6 (a) The TLP I-V curves and (b) the Tek370 I-V curves of stacked NMOS

Table 3.1

The measurement data of stacked NMOS

| | TLP | | | Tek370 | DC | ESD(*) |
|---|---|---|---|---|---|---|
| | $V_{t1}$(V) | $V_h$(V) | $I_{t2}$(A) | $V_h$(V) | BV(V) | HBM(V) |
| **1 unit** | 9.88 | 6.32 | 3.18 | 6.92 | 9.4 | 6.0k |
| **2 units** | 19.81 | 13.94 | 3.30 | 13.25 | 19.0 | 6.0k |
| **3 units** | 29.71 | 19.50 | 3.35 | 19.60 | 28.6 | 6.0k |
| **4 units** | 39.72 | 25.39 | 3.38 | 26.20 | 38.2 | 6.0k |
| **5 units** | 49.79 | 32.06 | 3.27 | 32.20 | 47.8 | 6.0k |
| **6 units** | 59.91 | 36.54 | 3.40 | 38.10 | 57.1 | 6.0k |
| **7 units** | 70.38 | 43.88 | 3.32 | 43.90 | 66.6 | 6.0k |
| **8 units** | 81.02 | 50.57 | 3.38 | - | 76.2 | 6.0k |
| **9 units** | 91.84 | 57.52 | 3.31 | - | 85.6 | 6.0k |
| **10 units** | 100.59 | 63.76 | 3.49 | - | 95.0 | 6.0k |

*ESD failure criteria: VBD shift> 20%

The following Fig. 3.7 shows three different stacked units, NMOS, NMOS with ESDN and NMOS with SST. NMOS with ESDN gets the highest $I_{t2}$ and followed by NMOS, and NMOS with SST's $I_{t2}$ is the lowest. Using ESDN can effectively enhance ESD robustness. Two central finger of NMOS with SST unit are used to trigger other fingers, so less fingers to dissipate TLP current. The lower $I_{t2}$ value indicates that not only less fingers dissipates energy but the device has no obvious problem in turn-on uniformity. Fig. 3.8 shows three different type of NMOS's I-V curves measured by TLP. All three types of NMOS can be stacked up for increasing the trigger and holding voltage. The stack of 3 units gets a similar $I_{t2}$ to the single block's $I_{t2}$. It is verified ESDN-implant works well for stacking to reach higher ESD robustness.

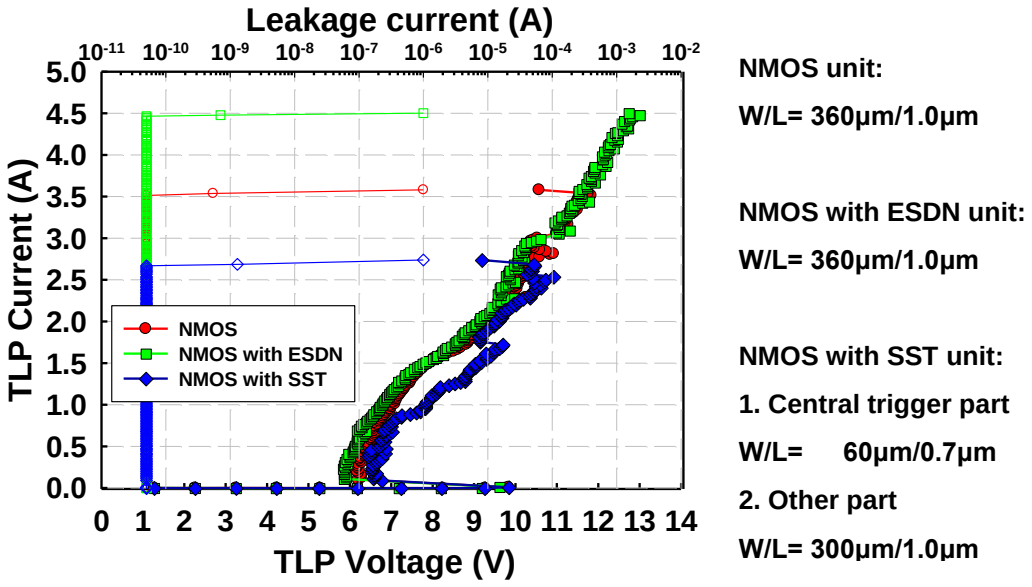



Fig. 3.7 The TLP I-V curves of NMOS, NMOS with ESDN and NMOS with SST

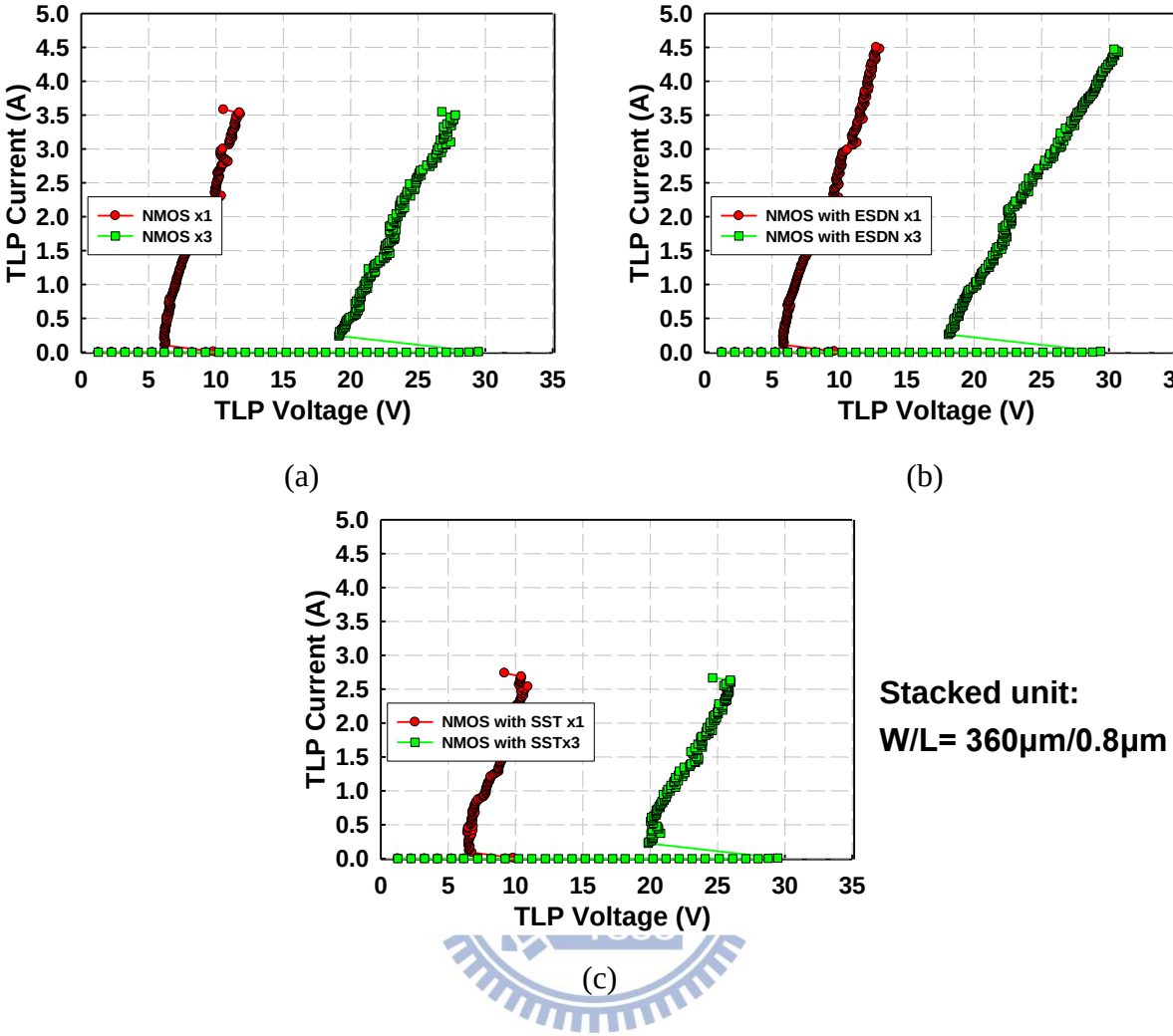



Fig. 3.8 The TLP I-V curves of (a) stacked NMOS, (b) stacked NMOS with ESDN and (c) stacked NMOS with SST

## 3.3 Stacks of Low-Voltage PMOS

### *3.3.1 Test Devices*

The test devices were all fabricated in a VIS 0.25-μm BCD process. All devices' total width is 360μm. In this process, 5-V PMOS had LDD structure. Stacking number was from 1 to 10 in this test.

There are three splits about PMOS in Fig. 3.9. The three types of PMOS are named PMOS1, PMOS2 and PMOS3 respectively. No common ESD-implant layer can be used in

PMOS, so the splits focus on the drain area and silicide blocking. PMOS1 has small drain area and full silicide on the device. PMOS2 has large drain area and full silicide on the device. PMOS3 has large drain area and partial silicide on the device

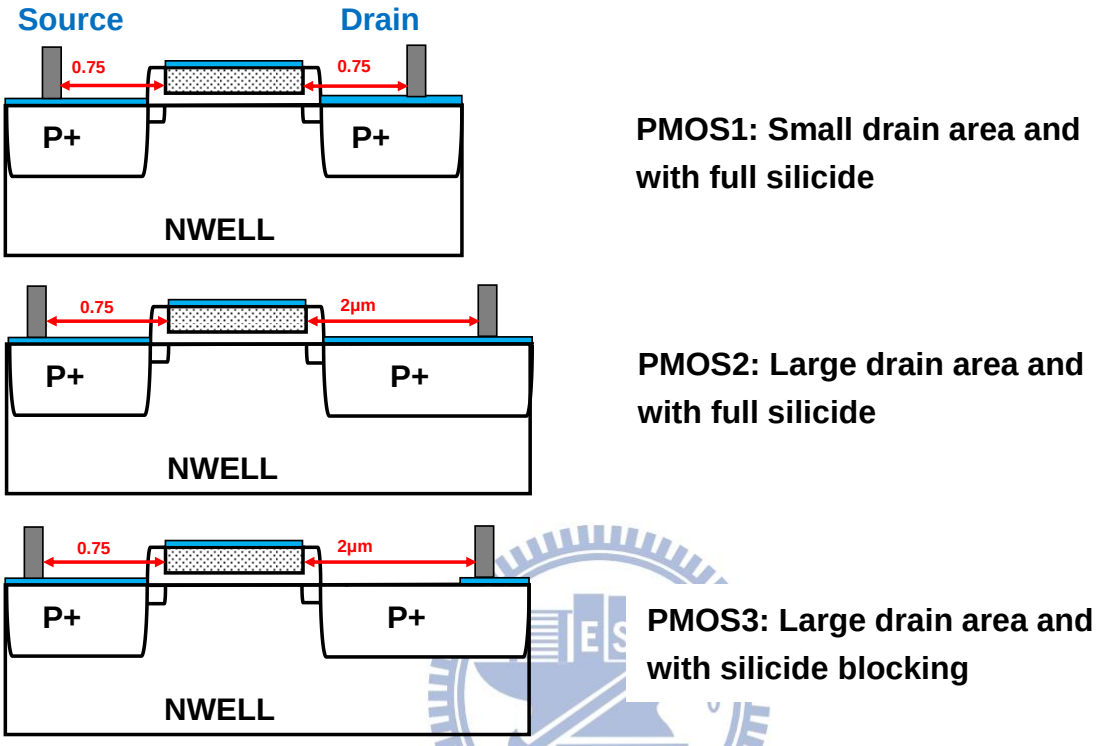



Fig. 3.9 The cross-section view of PMOS1, PMOS2 and PMOS3

### *3.3.2 Experiment Results*

PMOS's TLP I-V curves are shown in Fig. 3.10. All PMOS's total width is 360μm and channel length is 0.8μm. Three devices have similar trigger and holding voltage. PMOS3 acquires the highest $I_{t2}$, are followed by PMOS2's $I_{t2}$, and PMOS1 has the lowest $I_{t2}$. With silicide blocking on drain side, PMOS performs best in the TLP test. PMOS2 with larger drain area increases its current capability. With full silicide on drain side, the difference of $I_{t2}$ affected by drain area is relative small because the surface with silicide is still a low-resistance path.

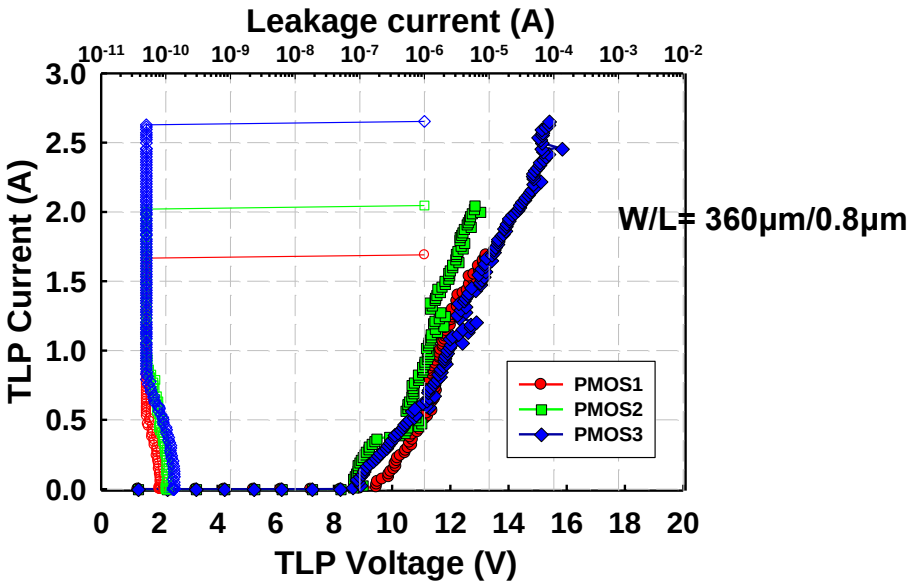
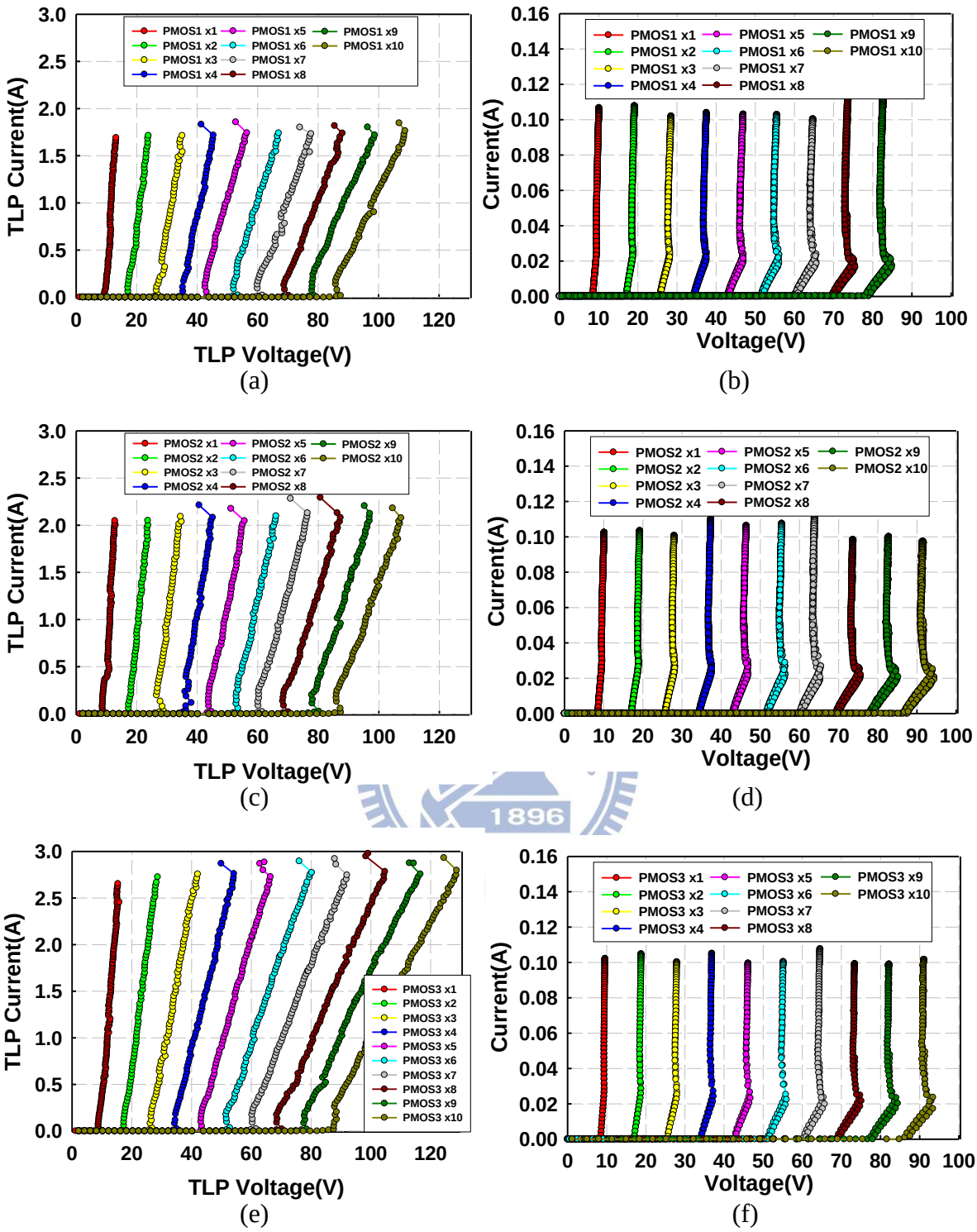



Fig. 3.10 The TLP I-V curves of PMOS1, PMOS2 and PMOS3

From Fig. 3.11, it can be observed that holding voltage measured by TLP is coherent to the holding voltage measured by dc curve tracer. All stacked PMOS's holding voltage can be multiple of single holding voltage. Stacked PMOS has the similar $I_{t2}$ to the single one, and stacked PMOS3 still gets more $I_{t2}$. All three series' values of holding voltage can range from 8.9 to 87 volts.

Table 3.2 describes the data from TLP, curve tracer, DC and ESD measurement. PMOS and stacked PMOS with large drain and silicide blocking can survive from 5.0kV in HBM. The PMOS2 series passes 4.0kV and PMOS1 series passes 4.0kV in HBM.

Table 3.3 shows area information. The stacking method can confirm high holding voltage under penalty of area. The area of a 3-cell stack roughly equals to the area of the HV ESD cell, but the stack is with a solid high holding voltage. Isolation rings occupy lots of area, over 2/3 of total area. Higher $I_{t2}$, smaller area and higher $V_h$ are important for the stacking purpose, so combine these parameters into the factor, $(I_{t2} \times V_h)/A$, for evaluating performance. The PMOS3 series gets higher value, and stacked PMOS1's value is quite similar as PMOS2's. Stacked PMOS3 performs best in this factor, and is suitable for stacking.




**Stacked unit: W/L= 360μm/0.8μm**

Fig. 3.11 Stacked PMOS1's (a) the TLP I-V curves and (b) the Tek370 I-V curves

Stacked PMOS2's (c) the TLP I-V curves and (d) the Tek370 I-V curves

Stacked PMOS2's (e) the TLP I-V curves and (f) the Tek370 I-V curves

Table 3.2

The measurement data of stacked PMOS

| | | TLP | | | Tek370 | DC | ESD |
|---|---|---|---|---|---|---|---|
| | | $V_{t1}$(V) | $V_h$(V) | $I_{t2}$(A) | $V_h$(V) | BV(V) | HBM |
| PMOS1 | 1 unit | 9.45 | 9.45 | 1.67 | 9.46 | 8.2 | 3.0k |
| | 3 units | 27.17 | 26.55 | 1.67 | 27.75 | 24.6 | 3.0k |
| | 6 units | 53.49 | 52.11 | 1.71 | 54.80 | 49.2 | 3.0k |
| PMOS2 | 1 unit | 8.99 | 8.66 | 2.02 | 9.52 | 8.2 | 4.0k |
| | 3 units | 29.01 | 26.58 | 2.04 | 27.60 | 24.6 | 4.0k |
| | 6 units | 53.53 | 52.86 | 2.06 | 55.20 | 49.0 | 4.0k |
| PMOS3 | 1 unit | 8.91 | 8.78 | 2.63 | 9.38 | 8.1 | 5.0k |
| | 3 units | 26.79 | 26.19 | 2.71 | 27.70 | 24.2 | 5.0k |
| | 6 units | 52.85 | 51.56 | 2.77 | 55.00 | 48.4 | 5.0k |

Table 3.3

Area information and comparison of PMOS in a BCD process

| | | Area(μm²) | | | TLP $I_{t2}$ (A) | Tek 370 $V_h$ (V) | $I_{t2}$/ Total area ($10^6$ A/m²) | ($I_{t2}$x $V_h$)/ Total area ($10^6$ VA/m²) |
|---|---|---|---|---|---|---|---|---|
| | | LV | Iso | Total | | | | |
| PMOS1 | 1 unit | 1608 | 4466 | 6074 | 1.67 | 9.46 | 2.76 | 26.11 |
| | 3 units | 4824 | 12272 | 17096 | 1.67 | 27.75 | 0.98 | 27.20 |
| | 6 units | 9648 | 23982 | 33630 | 1.71 | 54.80 | 0.51 | 27.95 |
| PMOS2 | 1 unit | 2175 | 5033 | 7208 | 2.02 | 9.52 | 2.80 | 26.66 |
| | 3 units | 6525 | 13763 | 20288 | 2.04 | 27.60 | 1.01 | 27.88 |
| | 6 units | 13050 | 26859 | 39909 | 2.06 | 55.20 | 0.52 | 28.70 |
| PMOS3 | 1 unit | 2175 | 5033 | 7208 | 2.63 | 9.38 | 3.65 | 34.24 |
| | 3 units | 6525 | 13763 | 20288 | 2.71 | 27.70 | 1.34 | 37.12 |
| | 6 units | 13050 | 26859 | 39909 | 2.77 | 55.00 | 0.69 | 37.95 |

Fig. 3.12 shows dc I-V curves of NMOS, PMOS, stacks of NMOS and PMOS in linear and log scale. It can be observed that PMOS and PMOSx 8's curves are with no steep jump in a logarithm scale. That plots illustrates that PMOS and a stack of PMOS has larger subthreshold leakage current under the stress close to the breakdown voltage. The leakage will limit for the uses.

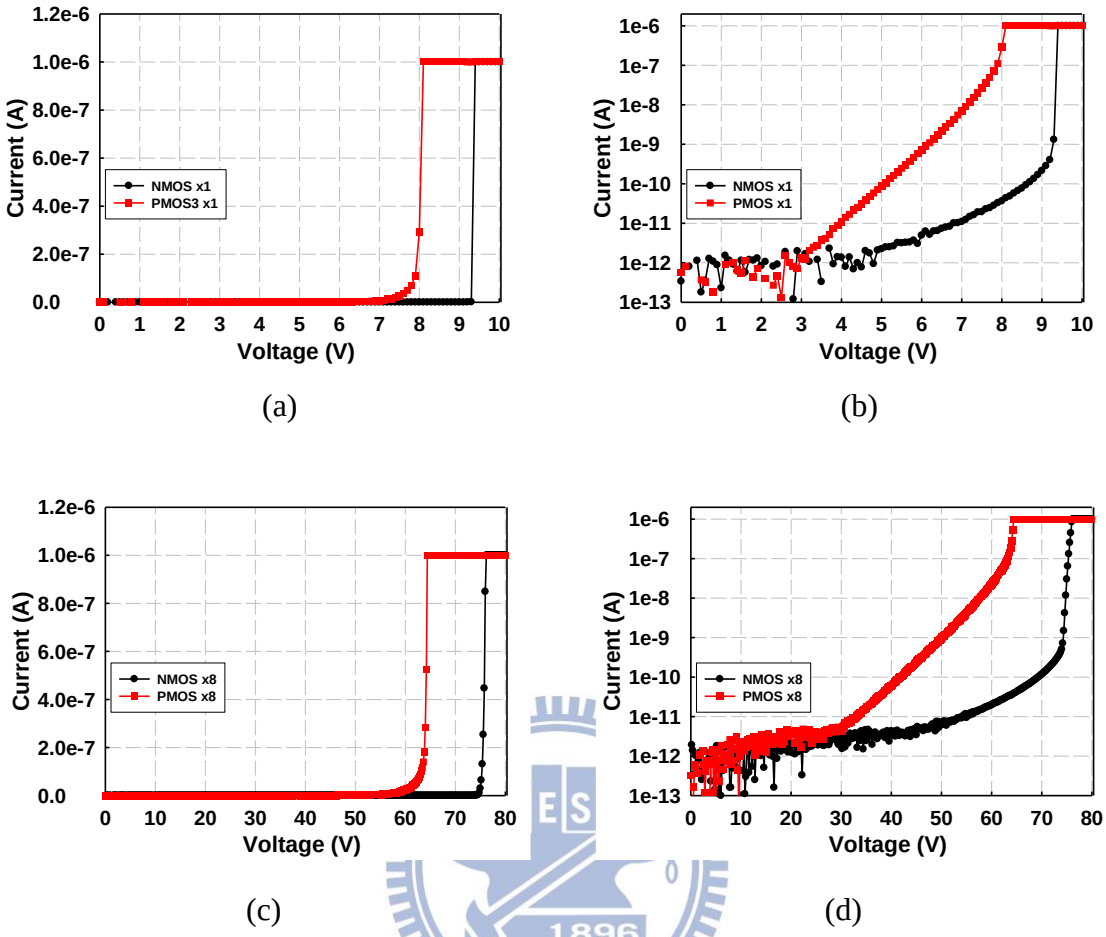



Fig. 3.12 The dc measurement of NMOS and PMOS (a) in a linear scale and (b) in a log scale, and the dc measurement of NMOSx8 and PMOSx8 (a) in a linear scale and (b) in a log scale

## 3.4 Stacked Configuration and Applications

### *3.4.1 Test Devices*

All above stacks from Ch 3.1 to Ch 3.3 are composed by units in line configuration. In Ch 3.4, stacks in folded configuration are examined and compared with stacks in line configuration. If stacks in folded configuration can work, the shape of stacks is more flexible to fit into various layouts.

All devices were fabricated in a VIS 0.25-μm BCD process. The single block's total width

was 360μm, and channel length was 0.8μm. The top view and metal routing could be seen in Fig. 3.13. Only two metal layers were used in these devices.

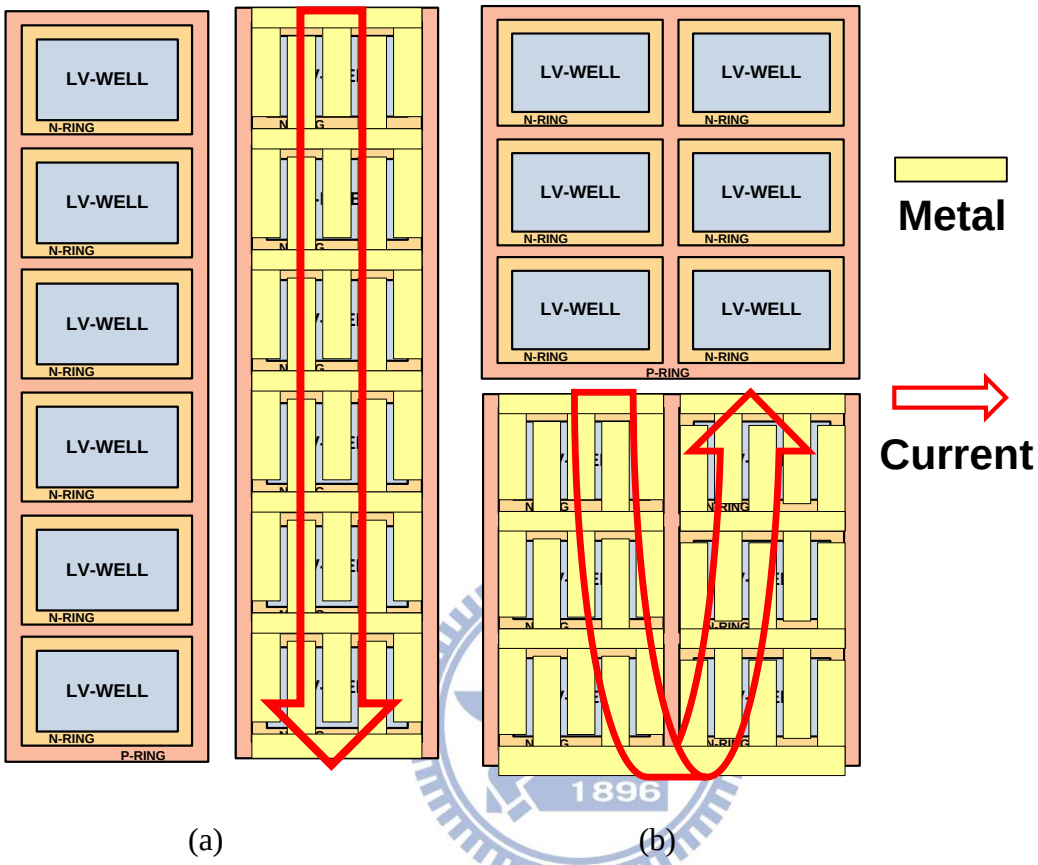



Fig. 3.13 The stacks (a) in line configuration and (b) in folded configuration

### *3.4.2 Experiment Results*

Fig. 3.15 shows the TLP information about stacks of NMOS, PMOS1, PMOS2 and PMOS3. Stacks of 6 devices and 9 devices are measured, and the curves show no obvious difference in different configuration except for the curves of stacked PMOS3. Stacks of devices perform almost the same in line and folded configuration, and trigger voltage, holding voltage and second breakdown current keeps the same values. Only the stack of PMOS3's curves in folded configuration bend inward in high TLP current level.

The TLP data and HBM levels are showed in Table 3.4. The characteristics in TLP data are almost the same. According to HBM data, stacked NMOS in folded configuration would

perform worse than the one in line configuration by 500V, but stacked PMOS performs better in folded configuration by 500V. It can be inferred that there may be another path to conduct the current away. That path is weaker than stacked NMOS, but shares current with stacked NMOS to get more ESD robustness.

The difference between two configuration is small. Folded configuration can make stacks more flexible to fit different layout area.

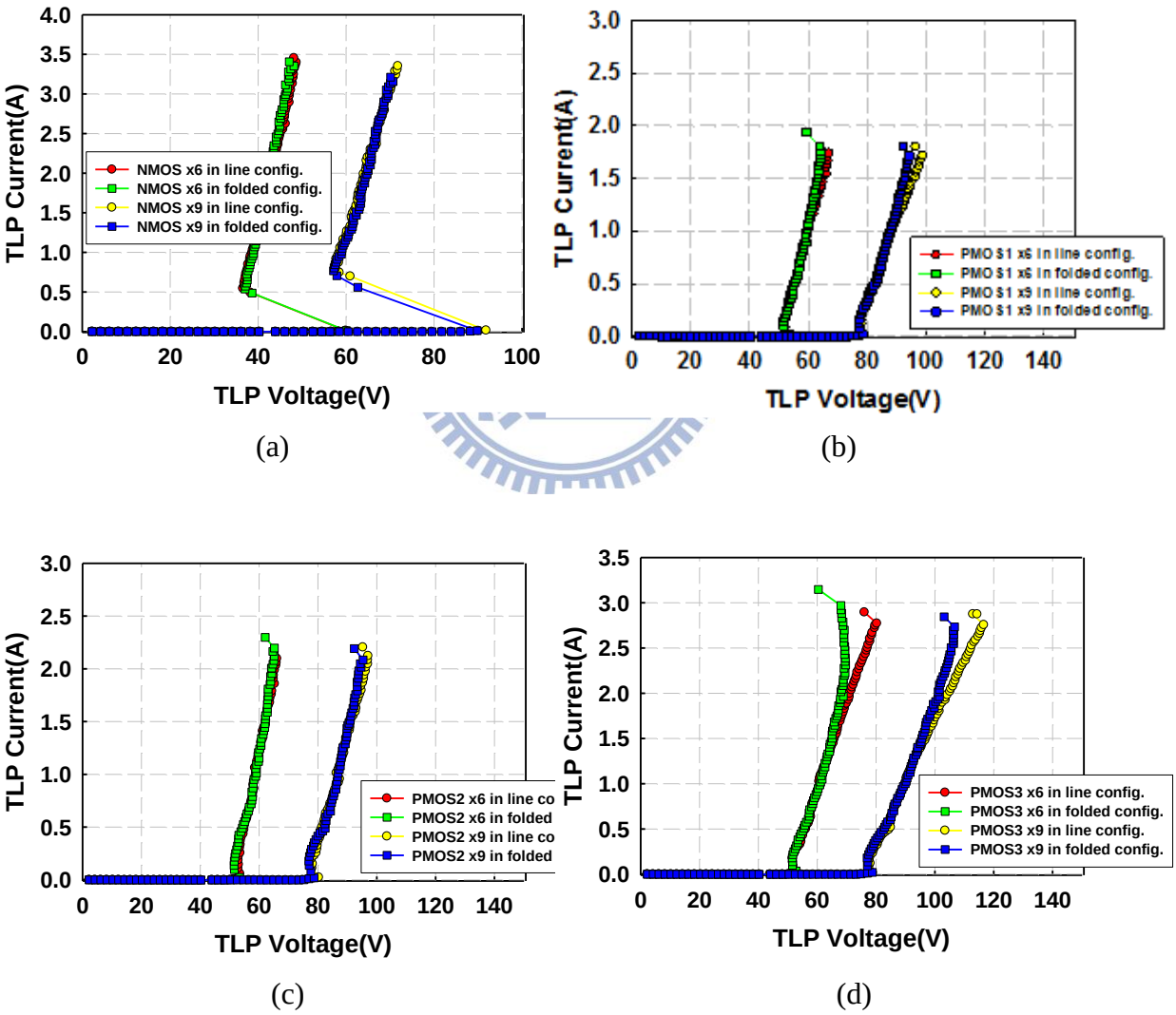



Fig. 3.14 The TLP I-V curves of (a) stacked NMOS, (b) PMOS1, (c) PMOS2 and (d) PMOS3 in line and folded configuration

Table 3.4

TLP and HBM data in different configuration

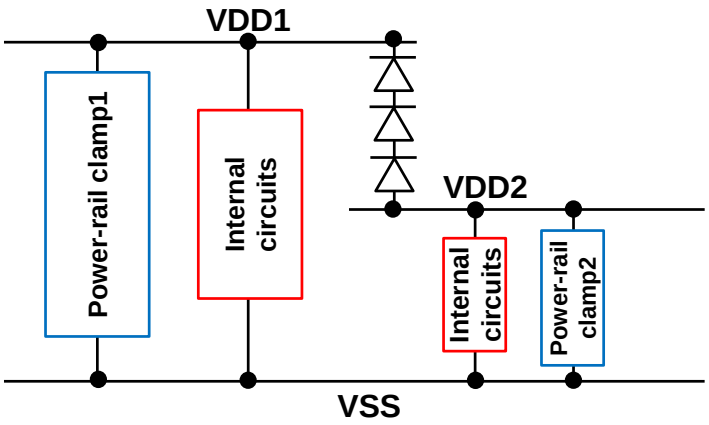
| | TLP | | | Tek370 | DC | ESD(*) |
|---|---|---|---|---|---|---|
| | $V_{t1}$(V) | $V_h$(V) | $I_{t2}$(A) | $V_h$(V) | BV(V) | HBM |
| **Stacked NMOS in line configuration** | | | | | | |
| **6 units** | 59.91 | 36.54 | 3.40 | 38.10 | 57.1 | 6.0k |
| **9 units** | 91.84 | 57.52 | 3.31 | - | 85.6 | 6.0k |
| **Stacked NMOS in folded configuration** | | | | | | |
| **6 units** | 60.03 | 37.01 | 3.35 | 37.90 | 57.2 | 5.5k |
| **9 units** | 89.82 | 57.14 | 3.16 | - | 85.8 | 5.5k |
| **Stacked PMOS3 in line configuration** | | | | | | |
| **6 units** | 52.86 | 51.56 | 2.77 | 55.0 | 48.4 | 5.0k |
| **9 units** | 78.53 | 77.61 | 2.87 | 81.8 | 72.6 | 5.0k |
| **Stacked PMOS3 in folded configuration** | | | | | | |
| **6 units** | 52.81 | 51.52 | 3.08 | 54.9 | 48.4 | 5.5k |
| **9 units** | 78.76 | 76.94 | 2.73 | 81.8 | 72.4 | 5.0k |

*ESD failure criteria: VBD shift> 20%

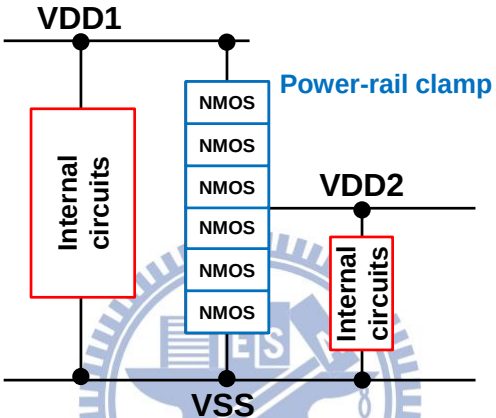
### *3.4.3 Sharing a Stack*

In different power domains, like Fig. 3.15(a), a typical scheme is shown that there is a unique power-rail clamp for each power line to ground. Between power lines, a diode string can be used for pin-to-pin ESD protection.

Stacking is gathering some units to reach the goal. Stacks of devices also can be used for power-rail clamps, and a stack can be shared in different power domains. In Fig 3.15(b), VDD1's the power-rail clamp is a NMOS stack, and VDD2 shares part of this clamp. This way is good at area efficiency, and the path, VDD1-to-VDD2, can be enhanced its ESD robustness by replacing diode string to a stack of NMOS.




(a)



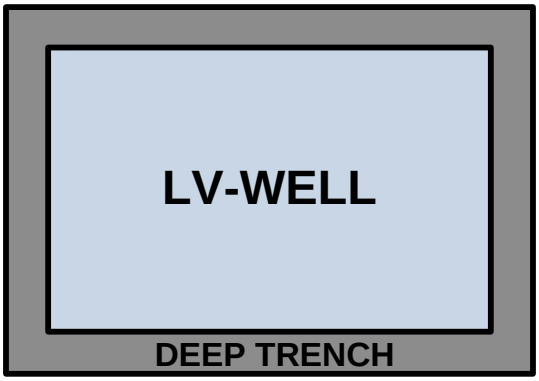

(b)

Fig. 3.15 (a) A typical protection scheme in two power domains (b) A sharing scheme

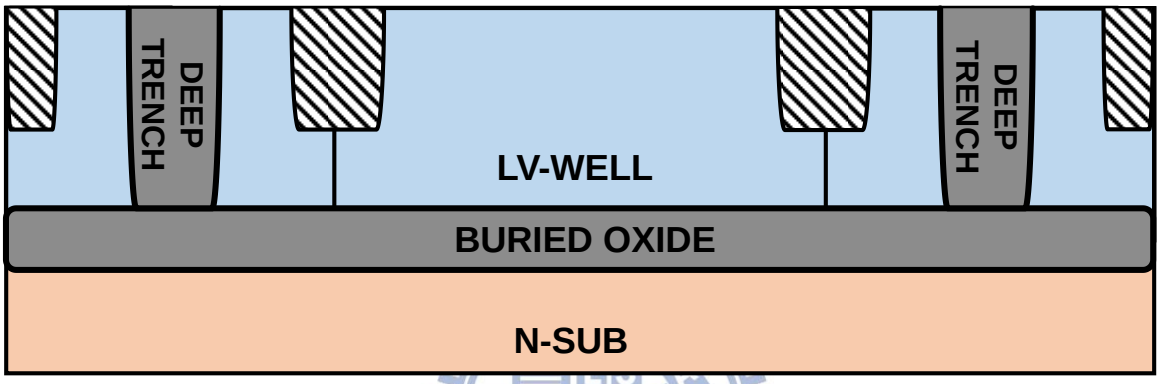
## 3.5 Stacking in a Silicon-on-Insulator Process

### *3.5.1 Isolation Rings*

The following content will introduce stacking into a SOI process. This process comprises deep trenches and buried oxide shown in Fig. 3.16. Deep trench and buried oxide here are used to isolate low-voltage well for the stacking purpose. The isolation rings occupy less area than the rings in a BCD process does due to deep trench and buried oxide.




(a)




(b)

Fig. 3.16 (a) Top view and (b) cross-section view of LV devices in HV environments in a SOI process

### *3.5.2 Test Devices*

The test devices were fabricated in a VIS 0.5-$\mu$m SOI process. In this process, polycide would be used, and no silicide on drain and source area. Except for two column contact on drain and source regions, other spacing was followed the minimum rules. 5-V PMOS's ESD robustness is worse in this process, so PMOS and PFOD with longer width were implemented. PMOS and PFOD with 800-$\mu$m width were stacked up for trigger and holding voltage.

Fig. 3.17 shows the cross-section view of PMOS and PFOD. The channel length of PMOS is 0.5 $\mu$m. In Fig 3.17(b), it can be defined the spacing between P+ is L. The L of PFOD is 0.9 $\mu$m in the minimum rule. It is expected stacked PFOD will have less leakage current because

removing gate stops gate-induced drain leakage.

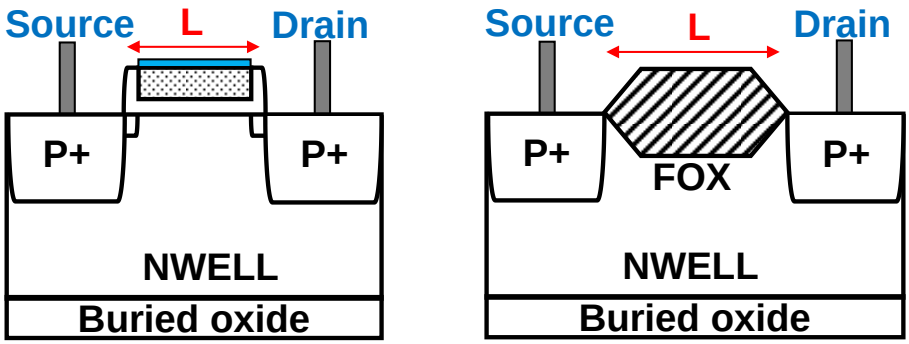



Fig. 3.17 The cross-section view of (a) PMOS and (b) PFOD in a SOI process

### *3.5.3 Experiment results*

PMOS and PFOD can also be stacked up for higher trigger and holding voltage without losing $I_{t2}$. The TLP curves are shown in Fig. 3.18. From Table 3.5, it can be observed that the ratio of isolation rings in total area is smaller than the one in a BCD process. In Fig. 3.19, PFOD reveals less leakage current under the stress close to the breakdown voltage because no gate structure induces that current. Stacked PMOS with 800-μm width can pass 5.5kV in HBM, and stacked PFOD with 800-μm width can pass 4.5kV in HBM.

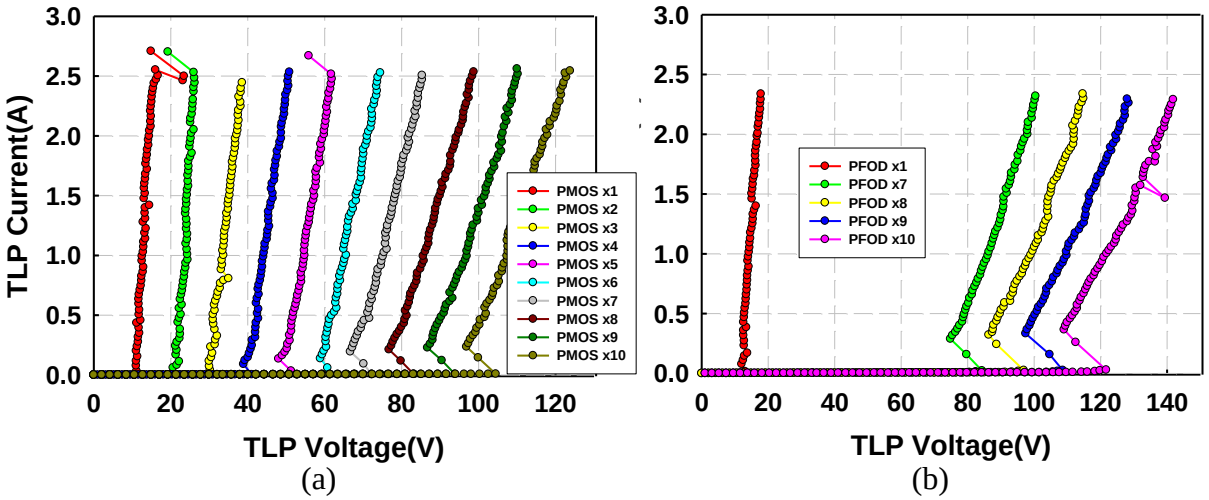



Fig. 3.18 The TLP I-V characteristics of (a) PMOS and (b) PFOD

Table 3.5

Area comparison and information of PMOS and PFOD in a SOI process

| | | Area(μm²) | | | TLP | | | ESD |
|---|---|---|---|---|---|---|---|---|
| | | LV | Iso | Total | $V_{t1}$(V) | $V_h$(V) | $I_{t2}$(A) | HBM |
| PMOS W/L= 500/0.5μm | 1 unit | 3239 | 1709 | 4948 | 10.52 | 10.52 | 2.50 | 5.5k |
| | 7 units | 22673 | 10175 | 32848 | 72.18 | 66.67 | 2.47 | 5.5k |
| | 8 units | 25912 | 11586 | 37498 | 83.16 | 76.74 | 2.50 | 5.5k |
| | 9 units | 29151 | 12997 | 42148 | 93.87 | 86.73 | 2.52 | 5.5k |
| | 10 units | 32390 | 14445 | 46835 | 104.48 | 96.89 | 2.52 | 5.5k |
| PFOD W/L= 500/0.9μm | 1 unit | 3630 | 1794 | 5424 | 13.08 | 12.07 | 2.29 | 4.5k |
| | 7 units | 25410 | 10771 | 36181 | 84.36 | 74.86 | 2.29 | 4.5k |
| | 8 units | 29040 | 12267 | 41307 | 96.93 | 86.38 | 2.30 | 4.5k |
| | 9 units | 32670 | 13763 | 46433 | 108.64 | 97.45 | 2.26 | 4.5k |
| | 10 units | 36300 | 15259 | 51559 | 121.61 | 109.02 | 2.25 | 4.5k |

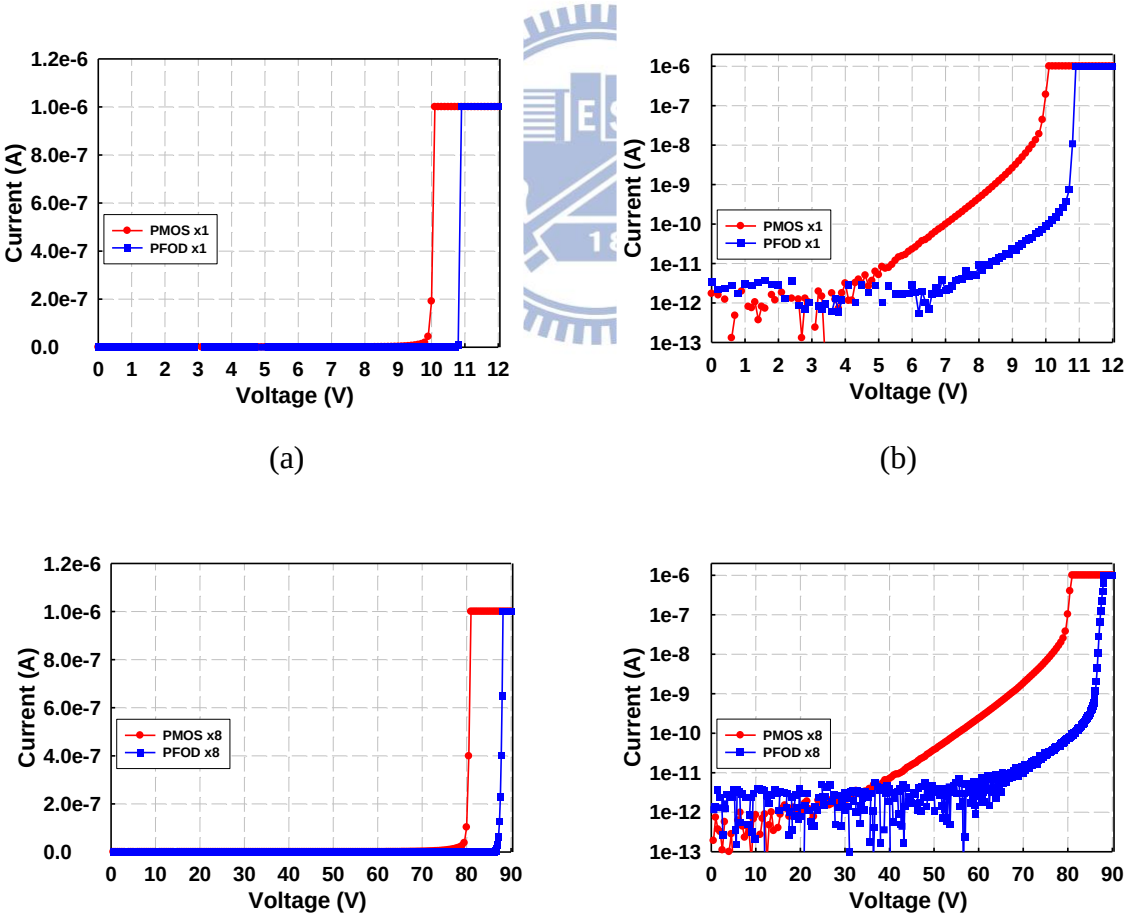



Fig. 3.19 The dc measurement of PMOS and PFOD (a) in a linear scale and (b) in a log scale, and the dc measurement of PMOSx8 and PFODx8 (a) in a linear scale and (b) in a log scale

## 3.6 Summary

Stacked NMOS and stacked PMOS were verified in a VIS 0.25-μm BCD process, they could increase the trigger voltage and holding voltage without losing ESD levels and $I_{t2}$. Stacks of 10 devices were also verified. A 10-NMOS stack's holding voltage reached 63V, and a 10-PMOS stack's holding voltage was over 85V.

Using ESDN-implant can increase NMOS's ESD robustness, and the implantation can also enhance the stack's ESD level. PMOS with silicide blocking can have the best efficient for ESD robustness per area among three PMOS's splits.

Stacking can be implemented in different configuration. A stack in folded configuration was fabricated, and acquired good ESD robustness. Different stacked configuration make stacks more flexible to the layout area.

Sharing one stack for different power domains can save area, and enhance ESD dissipating paths between power lines. A stack consists of blocks, and the whole stack can be used as a power-rail clamp and part of blocks can also be a power-rail clamp.

Isolation rings takes less area in a SOI process, but PMOS is weaker in a SOI process than the one in a BCD process. PMOS and PFOD can be stacked up for increasing holding voltage. PMOS has large leakage current when voltage difference close to breakdown. PFOD with no gate doesn't suffer the leakage problem.

# Chapter 4

# Stacks of NMOS with Native NMOS

The stack's trigger voltage is the summation of all single unis' $V_{t1}$, and the holding voltage is the summation of all single unit's $V_h$. A stack of NMOS has better ESD robustness than stacked PMOS does. In stacked NMOS's I-V curves, it can be observed that the trigger voltage can be reduced for fast turn-on speed.

## 4.1 An Ideal I-V Curves

Ideal characteristics are high ESD robustness, latchup-free design, fast turn-on speed and low on-resistance. After the voltage difference exceeds the supply voltage, the device turns on quickly and clamps the voltage above the supply voltage for latchup-free design until reaching high $I_{t2}$.

It is supposed that a stack of 3 NMOS's holding voltage is the target. It can be found in Fig. 4.1 that the curve of NMOSx3 can be improved by reducing the trigger voltage, and the trigger voltage of the stack of 2 NMOS is great for the ESD protection window design. The ideal case is to combine these two devices' merits, and achieves fast turn-on and latchup-free design. The device with double single unit's $V_{t1}$ and triple single unit's $V_h$ makes the I-V curve closer to the ideal.

The latchup-free condition is that the holding voltage is bigger than the supply voltage. ICs are supplied by dc source in the latchup test. The holding voltage should mainly adopt the value measured by dc curve tracer.

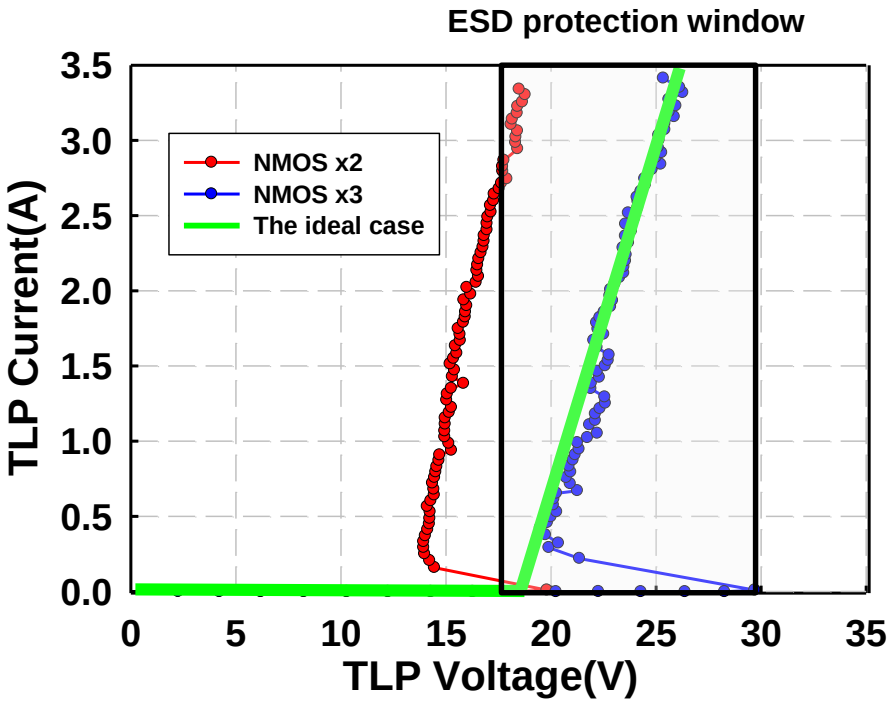


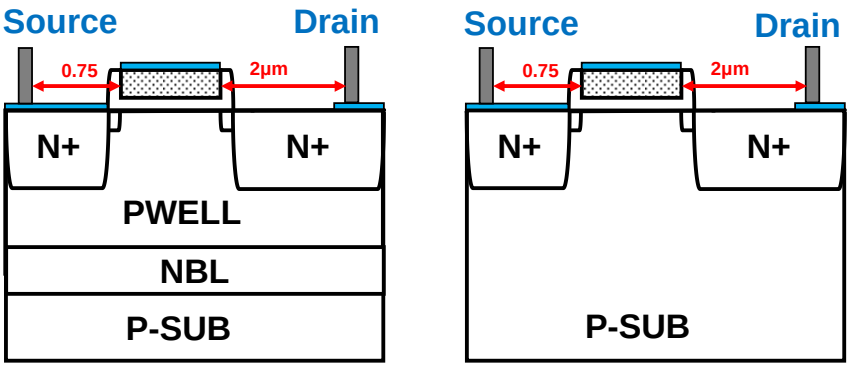

Fig. 4.1 The ideal TLP I-V curve in ESD protection design window

## 4.2 Stacking with Native NMOS

*4.2.1 Native NMOS*

Native NMOS is showed in Fig. 4.2(b), and native NMOS is made in P-SUB instead of PWELL. Native NMOS has no channel implant, and its threshold voltage is very small [21]. The I-V curves of gate-grounded native NMOS measured by TLP is illustrated in Fig. 4.3. It can be noticed that native NMOS can have large current under small voltage difference. The current of native NMOS boosts due to punch-through effect, and the punch-through voltage becomes smaller as the channel length becomes smaller.

Gate-grounded native NMOS is the stacked unit. Because of the small threshold voltage, native NMOS still has current over 1μA with gate-grounded connection under the small voltage difference. That is an already-on device, but it can be followed by NMOS in series. Because of series configuration, the breakdown voltage is the summation of all unit's breakdown voltage. The leakage problem is removed by cascaded configuration.




(a) (b)

Fig. 4.2 The cross-section view of (a) typical NMOS and (b) native NMOS

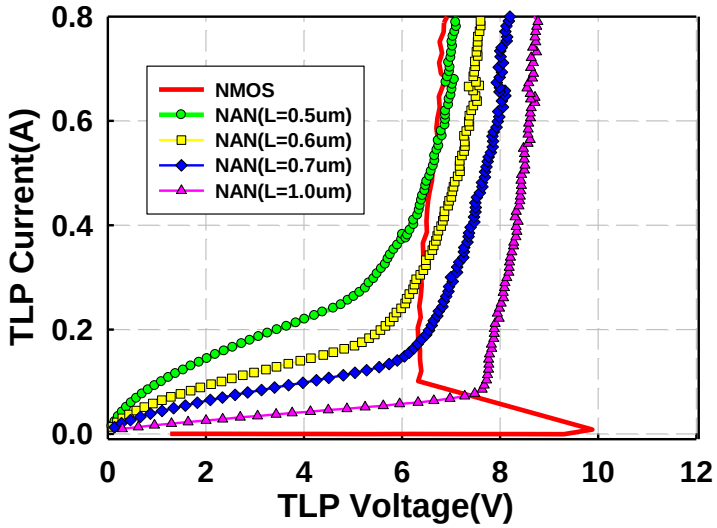
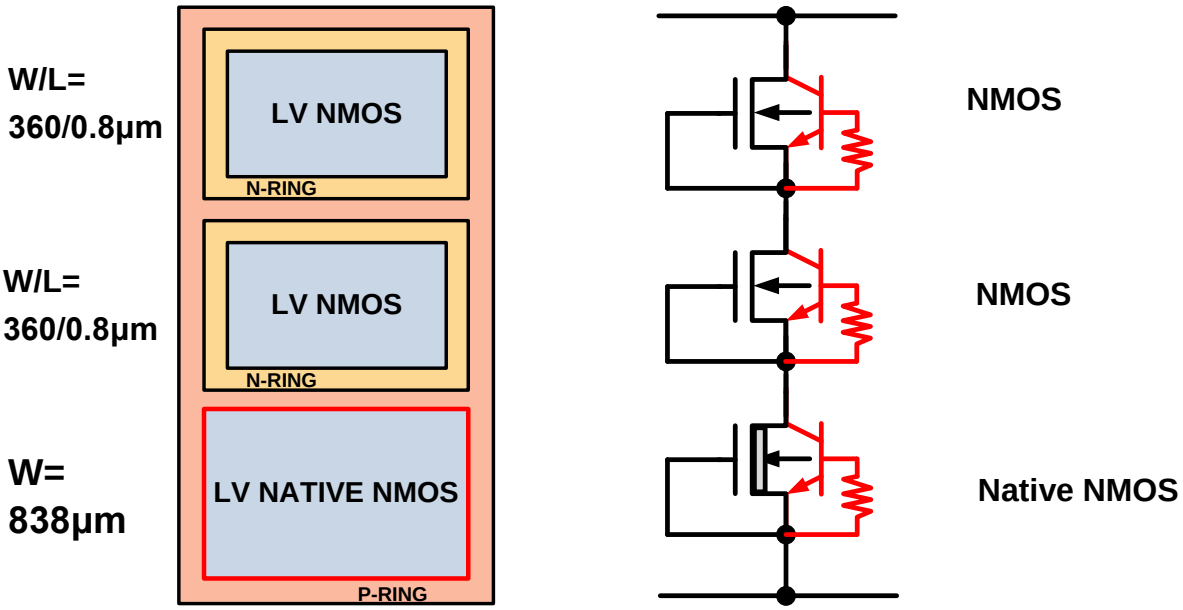



Fig. 4.3 The TLP I-V curves of native NMOS with different channel length

*4.2.2 Test Devices*

The test devices were all fabricated in a VIS 0.25-μm BCD process. The stack consists of 2 NMOS and 1 native NMOS with different channel length. NMOS's total width is 360 μm, and channel length is 0.8 μm. The native NMOS's total width is 838 μm.

Fig. 4.4 shows the top view and the equivalent circuit of 2 NMOS and 1 native NMOS in series. The stack can divide into 3 blocks, and each block occupied the same area. The third block can get rid of HV-NWELL ring, and the native NMOS's total width is longer than the first and the second NMOS's.




(a) (b)

Fig. 4.4 (a) The top view and (b) the equivalent circuit of the stack of 2 NMOS and 1 native NMOS in series

*4.2.3 Experiment Results*

It can be seen in Fig. 4.5(a) that the red curve is NMOSx2 and the blue curve is NMOSx3. The stacked unit's trigger voltage is named Vt1_unit and unit's holding voltage is named Vh_unit here. The ideal goal is the curve with trigger voltage at double Vt1_unit and holding voltage at triple Vh_unit. The legend, Nx2+NAN, indicates 2 NMOS and native NMOS in series in one stack. Fig. 4.5(b) is an enlarged picture of (a) in a low current level. In a low current level, the curves pull back as native NMOS's length is small. When the native NMOS's length is 0.7um, the TLP curve is close to the ideal case. There is a snapback phenomenon in high current level. After getting into a snapback region, the native NMOS would get a little damage, so the native NMOS's $I_{t2}$ should be the value of the last point before snapback.

It has to check the holding voltage by dc curve tracer. In Fig. 4.5(c), the trigger voltage of stacks are as low as double Vt1_unit, but the holding voltage is lower than triple Vh_unit. The

trigger voltage in TLP measurement is 19.96V, and the holding voltage in Tek360 measurement is 14.75V from the best curve, Nx2+NAN(L=1.0um) in Table 4.1.

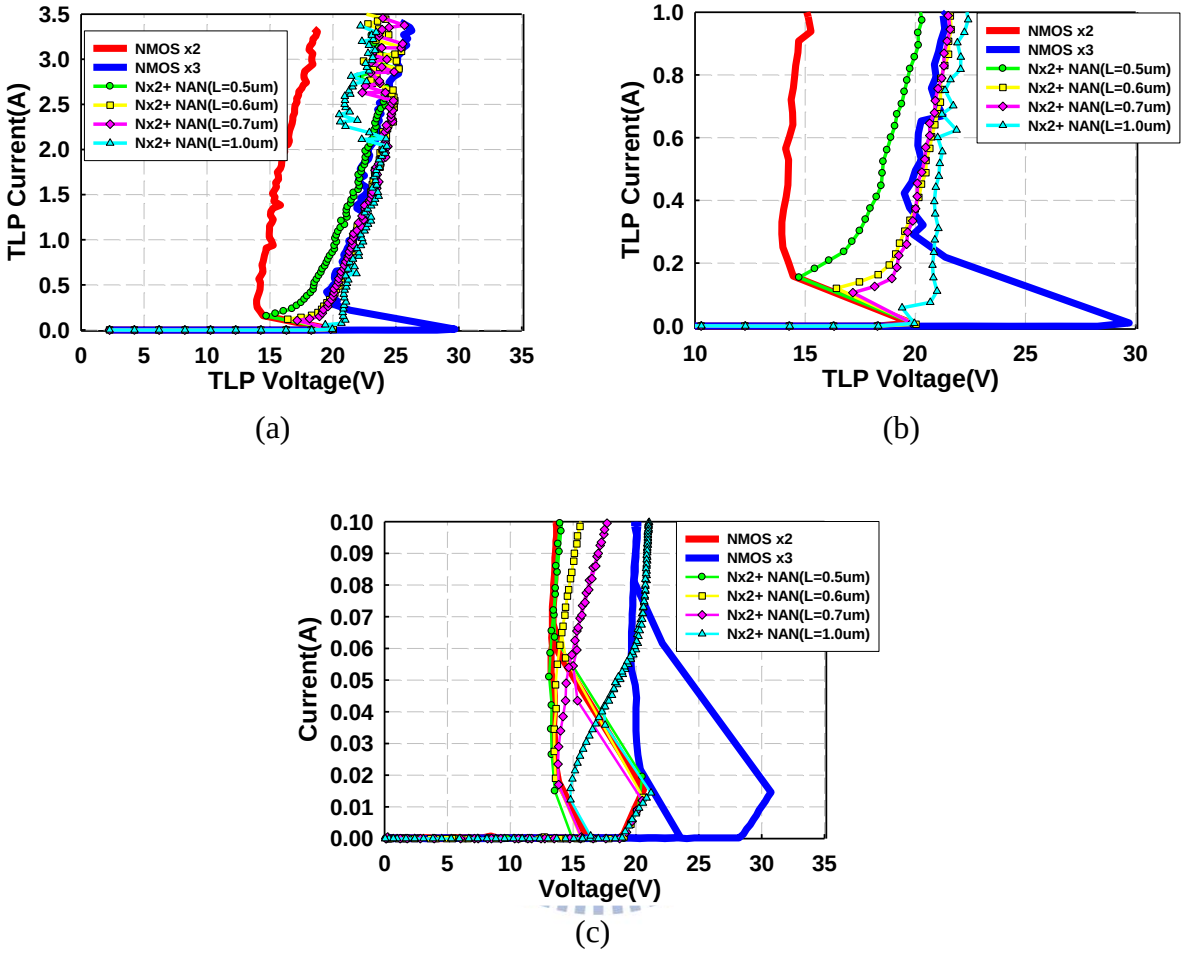



Fig. 4.5 (a) The TLP I-V curves of stacking with NAN (b) in a low current level (c) The Tek370 I-V curves of stacking with NAN

Table 4.1

The characteristics of stacking with native NMOS

| | TLP | | Tek370 |
|---|---|---|---|
| | $V_{t1}$(V) | $V_h$(V) | $V_h$(V) |
| NMOSx 2 | 19.81 | 13.94 | 13.25 |
| NMOSx 3 | 29.71 | 19.50 | 19.60 |
| Nx2+ NAN (L=0.5 μm) | 19.87 | 14.72 | 13.10 |
| Nx2+ NAN (L=0.6 μm) | 20.03 | 16.42 | 13.50 |
| Nx2+ NAN (L=0.7 μm) | 19.83 | 17.17 | 13.80 |
| Nx2+ NAN (L=1.0 μm) | 19.96 | 19.40 | 14.75 |

## 4.3 Stacking with Native-NMOS-Triggered NMOS

### *4.3.1 Test Devices*

The test devices were all fabricated in a VIS 0.25-μm BCD process. The stack consists of 2 NMOS and 1 native-NMOS-triggered NMOS with different channel length. NMOS's total width is 360 μm, and channel length is 0.8 μm. The native NMOS's width is 420 μm.

Replacing the native NMOS with native-NMOS-triggered NMOS should make the stack stronger for ESD protection because native NMOS's $I_{t2}$ is lower than NMOS's. It is expected that the stack composed of 2 NMOS and 1 native-NMOS-triggered NMOS (NATN) can have the holding voltage equaled to triple Vh_unit and the trigger voltage equaled to double Vt1_unit, and acquire more $I_{t2}$.

The cross-section view of native-NMOS-triggered NMOS is shown in Fig. 4.6. All anodes are connected together, and all cathodes are connected together. Native NMOS's source terminal is connected to P+ located in the middle of NMOS's drain. Native NMOS will conduct first, and the current will trigger the parasitic NPN in NMOS structure during an ESD event.

Fig. 4.7 reveals the top view and the circuit of this stack. It needs more area than the stack of 2 NMOS and 1 native NMOS's area.

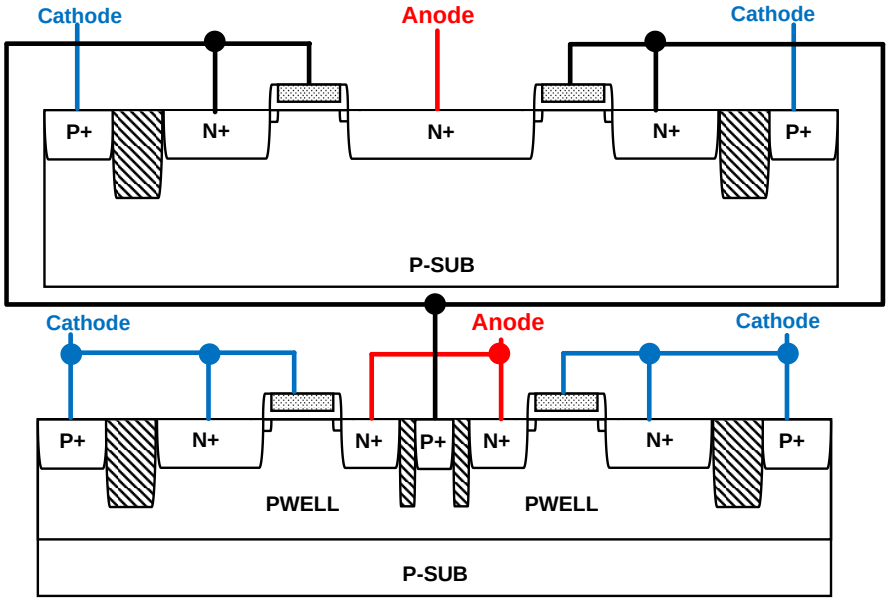
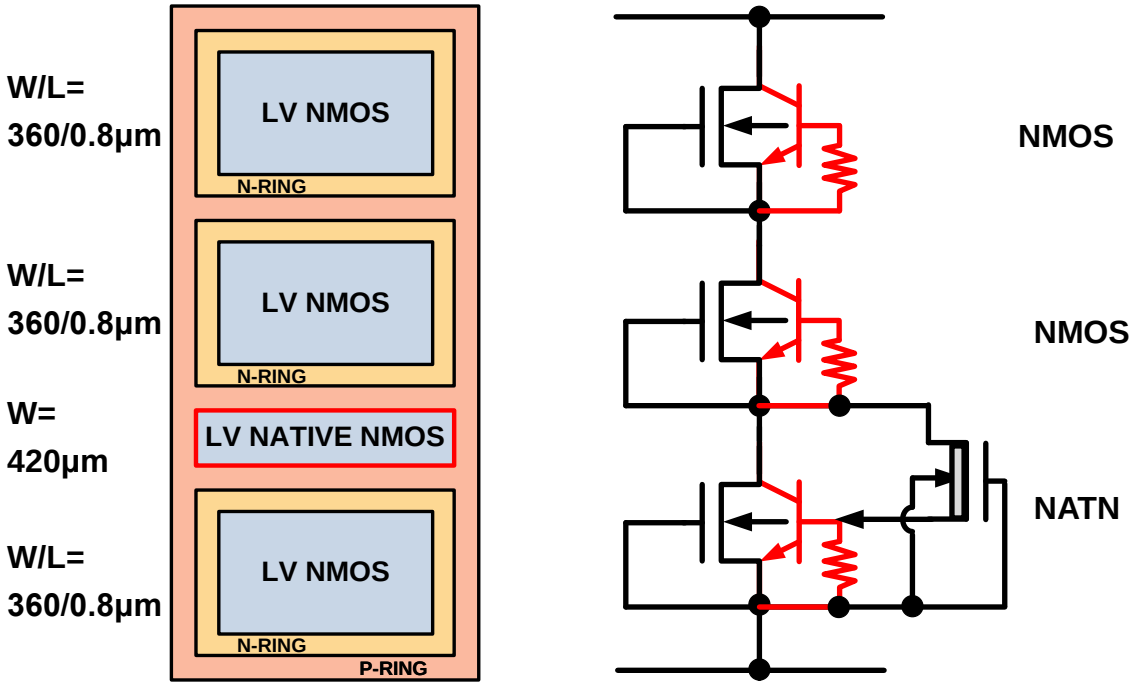



Fig. 4.6 The cross-section view of native-NMOS-triggered NMOS




(a) (b)

Fig. 4.7 (a) The top view and (b) the equivalent circuit of the stack of 2 NMOS and 1 native-NMOS-triggered NMOS in series

*4.3.2 Experiment Results*

The TLP I-V and Tek370 I-V curves are displayed in Fig. 4.8. The legend, Nx2+ NATN, means 2 NMOS and 1 native-NMOS-triggered NMOS in series in a stack. The holding voltage in TLP I-V curves have improved, and the holding voltage of the stack with NATN (L= 1.0μm) is close to triple Vh_unit.

Observing Tek370 I-V curves, it can be found that the holding voltage is still not high enough. The highest holding voltage is 16.15V, and that is still larger than the holding voltage of 2 NMOS in series by 2.9V.

Because native NMOS still has some current under small voltage difference, the holding voltage is not high as triple Vh_unit. But this solution still gives more choices on the holding voltage with fast turn-on speed. The best one in these curve is Nx2+ NATN (L= 1um). Its

holding voltage is 16.15V measured by Tek370, and trigger voltage is 21.78V measured by TLP system in Table4.2.

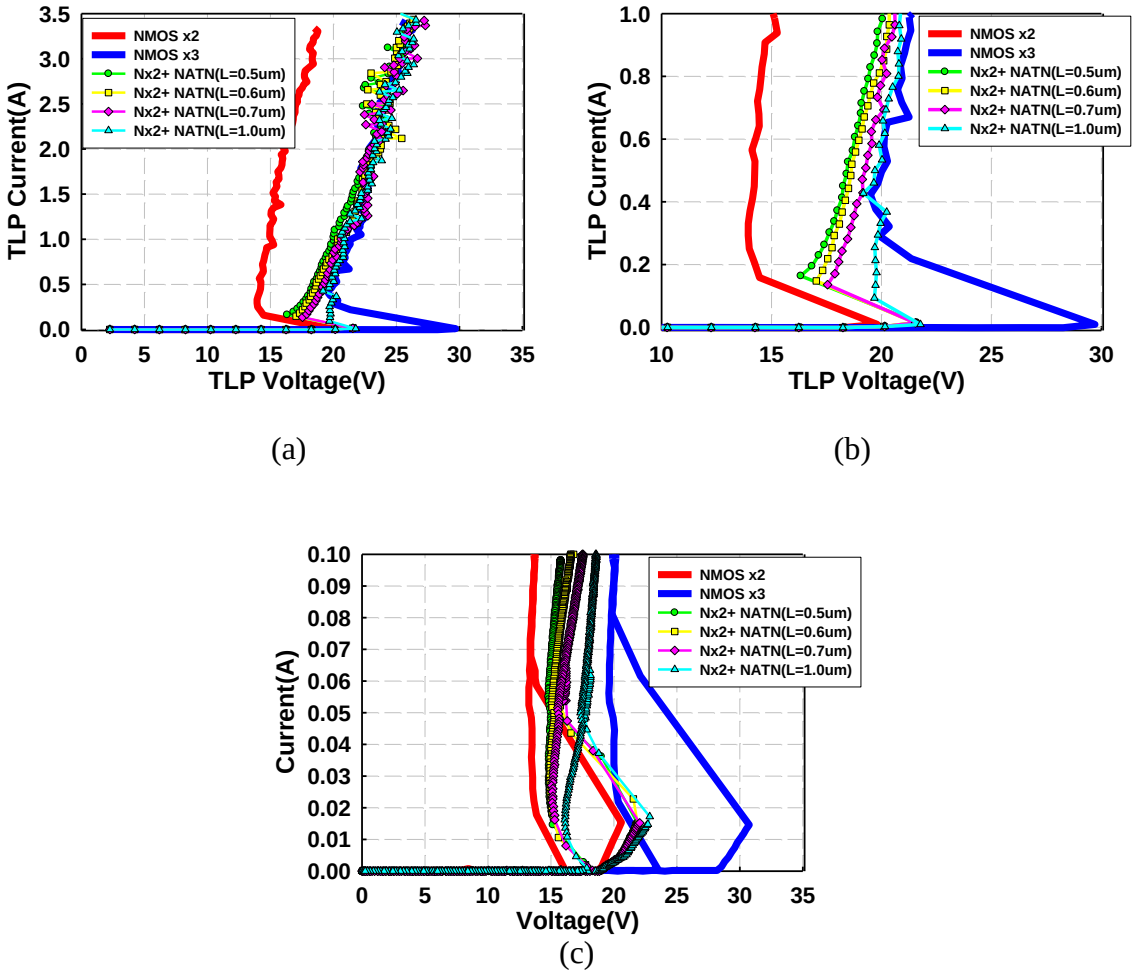



Fig. 4.8 (a) The TLP I-V curves of stacking with NATN (b) in a low current level (c) The Tek370 I-V curves of stacking with NATN

Table 4.2

The characteristics of stacking with NATN

| | TLP | | Tek370 |
|---|---|---|---|
| | $V_{t1}$(V) | $V_h$(V) | $V_h$(V) |
| NMOSx 2 | 19.81 | 13.94 | 13.25 |
| NMOSx 3 | 29.71 | 19.50 | 19.60 |
| Nx2+ NATN (L=0.5 μm) | 21.60 | 16.33 | 14.90 |
| Nx2+ NATN (L=0.6 μm) | 21.53 | 17.04 | 15.00 |
| Nx2+ NATN (L=0.7 μm) | 21.55 | 17.55 | 15.15 |
| Nx2+NATN (L=1.0 μm) | 21.78 | 19.68 | 16.15 |

## 4.4 Stacking with Self-Native-NMOS-Triggered NMOS

### *4.4.1 Test Devices*

The test devices were all fabricated in a VIS 0.25-μm BCD process. The stack consists of 2 NMOS and 1 self-native-NMOS-triggered NMOS with different channel length. NMOS's total width is 360 μm, and channel length is 0.8 μm. The third block can divide into two parts. The native NMOS is trigger part and its width is 105 μm. The other part is normal NMOS and its width is 733 μm.

It takes lots of additional area to implement the above design, and native NMOS should be merged into the last block. Self-native-NMOS-triggered NMOS's cross-section view is shown in Fig. 4.9. The stack of 2 NMOS and self-native-NMOS-triggered NMOS (SNATN) is revealed in Fig. 4.10.

In the third block, SNATN can be implemented by replacing the middle part of NMOS with native NMOS, and connecting native NMOS's source terminal to P+ located in other NMOS's drain.

After the voltage difference across the stack exceeds double Vt1_unit, the native NMOS will turn on first to trigger other NMOS in the same block. It has better area efficiency to implement native NMOS into the last block, and its area is more compact.

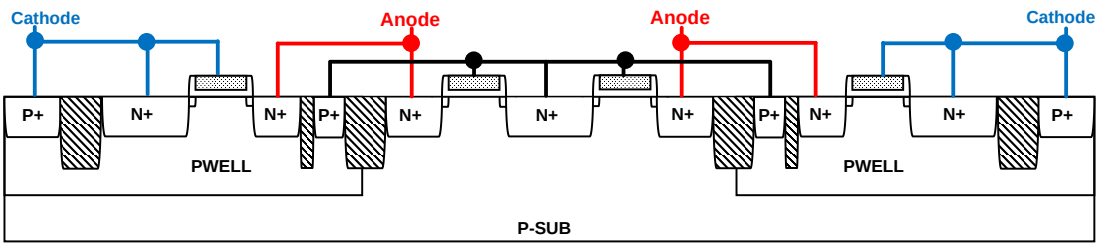
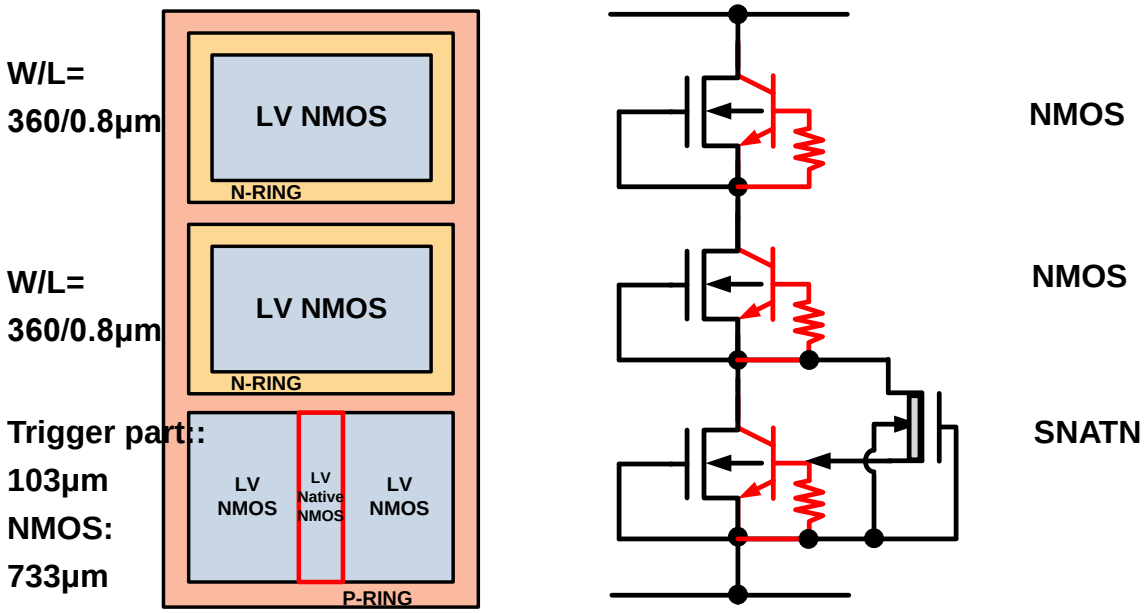



Fig. 4.9 The cross-section view of self-native-NMOS-triggered NMOS




(a) (b)

Fig. 4.10 (a) The top view and (b) the equivalent circuit of the stack of 2 NMOS and 1 self-native-NMOS-triggered NMOS in series

*4.4.2 Experiment Results*

The TLP and Tek370 measurement is shown in Fig. 4.11 and Table 4.3. The devices' holding voltage is as high as triple Vh_unit, but their trigger point is a little delayed from double Vt1_unit. The trigger voltage is slightly larger than double Vt1_unit. In Tek370 measurement, the holding voltage gets improved, and the trigger voltage is also slightly larger than double Vt1_unit.

In this stacking configuration, the holding voltage can increase by stacking, and the turn-on speed is improved by using SNATN as the third block in the stack. The best curve, Nx2+ SNATN(L=0.7μm), is the closest to the ideal case, and that stack's holding voltage is 18.05V in Tek370 measurement and the trigger voltage is 23.90V in TLP measurement.

The device, stack of 2 NMOS and 1 SNATN with length 0.7μm, is also examined by transient-induced latchup test. Fig. 4.12 shows the pictures from the oscilloscope. In Fig. 4.12(a), the device is supplied by 18V. After the transient pulse from MM source, the devices

keep the voltage at 18V with no current. That means the device doesn't suffer latchup and the device's holding voltage is above 18V. In Fig. 4.12(b), the device is biased at 20V. After the transient noise from MM source, the device clamps the voltage at 18.4V, and latchup occurred with large current.

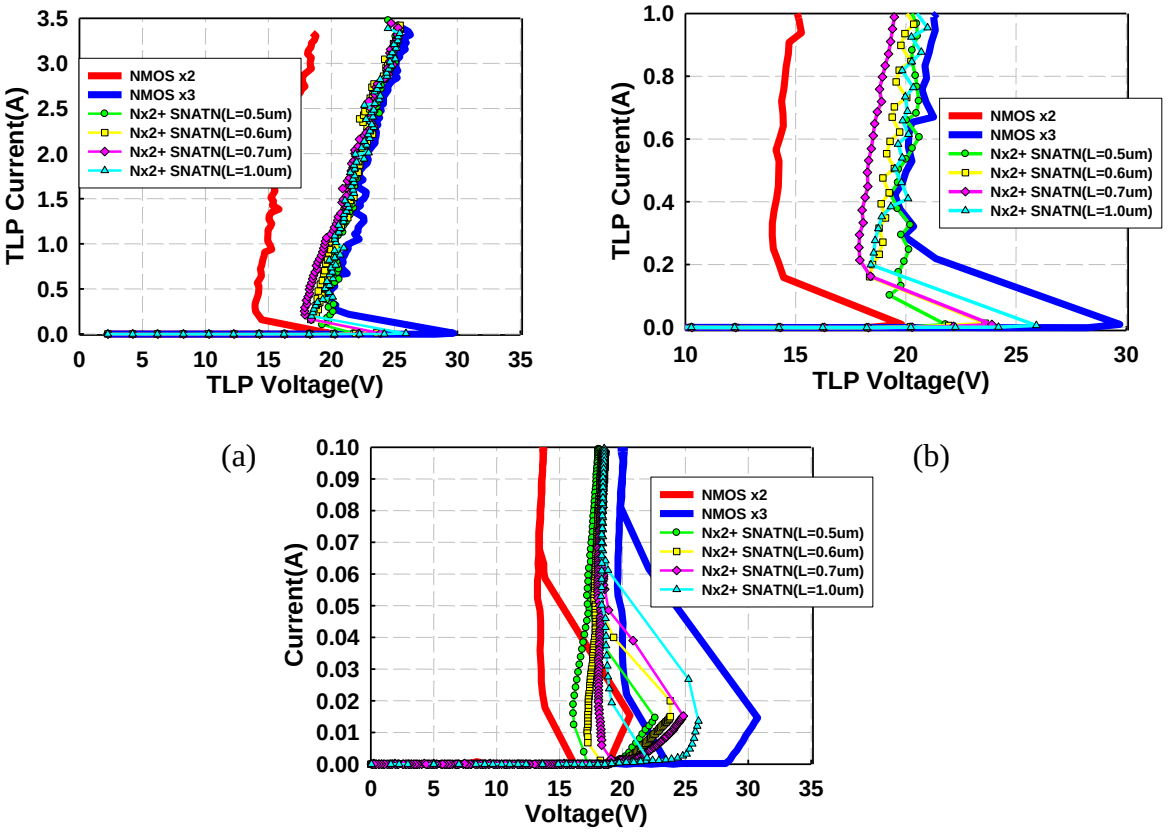
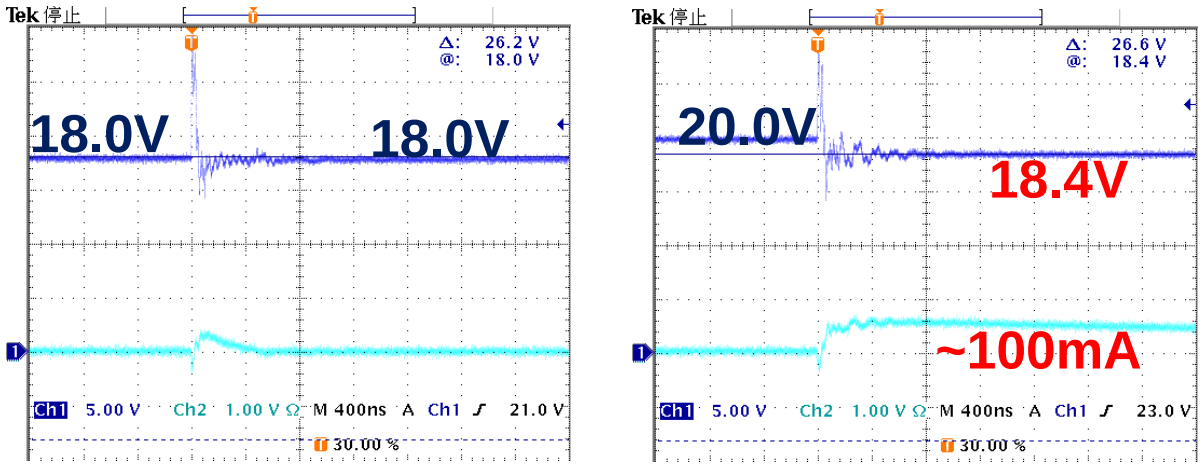



Fig. 4.11 (a) The TLP I-V curves of stacking with SNATN (b) in a low current level (c) The Tek370 I-V curves of stacking with SNATN

Table 4.3

The characteristics of stacking with SNATN

| | TLP | | Tek370 |
|---|---|---|---|
| | $V_{t1}$(V) | $V_h$(V) | $V_h$(V) |
| NMOSx 2 | 19.81 | 13.94 | 13.25 |
| NMOSx 3 | 29.71 | 19.50 | 19.60 |
| Nx2+SNATN (L=0.5 μm) | 21.80 | 19.27 | 16.10 |
| Nx2+SNATN (L=0.6 μm) | 23.60 | 18.36 | 17.25 |
| Nx2+SNATN (L=0.7 μm) | 23.90 | 17.87 | 18.05 |
| Nx2+SNATN (L=1.0 μm) | 25.92 | 18.41 | 18.40 |




(a) (b)

Fig. 4.12 TLU measurement with (a) 18V (b) 20V supply

## 4.5 Summary

It is supposed that the holding voltage of a 3-NMOS stack is the target in the ESD protection window. Reducing the 3-NMOS stack's trigger voltage can enhance turn-on speed. Replacing the last NMOS in the stack with native NMOS can reduce the trigger voltage. However, the holding voltage is not high as triple Vh_unit due to its large leakage.

Native-NMOS-triggered NMOS (NATN) is also served as the last block of a stack for stronger ESD robustness and triple Vh_unit, but it takes additional area. Self-native-NMOS-triggered NMOS (SNATN) is more compact in area. Embedding native NMOS in the middle of the NMOS array is a good way to implement.

The stack of 2 NMOS and 1 SNATN(L=0.7μm) in series has fabricated. It can reduce trigger voltage by 5.8V, and its holding voltage is about 18V. The holding voltage is also verified by TLU measurement.

# Chapter 5

# Conclusions and Future Work

Stacking LV devices for ESD robustness and latchup-free design is carefully examined and verified in this thesis.

## 5.1 Conclusions

Stacked NMOS, stacked PMOS and stacked PFOD have been verified their good ESD robustness with high holding voltage. Even the 10-devices stack can also keep the same $I_{t2}$ and an ESD level with 10 times holding voltage with isolation rings. ESDN-implant can be used to increase ESD robustness more. The 10-NMOS stack can survive 6.0Kv in HBM, and its holding voltage is 63V in a VIS 0.25-μm BCD process. The 10-PMOS can pass 5.0Kv in HBM, and its holding voltage is 91V in a VIS 0.25-μm BCD process. Table 5.1 shows the overall information.

Stacked devices are fabricated in line and folded configuration. In both configuration, stacked devices are both good at ESD robustness and high holding voltage. Stacking in different shapes is applicable. The area of stacked devices is flexible for the layout.

Replacing the last NMOS with native NMOS is a good way to increase turn-on speed. Native NMOS with small threshold voltage is an already-on device, but the $I_{t2}$ of native NMOS is not high enough. Using native-NMOS-triggered NMOS (NATN) can reach a higher ESD level. Self-native-NMOS-triggered NMOS (SNATN) can be implement in more compact area. Inserting native NMOS into the middle part of NMOS array makes more compact area. The best stack of 2 NMOS and 1 SNATN can reduces trigger voltage by 5V. Table 5.2 shows the overall information.

Table 5.1

Summary of stacked devices in a VIS 0.25-μm BCD process

| | Area(μm$^2$) | $V_{t1}$(V) | $V_h$(V) | $I_{t2}$(A) | HBM(kV) |
|---|---|---|---|---|---|
| **Stacked NMOS series (1~10)** | 7208~ 66071 | 9.88~ 100.59 | 6.32~ 63.76 | 3.3 | 6.0 |
| **Stacked PMOS series (1~10)** | 7208~ 66071 | 8.91~ 87.64 | 8.78~ 87.64 | 2.7 | 5.0 |

Table 5.2

Summary of stacked NMOS with native NMOS in a VIS 0.25-μm BCD process

| | Area (μm$^2$) | TLP | | Tek370 |
|---|---|---|---|---|
| | | $V_{t1}$ (V) | $I_{t2}$ (A) | $V_h$ (V) |
| **NMOSx2** | 13748 | 19.81 | 3.30 | 13.25 |
| **NMOSx3** | 20288 | 29.71 | 3.35 | 19.60 |
| **Nx2+NAN(L=1.0μm)** | 20288 | 19.96 | 2.12 | 14.75 |
| **Nx2+NATN(L=1.0μm)** | 24468 | 21.78 | 3.43 | 16.15 |
| **Nx2+SNATN(L=0.7μm)** | 20288 | 23.90 | 3.39 | 18.05 |

## 5.2 Future Work

*5.2.1 A Diode-Triggered Stack*

A diode string is served as a trigger circuit for the stack in Fig. 5.1. After the diode string has breakdown, the current flows through the resistor to turn on the last NMOS. The trigger voltage would be reduced. Fig. 5.2 is expected I-V curves.

It should be paid attention that the diode string may share some ESD current during the ESD stress of a high current level. The ESD level may be limited by the diode string, so there is a trade-off consideration between diodes' area and $I_{t2}$ of the whole diode-triggered stack.

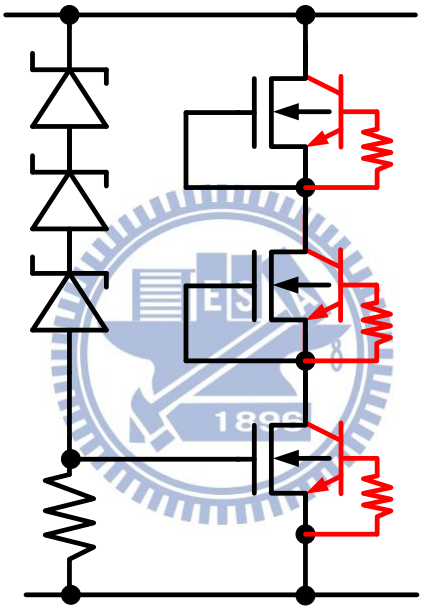


Fig. 5.1 The circuit of a diode-trigged stack

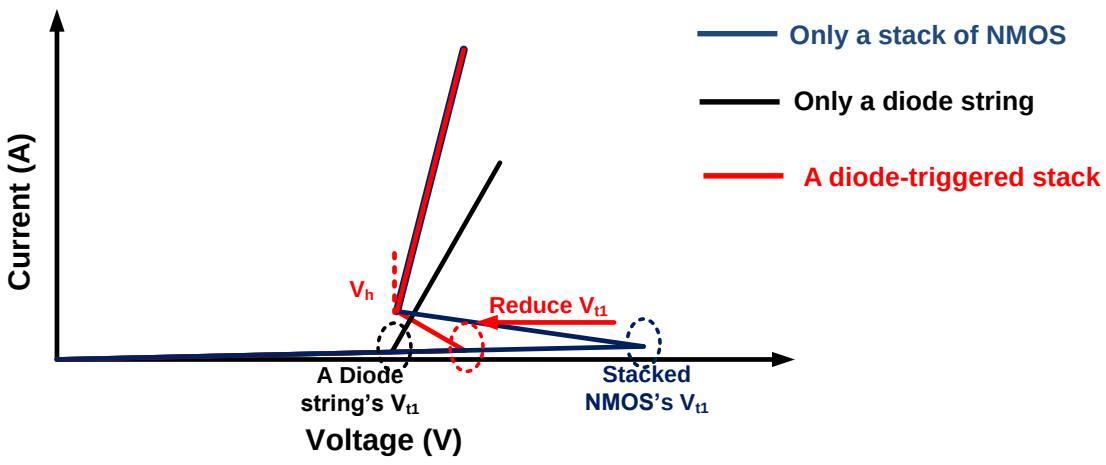



Fig. 5.2 The expected I-V curves of a diode-triggered stack

*5.2.2 A Stack of LV PMOS with HV SCR*

High initial current also can enhance latchup-immunity. The top view of this structure is shown in Fig. 5.3. A stack of PMOS conducts the current first and blocks some noise. After the voltage exceeds the trigger voltage of HV SCR, the device has snapback due to the conducting path of HV SCR. The expected I-V curves is shown in Fig. 5.4.

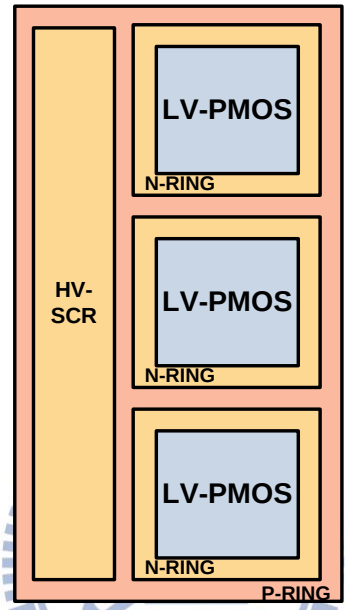



Fig. 5.3 The top view of a stack of LV PMOS with HV SCR

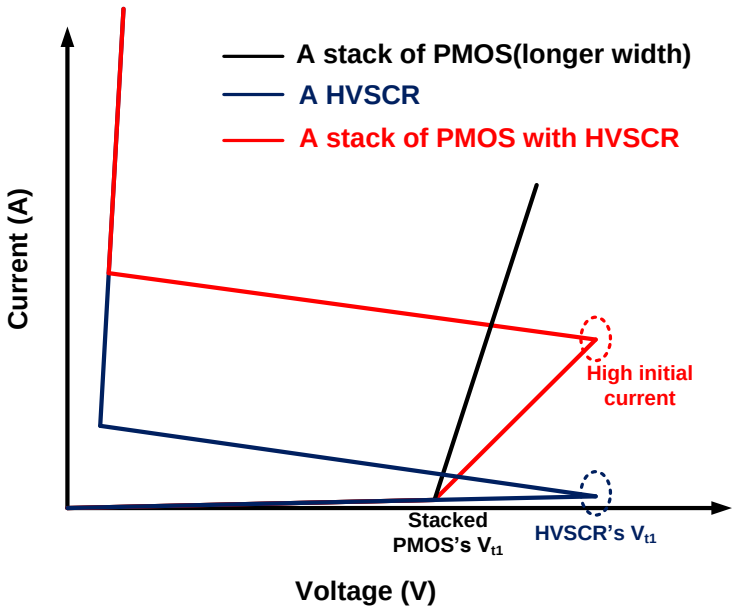



Fig. 5.4 The expected I-V curves of a stack of LV PMOS with HV SCR

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