國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

低溫多晶矽製程之類比積體電路設計與實現

DESIGN AND IMPLEMENTATION OF ON-PANEL ANALOG CIRCUITS IN LOW TEMPERATURE POLY SILICON (LTPS) PROCESS FOR DISPLAY PANEL APPLICATIONS

研 究 生：王 資 閔 (Tzu-Ming Wang)

指導教授：柯 明 道 (Ming-Dou Ker)

中華民國九十九年十月

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中華民國九十九年十月

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摘要

與傳統的非晶矽(amorphous silicon)薄膜電晶體(thin film transistor)相比較，低溫多晶矽(low temperature poly silicon)薄膜電晶體相對具有較高的電子遷移率(mobility)、較低的臨界電壓(threshold voltage)、和較高的生成穩定度，這些特性皆有利於顯示面板上的系統整合，進而使面板達到小巧、高穩定度和高解析度的特點。也因為這些特點，使得低溫多晶矽技術被視為最理想技術之一，期能應用在可攜式系統上，像是數位相機、手機、個人數位助理等，進而達到系統面板(system-on-panel)之應用。此外，系統面板之應用，在未來也會因為較低製作成本和較短的產品生成時間而一步一步的被實現。在過去幾年內，為了達到系統面板之應用，一些面板週邊的電路，像是直流-直流轉換器(DC-DC converter)、暫存器(register)、驅動電路(driver circuit)和數位至類比轉換器(DAC)等皆已被整合在玻璃基板上。另外，一些應用於不同方向且整合在玻璃基板上的出色研究也相繼被提出來，像是中央處理器(CPU)、記憶體、帶隙參考電壓電路(bandgap reference circuit)和射頻識別(RFID)標籤解調器(demodulator)。

雖然在低溫多晶矽製程中，利用加大多晶晶格來增加了元件的效能，但是這也在液晶面板上，造成了元件和元件間的隨機變異。而不規則的晶界、閘極絕緣界面的缺限、和在通道上的不完整離子摻雜也對低溫多晶矽的薄膜電晶體的電性特性造成了變異。一些像是熱載子應力、負偏壓溫度不穩定性和一些可靠度的問題已經證實，多晶膜電晶體的不穩定性是比單晶的

矽製程金氧半場效電晶體還要更為嚴重。此外，在低溫多晶矽製程上的元件特性變異，相較於互補式金氧半導體製程而言也是更為嚴重。因此在實現低溫多晶矽製程之積體電路設計上，這些元件的變異性也是必需被考慮的。

在第二章中，本論文提出了玻璃基板上具有伽瑪校正(gamma correction)功能之六位元折疊(folded)電阻串數位至類比轉換器。藉著折疊電阻電路(folded R-string circuit)、分割的數位解碼器(segmented digital decoder)和重新排序之解碼電路(reordering decoding circuit)，所提出之數位至類比轉換器與傳統的電路比較，可以有效的降低約六分之一的面積。

在第三章中，本論文提出了兩個具有位準轉換功能並包含伽瑪校正數位至類比轉換器之類比輸出緩衝器。利用了運算放大器(OPAMP)、解碼器、電阻串、開關和具有 3-V 伽瑪校正之數位至類比轉換器，所提出之第一個類比輸出緩衝器可以直接驅動 5-V 的液晶面板(liquid crystal panel)，而不用重新設計適用於 5-V 伽瑪校正之數位至類比轉換器。

本論文第四章提出了一應用於觸碰式面板之玻璃基板上讀出電路。所提出之電路利用了開關-電容(switched-capacitor)技巧，來加大因為觸碰式面板的電容變化而造成的電壓差，並且也採用了相關性雙採樣(correlated double sampling)之技巧來降低因為製程變異而導致的偏移(offset)。所提出之電路最低可判別的電壓差為 40 mV，並且可利用 4 位元的數位輸出來分辨觸碰到之面積。

第五章提出一應用於觸碰式面板之玻璃基板上具有數位校正(digital correction)功能的讀出電路。此電路包含了轉導(Gm)放大器、計數器(counter)和數位校正電路。所提出之電路只需要小部份之類比電路，並利用數位校正電路來補償低溫多晶矽製程造成的較大製程變異和較差的元件特性。跟第四章所提之電路相比較，本章所提之電路具有較低的電路複雜度、較低的功率消耗和較簡單的補償方式，但是相對而言，也因此需要較大的電路面積和會有較低的操作頻率。

第六章則是總結了本篇論文的主要結果，並且提出一些未來可以改善或新應用的建議。

DESIGN AND IMPLEMENTATION OF ON-PANEL ANALOG CIRCUITS IN LOW TEMPERATURE POLY SILICON (LTPS) PROCESS FOR DISPLAY PANEL APPLICATIONS

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Abstract

Compared with conventional amorphous silicon (a-Si) thin film transistors (TFTs), some characteristics, such as higher carrier mobility, lower threshold voltage, and higher stability, of low temperature poly silicon (LTPS) TFTs can achieve compact, highly reliable, and high resolution for system integration within a display panel. For these features, LTPS technology is conceived as one of most desirable technology to accomplish realization of system-on-panel (SOP) application for portable systems, such as digital camera, mobile phone, personal digital assistants (PDAs) and so on. In addition, SOP application will be implemented step by step in the future to reduce the fabrication cost and shorten the product lead time. In the past few years, some peripheral circuits of display panel, like DC-DC converter, register, driver circuits, and digital-to-analog converter (DAC), had been integrated on glass substrate for SOP application. Furthermore, some remarkable advances had also been implemented on glass substrate, such as central processing unit (CPU), memory, bandgap reference circuit, and demodulator for RFID tags.

Although using LTPS process can enlarge poly-grain size to improve the device performance, it usually accompanies a random device-to-device variation on LCD panel. The harmful effects of irregular grain boundaries, gate-insulator interface defects, and incomplete ion-doping activation in thin poly-silicon channels result in the variation on electrical

characteristics of LTPS TFTs. Some properties such as hot carrier stress (HCS), negative bias temperature instability (NBTI), and reliability issues have been proved that the instability of polysilicon TFTs is more serious than that of single-crystalline silicon MOSFETs. In addition, the device characteristic variations in LTPS technology are also quite larger compared with CMOS technology, so the effect of device variation must be considered for on-panel circuit design.

In chapter 2, a 6-bit folded R-string DAC with gamma correction on glass substrate is designed and verified in 3-μm LTPS technology. By using the folded R-string circuit, segmented digital decoders, and reordering decoding circuit, the area of the new proposed DAC circuit can be effectively reduced to about one sixth of the traditional one.

In chapter 3, two analog output buffers with level shifting function on glass substrate for panel application is designed and fabricated in a 3-μm LTPS technology. By using OPAMP, decoder (decoder 2), R-string (R1, R201-R237), switches (MR01-MR37), and DAC with 3-V gamma correction parameters, the new proposed analog output buffer I can drive 5-V liquid crystal panel without re-designing the DAC with 5-V gamma correction parameters.

In chapter 4, a new on-panel readout circuit for touch panel applications is designed and fabricated in a 3-μm LTPS technology. The switched-capacitor (SC) technique is applied to enlarge the voltage difference from the capacitance change of touch panel, and the correlated double-sampling (CDS) technique is also employed to reduce the offset owing to process variation. The minimum detectable voltage difference of the proposed circuit is 40 mV, and the different touch area can be identified by the 4-bit digital output.

In chapter 5, a new on-panel readout circuit with digital calibration, which contains transconductance amplifier, counter, and digital correction circuit, for touch panel applications is designed and verified in a 3-μm LTPS technology. In the proposed circuit, only a small amount of analog circuitry is required and larger variation and worse device characteristics in LTPS process can therefore be compensated by the digital calibration circuit. Compared with proposed circuit in chapter 4, the proposed circuit in chapter 5 shows lower circuit complexity, lower power consumption, and easier calibration methodology. On the contract, the proposed circuit in chapter 5 also presents larger layout area and lower detection speed.

Chapter 6 summarizes the main results of this dissertation. Some suggestions for the future works are also addressed in this chapter.

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王　資　閔

謹誌於竹塹交大

九十九年　十月

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Chapter 1

Introduction

In this chapter, the background of this dissertation is discussed. First, thin-film-transistor (TFT) liquid crystal display (LCD) is discussed. Then, low temperature poly-silicon (LTPS) technology, system-on-panel (SOP) application, and design consideration for on-panel circuit are introduced. Finally, the rest of this dissertation is organized.

1.1 Thin-Film-Transistor Liquid Crystal Display [1]-[17]

The liquid-crystal display (LCD) industry has shown rapid growth in consumer electronic markets, namely, computers, monitors, mobiles, and televisions. For high-speed communication networks, the emerging portable information tools are expected to grow in following on the rapid development of display technologies. Thus, the development of higher specification is demanded for LCD as an information display device. Moreover, the continual growth in network infrastructures will drive the demand for displays in mobile applications and flat panels for computer monitors and TVs. The specifications of these applications will require high-quality displays that are inexpensive, energy-efficient, lightweight, and thin.

Amorphous silicon (a-Si) thin-film transistors (TFTs) are widely used for flat-panel displays. However, the low field-effect mobility (ability to conduct current) of a-Si TFTs allows their application only as pixel switching devices; they cannot be used for complex circuits. In contrast, the high driving ability of polycrystalline Si (p-Si) TFTs allows the integration of various circuits such as display drivers. Eliminating LSI (large-scale integration) chips for display drivers will decrease the cost and thickness of displays for various applications.

There are high-temperature and low-temperature poly-Si TFTs, defined by the maximum process temperature they can withstand. The process temperature for high-temperature poly-Si can be as high as 900°C. Hence, expensive quartz substrates are required, and the profitable substrate size is limited to around 6 inch (diagonal). Typical applications are

limited to small displays. The process temperature for low-temperature poly-Si (LTPS) TFTs, on the other hand, is less than 600°C, which would allow the use of low-cost glass substrates. This makes possible direct-view large-area displays—for example, UXGA (ultra extended graphics array) monitors of up to 15.1 inch (diagonal) with a resolution of 1600 x 1200 pixels. For this reason, LTPS technology has been applied to not only small-sized displays, but also medium- and large-screen products.

1.1.1 History of TFT LCD

Thin-film-transistor (TFT) liquid crystal display (LCD) is a flat display within liquid-crystal inside the display and each pixel is controlled by a TFT. The market of TFT LCD is growing in consumer electronics, computers, and communication systems. The concept of TFT LCD was first mentioned in 1966. In 1966, the possibility of using TFTs as display switch was mentioned by Weimer. A sandwich cell consisting of a transparent front electrode, a reflecting back electrode, and nematic liquid-crystal in between, was proposed by Heilmeier in 1968. When there was no applied field, the cell displays black. When a dc voltage was applied, the liquid crystal became turbulent and scattered light: the cell appeared white. For active-matrix LCD, the diode or transistor utilized as switch and storage capacitors implemented in parallel were mentioned in 1971. In 1973, Brody proposed the CdSe TFT for active-matrix liquid crystal panel with 14000 transistors, storage capacitors, and twisted-nematic (TN) liquid crystal cell, where TN liquid crystal cell was first mentioned by Schadt and Helfrich, and presents low-voltage operation, low power consumption, and fast response time.

After that, the development of practical TFT LCD has been studied and implemented for more than thirty years with many novel applications. In addition, TFT LCD exhibits higher contrast, larger viewing angle, and faster response time compared with that of traditional LCD. Therefore, TFT LCD panel grows rapidly for large panel application, like television, and for small panel applications such as digital camera, mobile phone, personal digital assistants (PDAs) and so on.

1.1.2 Configuration of TFT LCD

The structure of thin-film-transistor liquid crystal display is shown in Fig. 1.1 with two glass substrate, TFT array substrate and color filter substrate, and liquid crystal is filled in the center of LCD panel. A backlight module including an illuminator and a light guilder is also

needed since liquid crystal molecule cannot light by itself. However it usually consumes the most power of the system, some applications such as mobile communications try to exclude or replace it from the system. Although the pixel transparent are reduced by opaque TFT, which means a brighter backlight is required, the increased isolation between adjacent pixels can reduce the leakage current between the top and bottom substrate. In order to obtain better display quality, the cell gap of the liquid crystal, which is the spacer between two glass substrates, has to be precisely controlled to a specific value, e.g., 5 μm. This gap must be uniform and reproducible over the whole display area. Therefore, transparent spacers such as plastic beads are placed on the surface of the glass substrate.

In TFT array substrate, there is a polarizer, a glass substrate, a transparent electrode, and an orientation layer. In color filter substrate, there is an orientation layer, a transparent electrode, color filters, a glass substrate and a polarizer. Most transparent electrodes are made by ITO, and they can control the directions of liquid crystal molecules in each pixel by voltage supplied from TFT on the glass substrate. Color filters contain three original colors, red, green, and blue (RGB). As the degree of light, named “gray level”, can be well controlled in each pixel covered by color filer, more than million kinds of colors can be obtained.

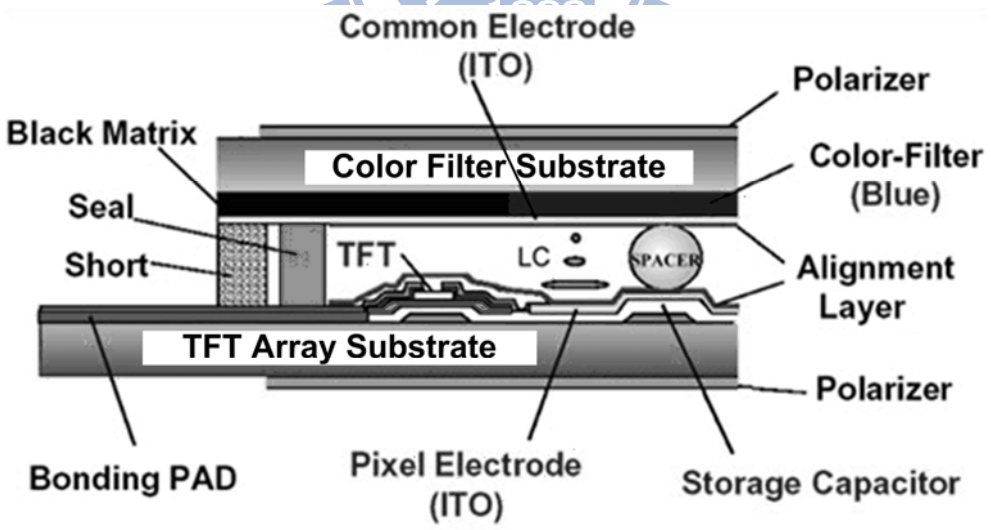


Fig. 1.1. The structure of thin-film-transistor liquid crystal display.

Most liquid crystal cell are twisted-nematic type in which the director (orientation) of the liquid crystal molecules is twisted 90° between the TFT substrate and the common electrode substrate. The polarizer can block or pass the light by changing the phase of the

polarizer. In general, the first polarizer of a couple of polarizers is called *polarizer* as well as the second one is called *analyzer*. The light is blocked by a couple of polarizers with 90° phase error, which is shown in Fig. 1.2 (a). If the liquid crystal molecule is twisted by applying the specific electric field across it, the light still can pass the polarizer due to the direction of liquid crystal molecules varying with electric field and it can guide the light along the long axis, shown in Fig. 1.2 (b).

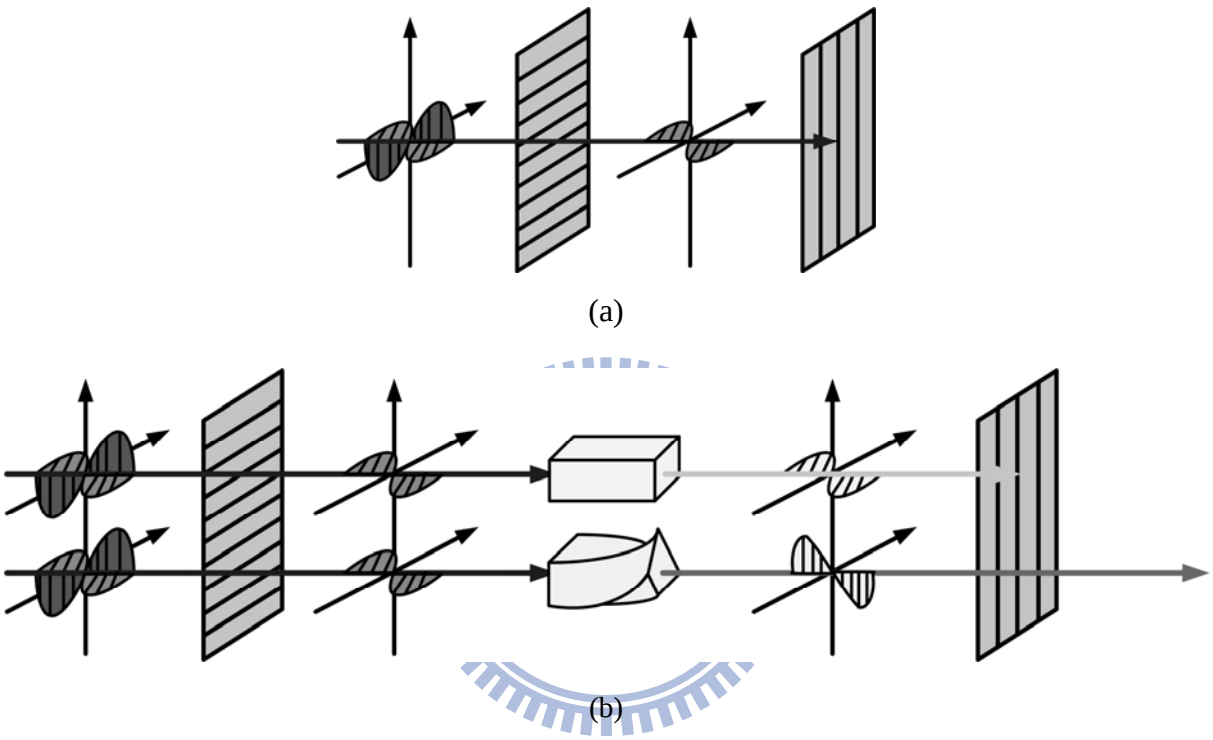


Fig. 1.2. (a) A couple of polarizers with 90° phase error and (b) a couple of polarizers with liquid crystal.

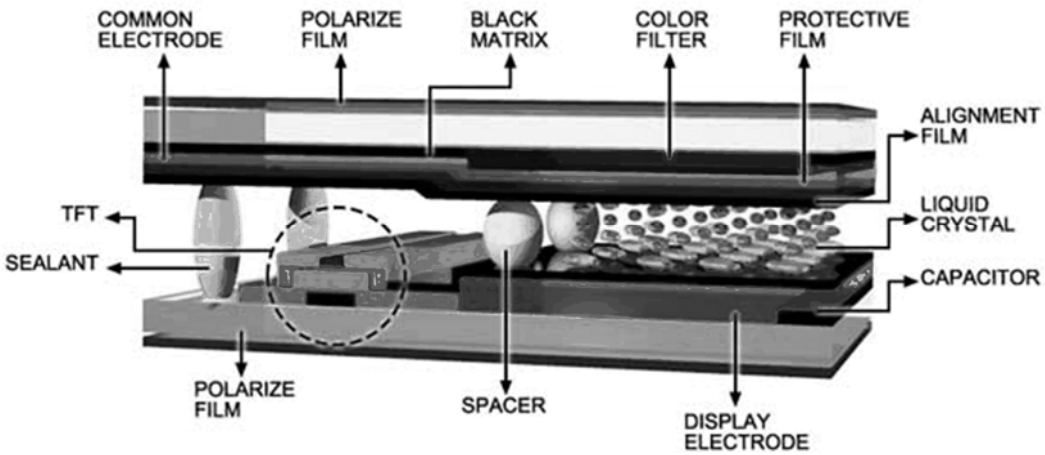


Fig. 1.3. The cross section of an AMLCD sub-pixel.

One dot is the most fundamental unit of LCD panel and each dot can express one kind of original color. Because one full color should be mixed with three original colors, each pixel contains three dots. As a result, if the resolution of gray level of each dot is 8 bits, then the whole panel can show 16,777,216 (28×28×28) kinds of colors at all. Fig. 1.3 shows the cross section of an AMLCD sub-pixel.

Fig. 1.4 and Fig. 1.5 show the layout and equivalent circuit of each sub-pixel, including two major structures, the C_S on common mode and C_S on gate mode. The right-down region of the sub-pixel layout is the TFT switch, and the region of each sub-pixel area excluding TFT switch and storage capacitor (C_S) is called aperture region, which is the largest window for light passing. So the larger ratio of aperture region to pixel area is the better performance of the TFT-LCD panel. In Fig. 1.5, the M_S is a thin film transistor as a switch. The C_{lc} is the effective capacitor of liquid crystals, and C_S is the storage capacitor used to maintain the voltage level of liquid crystals during the hold time of frame transitions. The C_{gd} is the parasitic capacitor between gate line and effective liquid crystal capacitor. The structure, C_S on gate, which connects the bottom of the storage capacitor to the previous row of the gate line has some benefits. By this structure, we can compensate the unstableness of voltage level due to the clock feed-through effect from C_{gd}. Furthermore, this structure also has larger aperture ratio. But the trade-off with the C_S on gate method is an increase in the RC time constant of the gate line, which reduces the TFT switching performance.

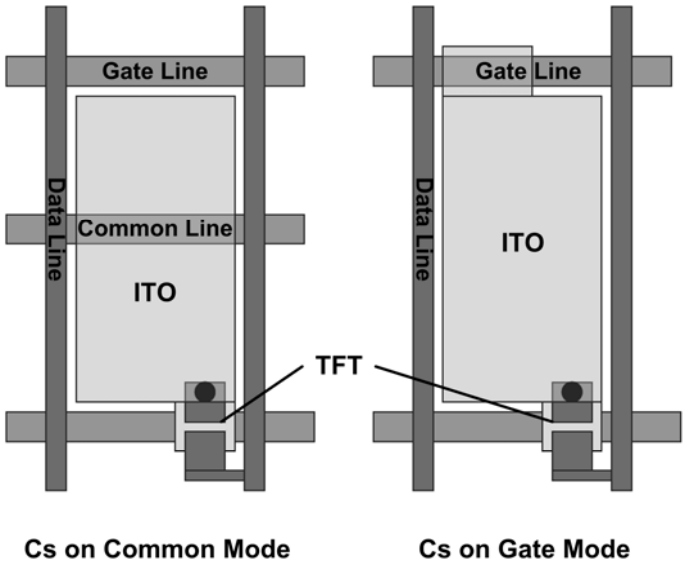


Fig. 1.4. The layout view of a TFT-LCD sub-pixel: (a) CS on common mode and (b) CS on gate mode.

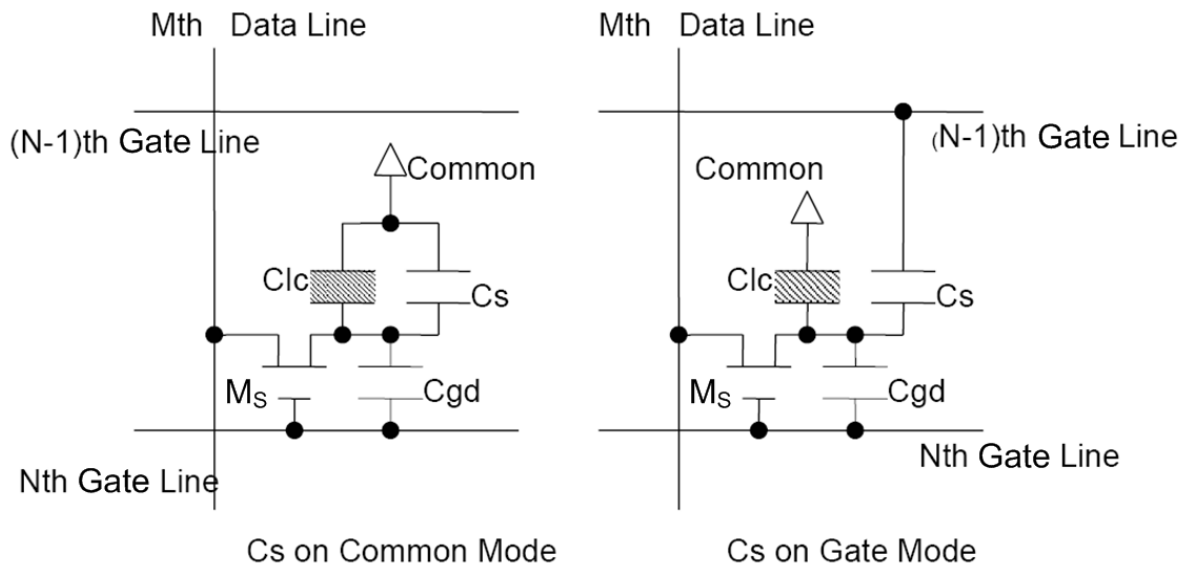


Fig. 1.5. The equivalent circuit of a TFT-LCD sub-pixel: (a) CS on common mode and (b) CS on gate mode.

The periphery circuit blocks of LCD panel are roughly composed of four parts-display panel, timing control circuit, scan driver circuit, and data driver circuit. Fig. 1.6 shows the block diagram of the TFT-LCD panel circuits. Display panel is constructed of the active matrix liquid crystals and the operation of the active matrixes is similar to DRAM (dynamic random access memory) which is used to charge and discharge the capacitor of the pixel. Timing control circuit is responsible for transmitting RGB (red, green, and blue) signals to the data driver and controlling the behavior of scan driver. As soon as one voltage level of the scan lines rises, the RGB signals are transmitted through the data driver. After a period, the voltage level of this scan line is disabled and next scan line is turned on. All voltage levels of those scan lines are raised in turn.

Scan driver circuit consists of shifter register, level shifter, and digital output buffer. Shifter register is used to store digital input signals then transit to the next stage according to timing control circuit. Because the turn-on voltage of active matrixes is higher, scan driver should drive the active pixels with a high voltage. The purpose of the level shifter is to convert the digital signal to higher voltage level. Finally, since the scan lines can be modeled as RC (resister and capacitor) ladder, the digital output buffer should be used in the last stage for driving the large load.

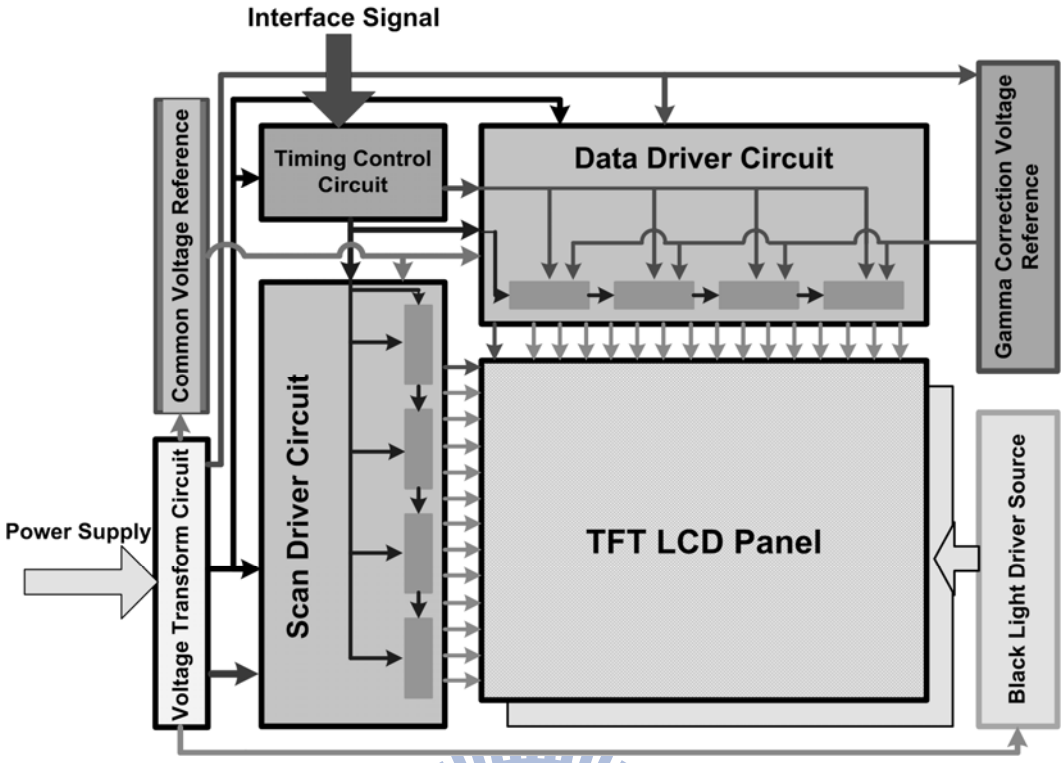


Fig. 1.6. The block diagram of TFT-LCD panel circuits.

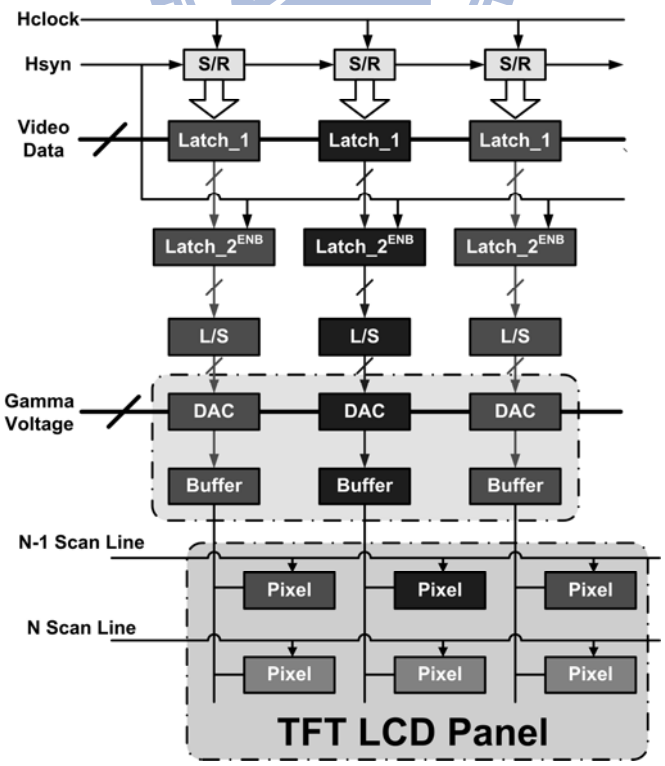


Fig. 1.7. The basic diagram of data driver circuit for TFT LCD panel.

Data driver circuit, shown in Fig. 1.7, is composed of shifter register, data latch, level shifter, digital-to-analog converter (DAC), and analog output buffer. The first three parts classify as digital architectures, and the other two parts belong to analog architectures. Shifter register and data latch manage to transit and store the RGB signals. Also, the purpose of level shifter is the same as the one in scan driver circuit, which is applied to translate the RGB signal to a higher level voltage. In addition, digital-to-analog converter is used to convert the digital RGB signal to analog gray level. The analog output buffer is applied to drive active pixels into a desired gray level. However, the LCD panel usually has large load, especially in larger panel display or higher resolution display, so the analog output buffer should enhance the driving capability of the data driver.

1.2 Low Temperature Poly-Silicon Technology [6]-[8]

As the developing of digital life and growing of flat display market, low temperature poly-silicon (LTPS) technology has become an important feature for high image quality display due to the high performance and high resolution. Compared with conventional amorphous silicon (a-Si) thin film transistors (TFTs), some characteristics, such as higher carrier mobility, lower threshold voltage, and higher stability, of low temperature poly silicon (LTPS) TFTs can achieve compact, highly reliable, and high resolution for system integration within a display panel.

1.2.1 Background

In 1991, the 400 dpi image sensors including poly-Si TFT scanning circuits, readout circuits, and a-Si photodiodes fabricated on borosilicate glass had been developed [19]. This was the first contact type image sensor with TFT analog buffer amplifiers. The operating frequency range of scanning circuits is between 200 kHz and 1 MHz. The readout circuits incorporating TFT analog impedance converters decrease photodiode impedance by more than three orders of magnitude and improve the linearity between illumination intensity and the sensor output. High-resolution reading is achieved by the new contact type linear image sensors with a storage time of 2 ms/line. In [20], a 2.15 inch diagonal, QCIF (144xRGBx176) reflective color TFT-LCD with digital memory on glass (DMOG) technology, using LTPS technology was proposed. This panel was able to display 4bit x RGB (4096-colors) images and 1bit x RGB (8-colors) still image in power save mode (still mode). Using DMOG technology, peripheral driving circuits and the controller IC can be suspend, and the low

power consumption can be achieved. This technology can be used not only for mobile telephones but also other mobile apparatuses like electric books, because low power consumption is the key requirement for mobile apparatuses. The production of LTPS TFT LCDs has been increased years by years, and the production technology has also been improved for different sized LCD products to integrate various types of circuits. The LTPS technology is one of the most important features for TFT LCD panel applications.

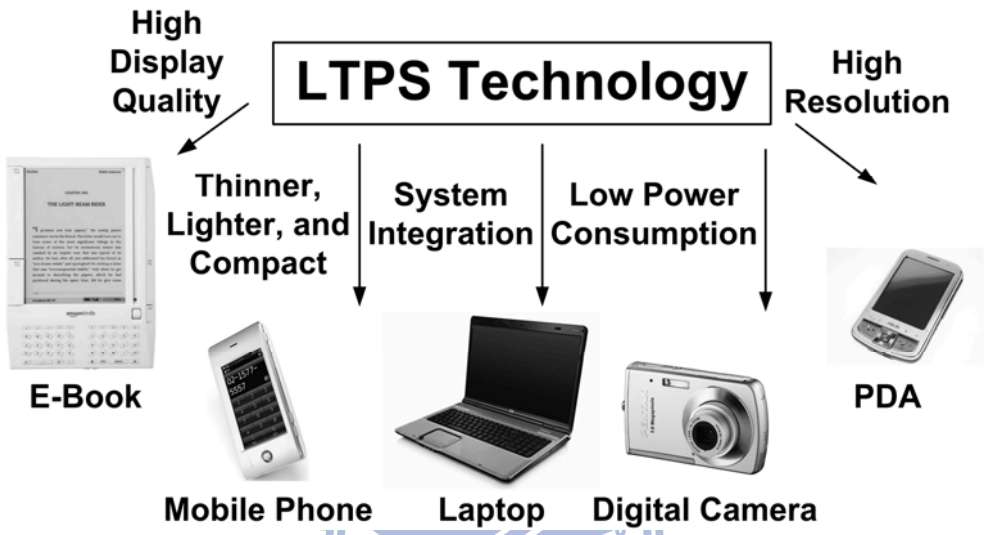


Fig. 1.8. The application of LTPS technology on TFT-LCD panel.

Fig. 1.8 shows the applications of LTPS technology on TFT-LCD panel. LTPS-TFT can be utilized not only for the switches on panel but also for some other applications: static random access memories, nonvolatile memories [21], linear image sensor [22], photo-detector amplifier, digital cameras, personal digital assistant, and so on, due to its higher carrier mobility, lower threshold voltage, and higher stability. Although the preparation of LTPS film is apparently more complicated than a-Si, LTPS TFT has 100 times higher mobility than a-Si TFT and can provide complementary circuit on the glass substrate. Some significant advantages for LTPS over a-Si are shown below: (1) the capability for integrating peripheral circuits on glass substrate can decrease peripheral dimension and fabrication cost, (2) higher aperture ratio can be achieved by higher mobility of LTPS TFT because the pixel size can be further reduced. Therefore, there are more additional pixel areas for light transmission. (3) Vehicle for OLED: Higher mobility means ample current supply required by OLED device driving, (4) Module's compactness: Less PCB area required due to the integration of peripheral circuits on Glass [2].

1.2.2 Characteristics and Structures

Fig. 1.9 shows the simplified structure of (a) N-type TFT and (b) P-Type TFT, where N-type TFT has a lightly doped drain (LDD) to decrease the leakage current. In general, the gate of LTPS TFT is on the top of glass substrate (top gate) and the gate of a-Si TFT is on the bottom of glass substrate (bottom gate). The difference between these two structures (LTPS and a-Si) result in some advantages in LTPS TFT such as lower channel resistance, thinner gate oxide isolated layer, thicker gate oxide metal layer, and non-overlap between gate to source/drain.

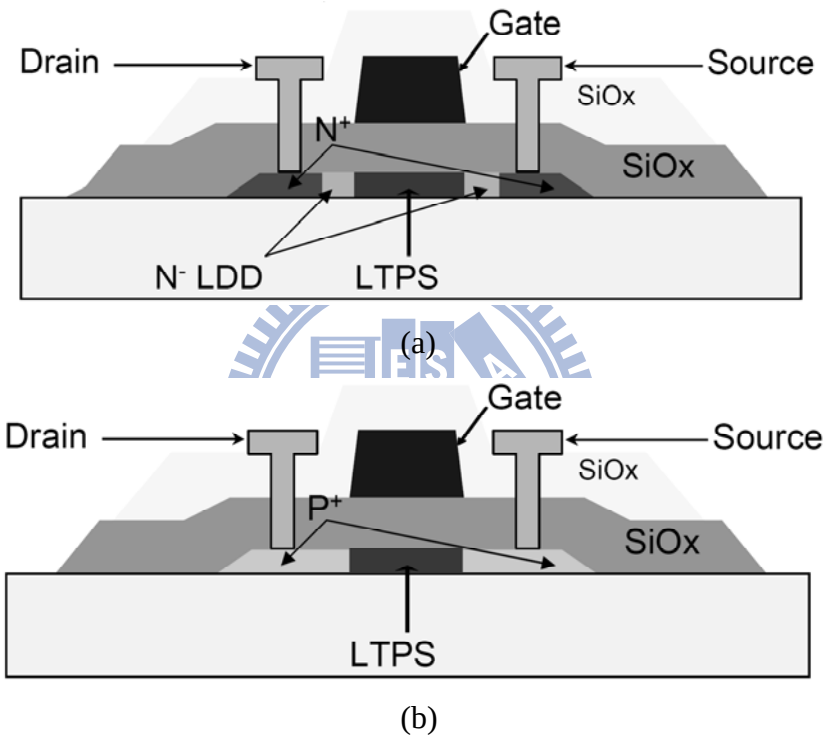


Fig. 1.9. The simplified structure of (a) N-type TFT and (b) P-Type TFT.

Poly-silicon is a silicon-based material, which contains numerous Si grains with sizes ranging from 0.1 to several um. In semiconductor manufacturing, poly-silicon is usually prepared by LPCVD (Low Pressure Chemical Vapor Deposition) and then annealed above 900°C, i.e. so called SPC (Solid Phase Crystallization) method. Obviously, the same way could not be applied to FPD industry since the strain temperature of glass is only about 650°C. Therefore, low temperature poly-silicon (LTPS) technology is the novel technology specific for FPD application. Currently, there are several approaches in the preparation of LTPS film on glass or plastic substrate: Metal Induced Crystallization, Cat-CVD, and Laser

anneal. Metal Induced Crystallization (MIC) is a kind of SPC method but, compared to conventional SPC, it can achieve poly-silicon under lower temperature (about 500°C - 600°C). This is because a thin metal layer is coated before crystallization anneal. The metal element is the key in lowering the activation energy of crystallization. Cat-CVD directly deposits poly-film without further thermal anneal. The deposition temperature has reportedly gone as low as 300°C. The growth mechanism involves the catalytic cracking reaction of SiH_4-H_2 mixture. Laser anneal is the most popular method used currently. Excimer laser is used as an energy source to heat and melt a-Si with low Hydrogen content. It is later recrystallized as poly-film [2].

1.3 System-on-Panel Display Applications

Fig. 1.10 shows the trends for SOP applications. SOP application has the potential to realize compact, highly reliable, and high resolution display by integrating functional circuits within a display. For normal display panel, TABs are connected to the left and bottom sides of a panel with driver ICs. Integration of driver ICs with LTPS TFTs on panel can achieve COG (chip on glass) but it still requires FPC (flexible printed cable) connection on the bottom for other functional circuits. The most common failure mechanism of TFT-LCDs, disconnection of the TABs, is therefore decreased significantly with the save in omitting the usage of ICs and all sub-circuits integrated on panel. Besides, the cost of panel becomes lower, as well as the higher yield rate can be also achieved [23]-[25]. Furthermore, some poly-Si TFT characteristics, such as high carrier mobility, low threshold voltage, high stability, and high reliability, are required to fulfill the SOP application. Such integration technology contributes to shorten the product lead time because the assemblage of CMOS ICs can be eliminated. Currently, such integration has been proceeding from simple digital circuits to the sophisticated ones, and other functional circuits utilized on panel will be also integrated in the future to achieve SOP applications.. Moreover, LTPS technology is compatible with OLED (organic light emitting diode), which is another promising display device. Therefore, design of driving circuits for TFT-LCD in LTPS technology has been proceeding.

SOP application also has a potential of integration of input function other than output function of display, which will pave the way for future displays. These various ways of integration are totally expressed by SOP technology. The input display technology opens opportunities for new applications for personal and business use [26]. The new technology is

scalable up and down, and can be applied to diverse products, from cellular phones to personal computers. The full scope to our imagination concerning future use of “Input Display” is shown in Fig. 1.11. Its wide range of usage will include recording of text or images for on-line shopping and the like, without a scanner device saving personal data and images to a computer, and personal identification, auto-power control with photo-sensor (or ambient light sensor, shown in Fig. 1.12) suitable for extremely low power cellular phone, detecting the position of finger or pen for some touch-sensing (a new touch-panel is shown in Fig. 1.13), and so on.

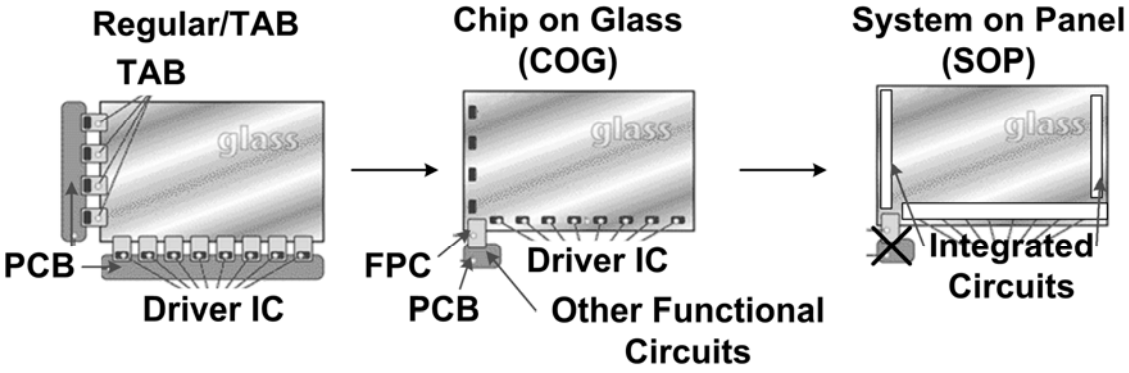


Fig. 1.10. Trends for system-on-panel applications.

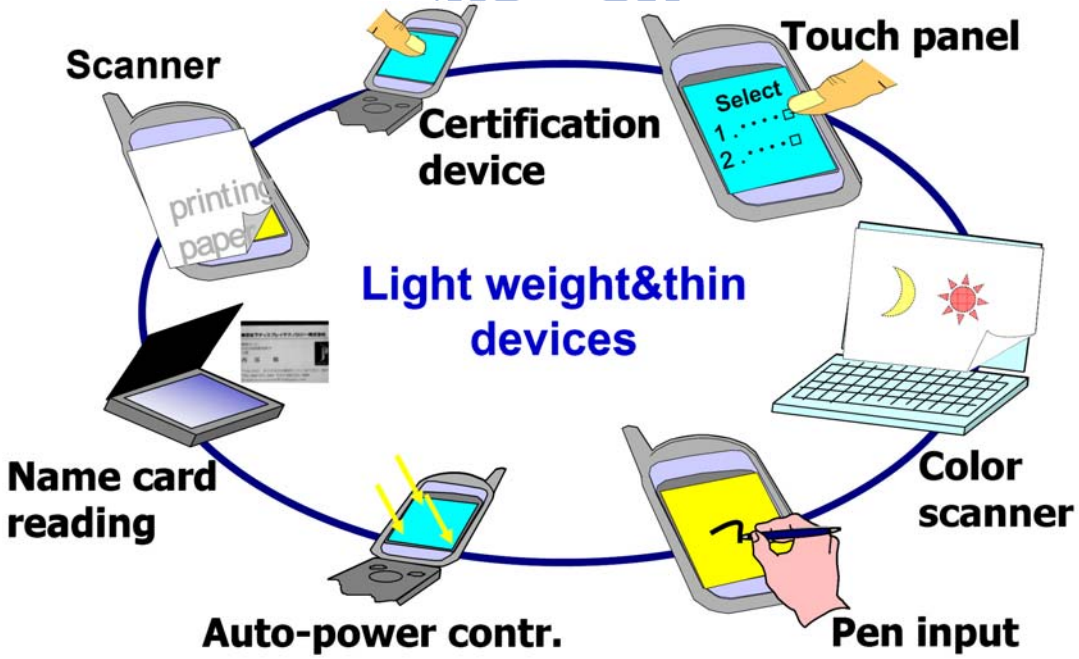


Fig. 1.11. Future application of “Input Display”.

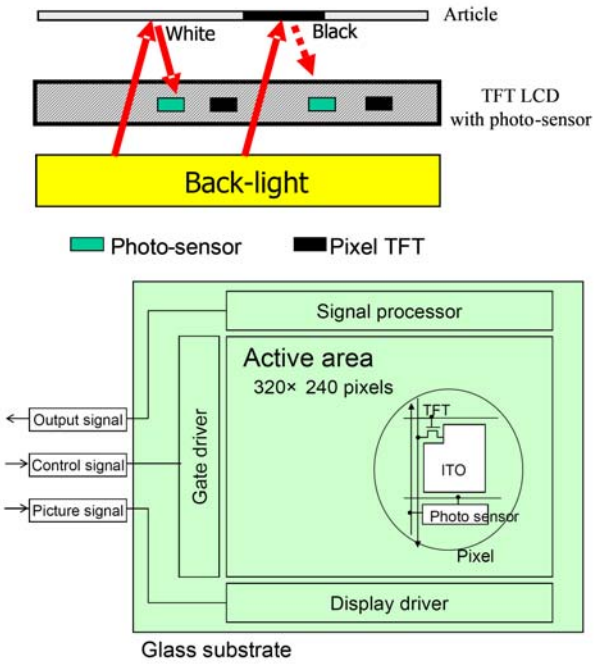


Fig. 1.12. The principle and structure of the photo-sensing display.

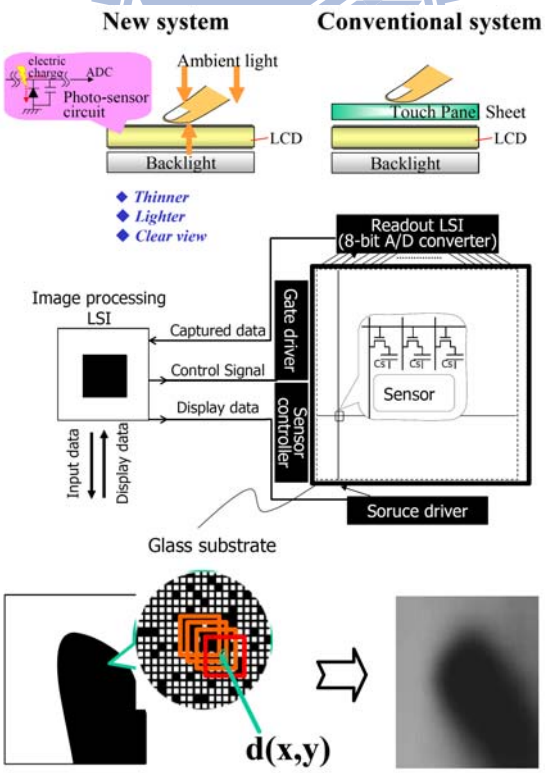


Fig. 1.13. The system architecture and image-capturing finger of this new touch-panel.

The history of touch panel and multi-touch application are reported in [27]-[30]. Touch screens has at least 40-year history. Multi-touch and some of the gestures associated with it, are over 25 years. In 2007, the announcement of Apple iPhone and Microsoft Surface gave a serious boost to interest in touch interfaces-especially those that incorporate multi-touch. After that, touch, multi-touch, and the gesture-based interfaces have become the basic requirement in mobile devices, desktop computers, laptops, and large format displays. In addition, 3-dimensional display also gets great interests in the future SOP applications since 2D display and 2D touch technology cannot satisfy user's requirement at a display interface [31]-[32]. By using the information provided by additional dimension, such systems will enable complex operations to be performed simply and efficiently through intuitive motions of even a single finger. Nevertheless, flexible display is of increasing interest recently, however, there are many technology issues of the manufacturing of displays on flexible substrate [33]-[34]. The substrate, gas barrier, backplane, display mode, and encapsulation are still the major issues since there have been significant advances in flexible optoelectronic devices with organic functional layers in the last few years.

According to above discussion, the fabrication cost will gradually be lowed and SOP (system on panel) will be implemented step by step in the future. Such integration technology contributes to shorten the product lead-time because lengthy development time of ICs can be eliminated. Actually, this integration level has been proceeding from simple digital circuits to the sophisticated ones such as digital-to-analog converters (DACs) [26]. Moreover, LTPS technology is compatible with OLED, which is another promising display device. Therefore, design of driving circuits for TFT-LCD in LTPS technology is worthy expecting in the future.

1.4 Design Consideration for On-Panel Circuit [33]-[39]

From chapter 1.2 and 1.3, the polysilicon TFTs have features of higher mobility, higher reliability, and lower threshold voltage, so SOP applications can be achieved by integrating circuits or systems utilized for panel. Since the maximum process temperature of LTPS is lower than 600°C, LTPS TFTs can be fabricated on a wide variety of cheap glasses to further reduce the cost. However, compared with the requirement as being a switch, polysilicon TFTs requires good electrical stability as being utilized to integrate circuits or systems on panel. Some properties such as hot carrier stress (HCS), negative bias temperature instability (NBTI), and reliability issues have been proved that the instability of polysilicon TFTs is

more serious than that of single-crystalline silicon MOSFETs. Besides, the diverse and complicated grain distribution in the polysilicon file, so polysilicon TFTs suffer serious variation of device behavior, especially in mobility and threshold voltage, which are two important features in the realization of on-panel circuit integration.

Although using LTPS process can enlarge poly-grain size to improve the device performance, it usually accompanies a random device-to-device variation on LCD panel. The harmful effects of irregular grain boundaries, gate-insulator interface defects, and incomplete ion-doping activation in thin poly-silicon channels result in the variation on electrical characteristics of LTPS TFTs. In Table 1.1, the average and standard deviation of mobility variation for n- and p-channel TFTs at hot-carrier and on-current condition were reported [35]. The mobility degradation for n-channel TFTs is more serious at hot-carrier stress condition than that at on-current condition which means that the hot-carrier degradation dominates the mechanism for n-channel TFTs. Fig. 1.14 shows the threshold voltage variation for n-type TFTs in different locations on LCD panel [38]. The variation of threshold voltage for LTPS n-type TFTs in different panel locations has wide distribution from 0.75 V to 2.15 V. In addition, the degradation of (a) n-type and (b) p-type TFTs at different stress conditions are shown in Fig 1.15 [39]. From the aforementioned data reports, the device characteristic variations in LTPS technology are quite larger compared with CMOS technology, so the effect of device variation must be considered for on-panel circuit design.

TABLE 1.1 [35]

MOBILITY VARIATION FOR N-CHANNEL AND P-CHANNEL TFTS

		Average (%)	Std. Dev.
Hot-Carrier	N-Channel	-38.627	6.65
	P-Channel	+7.054	2.72
On-Current	N-Channel	+11.828	3.28
	P-Channel	+2.251	0.6525

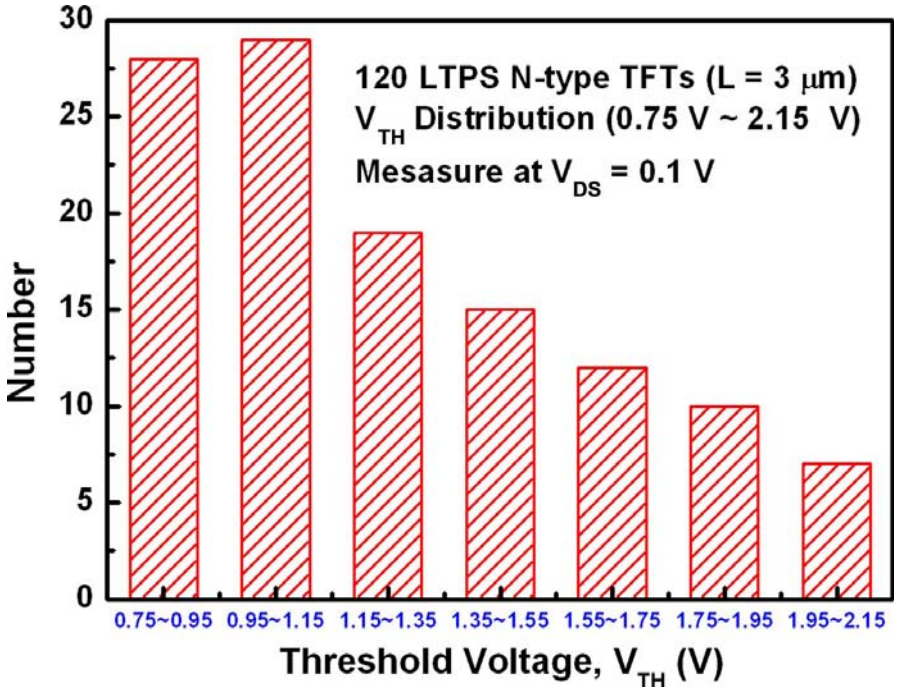
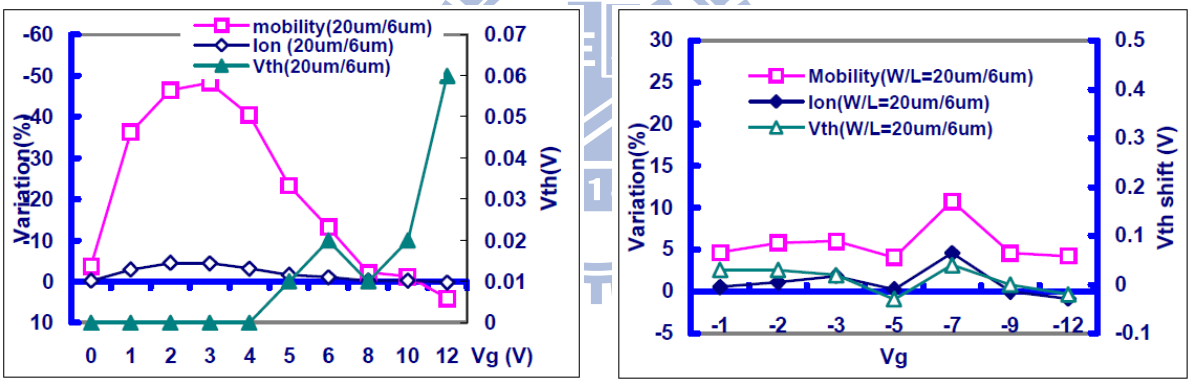


Fig. 1.14. Threshold voltage variation for n-type TFTs in different locations on LCD panels [38].



(a) (b)

Fig. 1.15. The degradation of (a) n-type and (b) p-type TFTs at different stress conditions [39].

1.5 Organization of This Dissertation

In this dissertation, some on-panel analog circuits has been designed and implemented in LTPS process for display panel applications. The functionality and performance of the proposed circuits in this dissertation have been demonstrated by simulated and measured results of the fabricated test chips. The achievements of this dissertation have been published or submitted to international journal and conference papers.

In chapter 2, a 6-bit folded R-string DAC with gamma correction on glass substrate is designed and verified in 3-μm LTPS technology. In chapter 3, two analog output buffers with level shifting function on glass substrate for panel application is designed and fabricated in a

3-μm LTPS technology. In chapter 4, a new on-panel readout circuit for touch panel applications is designed and fabricated in a 3-μm LTPS technology. In chapter 5, a new on-panel readout circuit with digital correction, which contains Gm amplifier, counter, and digital calibration circuit, for touch panel applications is designed and verified in a 3-μm LTPS technology. Chapter 6 summarizes the main results of this dissertation. Some suggestions for the future works are also addressed in the chapter.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Chapter 2

Digital-to-Analog Converter with Gamma Correction on Glass Substrate for TFT-Panel Applications

Low temperature poly-silicon (LTPS) technology has a tendency towards integrating all circuits on the glass substrate. However, the poly-Si TFTs suffered poor uniformity with large variations on the device characteristics due to the narrow laser process window for producing large-grained poly-Si TFTs. The device variation is a serious problem for circuit realization on the LCD panel, so how to design reliable on-panel circuits is a challenge for system-on-panel (SOP) applications. In this work, a 6-bit R-string digital-to-analog converter (DAC) with gamma correction on glass substrate for TFT panel application is proposed. The proposed circuit, which is composed of folded R-string circuit, segmented digital decoder, and reordering decoding circuit, has been designed and fabricated in a 3-μm LTPS technology. The transistor number of the new proposed DAC circuit is effectively reduced to about one sixth compared with the traditional one in the same LTPS process [41]-[42].

2.1 Introduction

Because the electron mobility of LTPS TFTs is about 100 times larger than that of the conventional amorphous silicon (a-Si) TFTs [1], LTPS TFT-LCD technology has some features of compact, highly reliable, and high resolution for system integration within a display. For these features, LTPS technology is suitable for realization of system-on-panel (SOP) application and such a system integration roadmap of LTPS TFT-LCD had been reported in some literature [21]. Besides, the distinctive feature of the LTPS TFT-LCD is the elimination of TAB-ICs (integrated circuits formed by means of an interconnect technology known as tape-automated bonding). Therefore, the reliability and yield of the manufacturing, high-resolution display, and more flexibility in the design of display system can be further

achieved [22]. LTPS TFTs can be used to manufacture complementary metal oxide semiconductor (CMOS) devices in the same way as in crystalline silicon metal oxide semiconductor field-effect transistors (MOSFETs). Fig. 2.1 shows the cross sectional structure of p-channel TFT and n-channel TFT in a LTPS process, where the n-channel TFT has the lightly doped drain (LDD).

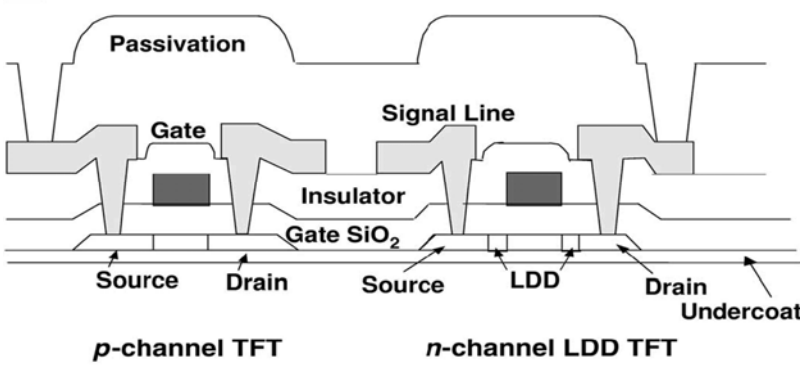


Fig. 2.1. The schematic cross-section view of device structures of a p-channel TFT and n-channel TFT in a LTPS process. The n-channel TFT has lightly doped drain (LDD).

The periphery circuit blocks of LCD panel are roughly composed of four parts — display panel, timing control circuit, scan driver circuit, and data driver circuit [6]. Display panel is constructed of the active matrix liquid crystals and the operation of the active matrixes is similar to DRAM (dynamic random access memory). Timing control circuit is responsible for transmitting RGB (red, green, and blue) signals to the data driver and controlling the behavior of scan driver. As soon as one voltage level of the scan lines rises, the RGB signals are transmitted through the data driver. After a period, the voltage level of this scan line is disabled and next scan line is turned on. All voltage levels of those scan lines are raised in turn [3].

SOP application will be implemented step by step in the future to reduce the fabrication cost. Such integration technology contributes to shorten the product lead time because the assemblage of CMOS ICs can be eliminated. Actually, this integration level has been proceeding from simple digital circuits to the sophisticated ones. Moreover, LTPS technology is compatible with OLED, which is another promising display device. Therefore, design of driving circuits for TFT-LCD in LTPS technology is worthy expecting in the future. In [35] and [38], the TFT devices had been reported to have large variation in the threshold voltage and the device characteristic, so the device characteristic variation is a very important issue

for analog circuit design in LTPS technology [42]. In this paper, a 6-bit R-string digital-to-analog converter (DAC) with gamma correction on glass substrate for TFT panel application is proposed. The proposed DAC with gamma correction design can reduce the area and complexity of the DAC on glass substrate, which is beneficial for data driver to be integrated in the peripheral area of TFT-LCD panels in LTPS process.

2.2 Gamma Correction and Digital-to-Analog Converters

2.2.1 Gamma Correction

Gamma correction of liquid crystal displays is involved due to the nonlinearity between luminance and human visual system (HVS). The pupils of the human's eyes would vary automatically for the change of the ambient light. For this reason, a data driver with gamma correction is necessary in TFT-LCD panel. The data driver circuit is required to compensate for the human visual system's transfer function. Fig. 2.2 shows the operation of the gamma correction for the normally white twisted nematic (NW-TN) type LCD panel [6]. The gamma correction system is composed of three relationships: (1) luminance vs. HVS brightness, (2) input digital code vs. pixel voltage, and (3) the Voltage-Transmission (V-T) curve of the NW-TN type liquid crystal. In general, the input digital codes (media codes) are designed to be direct proportion to brightness in human eye. In data driver circuit, DAC is used to convert the digital RGB signals to analog gray levels, so Gamma Correction System in Fig. 2.2 can be implemented by DAC with specified gamma correction transformation.

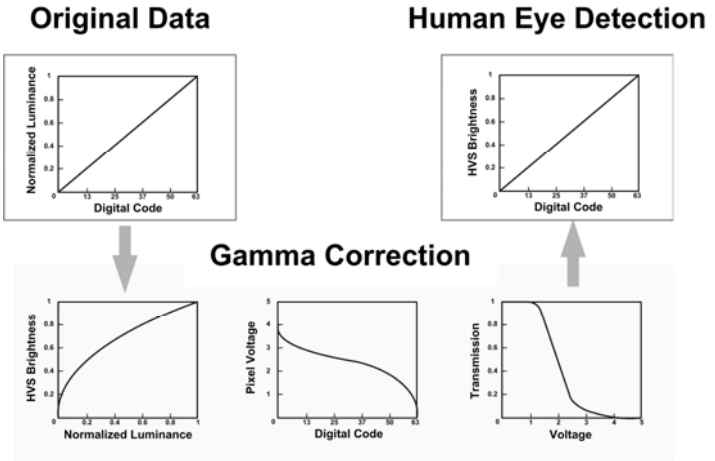


Fig. 2.2. The operation of the gamma correction for the normally white TN type LCD panel [3].

2.2.2 Digital-to-Analog Converters

Fig. 2.3 shows a 6-bit R-string DAC circuit with switch array decoding [43]. The architecture of this DAC requires no digital decoders and is usually used in LCD data drivers, because this architecture is simple for gamma correction design. However, the area of such traditional switch array becomes larger and larger, if the resolution of DAC becomes higher. The load at the output node (Vout) also becomes larger due to the huge switch array in this traditional design.

Fig. 2.4 shows a 6-bit R-string DAC with binary-tree decoding [44]. In opposition to the R-string DAC with switch array decoding, this circuit has less transistors in the decoding circuits. Nevertheless, the speed of this circuit is limited by the delay through the switch network. The timing skew among the switch-controlling signals often results in large glitches at Vout. This circuit also has larger RC-type load at the output node (Vout) due to the binary-tree switches.

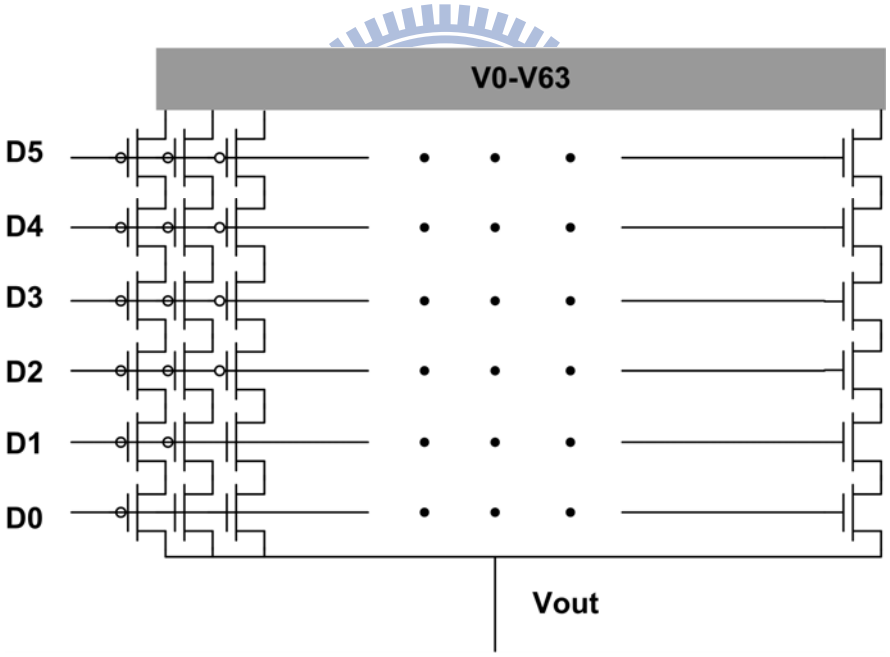


Fig. 2.3. A 6-bit R-string DAC with switch array decoding [43].

For higher-speed applications, Fig. 2.5 shows a 6-bit R-string DAC with digital decoder [45]. The switch network is connected to the digital decoder which is controlled by digital input code (Din). The load of the output node can be reduced by the digital decoder, because the output node is only connected to one column of analog switches. The operating speed of this DAC using digital decoder is faster than that with binary-tree decoding in Fig. 2.4. This

architecture is also more suitable for gamma correction design because it is easy to produce different sections in the resistor string. However, the area and complexity of the decoder circuits become larger and larger, if the resolution becomes higher. For this reason, this R-string DAC with digital decoder is not good enough for integrating the data driver in the higher resolution TFT-LCD panels.

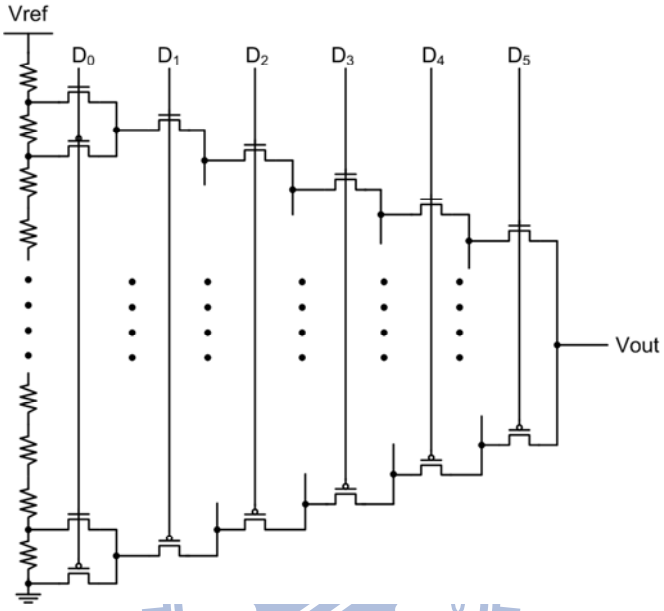


Fig. 2.4. A 6-bit R-string DAC with binary-tree decoding [44].

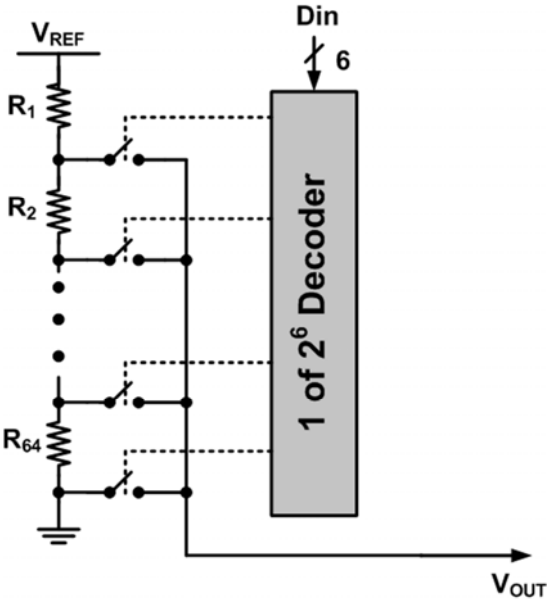


Fig. 2.5. A 6-bit R-string DAC with digital decoder [45].

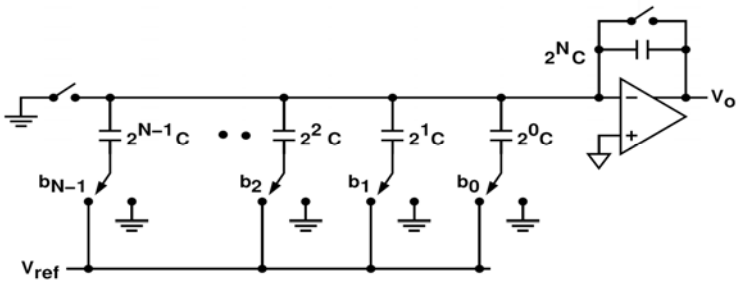


Fig. 2.6. The n-bit charge-redistribution DAC [44].

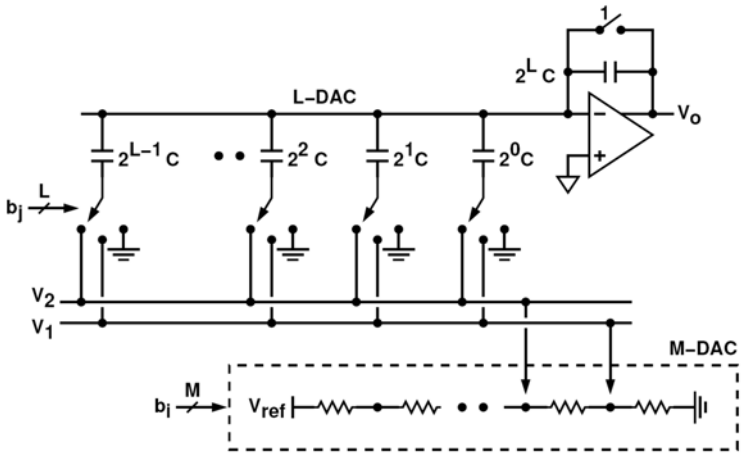


Fig. 2.7. The resistor-capacitor hybrid DAC [49].

As shown in Fig. 2.6, it is a charge-redistribution DAC [41]. The basic idea is to replace the input capacitor of a switched-capacitor (SC) gain amplifier by programmable capacitor array of binary-weighted capacitors. This circuit structure has some advantages compared with the resistor-string DAC in Fig. 2.3-2.5. First, the process matching for capacitor is better than that of resistor string. Second, charge-redistribution DAC consumes less power because it has no DC path in this circuit. However, this method is very difficult to achieve gamma correction for TFT LCD application. In other word, it cannot compensate the inherent characteristic of liquid crystal.

By utilizing multiple R-string technique, DAC circuits with advantages of higher-resolution and smaller area had been proposed [46]-[48]. However, by utilizing multiple R-string technique, it is very difficult to implement the totally nonlinear relationship between each gray level required for the gamma correction compensation. The first R-string divides the voltage levels nonlinearly and the second R-string divides two adjacent nodes of

the first R-string again linearly. Therefore, the output voltage cannot totally meet the correct voltage level in each gray level of gamma correction.

The benefits and drawbacks of resistor-string DAC and charge-redistribution DAC have been briefly discussed. A resistor-capacitor hybrid [49], which had been proposed with benefits and without the drawbacks in the aforementioned DAC, is shown in Fig. 2.7. In this circuit, the upper bits are adopted in resistor-string architecture and the lower bits are employed the charge-redistribution structure. This hybrid structure can achieve higher performance in operating speed, die area, and power consumption. However, it is difficult to realize such hybrid structure in LTPS process due to design consideration aforementioned in chapter 1.4. In [50]-[52], the performance of DAC circuits for LCD column driver, high-speed current-steering, and phase-calibrated applications are better than that of some traditional architectures of aforementioned DAC. The reason is the devices suffer worse electrical characteristic and larger variation in LTPS technology compared with that in CMOS technology. Therefore, the complexity and the implementable ability are firstly considered in the design of DAC circuit in LTPS technology.

2.3 On-Panel R-String Digital-to-Analog Converter with Gamma Correction

2.3.1 Design of Gamma Correction

The display transfer function is shown in Fig. 2.8. From previous section, there is a nonlinearity relationship between luminance (Luminance Domain) and human visual system (Brightness Domain). For this reason, the gamma correction design is necessary in TFT-LCD panel. The nonlinearity between gray level (GL) domain and luminance domain can be corrected by gamma correction design with the formula shown in Fig. 2.8. For a 6-bit gamma correction design, the transform function about this system can be expressed

$$\frac{T(GL)-T_{\min}}{T_{\max}-T_{\min}}=(GL/63)^{\gamma}, \tag{2.1}$$

$$T(GL)=(T_{\max}-T_{\min})(GL/63)^{\gamma}+T_{\min}, \tag{2.2}$$

$$L(GL)=T(GL)\cdot K_{backlight}, \text{ and} \tag{2.3}$$

$$L(GL)=(L_{\max}-L_{\min})(GL/63)^{\gamma}+L_{\min}, \tag{2.4}$$

where T is the transmission, GL is gray level, γ is gamma value, and L is luminance. From above formula, the transform function between transmission and gray level is shown in equation (2). Fig. 2.9 shows the percentage transmission vs. voltage (rms) of the liquid crystal and the liquid crystal is a normally white TN-type liquid crystal. The pixel voltage corresponding to each gray level can be obtained from the pixel voltage with gamma value of 2.2, the transform function in equation (2), and the V-T curve of this liquid crystal.

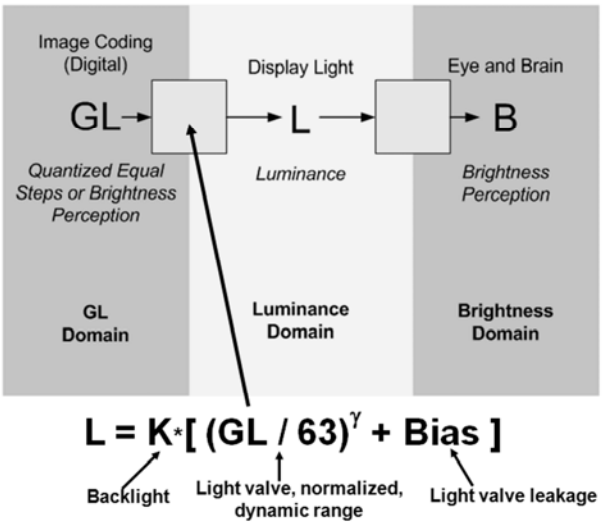


Fig. 2.8. The transform function of display system.

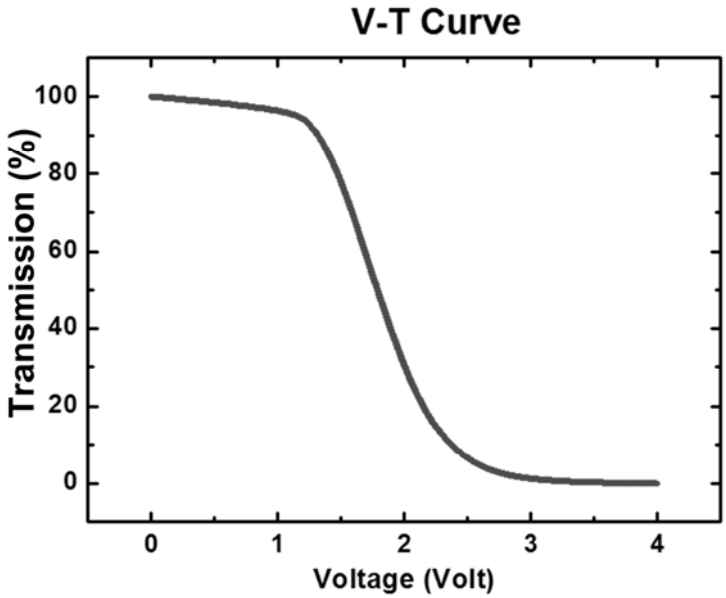


Fig. 2.9. The percentage transmission vs. voltage (rms) of the liquid crystal.

2.3.2 Design Consideration and Circuit Operation

From above discussions, resistor-string DAC, charge-redistribution DAC, and resistor-capacitor have been briefly discussed. With design consideration aforementioned in chapter 1.4, resistor-string DAC is easier to implement totally nonlinear relation between each gray level to meet gamma correlation requirement for display panel applications, and the capacitance variation is larger than resistance variation in LTPS process. Therefore, resistor-string DAC is suitable for realization of on-panel DAC with gamma correction.

The R-string DAC with digital decoder in Fig. 2.5 is an appropriate technique for reducing the loading of the output node. It also has a simple structure for layout floorplan and suitable for gamma correction design. But this architecture has too large area of the decoder in high resolution DAC. For this reason, a new architecture to reduce the area of the decoder is proposed in Fig. 2.10. The transistor number of the decoder is not linearly increased but exponentially increased with the growing of the bit number. Fig. 2.10 shows the proposed 6-bit R-string digital-to-analog converter (DAC) with gamma correction on-glass substrate for TFT panel application. The smaller area and lower complexity can be achieved in this new design. The new proposed R-string DAC in Fig. 2.10 is composed of folded R-string circuit, switch array, two identical segmented decoders, and the reordering decoding circuit [53]. The input signal Din is segmented into two parts (MSBs and LSBs) and assigned to two identical segmented decoders. The MSBs determine the only single row to be selected through one segmented decoder while all others remain unselected. This operation connects eight adjacent resistor nodes in the selected row to reordering decoding circuit. At the meanwhile, the LSBs determine one of eight resistor nodes in the selected row to be connected to the output node (Vo) through the reordering decoding circuit and the other segmented decoder. Therefore, the output voltage matches the correct gray level. In addition, the reordering decoding circuit is an important part in the proposed DAC to solve the function error using two identical segmented decoders. Without reordering decoding circuit in the proposed circuit, when the LSBs of input signal Din are required to select the highest voltage level in each row, the lowest voltage level will be chosen in even rows on the contrary and the highest voltage level will be chosen in odd rows due to the folded R-string circuit. With the reordering decoding circuit, the proper voltage level can be correctly chosen to meet each gray level of gamma correction.

With the R-string approach, the DAC has guaranteed monotonicity and also has higher accuracy, because the accuracy of the R-string DAC is dependent on the ratio of resistors, not

dependent on absolute resistor values [54]. Furthermore, the area of the proposed folded R-string DAC with gamma correction can be reduced because the reordering decoding circuit can simplify the decoder circuit. Otherwise, the decoder connected to LSBs has to be redesigned so the right voltage level can be chosen in even rows. Besides, the partial decoding function is replaced by the signal paths routing of the reordering decoding circuit. The fundamental decoders can be utilized for the two identical segmented digital decoders.

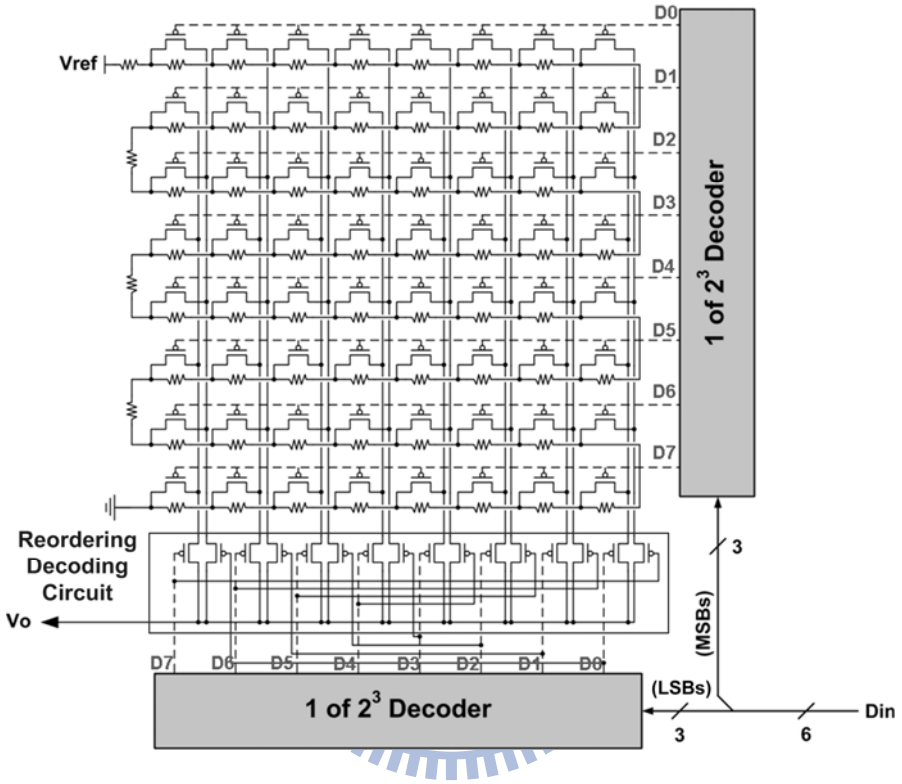


Fig. 2.10. The proposed 6-bit R-string digital-to-analog converter (DAC) with gamma correction on glass substrate for TFT panel application.

2.3.3 Simulated Results and Comparison

The 1 of 2^6 Decoder in the traditional design of Fig. 2.6 needs 64 6-input NAND gates and 6 inverters, while the 1 of 2^3 Decoder in the new proposed design of Fig. 2.10 only needs 8 3-input NAND gates and 3 inverters. Therefore, the total transistors of the decoders can be decreased from 780 to 124 in such a 6-bit DAC, as compared in Fig. 2.11. The transistor number of the R-string DAC can be effectively reduced to about one sixth of the traditional one by using this proposed architecture. This new proposed 6-bit folded R-string DAC with segmented digital decoders is also more suitable for applying with different gamma corrections in TFT-LCD panels.

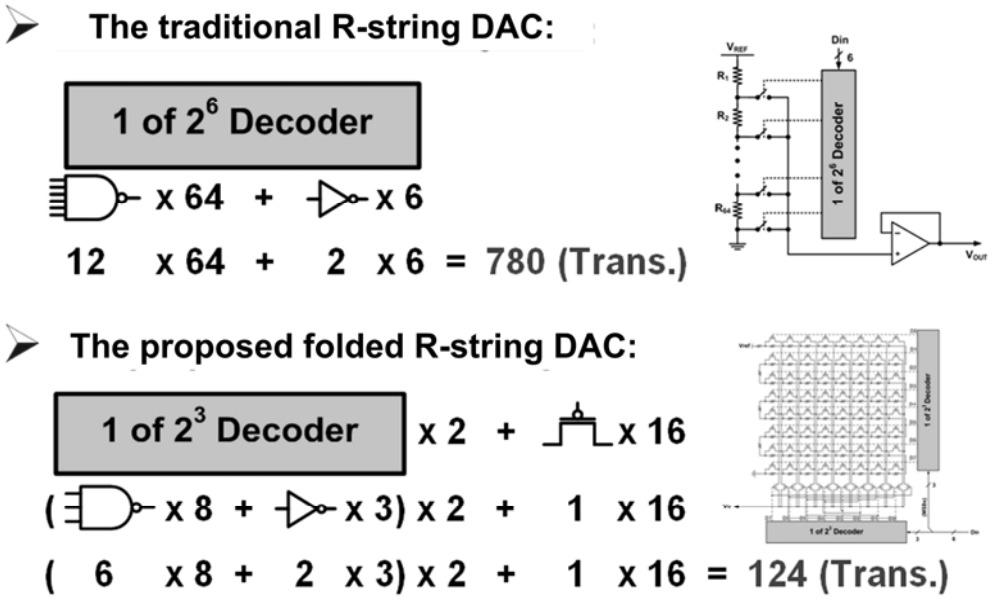


Fig. 2.11. The comparison of the transistors number of the decoders between the traditional and proposed 6-bit R-string DAC.

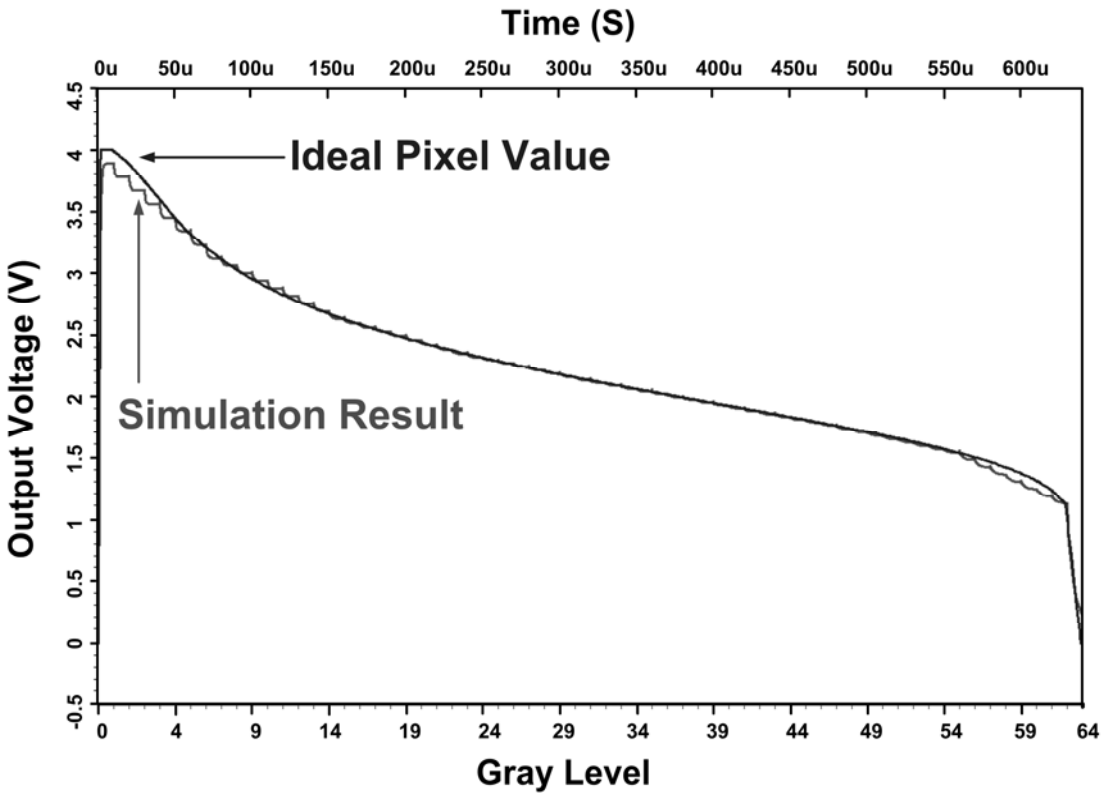


Fig. 2.12. The simulation result of 6-bit R-string digital-to-analog converter (DAC) with gamma correction in 3-μm LTPS technology at 100-kHz operation frequency.

The pixel value can be derived with gamma value of 2.2 by using the transform function with proper resistance ratio. The proposed circuit has been designed and verified by the Eldo software with the RPI model (Level=62) in a 3-μm LTPS process. The simulation result of this DAC, assigned a series of digital input codes from 000000 (GL=0) to 111111 (GL=63) at 100-kHz operation frequency, is shown in Fig. 2.12. Around the lowest and highest gray levels, some data of simulation result don't well agree to the ideal pixel value. The reason is the ideal pixel value in highest gray level is 0 while in lowest gray level is the highest voltage value (usually is VDD). In this design of R-string DAC, the R-string is divided into eight intervals to fit the ideal pixel value and each interval is divided into the same sub-interval again. Therefore, the lowest gray level is not well fitted to the ideal pixel value of VDD and this sub-interval also doesn't well agree to the ideal pixel value. The similar situation is happened in the highest gray level.

2.4 Experimental Results and Discussion

The proposed 6-bit R-string DAC with gamma-correction on glass substrate for TFT panel application has been designed and fabricated in a 3-μm LTPS process. The die photo of the fabricated DAC circuit on glass substrate is shown in Fig. 2.13, which occupies an area of 1110 μm x 1180 μm. Such area is relatively large compared with the specification for pitch area of display panel. However, the layout style in this work is to verify the feasibility of the proposed circuit. Suitable adjustment can be made according to different display panel applications. The largest resistor used in the DAC is 56.48 kΩ with the occupied layout area of 75 μm x 112 μm in a 3-μm LTPS process. Due to the gamma correction design, the resistors have different values in each gray level and the total resistor used in the DAC is 199.95 kΩ. The resistor value can be adjusted according to different liquid crystals. If the output of DAC is connected to a buffer, the resistor value can be drawn larger to reduce the power consumption from the R-string. The measured results of output voltage in the proposed R-string DAC with gamma correction in 3-μm LTPS process are shown in Fig. 2.14. With the transform function and proper resistance ratio, the measured results well agree to the simulation results with a gamma value of 2.2. The measured results are just the output of the R-string and the buffer is not added in the layout.

Although LTPS process with enlarged poly-grain size can improve the device performance, it usually accompanies a random device-to-device variation on LCD panel. The harmful effects of irregular grain boundaries, gate-insulator interface defects, and incomplete

ion-doping activation in thin poly-silicon channels often result in the variation on electrical characteristics of LTPS TFTs [36].

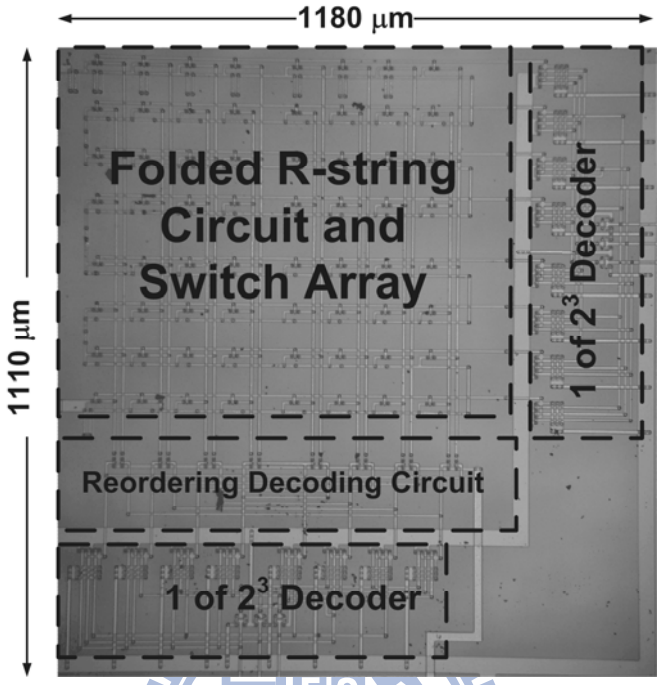


Fig. 2.13. The on-glass photo of 6-bit R-string DAC with gamma-correction realized in 3-μm LTPS process.

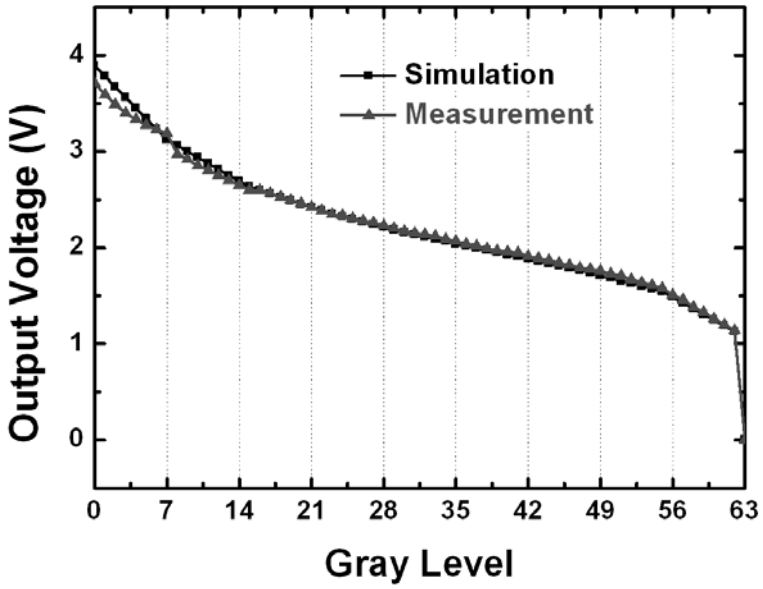


Fig. 2.14. The measured results of output voltage in the fabricated on-glass substrate R-string DAC with gamma correction in 3-μm LTPS process.

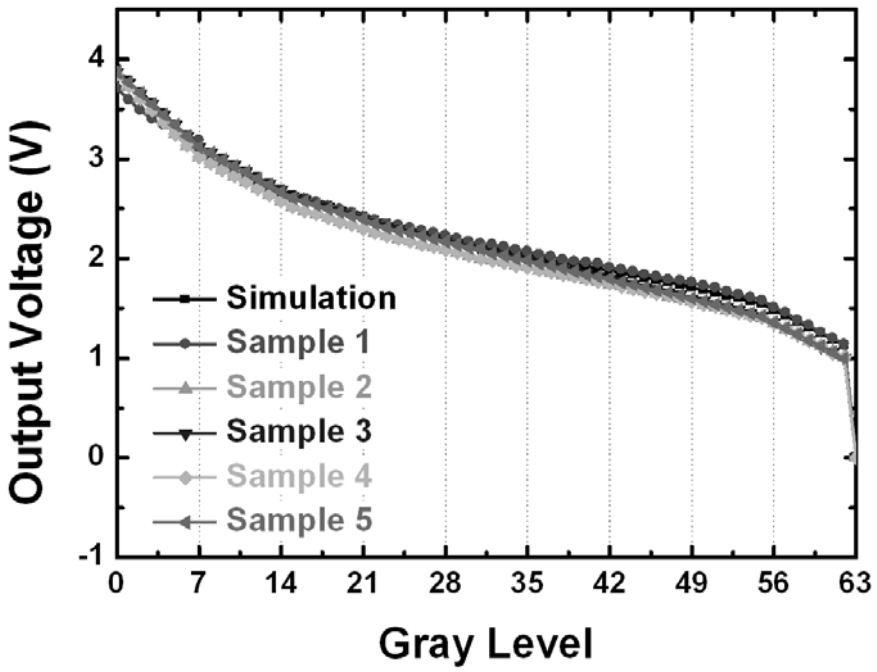


Fig. 2.15. The measured results on output voltage among five fabricated R-string DAC samples in 3-μm LTPS process.

In spite of many advantages of LTPS technology, main applications are still limited to small size displays. The reason is that the poly-Si TFTs have poor uniformity and suffer from large variations on the device characteristics due to the narrow laser process window for producing large-grained poly-Si thin film. The random grain boundaries and trap density exist in the channel region. This leads to some problems in real product applications such as non-uniformity brightness in panel, error reading in digital circuits, current gain mismatching in analog circuits, and so on [38].

Fig. 2.15 shows the measured results of the proposed R-string DAC among five different samples. INL and DNL are two important characteristics of DAC circuit. Integral nonlinearity (INL) is usually defined to be the deviation from a straight line and differential nonlinearity (DNL) is defined the variation in analog step sizes away from 1 LSB [44]. However, in this work, the proposed DAC circuit presents nonlinear relationship between each gray level due to gamma correction compensation, that is, the LSB is not a constant value. Therefore, Fig. 2.16 shows (a) the averaged output voltage, (b) maximum error, (c) standard deviation, and (d) percentage error among five fabricated R-string DAC samples in 3-μm LTPS process. The percentage error shown in Fig. 2.16 (d) is defined as

$$\frac{Ideal\_Voltage - Measured\_Voltage}{Ideal\_Voltage} \cdot 100. \tag{2.5}$$

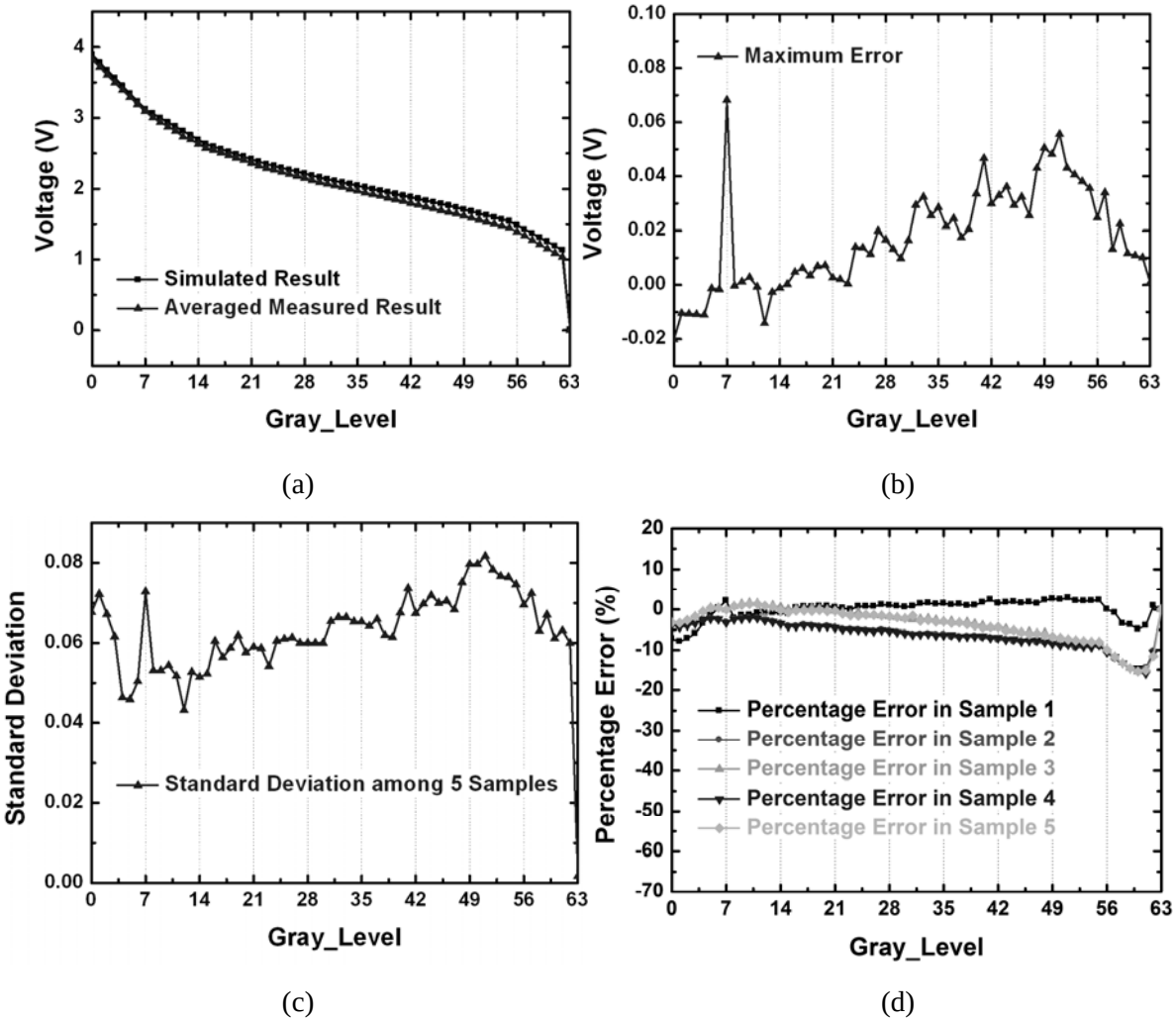


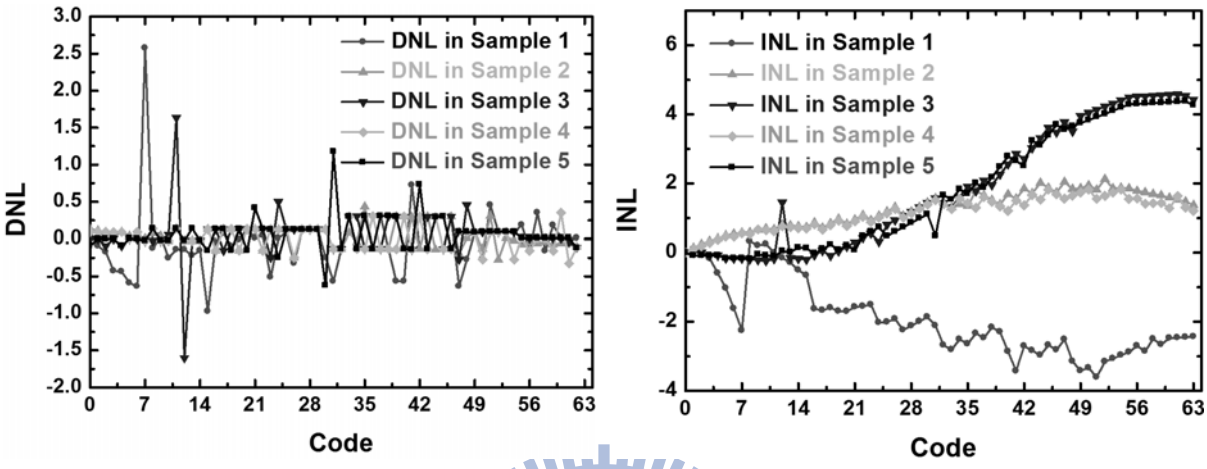
Fig. 2.16. (a) The averaged output voltage, (b) maximum error, (c) standard deviation, and (d) percentage error in five fabricated R-string DAC samples in 3-μm LTPS process.

The standard deviation has large difference at the gray_level 63. The reason is that the simulation voltage in gray_level 63 is about 0.005V, and the measured voltage in five different samples are 0.002, 0.006, 0.003, 0.005, and 0.005, respectively. The variation of each sample is due to the non-uniformly resistor doping. To eliminate the variation on each sample, the calibration circuit or layout optimization should be developed [53]. In addition, Fig. 2.17 shows DNL and INL for the proposed DAC circuit which presents nonlinear relationship between each gray level due to gamma correction compensation. Since the LSB is not a constant value in the proposed circuit, DNL and INL are derived by:

$$DNL_i = \left(\frac{(Measured\_V_{i+1} - Measured\_V_i) - (Simulated\_V_{i+1} - Simulated\_V_i)}{(Simulated\_V_{i+1} - Simulated\_V_i)} \right), \quad (2.6)$$

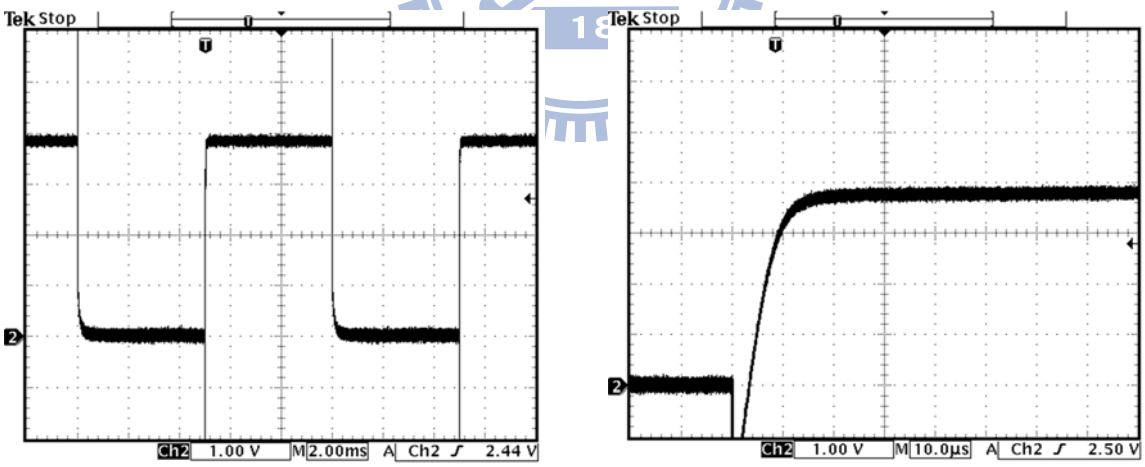
$$INL_i = \sum_i DNL_i \cdot \quad (2.7)$$

The INL shows largest variation on the highest code due to the aforementioned reason.



(a) (b)

Fig. 2.17. (a) DNL and (b) INL in five fabricated R-string DAC samples in 3-μm LTPS process.



(a) (b)

Fig. 2.18. (a) Measured output waveform when digital codes vary from 000000 to 111111 at 100Hz and (b) measured output waveform for settling time evaluation.

Fig. 2.18 (a) shows the measured output waveform when digital codes vary from 000000 to 111111 at 100 Hz, and Fig. 2.18 (b) shows the measured output waveform for settling time

evaluation. The overshooting (undershooting) phenomenon comes from the higher (lower) supply (ground) voltage, which is utilized to fully turn-on (turn-off) the switches in switch array, applied in the decoders. In Fig. 2.18 (b), the settling time is within 20 μs when the output node (Vo) is directly connected to the oscilloscope; therefore, the output loading is about 10 pF due to voltage probe. The performance comparison among this work and some prior arts are summarized in Table 2.1.

TABLE 2.1

PERFORMANCES COMPARISON AMONG THIS WORK AND SOME PRIOR ARTS

	This work	[48]	[50]
Technology	3-μm LTPS	2-μm LTPS	0.35-μm CMOS
Power Supply	4 V	N/A	5 V
Number of Bits	6	8	10
Maximum DNL	Fig. 2.16 and 2.17	< 1 LSB	3.83 LSB
Maximum INL	Fig. 2.16 and 2.17	N/A	3.84 LSB
Settling Time	< 20 μs	N/A	3μs
Power Consumption	82 μW	N/A	3 μA/buffer
Area	1110 μm x 1180 μm	3 mm x 30.24 mm for DAC and digital logic	0.2 mm x 1.26 mm for 4 channels

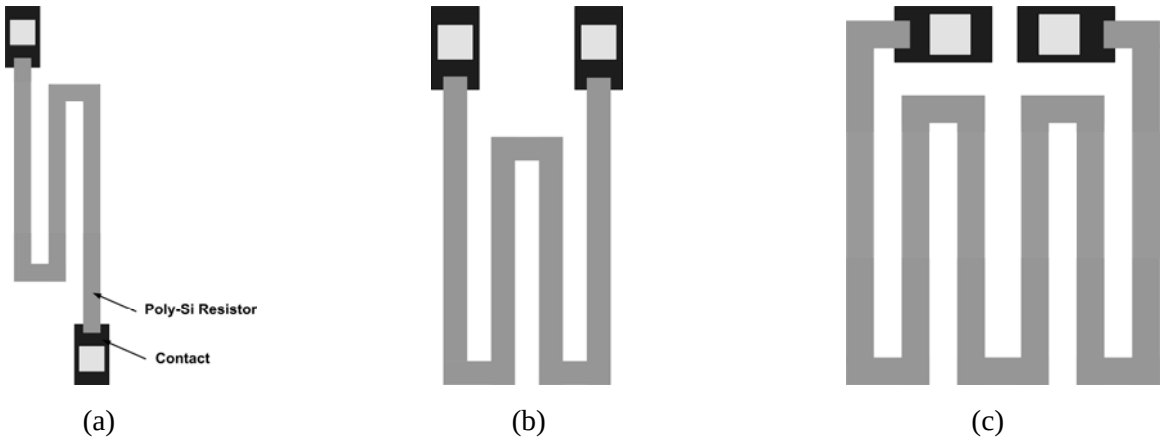


Fig. 2.19. Three different layouts to realize resistor on glass substrate [55].

Fig. 2.19 shows three different layouts in resistor [55]. The two contacts of a serpentine resistor should reside as close to one another as possible to minimize the impact of thermoelectrics. Fig. 2.19 (a) has unnecessarily large thermal variations due to an excessive separation between its contacts. In Fig. 2.19 (b), the layout reduces thermal variability and improves matching by bringing the resistor heads into closer proximity. However, this layout is vulnerable to misalignment errors. Fig. 2.19 (c) eliminates the misalignment vulnerability. Besides, the trimming technique [56] used in bandgap reference circuit can be further adopted to get precise output voltage for this DAC on glass substrate.

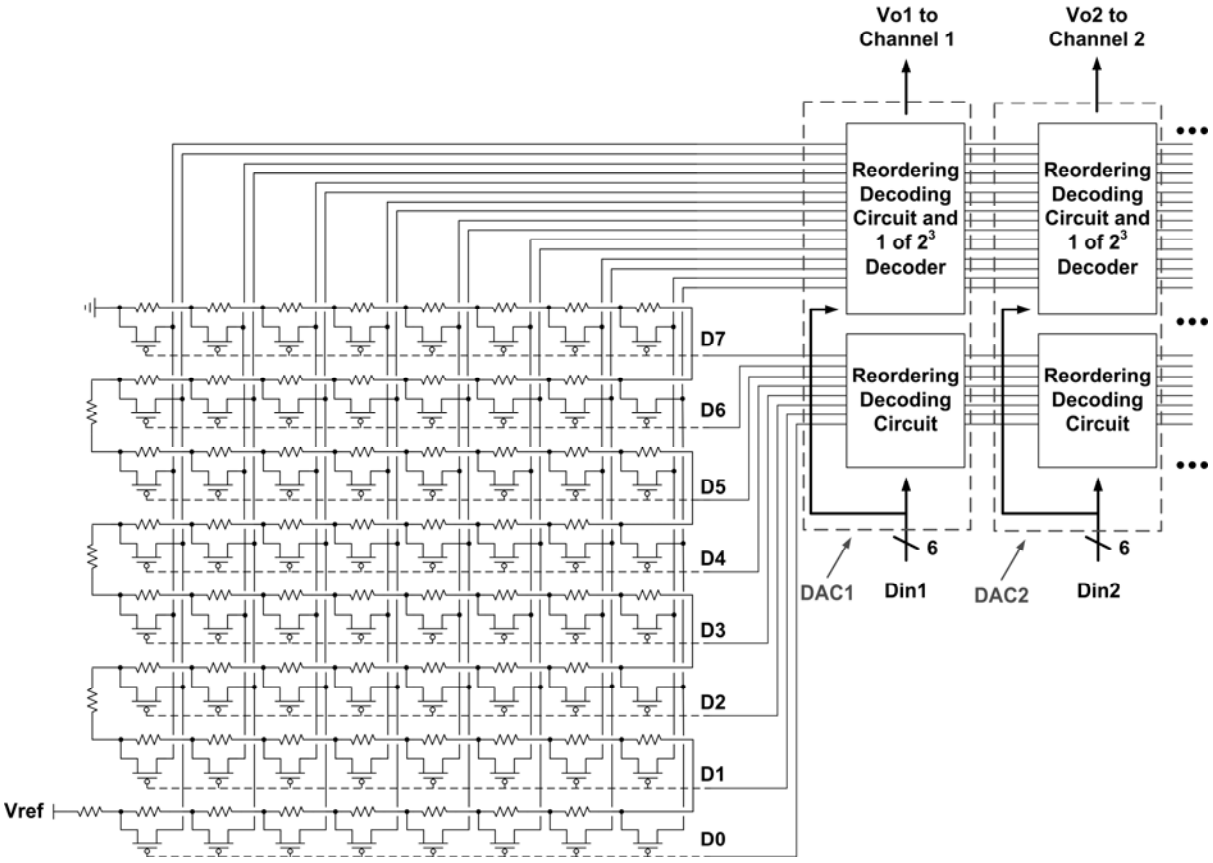


Fig. 2.20. Suggested layout arrangement of the proposed circuit with shared R-string for multiple channels in LTPS TFT panels.

Finally, the R-string is often shared by several output channels for TFT panel applications, so the routing will be complex. Therefore, the occupied layout area and location should be optimized in the commercial TFT panels. In this work, the optimization on the layout area and location of DAC is not well provided because the main purpose of this work is to verify the function and performance of DAC implemented in LTPS process. For

commercial TFT panel applications, one suggested layout arrangement is shown in Fig. 2.20. In Fig. 2.20, the R-String is shared by several DACs, and each DAC is composed of only two decoders and one reordering circuit. In addition, the output of each DAC (Vo) will be connected to each channel correspondingly. The control signals for each DAC are in parallel to each other, so the DAC can be simply duplicated for several channels with the shared R-string.

2.5 Summary

Compared with DAC circuits implemented in CMOS process for LCD column driver, the proposed circuit shows worse performance than that of some traditional architectures of aforementioned DAC. The reason is the devices suffer worse electrical characteristic and larger variation in LTPS technology compared with that in CMOS technology. With consideration of the complexity and the implementable ability, a 6-bit folded R-string DAC with gamma correction on glass substrate has been successfully designed and verified in 3-μm LTPS technology. By using the folded R-string circuit, segmented digital decoders, and reordering decoding circuit, the transistor number of the new proposed DAC circuit can be effectively reduced to about one sixth of the traditional one. Furthermore, the proposed architecture is suitable for gamma correction design in different LTPS processes by modifying the corresponding R-string value and the decoder. With more analog and digital circuits realized on the glass substrate in LTPS technology, the goal of system-on-panel (SOP) applications can be achieved in the near future.

The content of this chapter was co-work with Mr. Yu-Hsuan Li when he studied his B.S. degree in National Chiao-Tung university [57], and was also published in [40], [41], [53] with co-author of Mr. Yu-Hsuan Li.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Chapter 3

Analog Output Buffers with Level Shifting Function on Glass Substrate for Panel Applications

Two analog output buffers with level shifting function containing the digital-to-analog converter (DAC) circuit with gamma correction have been designed and verified in a 3-μm low temperature poly-silicon (LTPS) technology, which are suitable for integrated on glass substrate for panel application,. The new proposed circuits utilize the DAC with gamma correction of 3-V liquid crystal (LC) specification, but it can also drive the 5-V liquid crystal to meet the desired 5-V gamma curve without re-designing the DAC with 5-V gamma correction parameters [58]-[59].

3.1 Introduction

LTPS technology with higher mobility characteristic, which has been widely applied in active matrix liquid crystal display (AMLCD), is conceived as one of most desirable technology to accomplish system-on-panel (SOP) integration for portable systems, such as digital camera, mobile phone, personal digital assistants (PDAs), notebook, and so on. The periphery circuit blocks of LCD panel are roughly composed of four parts: display panel, timing control circuit, scan driver circuit, and data driver circuit. Display panel is constructed of the active matrix liquid crystals and the operation of the active matrixes is similar to DRAM (dynamic random access memory) which is used to charge and discharge the capacitor of the pixel. Timing control circuit is responsible for transmitting RGB (red, green, and blue) signals to the data driver and controlling the behavior of scan driver. Data driver circuit, shown in Fig. 3.1, is composed of shifter register (S/R), data latch, level shifter (L/S), DAC, and analog output buffer. Shifter register and data latch are used to transit and store the RGB signals while level shifter translates the RGB signal to a higher voltage level due to the higher operating voltage of active matrixes. In addition, DAC is used to convert the digital RGB signal to analog gray level with consideration of gamma correction. The LCD panel

with larger panel size or higher resolution display results in larger load to this signal, so the analog output buffer is essential to provide the driving capability of the data driver [6].

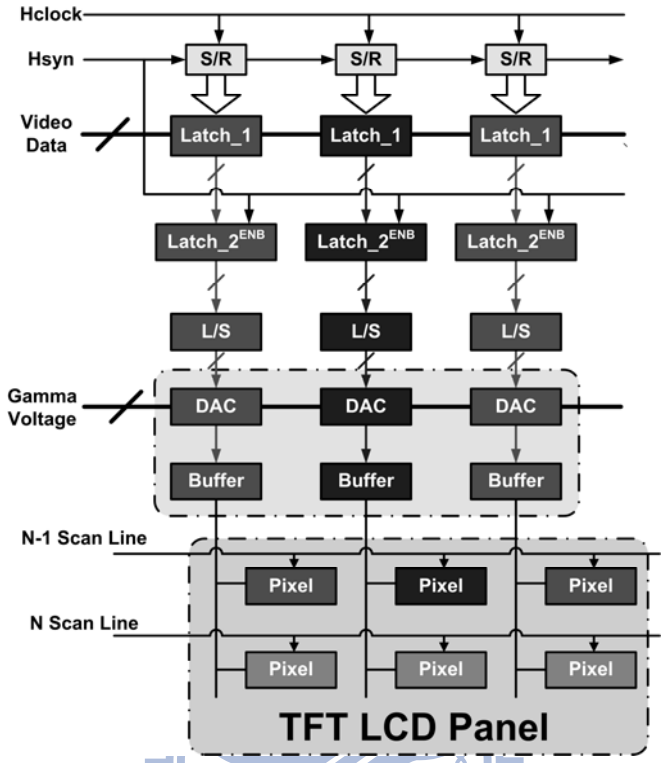


Fig. 3.1. The basic diagram of data driver circuit for TFT LCD panel [6].

SOP application has the potential to realize compact, highly reliable, and high resolution display by integrating functional circuits within a display. For a-Si TFT-LCDs, TAB-ICs are connected to the left and bottom sides of a panel as the Y driver and the X driver, respectively. Integration of the Y and X drivers with LTPS TFTs on panel requires PCB (printed circuit board) connection on the bottom of the panel only. The most common failure mechanism of TFT-LCDs, disconnection of the TAB-ICs, is therefore decreased significantly with the save in omitting the usage of ICs and all sub-circuits integrated on panel. Besides, the cost of panel becomes lower, as well as the higher yield rate can be also achieved [23]. Furthermore, some poly-Si TFT characteristics, such as high carrier mobility, low threshold voltage, high stability, and high reliability, are required to fulfill the SOP application. Such integration technology contributes to shorten the product lead time because the assemblage of CMOS ICs can be eliminated. Currently, such integration has been proceeding from simple digital circuits to the sophisticated ones. Moreover, LTPS technology is compatible with OLED (organic light emitting diode), which is another promising display device. Therefore, design

of driving circuits for TFT-LCD in LTPS technology has been proceeding. In [48], a TFT-based 8-bit source driver for 2.0 inch QVGA AMOLED panels had been proposed to reduce source driver size about 40%. In [35] and [42], the TFT devices had been reported to have large variation in the threshold voltage and device characteristics, so the device characteristic variation is a very important issue for analog circuit design in LTPS technology. The carrier mobility depends on the grain size of the active poly-Si layer, and the deviation of the TFT characteristics is related to the quality of the poly-Si layer [60]. Some recent works had been reported to suppress the variation of poly-Si TFT characteristics to further redeem SOP application. In [38], a class-B output buffer with offset compensation had been proposed to compensate the offset of output buffer to provide high resolution display and uniform brightness display. In [61], a new gate-bias generating technique with threshold-voltage compensation had been presented to reduce the impact of threshold-voltage variation on analog circuit performance in LTPS technology.

Some kinds of circuits had been successfully integrated on TFT-LCD substrates for SOP application. In [62], a low power consumption TFT-LCD with dynamic memory embedded in each pixel has been proposed to hold a digital data corresponding to display image in the memory, so the operation of data driver can be simplified to reduce power consumption. In [63], it reported the first LCD equipped with all the circuits to display static images continuously for up to one year powered with a button battery. In [64], an 8-bit CPU containing 13,000 TFTs on a glass substrate reported to demonstrate the feasibility of the SOP.

In this work, two analog output buffers with level shifting function containing the DAC circuit with gamma correction have been designed and verified in a 3-μm low temperature poly-silicon (LTPS) technology, which are suitable for integrated on glass substrate for panel application. The new proposed circuits utilize the DAC with gamma correction of 3-V liquid crystal (LC) specification, but it can also drive the 5-V liquid crystal with the desired 5-V gamma curve without re-designing the DAC with gamma correction parameters.

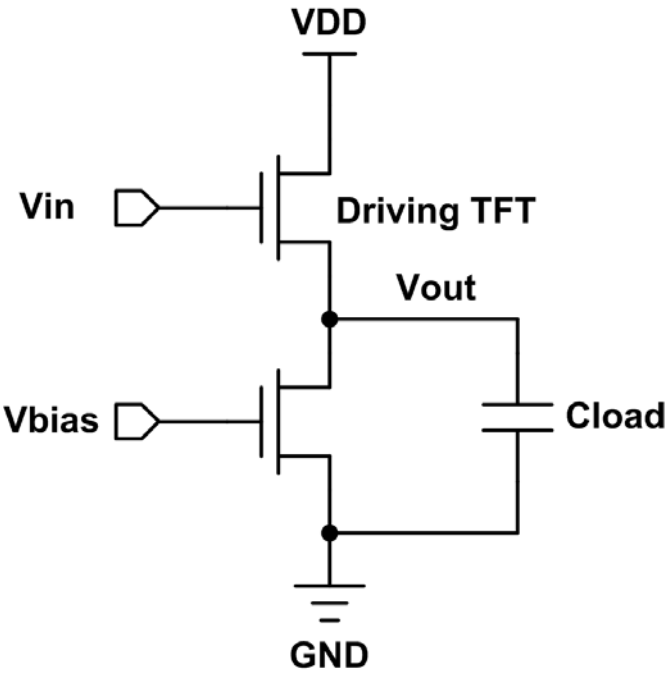
3.2 Conventional On-Panel Analog Output Buffer

3.2.1 Source Follower Type

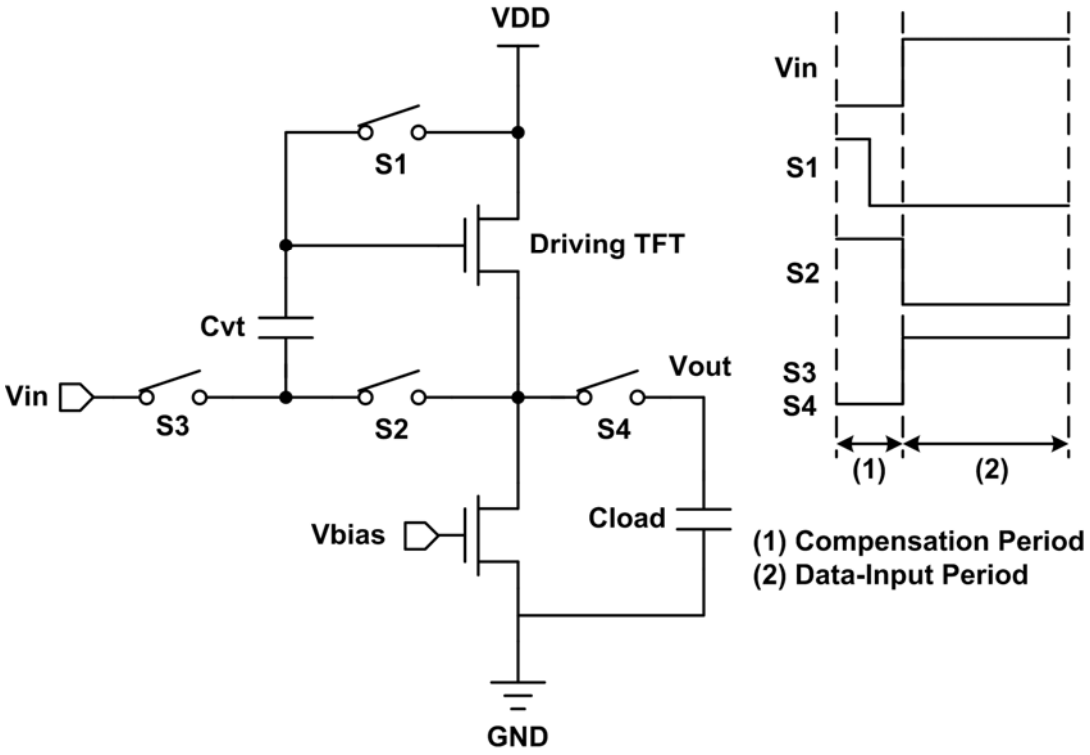
Source follower is one of the most popular analog output buffers integrated on the glass substrate for data driver duo to its high input impedance and low output impedance. For such

simple architecture, some drawbacks are found, such as smaller output swing and higher input offset voltage. Fig. 3.2(a) shows the conventional source follower of analog output buffer with active load [65]. The final output voltage (Vout) in Fig. 3.2(a) with different input voltage (Vin) is kept constant but has an offset voltage from the input level, in which the offset is determined mainly by the threshold voltage of the driving TFT. Besides, the threshold voltage may not be a constant in different panel locations due to the LTPS device variation. To balance the input offset voltage, Fig. 3.2(b) shows the modified source follower of analog output buffer with compensation capacitor. In the compensation period (1), S1 and S2 are turned on, so the voltage drop is stored in compensation capacitor (Cvt). In the data-input period (2), S1 and S2 are turned off while S3 and S4 are turned on. At the meanwhile, the gate voltage of the driving TFT is applied with the voltage difference hold in Cvt added to the input voltage Vin. Thus, the output voltage is compensated by the voltage stored in Cvt.

The offset voltage was deceased by the aforementioned compensation technique. However, the offset voltage, which is predominantly governed by the threshold voltage of TFT, may not be stored exactly in the capacitor due to the subthreshold leakage current. The subthreshold characteristic of poly-Si TFT is rather poor compared with well-known MOSFETs in the silicon CMOS technology, and the large subthreshold current of poly-Si TFTs increases the offset voltage of analog buffers [66]. In addition, compensation capacitor utilized in this technique may also consume larger area. Therefore, Fig. 3.3 shows the analog buffer of source follower type with device matching technique and its timing diagram of operation. When the reset signal (Reset) is low, the voltage in output loading capacitor (Cpanel) is reset. The input signal (Vdata) is applied when the Reset becomes high, so the voltage in node A (Va) grows to Vdata+|Vth| due to the diode connection of P1. (Vth is the threshold voltage of P-type TFT.) After that, P4 is turned on with the active signal and Va decreases due to bootstrapping effect, as well as Vss is transferred to Cpanel. As Va decreases to Vdata-|Vth|, diode-connected P2 is turned on to hold this voltage. Therefore, the source voltage of P3 is about Vdata and the threshold voltage is compensated by device matching. This analog buffer with device matching technique can reduce the offset generated from the subthreshold current of poly-Si TFT, but without using additional capacitor to store the threshold voltage of a poly-Si TFT.



(a)



(b)

Fig. 3.2. (a) Conventional source follower analog output buffer with active load, and (b) the modified source follower analog output buffer with compensation capacitor [65].

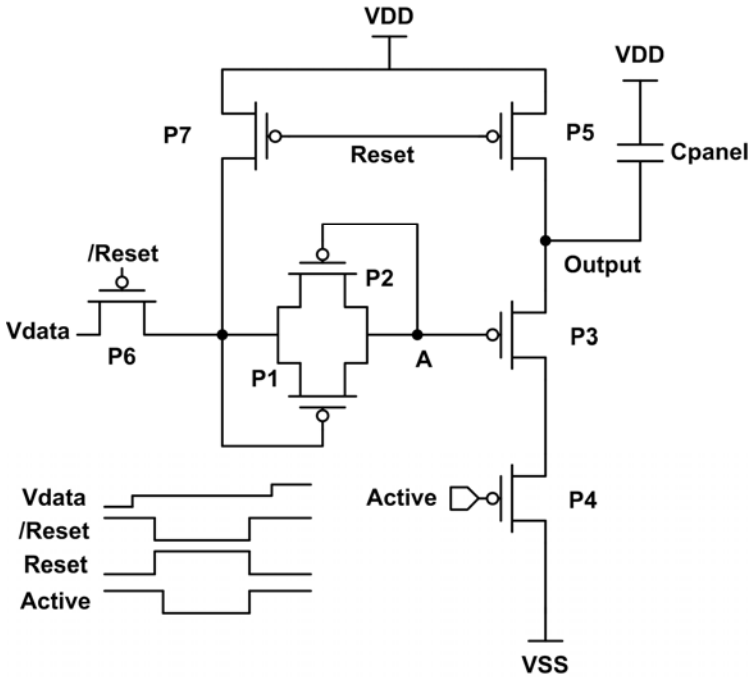


Fig. 3.3. An analog buffer of source follower with device matching technique and its timing diagram of operation [66].

3.2.2 Two-Stage OP AMP

Compared with the analog output buffer of source follower type, the unity-gain analog output buffer with an OP amp has higher on-panel analog driving capability [67]. Fig. 3.4 shows the two-stage OP amp utilized for unity-gain analog output buffer with Miller compensation and nulling resistor (M10 and Cc). As a unity-gain buffer, the output node (Vo) is connected to the negative input node (V_{i-}) and the input signal is applied to the positive input node (V_{i+}). This output buffer comprises four parts as following. The 1st part consists of p-channel differential pair (M1 and M2) with n-channel current mirror load (M3 and M4) and a p-channel tail current source (M5). The second part is a common-source amplifier stage (M6 and M7), which can improve the open-loop gain and reduce the input offset voltage. The 3rd part is a constant gm bias circuit (M11-M16 and R_B), which can provide a more stable voltage reference. The 4th part is start-up circuit (M21-M24) to turn on the bias circuit in the beginning of power-on operation and be turned off after bias circuit working. The two stage OP amp has larger unity-gain frequency, better slew rate, lower input offset voltage, better immunity to noise, and more steady circuit performance, as comparing to the analog output buffer of source follower type. Furthermore, input offset can be further reduced by the larger open loop gain of OP amp.

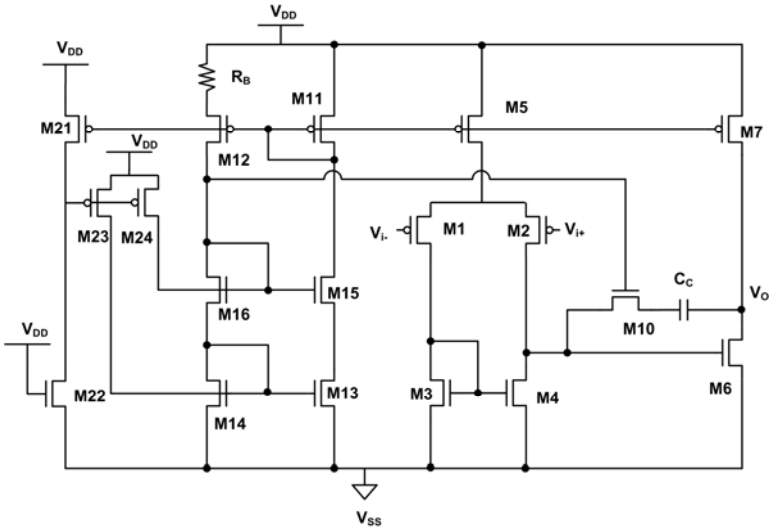


Fig. 3.4. Two-stage OP amp utilized for unity-gain analog output buffer [67].

3.2.3 Level-Change Analog Amplifier

Fig. 3.5 shows a level-change analog amplifier which maximizes monolithic circuit integration, in particular targeting the monolithic integration of high performance analog circuits [68]. This circuit consists of a differential amplifier, an offset-removing capacitor "Coc," and one set of switches allowing connections to 4 voltages. At T1 and T3 period, Coc is precharged to voltage level determined by the switch settings. At T2 and T4 period, voltage level of Vref is therefore shifted to the output decided by Vx and Vss, where Vref is corresponding to the image data for an LCD.

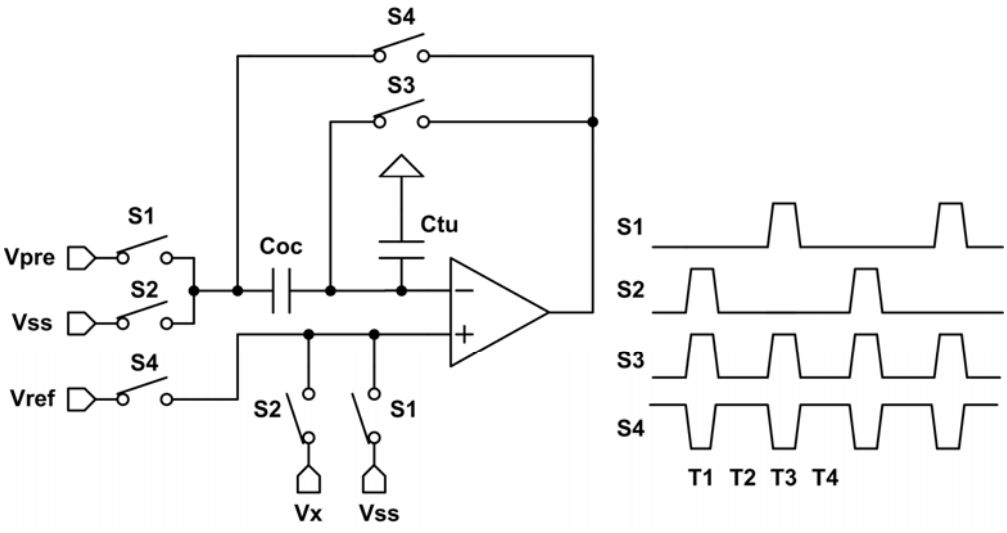


Fig. 3.5. A level-change analog amplifier [68].

3.3 On-Panel Analog Output Buffers with Level Shifting Function

3.3.1 Design Consideration

As mentioned above, DAC is used to convert the digital RGB signal to analog gray level with consideration of gamma correction. The LCD panel with larger panel size or higher resolution results in larger load to this signal, so the analog output buffer is essential to provide the driving capability of the data driver to drive the liquid crystal with appropriate analog gray level. In general, each liquid crystal under the selected operation voltage has its corresponding gamma curve. Therefore, for various liquid crystal displays, the DAC circuit is indispensable to be redesigned as well. In general, the capacitive loading for one pixel is about 300 fF. For XGA display panel application, the effective capacitive loading can be roughly determined by 1024 x 768 x 3(rgb) x 300 fF.

In this work, two new analog output buffers with level shifting function are proposed to realize the DAC with gamma correction of 3-V liquid crystal (LC) specification, and it can also drive the 5-V liquid crystal with the desired 5-V gamma curve without re-designing the DAC with 5-V gamma correction parameters. Since the two-stage OP amp has larger unity-gain frequency, better slew rate, lower input offset voltage, better immunity to noise, and more steady circuit performance, as comparing to the analog output buffer of source follower type, the OP amp integrated in the two proposed analog output buffers with level shifting function is the same as that shown in Fig. 3.4. Furthermore, input offset can be further reduced by the larger open loop gain of OP amp. With design consideration aforementioned in chapter 1.4, the proposed analog output buffer II shows better consistent to ideal gamma curve with gamma value of 2.2 than that of the proposed circuit I.

3.3.2 On-Panel Analog Output Buffer I with Level Shifting Function and Simulated Results

Fig. 3.6 shows the new proposed analog output buffer I with level shifting function on glass substrate for panel application in 3-μm LTPS technology with AVDD1 = 3V, AVDD2 = 6V, and R1 = 400kΩ. R-string (RS00-RS64) and decoder 1 with digital input code Din are 6-bit R-string DAC circuit with gamma correction implemented by the R-string for 3-V liquid crystal panel application. When Din is 000000, decoder 1 transforms the digital input

code to only turn on MS01, and V0 is assigned to Vin+ of OPAMP in Fig. 3.6. In the meantime, all the other voltages (V1-V63) are not transmitted to Vin+. Therefore, with proper digital input code, the corresponding voltage level can be correctly chosen to meet each gray level in Vin+ for DAC circuit with gamma correction for 3-V liquid crystal panel application.

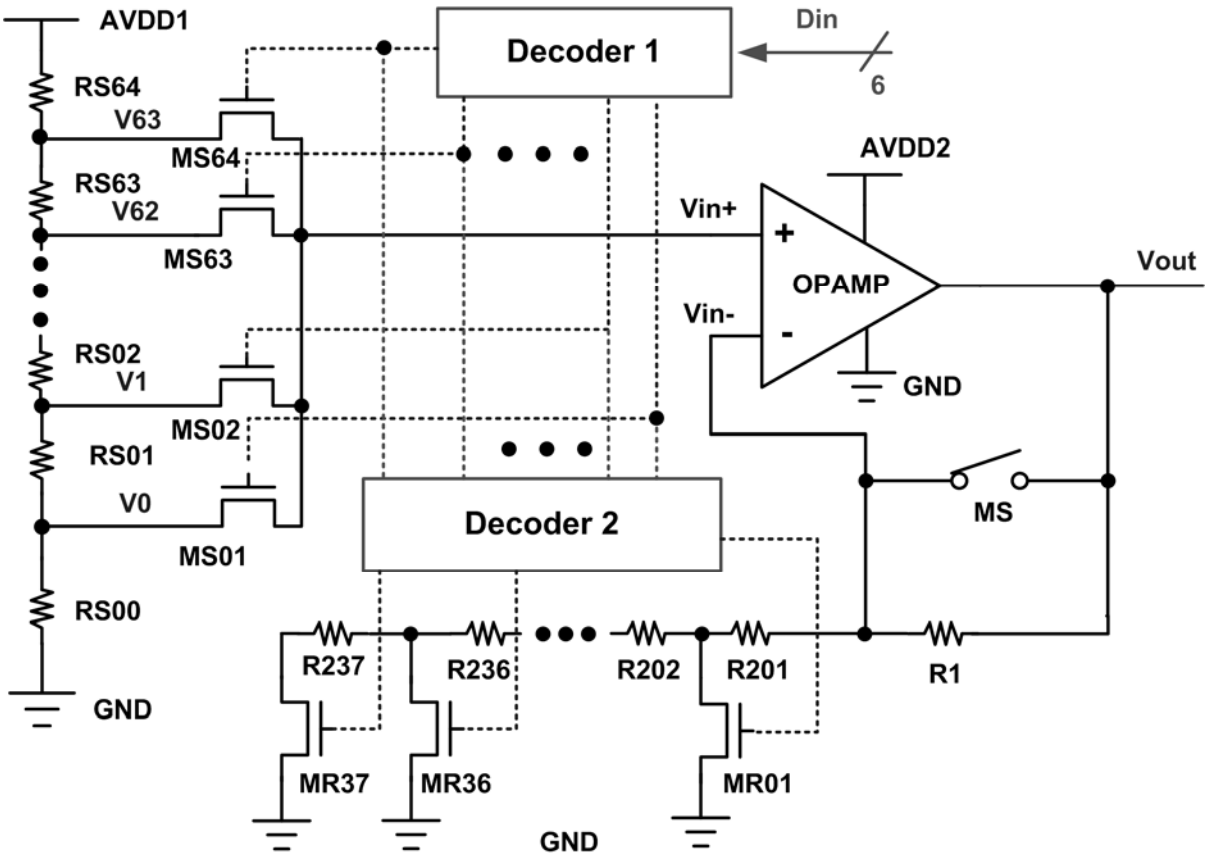


Fig. 3.6. The new proposed analog output buffer I with level shifting function on glass substrate.

Fig. 3.7 shows the resistance utilized in the proposed circuit I for (a) RS00-RS64, which are provided by the LCD panel manufacturer, and (b) R201-R237, which are designed for converting 3-V gamma correction to 5-V application. Fig. 3.8 shows two gamma curves for the liquid crystal panel under different (3-V or 5-V) operating voltages. In Fig. 3.7 (a), the larger resistance variation between RS63 and RS64 is to make V63 = 2.61V, which is close to AVDD1 = 3V. In addition, RS01-RS05 also shows large resistance variation due to large voltage degradation from gray level 5 to 1 in Fig. 3.8. In order to meet gray level 0 close to 0V, RS00 also shows larger resistance. In Fig. 3.7 (b), R201 shows the largest resistance because the largest voltage variation happened at gray level 63 from converting 3-V to 5-V gamma correction. Besides, for liquid crystal under different operating voltages, such as 5-V

display panel, the 5-V gamma curve is different to that under 3-V application. Since the applied voltages in each gray level for 5-V gamma curve cannot be simply derived from applied voltages for 3-V gamma curve by adding a constant or a linear transformation, the applied voltages for 3-V and 5-V gamma curves show nonlinear relationship in each gray level. In the new proposed circuit I, 6-bit R-string DAC with gamma correction for 3-V liquid crystal display is not needed to be re-designed for 5-V operation. OPAMP, decoder 2, R1, R201-R237, and MR01-MR37 are proposed to operate the analog output buffer with level shifting function to meet 5-V operation. Decoder 2 receives the input signal from decoder 1 to turn on only one switch of MR01-MR37 at the same time. For example, if MR01 is turned on, the OPAMP behaves like an non-inverting amplifier with it function shown below

$$Vout = Vin\left(1+\frac{R1}{R201}\right) \quad , \tag{3.1}$$

where Vin=Vin+=Vin- if the gain of OPAMP is large enough. Therefore, with suitable design of R201-R237, gamma curve for 5-V liquid crystal panel can be achieved without re-designing the 6-bit R-string DAC that has been realized with 3-V gamma correction parameters. The proposed circuit has been designed and verified by the Eldo software with the RPI model (Level=62) in a 3-μm LTPS process. Fig. 3.9 shows the simulated gamma curves of the proposed circuit in a 3-μm LTPS technology for liquid crystal panel under 3-V or 5-V operations. Vin+ is the output gamma curve of 3-V liquid crystal panel and Vout is the output gamma curve of 5-V liquid crystal panel.

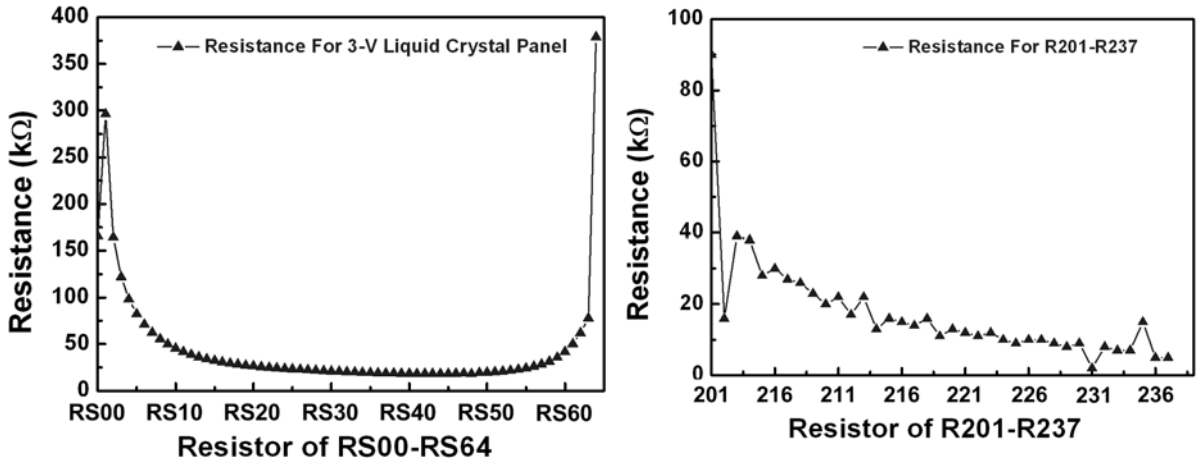


Fig. 3.7. Resistance utilized in the proposed circuit I for (a) RS00-RS64 and (b) RS201-RS237.

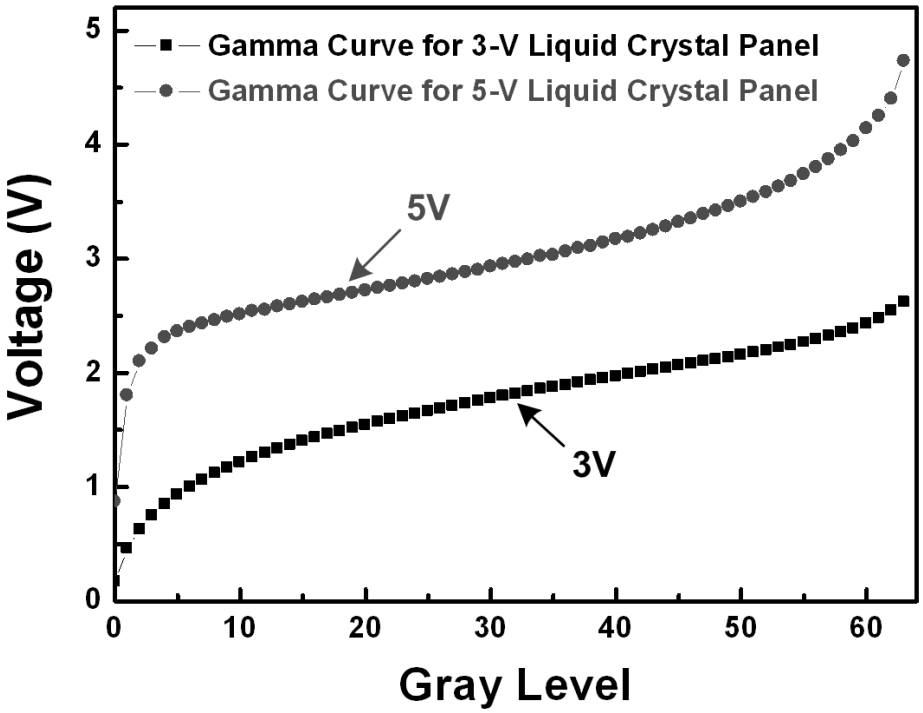


Fig. 3.8. Gamma curves for 3-V and 5-V liquid crystal panels.

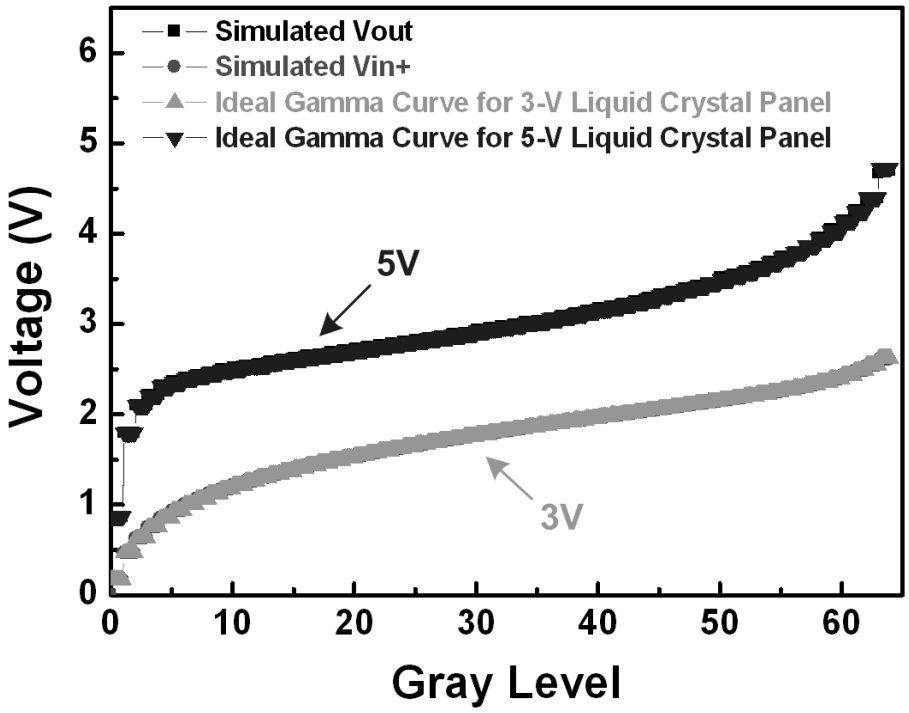


Fig. 3.9. Simulated gamma curves of the new proposed circuit I for the liquid crystal panel under 3-V or 5-V operations.

3.3.3 On-Panel Analog Output Buffer II with Level Shifting Function and Simulated Results

In the proposed circuit I, the level shifting function is strongly depended on the absolute value of resistors (R201-R237). Although LTPS process with enlarged poly-grain size can improve device performance, it usually accompanies a random device-to-device variation on LCD panel. The harmful effects of irregular grain boundaries, gate-insulator interface defects, and incomplete ion-doping activation in thin poly-silicon channels often result in the variation on electrical characteristics of LTPS devices [36]. The absolute value of resistors (R201-R237) is therefore easily not well consistent to the simulated result after fabrication. Therefore, Fig. 3.10 shows the new proposed analog output buffer II with level shifting function on glass substrate for panel application in 3-μm LTPS technology with AVDD1 = 3V, AVDD2 = 6V, AVDD3 = -3V, and R1 = R2 = 900kΩ. The main idea of proposed circuit II is similar to the proposed circuit I but the level shifting function is modified below

$$Vout = Vin\left(1+\frac{R1}{R2}\right) - Va\left(\frac{R1}{R2}\right), \tag{3.2}$$

where Va is the amendment voltage derived from RA01-RA31 and MA01-MA30.

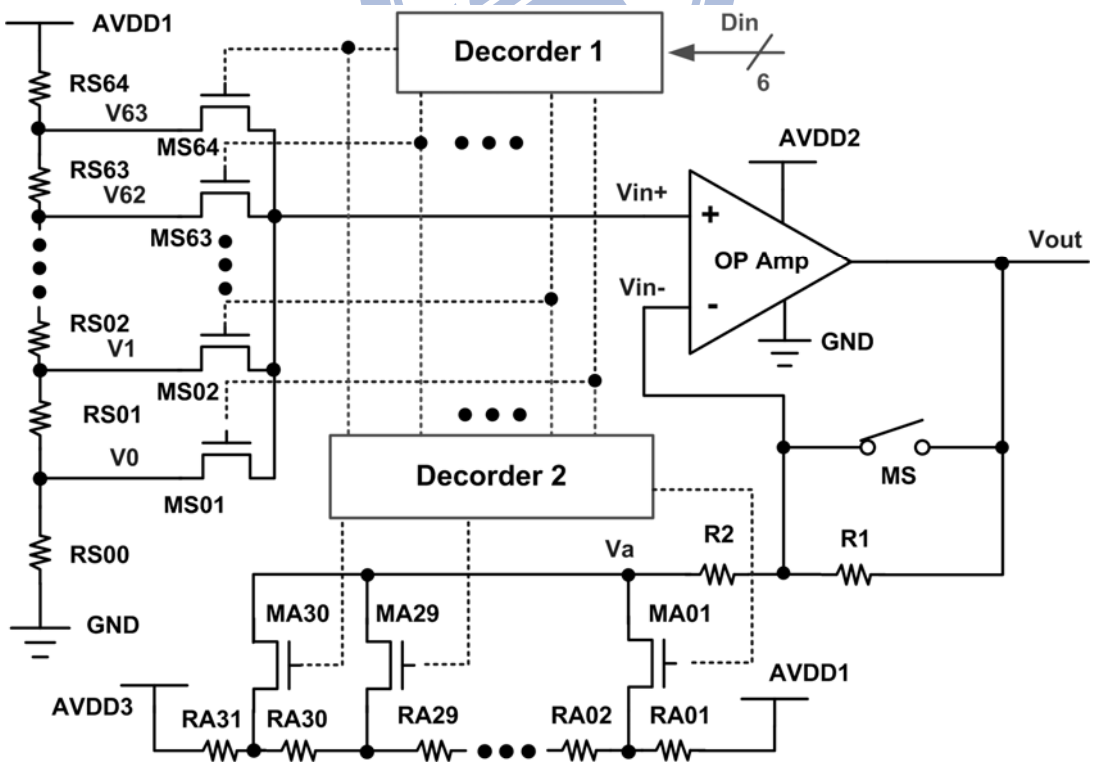
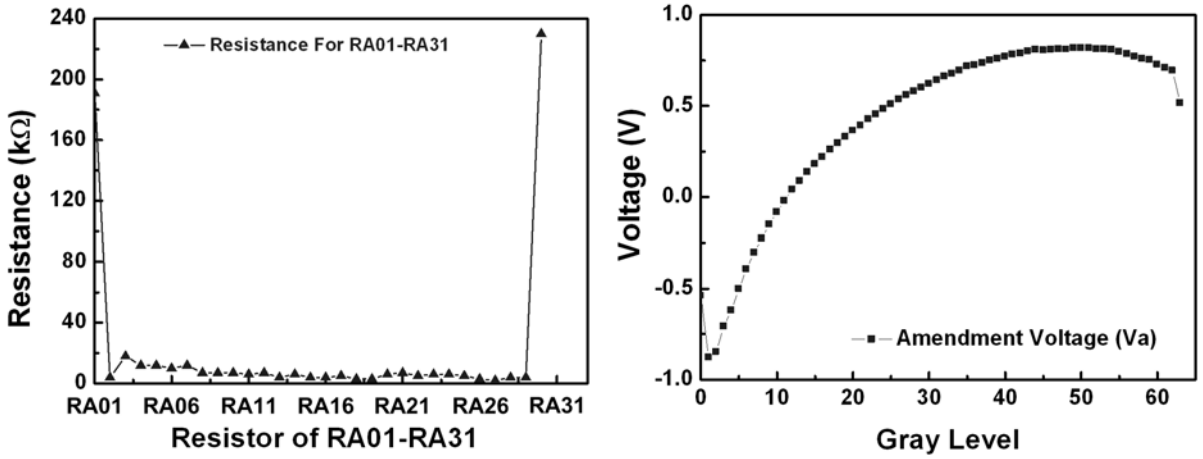


Fig. 3.10. The new proposed analog output buffer II with level shifting function on glass substrate.



(a) (b)

Fig. 3.11. (a) Resistance utilized in the proposed circuit II for RA01-RA31 and (b) the amendment voltage Va in each gray level.

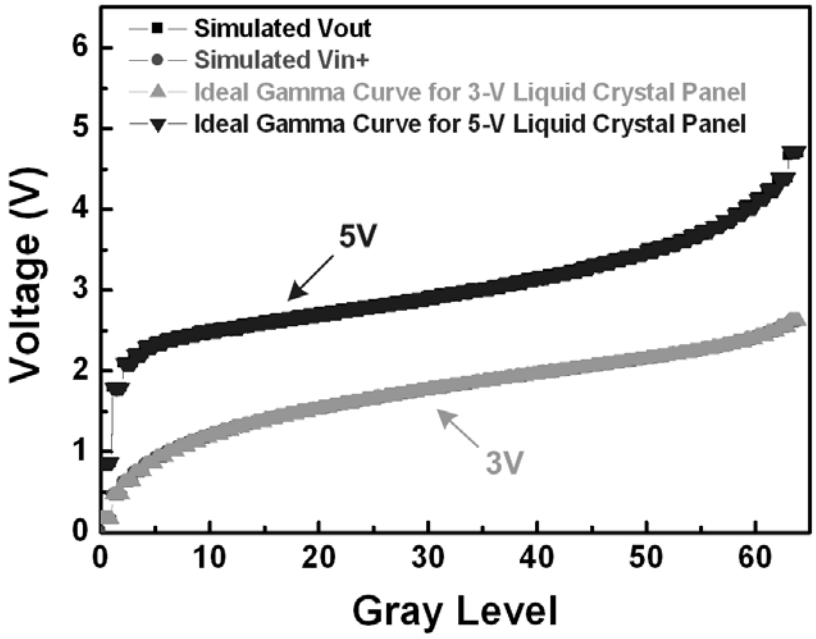


Fig. 3.12. Simulated gamma curves of the new proposed circuit II for the liquid crystal panel under 3-V or 5-V operations.

The operation of the proposed circuit II is similar to that of the proposed circuit I in the former part and RS00-RS64 are the same as that in the proposed circuit I. Nevertheless, when decoder 2 receives the input signal from decoder 1, only one switch of MA01-MA37 is turned on at the same time. Therefore, suitable amendment voltage Va is decided by the ratio of RA01-RA31. Fig. 3.11 shows (a) resistance utilized in the proposed circuit II for

RA01-RA31 and (b) the amendment voltage Va in each gray level for converting the 3-V gamma correction to 5-V application. In Fig. 3.11(a), RA01 and RA31 show the lager resistance because the amendment voltage is varied from -1V to 1V but AVDD3 is -3 V as well as AVDD1 is 3 V. In the proposed circuit II, the RA01-RA31 has guaranteed monotonicity to result in higher accuracy of amendment voltage Va, because the accuracy of Va is dependent on the ratio of resistors, not dependent on absolute resistor values. The proposed circuit has been designed and verified by the Eldo software with the RPI model (Level=62) in a 3-μm LTPS process. Fig. 3.12 shows the simulated gamma curves of the proposed circuit II in a 3-μm LTPS technology for liquid crystal panel under 3-V or 5-V operations. Vin+ is the output gamma curve of 3-V liquid crystal panel and Vout is the output gamma curve of 5-V liquid crystal panel. Finally, in Fig. 3.6 and Fig. 3.10, the switch MS is utilized to control the proposed circuits to be operated under 3-V or 5-V application. For 5-V application, the switch MS is open, so the proposed circuits can be performed just like mentioned above. For 3-V application, the switch MS is shorted, so the output of OPAMP (Vout) is connected to the negative input of OPAMP (Vin-) to perform like a non-inverting amplifier. Therefore, the proper 3-V gamma value (V0-V63) can be transformed to output (Vout) correctly.

3.4 Experimental Results and Discussion

The new proposed circuits have been designed and fabricated in a 3-μm LTPS technology. Fig. 3.13 shows the die photo of the fabricated analog output buffer I and analog output buffer II with level shifting function on glass substrate, where the area is 3200μm x 7600μm. Fig. 3.14 shows the measured results in Vout and its variation for the proposed circuit I with gamma curve for 5-V liquid crystal panel but designed with the resistance ratio of 3-V gamma correction. Somewhat, the measured result with its variation from -0.1V to -0.6V is not so well matching with the simulated result due to the variation of on-glass resistance after fabrication in LTPS process. Suitable adjustment on the layout of R-string resistance in the LTPS process, a more precise result of the proposed circuit I can be achieved.

As mentioned in Fig. 2.19 [55]. The two contacts of a serpentine resistor should reside as close to one another as possible to minimize the impact of thermoelectrics. The serpentine layout style in Fig. 2.19 (a) has large thermal variations due to an excessive separation between its contacts. In Fig. 2.19 (b), the layout reduces thermal variability and improves

matching by bringing the resistor heads into closer proximity. However, this layout is vulnerable to misalignment errors. If the resistor body shifts downward relative to the resistor heads, then the length of the resistor increases by twice the misalignment. This vulnerability can be eliminated by the layout style in Fig. 2.19 (c). Besides, the trimming technique [56] used in bandgap reference circuit can be further adopted to get precise output voltage for the proposed circuits on glass substrate.

Fig. 3.15 shows measured results in Vout and its variation for the proposed circuit II with gamma curve for 5-V liquid crystal panel but designed with the resistance ratio of 3-V gamma correction. As mentioned above, RA01-RA31 has guaranteed monotonicity to result in higher accuracy of amendment voltage Va, because the accuracy of Va is dependent on the ratio of resistors, not dependent on absolute resistor values. The measured results in the proposed circuit II show better consistent and much smaller variation (about -0.06V to 0.1V) to the ideal gamma curve with gamma value of 2.2. However, the proposed circuit II requires another supply voltage AVDD3.

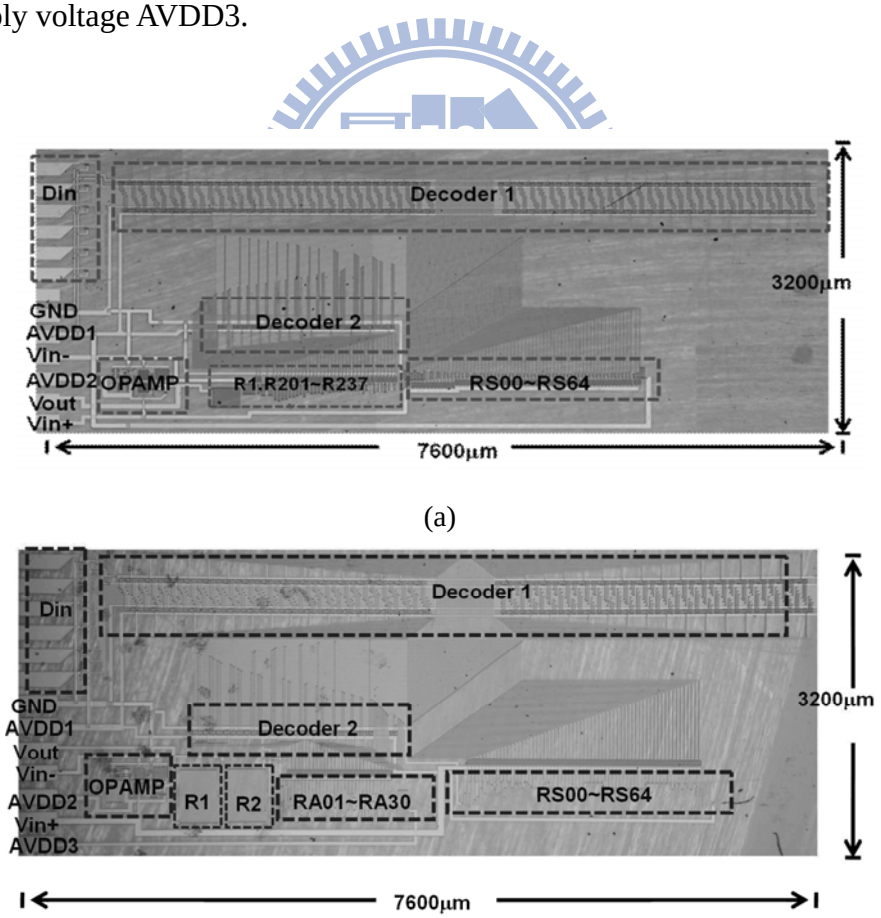
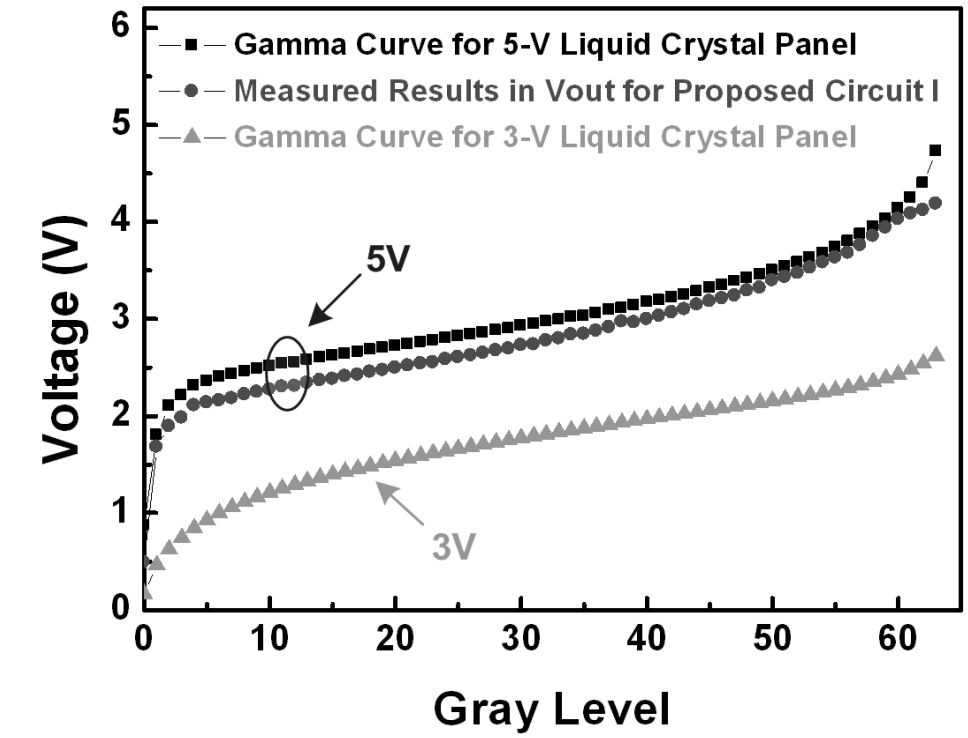
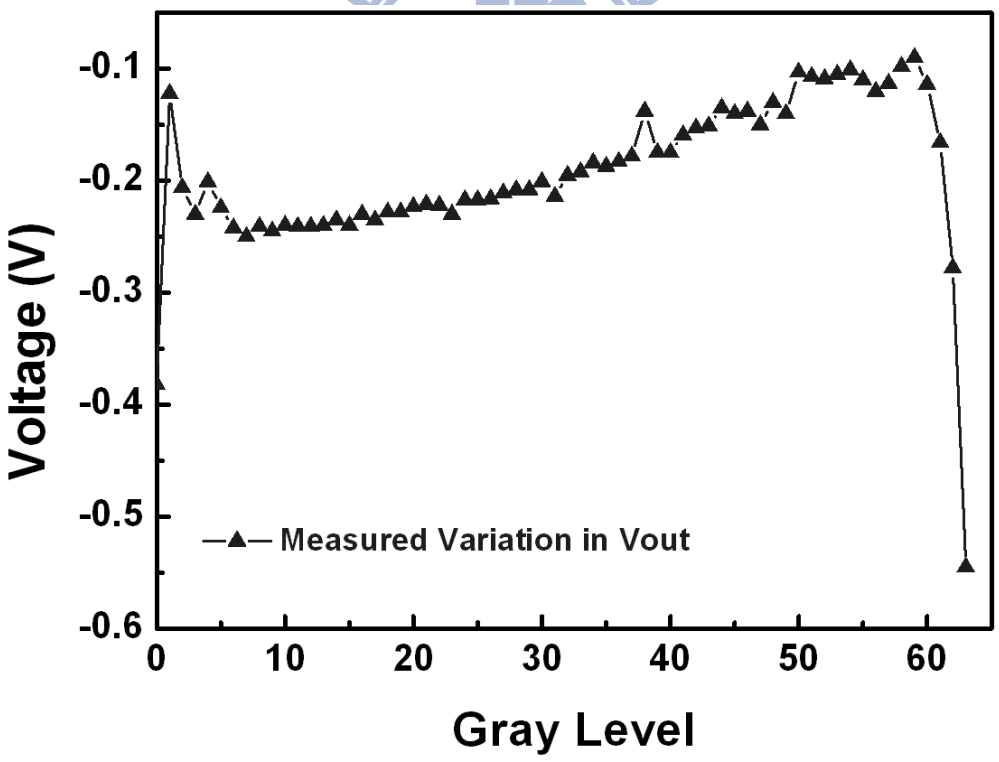


Fig. 3.13. Die photo of the fabricated (a) analog output buffer I, and (b) analog output buffer II, with level shifting function on glass substrate in a 3-μm LTPS technology.

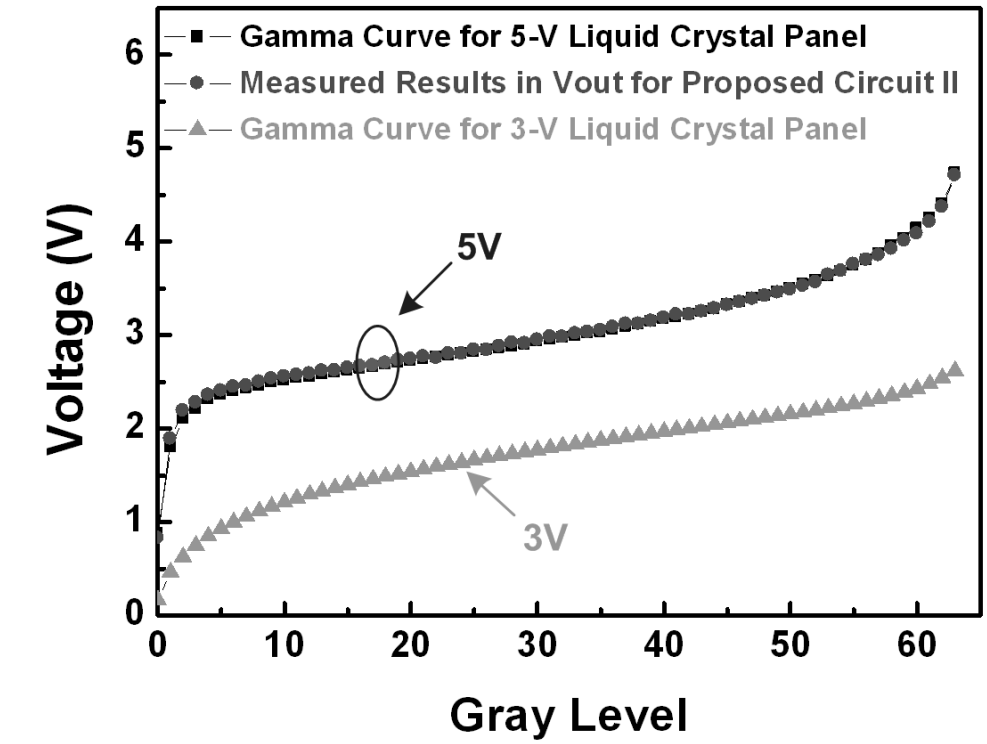


(a)

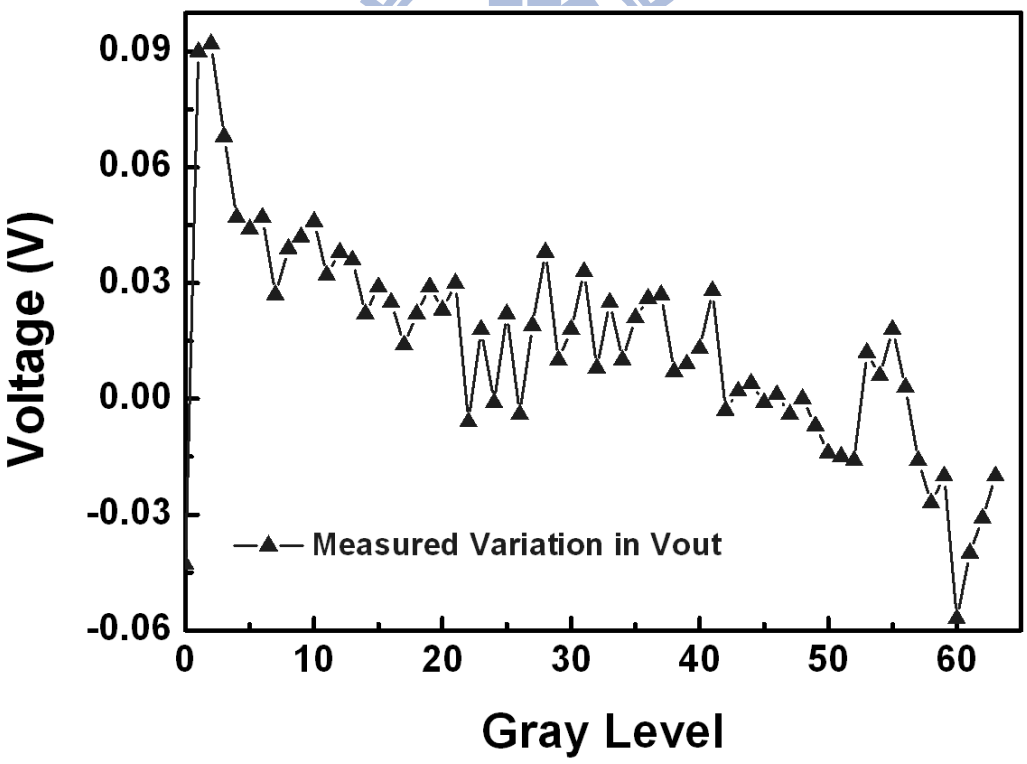


(b)

Fig. 3.14. Measured results for the new proposed circuit I in (a) Vout and (b) its variation with gamma curve for 5-V liquid crystal panel but designed with the resistance ratio of 3-V gamma correction.



(a)



(b)

Fig. 3.15. Measured results for the new proposed circuit II in (a) Vout and (b) its variation with gamma curve for 5-V liquid crystal panel but designed with the resistance ratio of 3-V gamma correction.

3.5 Summary

In order to realize the requirement that using the DAC with gamma correction of 3-V liquid crystal (LC) specification to drive the 5-V liquid crystal with the desired 5-V gamma curve without re-designing the DAC with 5-V gamma correction parameters, the two-stage OP amp is applied in the proposed circuits due to its larger unity-gain frequency, better slew rate, lower input offset voltage, better immunity to noise, and more steady circuit performance.

With design consideration aforementioned in chapter 1.4, two analog output buffers with level shifting function on glass substrate for panel application has been successfully designed and fabricated in a 3-μm LTPS technology. By using OPAMP, decoder 2, R1, R201-R237, MR01-MR37, and DAC with 3-V gamma correction parameters, the new proposed analog output buffer I can drive 5-V liquid crystal panel without re-designing the DAC with 5-V gamma correction parameters. By utilizing amendment voltage Va derived from RA01-RA31 and MA01-MA30, the measured results in the new proposed analog output buffer II show better consistent to ideal gamma curve with gamma value of 2.2.

The content of this chapter was co-work with Mr. Sao-Chi Chen when he studied his B.S. degree in National Chiao-Tung university [69], and was also published in [58], [59] with co-author of Mr. Sao-Chi Chen.

Chapter 4

Readout Circuit on Glass Substrate for Touch Panel Applications

A readout circuit on glass substrate for touch panel application has been designed and fabricated in a 3-μm low temperature poly-silicon (LTPS) technology. In this work, the switched-capacitor (SC) technique is applied to amplify the small voltage difference from capacitance change due to the touch event on panel. In addition, the correlated double-sampling (CDS) technique is also employed to reduce the offset originated from LTPS process variation. The minimum detectable voltage difference of the proposed circuit is 40 mV. To further identify the different touch area during touch events, a 4-bit analog-to-digital converter is used to converter the output of readout circuit into 4-bit digital codes [70], [71].

4.1 Introduction

Owing to the higher carrier mobility, lower threshold voltage, and higher stability of low temperature poly-silicon (LTPS) thin-film transistors (TFTs), some analog and digital circuits have been integrated on glass substrate in the active-matrix liquid crystal display (AMLCD) [72]-[74]. By integrating peripheral functional circuits on the display panel, higher resolution, smaller size, and high reliability can be further achieved for the system-on-panel (SOP) application. Since the carrier mobility depends on the grain size of the active poly-Si layer, the deviation of the TFT characteristic is dependent on the quality of the poly-Si layer. The device variation compression is especially needed to be considered when the peripheral functional circuits are integrated on panels [36], [58], [75].

Since some remarkable advances had been made for peripheral functional circuits, more kinds of circuits had been also implemented on the glass substrate for SOP applications [38], [48], [61]. In [76], a metal-nitride-oxide-silicon one-time-programmable cell with fast programming, high reliability, and fully process compatible to low-temperature polycrystalline-silicon panel had been reported for system-on-panel application. Through

channel FN programming, superior data retention and low-power operation were therefore achieved. In [77], an amplitude-shift-keying (ASK) demodulator implemented in LTPS technology for RF identification tags embeddable on panel displays had been reported with the highest ASK modulated data rate of 100 kb/s.

Recently, touch sensing gets great demand on panel applications such as PDA, tabled PCs, and smart phones, due to its intuitive operation and the advantages of easier and faster entry of the information. Integration of touch sensing function is convinced to be one of the value-adding solutions that can be applicable to the present flat panel displays (FPDs) [78]-[80].

4.2 Conventional Readout Circuits

4.2.1 Touch Panel Controller

Fig. 4.1 shows the block diagram of touch panel controller implemented with LTPS TFTs on a glass substrate to control a 4-wire resistive touch panel [78]. It induces voltage gradient across either plate of a 4-wire resistive touch panel, and senses the intermediate potential at the touch position. After that, the sensed potential is compared with seven reference voltages and the 7-bit output of the comparators is converted to two sets of 3-bit data for the x- and y-coordinate respectively by the encoder. According to the 6-bit data, the touch position in x- and y-direction can be obtained.

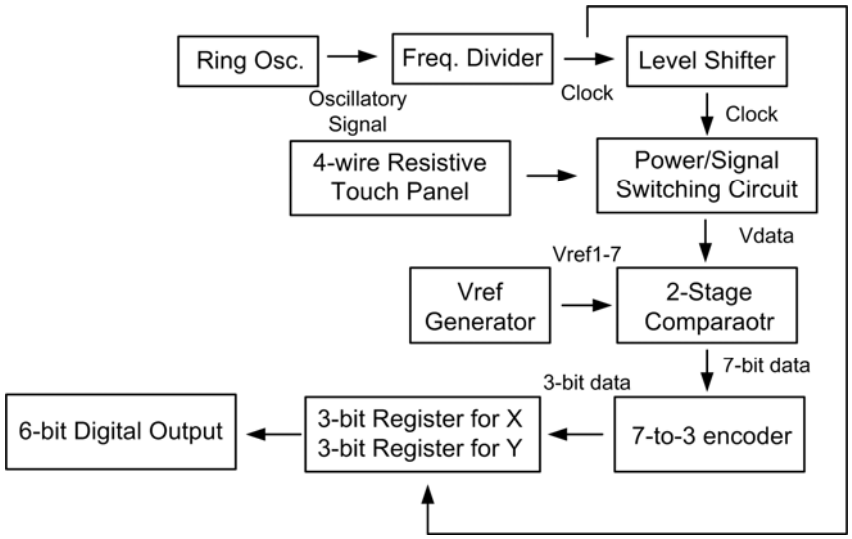


Fig. 4.1. The block diagram of touch panel controller [78].

4.2.2 Touch-Sensor-Embedded Display Panel

Fig. 4.2 shows the readout circuit of the integrated long-side of the LCD driver IC (LDI) with readout function for touch-sensor-embedded display panels [79]. An electric charge is generated in the photo TFT depending on the intensity of incident light. The input current is converted into voltage signal through the integrator. When the Reset is high, the feedback capacitor C_i is shorted and V_{o_op1} equals to V_{ref} and plus its own voltage corresponding to the given input current. This voltage, V_r, is stored in C_r when SPL0 is set to low. When the Reset is low, the input current is converted into output voltage by the integrator. The output voltage of V_{o_op1} decreases with time and the voltage at the falling edge of SPL1, V_s, is stored on C_s. With global charge amplifier and ADC, the difference between V_r and V_s can be distinguished and digitalized into 8-bit digital codes [79].

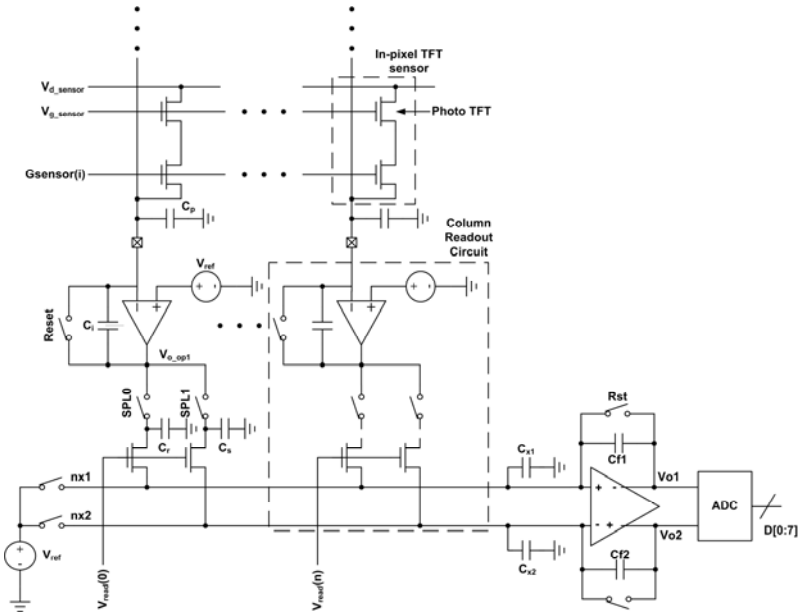


Fig. 4.2. The readout circuit of the integrated long-side of the LCD driver IC (LDI) with readout function for touch-sensor-embedded display panels [79].

4.2.3 Liquid Crystal Capacitive Sensor Circuit

Fig. 4.3 shows the embedded liquid crystal capacitive sensor and its readout circuit [80]. In Fig. 4.3(a), the voltage of V_{gw} is controlled by the coupling effect from Gn in the reading period. The liquid crystal capacitance (C_{lc}) is defined by a sensor gap between the common electrode and sensor electrodes on a TFT substrate. The sensor gap is reduced when the

sensor is touched. Therefore, the capacitance is increased as well as the voltage of V_{gw} is decreased. The voltage difference at V_{gw} can be further amplified and converted into current signal (I_{ro}) by TFT_1. Fig. 4.3(b) shows the readout circuit with the integrator and the A/D converter. The output voltage (V_{ro}) is reset to V_{ref} first. Due to the voltage difference from V_{gw}, I_{ro} in the non-touch state is larger than that in the touch state. By applying the A/D converter, the touch and non-touch events can be converted to the digital output.

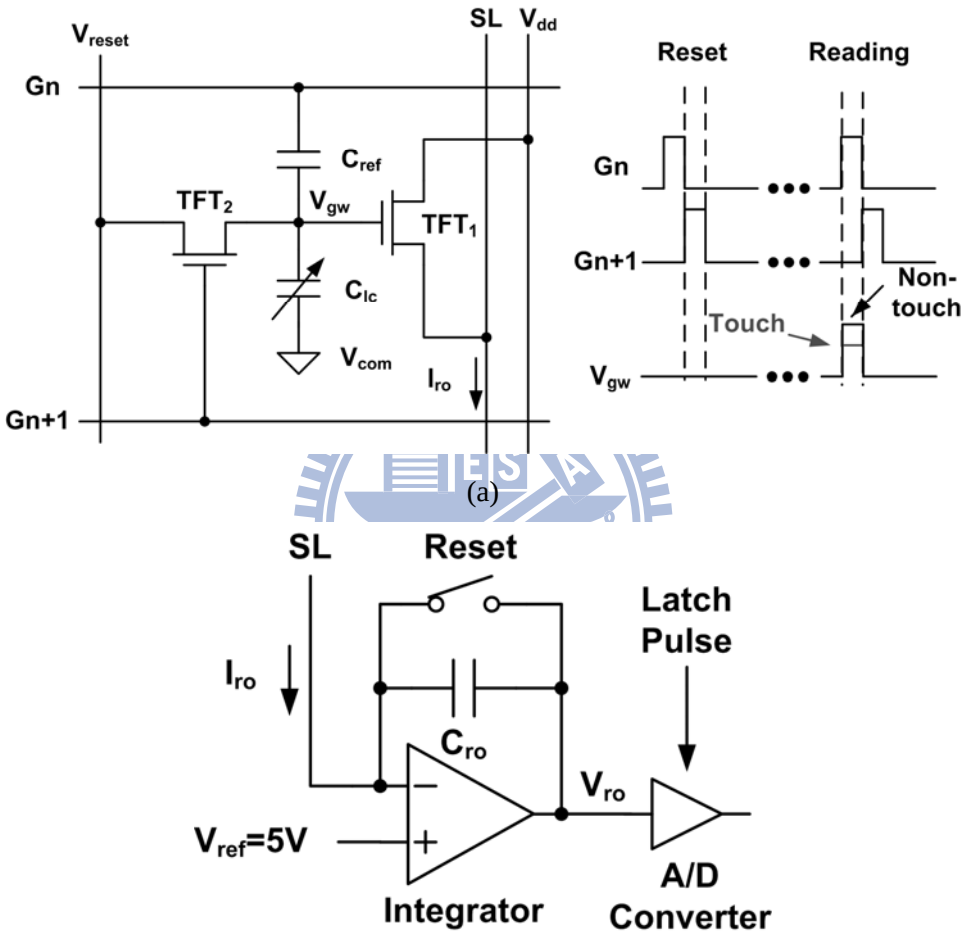


Fig. 4.3. (a) Liquid crystal capacitive sensor circuit and (b) the corresponding readout circuit [80].

In this work, a new readout circuit on glass substrate for touch panel application has been designed and fabricated in a 3-μm low temperature poly-silicon (LTPS) technology. Fig. 4.4 shows the block diagram of touch panel system. There are totally 14 and 8 capacitive sensor lines in the x- and y-direction respectively on the touch panel. When the touch panel is touched, the total capacitance of the capacitive sensor line will be changed. By applying the

switched-capacitor (SC) circuit, the voltage difference from capacitance change due to the touch events can be amplified. In addition, the corrected double-sampling (CDS) technique is also employed to reduce the offset originated from process variation. To further identify the different touch area during the touch events, a 4-bit analog-to-digital converter (ADC) is used to converter the output of readout circuit into 4-bit digital codes. Finally, by analyzing the 4-bit digital codes, the corresponding functions, such as zoom in, zoom out, move, and so on, can be performed on the touch panel by the appropriate algorithm of software in the system.

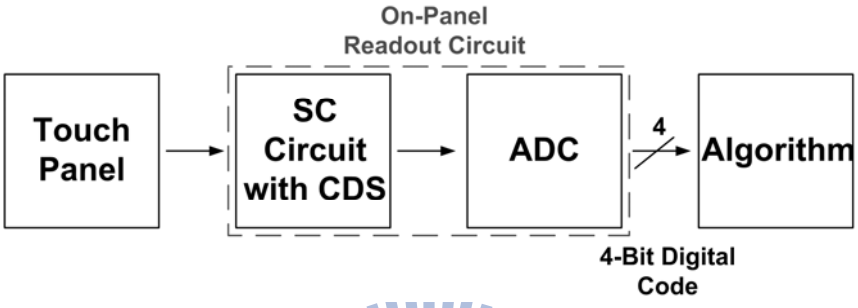


Fig. 4.4. The block diagram of touch panel system.

4.3 On-Panel Readout Circuit for Touch Panel Applications

4.3.1 Equivalent Model of the Capacitive Sensor Line

Fig. 4.5 shows the equivalent RC model of one capacitive sensor line on a 2.8 inch touch panel provided by the panel manufactory with total R of 150 kΩ and C of 100 pF. The Fanout block is the equivalent parasitic RC network of the interconnect line between the sensor line to the output node Fin. The touch capacitor ($C_{\_touch}$) is varied from 0.5 pF to 2 pF according to the different touch area. When the sensor line is touched by the finger, $C_{\_touch}$ is added in parallel to the touched node and the total capacitance on the capacitive sensor line is also changed. Since the different touch area is represented by different digital outputs of readout circuits, multi-touch events can be further determined by analyzing both digital outputs of readout circuits in the x- and y-direction through the appropriate algorithm of software in the system.

In order to discriminate between the touch and non-touch events, that is, to detect the capacitance change from $C_{\_touch}$, each node on the sensor line is pre-charged to 6 V at the beginning. When the touch event happened, the voltage at the output node Fin (V_{Fin}) will be

changed to

$$V_{FIN} = \frac{C_{total}}{C_{total} + C_{\_touch}} \cdot V_{pre-charge}, \tag{4.1}$$

where $V_{pre\text{-}charge}$ = 6 V, C_{total} = 100 pF, $C_{\_touch}$ = 0.5 pF - 2 pF. Therefore, the voltage level at output node Fin under the touch event can be derived from 5.88 V to 5.97 V with the corresponding $C_{\_touch}$ value from 2 pF to 0.5 pF. For such a capacitive sensor line, the capacitance change due to the touch event can be indicated by the voltage change. So the on-panel readout circuit is designed to distinguish the voltage difference at the Fin node. In this work, the switch-capacitor (SC) technique is applied to enlarge the voltage difference from capacitance change in the touch panel and the corrected double-sampling (CDS) technique is employed to reduce the offset owing to process variation. In addition, the different touch area is further identified by the 4-bit digital output code from on-panel analog-to-digital converter (ADC).

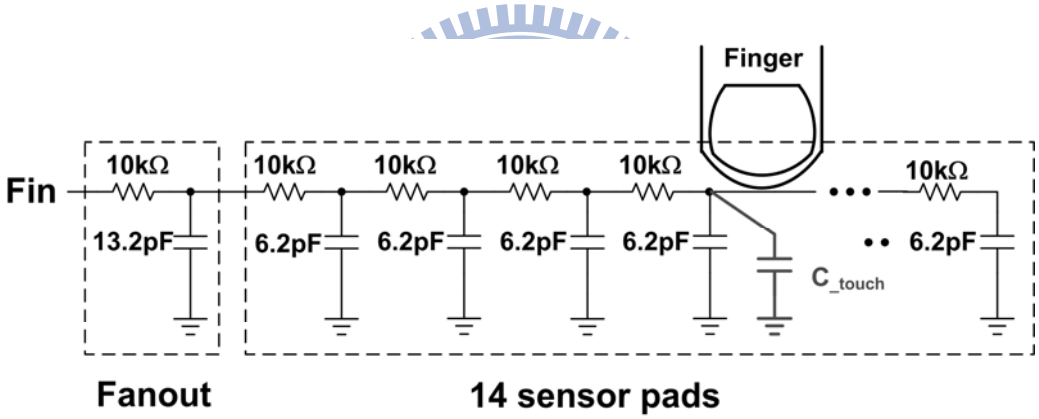


Fig. 4.5. The equivalent RC model of one capacitive sensor line on a 2.8 inch panel.

4.3.2 Design Consideration and Circuit Implementation

From design consideration aforementioned in chapter 1.4, the device characteristic variations in LTPS technology are quite larger compared with CMOS technology, so the effect of device variation must be considered for on-panel circuit design. In chapter 3, a two stage OP amp. on glass substrate had been implemented and discussed in [69]. Since Miller compensation and nulling resistor are necessary for two-stage OP amp., random device-to-device variation on resistor and capacitor in LTPS process exert quite influence on performance of two-stage OP amp. Therefore, the folded-cascode operational amplifier is utilized in the proposed circuit. In addition, the corrected double-sampling (CDS) technique

is employed for on-panel circuit design to reduce the offset originated from LTPS process variation.

Fig. 4.6 shows the new proposed on-panel readout circuit for touch panel applications in a 3-μm LTPS technology. The proposed circuit is designed to detect the capacitance change from the capacitive sensor line shown in Fig. 4.5. The proposed circuit is composed of two parts. One is the switched-capacitor (SC) circuit with correlated double sampling (CDS) technique [44], and the other is on-panel analog-to-digital converter (ADC) [81]. The SC technique is applied to amplify the small voltage difference between V_i and V_{ref} with the factor of C_1/C_2, where V_i is the voltage from the output node (Fin) of the sensor line. Since the TFTs suffer large device variation in LTPS process compared with that in CMOS silicon process, the CDS technique is utilized to eliminate the offset of operation amplifier (OP). The effect of the input offset can be modeled as an error voltage source (V_{os}) placed in series with the positive input of OP.

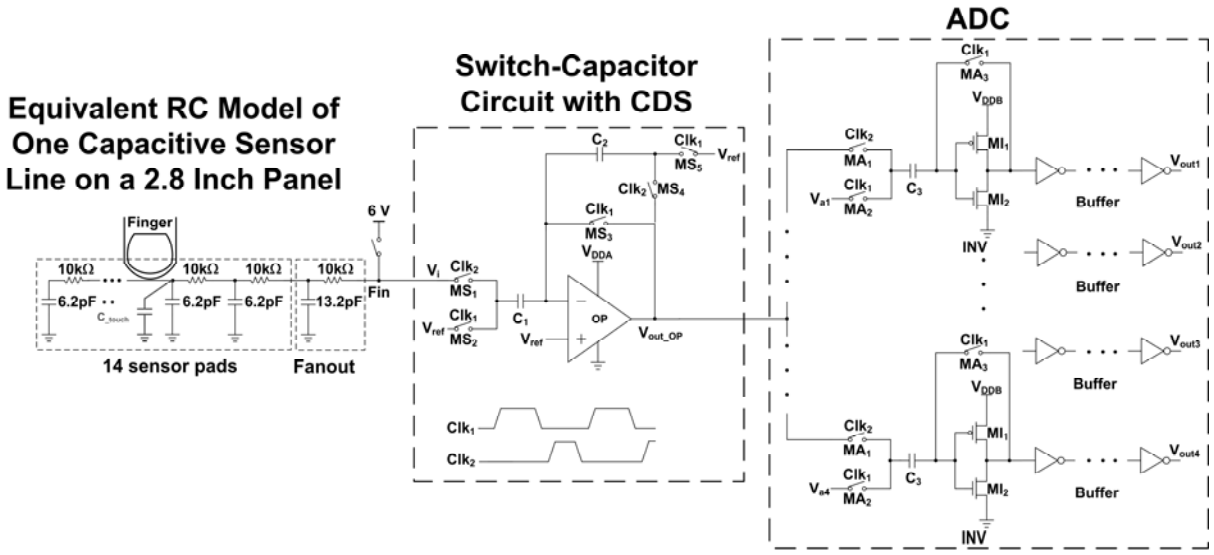


Fig. 4.6. New proposed on-panel readout circuit to sense the voltage change due to the capacitance change on the touch panel in a 3-μm LTPS technology.

Fig. 4.7 shows the on-panel switched-capacitor circuit with CDS during the logical high in (a) Clk_1 and (b) Clk_2. In Fig. 4.7 (a), the voltage across C_2 is reset and both the voltages across C_1 and C_2 are equal to the input offset of OP ($V_{os}(t_1)$) at t1. In Fig. 4.7 (b), V_i charges C_1 and the charging current flows across C_2. Consequently, the change in charge across C_1 equals to the change in charge across C_2. So, the output voltage (V_{out_OP}) at t_2 can be derived by

$$V_{out\_OP}(t_2) = V_{ref} + \frac{C_1}{C_2} \cdot (V_{ref} - V_i) + [V_{os}(t_2) - V_{os}(t_1)] \cdot \left(1 + \frac{C_1}{C_2}\right), \quad (4.2)$$

whereas the output voltage is only valid during the logical high in Clk_2. The offset voltage is also cancelled since the error voltage source was assumed to be independent of time.

The second part of the proposed circuit is the on-panel ADC. Since the voltage level at V_{out_OP} with analog signals usually cannot be directly applied for digital processing when the sensor line is touched, an on-panel ADC is required. Furthermore, with different V_a (V_{a1} to V_{a4}) of reference voltage, the output voltage of OP (V_{out_OP}) can be digitalized according to the different input voltage (V_i). As the Clk_1 is high, the logical threshold voltage (V_t) of the inverter (INV) is stored in C_3 as well as V_a. When the Clk_2 is high, (V_{out_OP}+V_t-V_a) is applied to the input of INV and the logical threshold voltage (V_t) of the INV can be further cancelled. Therefore, the output of ADC depends only on (V_{out_OP}-V_a) and it shows logical high when the sensor line is touched. Finally, the different touch area can be identified by the 4-bit digital output (V_{out1} to V_{out4}) from on-panel ADC.

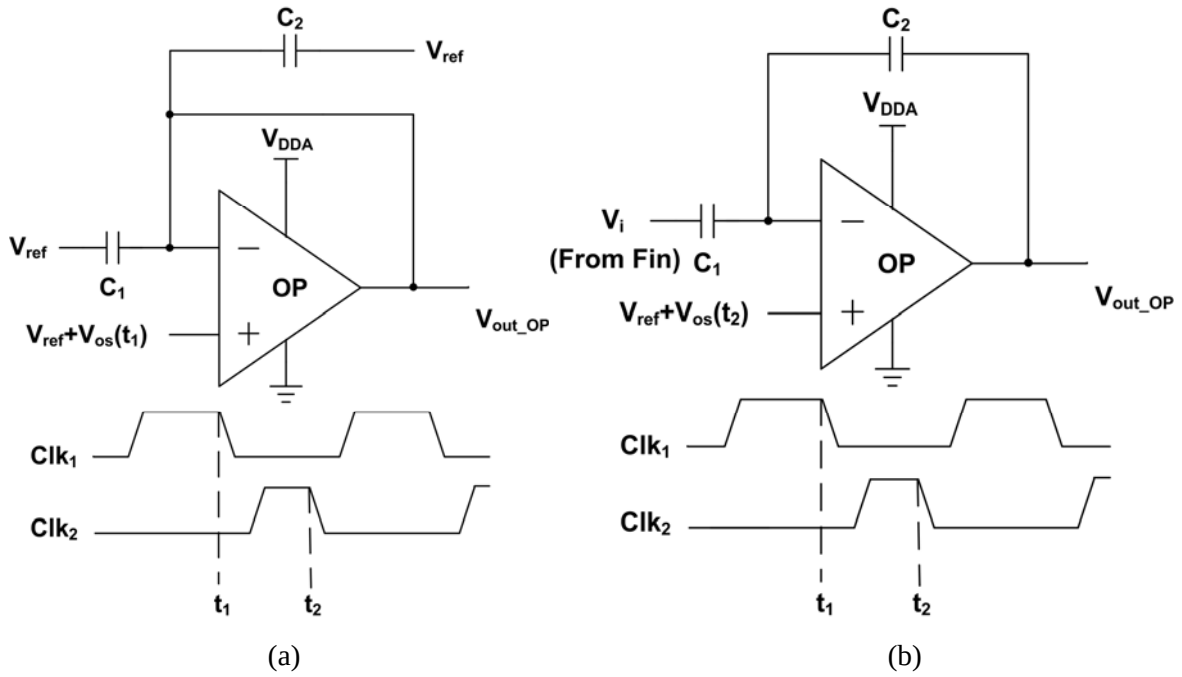


Fig. 4.7. The proposed switch-capacitor readout circuit with CDS during the logical high in (a) Clk_1 for reset with offset storage and (b) Clk_2 for amplification and offset cancellation.

The schematic diagram of the folded-cascode operational amplifier (OP) used in this work is shown in Fig. 4.8. Compared with the traditional two stage operational amplifier, this

architecture exhibits better input common mode range, power supply rejection ratio, larger gain, and easier frequency compensation [44]. The proposed circuit has been designed and verified by the Eldo software with the RPI model (Level=62) in a 3-μm LTPS process [82]. With consideration of implementation for SC and CDS techniques, and requirement for operating frequency (tens herts) and detection range (0.5 pF~ 2 pF) of touch panel applications, the simulated frequency response of the folded-cascode OP in open-loop condition is shown in Fig. 4.9 under the supply voltage (V_{DDA}) of 10 V. The DC gain and the phase margin are 60.5 dB and 70°, respectively. The simulated unit gain bandwidth is 12.8 MHz. Fig. 4.10 shows the simulated output voltage of the switch-capacitor circuit with CDS. The output voltage shows 6.89 V, 6.69 V, 6.48 V, 6.26 V, and 6.03 V under V_i = 5.88 V, 5.91 V, 5.94 V, and 5.97 V, respectively. The output voltage is only valid when the Clk_2 is high.

Fig. 4.11 shows the simulated result of the proposed circuit under the non-touch event with V_{DDA} = V_{DDB} = 10 V, V_{ref} = 6 V, V_{a1} = 6.15 V, V_{a2} = 6.36 V, V_{a3} = 6.6 V, V_{a4} = 6.8 V, Clk_1 = Clk_2 = 100 kHz, C_1 = 8 pF, and C_2 = 1 pF. By applying the SC and CDS technology, the output voltage of the proposed circuit (V_{out1} to V_{out4}) is only valid when the Clk_2 is high. Therefore, the non-touch event of the proposed circuit shows the digital output code of '0000' when the Clk_2 is high. Fig. 4.12 shows the simulated results under different V_i. The digital code of ADC presents '1111,' '1110,' '1100,' and '1000' under V_i = 5.88 V, 5.91 V, 5.94 V, and 5.97 V, respectively.

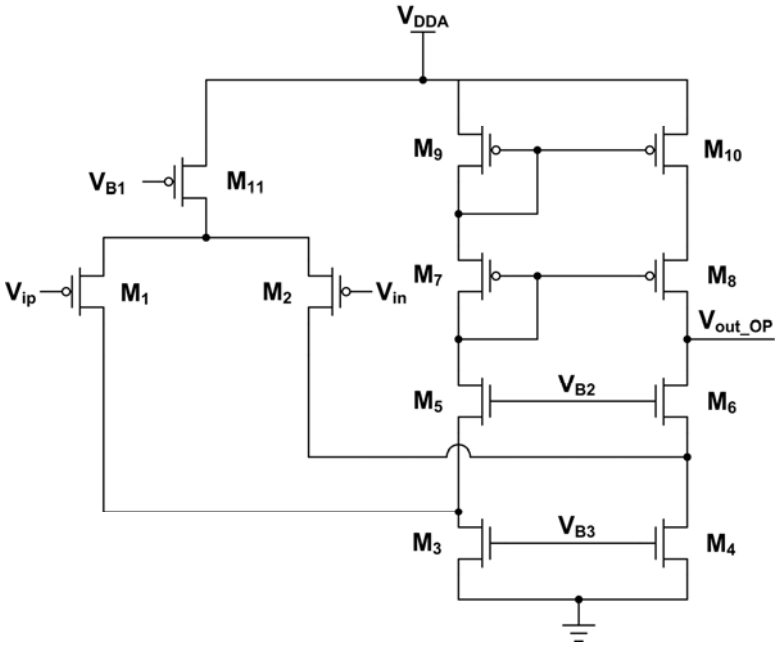


Fig. 4.8. The schematic diagram of the folded-cascode operational amplifier (OP).

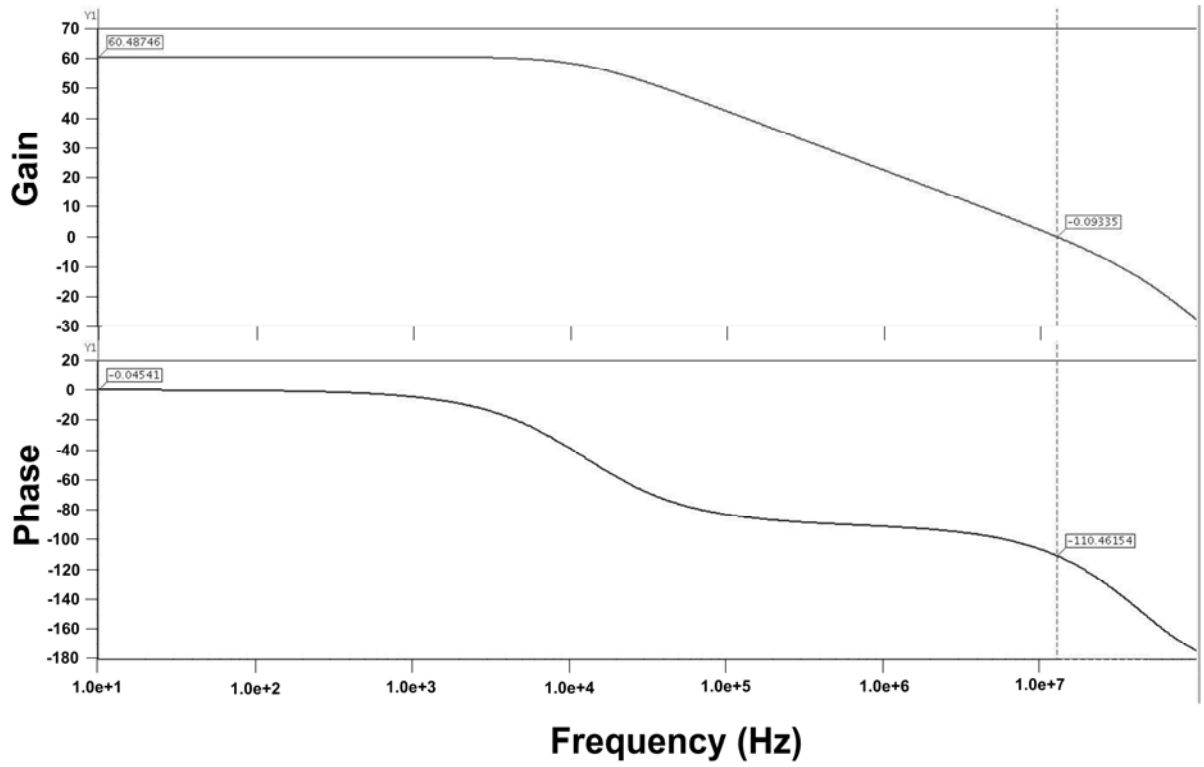


Fig. 4.9. The simulated frequency response of the folded-cascode operational amplifier in open-loop condition.

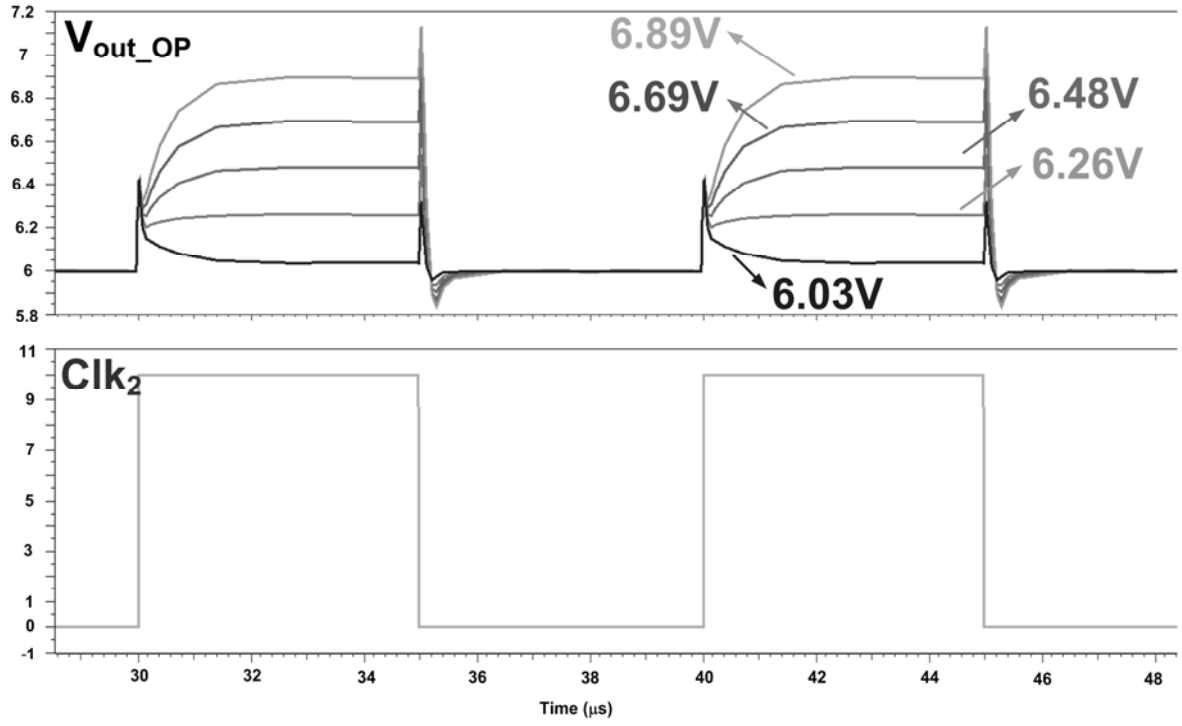


Fig. 4.10. The simulated output voltage of the switch-capacitor circuit with CDS with different input signals from V_i.

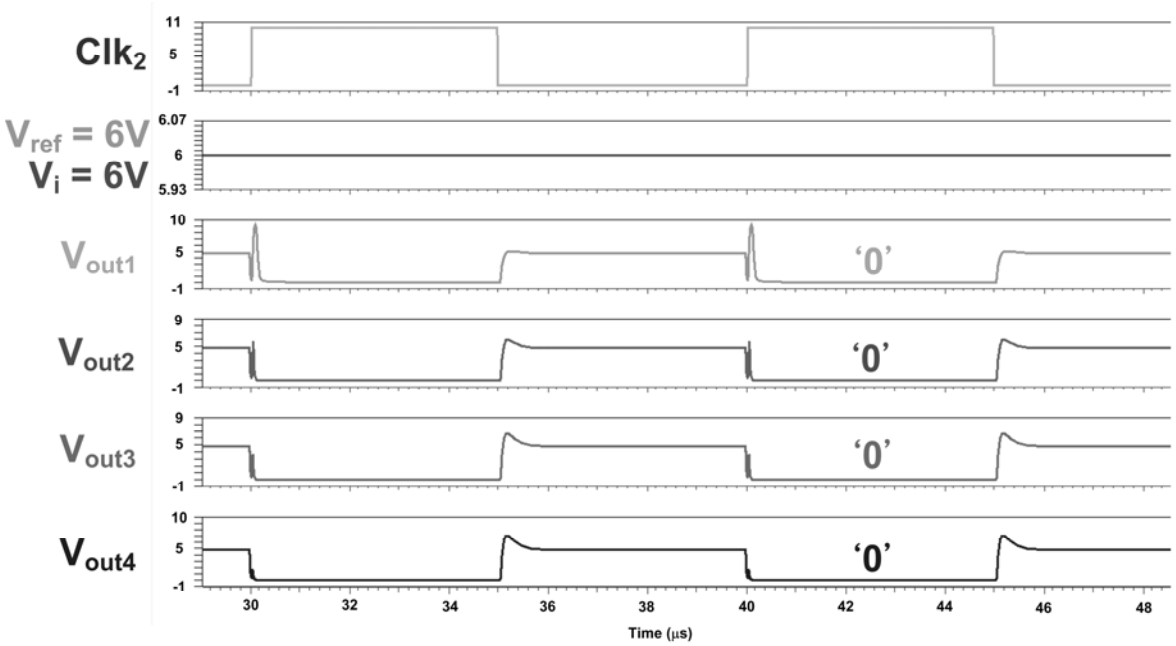


Fig. 4.11. The simulated result of the proposed circuit under the non-touch event with the digital output code of '0000'.

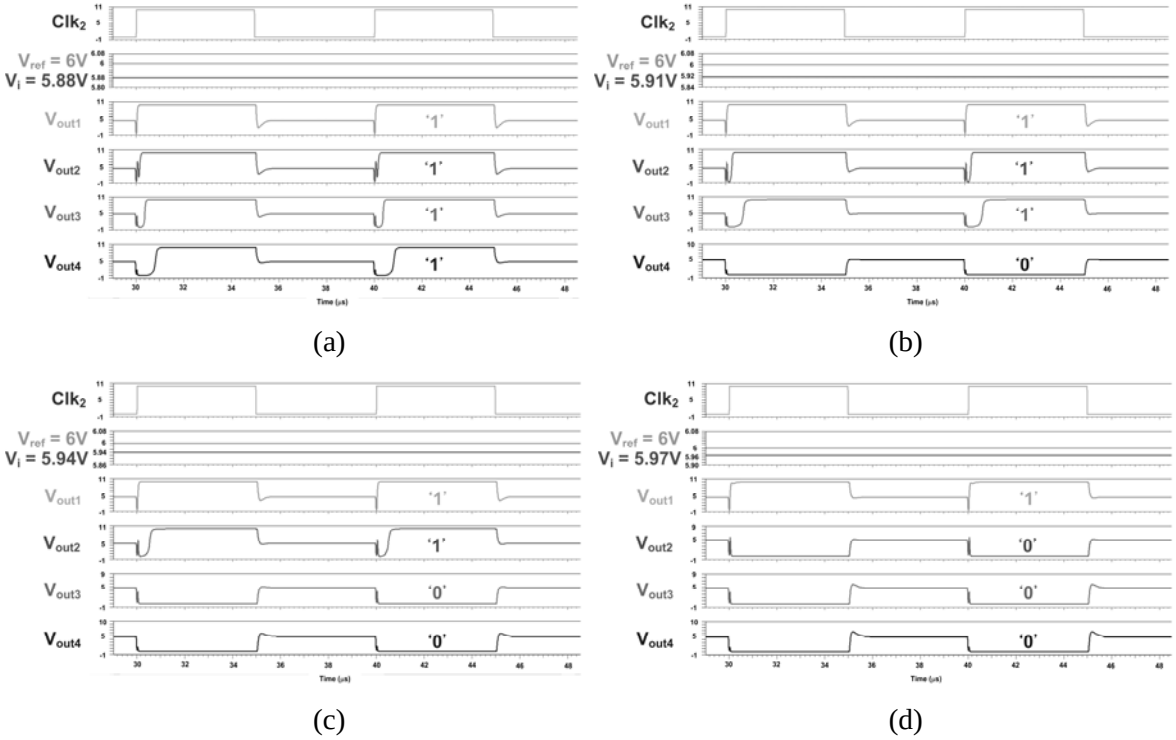


Fig. 4.12. The simulated results of the proposed readout circuit with (a) V_i = 5.88 V (digital output code: '1111'), (b) V_i = 5.91 V (digital output code: '1110'), (c) V_i = 5.94 V (digital output code: '1100'), and (d) V_i = 5.97 V (digital output code: '1000'), where the V_{ref} is kept at 6 V.

4.4 Experimental Results

4.4.1 Indium Tin Oxide

The new proposed circuits have been designed and fabricated in a 3-μm LTPS technology. Fig. 4.13 shows the die photo of the fabricated readout circuit with Indium Tin Oxide (ITO) on glass substrate, where the ITO is utilized to verify the capacitive sensor line shown in Fig. 4.5. The ITO is drawn with the equivalent resistance of 150 kΩ in the square form instead of a line in Fig. 13 due to the limitation of layout area in the experimental chip. The area of ITO is 2800 μm x 2450 μm and the area of on-panel readout circuit is 980 μm x 630 μm. Fig. 4.14 shows the fabricated circuit on glass substrate with ITO to verify the readout function of the proposed circuit, when the ITO, which is utilized to verify the capacitive sensor line shown in Fig. 4.5, is touched by a finger. The 4-bit digital output code is utilized to identify the different touch area and to enhance the resolution of the touch panel.

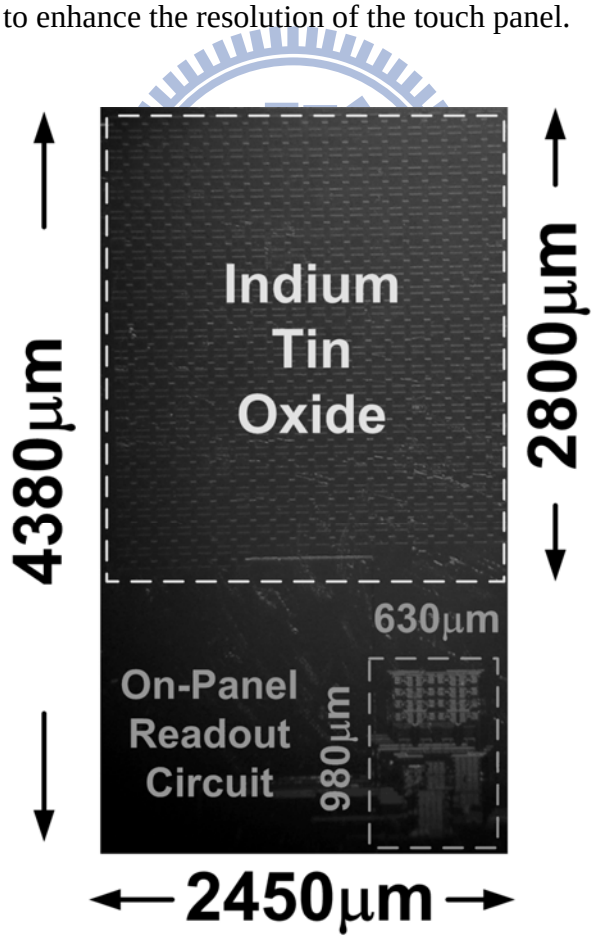


Fig. 4.13. The die photo of the fabricated readout circuit with Indium Tin Oxide (ITO) on glass substrate, where the ITO is utilized to verify the capacitive sensor line shown in Fig. 4.5.

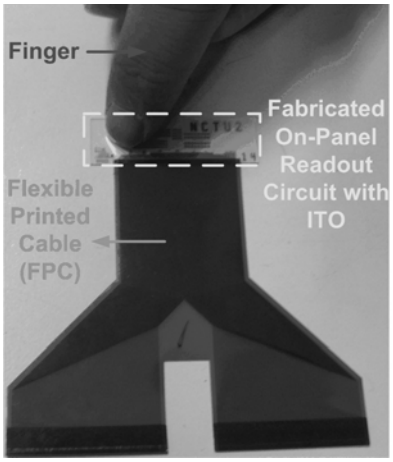


Fig. 4.14. The fabricated circuit on glass substrate with ITO to verify the readout function of the proposed circuit, when the ITO, which is utilized to verify the capacitive sensor line shown in Fig. 4.5, is touched by a finger.

4.4.2 Measured Results with External Applied Voltage

The fabricated readout circuit is first verified with the externally applied input signals (V_i). Fig. 4.15 shows the measured result of the fabricated circuit under non-touch event (V_i = 6 V), where the digital output code is '0000.' Fig. 4.16 shows the measured results of the fabricated circuit under different V_i. The digital output code shows '1111,' '1110,' '1100,' and '1000' under V_i = 5.88 V, 5.9 V, 5.93 V, and 5.96 V, respectively.

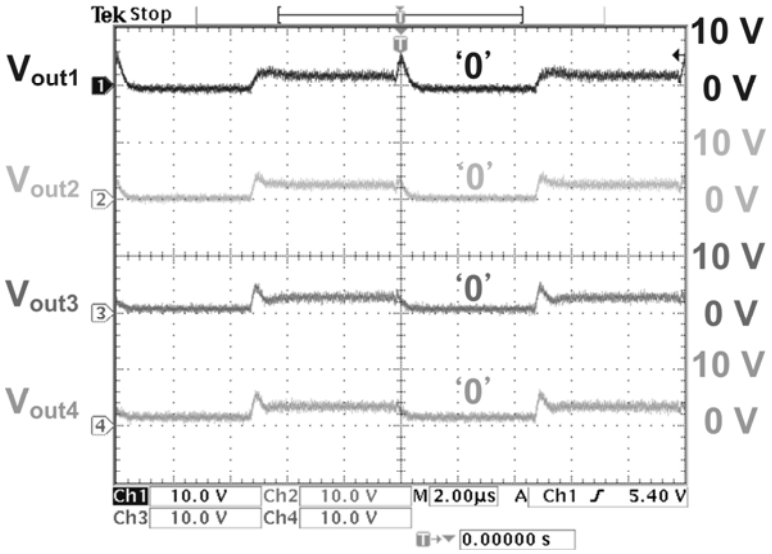
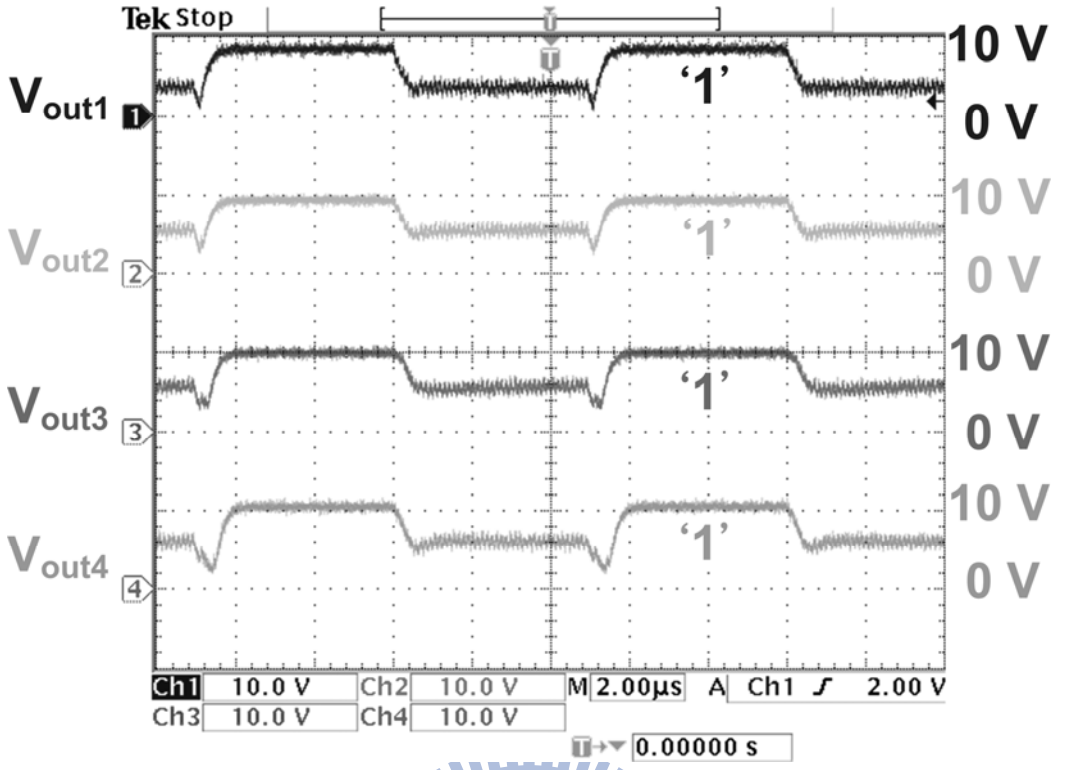
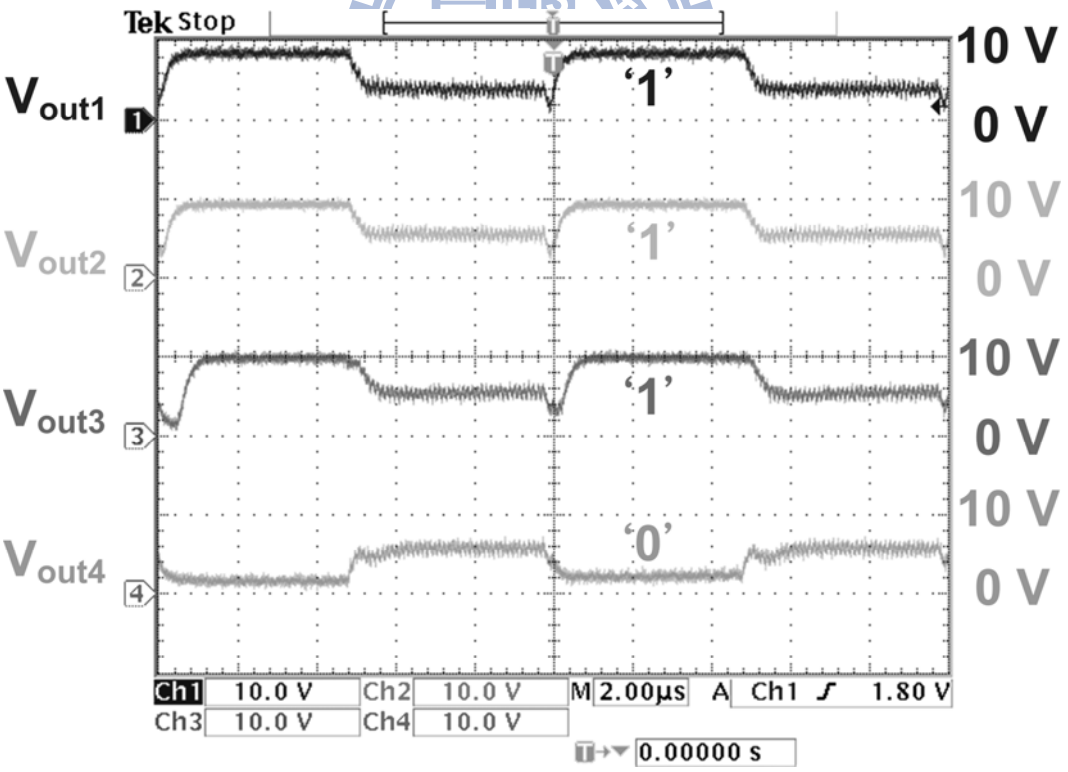


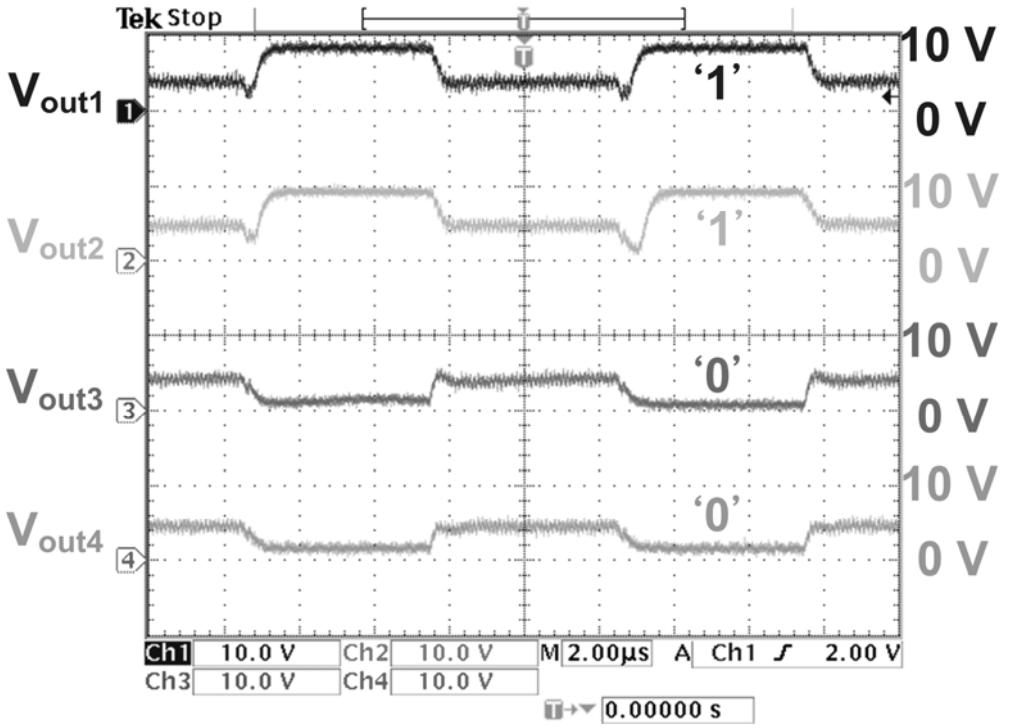
Fig. 4.15. The measured result of the fabricated circuit under non-touch event (Vi = 6V) with the output code of '0000'.


Tek Stop
Vout1
Vout2
Vout3
Vout4
'1'
'1'
'1'
'1'
10 V
0 V
10 V
0 V
10 V
0 V
10 V
0 V
Ch1 10.0 V Ch2 10.0 V M 2.00µs A Ch1 2.00 V
Ch3 10.0 V Ch4 10.0 V
0.00000 s

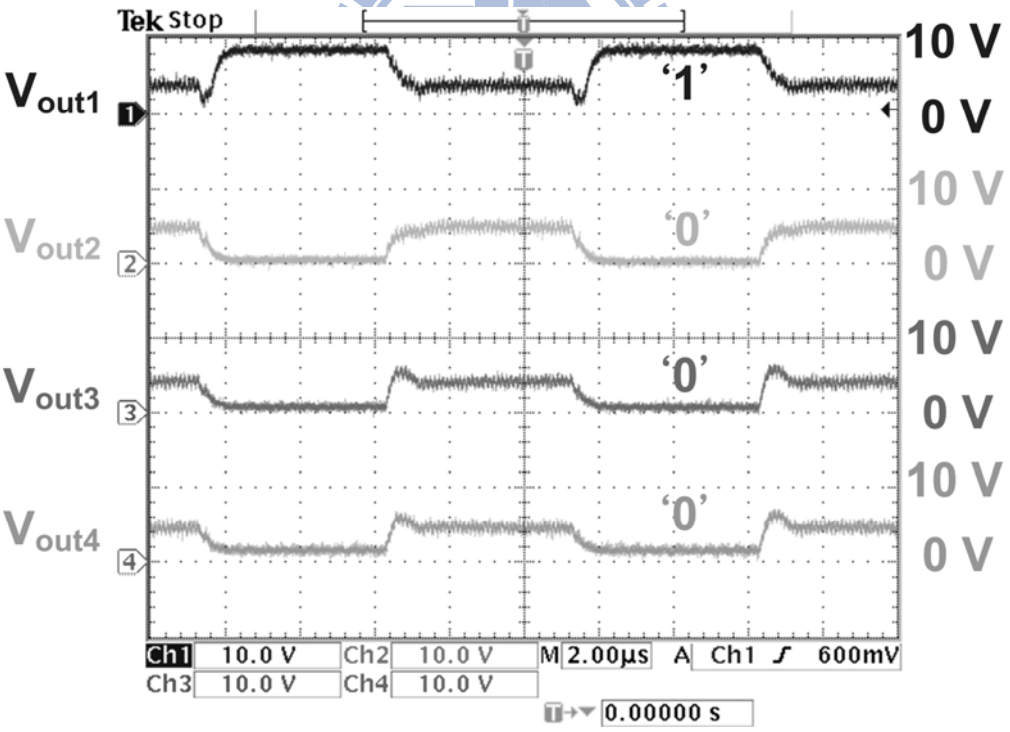
(a)


Tek Stop
Vout1
Vout2
Vout3
Vout4
'1'
'1'
'1'
'0'
10 V
0 V
10 V
0 V
10 V
0 V
10 V
0 V
Ch1 10.0 V Ch2 10.0 V M 2.00µs A Ch1 1.80 V
Ch3 10.0 V Ch4 10.0 V
0.00000 s

(b)



(c)



(d)

Fig. 4.16. The measured results of the fabricated readout circuit verified with the applied V_i signal of (a) 5.88 V (digital output code: '1111'), (b) 5.9 V (digital output code: '1110'), (c) 5.93 V (digital output code: '1100'), and (d) 5.96 V (digital output code: '1000'). The corresponding digital codes can be successfully generated at the output V_{out1}, V_{out2}, V_{out3}, and V_{out4}.

4.4.3 Measured Results under Touched Area of ITO by Finger

Since the TFTs may suffer large device variation in LTPS process compared with that in CMOS silicon process, the minimum detectable voltage difference is 40 mV in the measured results. After the successful verification of readout function, the fabricated chip is measured by the different touch area of the finger with a 100-pF capacitor connected to the Vi node, which is used to simulate the touching event modeled in Fig. 4.5. The different digital output codes are confirmed according to the different touch area of ITO. Fig. 4.17 shows the measured result of the fabricated circuit under non-touch event, where the digital output code is '0000.' Fig. 4.18 shows the measured results of the fabricated circuit under different touch area. The digital output code shows '1111,' '1110,' '1100,' and '1000' when the touched area by finger is covered with full, 3/4, 1/2, and less than 1/4 of the ITO area, respectively. By further analyzing the 4-bit digital codes, the corresponding functions, such as zoom in, zoom out, move, and so on, can be performed on the touch panel by the appropriate algorithm of software in the system.

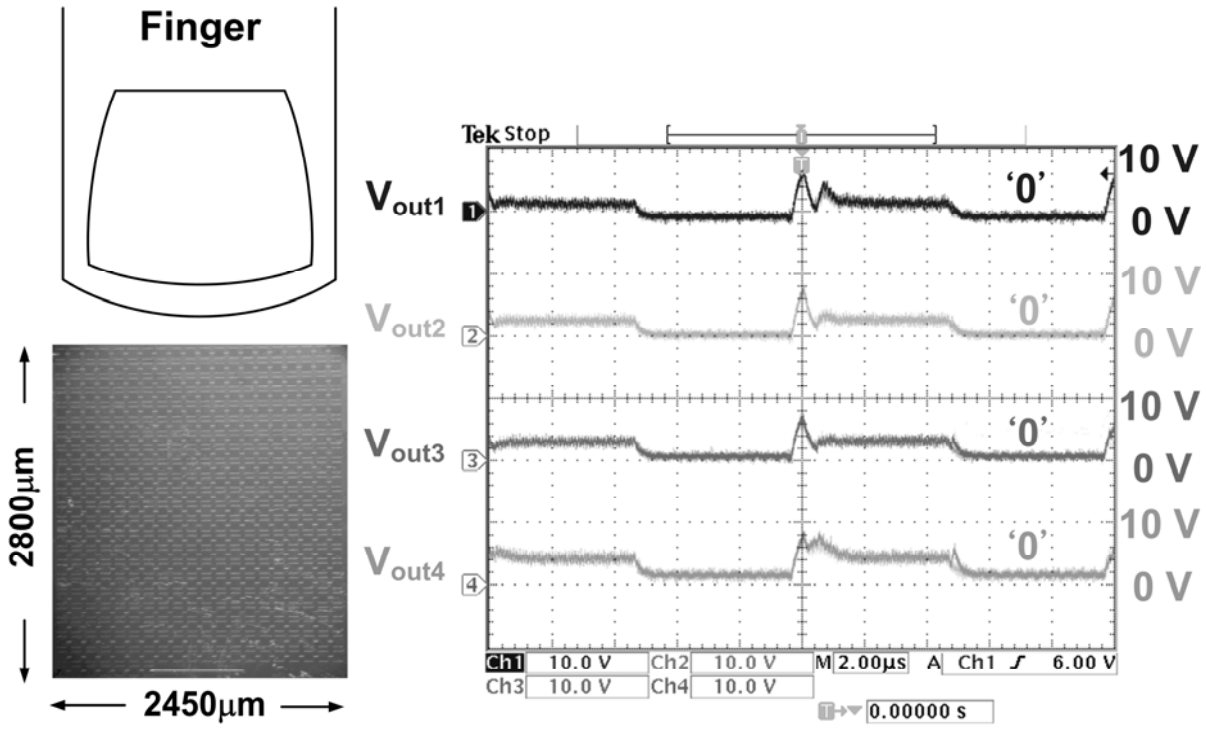
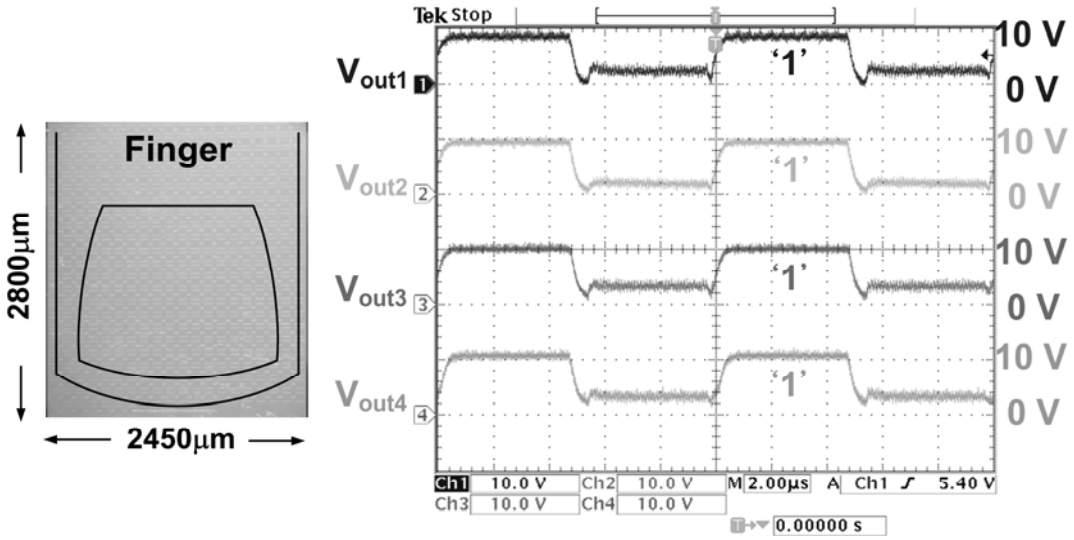
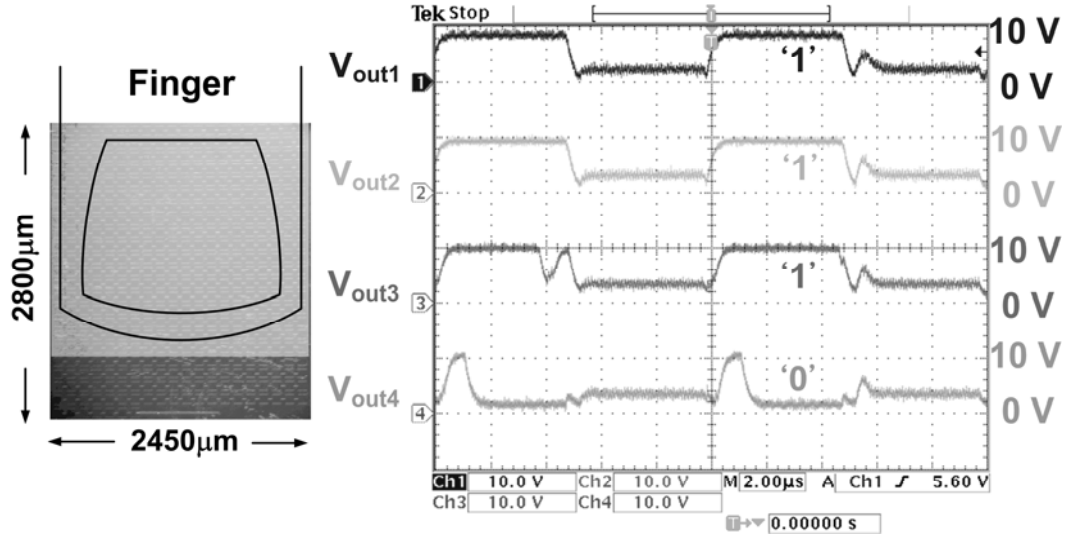


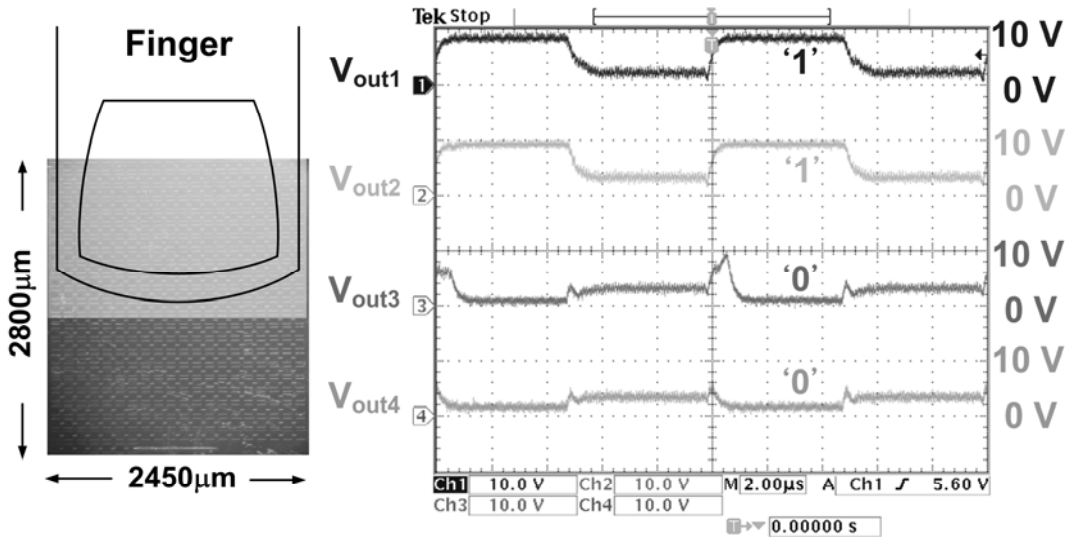
Fig. 4.17. The measured result of the fabricated circuit under non-touch event.


Finger
2800μm
2450μm
Tek Stop
Vout1
Vout2
Vout3
Vout4
'1'
'1'
'1'
'1'
10 V
0 V
10 V
0 V
10 V
0 V
10 V
0 V
Ch1 10.0 V Ch2 10.0 V M 2.00μs A Ch1 5.40 V
Ch3 10.0 V Ch4 10.0 V
0.00000 s

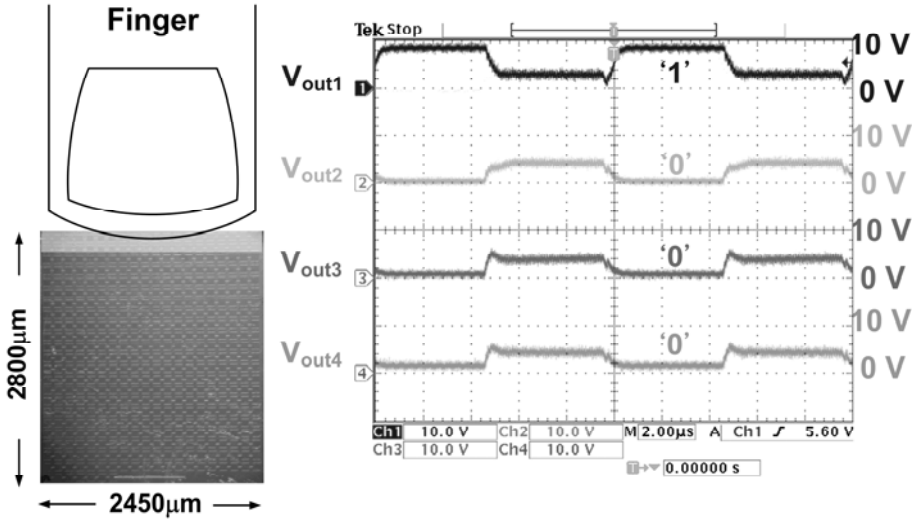
(a)


Finger
2800μm
2450μm
Tek Stop
Vout1
Vout2
Vout3
Vout4
'1'
'1'
'1'
'0'
10 V
0 V
10 V
0 V
10 V
0 V
10 V
0 V
Ch1 10.0 V Ch2 10.0 V M 2.00μs A Ch1 5.60 V
Ch3 10.0 V Ch4 10.0 V
0.00000 s

(b)


Finger
2800μm
2450μm
Tek Stop
Vout1
Vout2
Vout3
Vout4
'1'
'1'
'0'
'0'
10 V
0 V
10 V
0 V
10 V
0 V
10 V
0 V
Ch1 10.0 V Ch2 10.0 V M 2.00μs A Ch1 5.60 V
Ch3 10.0 V Ch4 10.0 V
0.00000 s

(c)



(d)

Fig. 4.18. The measured results of the fabricated readout circuit under the touched area by finger covered with (a) full, (b) 3/4, (c) 1/2, and (d) less than 1/4 of the ITO area.

4.5 Summary

A new on-panel readout circuit for touch panel applications has been designed and fabricated in a 3-μm low temperature poly-silicon (LTPS) technology. For the purpose of touch-event detection, the switched-capacitor (SC) technique is applied to enlarge the voltage difference from the capacitance change of touch panel. With design consideration in chapter 1.4, the folded-cascode operational amplifier is utilized in the proposed circuit instead of two-stage OP amp. because random device-to-device variation on unlling resistor and Miller compensation capacitor in LTPS process exert quite influence on the performance of on-panel readout circuit in LTPS process. In addition, the corrected double-sampling (CDS) technique is employed for on-panel circuit design to reduce the offset originated from LTPS process variation.

The minimum detectable voltage difference of the proposed circuit is 40 mV, with corresponding capacitance change of 0.5 pF under total capacitance of 100 pF, and the different touch area can be identified by the 4-bit digital output. The proposed readout circuit for touch panel application on glass substrate can be integrated in the active matrix LCD (AMLCD) panels to increase the sensing resolution of touch panel for SOP applications.

Chapter 5

Readout Circuit on Glass Substrate with Digital Correction for Touch Panel Applications

In this chapter, a readout circuit on glass substrate with digital correction for touch panel application, which contains transconductance amplifier, counter, and digital correction circuit, has been designed and simulated in a 3-μm low temperature poly-silicon (LTPS) technology. In this work, the voltage difference from capacitance change due to the touch event on panel is converted to current change by transconductance amplifier. By charging and discharging the capacitor in the counter, the counter displays different digital output codes according to touch or non-touch event. Furthermore, not only the touch or non-touch event can be distinguished but also the influence of process variation can be compensated by digital correction circuit.

5.1 Introduction

Low temperature poly-silicon (LTPS) technology exhibits numerous advantages over amorphous-silicon (a-Si) technology in display applications, resulting high resolution, small size, low power, high reliability, and further reduction in the cost. For these features, LTPS thin-film transistors (TFTs) can be utilized to achieve system-on-panel (SOP) applications, where some peripheral functional circuits are integrated on panel, such as digital-to-analog converter, timing controller, DC-DC converter, and interface circuits. Furthermore, the operating voltage and scale of device should be also shrunk for low power consumption and a narrow picture frame as the integration of peripheral functional circuits progresses [83]-[86]. Fig. 5.1 shows the trends in mobile system-on-panel liquid crystal displays [84]. Broadband services get great demands as wireless transmission speed is increasing, so the features of LTPS technology is highly requested to encourage the further spread of SOP applications.

SOP applications with LTPS TFTs had been developed for many years and the integration of peripheral functional circuits had also been achieved. By using LTPS TFT technology, a

2.2-inch QVGA format system display with integration of a low voltage 6-bit RGB parallel interface circuit was developed [87]. A low voltage interface circuit with 1.8-V operating voltage and a horizontal driver, which allows for narrower frame width, were integrated in this panel. In [88], a low-power and small-area holding latch with level-shifting function using LTPS TFTs for mobile applications was proposed with a 5-μm design rule on a glass substrate for power and cost effectiveness. In [89], a novel low-power consumption all-digital system-on-glass display with serial interface was mentioned by combining the technique of integration of serial data receiver function and pixel memory circuits. This panel switches the display mode according to the command and all the data are directly communicated with circuits inside panel. In addition, the number of interface pins is very few so it is suitable for the portable products.

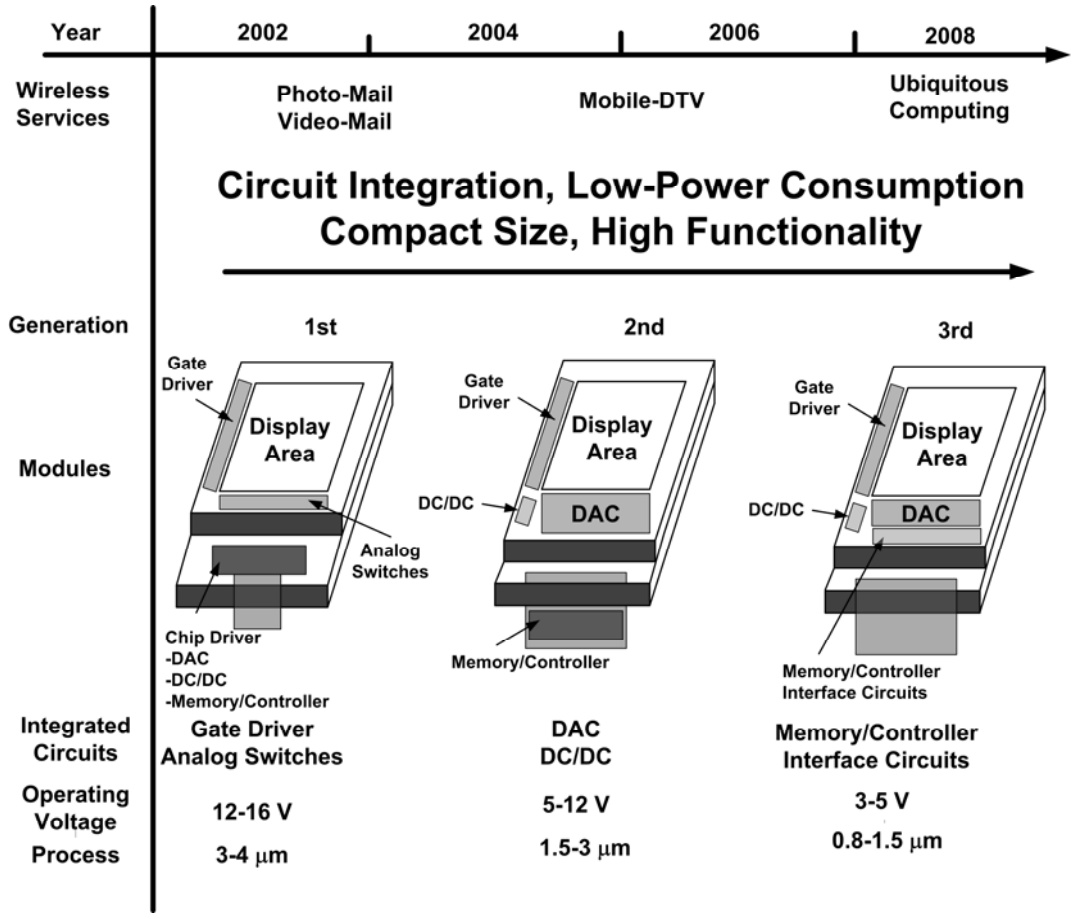


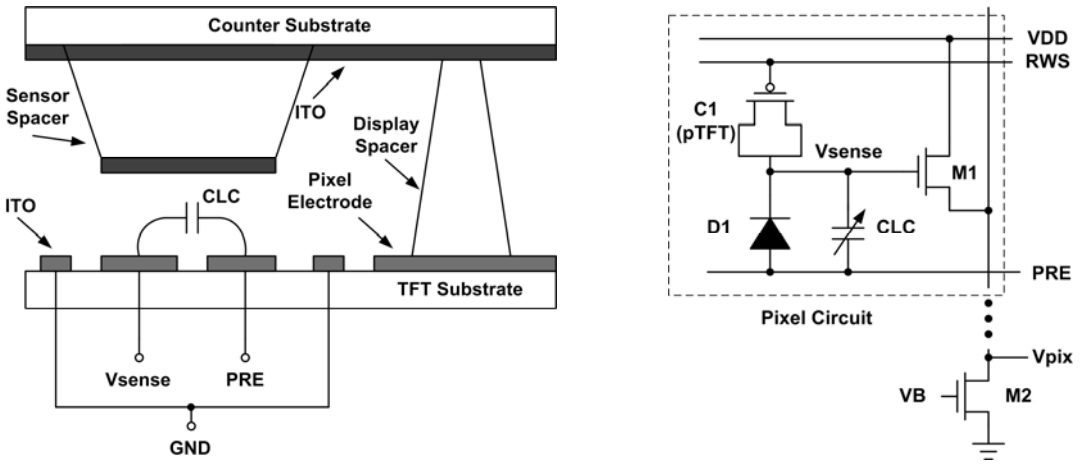
Fig. 5.1. Trends in mobile system-on-panel liquid crystal displays [84].

Many researches had been reported for integration of peripheral functional circuits and there were some other improvement for SOP applications [90]-[92]. The first RF frequency

divider on glass substrate was reported in [90]. The single-stage ring oscillator was developed with additional cross-coupled transistor pair to increase the phase shift and the operating frequency was extended from 60 Hz to 18 MHz. The locking range of the frequency divider is 2 MHz and the overall operation frequency is from 120 Hz to 8 MHz. In [91], a phase-locked loop (PLL) with self-calibrated charge pumps (CPs) was proposed in a 3-μm LTPS TFT technology with maximal locked time of 1.75 ms. A voltage scaler and self-calibrated CPs were used to reduce the static phase error, reference spur, and jitter of LTPS-TFT PLL. In addition to the SOP applications on integration of radio frequency (RF) circuits, an integrated ambient light sensor fabricated with LTPS technology was also developed on a display panel [92]. Backlight noise elimination, large photo sensing area, high ambient light transmittance, and good flexibility in circuit integration with a vertical stacking structure were achieved by the photo sensor with nano-crystalline silicon buried in an SRO file sandwiched between the bottom metal and top ITO electrodes.

Recently, touch panels have gained significant interest and market penetration with its intuitive operation and advantages of easier and faster entry of the information for electronic devices as PDA, tabled PCs, and smart phones [93]. Capacitive-type touch panels have been widely adopted in high-end mobile applications due to the capability of multi- and soft-touch with higher durability and light transmittance over resistive-type touch panels. Furthermore, there is a desire to integrate touch-screen panel, readout circuits, and other function blocks for touch panel to reduce system cost and achieve SOP applications [94]-[96].

In [93], a novel pixel circuit for an in-cell capacitive type force-sensitivity touch panel is presented. Fig. 5.2 (a) shows the structure of planar type sensor capacitor which both electrodes are formed in the ITO layer of the TFT substrate. A protrusion is fabricated on the counter substrate opposite electrodes to improve the sensor response, which is to increase the relative change in capacitance to cell-gap deformation. A key advantage of this structure is the isolation between the sensor and display operation. Fig. 5.2 (b) shows the sensor pixel circuit schematic diagram. The pixel circuit is composed of an amplifier transistor, M1, a liquid crystal sensor capacitor, CLC, a read-out capacitor, C1 (which is formed by a voltage-dependent integration capacitor), and a DC biasing diode, D1. The voltage of sensing node, Vsense, rises as the touch event happened, to turn M1 on and forming a source follower amplifier with the bias transistor, M2. The output voltage generated by the source follower amplifier, Vpix, is sampled and held by the sensor column readout circuits.



(a) (b)

Fig. 5.2. (a) Structure of planar type sensor capacitor and (b) the sensor pixel circuit schematic diagram [93].

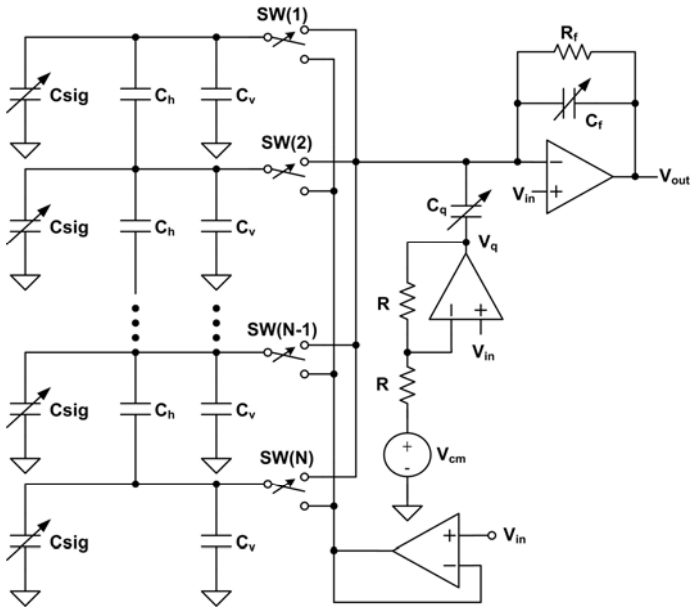


Fig. 5.3. The schematic diagram of charge amplifier and compensation circuits [94].

Fig. 5.3 shows the schematic diagram of charge amplifier and compensation circuits utilized in a mobile-display-driver IC embedding a capacitive touch-screen controller system [94]. The charge amplifier measures the capacitances of the sensing line that are composed of signal component (Csig), horizontal- (C_h), and vertical-parasitic (C_v) capacitances and the signal component is the overlapped capacitance between the sensing line and the finger. However, the parasitic capacitance results in a reduced dynamic range allocated to the signal

component, which means the sensitivity is also reduced in the sensor. In order to overcome this issue, a single charge amplifier is connected to each sensing line one by one using a switch array [97]. To further reduce the effect of horizontal parasitic capacitance, the voltage across the C_h is designed to 0 when a sensing line is connected to the charge amplifier. To reduce the effect of vertical parasitic capacitance, a compensation capacitor and a compensation pulse (V_q) are utilized to make output voltage (V_{out}) independent of the C_v. Since the effect of horizontal/vertical-parasitic capacitances are eliminated, the output voltage can be derived:

$$\frac{V_{out}}{V_{in}}(s)=\frac{1+sR_f\left(C_f+Csig\right)}{1+sR_fC_f}. \tag{5.1}$$

In [95], an innovative design of touch panel embedded in LCD which includes a capacitive type touch panel and integrated color sequence display (CSD) is proposed to achieve higher transparency, lower interference, higher yield and improved touch sensitivity compared with that of the conventional one. Furthermore, the new structure is also coated thin films on single side for external touch panel so the structure can be produced flexibly depends on customer's demand. Fig. 5.4 shows the novel design structure for internal touch display. Both X and Y sensor are coated on the same layer and the material of black matrix is changed from resin to metal to be a shielding layer to avoid interferences from LCD (VCOM and Data) [95].

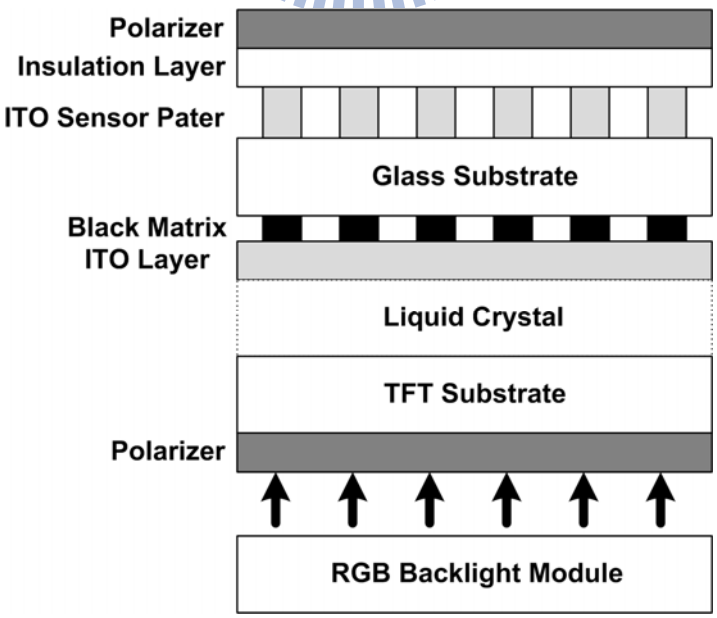


Fig. 5.4. Novel design structure for internal touch display [95].

Because the degraded sensitivity in large panel with high loop impedance, the applications of projective capacitive touch panels are limited only to small glass-based display devices. The resistance of the sensing electrode, such as indium tin oxide (ITO), must be reduced to increase the capability of implementation for large-area flexible display with touch-sensing [96]. Fig. 5.5 shows the cross-section schematic of a touch sensing film. The film thickness is only 20 μm and transmittance is more than 90%. The touch sensitivity is not degraded after bending under 2 cm curvature radius for more than 5000 times. The sheet resistance of transparent conductive oxide layer is less than 20 Ω/□. The ultra-thin colorless PI substrate, which has higher transition temperature and higher chemical resistance to enable high-temperature ITO deposition with low sheer resistance, is coated on glass with de-bounding layer. The transparent sensing electrode, ITO, is sputter-deposited at room temperature and patterned by oxalic acid. All the process temperatures of the ultra-thin touch panels is kept under 220°C [96].

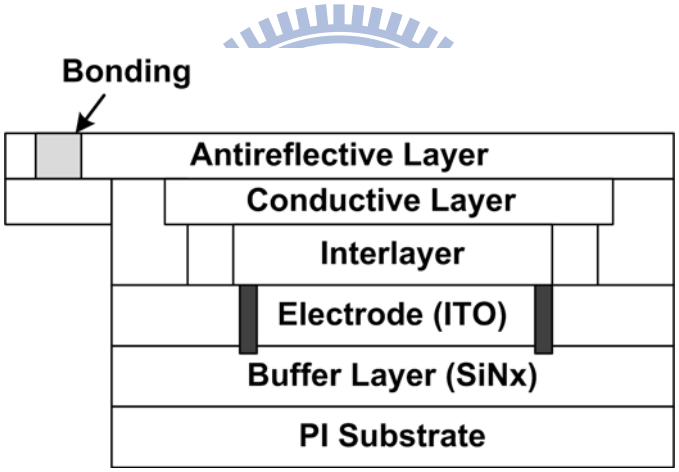


Fig. 5.5. Cross-section schematic of a touch sensing film [94].

In this work, a new readout circuit on glass substrate for touch panel application has been designed and simulated in a 3-μm low temperature poly-silicon (LTPS) technology. Fig. 5.6 shows the block diagram of touch panel system. There are totally 14 and 8 capacitive sensor lines in the x- and y-direction respectively on the touch panel. When the touch panel is touched, the total capacitance of the capacitive sensor line will be changed. The voltage difference from capacitance change due to the touch event on panel is converted to current by transconductance amplifier. By charging and discharging the capacitor in the counter, the counter displays different digital output codes under touch or non-touch event. The digital

output codes from the counter are stored in digital correction circuit periodically and not only the touch or non-touch event can be distinguished by digital output codes of digital correction circuit but also the effect of process variation can be compensated. Finally, by analyzing the digital output codes, the corresponding functions, such as zoom in, zoom out, move, and so on, can be performed on the touch panel by the appropriate algorithm of software in the system.

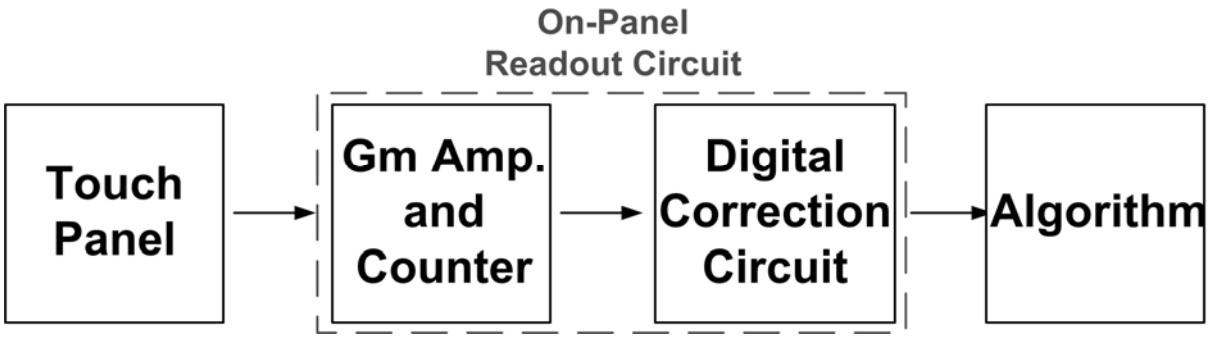


Fig. 5.6. The block diagram of touch panel system.

5.2 Methodology for Correction of Analog Circuits

In practical implementation of analog circuits, physical parameters (e.g. oxide thickness, physical dimensions, doping profile) are subject to variations due to instabilities of the fabrication technology. The achievable tolerance of individual component values thus depends on the accuracy of the manufacturing process, and cannot be totally reduced. However, analog circuit design rarely relies on the absolute value of single physical components, but rather on relative values of several components. The relative values can be achieved by utilizing appropriate design techniques, which are discussed in this section, so high-precision circuits can be realized even with poor manufacturing processes [98].

The most common technique for improving the precision of analog blocks is matching. The following rules should be applied for optimum matching of integrated components: same structure, same temperature, same shape, same size, minimum distance, common-centroid geometries, same orientation, same surroundings, and non-minimum size. Mismatch of active and passive devices represents a major limitation to the accuracy of analog circuits. It can be minimized by respecting a set of basic rules. Designs must be based on sound concepts that take maximum advantage of all available components [99].

Operational amplifier is one of the most important components in analog circuit design and it suffers many imperfections such as flicker noise, offset, and so on at low frequency or

even DC. The idea of chopper stabilization is to transpose the signal to a higher frequency to eliminate these effects, to amplify the modulated signal, and finally to demodulate the amplified signal back to the baseband [100], [101]. Fig. 5.7 shows the functional schematic of a chopper amplifier [98]. A modulation signal m(t) periodically changes the polarity of the input signal Vin and the equivalent input offset (V_{offset}) and noise (V_{noise}) are applied to ideal amplifier block (A). The amplified signal is demodulated by sign changes using the same signal as for input modulation, resulting in the system output Vout. Therefore, Vout is correctly presented in the base band but the higher frequency component should be removed with additional low-pass filer.

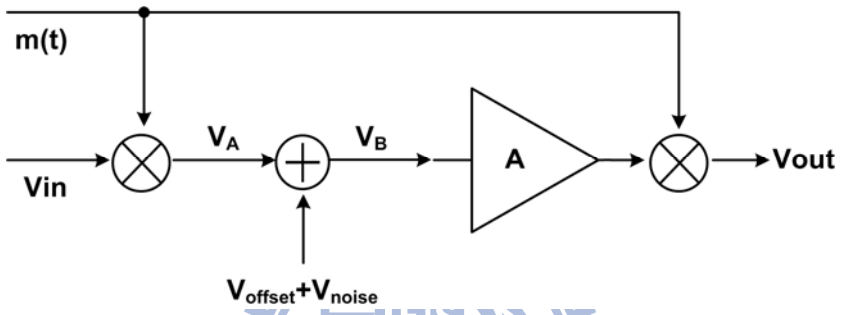


Fig. 5.7. Functional schematic of a chopper amplifier [98].

Autozero is another common technique used to minimize offset and flicker noise in amplifiers. The main idea is to first sample the undesired effect and then to subtract it during the second phase when the input signal is processed by the imperfect amplifier [45]. Fig. 5.8 shows the principle of autozero amplifier in (a) sampling phase and (b) processing phase [101]. The amplifier with gain A is ideal and the noise (V_N) and offset (V_o) of the amplifier is represented by the voltage source connected to the positive input. During the sampling phase, the amplifier is disconnected from the input signal by switch S_{in}, and $V_N + V_o$ are sampled on capacitor C_{AZ} across switch S_{FB}:

$$V_C = \frac{A}{1+A}(V_o + V_N). \tag{5.2}$$

During the processing phase, the amplifier is used in its normal processing configuration. The autozero capacitor is connected so that it cancels the effect of the parasitic voltage source.

Correlated double sampling (CDS) is similar to the autozero technique as mentioned above. With autozero, the noise is first sampled, and then the amplifier performs continuous-time output, subtracting the sampled noise value. However, in the second phase of

CDS, it samples signal and the subtraction of two sampled values allows removing the offset and noise from the signal. The first application of CDS was in CCD sensors, but the same technique can be utilized in any sampled signal processing system [102].

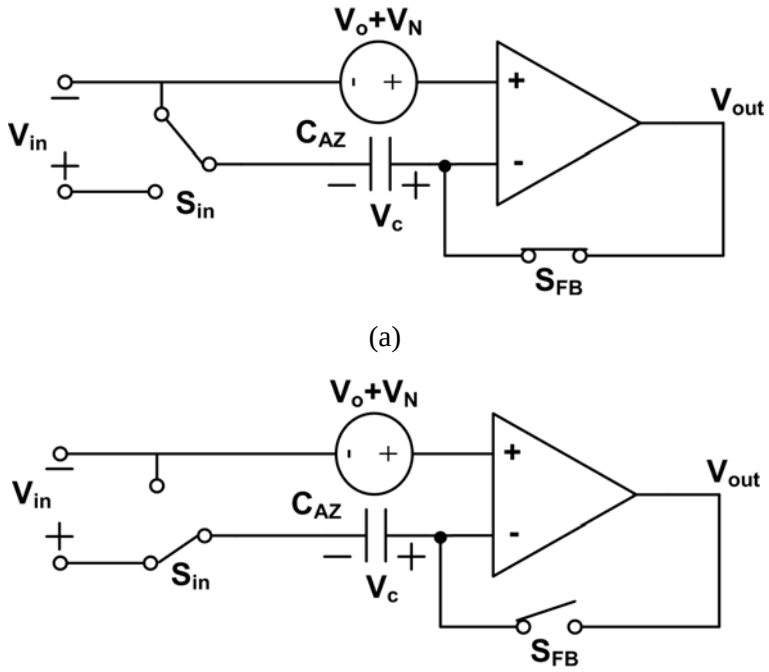


Fig. 5.8. The principle of autozero amplifier in (a) sampling phase and (b) processing phase [99].

The aforementioned compensation and correction techniques put the emphasis on most widespread solutions for calibrating analog circuits. Furthermore, there are many other systems, like digital-to-analog and analog-to-digital converters, where specific techniques are used for improving performance of analog circuits. In this work, the digital correction circuit is composed two registers, which are utilized to store the digital output of counter periodically, and exclusive-or (XOR) gate, which is to compare the output of two registers. The touch or non-touch event can be further distinguished by output of XOR gate.

5.3 On-Panel Readout Circuit with Digital Correction for Touch Panel Application

5.3.1. Equivalent Model of the Capacitive Sensor Line

Fig. 4.5 shows the equivalent RC model of one capacitive sensor line on a 2.8 inch touch

panel provided by the panel manufactory with total R of 150 kΩ and C of 100 pF. The Fanout block is the equivalent parasitic RC network of the interconnect line between the sensor line to the output node Fin. The touch capacitor (C_touch) is varied from 0.5 pF to 2 pF according to the different touch area. When the sensor line is touched by the finger, C_touch is added in parallel to the touched node and the total capacitance on the capacitive sensor line is also changed. Multi-touch events can be further determined by analyzing both digital outputs of readout circuits in the x- and y-direction through the appropriate algorithm of software in the system. In order to discriminate between the touch and non-touch events, that are to detect the capacitance change from C_touch, each node on the sensor line is pre-charged to 10 V at the beginning. When the touch event happened, the voltage at the output node Fin (V_{Fin}) will be changed to

$$V_{FIN} = \frac{C_{total}}{C_{total} + C\_touch} \cdot V_{pre-charge}, \tag{5.3}$$

where $V_{pre\text{-}charge}$ = 10 V, C_{total} = 100 pF, C_touch = 0.5 pF - 2 pF. Therefore, the voltage level at output node Fin under the touch event can be derived from 9.8 V to 9.95 V with the corresponding C_touch value from 2 pF to 0.5 pF. For such a capacitive sensor line, the capacitance change due to the touch event can be indicated by the voltage change. So the on-panel readout circuit is designed to distinguish the voltage difference at the Fin node.

5.3.2. Design Consideration and Circuit Implementation

From chapter 4, a new on-panel readout circuit with SC and CDS techniques for touch panel applications has been designed and fabricated in a 3-μm LTPS technology. However, with design consideration aforementioned in chapter 1.4, the device characteristic variations in LTPS technology are quite larger compared with CMOS technology, so the effect of device variation must be considered for on-panel circuit design. Although SC and CDS techniques result in the higher performance for on-panel readout circuit, the complexity of such circuit is still too high for implementation in LTPS process. In this chapter, new on-panel readout with digital correction for touch panel is proposed. The proposed circuit is composed of larger digital part, smaller analog part, and digital correction circuit, so it can be realized more easily and successively compared with that in chapter 4 in LTPS process.

Fig. 5.9 shows the new proposed on-panel readout circuit with digital correction for touch panel applications in a 3-μm LTPS technology. The proposed circuit is composed of three parts: transconductance amplifier (Gm. Amp.), counter, and digital correction circuit. The

gate of Gm amplifier is connected to Fin node of one capacitive sensor line shown in Fig. 4.5. In the i_{th} sensor line, the voltage variance at Fin node is converted to different current (I_{Fin_i}) by Gm amplifier as the touch event happened. By charging the capacitor in counter (C_c), the voltage of capacitor (V_c) rises as well as 7-bit counter starts to count. The Schmitt trigger is utilized to control the charge or discharge of C_c by MS1 and MS2, and the output of Schmitt trigger (SM1) is used as the reset signal of 7-bit counter and the clock signal of 1-bit counter. As V_c reaches to the higher threshold voltage of Schmitt trigger, MS2 is turned on as well as MS1 is turned off. The 7-bit counter stops counting and V_c is decreased. When V_c reaches to the lower threshold voltage of Schmitt trigger, MS2 is turned off as well as MS1 is turned on. The 7-bit counter starts counting again and V_c is increased. Since the current of Gm amplifier (I_{Fin_i}) is different due to touch or non-touch event, the charging/discharging time of V_c is also different, which means that the 7-bit counter shows different output (A6-A0) under touch or non-touch event. However, even under the same touch or non-touch event, 7-bit counter in different sensor line show various output due to the process variation of LTPS technology. The digital correction circuit is necessary to overcome this issue.

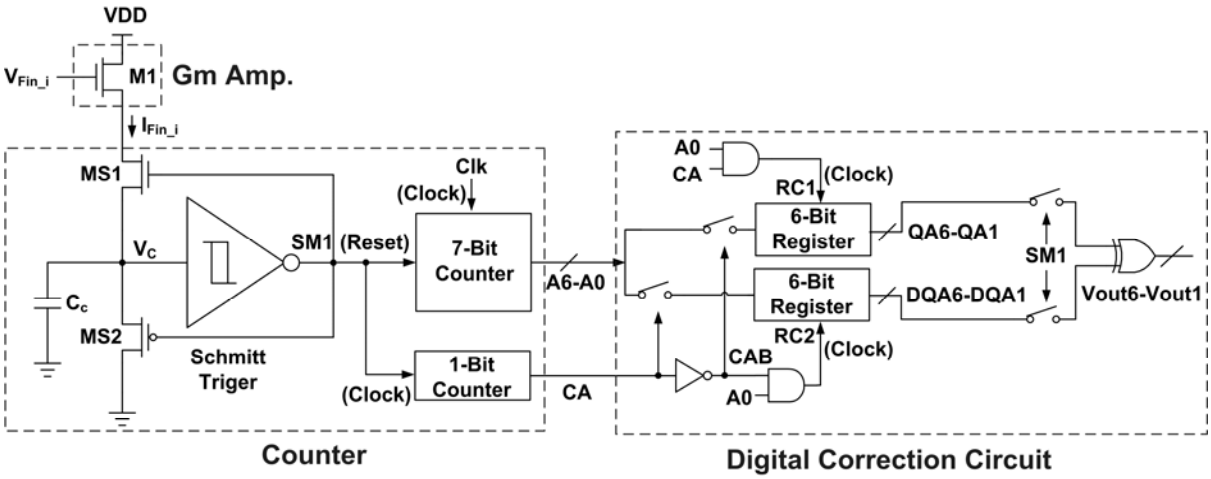
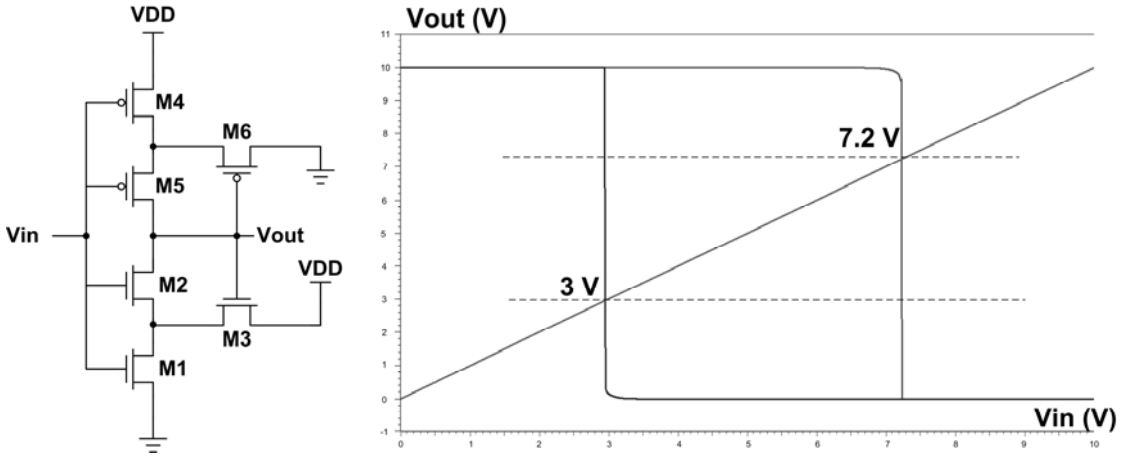


Fig. 5.9. New proposed on-panel readout circuit with digital correction to sense the voltage change due to the capacitance change on the touch panel in a 3-μm LTPS technology.

In digital correction circuit, two 6-bit registers are utilized to store the output from 7-bit counter (A6-A1) periodically according to the output of 1-bit counter (CA). The least significant bit of 7-bit counter (A0) is combined with CA by logical operation to perform the clock of two 6-bit registers so the proposed circuit needs only one external clock signal, which is applied to 7-bit counter. After that, the outputs of two 6-bit registers (QA6-QA1 and

DQA6-DQA1) are compared by XOR gate as SM1 is in low logic level. Some of the output for XOR gate show logic high when the touch event happened as well as the logic low is displayed for all output of XOR gate under non-touch event. Even if 7-bit counter in different sensor line show various output due to the process variation of LTPS technology, the digital correction circuit can compensate the effect of process variation by storing output from 7-bit counter (A6-A1) periodically and comparing the outputs of two 6-bit registers (QA6-QA1 and DQA6-DQA1) by XOR gate. The number of bit for counter and registers are depended on the resolution and operating frequency required by the specification of touch panel applications.

Fig. 5.10 shows (a) the schematic of Schmitt trigger and (b) its simulated results under 10-V supply voltage. The hysteresis characteristic raises the switching point when the input is low and lowers the switching point when the input is high. The higher threshold voltage and lower threshold voltage of Schmitt trigger are 7.2 V and 3 V, respectively. Fig. 5.11 shows the D-type positive-edge-trigger flip-flop, which is utilized for counters and registers in the proposed circuit, with its schematic, graphic symbol, and characteristic table [103]. Two latched respond to the external D (data) and Clock inputs and the third latch provides the outputs for the flip-flop. In addition, one additional reset signal (Reset) is applied. When Reset = '0', the D-type positive-edge-trigger flip-flop is reset, that is, Q = '0' whether D = '1' or '0'. Fig. 5.12 shows the schematic of (a) N-bit counter and (b) N-bit register, which are implemented with D-type positive-edge-trigger flip-flop shown in Fig. 5.12.



(a) (b)

Fig. 5.10. (a) The schematic of Schmitt trigger and (b) its simulated results.

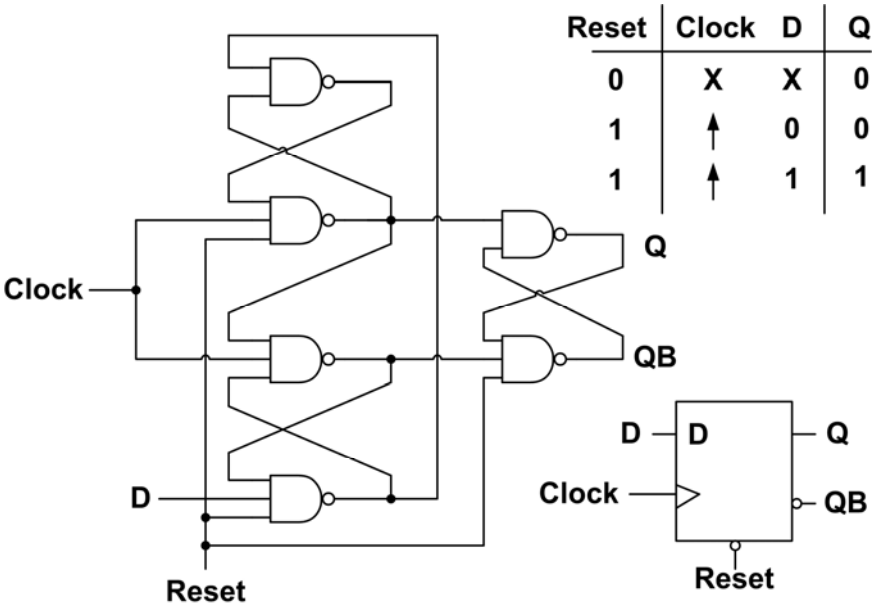


Fig. 5.11. The D-type positive-edge-trigger flip-flop with its schematic, graphic symbol, and characteristic table [103].

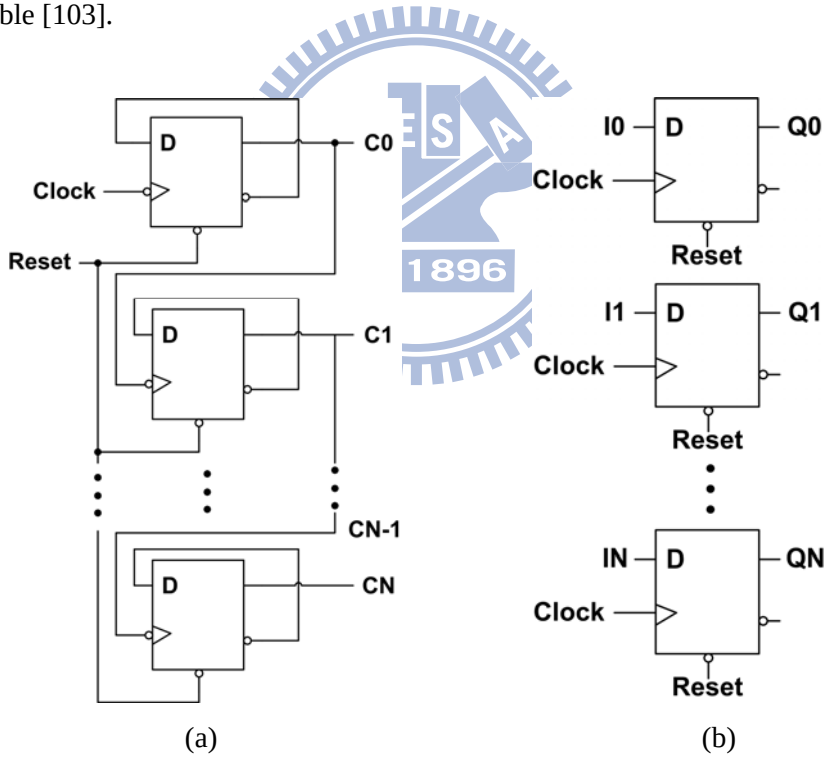


Fig. 5.12. The schematic of (a) N-bit counter and (b) N-bit register.

5.3.3. Simulated Results of the Proposed Circuit

The proposed circuit has been designed and simultaed by the Eldo software with the RPI model (Level=62) in a 3-μm LTPS process [82]. Fig. 5.13 shows the simulated output of 7-bit

counter in the proposed circuit under non-touch event (V_{Fin_i} = 10V) with VDD = 10 V, MS1 = MS2 = 4 μm/20 μm, C_c = 10 pF, and Clk = 10 MHz. V_c is increasing and decreasing according to the higher threshold voltage and lower threshold voltage of Schmitt trigger and the counter is reset as SM1 = '0'. The simulated output of (a) the top 6-bit register and (b) the bottom 6-bit register in the proposed circuit under non-touch event (V_{Fin_i} = 10V) is shown in Fig. 5.14. In Fig. 5.14, the output of 7-bit counter is stored separately in two 6-bit register periodically, and each output of two 6-bit registers is held as the other one is storing the output of 7-bit counter. By applying the XOR gate to compare the outputs of two 6-bit registers, each output of XOR gate displays logic low under the non-touch event. Therefore, Fig. 5.15 shows the simulated results of the proposed circuit under non-touch event (V_{Fin_i} = 10V) with all digital outputs are '0'.

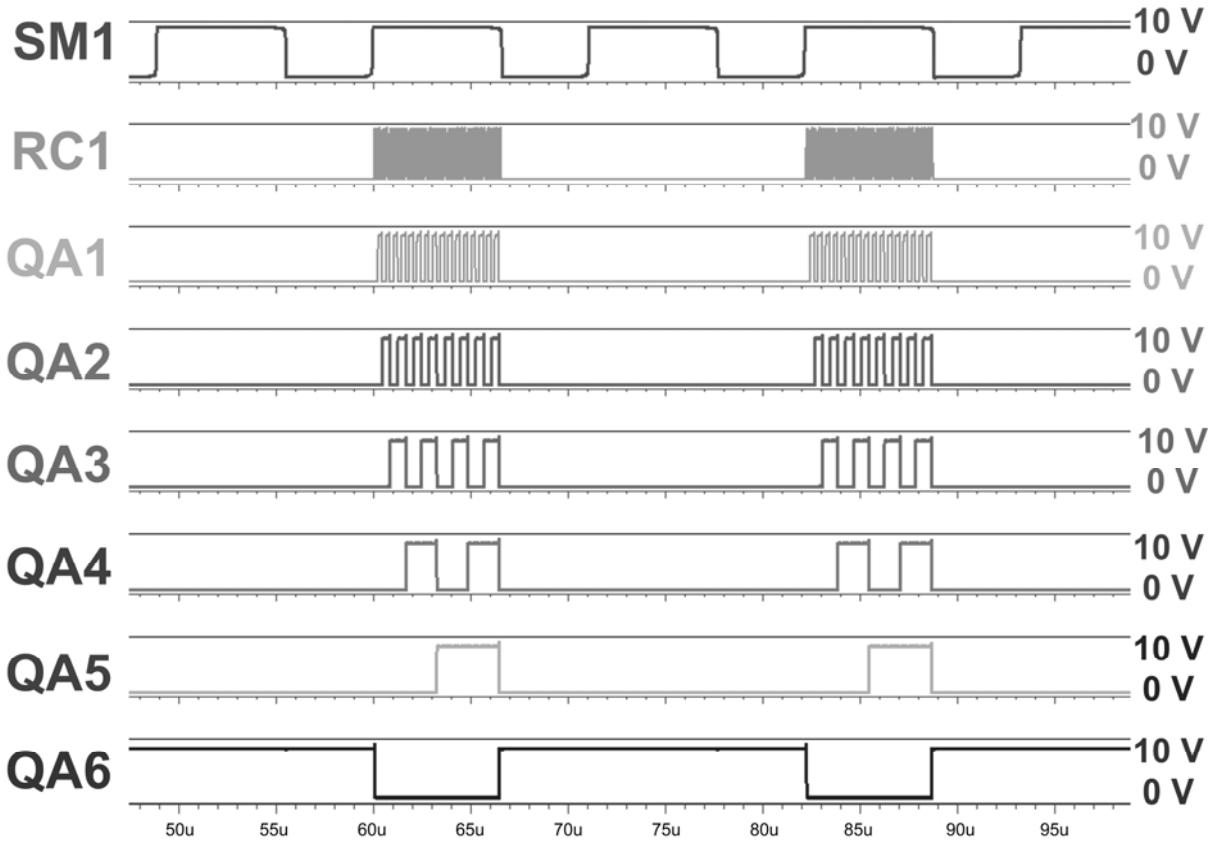
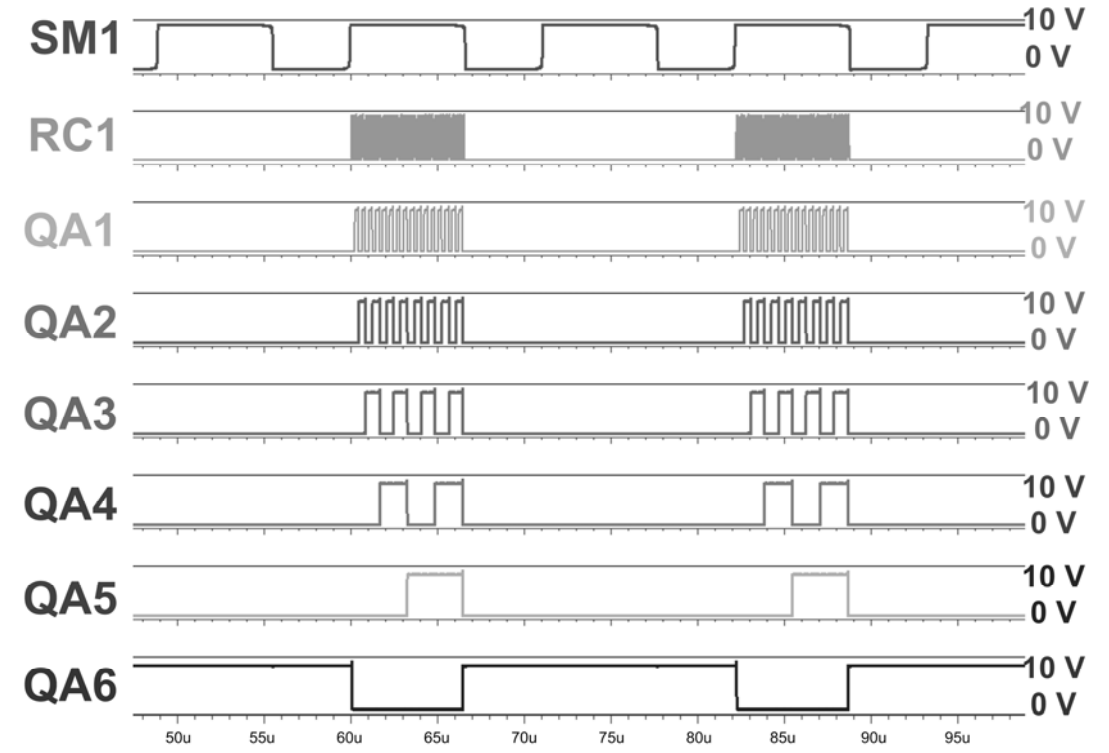
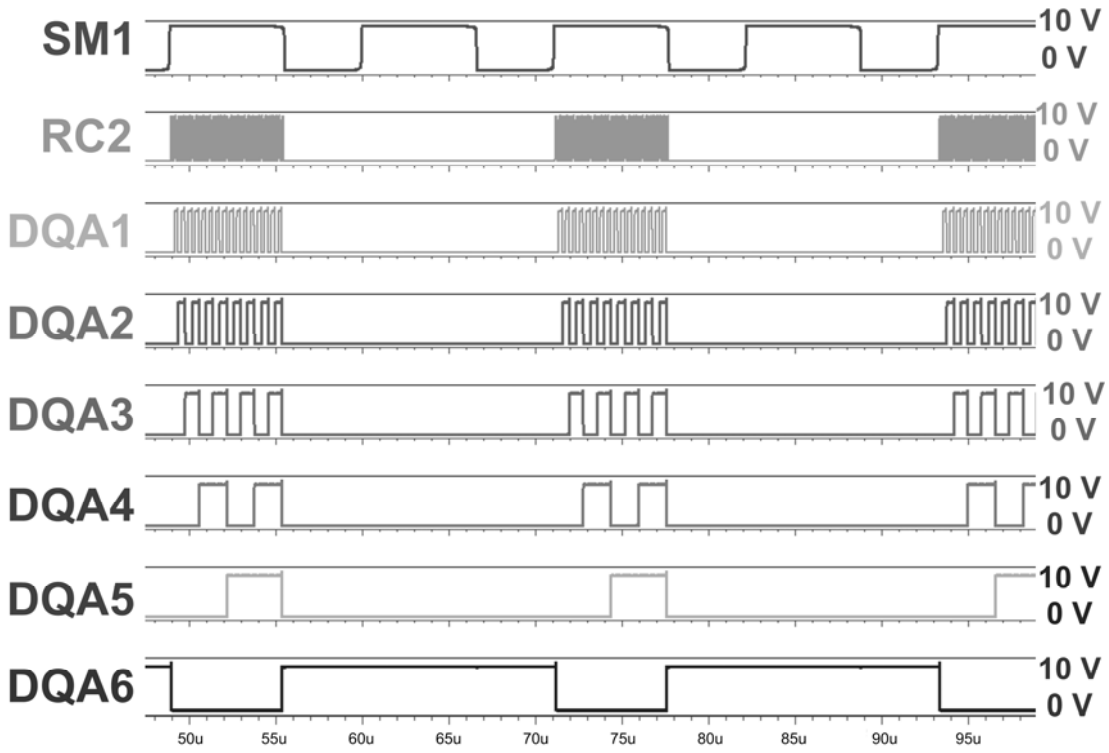


Fig. 5.13. The simulated output of 7-bit counter in the proposed circuit under non-touch event (V_{Fin_i} = 10V).



(a)



(b)

Fig. 5.14. The simulated output of (a) the top 6-bit register and (b) the bottom 6-bit register in the proposed circuit under non-touch event (V_{Fin_i} = 10V).

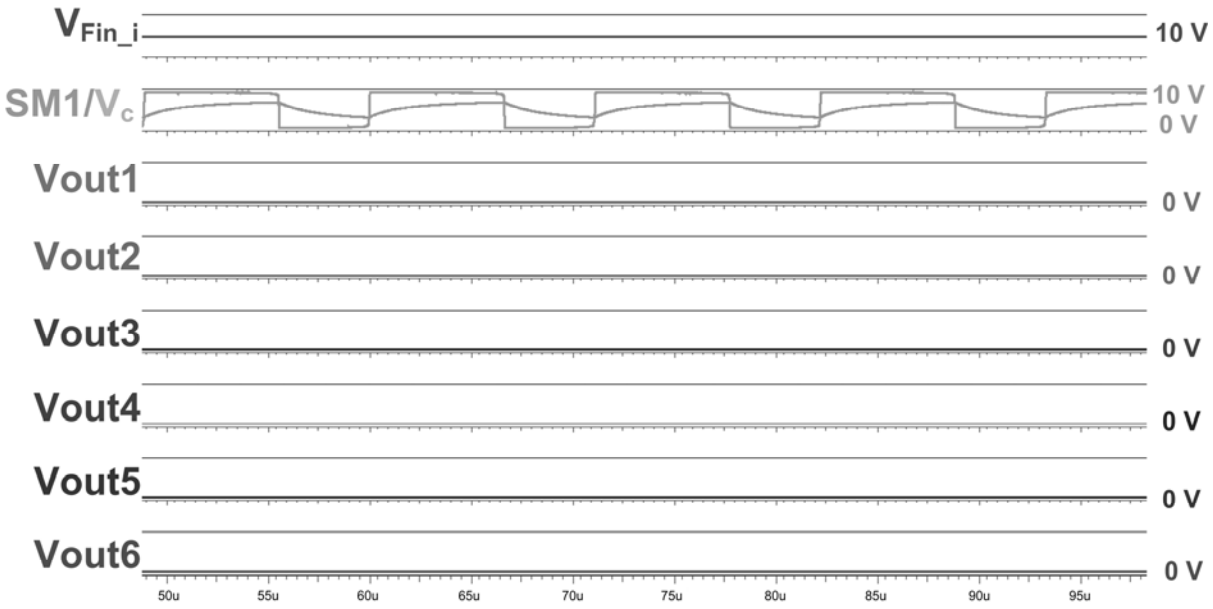
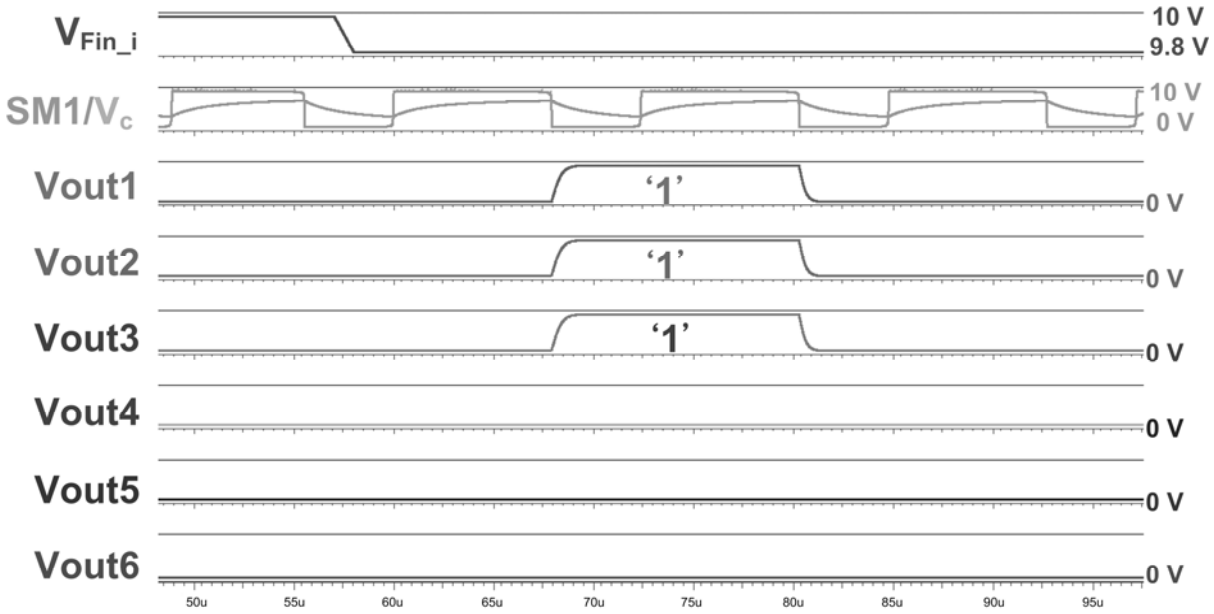


Fig. 5.15. The simulated results of the proposed circuit under non-touch event (V_{Fin_i} = 10V) with all digital outputs are '0'.

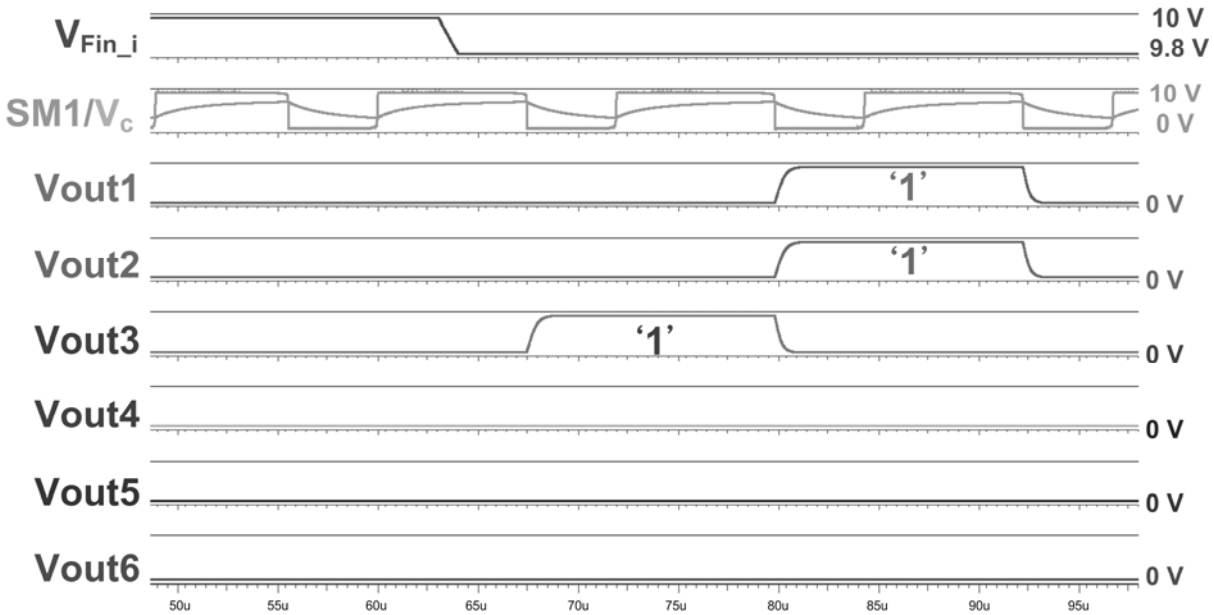
Fig. 5.16 shows the simulated results of the proposed circuit under 2-pF touch event (V_{Fin_i} = 9.8 V) with some digital outputs are '1' in (a) SM1 = '0' and (b) SM1 = '1'. Since the output of 7-bit counter is stored separately in two 6-bit register periodically, some outputs of XOR gate show '1' right after the touch event happened and each output of XOR gate still displays logic low before the touch event happened and after some outputs of XOR gate showing '1'. Furthermore, the period for some outputs of XOR gate showing '1' may be different under different touching time, that is, when SM1 = '0' and SM1 = '1' because the effect of variant charging time on C_c results in different output of 7-bit counter. Fig. 5.17 shows the simulated results of the proposed circuit under 0.5-pF touch event (V_{Fin_i} = 9.95 V) with some digital outputs are '1' in (a) SM1 = '0' and (b) SM1 = '1'.

In order to consider the influence of process variation from LTPS technology on the proposed circuit, the 20% threshold voltage variation of pTFT and nTFT are also simulated in a 3-μm LTPS technology. Fig. 5.18 shows the simulated results of the proposed readout circuit with (a) 2-pF touch event (V_{Fin_i} = 9.8 V) under +20% threshold voltage variation, (b) 2-pF touch event (V_{Fin_i} = 9.8 V) under -20% threshold voltage variation, (c) 0.5-pF touch event (V_{Fin_i} = 9.95 V) under +20% threshold voltage variation, and (d) 0.5-pF touch event (V_{Fin_i} = 9.95 V) under -20% threshold voltage variation. According to the simulated results, the proposed readout circuit on glass substrate with digital correction can not only distinguish

the touch or non-touch event but also can compensate the influence of process variation by digital correction circuit.

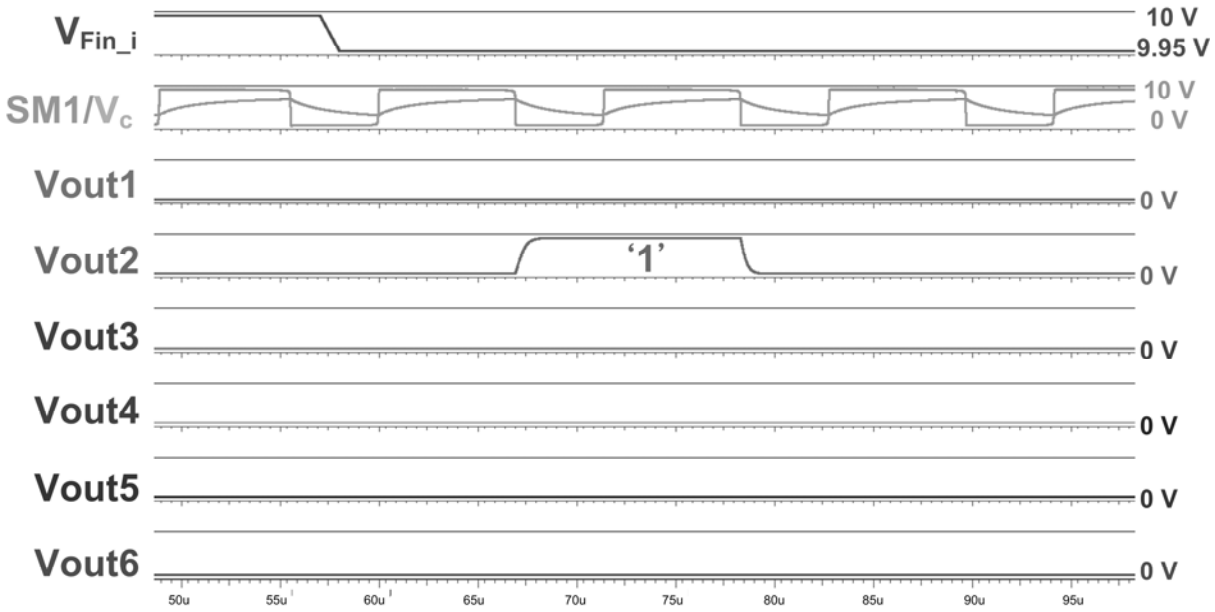


(a)

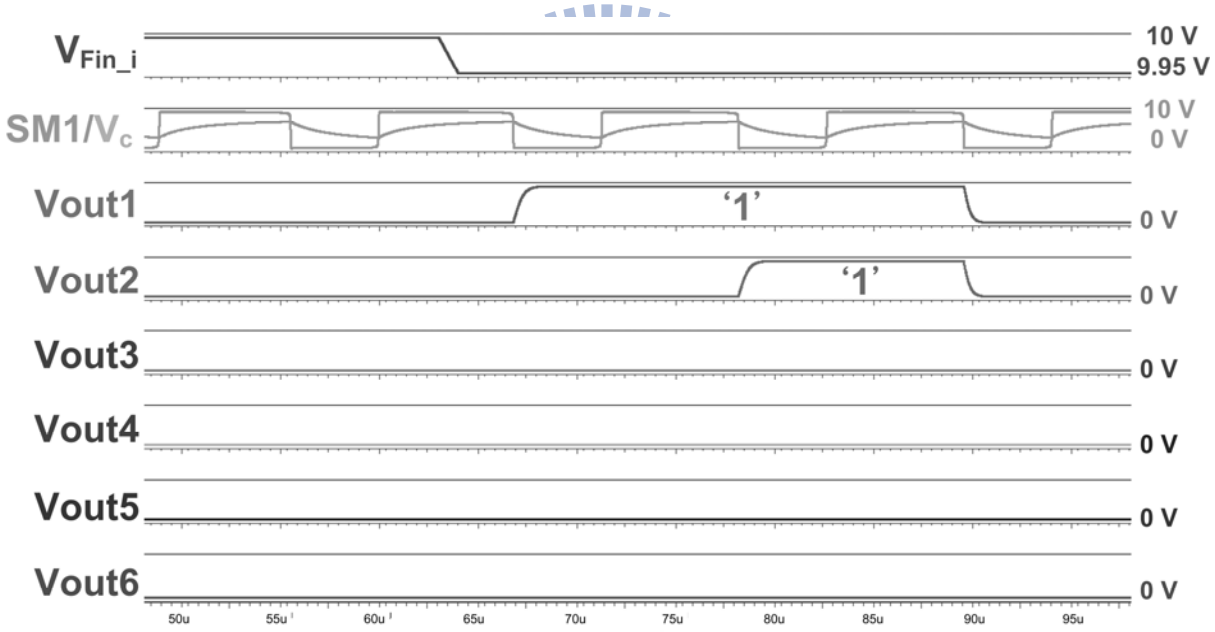


(b)

Fig. 5.16. The simulated results of the proposed circuit under 2-pF touch event (V_{Fin_i} = 9.8 V) with some digital outputs are '1' in (a) SM1 = '0' and (b) SM1 = '1'.



(a)



(b)

Fig. 5.17. The simulated results of the proposed circuit under 0.5-pF touch event (V_{Fin_i} = 9.95 V) with some digital outputs are '1' in (a) SM1 = '0' and (b) SM1 = '1'.

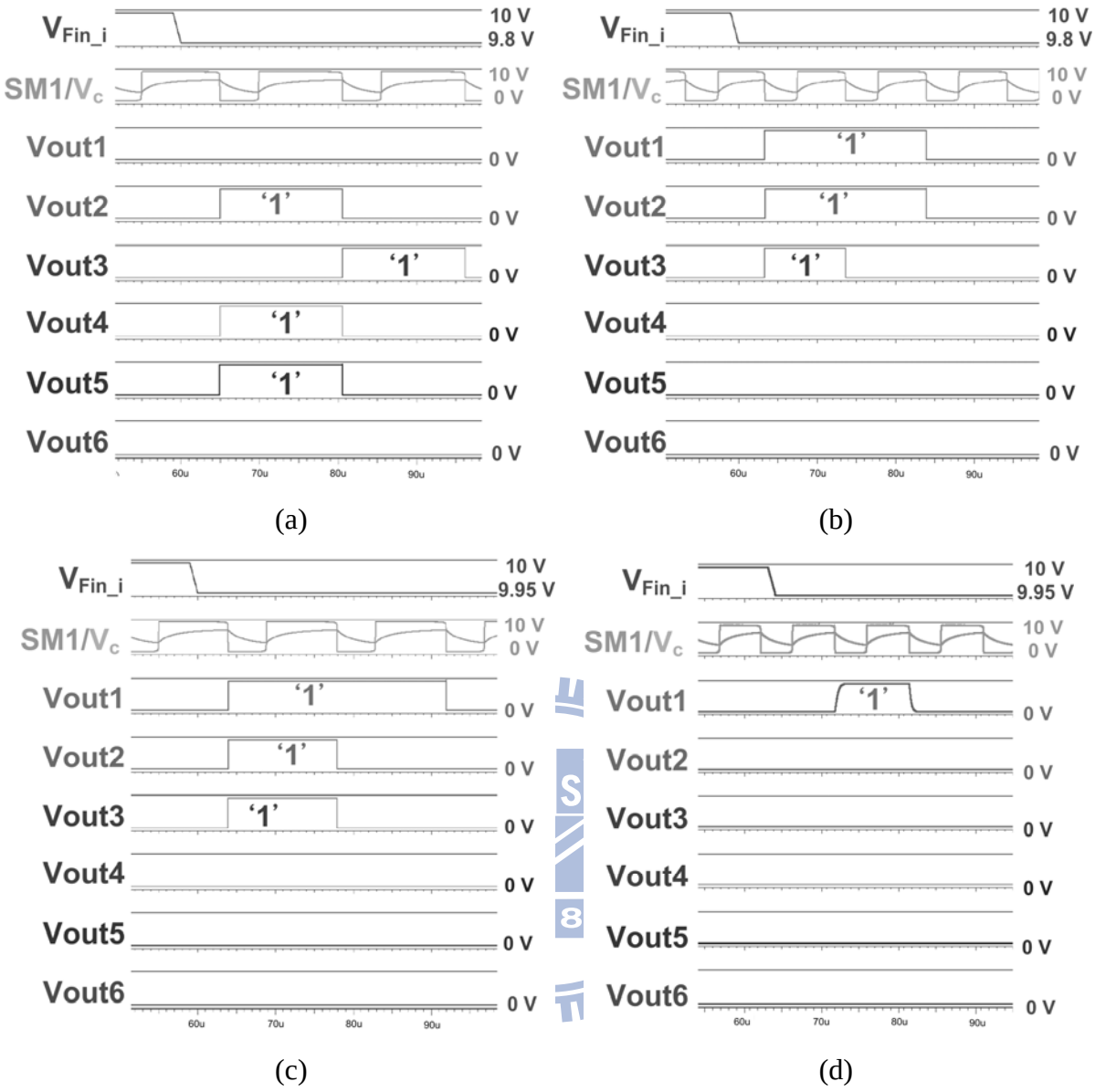


Fig. 5.18. The simulated results of the proposed readout circuit with (a) 2-pF touch event (V_{Fin_i} = 9.8 V) under +20% threshold voltage variation, (b) 2-pF touch event (V_{Fin_i} = 9.8 V) under -20% threshold voltage variation, (c) 0.5-pF touch event (V_{Fin_i} = 9.95 V) under +20% threshold voltage variation, and (d) 0.5-pF touch event (V_{Fin_i} = 9.95 V) under -20% threshold voltage variation.

The layout of the proposed circuit is illustrated in Fig. 5.19 in a 3-μm LTPS technology with the area of 1030 μm x 2410 μm. The proposed circuit is composed of Gm amplifier, Schmitt trigger, 1-bit counter, 7-bit counter, two 6-bit registers, and one XOR gate. The fabricated chip to verify this design is now under wafer fabrication. The measured results in glass chip will be shown in the future. Table I shows the performance comparison among [70] and this work. The proposed circuit in this work is composed of larger digital part, smaller

analog part, and digital correction circuit, so it can be realized more easily and successively compared with that in chapter 4 in LTPS process. The proposed circuit in the prior art consumes larger power consumption due to the compensation period for on-panel ADC but it also shows smaller area. The correction technique of correlated double sampling (CDS) is applied in [70] as well as the digital correction circuit is applied in the proposed circuit to compensate the device variation from LTPS process. Since there is larger digital part in the proposed circuit, the complexity of prior art is higher than that of the proposed circuit.

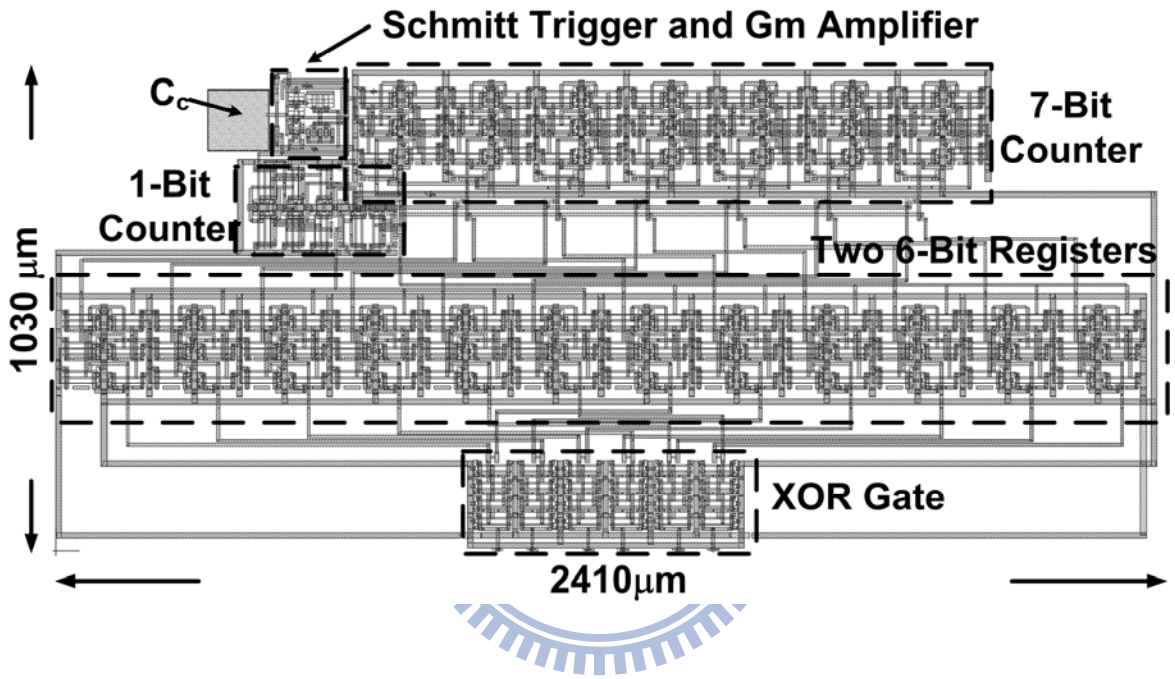


Fig. 5.19. The layout of the proposed circuit in a 3-μm LTPS technology.

TABLE 5.1

PERFORMANCES COMPARISON AMONG THIS WORK AND PRIOR ART

	Chap. 4	This work
Detection Range	0.5 pF ~ 2 pF	
Complexity	High	Low
Avg. Current Consumption	13.9 mA	0.44 mA
Detection Time	10 μs	20-30 μs
Area	980 μm x 630 μm	1030 μm x 2410 μm
Compensation Technique	CDS	Digital

5.4 Summary

With design consideration in chapter 1.4, the proposed circuit in this chapter is composed of larger digital part, smaller analog part, and digital correction circuit, so it can be realized more easily and successively compared with that in chapter 4 in LTPS process. In chapter 4, a new on-panel readout circuit with SC and CDS techniques for touch panel applications has been designed and fabricated in a 3-μm LTPS technology. Although SC and CDS techniques result in the higher performance for on-panel readout circuit, the complexity of such circuit is still too high for implementation in LTPS process.

In this chapter, a readout circuit on glass substrate with digital correction for touch panel application, which contains Gm amplifier, counter, and digital correction circuit, has been designed and simulated in a 3-μm low temperature poly-silicon (LTPS) technology. In this work, the voltage difference from capacitance change due to the touch event on panel is converted to current by Gm amplifier. By charging and discharging the capacitor in the counter, the counter displays different digital output codes according to touch or non-touch event. According to the simulated results, the proposed readout circuit on glass substrate with digital correction can not only distinguish the touch or non-touch event but also can compensate the influence of process variation by digital correction circuit.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Chapter 6

Conclusions and Future Works

This chapter summarizes the main results and contributions of this dissertation. Suggestions for future research topics in the fields of on-panel analog circuits design in low temperature poly-silicon for display panel applications are also provided in this chapter.

6.1 Main Results of This Dissertation

In this dissertation, some on-panel analog circuits have been designed and implemented in LTPS process for display panel applications. With design consideration in chapter 1.4, the functionality and performance of the proposed circuits in this dissertation have been demonstrated by simulated and measured results of the fabricated test chips. The achievements of this dissertation have been published or submitted to international journal and conference papers. The research topics of this dissertation including: (1) a 6-bit folded R-string DAC with gamma correction on glass substrate, (2) two analog output buffers with level shifting function containing the DAC circuit with gamma correction, (3) a readout circuit on glass substrate for touch panel application, and (4) a readout circuit with digital correction on glass substrate for touch panel application in 3-μm LTPS process.

In chapter 2, compared with DAC circuits implemented in CMOS process for LCD column driver, the proposed circuit shows worse performance than that of some traditional architectures of aforementioned DAC. The reason is the devices suffer worse electrical characteristic and larger variation in LTPS technology compared with that in CMOS technology. With consideration of the complexity and the implementable ability, a 6-bit folded R-string DAC with gamma correction on glass substrate has been successfully designed and verified in 3-μm LTPS technology. By using the folded R-string circuit, segmented digital decoders, and reordering decoding circuit, the transistor number of the new proposed DAC circuit can be effectively reduced to about one sixth of the traditional one. Furthermore, the proposed architecture is suitable for gamma correction design in different LTPS processes by modifying the corresponding R-string value and the decoder. With more

analog and digital circuits realized on the glass substrate in LTPS technology, the goal of system-on-panel (SOP) applications can be achieved in the near future.

In chapter 3, in order to realize the requirement that using the DAC with gamma correction of 3-V liquid crystal (LC) specification to drive the 5-V liquid crystal with the desired 5-V gamma curve without re-designing the DAC with 5-V gamma correction parameters, the two-stage OP amp is applied in the proposed circuits due to its larger unity-gain frequency, better slew rate, lower input offset voltage, better immunity to noise, and more steady circuit performance. With design consideration aforementioned in chapter 1.4, two analog output buffers with level shifting function on glass substrate for panel application has been successfully designed and fabricated in a 3-μm LTPS technology. By using OPAMP, decoder 2, R1, R201-R237, MR01-MR37, and DAC with 3-V gamma correction parameters, the new proposed analog output buffer I can drive 5-V liquid crystal panel without re-designing the DAC with 5-V gamma correction parameters. By utilizing amendment voltage Va derived from RA01-RA31 and MA01-MA30, the measured results in the new proposed analog output buffer II show better consistent to ideal gamma curve with gamma value of 2.2.

In chapter 4, a new on-panel readout circuit for touch panel applications has been designed and fabricated in a 3-μm low temperature poly-silicon (LTPS) technology. For the purpose of touch-event detection, the switched-capacitor (SC) technique is applied to enlarge the voltage difference from the capacitance change of touch panel. With design consideration in chapter 1.4, the folded-cascode operational amplifier is utilized in the proposed circuit instead of two-stage OP amp. because random device-to-device variation on unlling resistor and Miller compensation capacitor in LTPS process exert quite influence on the performance of on-panel readout circuit in LTPS process. In addition, the corrected double-sampling (CDS) technique is employed for on-panel circuit design to reduce the offset originated from LTPS process variation. The minimum detectable voltage difference of the proposed circuit is 40 mV, with corresponding capacitance change of 0.5 pF under total capacitance of 100 pF, and the different touch area can be identified by the 4-bit digital output. The proposed readout circuit for touch panel application on glass substrate can be integrated in the active matrix LCD (AMLCD) panels to increase the sensing resolution of touch panel for SOP applications.

In chapter 5, with design consideration in chapter 1.4, the proposed circuit in this chapter is composed of larger digital part, smaller analog part, and digital correction circuit,

so it can be realized more easily and successively compared with that in chapter 4 in LTPS process. In chapter 4, a new on-panel readout circuit with SC and CDS techniques for touch panel applications has been designed and fabricated in a 3-μm LTPS technology. Although SC and CDS techniques result in the higher performance for on-panel readout circuit, the complexity of such circuit is still too high for implementation in LTPS process. In this chapter, a readout circuit on glass substrate with digital correction for touch panel application, which contains Gm amplifier, counter, and digital calibration circuit, has been designed and verified in a 3-μm low temperature poly-silicon (LTPS) technology. In this work, the voltage difference from capacitance change due to the touch event on panel is converted to current by Gm amplifier. By charging and discharging the capacitor in the counter, the counter displays different digital output codes according to touch or non-touch event. According to the simulated results, the proposed readout circuit on glass substrate with digital correction can not only distinguish the touch or non-touch event but also can compensate the influence of process variation by digital correction circuit.

6.2 Future Works

Some on-panel analog circuits design in low temperature poly-silicon for display panel applications have been proposed and verified in this dissertation. To integrate all kind of circuits within a display for SOP application is the trend to achieve compact, highly reliable, and high resolution display. At present, many remarkable advances have been done not only on the circuit integration such as analog-to-digital converter, DC-DC converter, bandgap reference circuit, memory, demodulator for RFID Tags, phase-locked loop, and so on, but also on some other applications for system integration like sensor, touch screen panel, CPU, and so forth. The integration of circuits or systems on panel for SOP application should take power consumption into consideration, since low power consumption of electric products is an important target for energy saving and for longer operating time especially in portable devices.

In addition, trends toward larger display panel applications, current consumption and temperature effect of on-panel circuits are more important due to the feature of glass substrates utilized in LTPS process. Current density of ITO layer in LTPS process is less than that of metal layer in CMOS process, so the capability for current supply is limited by such feature. Quality viewing performance in small formats and high strength in thin form factors are also creating challenges for display components. Since the electrothermal enhanced

migration of Si atoms at the grain boundary plays a greatly important role for LTPS TFTs under high-current situations, to reduce the size of the grain boundary and to design the low-power circuit will be the first priority for system-on-panel applications [102], [103]. Thermal dissipation in LTPS process is much worse than that in CMOS process due to the feature of glass substrates utilized in LTPS process. Temperature effect should be considered for on-panel circuit design. Finally, the emphasis should be putted on green technologies, multi-touch display, 3-D displays, and flexible displays in the future.

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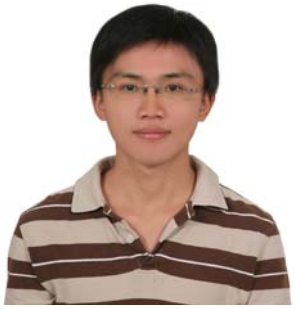
Vita



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論文名稱：低溫多晶矽製程之類比積體電路設計與實現

Design and Implementation of On-Panel Analog Circuits in Low Temperature Poly Silicon (LTPS) Process for Display Panel Applications

Publication List

(A) Referred Journal Papers:

[1] **Tzu-Ming Wang**, M.-D. Ker, and H.-T. Liao, "Design of mixed-voltage-tolerant crystal oscillator circuit in low-voltage CMOS technology," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 56, no. 5, pp. 966-974, May 2009.

[2] **Tzu-Ming Wang**, M.-D. Ker, and S.-C. Chen "Design of analog output buffer with level shifting function on glass substrate for panel application," *IEEE/OSA Journal of Display Technology*, vol. 5, no. 9, pp.368-375, Sep. 2009.

[3] **Tzu-Ming Wang**, Y.-H. Li, and M.-D. Ker, "Digital-to-analog converter with gamma correction on glass substrate for TFT-panel applications," *Journal of Society for Information Display*, vol. 17, no. 10, pp. 785-794, Oct. 2009.

[4] **Tzu-Ming Wang** and M.-D. Ker, "Design and implementation of readout circuit on glass substrate for touch panel applications," *IEEE/OSA Journal of Display Technology*, vol. 6, no. 8, pp.290-297, Aug. 2010.

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(B) International Conference Papers:

[1] **Tzu-Ming Wang**, M.-D. Ker, S. Yeh., and Y.-C. Chang, "Low-power wordline voltage generator for low-voltage flash memory," *Proc. of IEEE Int. Conf. on Electronics, Circuits and Systems*, 2006, pp. 220-223.

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converter with reordering decoder circuit in LTPS technology," *Proc. of Int. Workshop on Active-Matrix Flatpanel Displays and Devices*, 2008, pp. 221-224.

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(C) Local Conference Papers:

[1] **Tzu-Ming Wang** and M.-D. Ker, "Design of analog circuits on glass substrate," *Proc. of Int. PhD Student Workshop on SOC*, 2008.