國 立 交 通 大 學

光電工程研究所

博 士 論 文

玻璃基板上之電路設計與實現及其於顯示系統之應用

DESIGN AND IMPLEMENTATION OF ON-PANEL CIRCUITS FOR APPLICATIONS IN DISPLAY SYSTEM

研 究 生：竹 立 煒 (Li-Wei Chu)

指導教授：劉 柏 村 (Po-Tsun Liu)
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中華民國一百零一年六月

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摘要

隨著現今科技的演進，智慧型手機以及平板電腦已將取代筆記型電腦與個人數位助理(Personal Digital Assistant, PDA)裝置，因為其可提供行動網路、多媒體數位與內建全球定位系統(Global Positioning System, GPS)等功能，而這些產品的問世為顯示器與半導體的市場帶來了大幅度的成長，也因此客戶們對於具備高速資料傳輸的產品有了更多的需求，所以顯示裝置具備薄邊框(narrow bezel)、低功耗與高速運算等功能將可大量增加產品的普及性與銷售量。

為了達到顯示裝置對於薄邊框的需求，液晶顯示器(Liquid Crystal Display, LCD)中的閘極驅動電路(gate driver)使用薄膜電晶體(Thin-Film-Transistor, TFT)設計已成為一個主要的趨勢，因為有成熟的顯示技術、低成本的製程與減少互補式金氧半(Complementary Metal-Oxide-Semiconductor, CMOS)積體電路(Integrated Circuit, ICs)的數量等優點，此外為了降低顯示裝置於靜態畫面顯示時所消耗的功耗，記憶體內嵌於畫素(Memorry-In-Pixel (MIP)的概念也被提出並使用薄膜電晶體所設計，然而設計薄膜電晶體的電路相對於 CMOS 電路主要面對到較低的載子傳輸能力以及高電壓驅動導致穩定度下降的兩個重要挑戰，而為了降低較低載子傳輸能力的限制，薄膜電晶體在佈局時會使用較大的面積推動面板內部的負載，但也不可避免造成電路具有較大的寄生(parasitic)效應，再加上薄膜電晶體電路的耐久度也是一個需要解決的問題，因為當薄膜

電晶體經過長期電壓的施加，薄膜電晶體的主動層會產生大量缺陷(defects)進而使電晶體的臨界電壓偏移減少了顯示產品的耐久度，所以前述的兩項因素為薄膜電晶體電路的主要設計挑戰。此外大型積體電路(Large Scale Integration, LSI)接合於顯示面板是為了減少 IC 的腳位以及增加處理射頻(Ratio Frequency, RF)訊號的能力，然而射頻前段電路是與外部天線或濾波器所連接，所以其必然需要靜電放電(ElectroStatic Discharge, ESD)防護電路的放置，但靜電放電防護元件無可避免的會讓輸入與輸出的銲墊(Pad)增加額外寄生的效應，因此設計靜電放電防護元件於面板上的電路也是一個重要的挑戰，即同時達到最高靜電放電的耐受度以及最小射頻訊號的損失。

總結前述的電路設計的挑戰即為本研究論文的主題:設計與實現玻璃基板上之電路及其於顯示系統的應用，本論文的章節包括：(1) 設計可消除電晶體臨界電壓的閘極驅動電路於非晶矽薄膜製程、(2) 設計低功率閘極驅動電路以非晶矽薄膜製程於薄邊框面板的應用、(3) 類比畫素記憶體電路以低溫多晶矽製程於低功耗顯示器的應用、 (4) 電感觸發觸發矽控整流器的靜電放電防護電路以 65 奈米 CMOS 製程於 60GHz 低雜訊放大器的應用、(5) 設計雙波段靜電放電防護電路於毫米波電路的應用。

本論文第二章提出一種新型的閘極驅動電路並成功以非晶矽薄膜電晶體設計與製作於 3.8 吋 WVGA(480xRGBx800)規格的面板，此提出之電路利用電晶體臨界電壓消除之方式，使閘極驅動電路的輸出上升時間(Rise Time)減少了 24.6%，進而使其可應用於高解析度之顯示器。本論文第三章利用四個時脈(Clock)訊號設計閘極驅動電路，使得推升電晶體同時具備輸出充電與放電的功能，進而使電路的佈局面積有效的縮小並可於薄邊框的顯示器應用，此外因為減少了時脈訊號的工作週期(Duty Cycle)，所以此提出之電路可以減少靜態功率的消耗，而電路的掃描方向也只需透過切換兩個直流訊號即可達到反向顯示的功效，此所提出之電路已成功展示於 WXGA(1440xRGBx800)規格的面板且通過合作公司的穩定度測試。

本論文第四章提出兩種多晶矽薄膜電晶體類比記憶體電路於低功耗應用的液晶顯示器之設計，此電路將反轉畫素電壓透過互補式源極追隨器(Source Follower)使資料訊號可儲存於電容上，並將顯示靜態影像的畫框時間由 60Hz 降低至 3.16Hz，而輸出的電壓的衰減也小於 0.1V 於 1 到 4V 的資料訊號輸入中，本論文亦提出一種可補償電晶體臨界電壓的設計，達到減少源極追隨器的輸出電壓對於電晶體臨界電壓的相依性。

本論文第五章提出使用電感加速矽控整流器導通速度的靜電放電防護電路，而電感的感值與矽控整流器的寄生電容可設計共振於射頻電路所操作的頻率，進而降低射頻訊

號的損耗(Loss)，而此提出之射頻靜電放電防護電路已驗證於 65 奈米 CMOS 製程並操作於 60GHz，且為了射頻接收器的射頻特性和靜電放電防護能力的證實，所提出的電感觸發矽控整流器靜電放電防護電路已成功應用於 60GHz 低雜訊放大器中並獲得良好的成果。本論文第六章提出雙波段(24GHz 與 60GHz)靜電放電防護電路，此電路由二極體、矽控整流器、P 型電晶體與電感所組成，而為了驗證雙波段的射頻特性與靜電放電的防護能力，所提出之電路已成功應用於雙波段低雜訊放大器中，量測的結果展示了超過 2.75kV 的人體放電模式(Human Body Model, HBM)且雙波段射頻的特性也僅有些微的損耗。

第七章總結本論文的研究成果，並提出數個接續本論文研究方向的研究題目。本論文所提出的各項新型設計，皆已搭配面板整合或實驗晶片加以驗證。此外本研究有數篇國際期刊與國際研討會論文發表，並有數項創新設計已提出中華民國及美國專利申請。

DESIGN AND IMPLEMENTATION OF ON-PANEL CIRCUITS FOR APPLICATIONS IN DISPLAY SYSTEM

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Abstract

With current technology advancements, smart phones and tablet computers are fast becoming a viable alternative to PDAs and laptops, offering features such as mobile internet applications, multi-media functionality, and inbuilt GPS capabilities. The emergence of these products brings the progressive growing of display market. Therefore, display devices with narrow bezel, low power consumption, and high speed data capabilities are gaining the sale volume and popularity.

For the narrow bezel demands of display devices, gate driver circuit using thin-film-transistor (TFT) has become a main stream for the liquid crystal display (LCD) due to the mature manufacturing, low-cost processing, and reducing of complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs). Furthermore, the design of memory-in-pixel (MIP) using TFT is as well as proposed to meet the low power consumption of mobile displays, which provided a low power standby mode for continuous display of static images. Nevertheless, design of TFT driver encounters two main challenges which are the lower field-effect mobility and the reliability issue under high voltage stress as compared

with CMOS transistors. In order to alleviate the low mobility restriction, the larger width of the main driving TFT is required to drive the panel, however it accompanies with large parasitic effects inevitably. In addition, the reliability issue of the TFT drivers is as well as a notable challenge. While TFT suffers long term high voltage stress, the defect-state creation will cause threshold voltage shifts to decrease the life time of the driver. Consequently, these characteristics increase the design challenge of TFT driver circuits. Besides, large scale integration (LSI) mounted on-panel area is primarily used to minimize footprint of the IC and suited to handling high-frequency (RF) signals. However, since the RF front-end circuits connect the RF transceiver to the external antenna or band-select filter, they must need electrostatic discharge (ESD) protections. The ESD protection devices at the I/O pads inevitably cause parasitic effects on the signal path and lead to the design challenge for on-panel RF circuits, which is to achieve the highest ESD robustness with the smallest RF performance degradation.

The aforementioned design challenges of on-panel circuits for applications in display system form the motivation of this dissertation. The research topics of this dissertation including: (1) integrated gate driver with threshold voltage drop cancellation in amorphous silicon (a-Si) technology, (2) low power gate driver in a-Si technology for narrow bezel panel application, (3) analog pixel memory in low temperature poly silicon (LTPS) technology for low power display, (4) ESD protection design for 60GHz low noise amplifier (LNA) with inductor-triggered silicon-controlled rectifier (SCR) in 65nm CMOS process, and (5) dual-band ESD protection for 24/60 GHz millimeter-wave circuits.

In chapter 2, a new integrated gate driver on array (GOA) has been successfully designed and fabricated by amorphous silicon (a-Si) technology for a 3.8-inch WVGA (480xRGBx800) TFT-LCD panel. With the proposed threshold voltage drop cancellation technique, the output rise time of the proposed integrated gate driver can be substantially decreased by 24.6% for high resolution display application. In chapter 3, with utilizing four clock signals in the design of GOA, the pull-up transistor has ability for both output charging and discharging, and layout size of the proposed gate driver can be narrowed for bezel panel application. Moreover, lower duty cycle of clock signals can decrease static power loss to further reduce the overall power consumption of the proposed gate driver. The scan direction of the proposed gate driver can be adjusted by switching two direct control signals to present the reversal display of image. Additionally, the proposed gate driver has been successfully demonstrated in a 4.5-inch WXGA (1440xRGBx800) TFT-LCD panel and passed reliability tests of the supporting foundry.

In chapter 4, two types of analog memory cells realized in 3μm LTPS technology are proposed to achieve low power application for thin film transistor liquid crystal displays (TFT-LCDs). By employing the inversion signal in the storage capacitor with complementary source follower, the frame rate to refresh the static image can be reduced from 60Hz to 3.16Hz with the output decay less than 0.1V under the input data from 1V to 4V. To further diminish threshold voltage drop from source follower structure, a compensation technique is implemented to the proposed analog memory cells.

In chapter 5, an SCR device assisted with an inductor is proposed to improve the turn-on efficiency for ESD protection. Besides, the inductor can be also designed to resonate with the parasitic capacitance of the SCR device at the selected frequency band for RF performance fine tuning. Experimental results of the ESD protection design with inductor-triggered SCR in a nanoscale CMOS process have been successfully verified at 60GHz frequency. To verify the RF characteristics and ESD robustness in the RF receiver, the inductor-triggered SCR has been applied to a 60GHz low-noise amplifier (LNA). In chapter 6, dual-band ESD protection cell is proposed for 24/60 GHz ESD protection. The proposed cell consisted of a diode, a silicon-controlled rectifier (SCR), a PMOS, and inductors. To verify the dual-band characteristics and ESD robustness for the RF receiver, the proposed ESD protection circuit had been applied to a 24/60 GHz low-noise amplifier (LNA). Measurement results present over 2.75kV human-body-model (HBM) ESD robustness with little RF performance degradation.

Chapter 7 summarizes the main results of this dissertation. Some suggestions for the future works are also addressed in this chapter.

In this dissertation, several novel designs have been proposed in the aforementioned research topics. Measured results of the integrated panels and fabricated test chips have demonstrated the performance improvement. The achievements of this dissertation have been published or submitted to several international journal and conference papers. Several innovative designs have been applied for patents.

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在這段求學的過程中,『凌巨科技股份有限公司』提供的產學合作計畫，並得到『面板設計部』給予我研究上的支持與協助，從實驗電路的下線與面板的整合支援協助，使得我實驗研究能夠順利完成。在此特別要感謝濮家銓副總、陳佳興處長、周凱茹經理、吳哲耀課長和工程師賴谷皇等人所給予的支持與鼓勵。同樣也感謝『台灣積體電路股份有限公司』提供的產學合作計畫，並透過『設計技術平台部門』給予研究上的協助，從實驗晶片下線到高頻與靜電放電量測的支援與協助。在此特別要感謝宋明相副處長、曾仁洲經理、盧澤華經理和工程師洪彬舫、李孝純、魏佑霖、蔡銘憲、張子恆等人所給予的支持與鼓勵，使本論文的研究成果得以成功驗證，並順利發表於國際期刊與國際研討會。

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竹 立 煒

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Chapter 1

Introduction

In this chapter, the background of this dissertation is discussed. First, thin-film-transistor (TFT) liquid crystal display (LCD) is discussed. Then, thin-film silicon technology, system-on-panel (SOP) application, and design consideration for on-panel circuit are introduced. Finally, the organization of this dissertation is described.

1.1. Thin-Film-Transistor Liquid Crystal Display [1]-[9]

In recent years, smart phones and tablet computers are fast becoming a viable alternative to PDAs and laptops, offering features such as mobile internet applications, multi-media functionality, and inbuilt GPS capabilities. The emergence of these products brings the progressive growing of TFT LCDs market. Therefore, display devices with narrow bezel, low power consumption, and high speed data capabilities are gaining the sale volume and popularity. Besides, for high-speed communication networks, the emerging portable information tools are expected to grow in following on the rapid development of display technologies. Thus, the development of higher specification is demanded for LCD as an information display device. Moreover, the continual growth in network infrastructures will drive the demand for displays in mobile applications and flat panels for computer monitors and TVs. The specifications of these applications will require high-quality displays that are nexpensive, energy-efficient, lightweight, and thin.

1.1.1. History of Liquid Crystal Display

Thin-film-transistor (TFT) liquid crystal display (LCD) is a flat display within liquid-crystal inside the display and each pixel is controlled by a TFT. The market of TFT LCD is growing in consumer electronics, computers, and communication systems. The concept of TFT LCD was first mentioned in 1966. In 1966, the possibility of using TFTs as display switch was mentioned by Weimer. A sandwich cell consisting of a transparent front electrode, a reflecting back electrode, and nematic liquid-crystal in between, was proposed by

Heilmeier in 1968. When there was no applied field, the cell displays black. When a dc voltage was applied, the liquid crystal became turbulent and scattered light: the cell appeared white. For active-matrix LCD, the diode or transistor utilized as switch and storage capacitors implemented in parallel were mentioned in 1971. In 1973, Brody proposed the CdSe TFT for active-matrix liquid crystal panel with 14000 transistors, storage capacitors, and twisted-nematic (TN) liquid crystal cell, where TN liquid crystal cell was first mentioned by Schadt and Helfrich. After that, the development of practical TFT LCD has been studied and implemented for more than thirty years with many novel applications. In addition, TFT LCD exhibits higher contrast, larger viewing angle, and faster response time compared with that of traditional LCD. Therefore, TFT LCD panel grows rapidly for large panel application, like television, and for small panel applications such as digital camera, mobile phone, personal digital assistants (PDAs). With current technology advancements, smart phones and tablet computers are fast invented and becoming more attractive products for customers to pursuit as results of offering more multi-media functionalities.

1.1.2. Configuration and Operation of LCD

The structure of thin-film-transistor liquid crystal display is sandwich-like. It consists two flat glasses and the liquid crystal (LC) filled between two glasses as figure shown in Fig. 1.1. A backlight module including an illuminator and a light guilder is also needed since liquid crystal molecule cannot light by itself [1].

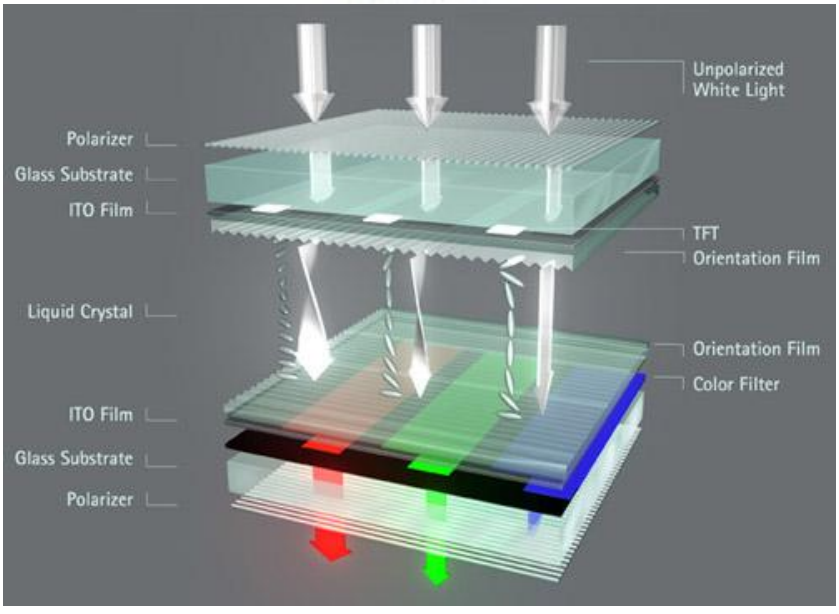
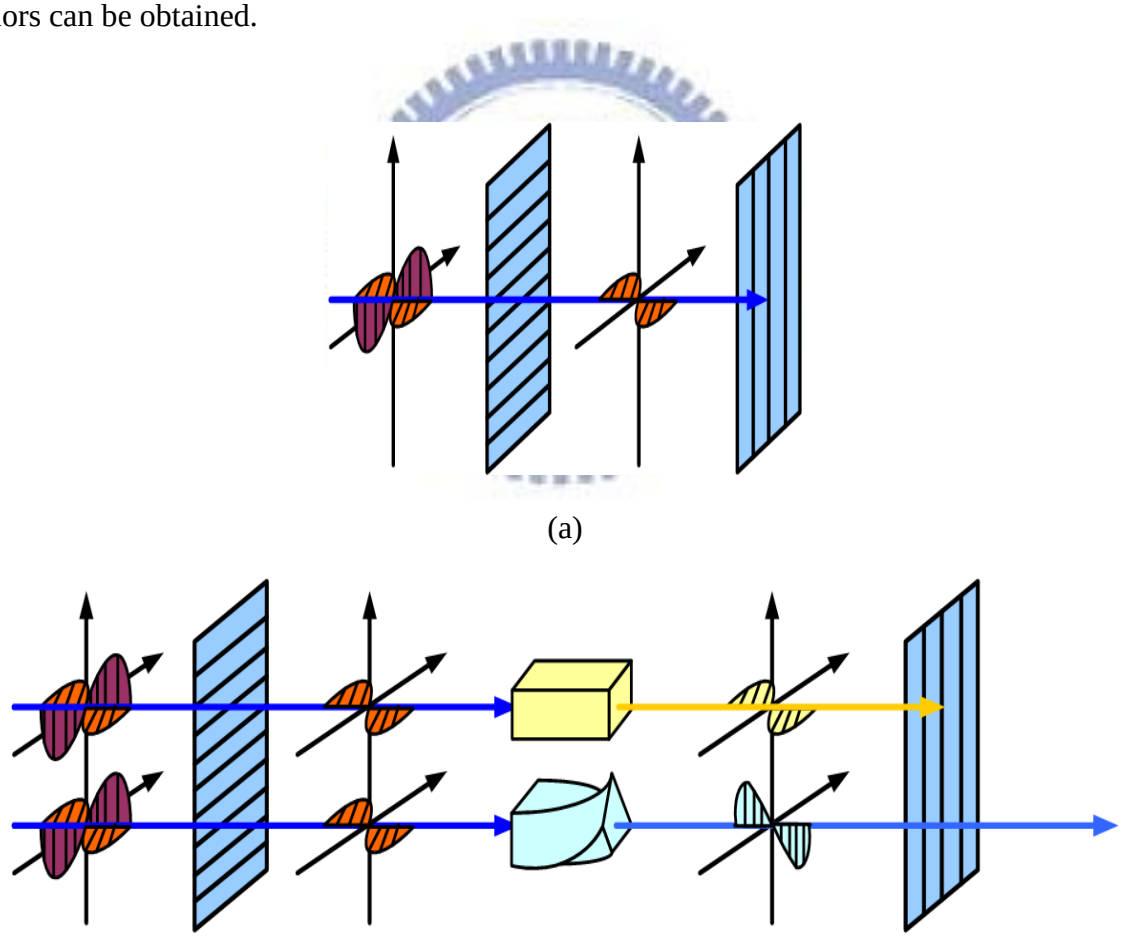


Fig. 1.1. The structure of thin-film-transistor liquid crystal display.

In order to obtain better display quality, the cell gap of the liquid crystal, which is the spacer between top and bottom glass substrate in Fig. 1.1, has to be precisely controlled to a specific value, e.g., 5 μm. This gap must be uniform and reproducible over the whole display area. Therefore, transparent spacers such as plastic beads are placed on the surface of the glass substrate.

In TFT array substrate at the top side in Fig. 1.1, there is a polarizer, a glass substrate, a transparent electrode (ITO film), and an orientation layer. In color filter substrate at the bottom side in Fig. 1.1, there is an orientation layer, a transparent electrode, color filters, a glass substrate and a polarizer. ITO films can control the directions of liquid crystal molecules in each pixel by voltage supplied from TFT on the glass substrate. Color filters contain three original colors, red, green, and blue (RGB). As the degree of light, named "gray level", can be well controlled in each pixel covered by color filer, more than million kinds of colors can be obtained.



(a)

(b)

Fig. 1.2. (a) A couple of polarizers with 90 phase difference and (b) a couple of polarizers with liquid crystal.

The polarizer can block or pass the specific light by changing the phase of the polarizer. There are two polarizers including the first polarizer called polarizer and the second polarizer called analyzer. If the couple of polarizers have 90° phase difference, the light can be blocked which is shown in Fig. 1.2(a). But if liquid crystal molecule is twist by applying the specific electric field across it, the light still can pass the polarizer. This is because the direction of liquid crystal molecules varies with electric field and it can guide the light along the long axis, shown in Fig. 1.2(b).

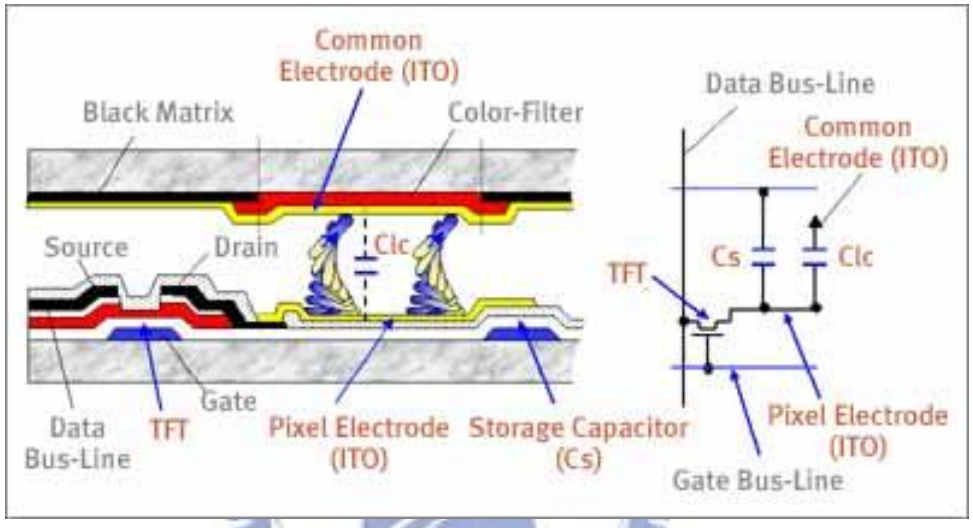


Fig. 1.3. The cross section and equivalent circuit of an AMLCD sub-pixel.

Fig. 1.3 shows the cross section and equivalent circuit of an AMLCD sub-pixel. The LC layer can be considered as a capacitor; therefore, transparency of LC can be changed by applying voltage between common electrode and pixel electrodes. Each sub-pixel has its sub-pixel electrode so that we can determine luminance of each color through input image data. In order to input data accurately and successively, the thin film transistors (TFTs) play a crucial role in active matrix (AM) method, which is the main display style for LCDs. Furthermore, each sub-pixel includes a TFT, a storage capacitor, a portion of a gate line, and a portion of data line. The TFT is like a switch that is responsible for controlling data voltage transport into the storage and LC capacitors. In the end, the modulated light brings about dark or bright of red, green, and blue. With different combination of three original colors, perceive full color of image can be presented. The resolution of a screen is defined as the number of pixels, the more pixels means the better quality of display. To get better image quality, the non-transmitted area in each pixel such as TFTs and storage capacitors should be minimized.

1.1.3. Mobile Display System of TFT LCD

Fig. 1.4 depicts the block diagram of mobile display system of TFT LCD and its fundamental operation blocks are mainly divided into three parts: RF transceiver, analog base band, and digital baseband [5].

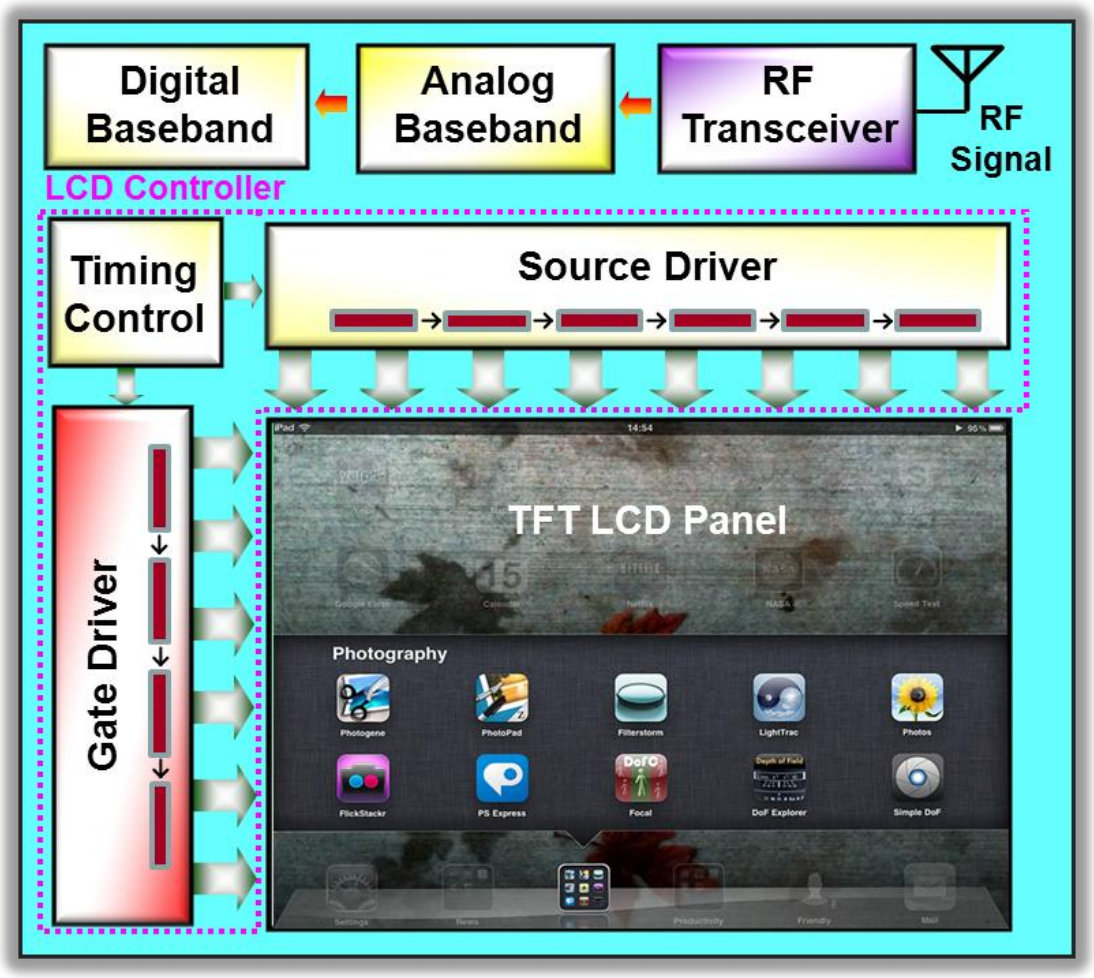


Fig. 1.4. The block diagram of mobile display system of TFT LCD.

For the RF transceiver, it is the section that transmits and receives certain frequency to a network and synchronizes to other phone. It is based on two main circuits, transmitter and receiver. A simple mobile phone uses these two circuits to correspond to another mobile phone. For the analog base band, this section is used to convert analog to digital (A/D) and digital to analog signals (D/A), and it is composed of different types of circuits, such as control section, charging section, and audio codecs section. For the digital base band, is is the part where all application being process. Digital baseband is used in mobile phones to handle data input and output signal like driving applications commands and LCD controller.

The LCD controller in Fig. 1.4 is composed of timing control, scan driver, and data driver circuits. The TFT LCD panel is constructed of the active matrix liquid crystals and the operation of the active matrixes is similar to DRAM (dynamic random access memory) which is used to charge and discharge the capacitor of the pixel. Timing control circuit is responsible for transmitting RGB (red, green, and blue) signals to the data driver and controlling the behavior of scan driver. As soon as one voltage level of the scan lines rises, the RGB signals are transmitted through the data driver. After a period, the voltage level of this scan line is disabled and next scan line is turned on. All voltage levels of those scan lines are raised in turn.

Scan driver circuit consists of shifter register, level shifter, and digital output buffer. Shifter register is used to store digital input signals then transit to the next stage according to timing control circuit. Because the turn-on voltage of active matrixes is higher, scan driver should drive the active pixels with a high voltage. The purpose of the level shifter is to convert the digital signal to higher voltage level. Finally, since the scan lines can be modeled as RC (resister and capacitor) ladder, the digital output buffer should be used in the last stage for driving the large load.

Data driver circuit includes shifter register, data latch, level shifter, digital-to-analog converter (DAC), and analog output buffer. The first three parts classify as digital architectures, and the other two parts belong to analog architectures. Shifter register and data latch manage to transit and store the RGB signals. The purpose of level shifter is the same as the one in scan driver circuit, which is applied to translate the RGB signal to a higher level voltage. In addition, digital-to-analog converter is used to convert the digital RGB signal to analog gray level. The analog output buffer is applied to drive active pixels into a desired gray level.

1.2. Thin-Film Silicon Technology [10]

As the developing of digital life and growing of flat panel display market, thin-film silicon technology plays an important role due to the mature manufacturing, low-cost processing for large area fabrication. A thin-film transistor (TFT) is a field-effect transistor made by this process to form the silicon active layer as well as the dielectric layer and metallic contacts over a supporting substrate. This differs from the conventional transistor where the semiconductor material typically is the substrate, such as a silicon wafer. The characteristics of a silicon based thin-film-transistor depend on the crystalline state; that is,

the semiconductor layer can be either amorphous silicon, microcrystalline silicon, or it can be annealed into polysilicon.

1.2.1. Amorphous Silicon Technology

Hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) is an mature technology and widely use as switching device in AMLCDs. The major advantages that makes this technology been widely used are its good electronic properties such as high photoconductivity, low cost fabrication at low temperatures, uniform device characteristics.

Amorphous silicon thin-film-transistors can be made with a wide variety of structures and materials. Basically there are four types of planar TFT (Fig. l.5), defined by the order of deposition of the semiconductor layer, the gate insulator layer, the source-drain contacts, and the gate electrode [11].

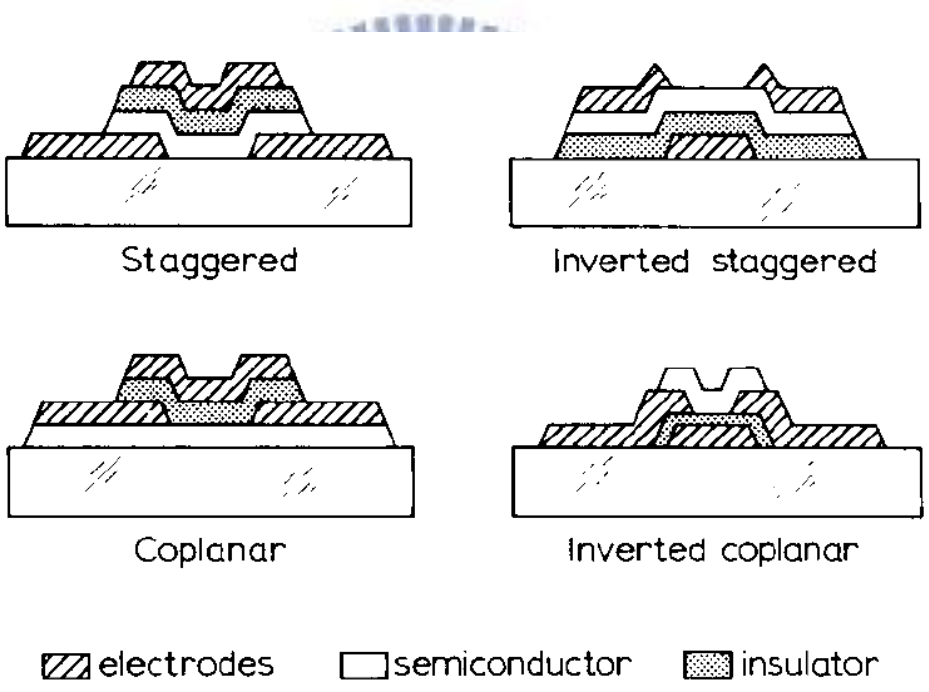


Fig. 1.5. Amorphous silicon thin-film-transistor configurations.

The staggered TFT structures have the source and drain contacts on one side of the semiconductor and the gate electrode on the opposite side, while the coplanar structures have all three electrodes on the same side of the semiconductor film. In the “inverted” structures, the gate electrode is the first layer deposited on the glass substrate. A-Si TFTs have been made with all four structures, but to date all devices used in practical applications use one of the staggered structures. For a-Si TFT’s, the most popular structure and the one responsible

for the state of the art performance, is the inverted-staggered TFT, which uses silicon nitride as the gate insulator and its five masks process are shown in Fig. 1.6.

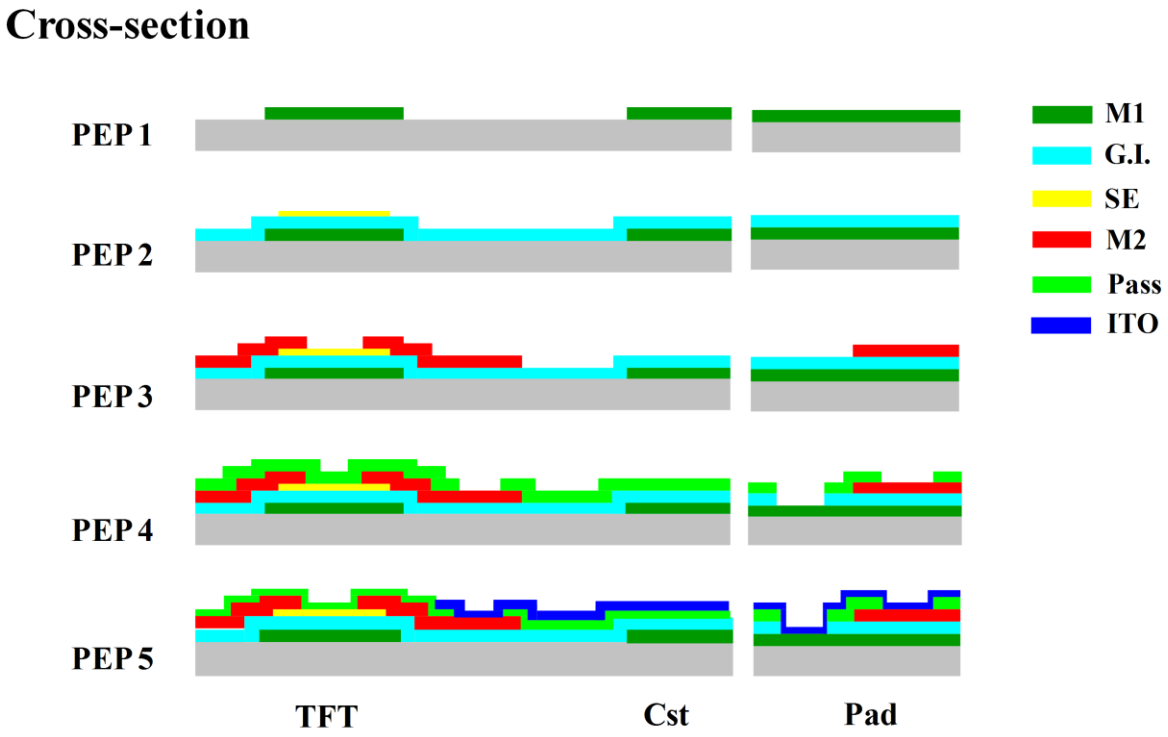


Fig. 1.6. The cross-section of inverted-staggered a-Si TFTs under five masks process.

The first mask is utilized to define metal 1 (M1), and the second mask is used to define the active layer of a-Si (SE). Metal 2 (M2), and N+ a-S are defined in the third mask. After that, passivation layer is etched to form a connecting bridge for the flowing ITO film process in the fourth mask. Finally, ITO film is defined for completing the devices of TFT, storage capacitor (Cst), and pad.

1.2.2. Low Temperature Poly-Silicon Technology

Low temperature poly-silicon (LTPS) technology has become an important feature for high image quality display due to the high performance and high resolution. Compared with conventional a-Si TFTs, some characteristics, such as higher carrier mobility, lower threshold voltage, and higher stability, of low temperature poly silicon (LTPS) TFTs can achieve compact, highly reliable, and high resolution for system integration within a display panel. Besides, the capability for integrating peripheral circuits on glass substrate can decrease peripheral dimension and fabrication cost and higher aperture ratio can be achieved by higher

mobility of LTPS TFT because the pixel size can be further reduced.

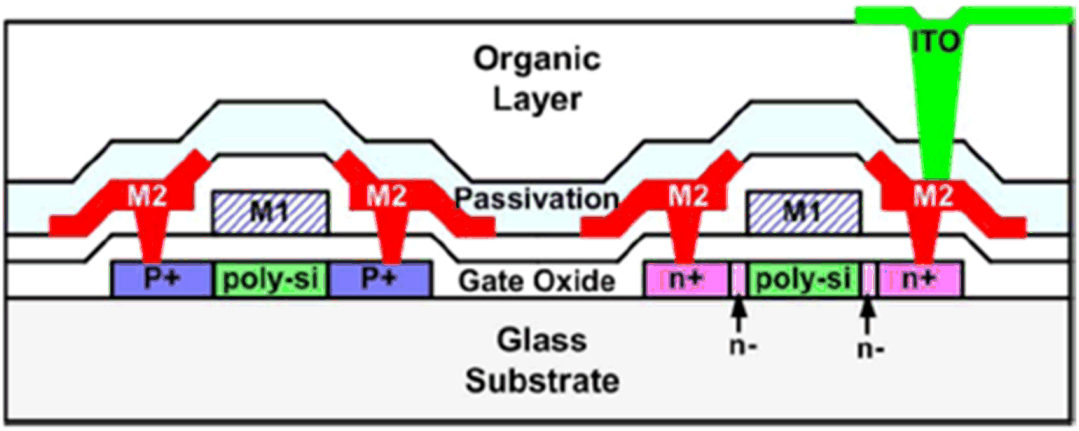


Fig. 1.7. The cross-section of poly silicon TFTs. (left side is P-type TFT and right side is N-type TFT).

Fig. 1.7 shows the cross-section of poly silicon TFTs. Fabrication process starts from the buffer layer which was deposited on the glass substrate [12]. Then, the undoped 50-nm-thick a-Si layer was deposited and crystallized by XeCl excimer laser with a laser energy density varied from 340mJ/cm^2 to 420mJ/cm^2. The recrystallized poly-Si films were patterned into the active islands. Afterward, a 60-nm-thick oxide layer was deposited as the gate insulator. Then, the 200-nm-thick molybdenum was deposited and patterned as the gate electrode. The N-doping was direct self-aligned to the gate electrode without additional mask process. The N+source/drain regions were defined by one mask. The dopants were activated by thermal process. After the deposition of nitride passivation and the formation of contact holes, the 550-nm-thick titanium/aluminum/titanium tri-layer metal was deposited and patterned to be the metal pads.

For summary thin-film the silicon technology, Fig. 1.8 presents comparison results between amorphous, poly, and single crystal silicon. It is clear that the silicon structure is strong related to the carrier mobility. The mobility is only about 0.5 to 1 cm^2/V.s for the amorphous silicon, and poly silicon shows 50 to 100 cm^2/V.s. The mobility of single crystal silicon presents over 600cm^2/V.s. However, although single crystal of wafer process has the largest mobility, it can't be made on the glass substrate since the manufacture temperature is over 900 degree Celsius and its cost is too high to fabricate devices on large panel. Besides, even if amorphous silicon shows the lowest mobility, it still has the advantages of low cost fabrication at low temperatures, uniform device characteristics, and high photoconductivity.

Therefore, the implementation of these technologies should concern their pros and cons to utilize them to suitable applications. As shown in Fig. 1.8, single-crystal-silicon transistor based large-scale-integration (LSI) can be operated at high frequency (up to GHz), so the display system can be applied, and which can be mounted at the printed circuit board (PCB) or on panel as result of the high-temperature process. Furthermore, compared with a-Si TFT, poly silicon TFT can achieve compact, highly reliable, and high resolution to realize driver circuits on glass substrate, such as data driver or gate driver in Fig. 1.4. For the pixel switching of the panel, a-Si TFT plays a significant role because that can fabricate on large size panel with lowest costs, and they have higher device uniformity than poly silicon TFTs.

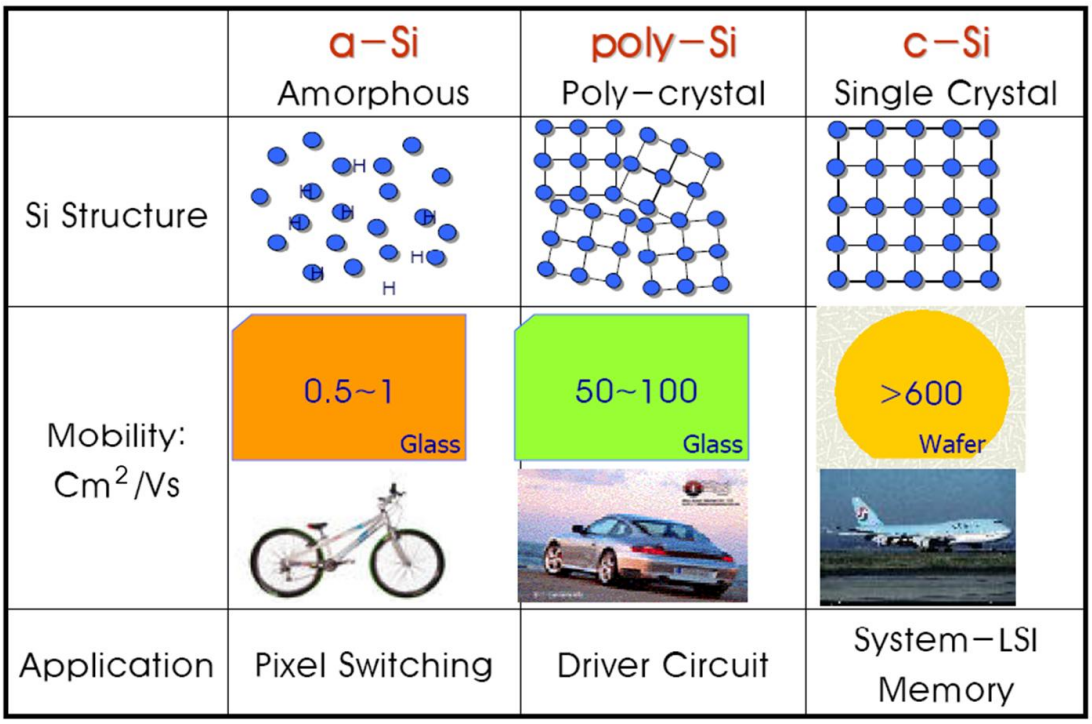


Fig. 1.8. Comparison results between amorphous, poly, and single crystal silicon.

1.3. System on Panel Display Applications

In recently, there are more and more practical uses amorphous and poly silicon technology of forming a part of display circuits on the glass substrate. Fig. 1.9 shows the trends for system on panel (SoP) applications [12]-[17]. SoP application has the potential to realize compact, highly reliable, and high resolution display by integrating functional circuits within a display. For normal display panel, TABs are connected to the left and bottom sides of a panel with driver ICs. Integration of driver ICs with TFTs on panel can achieve COG (chip on glass) but it still requires FPC (flexible printed cable) connection on the bottom for other

functional circuits. The most common failure mechanism of TFT LCD, disconnection of the TABs, is therefore decreased significantly with the save in omitting the usage of ICs and all sub-circuits integrated on panel. Besides, the cost of panel becomes lower, as well as the higher yield rate can be also achieved. Furthermore, for the poly-Si TFT characteristics, such as higher carrier mobility, and lower threshold voltage than a-Si TFTs, are required to fulfill the SoP application. Such integration technology contributes to shorten the product lead time because the assemblage of CMOS ICs can be eliminated. Currently, such integration has been proceeding from simple digital circuits to the sophisticated ones, and other functional circuits utilized on panel will be also integrated in the future to achieve SoP applications.

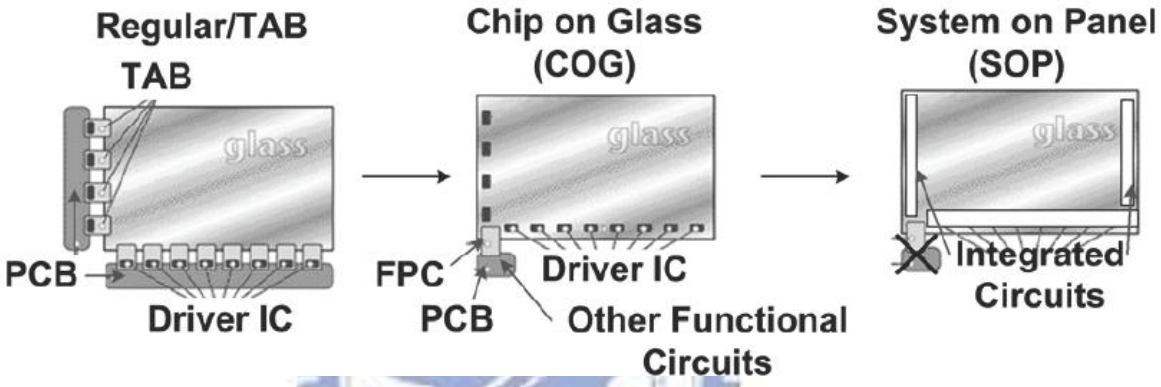


Fig. 1.9. Trends for system-on-panel applications.

Fig. 1.10 shows there are three kinds of peripheral circuits of the array panel including signal processor, display driver, and gate driver. The signal processor can capture and process the photo sensor signals, and then convert them to a suitable form for display. The converted signals are sent to the display driver and the captured images can be displayed. Last, the gate driver controls both the pixel TFT and the sensor circuit. Application to color image capturing has been realized by successively capturing through red, green, and blue (RGB) color filter, and then synthesizing their captured image.

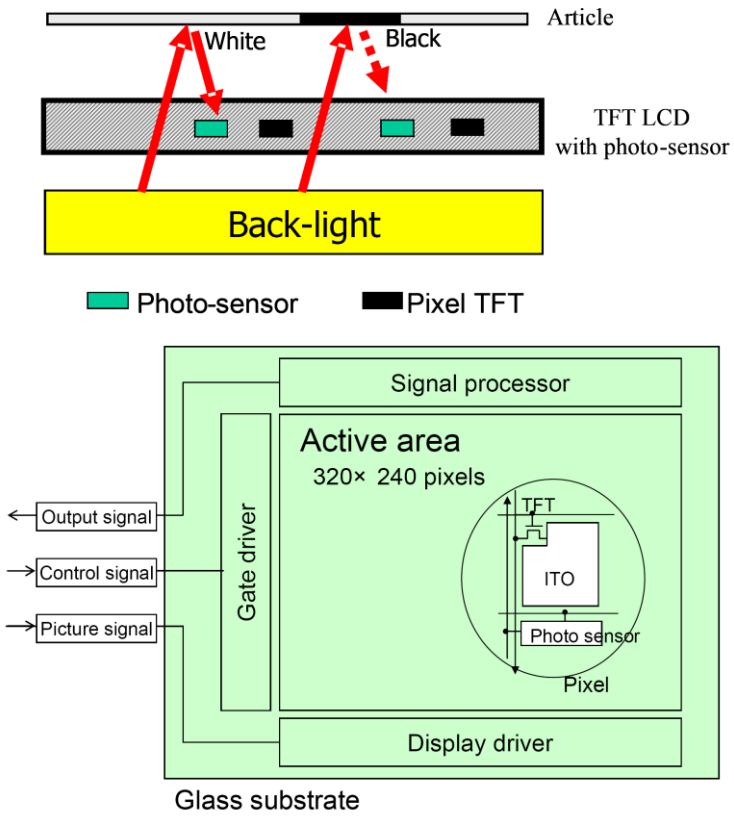
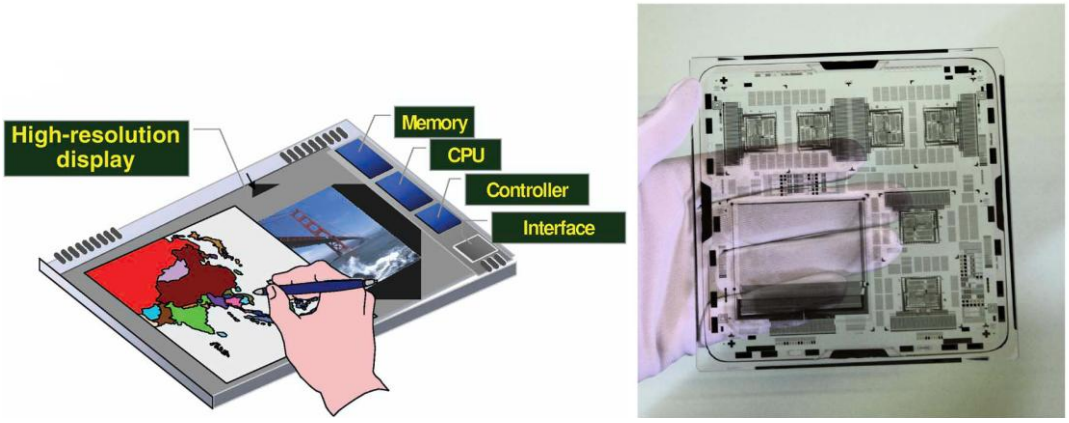


Fig. 1.10. The principle and structure of the photo-sensing display.

In the end, it may be possible to integrate the keyboard, CPU, memory, and display into a single "sheet computer". The schematic illustration of the "sheet computer" concept and a CPU with an instruction set of 1-4 bytes and an 8-bit data bus on glass substrate are shown in Fig. 1.11, respectively [17].

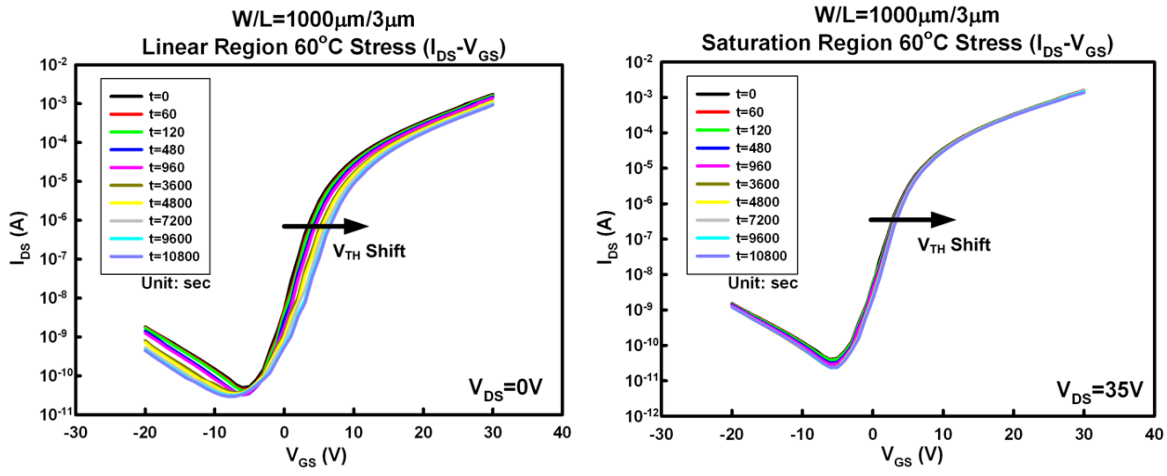


(a) (b)

Fig. 1.11. (a) The "sheet computer" concept and (b) a CPU with an instruction set of 1-4 bytes and an 8-bit data bus on glass substrate.

1.4. Design Consideration for On-Panel Circuit [18]-[22]

For the a-Si TFTs, since the SoP concepts have many features, they still have several obstacles to utilizing in circuits. First of all, the low carrier mobility causes speed and area limitation of a-Si:H TFT integrated circuits. Second, the lack of p-type TFT makes circuit design more difficult because it is impossible to implement complementary circuit structure. Third, high and variable parasitic capacitance due to the non-self-aligned device structure causes signal distortion due to the clock feed-through. Finally, the degradation of a-Si:H TFTs after long-term use would bring about the poor quality or error image of display. This is because the voltage stress biases on the devices so that increases of defects of channel and raises the threshold voltages (Vth) of TFTs, which is known as Vth shifts. Therefore, the reliability issue is critical for a-Si TFTs [18]-[19]. Fig. 1.12(a) and Fig. 1.12(b) illustrate the V_{TH} shifts of 3μm channel length a-Si TFT under 60°C and 35V operation in linear region and saturation region. Fig. 1.13 as well as describes the extracted parameters. It is clearly observed that the stress effects of a-Si TFT are serious when it is operated in linear region as compared in saturation region, and thereby the design of a-Si TFTs based circuit should pay more concern for which are operated in linear region.



(a) (b)

Fig. 1.12. Stressed I_{DS}-V_{GS} for 3μm channel length a-Si TFT under 60℃ and 35V operation in (a) linear region and (b) saturation region.

T(sec)		0	60	120	480	960	3600	4800	7200	9600	10800
Sat. region	V_{TH}	4.61	4.65	4.68	4.74	4.78	4.83	4.90	4.92	4.96	4.96
	μ_{FE}	0.50	0.49	0.49	0.49	0.49	0.49	0.49	0.49	0.48	0.48
	I_{off}	4.28E-11	4.13E-11	4.04E-11	3.36E-11	3.03E-11	2.50E-11	2.47E-11	2.45E-11	2.37E-11	2.40E-11
Linear region	V_{TH}	4.64	4.85	4.99	5.25	5.44	5.93	6.10	6.50	6.77	6.83
	μ_{FE}	0.52	0.50	0.49	0.47	0.45	0.41	0.39	0.37	0.35	0.33
	I_{off}	5.26E-11	4.61E-11	4.30E-11	3.51E-11	3.62E-11	4.70E-11	4.62E-11	4.45E-11	4.31E-11	4.13E-11

Fig. 1.13. Extracted parameters of the stress on 3μm channel length device.

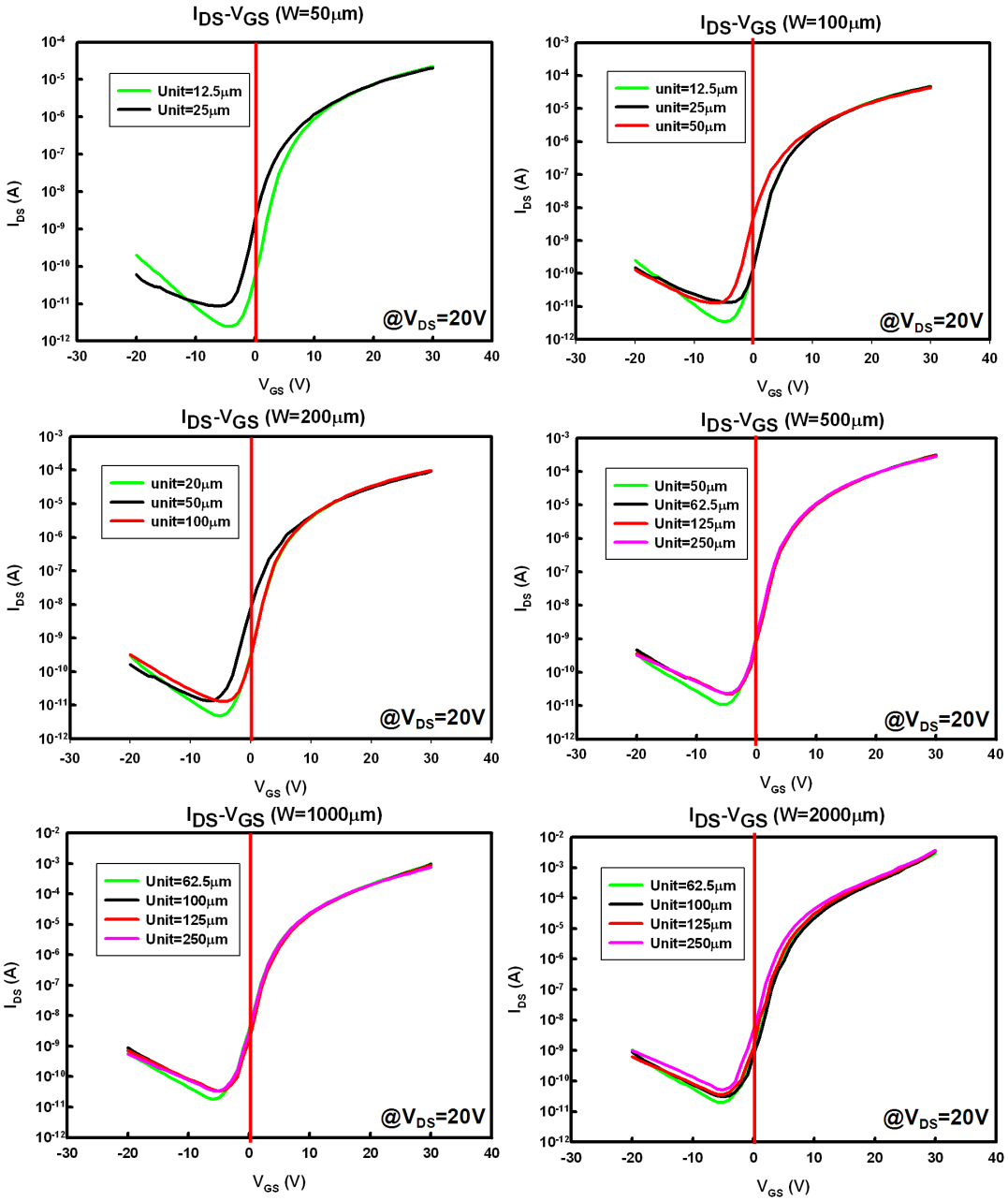


Fig. 1.14. The intersections of red lines and transfer curves represent I_{DS} when V_{GS} is 0V.

For other design considerations of a-Si TFT, when it is under turn-off state in pixel of panel, the gate to source voltage is about -7V and its leakage current is lower to be capable of application for pixel switching. Nevertheless, when it is applied to circuits, like gate driver, the gate to source voltage is about 0V. As shown in Fig. 1.14, larger leakage current is observed at the intersections and it will increase higher static power consumption for the driver circuits. Furthermore, since five masks process of a-Si TFT in Fig. 1.6 has only one via process, M1 and M2 can't be directly connected, and the ITO film should be inserted to link M1 and M2 for forming the pad, however, the series resistance between M1 and M2 will be increased due to higher sheet resistance of ITO film. Therefore, the design consideration of a-Si TFT driver should decrease the static power wastage and care about the layout issues.

For the poly-Si TFTs, since the maximum process temperature of LTPS is lower than 600 degree Celsius, LTPS TFTs can be fabricated on a wide variety of cheap glasses to further reduce the cost. However, compared with the requirement as being a switch, poly-Si TFTs requires good electrical stability as being utilized to integrate circuits or systems on panel.

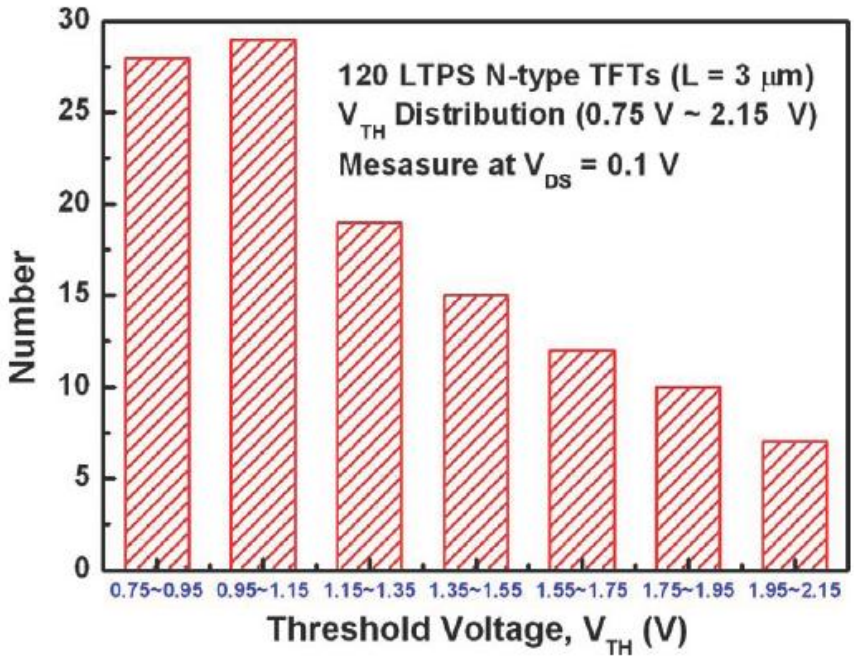


Fig. 1.15. Threshold voltage variation for n-type poly-Si TFTs in different locations on LCD panels.

Some properties such as hot carrier stress (HCS), negative bias temperature instability (NBTI), and reliability issues have been proved that the instability of polys-Si TFTs is more serious than that of single-crystal silicon transistors. Besides, the diverse and complicated

grain distribution in the poly-Si film, so poly-Si TFTs suffer serious variation of device behavior, especially in mobility and threshold voltage, which are two important features in the realization of on-panel circuit integration. Although using LTPS process can enlarge poly-grain size to improve the device performance, it usually accompanies a random device-to-device variation on LCD panel. The harmful effects of irregular grain boundaries, gate-insulator interface defects, and incomplete ion-doping activation in thin poly-silicon channels result in the variation on electrical characteristics of LTPS TFTs. The mobility degradation for n-channel TFTs is more serious at hot-carrier stress condition than that at on-current condition which means that the hot-carrier degradation dominates the mechanism for n-channel TFTs. Fig. 1.15 shows the threshold voltage variation for n-type TFTs in different locations on LCD panel. The variation of threshold voltage for LTPS n-type TFTs in different panel locations has wide distribution from 0.75 V to 2.15 V [20]-[22].

1.5. Organization of This Dissertation

The aforementioned design challenges of on-panel circuits for applications in display system form the motivation of this dissertation. The research topics of this dissertation including: (1) integrated gate driver with threshold voltage drop cancellation in amorphous silicon (a-Si) technology, (2) low power gate driver in a-Si technology for narrow bezel panel application, (3) analog pixel memory in low temperature poly silicon (LTPS) technology for low power display, (4) ESD protection design for 60GHz low noise amplifier (LNA) with inductor-triggered silicon-controlled rectifier (SCR) in 65nm CMOS process, and (5) dual-band ESD protection for 24/60 GHz millimeter-wave circuits.

In chapter 2, a new integrated gate driver on array (GOA) has been successfully designed and fabricated by amorphous silicon (a-Si) technology for a 3.8-inch WVGA (800xRGBx480) TFT-LCD panel. With the proposed threshold voltage drop cancellation technique, the output rise time of the proposed integrated gate driver can be substantially decreased by 24.6% for high resolution display application. In chapter 3, with utilizing four clock signals in the design of GOA, the pull-up transistor has ability for both output charging and discharging, and layout size of the proposed gate driver can be narrowed for bezel panel application. Moreover, lower duty cycle of clock signals can decrease static power loss to further reduce the overall power consumption of the proposed gate driver. The scan direction of the proposed gate driver can be adjusted by switching two direct control signals to present the reversal display of image. Additionally, the proposed gate driver has been successfully

demonstrated in a 4.5-inch WXGA (1440xRGBx800) TFT-LCD panel and passed reliability tests of the supporting foundry.

In chapter 4, two types of analog memory cells realized in 3μm LTPS technology are proposed to achieve low power application for thin film transistor liquid crystal displays (TFT-LCDs). By employing the inversion signal in the storage capacitor with complementary source follower, the frame rate to refresh the static image can be reduced from 60Hz to 3.16Hz with the output decay less than 0.1V under the input data from 1V to 4V. To further diminish threshold voltage drop from source follower structure, a compensation technique is implemented to the proposed analog memory cells.

In chapter 5, an SCR device assisted with an inductor is proposed to improve the turn-on efficiency for ESD protection. Besides, the inductor can be also designed to resonate with the parasitic capacitance of the SCR device at the selected frequency band for RF performance fine tuning. Experimental results of the ESD protection design with inductor-triggered SCR in a nanoscale CMOS process have been successfully verified at 60GHz frequency. To verify the RF characteristics and ESD robustness in the RF receiver, the inductor-triggered SCR has been applied to a 60GHz low-noise amplifier (LNA). In chapter 6, dual-band ESD protection cell is proposed for 24/60 GHz ESD protection. The proposed cell consisted of a diode, a silicon-controlled rectifier (SCR), a PMOS, and inductors. To verify the dual-band characteristics and ESD robustness for the RF receiver, the proposed ESD protection circuit had been applied to a 24/60 GHz low-noise amplifier (LNA). Measurement results present over 2.75kV human-body-model (HBM) ESD robustness with little RF performance degradation.

Chapter 7 summarizes the main results of this dissertation. Some suggestions for the future works are also addressed in this chapter.

Chapter 2

Integrated Gate Driver with Threshold Voltage Drop Cancellation in Amorphous Silicon Technology for TFT LCD Application

A new integrated gate driver has been successfully designed and fabricated by amorphous silicon (a-Si) technology for a 3.8-inch WVGA (480xRGBx800) TFT-LCD panel. With the proposed threshold voltage drop cancellation technique, the output rise time of the proposed integrated gate driver can be substantially decreased by 24.6% for high resolution display application. Moreover, the proposed noise reduction path between the adjacent gate drivers can reduce the layout area for slim bezel display. The transmittance brightness and contrast ratio of the demonstrated 3.8-inch panel show almost no degradation after the 500 hours operation under 70℃ and -20℃ conditions.

2.1. Background

In recent years, the consumer electronic devices with high resolution, light weight, narrow bezel, low cost, and low power consumption are gaining the popularity. Therefore, the integrated gate driver using amorphous silicon (a-Si) technology for the TFT-LCD has become the main stream due to the mature manufacturing, low-cost processing, and elimination of the gate driver ICs [23]–[34]. Nevertheless, design of the integrated gate driver encounters two main challenges which are the low field-effect mobility and the reliability issue under high voltage stress. In order to alleviate the low mobility restriction, the thousands micro-meter width of the main driving TFT is required to drive the gate line of the panel. However, it accompanies with a large parasitic capacitance inevitably. In addition, the reliability issue of the integrated gate driver is as well as a notable challenge. While a-Si TFT suffers long term high voltage stress, the defect-state creation in a-Si:H as well as the charge trapping at the interface of insulating and active layer will cause threshold voltage shifts to decrease the life time of the integrated gate driver [35]–[36].

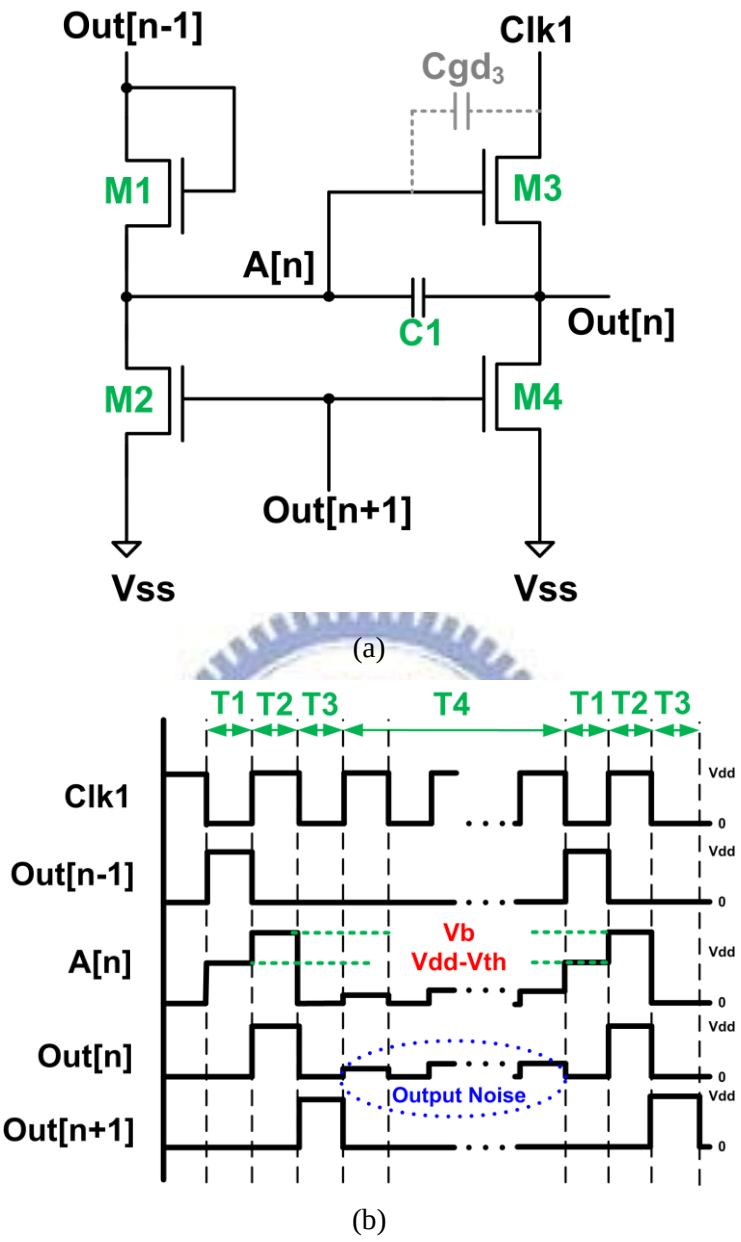


Fig. 2.1. (a) Schematic of the Thomson's shifter register circuit and (b) the corresponding control signals and outputs.

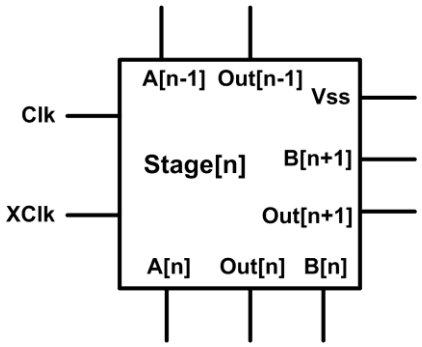
So far, a-Si integrated gate driver was originated from Thomson's shifter register which was composed of four transistors and one capacitor merely [24], [25]. Figs. 2.1(a) and 2.1(b) present the schematic and its corresponding control signals. In the T1 period, A[n] is pre-charged to Vdd-Vth through M1, where the Vth is the threshold voltage of M1 and [n] is the nth gate line of the panel. Subsequently, Clk1 becomes high and Out[n] is charged by M3. At this moment, A[n] is simultaneously boosted from Vdd-Vth to a higher voltage (Vb)

through C1. Out[n] represented the Vdd level in the T2 period. In the T3 period, M2 and M4 are turned on by the next output node (Out[n+1]) to discharge A[n] and Out[n]. The shifter register works repeatedly when voltage level of the previous output node (Out[n-1]) becomes high again. Therefore, Out[n] is floating during most of the frame time in the T4 period and output voltage is continuously coupled by Clk1 through the parasitic capacitance (Cgd3) to produce the output noise. For this reason, adding two transistors into Thomson's shifter register were proposed to form a noise reduction path to release output noise from clock coupling [27]. Nevertheless, it also led to a serious Vth shift for pull down TFTs since their operations were analogous to DC stress. To alleviate this effect, the manners of pull down TFTs operated alternately with the 50% duty cycle were proposed to reduce the stress effect [28], [29]. Besides, Choi et al. [30] reported the center-offset a-Si:H TFT which was utilized as pull-down TFTs in the integrated gate driver for higher reliability.

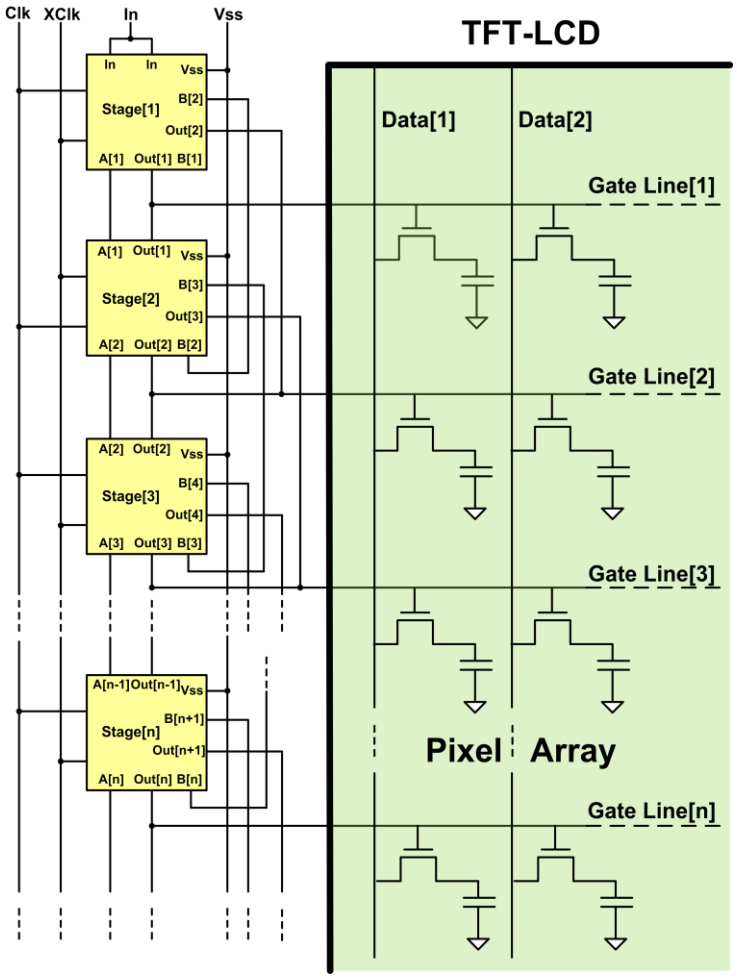
From the prior arts, the input transistor is mostly implemented by the circuit style of diode connection, similar as M1 in Fig. 2.1(a). Hence, A[n] is restricted to Vdd-Vth in the T1 period. The output rise time in the T2 period is thereby degraded due to the threshold voltage drop at A[n]. In this chapter, the proposed integrated gate driver uses the threshold voltage drop cancellation method to resolve the lower output rise time issue. Besides, the proposed noise reduction path between the adjacent gate drivers can reduce the layout area for slim bezel display.

2.2. Operation of Integrated Gate Driver with Threshold Voltage Drop Cancellation

The block diagram of the proposed integrated gate driver is shown in Fig. 2.2(a), which is composed of the input signals (A[n-1] and Out[n-1]), control signals (Clk and XClk), feedback signals (B[n+1] and Out[n+1]), and output signals (A[n], B[n], and Out[n]). Fig. 2.2(b) depicts the connections among the proposed integrated gate driver stages for TFT-LCD application. The block manipulation is activated while a start signal (In) inputs a high voltage level to Stage[1]. A pulse signal is subsequently generated at Out[1] and being acted as the start signal for Stage[2]. Accordingly, sequential pulse signal can be periodically transferred stage by stage for feeding the whole gate lines of the pixel array in TFT-LCD.

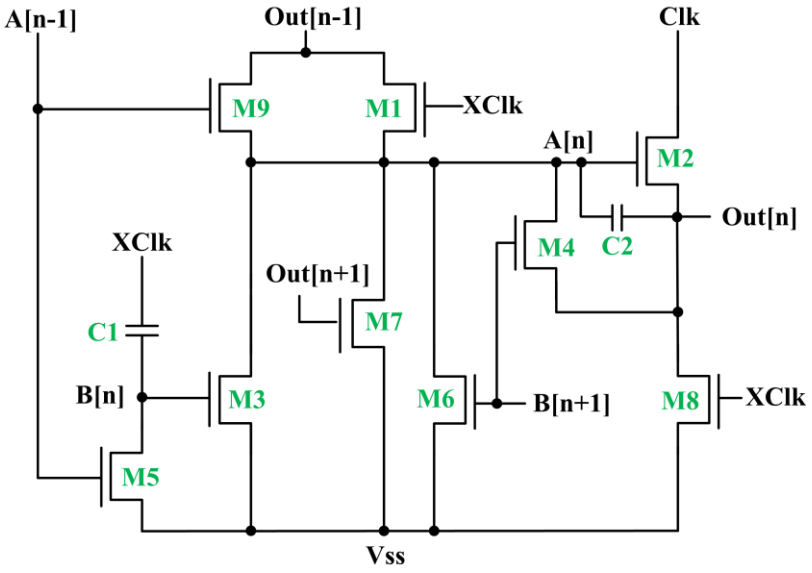


(a)

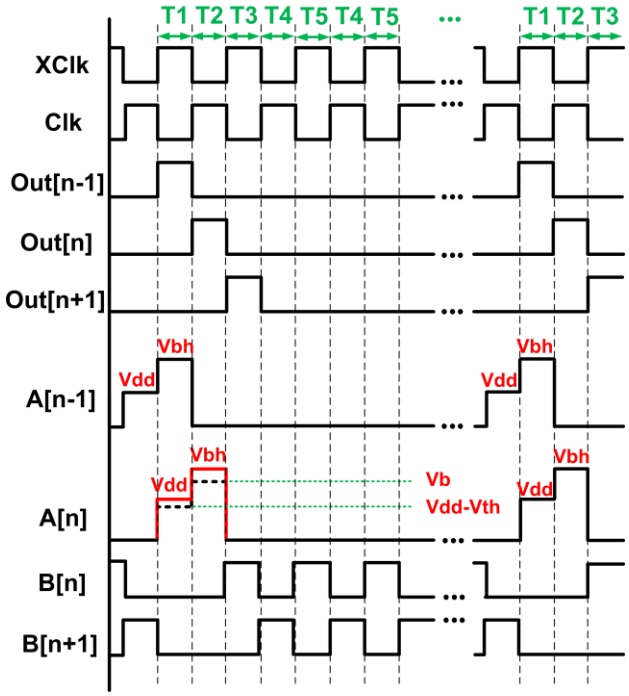


(b)

Fig. 2.2. (a) The block diagram and (b) the connections between stages of the proposed integrated gate drivers for TFT-LCD application.



(a)



(b)

Fig. 2.3. (a) The schematic diagram and (b) the corresponding operation waveforms of the proposed integrated gate driver.

Fig. 2.3(a) presents the schematic diagram of the proposed integrated gate driver with its corresponding waveforms in Fig. 2.3(b). The high and low voltage levels in Fig. 2.3(b) are defined as Vdd and Vss, respectively. The operation can be divided into five periods, T1, T2, T3, T4, and T5. In the T1 period, M1, M8, M5, and M9 are turned on by XClk and A[n-1]. The other transistors are turned off. At this moment, Out[n] is Vss through M8 and A[n] is

charged by M1 and M9. Because M1 is operated in saturation region (diode connection), the threshold voltage drop (Vdd-Vth) will be applied at A[n]. Nevertheless, M9 is operated with its gate voltage of Vbh, which is larger than Vdd in the T1 period, so A[n] is charged to Vdd through M9 to avoid the threshold voltage drop. Therefore, the node voltages of A[n] and Out[n] are Vdd and Vss at the end of this period. The design of M9 is utilized to cancel the threshold voltage drop as compared with the previous works using the diode connection (M1) merely.

In the T2 period, M1, M8, M5, and M9 are turned off by XClk and A[n-1]. Clk becomes high voltage level and then Out[n] is charged by M2. At this moment, A[n] is boosted through C2 from Vdd to a higher voltage level which is labeled as Vbh in Fig. 2.2(b). The current can be derived from the linear region of M2 and depicted as [10]

$$I_{M2} = K\frac{W}{L}(A[n]-Out[n]-Vth)^{\alpha-1}(Vdd-Out[n]) \tag{2.1}$$

where K and α are the process dependent parameters, and W/L is the aspect ratio of M2. Since I_{M2} is proportional to the A[n], higher A[n] leads to larger output charging current. Consequently, the output rise time of the proposed integrated gate driver can be substantially decreased due to larger IM2. In the T3 period, M1 and M8 are turned on by XClk. M3 and M7 are turned on by B[n] and Out[n+1]. The other transistors are all keep at off state. At this period, A[n] and Out[n] are discharged to Vss by M3, M7, and M8. M1 is as a feedback path from Stage[n] to Stage[n-1] to speed up the discharging process.

After the T3 period, it leads to the T4 and T5 alterative transition periods until Out[n-1] becomes high voltage level again. In these two periods, the output fluctuation noise induced by the clock transition (Clk and XClk) must be diminished to ensure the output with a constant voltage level (Vss). Therefore, an approach of sharing the noise reduction path between the adjacent gate drivers is proposed and shown in Fig. 2.4.

During the T4 period, M4 and M6 in Stage[n] are series connected with M1 and M3 in Stage[n+1] to form a discharging path (dash line) for settling A[n-1] and Out[n-1] to Vss. Similarly, M1 and M3 in Stage[n] are series connected with M4 and M6 in Stage[n-1] to form the other path (solid line) in the T5 period. Consequently, the noise is intensely minimized since both A[n] and Out[n] are discharged to Vss in the T4 and T5 periods. Besides, the layout area can be constructed with miniature size due to the sharing of the proposed noise reduction paths between the adjacent gate drivers.

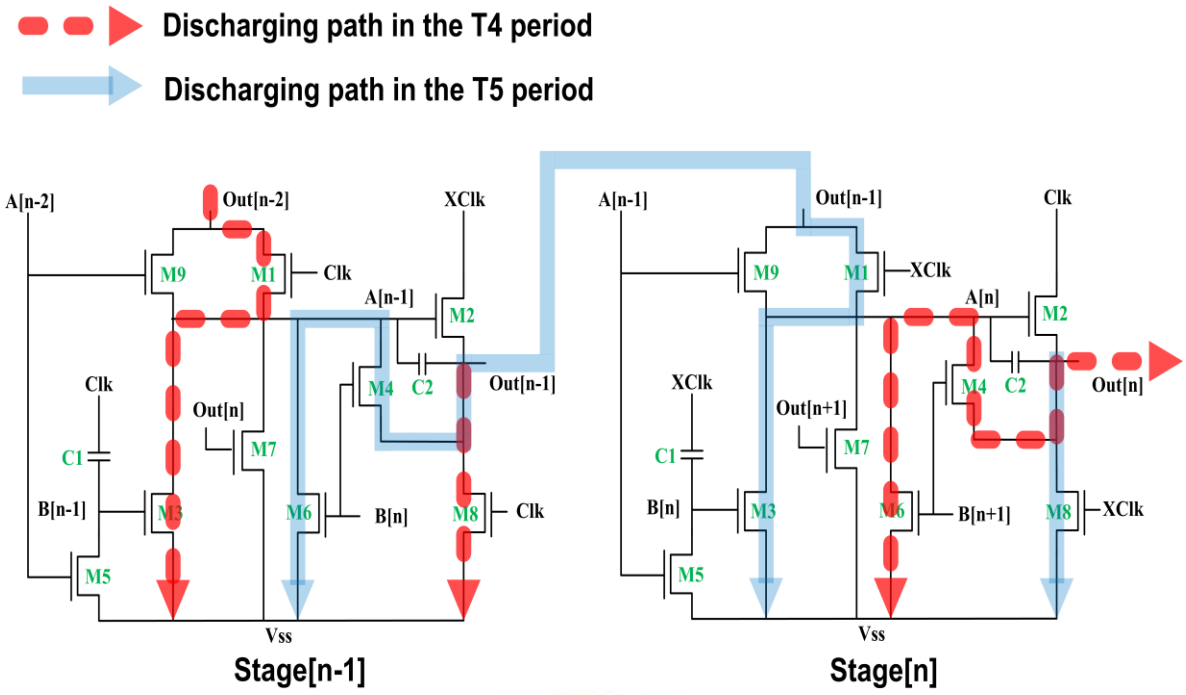


Fig. 2.4. Discharging paths between two adjacent stages in the T4 and T5 periods.

2.3. Experimental Results and Discussion

2.3.1. Simulation Results of the Proposed Integrated Gate Driver

The proposed integrated gate driver was designed and verified by HSPICE simulation with the RPI a-Si TFT model (Level=61) provided by the foundry. The field-effect mobility and threshold voltage of a-Si TFT are 0.369cm^2/V·s and 4.019V, respectively. The widths of M2 and M8 of the proposed integrated gate driver are designed with thousands micrometer for the faster speed in a few microsecond to pull up and down the output loading of oscilloscope. Although the lager widths of M2 and M8 can reinforce output charging and discharging speed, these accompany with larger parasitic capacitances which decrease the boosted voltage of A[n] (Vbh-Vdd in Fig. 2.3(b)) to further reduce the output charging speed [12]. Furthermore, the clock induced output noise of the integrated gate driver also becomes severely from larger parasitic capacitance [37]. The trade-off between speed and parasitic effects should be explicitly concerned during the design of the integrated gate driver. Therefore, the device parameters (channel width (W) to channel length (L) aspect ratio and capacitance) of the proposed integrated gate driver are indicated in Table 2.1 with the output loading (oscilloscope) of one capacitor (17pF) in parallel with one resistor (10MΩ). The input signals are composed of start (In), clock (Clk and XClk), and ground (Vss) signals with voltage levels from 25V to 0V. Besides, the duty cycle of the start and clock signals are 16.6ms and 80μs, respectively. The timing settings are according to the conventional frame

time 16.6ms (60Hz) and 400 row numbers of a TFT-LCD panel.

Fig. 2.5 illustrates the simulated output waveforms of the proposed integrated gate driver from the first to the fourth stage. Sequential pulse signals have been successfully observed in Fig. 2.5 to verify the output function of the proposed integrated gate driver. The rise time, fall time, and noise root mean square (RMS) voltage are represented in Table 2.2, where the rise and fall times are defined by the time difference between 10% to 90% pulse voltage levels, the noise RMS is the root mean square voltage of Out[n] in the T4 and T5 periods.

Table 2.1

Device Parameters of the Proposed Integrated Gate Driver

TFT aspect ratio W/L (μm/μm)			
M1	300/3	M6	150/3
M2	4000/3	M7	500/3
M3	100/3	M8	2000/3
M4	150/3	M9	100/3
M5	100/3		
Capacitance (pF)			
C1	4	C2	3

Table 2.2 presents that the rise times of Out[2], Out[3], and Out[4] are rapider than that of Out[1] (1.775μs) which can be simpler figured out through the transient waveforms of A[1] and A[2] in Fig. 2.6. Since the Stage[1] does not have the feedback signal (Vbh in Fig. 2.3(b)) from the previous stage, the voltage difference between A[1] and A[2] is about 3.56V, as derived from Eq. (2.1), A[n] is proportional to the charging current of M2, so Out[1] has longest rise time than that of other stages. With the proposed threshold voltage drop cancellation method, the rise time of the proposed integrated gate driver can be substantially decreased about 16%. Therefore, the first stage of the proposed integrated gate driver has to be set as a dummy stage to avoid the larger output rise time issue for panel integration.

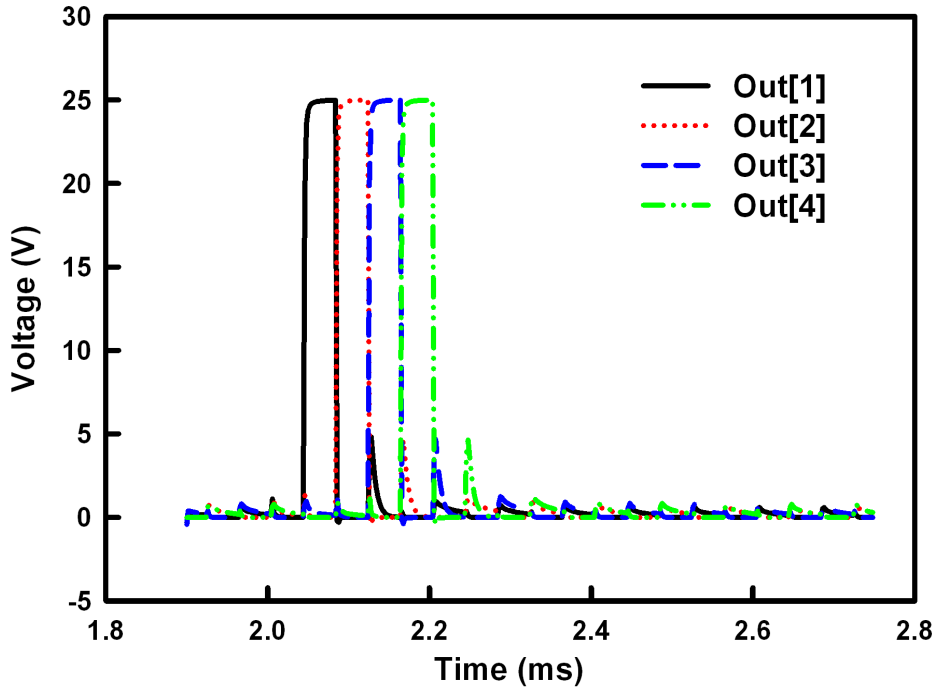


Fig. 2.5. The simulated output waveforms of the proposed integrated gate driver from the first to the fourth stages.

Table 2.2 presents that the rise times of Out[2], Out[3], and Out[4] are rapider than that of Out[1] (1.775μs) which can be simpler figured out through the transient waveforms of A[1] and A[2] in Fig. 2.6. Since the Stage[1] does not have the feedback signal (Vbh in Fig. 2.3(b)) from the previous stage, the voltage difference between A[1] and A[2] is about 3.56V, as derived from Eq. (2.1), A[n] is proportional to the charging current of M2, so Out[1] has longest rise time than that of other stages. With the proposed threshold voltage drop cancellation method, the rise time of the proposed integrated gate driver can be substantially decreased about 16%. Therefore, the first stage of the proposed integrated gate driver has to be set as a dummy stage to avoid the larger output rise time issue for panel integration. Furthermore, the issue of higher noise RMS decreases the holding capability of pixel array which will reduce the image quality of the panel. Table 2.2 depicts that the noise RMS values of the proposed integrated gate driver from Out[1] to Out[4] are comprehensively less than 0.13V that is much lower than the requested specification (0.5V) from the foundry. Consequently, these simulation results successfully confirm the proposed noise reduction path between the adjacent gate drivers which has lower noise RMS to be capable of panel integration.

Table 2.2

Simulated Results of the Proposed Integrated Gate Driver

	Rise time (μs)	Fall time (μs)	Noise RMS (V)
Out[1]	1.775	0.481	0.104
Out[2]	1.472	0.409	0.113
Out[3]	1.518	0.432	0.106
Out[4]	1.526	0.448	0.124

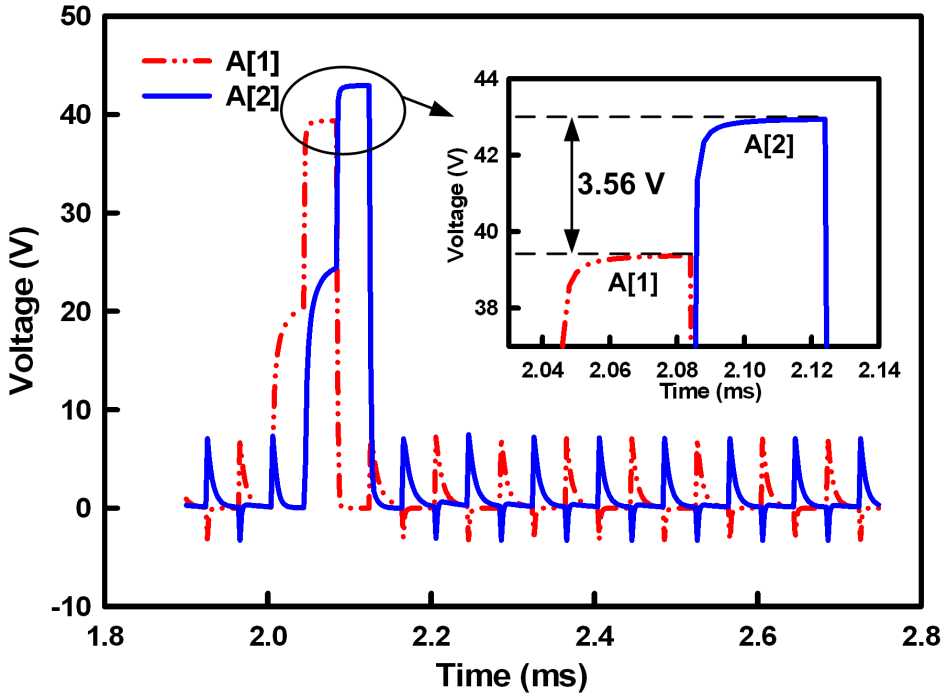
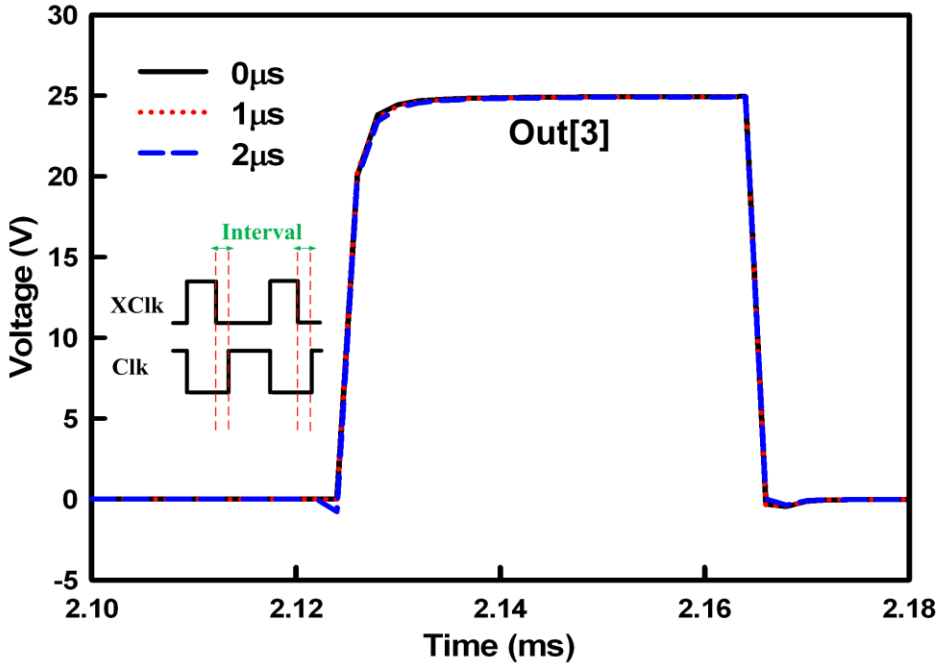


Fig. 2.6. The transient waveforms of A[1] and A[2] show the proposed integrated gate driver without (A[1]) and with (A[2]) threshold voltage drop cancellation method.

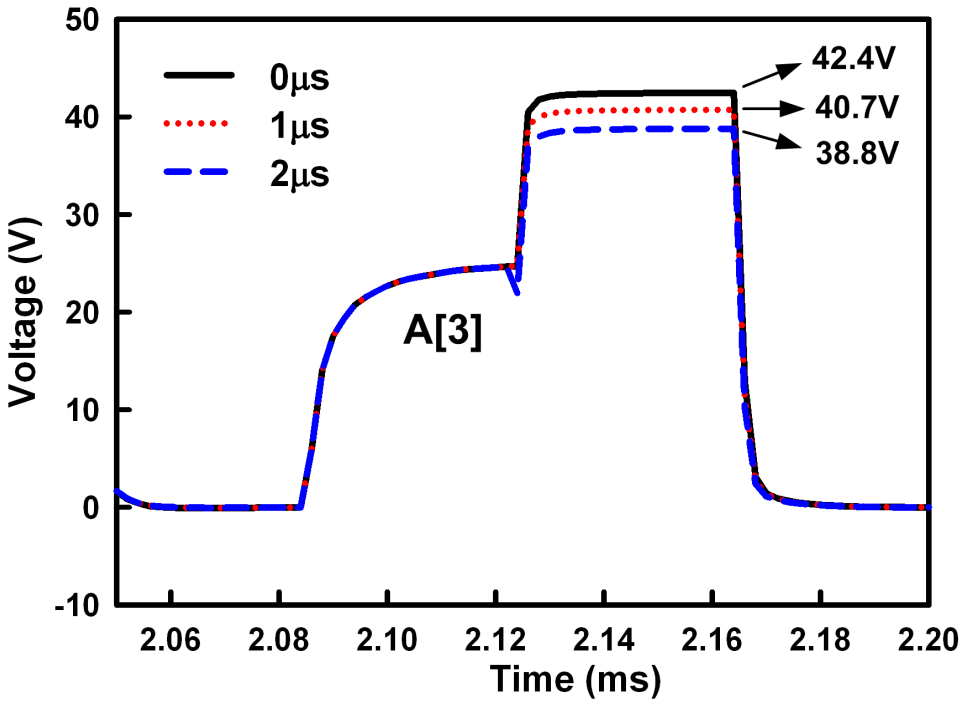
The discussions for a shortcoming of the proposed integrated gate driver are presented when it is applied to non-overlapping gate pulses, which has been proposed to prevent crosstalk between adjacent rows. For this reason, timing intervals between the falling edge of XClk and rising edge of Clk (both Clk and XClk are 0V) are varied to simulate the cases of overlapping and non-overlapping gate pulses. Fig. 2.7 depicts the simulated waveforms of the proposed integrated gate driver under three timing intervals (0μs, 1μs, and 2μs). As derived from Fig. 2.7(a), the output rising time is degraded from 1.518μs (0μs) to 1.88μs (2μs), and A[3] is also decreased from 42.4V (0μs) to 38.8V (2μs) in Fig. 2.7(b). These can be explained

that when Xclk goes low (after precharging A[3]) in the T2 period, A[3] will discharge through M9 because A[2] is still high, and this will reduce the overdrive of M2 when Clk eventually goes high. Therefore, M9 can provide additional drive and also be responsible for degrading the drive under the case of non-overlapping gate pulses. Furthermore, noise RMS is also increased from 0.106V (0μs) to 0.31V (2μs), that larger timing interval will diminish the noise reduction durations in the T4 and T5 periods, and thereby the lager noise RMS is revealed.

Since stabilities of a-Si TFTs are crucial factors for the integrated gate drivers, the following simulation results still show the proposed integrated gate driver that has highly reliability even under the case of 2μs interval for non-overlapping gate pulses. Fig. 2.8 shows the simulation results of A[1] and A[3] (a) before and (b) after all the a-Si TFTs in the proposed integrated gate driver are suffering from 3V threshold voltage shifts [38]. As shown in Fig. 2.8(a), A[1] (39.5V) has lager value than A[3] (38.8V), and the output rise times are 1.77μs (Out[1]) and 1.88μs (Out[3]) respectively, which seem to present that M9 is unnecessary for the integrated gate driver under the case of 2μs interval. Nonetheless, after all the a-Si TFTs in the proposed integrated gate driver are suffering from 3V threshold voltage shifts, Fig. 2.8(b) depicts that A[1] (36.9V) has lower value than A[3] (40.9V), and the output rise times are 3.24μs (Out[1]) and 1.96μs (Out[3]). The degradation rates of rise time of Out[3] and Out[1] are 4.3% and 45.4%, and these can be referred from the previous statements about M9. Although it can be responsible for degrading the drive under the case of non-overlapping gate pulses, when M9 suffers bias stress induced threshold voltage shifts, the discharging current through M9 is decreased, and it shows that A[3] has higher voltage from 38.8V to 40.9V in Fig. 2.8. Consequently, the proposed threshold voltage drop cancellation method is quite suitable for long term operation as compared with prior arts even under the case of 2μs interval.

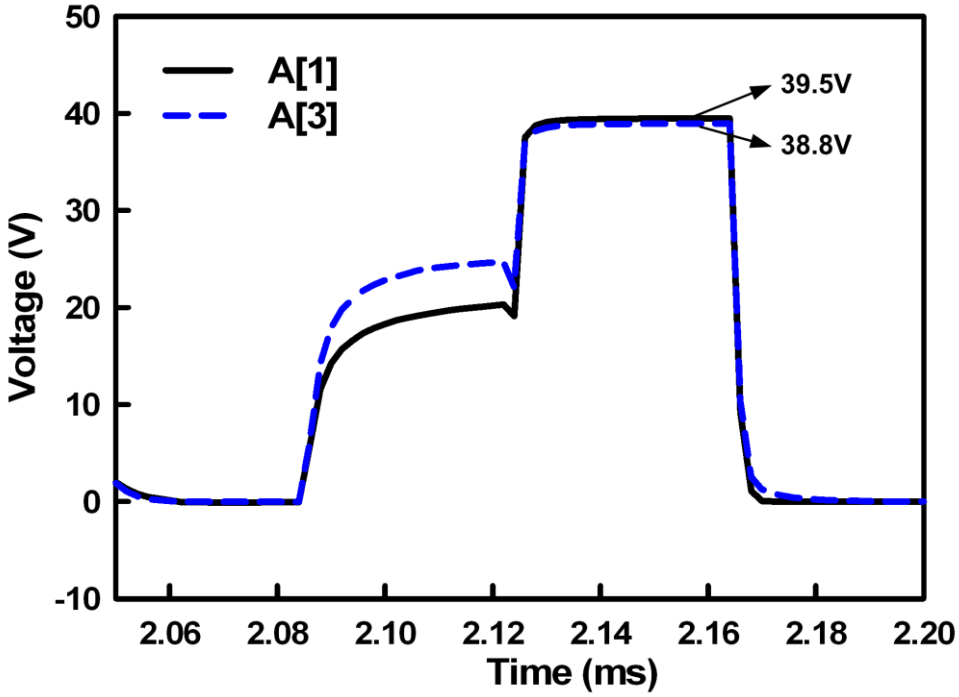


(a)

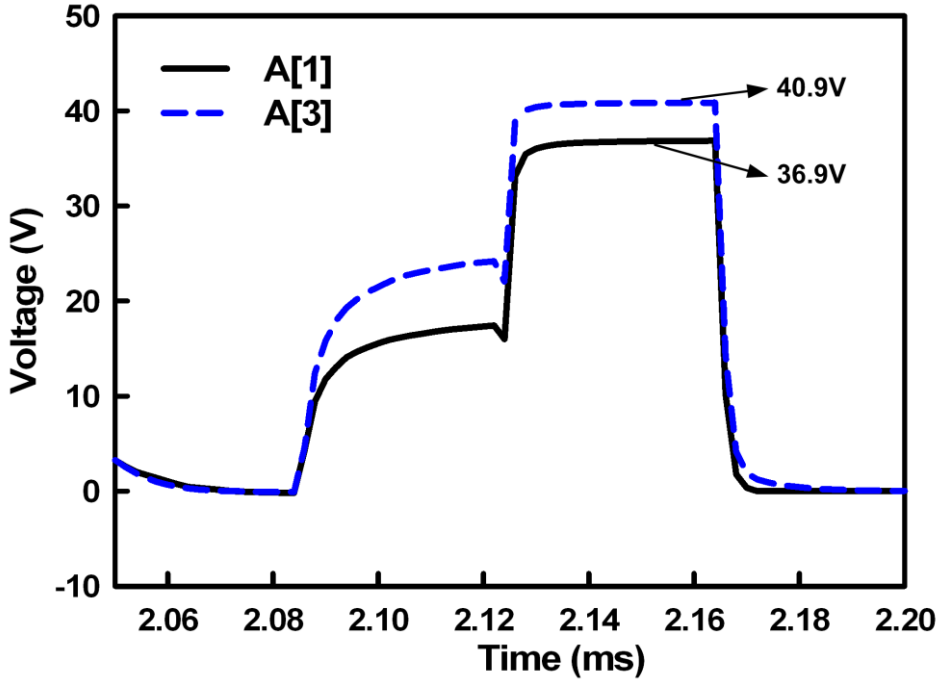


(b)

Fig. 2.7. The simulated (a) Out[3] and (b) A[3] waveforms of the proposed integrated gate driver under three timing intervals (0μs, 1μs, and 2μs).



(a)

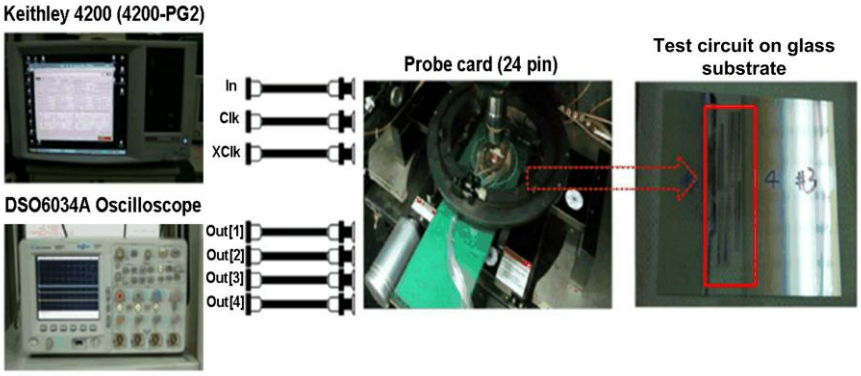


(b)

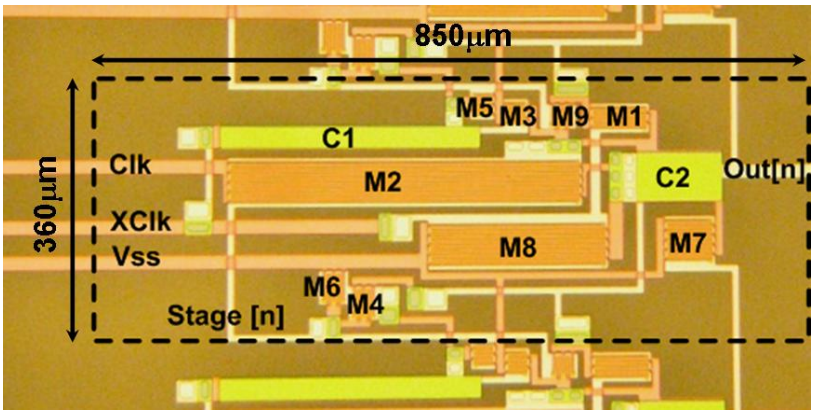
Fig. 2.8. The simulation results of A[1] and A[3] (a) before and (b) after all the a-Si TFTs in the proposed integrated gate driver are suffering from 3V threshold voltage shifts.

2.3.2. Measurement Results of the Proposed Integrated Gate Driver

For array verification, one hundred integrated gate driver stages realized with the proposed threshold voltage drop cancellation method are manufactured on glass substrate in amorphous silicon technology. As shown in Fig. 2.9(a), the measurement setups depict that the synchronous control signals (Clk, XClk, and In) are generated by the pulse card option for Keithley 4200 (4200-PG2), and the input range are set as 0V to 25V. Furthermore, digital oscilloscope is utilized to observe the output waveforms. The equivalent loading of its probes is one capacitor (17pF) in parallel with one resistor (10MΩ) which is equal to the simulation environment. Moreover, the probe card with 24 pins is applied for the connections between fabricated circuit and measurement equipments. Fig. 2.9(b) presents the die photo of the proposed integrated gate driver. Because the widths of M2 and M8 are designed with thousands micrometer for pulling up and down the output node (Out[n]), the larger layout area is occupied by M2 and M8 in Fig. 2.9(b).



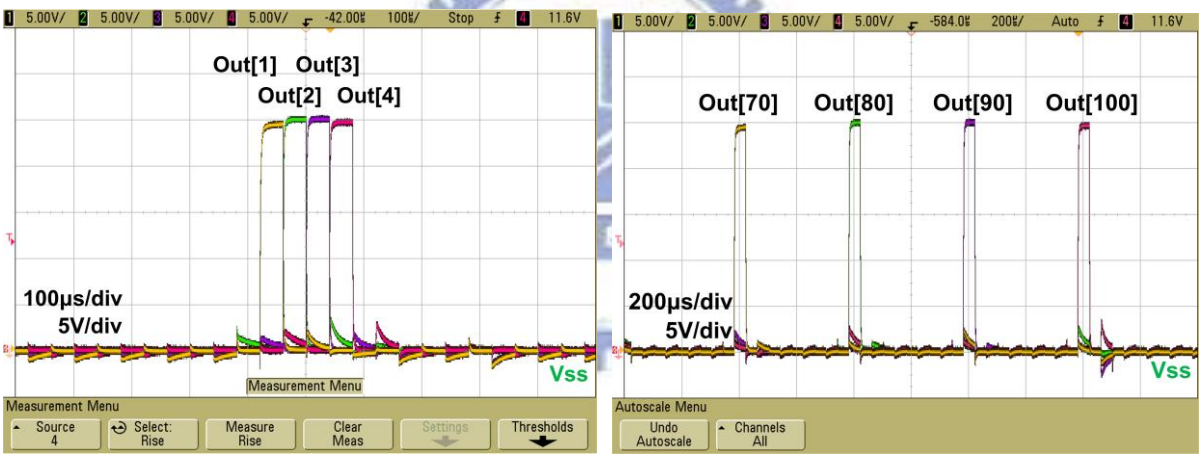
(a)



(b)

Fig. 2.9. (a) The measurement setups and (b) the die photo of the proposed integrated gate driver for array testing.

Fig. 2.10(a) shows the measured output waveforms of the proposed integrated gate driver from the first to fourth stages (Out[1], Out[2], Out[3], and Out[4]). In addition, Out[70], Out[80], Out[90], and Out[100] are shown in Fig. 2.10(b). The rise time, fall time, and noise RMS of Fig. 2.10(a) are represented in Table 2.3. As shown in Table 2.3, the rise time results of Out[2], Out[3] and Out[4] are rapider than Out[1] (2.32μs) about 24.6%. With the threshold voltage drop cancellation method, the decreasing of 24.6% on rise time has been successfully verified and it is compatible with the simulation results in Table 2.2. Besides, the noise RMS values are less than 0.32V to further determine the proposed noise reduction path between the adjacent gate drivers with lower noise RMS to be capable for panel integration. These results demonstrate that the proposed integrated gate driver has faster output charging speed and lower output fluctuation with fine layout area by using the threshold voltage drop cancellation method and sharing noise reduction path between the adjacent gate driver stages.



(a) (b)

Fig. 2.10. The measured output waveforms of the proposed integrated gate driver at the outputs of (a) Out[1], Out[2], Out[3], Out[4], and (b) Out[70], Out[80], Out[90], Out[100].

Table 2.3

Measurement Results of the Proposed Integrated Gate Driver

	Rise time (μs)	Fall time (μs)	Noise RMS (V)
Out[1]	2.32	1.41	0.318
Out[2]	1.68	1.21	0.28
Out[3]	1.75	1.12	0.25
Out[4]	1.67	1.17	0.278

2.3.3. Panel Integration in a 3.8-inch WVGA Panel

A 3.8-inch WVGA panel has been fabricated with the proposed integrated gate driver, and its specification is summarized in Table 2.4. The resolute ion of the panel is 480xRGBx800 with the contrast ratio of 350:1. Besides, the frame rate and back light brightness are 60Hz and 4500cd/m^2, respectively. Fig. 2.11 presents the photo of the proposed integrated gate drivers that are allocated at the both sides of pixel array in a 3.8-inch WVGA panel. The layout area of each stage is 207μmx900μm under the layout optimization.

Table 2.4

The specification of a 3.8-inch WVGA panel

	Specification
Panel size	3.8" diagonal
Resolution	480*RGB*800
Frame rate (Hz)	60
Pixel pitch (μm*μm)	103.5*103.5
Pixel density (ppi)	0.051
Back light brightness (cd/m^2)	4500
Contrast ratio	350:1
Integrated gate driver cell area (μm*μm)	207*900

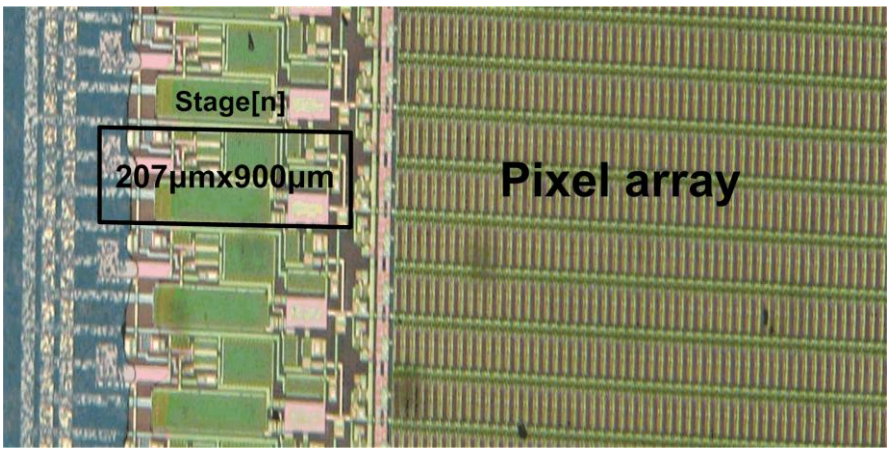
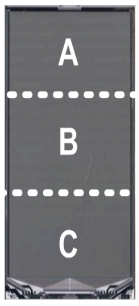


Fig. 2.11. The photo of the proposed integrated gate drivers that are allocated at the both sides of pixel array in a 3.8-inch WVGA panel.

Fig. 2.12. The display image of a 3.8-inch WVGA panel without the color filter cell.

Fig. 2.12 shows the display image of a 3.8-inch WVGA panel without the color filter cell. The average transmission brightness is 527cd/m^2 under the back light brightness of 4500cd/m^2, and the average contrast ratio is 353 in the demonstrated panel. For reliability (RA) testing, Fig. 2.13 and Fig. 2.14 show the contrast ratio and transmittance brightness of the demonstrated panel before and after 500 hours operating under 70℃ and -20℃ conditions at different panel locations (A, B, and C).

	Location A	Location B	Location C	Average
Before RA	365	358	335	353
-20ºC, 500hr	420	418	422	420
70ºC, 500hr	437	404	330	390



3.8-inch panel

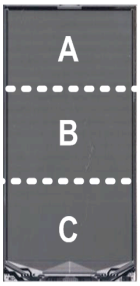
Fig. 2.13. Contrast ratio of the fabricated panel before and after 500 hours operating at different panel locations (A, B, and C).

Fig. 2.13 shows the average contrast ratio of the demonstrated 3.8-inch panel which is from 353 to 390 (70℃) and 420 (-20℃) after RA testing. Since these show the average contrast ratio that is not degraded after RA testing, the superior reliability of the proposed integrated gated driver is manifested. However, the larger variations before and after RA

testing could be as results of the definition of the contrast ratio, the ratio of the luminance of the brightest color (white) to the darkest color (black), which depicts that the luminance of the darkest color varies slightly to further prompt the contrast ratio with larger variation.

Unit: cd/m^2

	Location A	Location B	Location C	Average
Before RA	525	531	524	527
-20ºC, 500hr	501	527	516	515
70ºC, 500hr	514	503	508	508



3.8-inch panel

Fig. 2.14. Transmission brightness of the fabricated panel before and after 500 hours operating at different panel locations (A, B, and C).

Fig. 2.14 represents the average transmittance brightness which is from 527cd/m^2 to 508cd/m^2 (70℃) after RA testing. The decay rate is only less than 3.61% for passing the production standard of the foundry, where the decay rate is defined by the difference value of average transmittance brightness (527-508=19) divided the value before RA testing (527). In summary, these results have completely verified the proposed integrated gate driver with good reliability for high resolution panel integration.

2.4. Summary

An integrated gate driver with highly output charging speed has been successfully fabricated in amorphous silicon technology for a 3.8-inch WVGA panel. The output rise time of the proposed integrated gate driver is dramatically reduced about 24.6% by using the threshold voltage drop cancellation method. For panel reliability testing, the decay rate of transmittance brightness for the demonstrated 3.8-inch panel implemented with the new proposed integrated gate drivers represents less than 3.61%, and the contrast ratio shows almost no degradation after the operating of 500 hours under 70℃ and -20℃ conditions. The proposed gate driver is quite appropriate for integration into to the high resolution TFT-LCD panels.

Chapter 3

Low Power Gate Driver in Amorphous Silicon Technology for Narrow Bezel Panel Application

A new gate driver has been designed and fabricated by amorphous silicon (a-Si) technology. With utilizing four clock signals in the design of gate driver on array (GOA), the pull-up transistor has ability for both output charging and discharging, and layout size of the proposed gate driver can be narrowed for bezel panel application. Moreover, lower duty cycle of clock signals can decrease static power loss to further reduce the overall power consumption of the proposed gate driver. The scan direction of the proposed gate driver can be adjusted by switching two direct control signals to present the reversal display of image. The proposed gate driver has been successfully demonstrated in a 4.5-inch WXGA (1440xRGBx800) TFT-LCD panel and passed reliability tests of the supporting foundry.

3.1. Background

A variety of portable electronic devices have been introduced with small displays such as cellular phone and PDA (Personal Digital Assistants). Displays for portable electronic devices require high resolution, light-weight, and low power consumption. Therefore, the integrated gate driver using a-Si technology for the TFT-LCD has become the main stream due to the mature manufacturing, low-cost processing, and elimination of the gate driver ICs [39]-[47]. Nevertheless, design of the integrated gate driver by a-Si encounters three main challenges which are the low field-effect mobility, low reliability issue under high voltage stress, and the lack of P-type transistor. In order to alleviate the low mobility restriction, the thousands micro-meter width of the main driving TFT is required to drive the gate line of the panel. But the large parasitic capacitance affects the performance of circuit. In addition, the reliability issue of the integrated gate driver is as well as a notable challenge. While a-Si TFT suffers the DC-bias shift which results from charge trapping and defect creation leads to shorten the life time of the integrated driver [18], [19]. Besides, the structure of a-Si gate driver using only N-type transistor increase the difficulty of design for panel application.

So far, a-Si integrated gate driver was originated from Thomson's shifter register which was made up of four transistors and one capacitor merely [24], [25], and many methods have been developed to improve the circuit [39]-[47]. The circuit style of diode connection degrades the output rise time due to the threshold voltage drop on gate voltage of pull-up transistor, hence chapter 2 proposed a high rising time gate driver with a threshold voltage drop cancellation technique that decreases output rise time by 24.6% for high resolution display application [48]. However, the switching times of clock signals (Clk and XClk) with 50% duty cycle and large size of pull-up and pull-down transistors in chapter 2 caused high power consumption. Besides, Chun et al. [49] developed the bidirectional gate driver circuit with a-Si:H technology to change direction of vertical scan depending on the polarity of two control signals. Furthermore, Lin et al. [31] proposed a bidirectional gate driver circuit using the carrier buffer TFT to select the direction of transfer and does not suffer from the shift in the threshold voltage. In this chapter, the pull-up transistor is designed to has ability for both output charging and discharging with low duty cycle (25%) clock signals in proposed gate driver circuit, and the parasitic capacitances and layout size of gate driver are be narrowed for bezel panel application. Moreover, lower duty cycle of clock signals can decrease static power loss to further reduce the overall power consumption of the proposed gate driver. Besides, high performance bidirectional gate driver circuit is designed by simply switching two direct controlling signals with size reducing. The reversal display of image can easily be presented in proposed gate driver by only exchanging the polarity of control signals.

3.2. Operation of Low Power Gate Driver in Amorphous Silicon Technology

3.2.1. Low power Gate Driver for Single-Direction Scanning

The block diagram of the proposed low power integrated gate driver circuit is shown in Fig. 3.1(a), which is composed of the input signals (Out[n-2] and Out[n-1]), control signals (Clk1 and Clk3), feedback signal (Out[n+2]), and output signal (Out[n]). Fig. 3.1(b) depicts the connections among the proposed low power integrated gate driver circuit stages for TFT-LCD application. The block manipulation is activated while start signals (In1 and In2) input a high voltage level to Stage[1]. A pulse signal is subsequently generated at Out[1] and being acted as one of start signals for Stage[2]. Accordingly, sequential pulse signal can be periodically transferred stage by stage for feeding the whole gate lines of the pixel array in TFT-LCD.

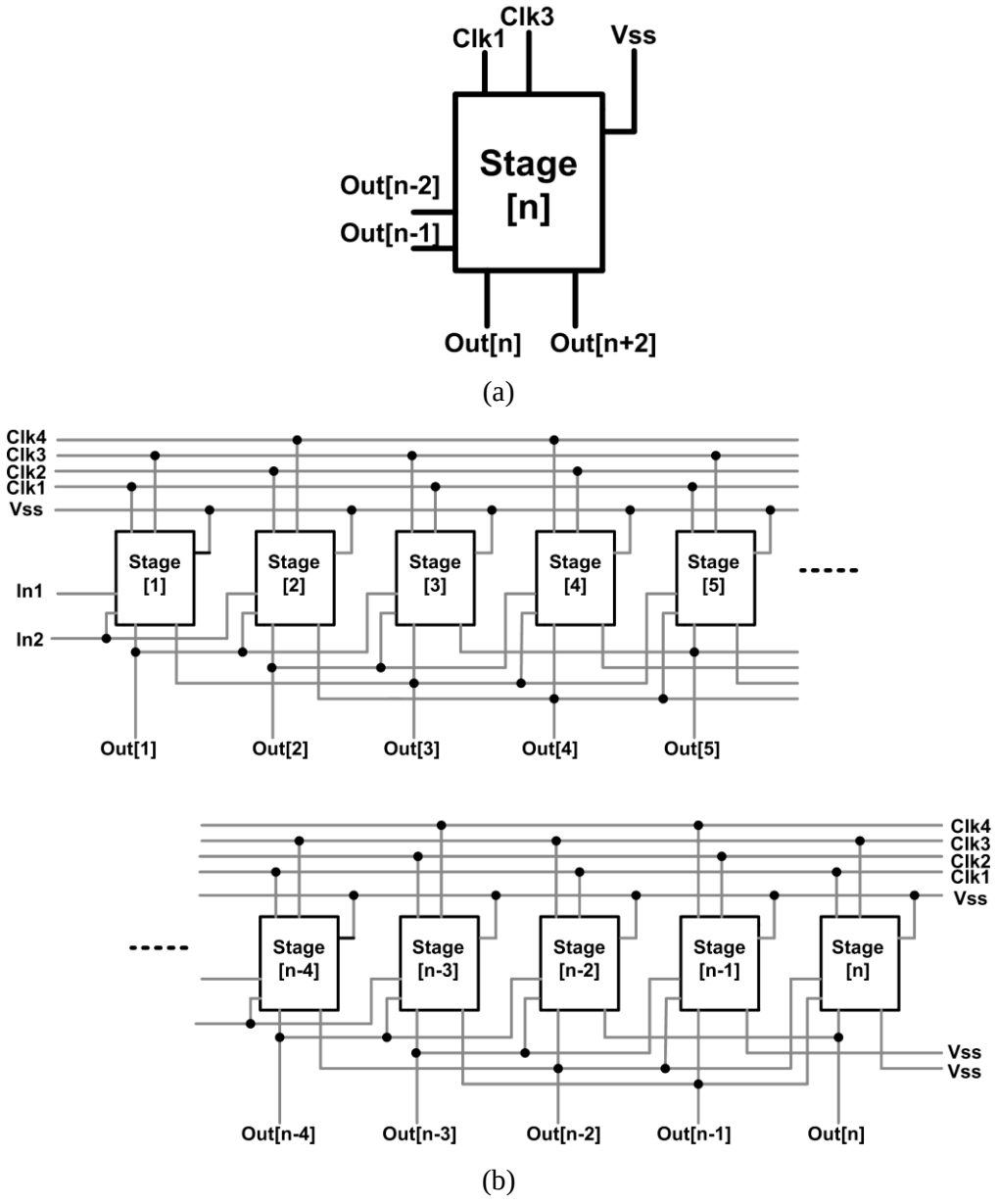


Fig. 3.1. (a) The block diagram and (b) the connections between stages of the proposed circuit for TFT-LCD application.

Fig. 3.2(a) presents the schematic diagram of the proposed low power integrated gate driver with its corresponding waveforms in Fig.3.2(b). The high and low voltage levels in Fig. 3.2(b) are defined as Vdd and Vss, respectively. Moreover, for the proposed circuit, the four clock signals have different phases and the duty of each clock signal is 25%. The operation can be divided into nine periods noted from T1 to T9. In the T1 period that Clk3 is high, M2, and M4 are turned on by Out[n-2] and Clk3. The other transistors are turned off. At this moment, Out[n] is Vss through M4 and A[n] is charged by M2. Next, in the T2 period, only

M1 is turned on and others are turned off. The A[n] is charger higher due to the second time charging. At the meanwhile, the Out[n] is still connects to Vss because of the on state of M3. After two periods of charging at A[n], the final voltage is completely charge to Vdd-Vth.

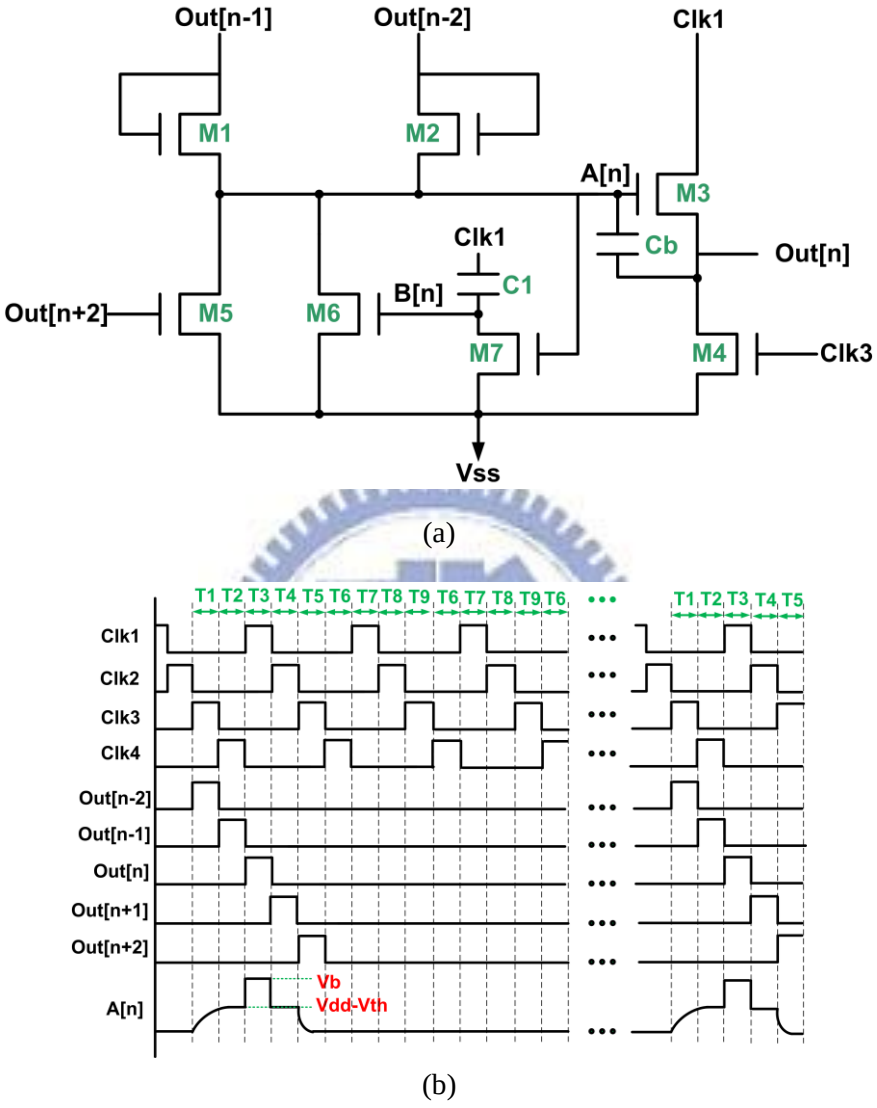


Fig. 3.2. (a) The schematic and (b) the corresponding operation waveforms of proposed circuit.

In the T3 period, M1, M2, M4, and M5 are turned off by Out[n-1], Out[n-2], Clk3, and Out[n+2]. Clk1 becomes high voltage level and then Out[n] is charged by M3. At this moment, A[n] is boosted through Cb from Vdd-Vth to a higher voltage level which is labeled as Vb in Fig. 3.2(b). The high A[n] provides M3 charging Out[n] with large current which is relative to the width of M3 as well. On the other hand, M6 turns on slightly at the transient of Clk1 from Vss to Vdd. However, this turn on process is swift and turned off immediately because of M7 connects to high voltage (A[n]) previously.

In the T4 period, all the TFTs and voltages maintain their last state except the Out[n] discharges because Clk1 is low in this period as well as A[n] decreases to Vdd-Vth caused by coupling from the capacitor Cb. In other words, M3 is the main role for charging and discharging as shown in Fig. 3.3, the width of M4 is narrowed and the layout of the proposed gate driver can be constructed with miniature size. Then, in T5 period, M4 and M5 are turned on by Clk3 and Out[n+2]. Others keep at off states and A[n] is discharged to Vss and Out[n] is maintaining at Vss because of M4. Although the discharge capacity of M5 is not strong enough, the speed of discharge doesn't influence the operation because Clk1 is at low voltage which is connected to Out[n] while A[n] is at high voltage. The steps of delivering a gate line pulse at Stage[n] complete the remaining operation periods are used for the noise immunity.

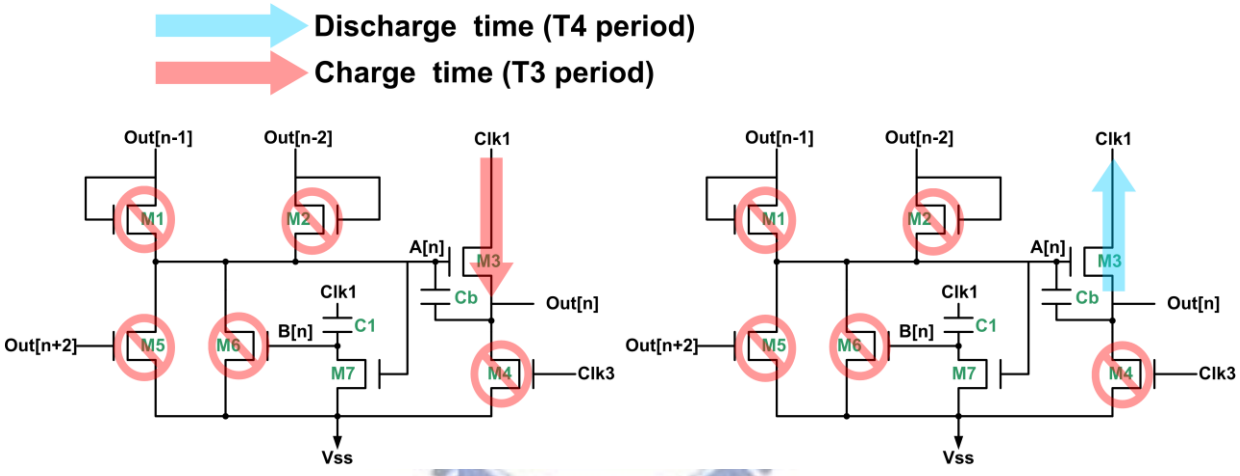


Fig. 3.3. The charge and discharge path by M3 for proposed circuit.

In T6 period, the Stage[n] is stationary, A[n] and Out[n] are kept at low voltage. Next period, T7, which Clk1 is high and results in noise, the A[n] is coupled by Clk1 through parasitic capacitances and results in charging at Out[n]. At meanwhile, M6 is used for eliminating the noise at A[n]. The Clk1 couples through C1, which is large enough to get high couple voltage at B[n], and M6 is turned on by B[n] so as to discharge the disturbance at A[n]. In the T8 period, the Clk1 transits from high to low voltage level at the beginning of this period. The variation is coupled to A[n] and affects Out[n], this makes voltages of A[n] and Out[n] become slightly negative. Finally, in T9 period, M4 is turned on by Clk3 and then connects Out[n] with Vss, and Out[n] is stable at low voltage level. Concequently, the following periods replicate the steps from T6 to T9 orderly until the next start signals (In1 and In2) come up.

3.2.2. Low power Gate Driver for Bidirectional Scanning

The block diagram of the bidirectional gate driver is shown in Fig. 3.4(a), which is composed of one input signals (Out[n-2]), control signals (Clk1, Clk3, Vdd_r and Vdd_b), feedback signals (Out[n+2]), and output signals (Out[n]). Fig. 3.4(b) depicts the connections of the driver blocks. For the forward scan direction, the block manipulation is activated while two start signals (In1_f and In2_f) input a high voltage level to Stage[1] and Stage[2]. A pulse signal is subsequently generated at Out[1] and being acted as the start signal for Stage[2]. Accordingly, sequential pulse signal can be periodically transferred stage by stage for feeding the whole gate lines of the pixel array in TFT-LCD. On the other hand, for the backward scanning, the start signals (In1_b and In2_b) are the impetus of the panel operation at Stage[n] that is the last stage of the gate driver circuit. The Out[n] is the initiative signal of Stage[n-1], and then the gate pulse appear at Out[n-1]. Repeatedly, the operation among blocks is the same as the forward direction. The only difference is the opposite of the order of gate pulses. Fig. 3.5(a) presents the schematic diagram of bidirectional gate driver circuit with its corresponding waveforms in Fig. 3.5(b). The high and low voltage levels in Fig. 3.5(b) are defined as Vdd and Vss, respectively. The operation can be divided into nine periods, noted from T1 to T9. The operation of bidirectional gate driver circuit is similar to the original proposed circuit.

For forward scanning, the Vdd_f and Vdd_r are connected to Vdd and Vss, respectively. In the T1 period, M1_f is turned on by Out[n-2]. The other transistors are turned off. At this moment, Out[n] is Vss through M4 and A[n] is charged by M1_f. Therefore, the node voltages of A[n] and Out[n] are almost Vdd-Vth at the end of this period. In the T2 period, M3 and M6 are turned on by A[n]. Hence, A[n] charges to Vdd-Vth, that is, the node of A[n] is charged early in T1 period and can reach Vdd-Vth completely, yet the Out[n] and B[n] connect to Vss. In the T3 period, the duration that delivers the pulse to the gate line, comes up with Clk1 transits from low to high level. In the T4 period, the A[n] is maintained at high voltage level so that Out[n] can be discharged through M3 cause of Clk1 is at low level. In the T5 period, the A[n] is finally discharged by M2_b. The turn on of M2_b is caused by Out[n+2] and the low voltage level of Vdd_b. Completed the function of delivering gate pulse at Out[n], the remaining periods are used for the noise elimination.

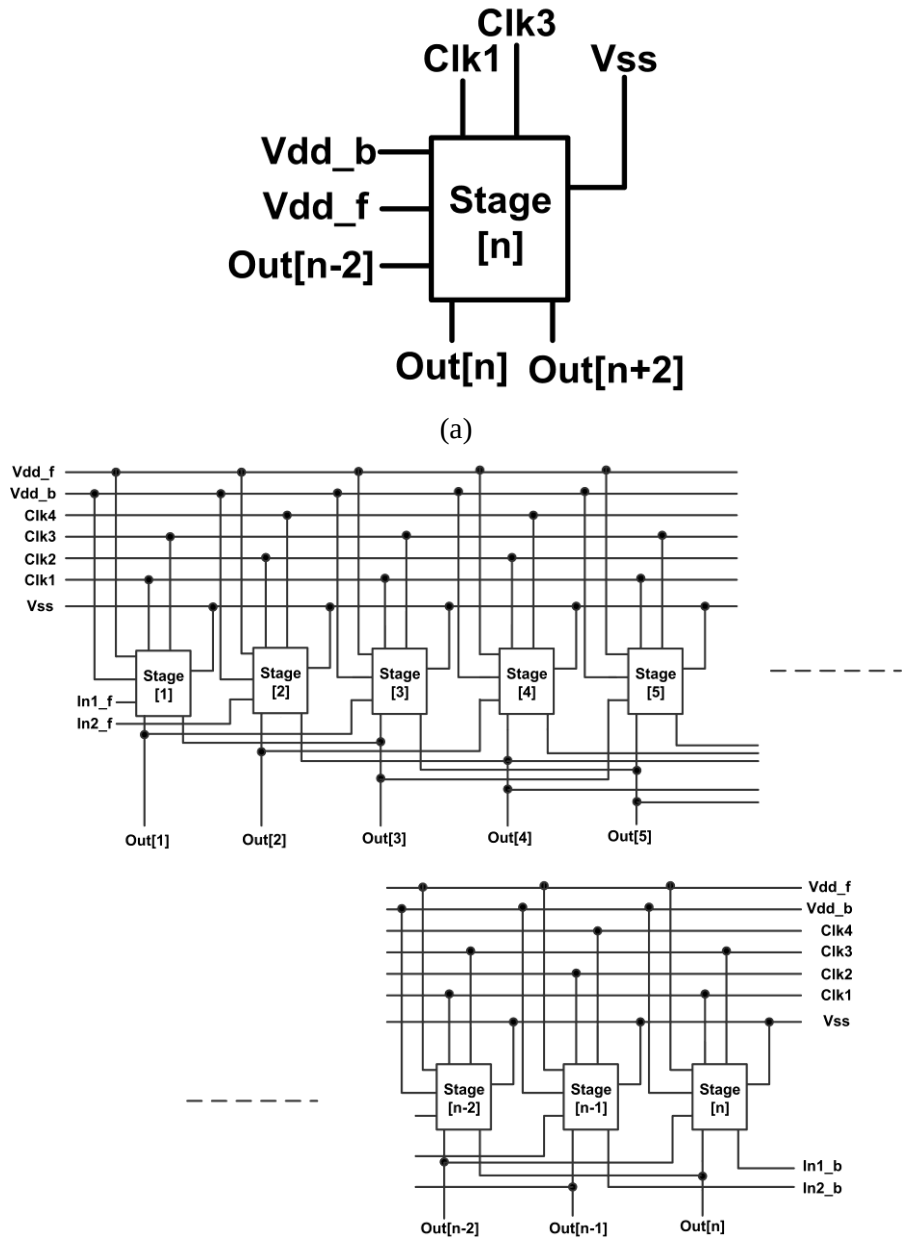
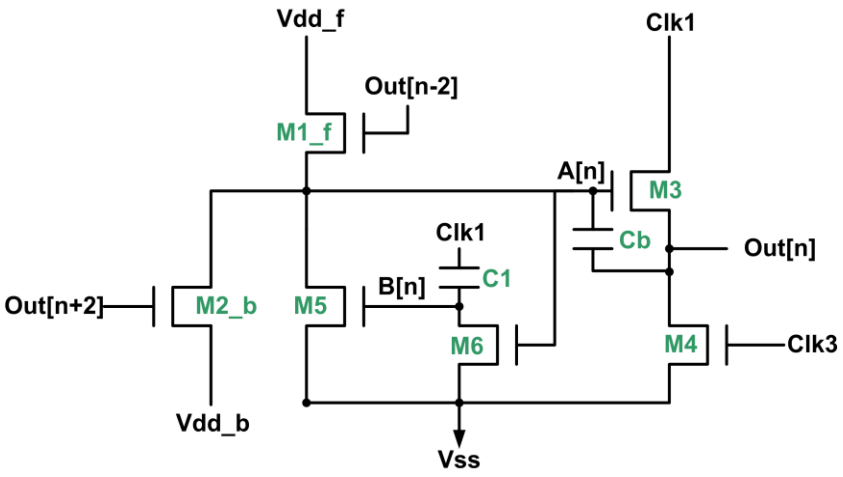
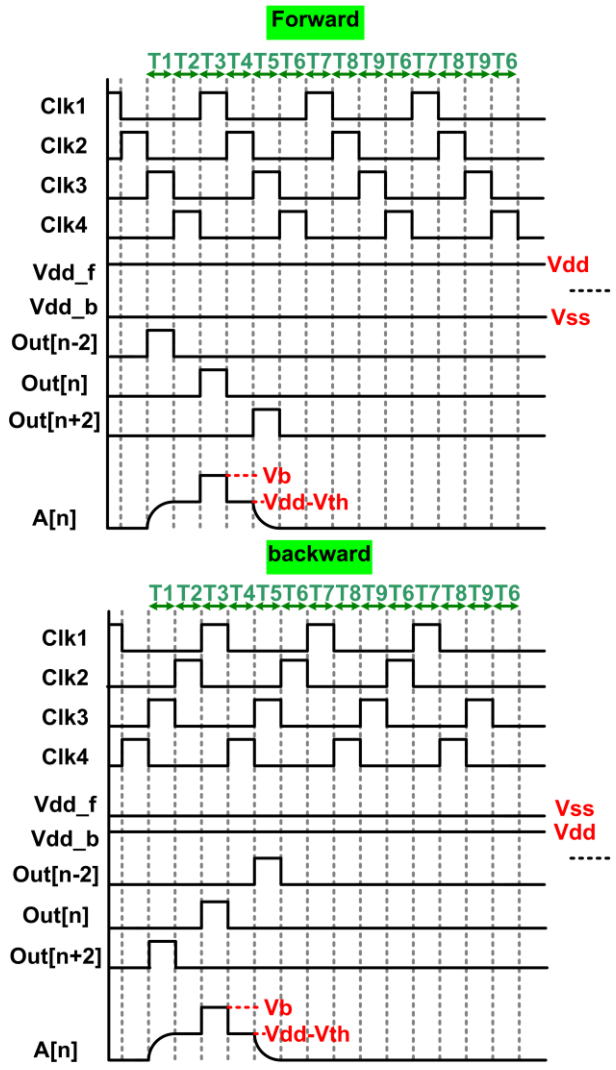


Fig. 3.4. (a) The block diagram and (b) the connections between stages of the proposed bidirectional gate driver circuit for TFT-LCD application.

From the T6 to T9 periods, the operation steps are the same as mentioned in Fig. 3.2. For the backward direction, the sequences of clock signals have been adjusted and the voltage level of Vdd_f and Vdd_b has to be exchanged. The operation is similar to forward direction where M2_b is used to charge the capacitor (Cb) in order to set node A[n] to high voltage level, and A[n] is reset by M1_f.



(a)



(b)

Fig. 3.5. (a) The schematic and (b) the corresponding operation waveforms of bidirectional gate driver circuit.

3.3. Experimental Results and Discussion

3.3.1. Simulation Results of Low Power Gate Driver

The proposed integrated gate driver was designed and verified by HSPICE simulation with RPI a-Si TFT model (Level=61) provided by the foundry. The field-effect mobility and threshold voltage are 0.369cm^2/V.s and 4.019V, respectively. Table 3.1 indicates the device parameter (channel width (W) to channel length (L) aspect ratio and capacitors) of the proposed gate driver with the output loadings of each stage are one capacitor (17pF) in parallel with one resistor (10MΩ). The width of M3 of the proposed gate driver is designed with thousands micrometer for faster to pulling up and down the output loading of oscilloscope.

Table 3.1

Device Parameters of the Proposed Integrated Gate Driver

TFT aspect ratio W/L (μm/μm) (proposed gate driver circuit)			
M1	300/3	M5	100/3
M2	300/3	M6	100/3
M3	3000/3	M7	100/3
M4	300/3		
(proposed bidirectional gate driver circuit)			
M1_f	300/3	M4	300/3
M2_b	300/3	M6	100/3
M3	3000/3	M7	100/3
Capacitance (pF)			
C1	2	Cb	3

The input signals are two start pulses (In1 and In2), four clock signals (Clk1, Clk2, Clk3, and Clk4), and ground signal (Vss) with voltage levels from 25V to 0V. Notice that the pulse width of each clock signal is 40μs with the operational period time of 160μs means the clock

duty is 25%. Furthermore, a quarter of clock duty reduces the stress effect of prominent transistors cause of low stress time for TFT, especially the pull down transistor of M4.

For single-direction scanning, Fig. 3.6 illustrates the simulated Out[n] waveforms of the proposed circuit from the first to the fourth stage. Sequential pulse signals have been successfully observed in Fig. 3.6 to verify the output function of proposed circuit. The rise time, fall time, and noise root mean square (RMS) voltage are represented in Table 3.2, where the rise and fall times are defined by the time difference between 10% to 90% pulse voltage levels, the noise RMS is the root mean square voltage of Out[n] from T6 to T9 periods.

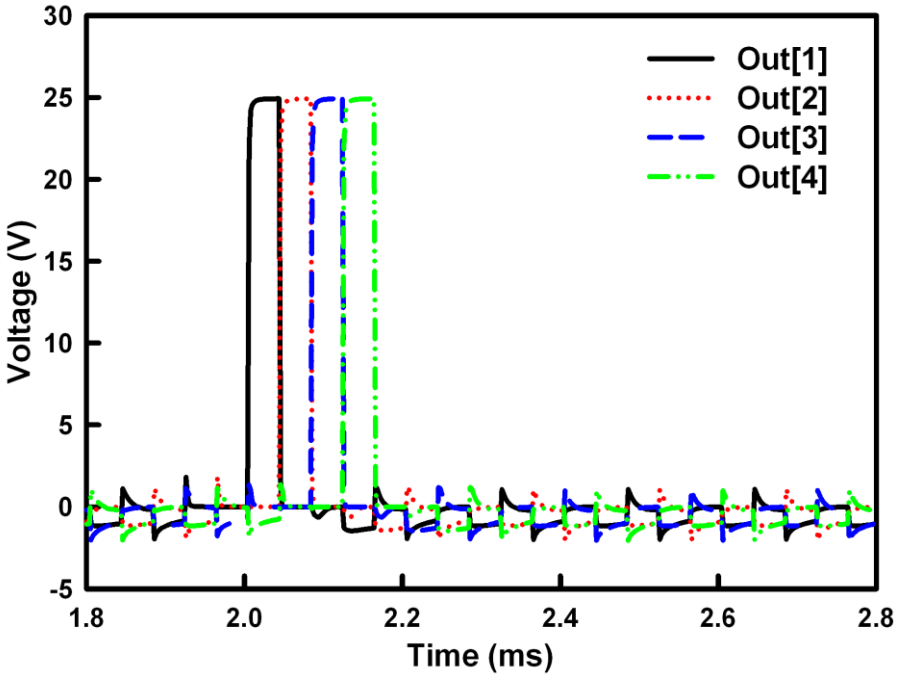


Fig. 3.6 Simulated waveforms of Out[n] for the proposed circuit.

Table 3.2

Simulated Results of the Proposed Circuit at the First to the Fourth Output

	Rising time (μs)	Falling time (μs)	Noise RMS (V)
Out[1]	1.065	0.586	0.813
Out[2]	1.052	0.651	0.833
Out[3]	1.103	0.593	0.872
Out[4]	1.082	0.593	0.871

Table 3.3

Comparison of Power Simulation between Proposed Circuit and GOA in Chapter 2

	Proposed circuit	GOA in chapter 2
Pavg (mW)	12.57	32.2

The power consumption of GOA is calculated from the clock signals and it can be divided into two parts: dynamic and static power, which are shown as follow

$$P = nACV^2 f + VI \,. \tag{3.1}$$

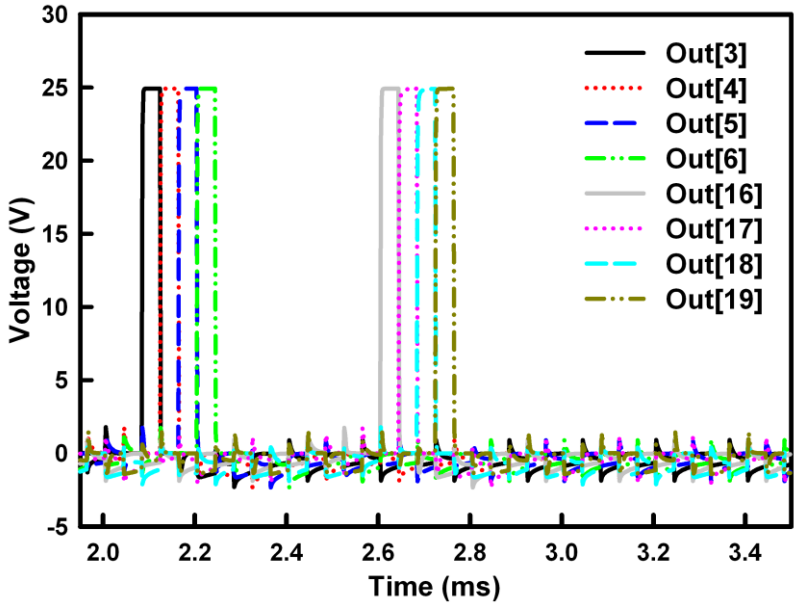
The first term is the dynamic power loss from clock signals' transition. Where A is the fraction of gate actively switching, C is the input loading capacitance of GOA cells, f is the frequency of clock, and n is the whole number of clocks in gate driver. In the proposed circuit, although the number of clocks is doubled, the frequency of clocks is reduced by half. It means that the dynamic power is not affected in the proposed gate driver. However, the proposed circuit deserts the pull-down transistor in chapter 2 to reduce the overall parasitic capacitance of GOA cells, so the dynamic power consumption is substantially reduced cause of smaller input loading capacitance.

The second term presents the static power loss from the static current I and voltage source V and the main static power loss of GOA cells is from the leakage current of M3 (when Out[n]=Vss, Clk1=Vdd, and A[n]=Vss in Fig. 3.2(a)), which is operated in forward sub-threshold region and its formula can be depicted as [10]

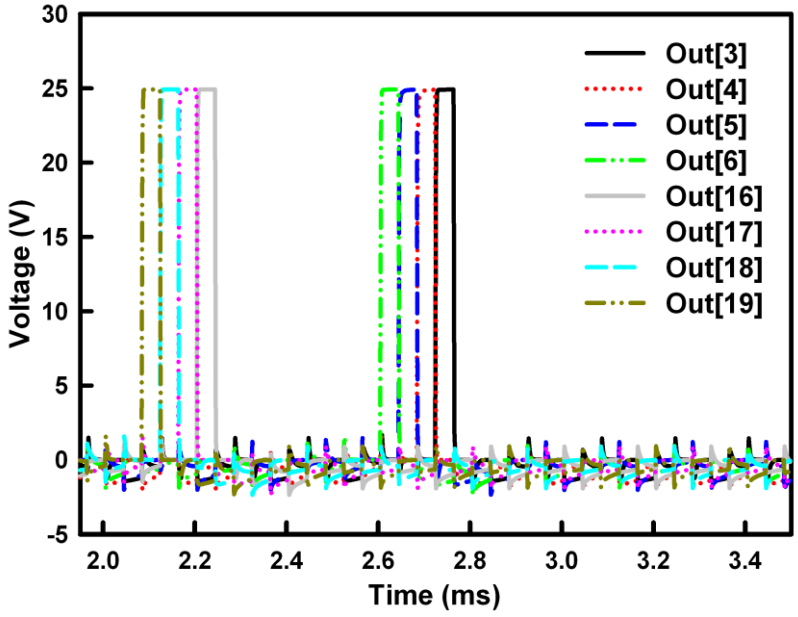
$$I_{DS} = I_0 \frac{W}{L} e^{(V_{GS} - V_T)_s / S} \,. \tag{3.2}$$

Where W and L are the effective channel width and channel length. VTS denotes the boundary of the forward sub-threshold. Sf is the forward sub-threshold slope, I0s is the magnitude of current in the sub-threshold region, and VGS is gate to source voltage. For the TFT-LCD panel application, when switching transistor in pixel is turned off, the gate to source voltage of it is about -7V and the leakage current is low. Nevertheless, when Out[n] of GOA is Vss, the gate to source voltage of M3 is about 0V and it induces larger leakage current to result higher static power consumption of GOA cells. For this reason, the lower duty cycle of clock signals of the proposed gate driver (25%) will reduce the duration of high voltage of the pull-up transistor (M3) that can achieve lower static power consumption.

Consequently, Table 3.3 shows the average power (Pavg) of the proposed circuit (12.57mW) which is much lower than the GOA in chapter 2 (32.2mW), and the overall power reduction ratio is about 61%.



(a)



(b)

Fig. 3.7. The simulated output waveforms of bidirectional gate driver circuit at the outputs Out[3], Out[4], Out[5], Out[6], Out[16], Out[17], Out[18] and Out[19], (a) forward direction and (b) backward direction.

For bidirectional scanning, Fig. 3.7(a) and Fig. 3.7(b) show the simulated waveforms of the proposed bidirectional gate driver circuit for forward and backward scanning. The simulated outputs results are shown in Table 3.4. Notices that the first outputs (Out[1] and Out[2]) and final outputs (Out[20] and Out[21]) are dummy stages and they are not shown in Fig. 3.7(a) and Fig. 3.7(b). Since the A[n] of dummy stages has no extra source such as M2_b in Fig. 3.5(a) to discharge it, the Out[n] will be high if the Clk is in high period. Nevertheless, although the outputs of dummy stages are malfunction, there is no effect on the consequences of bidirectional gate driver circuit since they are not used to the gate lines of panel.

Table 3.4

Simulated Results of Bidirectional Gate Driver Circuit for Forward and Backward Scanning

	Rising time (μs)	Falling time (μs)	Noise RMS (V)
Out[3]	1.14	0.73	0.65
Out[4]	1.14	0.75	0.7
Out[5]	1.11	0.73	0.71
Out[6]	1.14	0.76	0.7
Forward scanning			
	Rising time (μs)	Falling time (μs)	Noise RMS (V)
Out[19]	1.11	0.77	0.65
Out[18]	1.12	0.74	0.6
Out[17]	1.11	0.73	0.7
Out[16]	1.14	0.72	0.65
Backward scanning			

3.3.2. Measurement Results of the Proposed Integrated Gate Driver

For array verification, one hundred integrated gate driver which are manufactured on glass substrate in amorphous silicon technology. As shown in Fig. 3.8(a), the measurement setups depict that the synchronous control signals (Clk, XClk, and In) are generated by the pulse card option for Keithley 4200 (4200-PG2), and the input range are set as 0V to 25V. Furthermore, digital oscilloscope is utilized to observe the output waveforms. The equivalent loading of its probes is one capacitor (17pF) in parallel with one resistor (10MΩ) which is equal to the simulation environment. Moreover, the probe card with 24 pins is applied for the connections between fabricated circuit and measurement equipment. Fig. 3.8(b) and Fig. 3.8(c) present the die photo of the proposed integrated gate driver and bidirectional gate

driver circuit. Because the widths of M3 is designed with thousands micrometer for pulling up and down the output node (Out[n]), the larger layout area is occupied by M3 in Fig. 3.8(b) and Fig. 3.8(c).

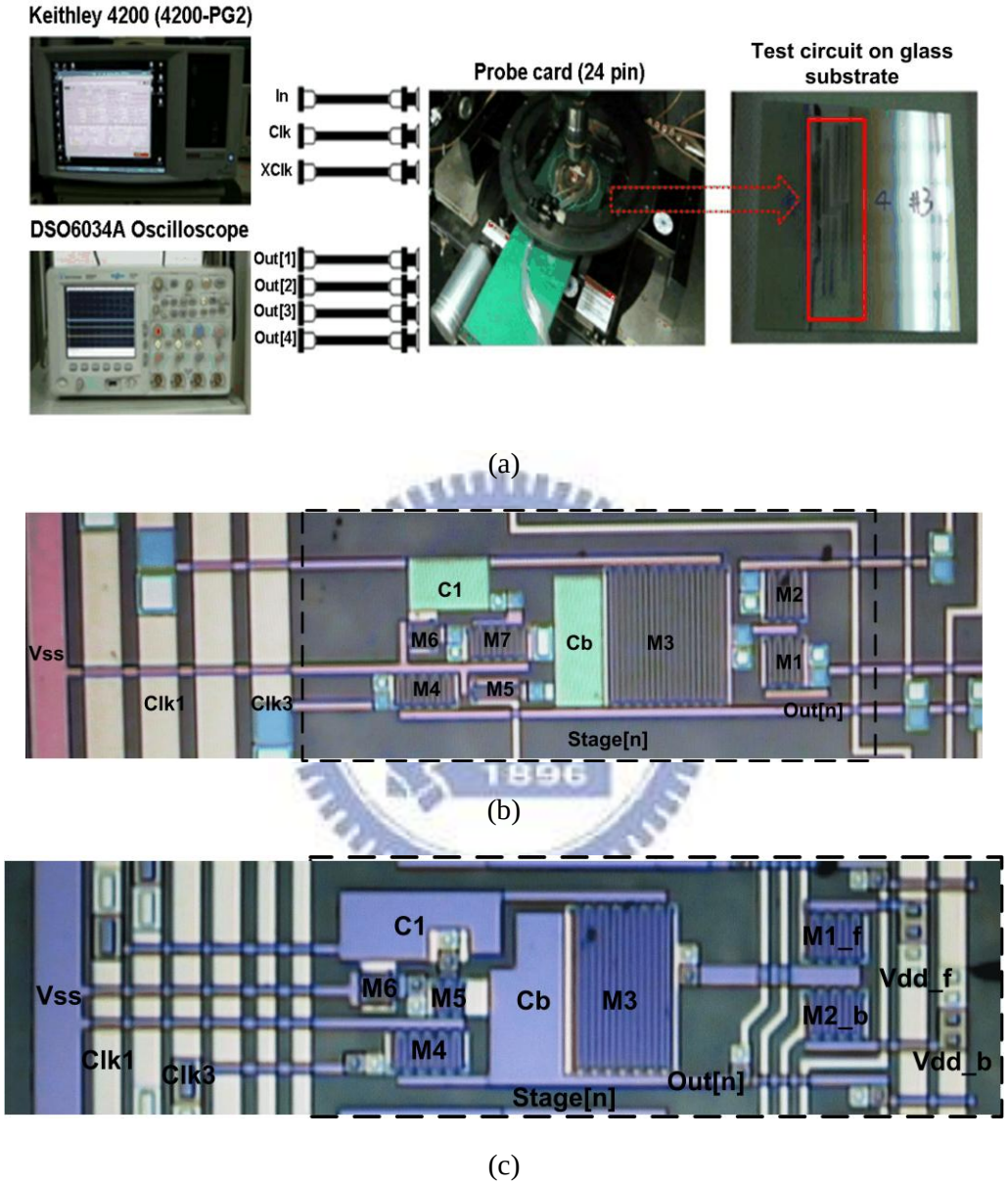
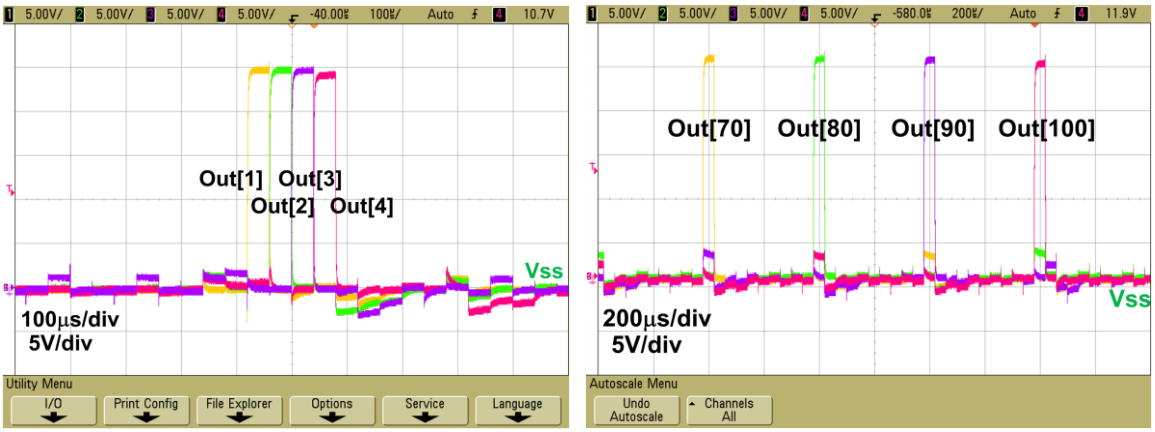


Fig. 3.8. (a) The measurement setups, (b) the die photo of the proposed integrated gate driver, and (c) bidirectional gate driver for array testing.



(a) (b)

Fig. 3.9. The measured output waveforms of the proposed gate driver circuit at the (a) head stages (Out[1], Out[2], Out[3], and Out[4]) and the (b) tail stages (Out[70], Out[80], Out[90], Out[100]).

For single-direction scanning, Fig. 3.9(a) shows the measured output waveforms of the proposed circuit from the first to fourth stages (Out[1], Out[2], Out[3], and Out[4]). In addition, Out[70], Out[80], Out[90], and Out[100] are shown in Fig. 3.5(b). The rising time, falling time, and noise RMS are represented in Table 3.5. These results demonstrate that the proposed integrated gate driver has faster output charging speed and the lower noise RMS are capable for panel integration.

Table 3.5

The Measured Results of the Proposed Gate Driver Circuit

	Rising time (µs)	Falling time (µs)	Noise RMS (V)
Out[1]	1.92	1.55	0.23
Out[2]	2.3	1.5	0.5
Out[3]	1.85	1.4	0.75
Out[4]	1.98	1.46	0.47
Out[70]	2.09	1.54	0.5
Out[80]	2.22	1.62	0.5
Out[90]	2.2	1.59	0.25
Out[100]	2.34	1.75	0.59

For bidirectional scanning, Fig. 3.10(a) and Fig. 3.10(c) shows the measured output waveforms of the bidirectional gate driver circuit from the first to fourth stages (Out[1], Out[2],

Out[3], and Out[4]) for the forward scanning and backward scanning. In addition, Out[50], Out[100], Out[101], and Out[102] are shown in Fig. 3.11(b) and Fig. 3.11(d). The rising time, falling time, and noise RMS are represented in Table 3.6.

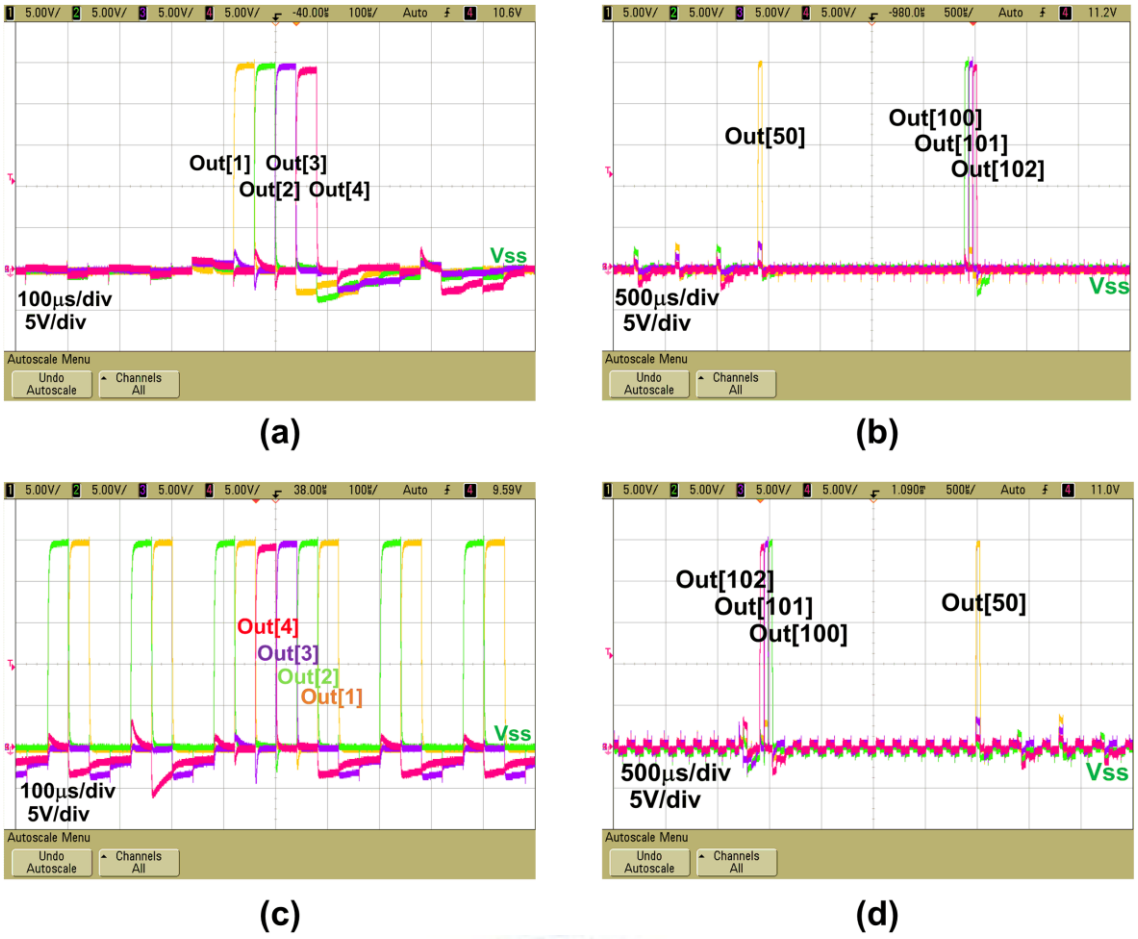


Fig. 3.10. The measured output waveforms of the bidirectional gate driver circuit by forward scanning for (a) (Out[1], Out[2], Out[3], and Out[4]) (b) Out[50], Out[100], Out[101] and Out[102]) and by backward scanning (c) (Out[1], Out[2], Out[3], and Out[4]) (b) Out[50], Out[100], Out[101] and Out[102]).

Notice that in Fig. 3.10, the outputs of final two stages for backward scanning, Out[1] and Out[2], are malfunction because A[n] has no extra source such as M2_b in Fig. 3.5(a) to discharge it, therefore, the Out[n] will be high if the Clk is in high period. Although the outputs of dummy stages are malfunction, there is no effect on the consequences of bidirectional gate driver circuit since they are not used to the gate lines of panel.

Table 3.6

The Measured Results of the Proposed Bidirectional Gate Driver Circuit

	Rising time (μs)	Falling time (μs)	Noise RMS (V)
Out[3]	2.2	1.65	0.62
Out[4]	2.37	1.84	0.54
Out[100]	2.46	1.86	0.83
Out[101]	2.5	2.44	0.72
Out[102]	2.9	3.16	0.7
Forward scanning			
	Rising time (μs)	Falling time (μs)	Noise RMS (V)
Out[102]	2.86	3.14	0.78
Out[101]	2.62	2.06	0.82
Out[100]	2.63	2.0	0.51
Out[4]	2.14	1.66	0.69
Out[3]	2.3	1.72	0.58
Backward scanning			

3.3.3. Panel Integration in a 4.5-inch WXGA Panel

A 4.5-inch WXGA panel has been fabricated with the proposed integrated gate driver, and its specification is summarized in Table 3.7. The resolution of the panel is 1440x800 with the contrast ratio of 1000:1. The frame rate and back light brightness are 60Hz and 4000cd/m^2, respectively.

Table 3.7

The Specification of a 4.2-inch WVGA Panel

	Specification
Panel size (mm*mm)	53.3*91.65
Resolution	1440X800
Frame rate (Hz)	60
Pixel pitch (μm*μm)	103.5*103.5
Back light brightness (cd/m^2)	4000
Contrast ratio	1000:1
Integrated gate driver cell area (μm*μm)	950*207

Besides, the demonstrated 4.5-inch panels are passed the reliability tests of the supporting foundry for operating after the 1000 hours operation under 70℃ and -20℃ conditions. Fig. 3.11 presents the photo of the proposed integrated gate drivers that are allocated at the both sides of pixel array in a 4.5-inch WXGA panel. The layout area of each stage is 950μmx207μm under the layout optimization. Fig. 3.12(a) shows the display image for forward scanning and Fig. 3.12(b) shows the reversal display of image for backward scanning of proposed gate drivers.

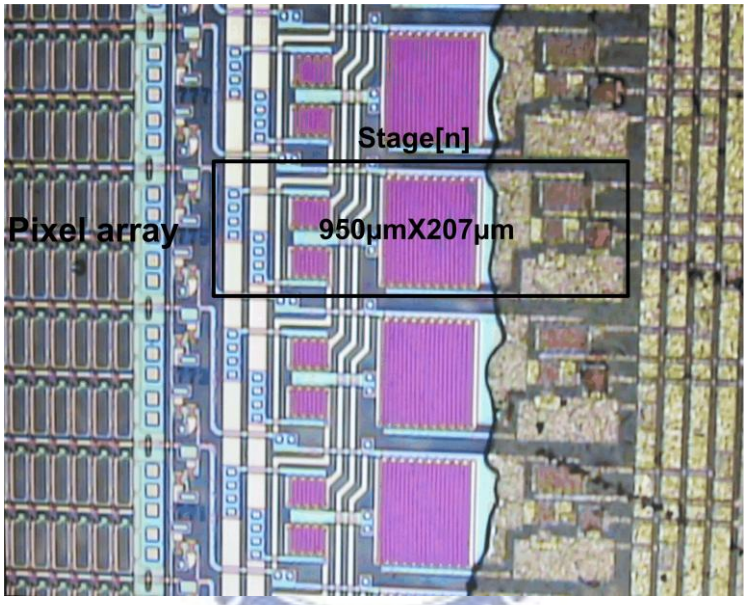
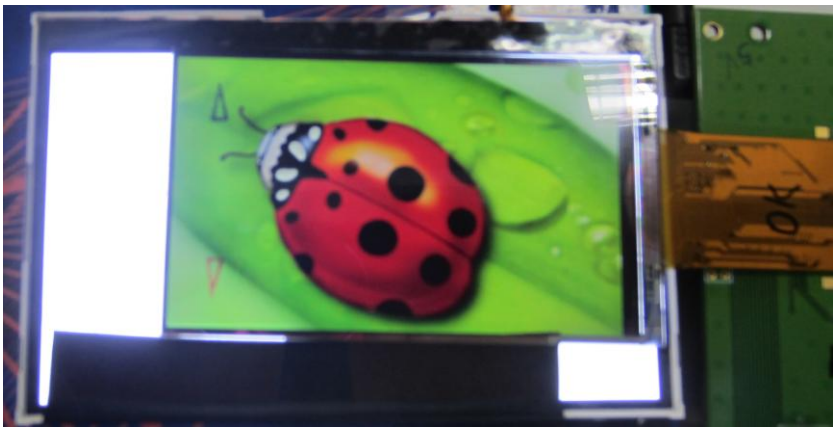


Fig. 3.11. The photo of the proposed integrated gate drivers that are allocated at the both sides of pixel array in a 4.5-inch WXGA panel.

(a)



(b)

Fig. 3.12. The display image of a 4.5-inch WXGA panel for (a) forward direction scanning and (b) backward direction scanning.

3.4. Summary

A new gate driver using amorphous silicon TFT technology has been successfully designed and fabricated for TFT-LCD application. The proposed gate driver utilizes four clock signals and only one output charge/discharge TFT to narrow the pixel size and achieve power reduction about 61%. Besides, the scan direction of the proposed gate driver can be adjusted by switching two control signals to accomplish the bidirectional function and it is as well as demonstrated on 4.5-inch WXGA panel successfully. Therefore, the proposed gate driver is quite appropriate for integration into to the high resolution and low power TFT-LCD panels.

Chapter 4

Analog Pixel Memory for Low Power Application in TFT-LCDs

Two types of analog memory cells realized in a 3-μm low temperature polycrystalline silicon (LTPS) technology are proposed to achieve low power application for thin film transistor liquid crystal displays (TFT-LCDs). By employing the inversion signal in the storage capacitor with complementary source follower, the frame rate to refresh the static image can be reduced from 60Hz to 3.16Hz with the output decay less than 0.1V under the input data from 1V to 4V. To further diminish threshold voltage drop from source follower structure, a compensation technique is implemented to the proposed analog memory cells. In addition, asymmetric output voltage can be also minimized by adding a reference voltage to achieve symmetric output waveform.

4.1. Background

Thin Film Transistor Liquid Crystal Displays (TFT-LCDs) have become a mainstream in display markets due to its compact, light-weight, and high contrast ratio. However, power consumption becomes a serious issue for the TFT-LCDs, especially for the portable products. The research reports mentioned that the power consumption almost comes from the backlight system and AC power supplying to liquid crystal of the source drivers [50]. Therefore, the memory-in-pixel (MIP) concept was proposed to meet low power application [51]-[57], which provided a low power standby mode for continuous display of static images without the power wastage on the source drivers. By refreshing the voltage level of scan lines, polarity inversion could be easily achieved even though the data is no longer furnished. So far, the literatures were reported with the digital MIP circuits [51]-[54]. They can be classified as two basic approaches: the static type and the dynamic type. In general, the static digital MIP circuit exhibits the lowest power consumption since the dynamic power is only consumed while pixels are charged during polarity inversion. However, the main drawback of the static digital MIP is too large in layout area for displays with a fine pixel pitch. The static MIP

circuits typically required seven or eight TFTs and six row lines per pixel. On the contrary, the dynamic digital MIP circuits are more attractive because of fewer TFTs and row lines per pixel. Fig. 4.1 shows the dynamic digital MIP circuit which is realized with three n-type TFTs for one bit operation [51]. The manipulation starts at pre-charging the data line in the initial state. During the reading period, the data line voltage can be defined by the gate bias (Vp) of M3. Whereas Vp is a higher voltage, the voltage of data line will be a lower one. After that, the inverse data is then written back onto Vp via M1 in the writing period. Consequently, Vp is coupled by the scan signal through Cs and held until the next operation period, where C_{LC} and Cs are the capacitance of liquid crystal and storage capacitor. The refresh operation must be performed row by row so the largest power is consumed in pre-charging of the data line.

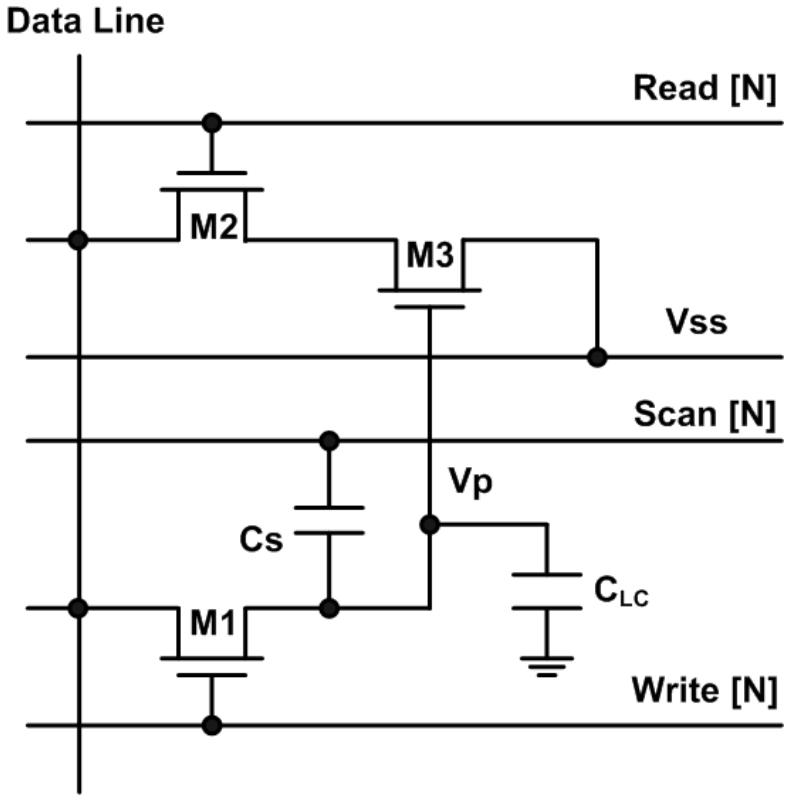


Fig. 4.1. The dynamic digital MIP circuit realized with three n-type TFTs for one bit operation.

For multi-bits application, static and dynamic digital MIP circuits still require many scan lines and capacitors to reach polarity inversion. Therefore, the adoption of analog concept for MIP circuit is attempted since it can achieve higher image quality with fewer components. However, the output voltage of the analog memory circuit may have inaccuracy with corresponding data signal, which means that the static image may be distorted by the asymmetric inversion voltage.

In this chapter, two types of analog memory cells with self-voltage inversion for MIP application are proposed, which have been realized in a conventional 3-μm LTPS process without additional process modification. By using the proposed circuits, the operating rate to refresh static image can be reduced from 60Hz to 3.16Hz. Asymmetric inversion voltage can be also minimized by adding a reference voltage to achieve symmetric output waveform. Moreover, a compensation technique is implemented to improve the threshold voltage drop on the output from the input data [58].

4.2. Operation and Simulation of New Proposed Analog Pixel Memory

Fig. 4.2 shows the block diagram of the proposed analog memory cell in a conventional pixel of LCD. There are two modes for dynamic and static operation of LCD image. During the normal mode, dynamic image can be performed by the conventional pixel operation through M_D. Furthermore, during the standby mode for static image, the scan driver switches input from row signal (Row [N]) to control signals. The proposed analog memory cell samples Vdata from source driver and cooperates with control signals to generate self-inversion voltage at Vout.

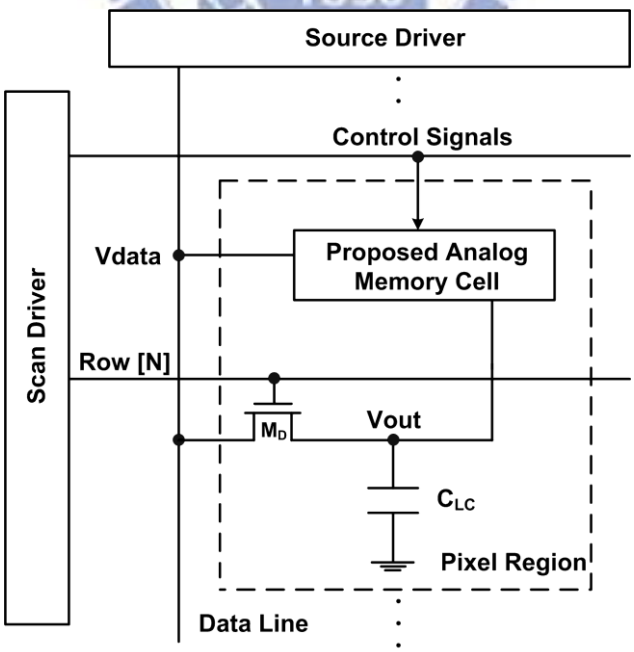


Fig. 4.2. The block diagram of the proposed analog memory cell in a conventional pixel.

4.2.1. New Proposed Analog Memory Cell I

Source driver provides Vdata (Vdata=|Vp|+|Vt|) to the data line for the proposed analog memory cell I, where Vp is the original pixel data and Vt is the threshold voltage of Poly-Si TFT. Fig. 4.3(b) depicts its corresponding waveforms of scan lines. After the proposed analog memory cell I samples the Vdata, the source driver can be turned off until the specific time is arrived. With 315.4ms as an example (nineteen times of typical TFT-LCD frame time), the source driver can be operated from 60Hz to 3.16 Hz for refreshing static image to save power.

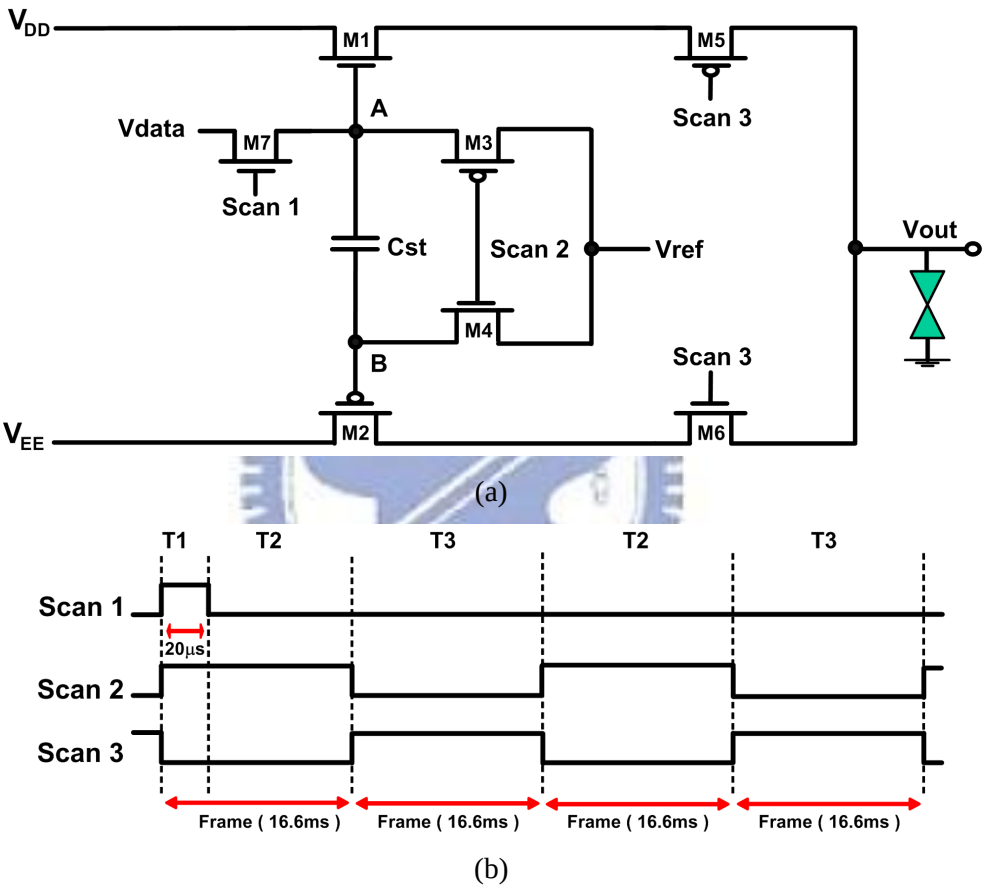


Fig. 4.3. Schematic of (a) the proposed memory cell I and (b) its corresponding control signals. The circuit is composed of two driving transistors (M1 and M2) and five switch transistors denoted as (M3, M4, M5, M6, and M7).

The proposed analog memory cell I shown in Fig. 4.3(a) is composed of two driving transistors (M1 and M2), and five switch transistors (M3, M4, M5, M6, and M7). During the standby mode, the operation of the proposed analog memory cell I is divided into three periods, including the pre-charging period (T1), the positive voltage holding period (T2), and the negative voltage holding period (T3). In the T1 period, Scan2 and Scan3 are set to turn

M3 and M6 off. The driving transistor M1 is operated as a source follower, and Vout becomes Vdata–Vtn at the end of this period, where Vtn is the threshold voltage of M1. In the meanwhile, the node voltages of the storage capacitor (Cst) are set with V_A=Vdata and V_B=Vref. In the T2 period, Scan1 becomes low to turn M7 off, and the other transistors are all kept at the previous states. The gate voltages of M1 and M2 are Vdata and Vref, respectively. Vout remains Vdata-Vtn at the positive data holding period (T2). At the T3 period, Scan2 and Scan3 are set to turn M4 and M5 off. Because M3 is turned on, Vref is applied to the node A. The voltage of node B goes to 2Vref-Vdata because Cst is boosted by the voltage at node A (V_A). At the beginning of T3 period, M2 is operated as a source follower. The output voltage goes to 2Vref-Vdata+|Vtp| and then holds this voltage level until the next period comes, where |Vtp| is the absolute threshold voltage of M2.

In the standby mode, Vout is varied according to the M1 and M2 source followers, respectively. The threshold voltage difference ΔVt between Vtn and |Vtp| will cause non-symmetric output waveforms at Vout, so liquid crystal can't present equal transmittance. In order to solve this issue, assume

$$\Delta Vt = Vtn - |Vtp|. \tag{4.1}$$

The request for the negative data holding period (T3) is generating the opposite sign of the output voltage (-Vout) during the positive data holding period (T2). Hence, Vout can be defined as -(Vdata-Vtn), and which gives

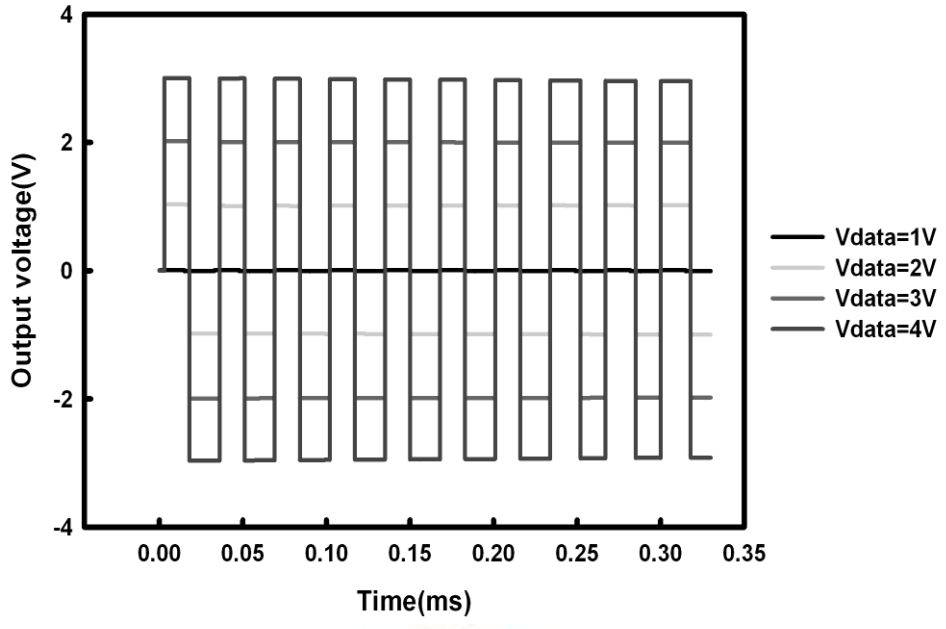
$$\begin{aligned} -(Vdata - Vtn) &= V_B + |Vtp|, \\ &= 2Vref - Vdata - |Vtp|. \end{aligned} \tag{4.2}$$

Derived from Eq. (4.2), the optimized reference voltage (Vref) can be set to achieve the cancellation of threshold voltage difference between M1 and M2. The reference voltage should be

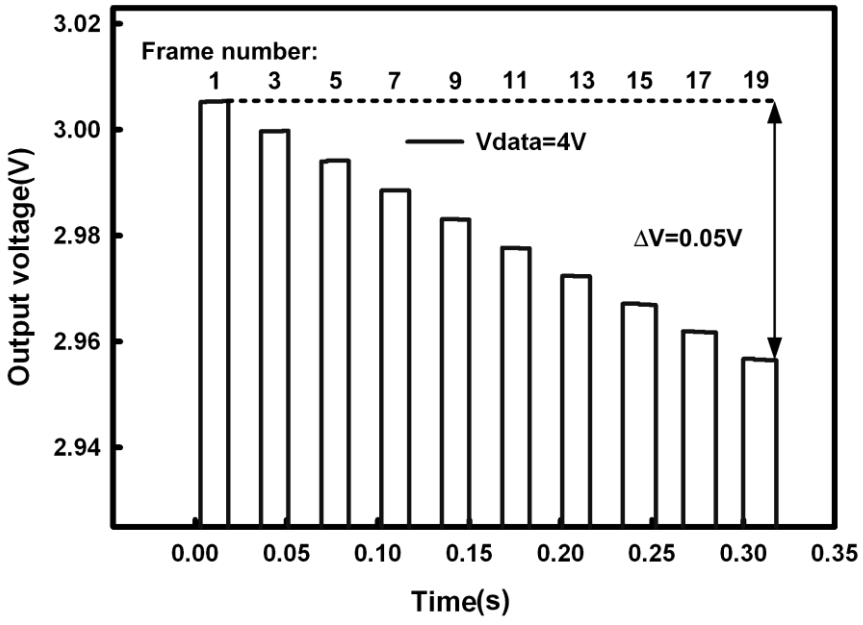
$$Vref = (Vtn - |Vtp|)/2 = \Delta Vt/2. \tag{4.3}$$

By adjusting the reference voltage, the problem of asymmetric inversion voltage in the proposed analog MIP can be solved by this design.

The proposed analog pixel memory cell I has been designed and verified by the HSPICE simulation with the RPI model (Level=62) of a 3-μm LTPS process provided by the foundry. The threshold voltage values of Vtn and Vtp are 0.9V and -0.9V, respectively.



(a)



(b)

Fig. 4.4. The simulation results of the output (Vout) in the proposed analog memory cell I under (a) Vdata of 1V, 2V, 3V, and 4V in twenty frame time per Scan1 pulse, and (b) the partial enlarged plot when Vdata is 4V.

The aspect ratio of channel width (W) to channel length (L), W/L, for driving transistors M1 and M2 are 30μm/5μm, and those for switch transistors (M3, M4) and (M5, M6, M7) are

3μm/5μm and 5μm/5μm, respectively. Furthermore, the storage capacitor is Cst=5pF and the DC voltage supplies are V_{DD}=5V and V_{EE}=-5V. Fig. 4.4 depicts the simulation results of the output (Vout) for the proposed analog memory cell I under Vdata of 1V, 2V, 3V, and 4V. The twenty frame time (20*16.6ms=332ms) per Scan1 pulse is set for the timing duration of Scan1 signal. The power consumption comes from the source driver only when Vdata is sampled by the proposed analog memory cell I. Afterward, the cell works between the positive and negative data holding periods to generate positive and negative pixel voltages at Vout only by the control signals. Fig. 4.4(a) shows the simulated output symmetric voltages no matter how the input data changes. Besides, the high and low voltage levels are decreased approximately a threshold voltage due to the operation of source followers.

Fig. 4.4(b) gives the partial enlarged plot of Fig. 4.4(a) when Vdata is 4V. After nineteen frame time, the simulation result shows that the output voltage decay (ΔV) is only 0.05V. This represents the proposed circuit can be effectively operated higher than 5-bit (data range/one gray scale=3/0.05=60) digital memory at the frame rate of 3.16Hz.

4.2.2. New Proposed Analog Memory Cell II with Threshold Voltage Compensation

Due to the threshold voltage drop of the output voltage from the input data in the proposed analog memory cell I, the analog memory cell II is then proposed to release this limitation. By applying the proposed analog memory cell II, source driver needs not provide Vdata of |Vp|+|Vt| to data line but provide Vdata of |Vp| only. Therefore, source driver doesn't have to modify the data signal with a threshold voltage shift and further reduce the algorithm complexity of source driver.

Fig. 4.5(a) depicts the proposed analog memory cell II and its corresponding waveforms of scan lines. The proposed analog memory cell II is composed of two driving transistors (M1 and M2), and seven switch transistors (M3, M4, M5, M6, M7, M8, and M9). The operation is divided into four periods, including the pre-charging period (T1), the threshold voltage (Vt) compensation period (T2), the positive voltage holding period (T3), and the negative voltage holding period (T4). In the T1 period, scan signals turn on the switches (M4, M5, M7, M8, and M9) and turn (M3 and M6) off, respectively. Vout becomes Vdata through M9, and V_A is charged to V_{DD}. In the T2 period, Scan2 goes to high to turn M7 off. M1 starts to release charge from V_A through M8 in a diode connect structure and V_A becomes Vdata+Vtn at the end of this period, where Vtn is the threshold voltage of M1. In the meanwhile, the storage

capacitor (Cst) is set to V_A=Vdata+Vtn and V_B=Vref. In the T3 period, Scan1 becomes low to turn M8 and M9 off. Scan2 goes to low to turn on M7, and the other transistors are all kept at the previous states. The gate voltages of M1 and M2 are Vdata+Vtn and Vref, respectively. Vout remains Vdata at the positive data holding period (T3). At the T4 period, Scan3 becomes high to turn M4 and M5 off. Because M3 is turned on, Vref is applied to the node A. The voltage of node B goes to 2Vref-(Vdata+Vtn) because Cst is boosted by the voltage at node A (V_A). At the beginning of T4 period, M2 is operated as a source follower. The output voltage goes to 2Vref-(Vdata+Vtn)+|Vtp| and then holds this voltage level until the next period comes, where |Vtp| is the absolute threshold voltage of M2.

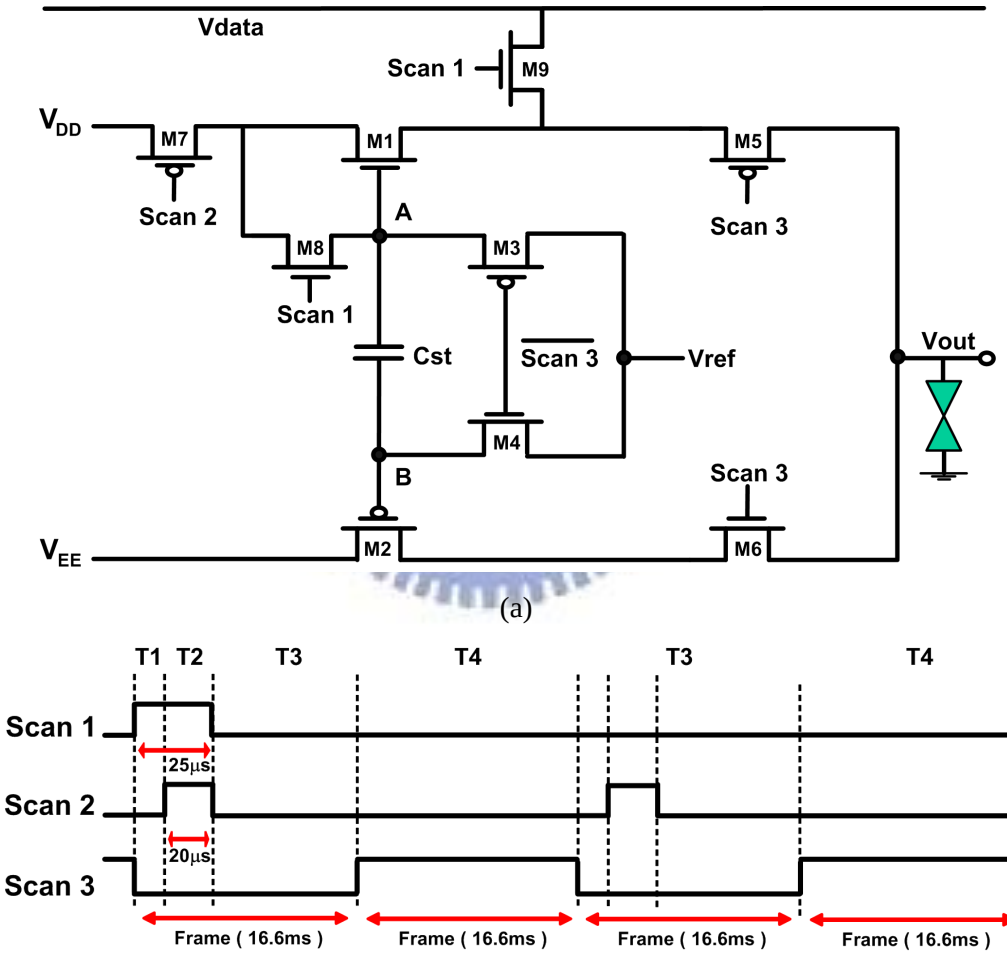


Fig. 4.5. Schematic of (a) the proposed memory cell II and (b) its corresponding control signals. The circuit is composed of two driving transistors (M1and M2) and seven switch transistors denoted as (M3, M4, M5, M6, M7, M8, and M9).

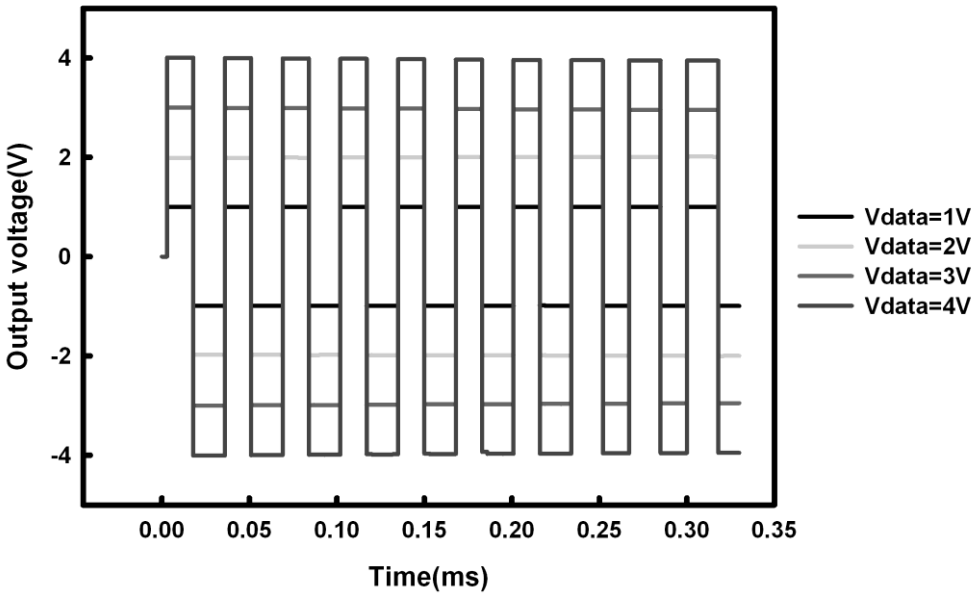
The threshold voltage difference between Vtn and |Vtp| will cause non-symmetric output

waveforms, so that liquid crystal cannot present equal transmittance. In order to solve this issue, the request for negative data holding period (T4) is to generate opposite sign voltage (-Vout) during the positive data holding period (T3). Vout will become -Vdata, which gives

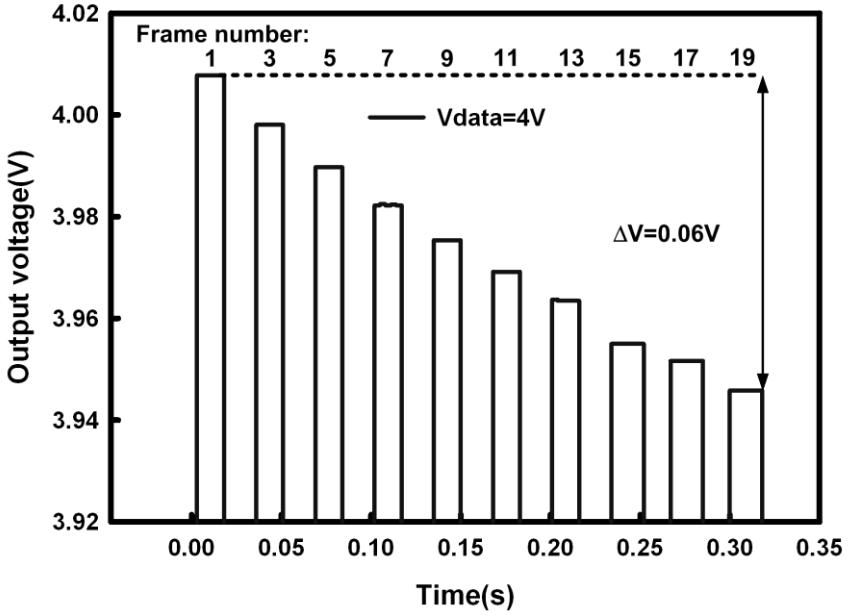
$$\begin{aligned} -Vdata &= V_B + |Vtp|, \\ &= 2Vref - (Vdata - Vtn) + |Vtp|. \end{aligned} \tag{4.4}$$

Derived from Eq. (4.4), the optimized reference voltage (Vref) can be set to achieve the cancellation of threshold voltage difference between M1 and M2. The reference voltage is the same as that shown in Eq. (4.3). By adjusting this reference voltage, the problem of asymmetric inversion voltage for analog MIP can be completely solved by the proposed analog memory cell II.

The aspect ratio of channel width (W) to channel length (L), W/L, for M1 and M2 are 30μm/5μm, and those for switch transistors (M3, M4) and (M5, M6, M7, M8, M9) are 3μm/5μm and 5μm/5μm, respectively. Furthermore, the storage capacitor (Cst) is 5pF and the DC voltage supplies are V_{DD}=5V and V_{EE}=-5V.



(a)



(b)

Fig. 4.6. The simulation results of the output (Vout) in the proposed analog memory cell II under (a) Vdata of 1V, 2V, 3V, and 4V in twenty frame time per Scan1 pulse, and (b) the partial enlarged plot when Vdata is 4V.

Fig. 4.6 depicts the simulation results of the output (Vout) for the proposed analog memory cell II under Vdata of 1V, 2V, 3V, and 4V. The output voltage levels of Fig. 4.6(a) are all the same as the input data. These results have successfully verified that the outputs are independent to the threshold voltage. Fig. 4.6(b) gives the partial enlarged plot of Fig. 4.6(a) when Vdata is 4V. After nineteen frame time, the simulation result shows that the output voltage decay (ΔV) is only 0.06V. This represents the proposed circuit can be effectively operated higher than 6-bit (data range/one gray scale=4/0.06=66.67) digital memory at the frame rate of 3.16Hz. Fig. 4.7 shows the output voltage (Vdata=3V) for M1 and M2 with equal threshold voltage shifts. The threshold voltage shifts are caused by the process variation or the stress under operation. The initial threshold voltage shifts can be minimized by adding the reference voltage (Vref) to achieve symmetric output waveform in the proposed analog memory cells. Besides, the proposed analog memory cells are composed of complementary source follower, the stress condition at V_A and V_B in Fig. 4.3(a) and Fig. 4.5(a) are similar under different input data. In Fig. 4.7, there is no apparent difference between the absolute threshold voltages from 0.9V to 1.9V with the step of 0.5V. The error rates, which is derived from the output voltage difference (ΔV in Fig. 4.7) dividing the threshold voltage difference,

are just 1.14% and 2.12%. The proposed analog memory cells are quite suitable for MIP application.

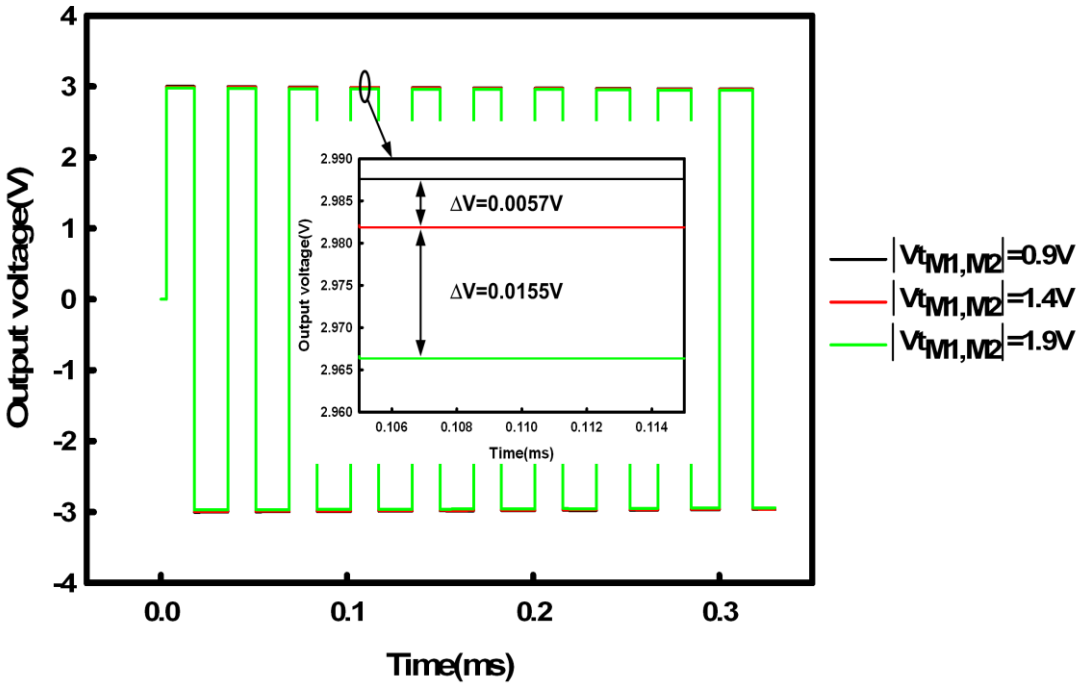
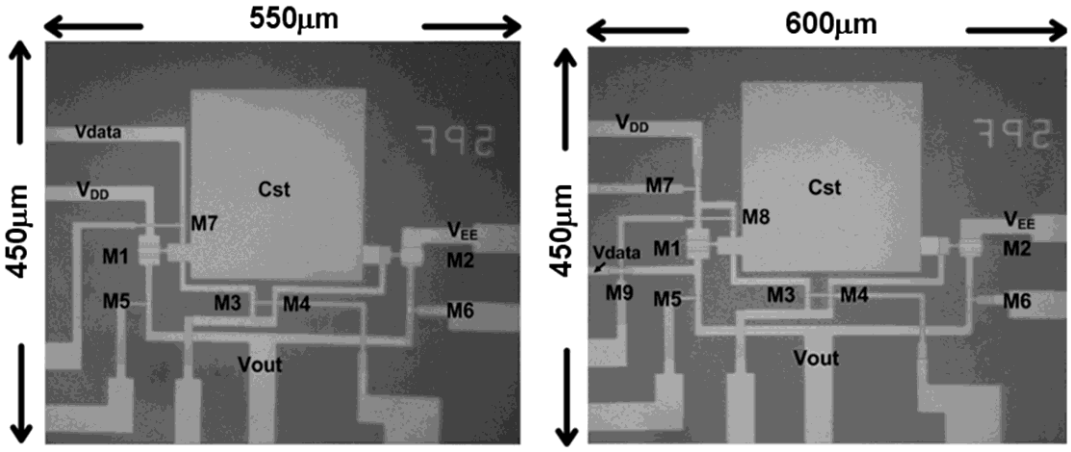


Fig. 4.7. The output voltage for M1 and M2 with equal shifts on threshold voltage of 0.9V, 1.4V, and 1.9V when Vdata is 3V.

4.3. Experimental Results and Discussion

4.3.1. Measurement Results of New Proposed Analog Memory Cell I

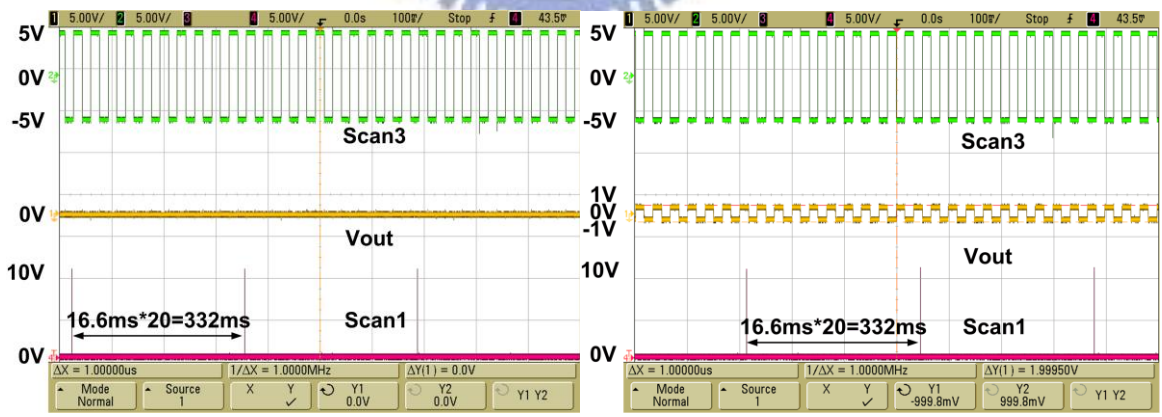
For measurement setup, synchronous signals are generated by the pulse card option for Keithley 4200 (4205-PG2). Input range of Scan1 is set as 0V to 10V. Scan2 and Scan3 are set as -5V to 5V. Digital oscilloscope is utilized to observe the output waveforms. The die photo of fabricated two types of the proposed analog memory cells are shown in Fig. 4.8. A large layout area is occupied by the storage capacitor (Cst) since it is fabricated by the interlayer oxide. The equivalent oxide thickness of the interlayer oxide is about eight times thicker than the gate oxide in TFT. For circuit verification, twenty frame time per Scan1 is used to verify the output waveforms whether it can meet the desired function. As shown in Fig. 4.9, the output inversion signal (Vout) are from 0V to 0V, 1V to -0.998V, 2V to -2.015V, and 3V to -2.975V, when Vdata varies from 1V to 4V with a step of 1V and Vref is 0.2V (ΔVt is about 0.4V).



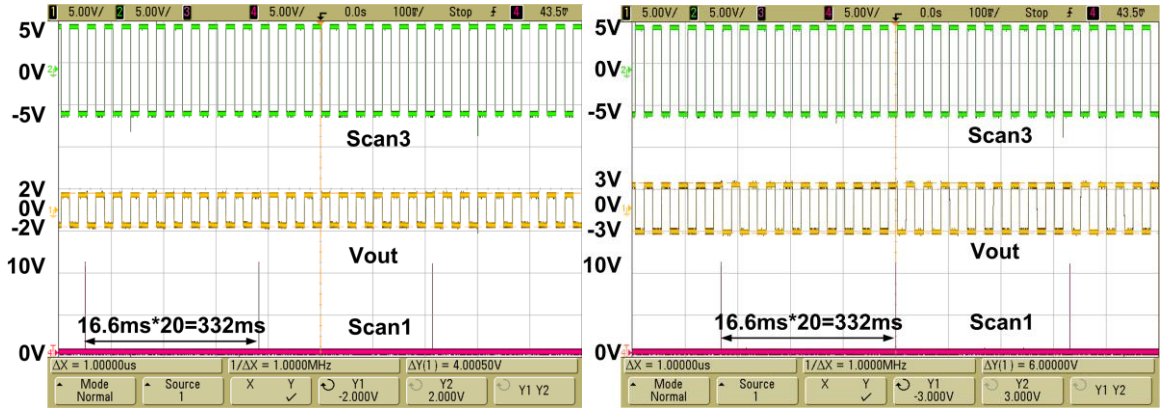
(a) (b)

Fig. 4.8. The die photo of the proposed (a) analog memory cell I, and (b) analog memory cell II, fabricated in a 3-µm LTPS process.

The definition of the inaccuracy for polarity inversion difference is |Vout_positive–|Vout_negative||, and which is no more than 0.025V because of Vref feeding. The threshold voltages of M1 (Vtn) and M2 (Vtp) are about 1V and -0.6V from the output results. Fig. 4.10 shows the enlarged plot for Vout as 0.5V/scale in Fig. 4.9(d) when Vdata is 4 V. The frame numbers are listed from the first to nineteenth, and which are corresponding to 3V (Y2: the first frame number) and 2.925V (Y1: the nineteenth frame number).



(a) (b)



(c) (d)

Fig. 4.9. Measured results of analog memory cell I with (a) Vdata=1V, (b) Vdata=2V, (c) Vdata=3V, and (d) Vdata=4V in twenty frame time (16.6ms*20=332ms) per Scan1 pulse.

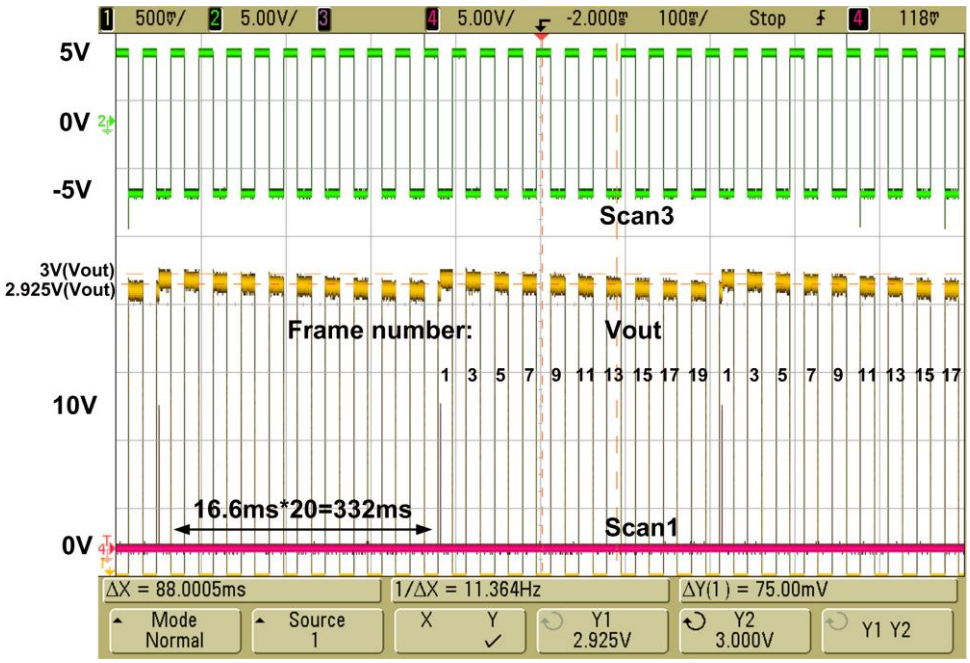


Fig.4.10. The enlarged plot for Vout as 0.5V/scale in Fig. 4.9(d) when Vdata is 4V.

Fig. 4.11 shows the summary of the output voltage under different frame numbers with Vdata of 2V, 3V, and 4V in the proposed analog memory cell I for the positive output voltage. The maximum output voltage decay is less than 0.075V after nineteen frame time when Vdata is 4V. It verified that the operating frequency of source driver can be reduced from 60Hz to 3.16Hz for static image. Besides, frame number can be chosen by the tolerance of specified output decay for higher resolution.

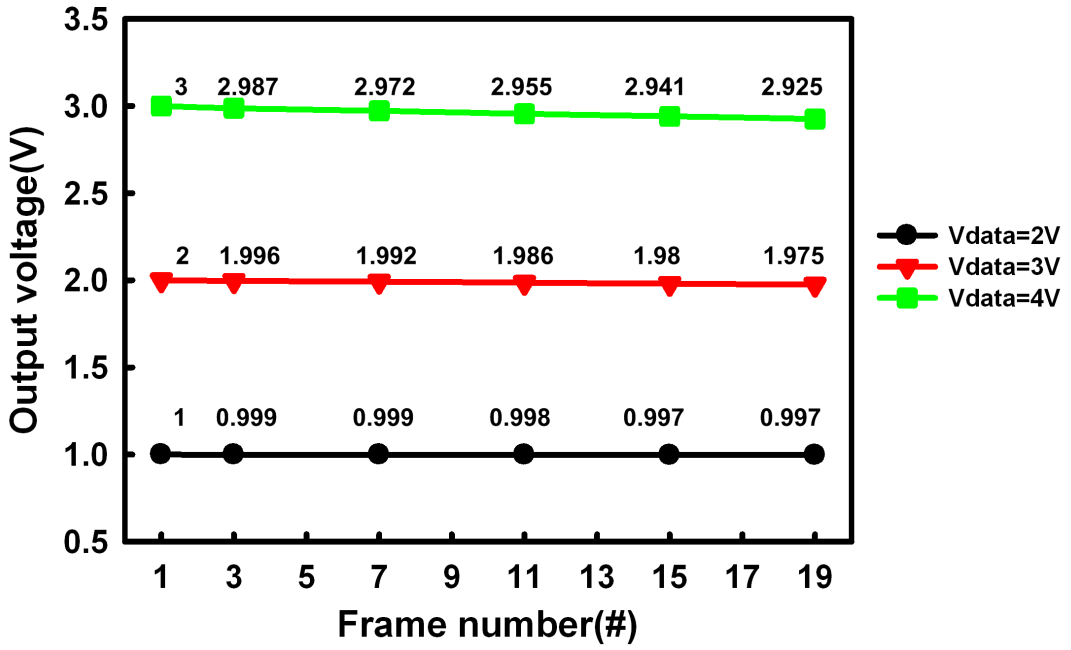
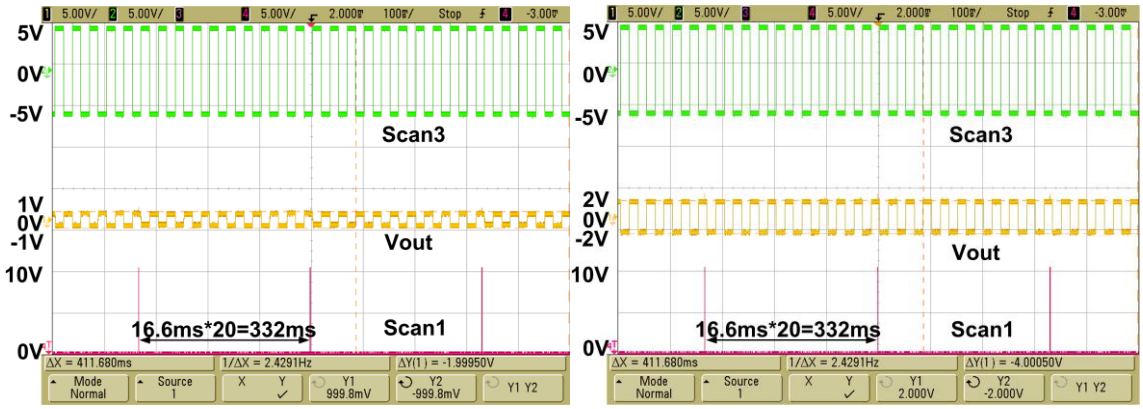


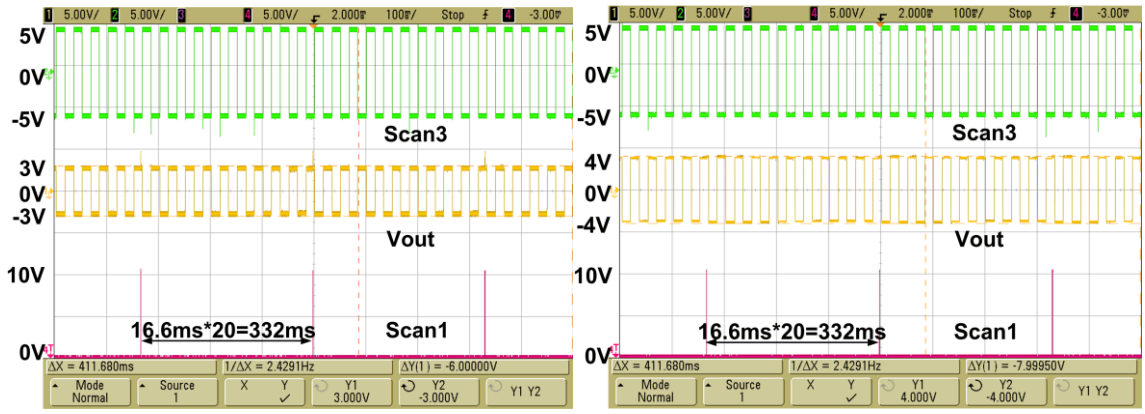
Fig. 4.11. The output voltage under different frame numbers with Vdata of 2V, 3V, and 4V in the proposed analog memory cell I for the positive output voltage.

4.3.2. Measurement Results of New Proposed Analog Memory Cell II with Threshold Voltage Compensation

Fig. 4.12 shows the output inversion signal (Vout) of the proposed analog memory cell II which are from 1V to -0.998V, 2V to -2.015V, 3V to -3.015V, and 4V to -4.025V, when Vdata varies from 1V to 4V with a step of 1V and Vref is 0.2V (ΔVt is about 0.4V). The inaccuracy for polarity inversion difference is no more than 0.025V.



(a) (b)



(c) (d)

Fig. 4.12. Measured results of analog memory cell II with (a) Vdata=1V, (b) Vdata=2V, (c) Vdata=3V, and (d) Vdata=4V in twenty frame time (16.6ms*20=332ms) per Scan1 pulse.

The output voltage can be directly obtained from Vdata without the threshold voltage issues which are consistent with the simulation results. Furthermore, the maximum output voltage decay is less than 0.1V after nineteen frame time when Vdata is 4V. Fig. 4.13 shows the enlarged plot for Vout as 1V/scale in Fig. 4.12(d) when Vdata is 4V. The entire output waveform is contained to show the output symmetry. The frame numbers are listed from first to nineteenth, and which are corresponding to 4V (Y1: the first frame number) and 3.9V (Y2: the nineteenth frame number).

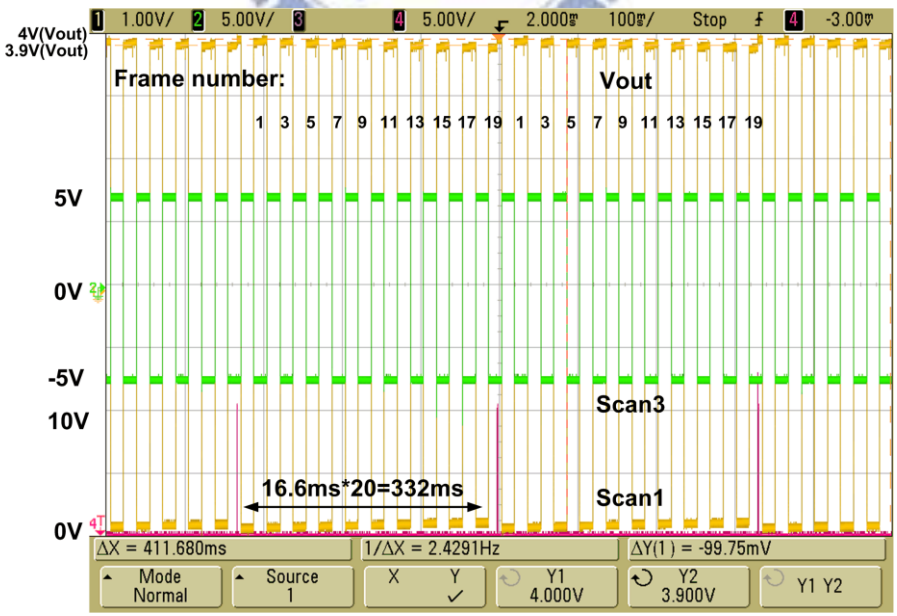


Fig. 4.13. The enlarged plot for Vout as 1V/scale in Fig. 4.12(d) when Vdata is 4V. The entire Vout waveform is contained to show the output symmetry.

Fig. 4.14 shows the summary of output voltage under different frame numbers with Vdata of 1V, 2V, 3V, and 4V in the proposed analog memory cell II for the positive output voltage. The frame number can be chosen by the tolerance of specified output decay for the application of better resolution. By integrating the proposed MIP circuit into the pixel, better image quality can be obtained.

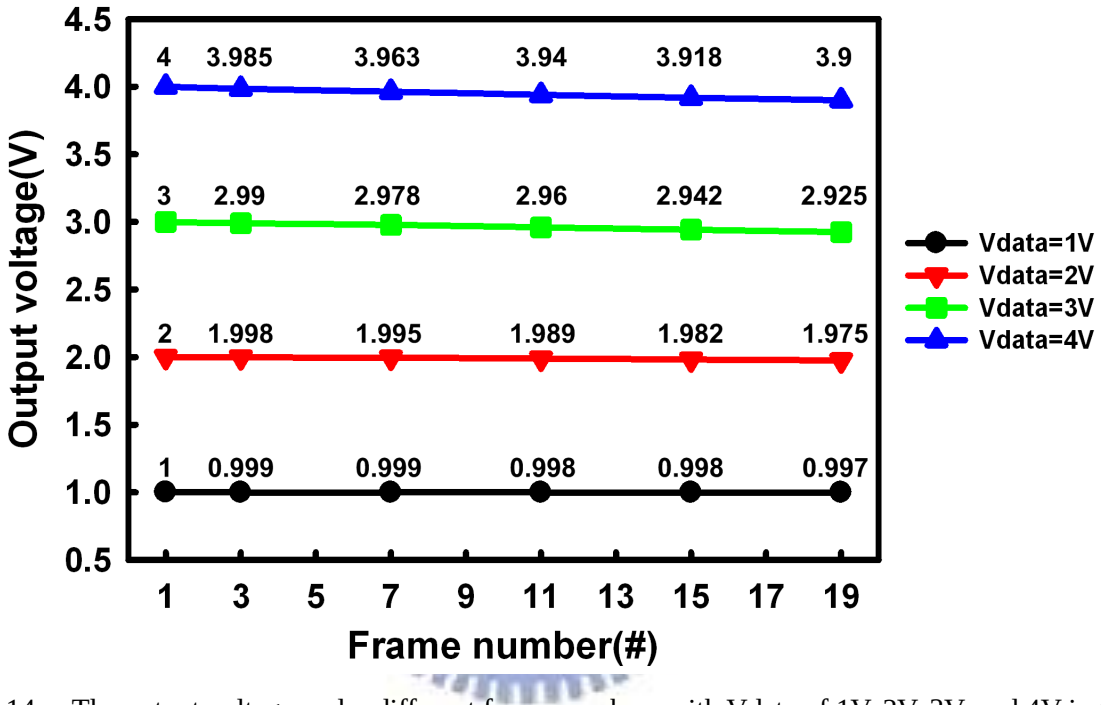


Fig. 4.14. The output voltage under different frame numbers with Vdata of 1V, 2V, 3V, and 4V in the proposed analog memory cell II for the positive output voltage.

The reason for the voltage decay as shown in Fig. 4.11 and Fig. 4.14 is caused by the parasitic effects of transistors. During the T3 to T4 periods in Fig. 4.5, V_A changes from Vdata+Vtn to Vref, and this transient voltage will couple the node B through the storage capacitor (Cst). Nevertheless, the existence of parasitic capacitance will decrease the coupling amount, and which will directly affect the output voltage. The voltage at node B can be shown in the following [59]

$$V_B = Vref - \frac{Cst}{Cgs2 + Cgd2 + Cst + Cgs4}(Vdata + Vtn - Vref). \quad (4.5)$$

The second term of Eq. (4.5) shows that the coupling amount is reduced due to the capacitive division, where Cgs2, Cgd2, and Cgs4 are the parasitic capacitance of M2 and M4. Moreover,

this effect takes place at every transition of polarization inversion to cause the output decay since there is no refreshed data to the storage capacitor. After more frame cycles, the holding voltage will be smaller than the previous one. In order to reduce such a non-ideal effect, storage capacitor (Cst) has to be designed as greater as possible to meet the ideal case in Eq. (4.4). However, it will become a trade off to the LCD's aperture ratio. The row time of this work is approximately 25μs and which limits the aspect ratio of M1 and M2 to charge the output. The simulation results show that the aspect ratio of 3μm/5μm is quite enough for the output loading of real pixel (300fF) in TFT-LCDs. On the contrary for the measurement consideration, the larger aspect ratio of 30μm/5μm has to be designed for the output loading of oscilloscope (10pF) and it leads to greater parasitic capacitance. Therefore, the storage capacitor (Cst=5pF) is applied to verify the functionality of the proposed circuits. The comparison of the conventional storage capacitor is about 0.2pF to 0.3pF.

Although equal threshold voltage shifts is applied in the proposed analog memory cell II in Fig. 4.7, the different threshold voltage shifts should be concerned in the real devices. When the stress poses different threshold voltage shifts between M1 and M2, the error rate (the output voltage difference (ΔV in Fig. 4.7) dividing the threshold voltage difference) of the proposed analog memory cell II becomes quite larger. Besides, the error rate is proportional to the difference value between the threshold voltage shifts of M1 and M2, since the threshold voltage of M1 is utilized to compensate the threshold voltage of M2 in the proposed analog memory cell II. Even though it can't compensate this difference value, the design concept still can decrease the effect of the equal threshold voltage shifts. Furthermore, the same Vref is utilized in the proposed analog memory cells under different input data. It can be derived that the higher input data (Vdata) results to larger inaccuracy for polarity inversion difference from the Eq. (4.2), Eq. (4.4), and Eq. (4.5). Nevertheless, the pixels are addressed in rows and columns in TFT-LCDs. The layout of Vref line should be parallel with the gate line (row) or source line (column) to control a large number of pixels. Therefore, the same Vref is applied in the measurement results under different input data.

4.4. Summary

Two proposed analog pixel memory cells for power saving application in TFT-LCDs have been successfully verified in a 3-μm LTPS process. The frame rate to refresh the static image can be reduced from 60Hz to 3.16Hz with the voltage decay at the output only less than 0.1V under the input data varies from 1V to 4V. Experimental results have successfully verified

that both of the proposed analog memory cells are suitable for the MIP application of high resolution. Besides, the compensation technique is used to improve the output voltage decay due to the threshold voltage drop.

Chapter 5

ESD Protection Design for 60GHz LNA with Inductor-Triggered SCR in 65nm CMOS Process

Large scale integration (LSI) mounted on-panel area is primarily used to minimize footprint of the IC and suited to handling high-frequency (RF) signals. However, since the RF front-end circuits connect the RF transceiver to the external antenna or band-select filter, they must need electrostatic discharge (ESD) protections. The ESD protection devices at the I/O pads inevitably cause parasitic effects on the signal path and lead to the design challenge for on-panel RF circuits, which is to achieve the highest ESD robustness with the smallest RF performance degradation. To effectively protect the radio-frequency (RF) circuits in nanoscale CMOS technology from electrostatic discharge (ESD) damages, the silicon-controlled rectifier (SCR) devices have been used as main on-chip ESD protection devices due to their high ESD robustness and low parasitic capacitance. In this chapter, an SCR device assisted with an inductor is proposed to improve the turn-on efficiency for ESD protection. Besides, the inductor can be also designed to resonate with the parasitic capacitance of the SCR device at the selected frequency band for RF performance fine tuning. Experimental results of the ESD protection design with inductor-triggered SCR in a nanoscale CMOS process have been successfully verified at 60GHz frequency. The ESD protection design with inductor-triggered SCR has been implemented in cell configuration with compact size, which can be directly used in the RF receiver circuits. To verify the RF characteristics and ESD robustness in the RF receiver, the inductor-triggered SCR has been applied to a 60GHz low-noise amplifier (LNA). Verified in a silicon chip, the 60GHz LNA with the inductor-triggered SCR can achieve good RF performances and high ESD robustness.

5.1. Background

The 60GHz frequency band has been allocated for unlicensed usage in the next-generation wireless communications [60]. The radio-frequency (RF) circuits operating at

this 60-GHz frequency have the benefits of excellent interference immunity, high security, multi-gigabit speed, and frequency re-usable, due to short transmission distance [61]. Several RF transceivers operated at this frequency had been realized in CMOS technologies [62], [63]. Nanoscale CMOS technologies have been used to implement RF circuits with the advantages of scaling-down feature size, improving high-frequency characteristics, low power consumption, high integration capability, and low cost for mass production. However, the thinner gate oxide in nanoscale CMOS technology seriously degrades the electrostatic discharge (ESD) robustness of IC products [64]. The general requirement for a commercial IC product is to pass 2-kV human-body-model (HBM) ESD tests [65]. Therefore, an on-chip ESD protection circuit must be added at the first stage of the RF receiver. As shown in Fig. 5.1, the ESD protection circuit is added to the input (RF_{IN}) pad of the low-noise amplifier (LNA) against ESD damages. Several ESD protection designs have been reported for RF circuits [66], [67]. Some ESD protection designs used for 60GHz RF LNA were also presented [68]-[71]. To minimize the impacts from the ESD protection circuit on RF performances, the ESD protection circuit at the input pads must be carefully designed.

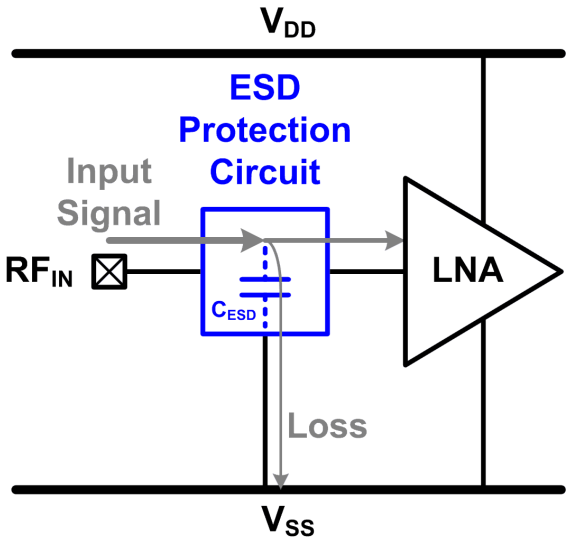


Fig. 5.1. ESD protection circuit added to the input (RF_{IN}) pad of LNA against ESD damages.

ESD protection devices cause RF performance degradation with several undesired effects [72], [73]. The parasitic capacitance (C_{ESD}) of the ESD protection device is one of the most important design considerations for RF circuits. Conventional ESD protection devices with large dimensions have large parasitic capacitances, which are difficult to be well tolerated in the RF front-end circuits. The parasitic capacitance will cause signal loss from the

pad to ground. Moreover, the parasitic capacitance will change the input matching condition. Besides, adding an ESD protection device to the RF receiver will degrade the noise figure. As the operating frequencies of RF circuits are further increased, on-chip ESD protection designs for RF applications are more challenging.

Among the ESD protection devices, such as the diode, MOS, BJT, or field-oxide device, the silicon-controlled rectifier (SCR) device has been reported to be useful for RF ESD protection design due to its higher ESD robustness within a smaller layout area and lower parasitic capacitance [74]. Besides, the SCR device can be safely used without latchup danger in advanced CMOS technologies with low supply voltage [75]. The device structure of the SCR device used in RF input pad is illustrated in Fig. 5.2(a). The RF_{IN} pad is connected to the first P+, which is formed in the N-well. The V_{DD} pad is connected to the pickup N+, which is formed in the same N-well. The V_{SS} pad is connected to the second N+ and the pickup P+, which are formed in the nearby P-well. The trigger port is connected to the third P+, which is formed in the same P-well. The SCR path between RF_{IN} and V_{SS} consists of P+, N-well, P-well, and N+. Besides, the parasitic diode path between RF_{IN} and V_{DD} consists of P+ and N-well/N+. The equivalent circuit of the SCR consists of a PNP BJT (Q_{PNP}) and a NPN BJT (Q_{NPN}), as shown in Fig. 5.2(b). The Q_{PNP} is formed by the P+, N-well, and P-well, and the Q_{NPN} is formed by the N-well, P-well, and N+. As ESD zapping from RF_{IN} to V_{SS}, the positive-feedback regenerative mechanism of Q_{PNP} and Q_{NPN} results in the SCR device highly conductive to make SCR very robust against ESD stresses. Under RF circuit operating conditions, the diode and SCR paths remain off to prevent from leakage. However, SCR has some drawbacks, such as higher trigger voltage and slower turn-on speed. To reduce the trigger voltage of an SCR device, the trigger signal can be sent into the base terminal of Q_{NPN} to enhance the turn-on speed. The voltage level of the trigger port is in reverse proportion to the trigger voltage of the SCR device. Therefore, some circuit design techniques are reported to enhance the turn-on efficiency of SCR devices, such as the gate-coupled, substrate-triggered, and gate-grounded-NMOS-triggered (GGNMOS-triggered) techniques [75]. Besides, some SCR devices with lower trigger voltage for RF applications are also presented, such as the diode-triggered SCR (DTSCR) [76]. However, adding a trigger circuit to SCR device also increases the parasitic capacitance seen at the RF_{IN} pad, which is hard to tolerate for RF circuits, especially in the 60GHz operating frequency.

In this chapter, a novel inductor-triggered SCR design is proposed for effective on-chip RF ESD protection for 60GHz frequency. The inductor acts as a conductive path to trigger the SCR device under ESD stress conditions. Besides, the inductor is used to compensate the

parasitic capacitance of ESD protection device under normal RF circuit operating conditions [77], [78]. This design can achieve low trigger voltage, fast turn-on speed, high ESD robustness, and low RF performance degradation. Without additional process modification, this inductor-triggered SCR design is realized by circuit and layout skills in a 65nm CMOS process.

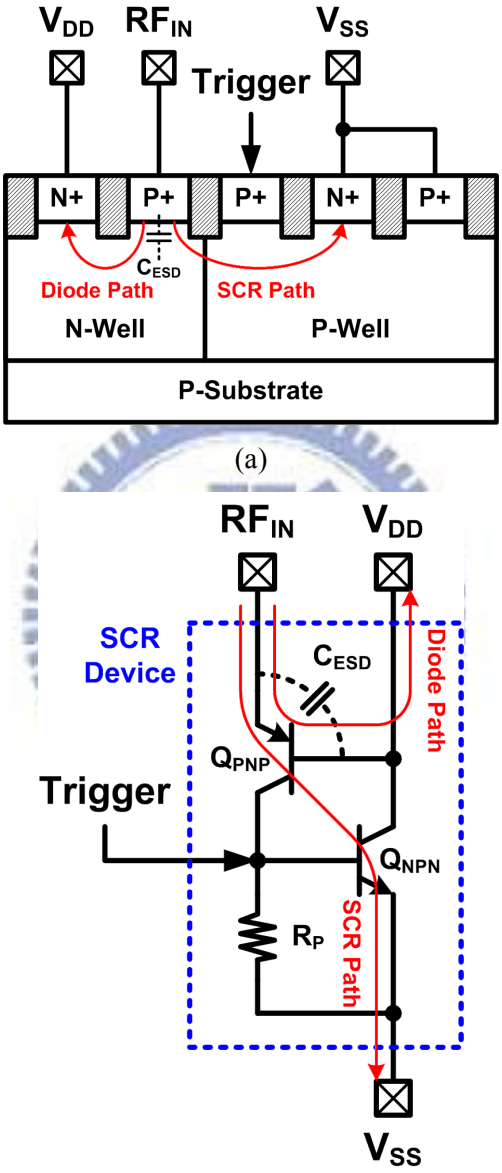


Fig. 5.2. (a) Device cross-sectional view, and (b) equivalent circuit, of SCR device used in RF input pad.

5.2. Realization of Inductor-Triggered SCR

5.2.1. Inductor-Triggered SCR Design

The new proposed inductor-triggered SCR is shown in Fig. 5.3, which consists of an SCR device, an inductor (L_{trig}), a MOS transistor (M_{trig}), and the RC-based ESD detection circuit. The PMOS transistor is selected for M_{trig} since it exhibits the initial-on function for ESD protection, which can quickly pass the trigger signal to SCR device [79]. The inductor is used to provide the trigger path between the RF_{IN} pad and the trigger port of the SCR device under ESD stress conditions. The PMOS transistor at the trigger path, which is controlled by the ESD detection circuit, is also turned on under ESD stress conditions. When the trigger signal passes from the RF_{IN} pad to the trigger port of the SCR device, the SCR device can be quickly turned on to discharge the ESD current. The RC-based ESD detection circuit is used to distinguish the ESD-stress conditions from the normal circuit operating conditions. Therefore, under normal power-on conditions, the PMOS transistor is turned off to block the steady leakage current path from the RF_{IN} pad to the trigger port of SCR device. Under normal RF circuit operating conditions, the inductor in series with the PMOS is used to compensate the parasitic capacitance of the SCR device (C_{ESD}).

Fig. 5.4 shows the proposed ESD protection scheme for an RF receiver, including the inductor-triggered SCR, the diode (D_N), and the power-rail ESD clamp circuit. The inductor-triggered SCR assisted with the diode (D_N) and the power-rail ESD clamp circuit is used to provide the ESD current discharging paths for the RF_{IN} pad. The power-rail ESD clamp circuit, which consists of the RC-inverter-triggered NMOS, is used to provide ESD current paths between V_{DD} and V_{SS} under ESD stress conditions. The R (~10kΩ) and C (~10pF) with the time constant of 0.1μs ~ 1μs can distinguish the ESD transients from the normal circuit operating conditions. Under normal circuit operating conditions, the node between R and C is charged to the high potential (V_{DD}). Under ESD stress conditions, the ESD voltage at V_{DD} has the fast rise time in the order of ~10ns. With the RC delay, the power-rail ESD clamp circuit is turned on to provide ESD current path from V_{DD} to V_{SS}. Since the power-rail ESD clamp circuit is placed between V_{DD} and V_{SS}, the impact on RF_{IN} pad is minor. The RC used in the power-rail ESD clamp circuit can also be used to control the PMOS in the inductor-triggered SCR. With such a configuration, the resistor for ESD detection circuit in the original inductor-triggered SCR can be merged into the power-rail ESD clamp circuit.

In the ESD protection design with the inductor-triggered SCR, the dimensions of the inductor (L_{trig}), PMOS transistor (M_{trig}), SCR device, and diode (D_N) can be designed to minimize the RF performance degradation. Since the capacitor used in power-rail ESD clamp circuit is large enough (~10 pF) to keep the node between R and C at ac ground under normal

RF circuit operating conditions, the impedance of the trigger path (Z_{trig}) seen at the RF_{IN} pad to ground can be calculated as

$$Z_{trig} \approx j\omega L_{trig} + \frac{1}{j\omega C_{trig}} = j\omega\left(L_{trig} - \frac{1}{\omega^2 C_{trig}}\right) \tag{5.1}$$

where the ω is the angular frequency and the C_{trig} can be expressed as

$$C_{trig} \approx C_{gs} + C_{gb}. \tag{5.2}$$

The C_{gs}, C_{gb}, and C_{db} denote the gate-to-source capacitance, gate-to-body capacitance, and drain-to-body capacitance of the PMOS transistor (M_{trig}), respectively. The resonance angular frequency (ω_o), which is designed to be the operating frequency of RF signal, can be obtained by

$$\omega_o = \frac{1}{\sqrt{\left(L_{trig} - \frac{1}{\omega_o^2 C_{trig}}\right) C_{ESD}}} \tag{5.3}$$

where the C_{ESD} is the parasitic capacitance contributed by the SCR and diode (D_N). The sizes of SCR and D_N depend on the required ESD robustness, while the size of M_{trig} transistor depends on the required trigger current. Once the sizes of M_{trig} transistor, SCR, and D_N have been chosen, the required inductance (L_{trig}) can be determined.

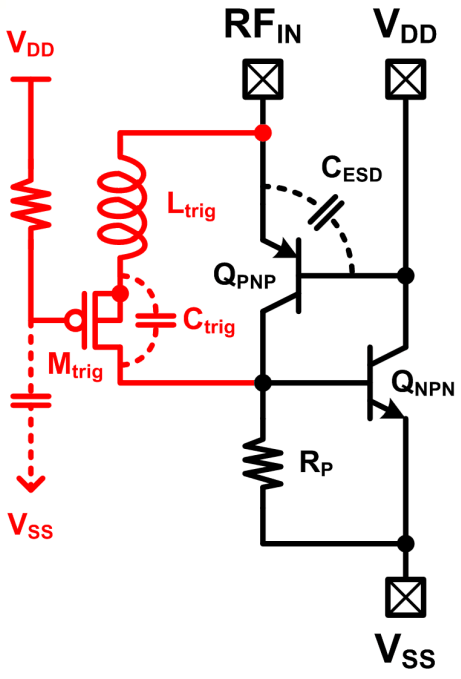


Fig. 5.3. Proposed inductor-triggered SCR for RF ESD protection.

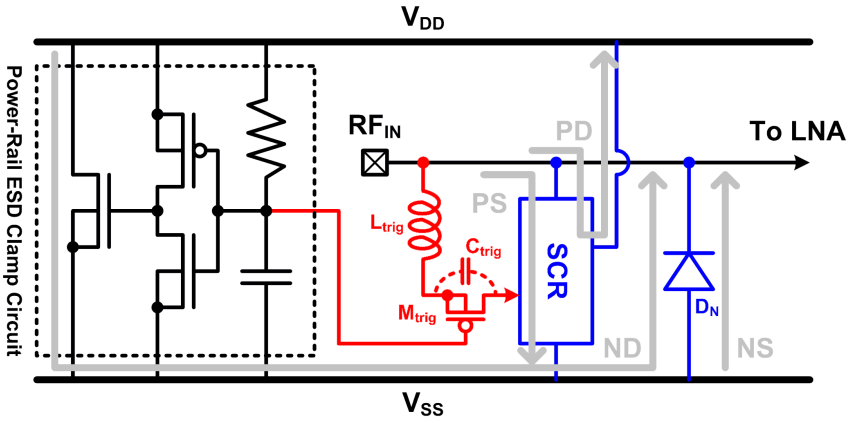


Fig. 5.4. Proposed ESD protection scheme for RF_{IN} pad with inductor-triggered SCR, D_N, and power-rail ESD clamp circuit.

Fig. 5.4 also shows the ESD current paths under positive-to-V_{SS} (PS), positive-to-V_{DD} (PD), negative-to-V_{SS} (NS), and negative-to-V_{DD} (ND) ESD stress conditions. During positive-to-V_{SS} ESD stress, ESD current will first pass through the inductor (L_{trig}) and PMOS (M_{trig}) to trigger the SCR device. The major ESD current will be discharged by the SCR device from the RF_{IN} pad to V_{SS}. Under positive-to-V_{DD} ESD stress, the ESD current will be discharged by the parasitic diode path embedded in the SCR device from the RF_{IN} pad to V_{DD}. During negative-to-V_{SS} ESD stress, the ESD current will be discharged by the forward-biased D_N from the V_{SS} to RF_{IN} pad. Under negative-to-V_{DD} ESD stress, the ESD current will be discharged by the power-rail ESD clamp circuit and the D_N from V_{DD} to RF_{IN} pad. The proposed ESD protection scheme in Fig. 5.4 can provide the corresponding current discharging paths with good ESD robustness.

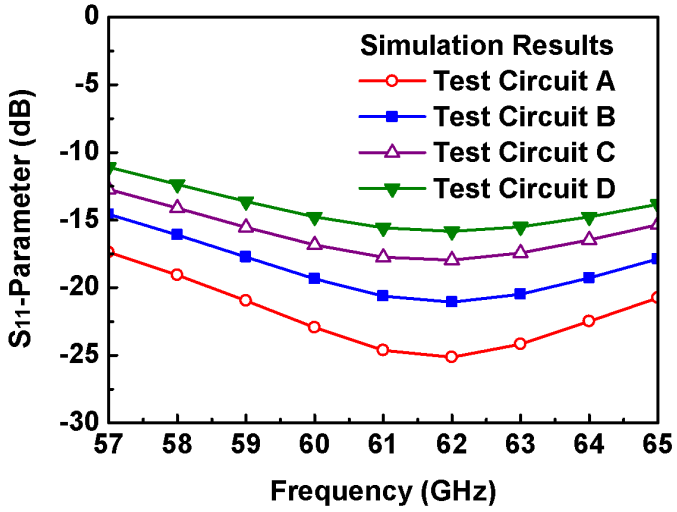
The device dimensions of the test circuits with the inductor-triggered SCR are listed in Table 5.1. A commercial 65nm CMOS technology is used in this chapter. The ESD protection circuit with the inductor-triggered SCR is designed for 60GHz RF applications. The test patterns include the test circuits A, B, C, and D. The size of SCR device used in the test circuits A, B, C, and D are split as 8μm, 15μm, 23μm, and 30μm, respectively. The size of D_N in test circuits A, B, C, and D are split as also 8μm, 15μm, 23μm, and 30μm, respectively. The parasitic capacitance (C_{ESD}) of ESD protection devices in test circuits A, B, C, and D at 60GHz are estimated as ~25fF, ~50fF, ~75fF, and ~100fF, respectively. The width / length of PMOS (M_{trig}) in each test circuit is kept at 100μm / 0.2μm, and the equivalent C_{trig} is ~50fF at 60GHz. Therefore, the required inductors (L_{trig}), including the parasitic inductance of metal connections, are ~0.38nH, ~0.27nH, ~0.23nH, and ~0.2nH for the test circuits A, B, C, and D.

5.2.2. Simulation Results of Inductor-Triggered SCR

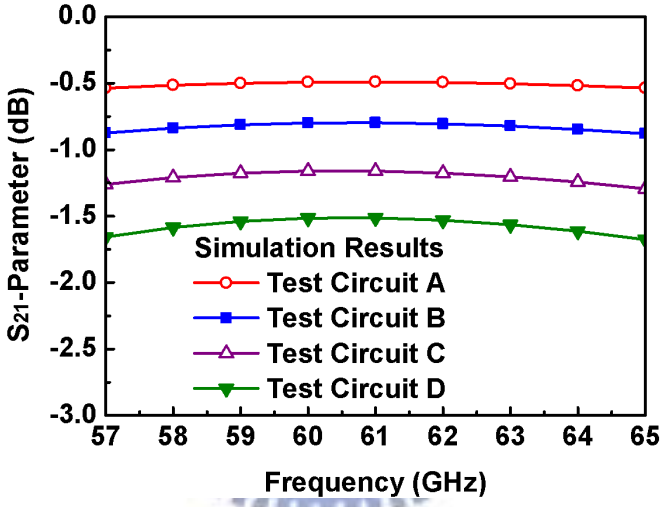
The RF characteristics of the test circuits are simulated by using the microwave circuit simulator ADS with the selected device dimensions. Since the SCR model is not provided in the given CMOS process, diodes with P+/N-well, N+/P-well, and N-well/P-well junctions are used to simulate the SCR devices. A signal source with 50-Ω impedance drives the port 1 (RF_{IN} pad) of the test circuit, and a 50-Ω load is connected to the port 2 to simulate the RF receiver. The voltage supply of V_{DD} (V_{SS}) is 1V (0V), and the dc bias of RF_{IN} is 0.5V. The simulated reflection (S_{11}) parameters are shown in Fig. 5.5(a). These ESD protection circuits exhibit good input matching (S_{11}-parameters < -10 dB) around 60GHz. The transmission (S_{21}) parameters are compared in Fig. 5.5(b). At 60GHz frequency, the test circuits A, B, C, and D have about 0.5dB, 0.8dB, 1.2dB, and 1.5dB power loss, respectively. Although the parasitic capacitance of the ESD protection devices can be resonated out, the losses are still contributed by the parasitic resistance of the SCR and D_N. Since these test circuits exhibit good RF performances between 57~65GHz, they can be operated at 60GHz even if some variation happens on device values.

The test circuits under normal power-on conditions and ESD transient events are simulated by using HSPICE. Under the normal power-on condition, the dc bias of RF_{IN} is raised from 0V to 1V with 1-ms rise time. The gate voltage of PMOS (M_{trig}) is biased at 1 V through the resistor of power-rail ESD clamp circuit, so M_{trig} can be kept off and no trigger signal is generated from the RF_{IN} pad to the SCR device. Fig. 5.6(a) shows the HSPICE-simulated voltage waveforms of the test circuit D under the normal power-on condition. The trigger signal remains at 0V, so the SCR device is kept in off state.

When a positive fast-transient ESD voltage is applied to RF_{IN} with V_{SS} grounded, the RC delay in the ESD detection circuit keeps the gate of M_{trig} at a relatively low voltage level compared to the fast rising voltage level at RF_{IN}. The M_{trig} can be quickly turned on by the ESD energy to generate the trigger signal into the trigger port of the SCR device. Finally, the SCR device can be fully turned on to discharge ESD current from RF_{IN} to V_{SS}. Fig. 5.6(b) shows the simulated voltage waveforms of the test circuit D under the ESD transition, where a 0V to 5V voltage pulse with 10-ns rise time is applied to RF_{IN} to simulate the fast transient voltage of human-body-model (HBM) ESD event [65]. With the limited voltage height of 5V in the voltage pulse, the simulation results can check the desired trigger function before the RF circuit breakdown.



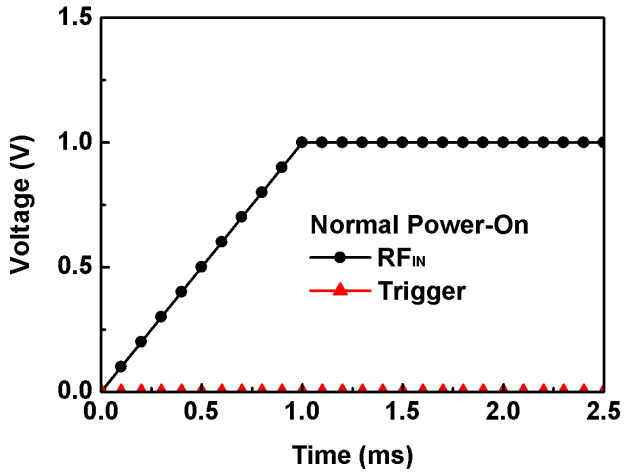
(a)



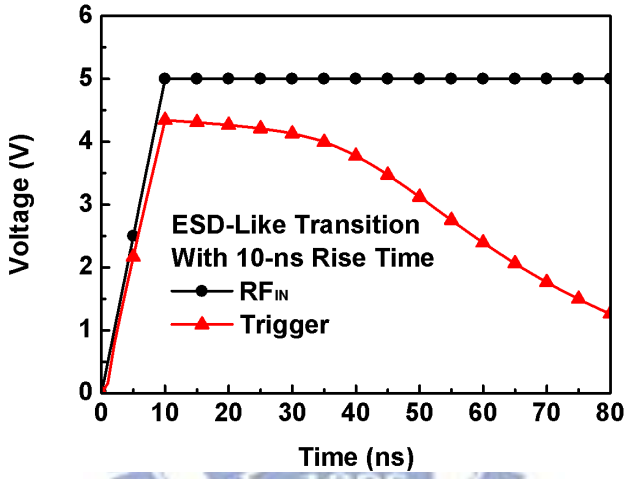
(b)

Fig. 5.5. Simulation results of proposed ESD protection scheme on (a) S_{11}-parameter and (b) S_{21}-parameter.

Fig. 5.6(c) shows the simulated voltage waveforms of the test circuit D under the other ESD transition, where a 0V to 5V voltage pulse with 0.1-ns rise time is applied to RF_{IN} to simulate the faster transient voltage of charged-device-model (CDM) ESD event [65]. With the large enough trigger signal, the SCR device should be triggered on before RF circuit breakdown during ESD stress condition.



(a)



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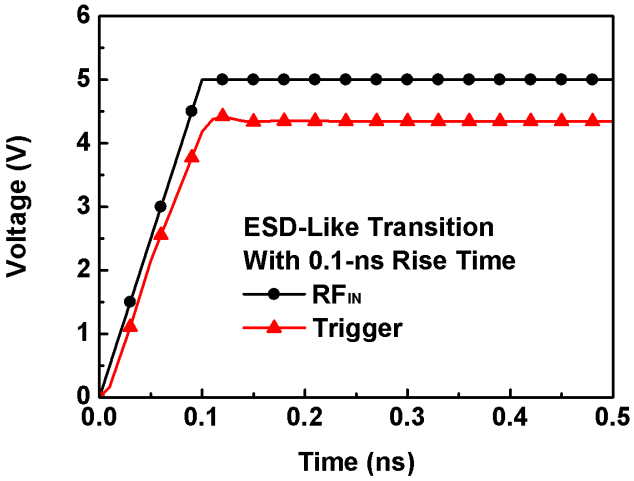


(c)

Fig. 5.6. HSPICE-simulated results of proposed ESD protection scheme under (a) normal power-on condition, (b) ESD-like transition with 10-ns rise time, and (c) ESD-like transition with 0.1-ns rise time.

5.3. Experimental Results of Inductor-Triggered SCR

The test circuits of inductor-triggered SCR have been fabricated in a 65nm salicided CMOS process without using the silicide-blocking mask. One set of the test circuits are implemented with ground-signal-ground (G-S-G) pads to facilitate on-wafer two-port S-parameters measurement, which are labeled as test circuits A, B, C, and D. The other set of the test circuits are implemented with the RF-NMOS emulators [71] for ESD tests, which are labeled as test circuits A', B', C', and D', as listed in Table 5.1. The RF-NMOS emulator, which consisted of one RF NMOS with gate terminal connected to the RF_{IN} pad, and the drain, source, and body terminals connected to V_{SS} pad, is used to simulate the RF receiver under ESD stress condition. The ESD robustness of the test circuits can be estimated by the test patterns with the RF-NMOS emulators. Except the RF-NMOS emulator, the device sizes of test circuits A, B, C, and D are equal to those of test circuits A', B', C', and D', respectively. The chip micrograph of the test circuit D is shown in Fig. 5.7.

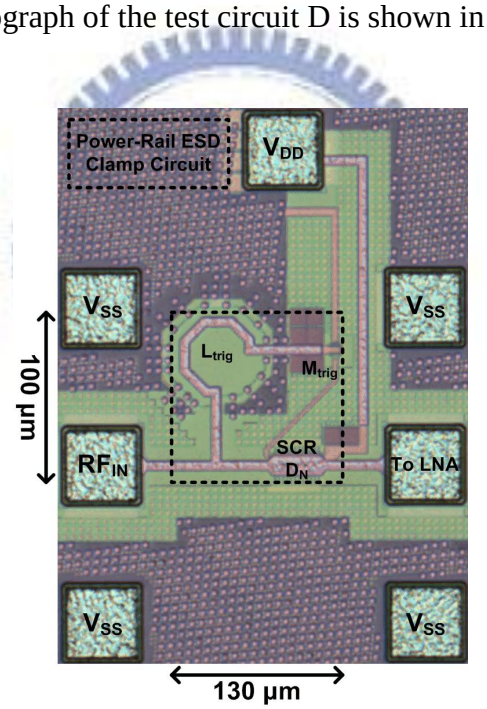


Fig. 5.7. Chip micrograph of test circuit D.

5.3.1. RF Performance of Inductor-Triggered SCR

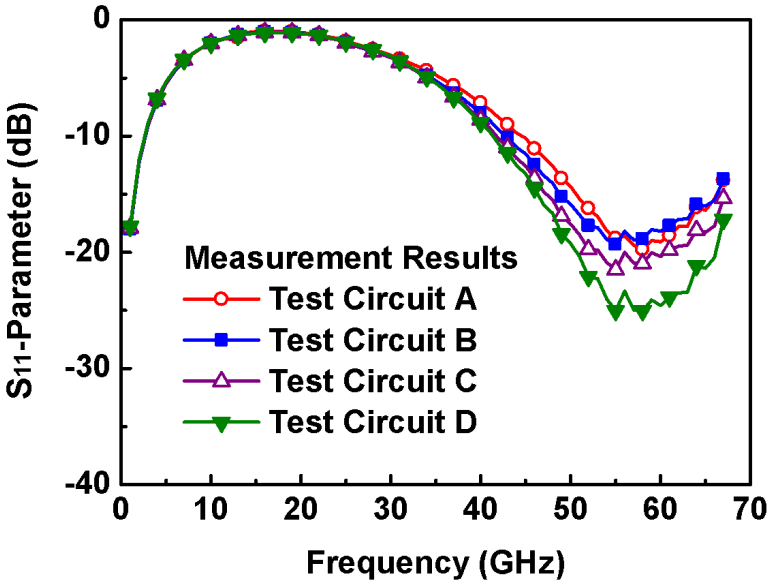
In order to extract the intrinsic characteristics of the test circuits in high frequencies, the parasitic effects of the G-S-G pads have been removed by using the L2L de-embedding technique [80]. With the on-wafer RF measurement, the S-parameters of these four test circuits have been extracted from 0GHz to 67GHz. The voltage supply of V_{DD} (V_{SS}) is 1V (0V), and the dc bias of RF_{IN} is 0.5 V (V_{DD}/2). The source and load resistances to the test

circuits are kept at 50-Ω. The measured S_{11}-parameters and S_{21}-parameters versus frequencies among the four test circuits are shown in Figs. 5.8(a) and 5.8(b), respectively. As shown in Fig. 5.8(a), these ESD protection circuits exhibit good input matching (S_{11}-parameters < -15dB) around 60GHz. At 60GHz frequency, the test circuits A, B, C, and D have about 1.2dB, 1.4dB, 1.6dB, and 1.8dB power loss, respectively.

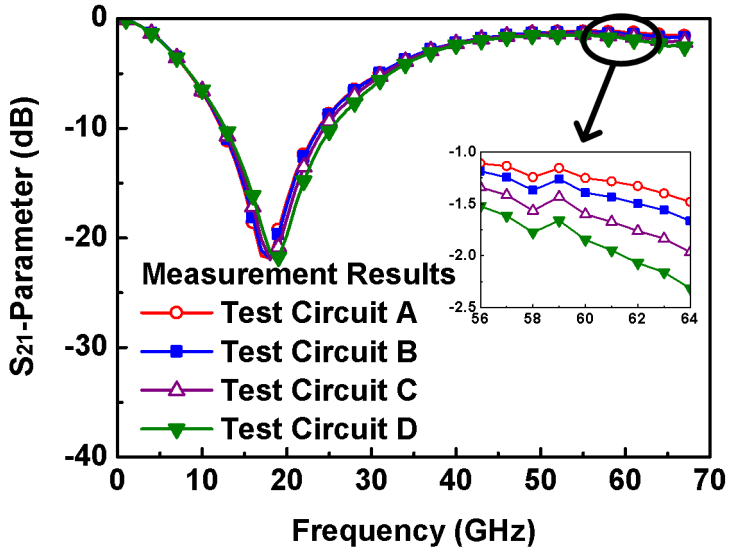
Table 5.1

Device Dimensions and Measurement Results of ESD Protection Designs

		Test Circuits							
		A	A'	B	B'	C	C'	D	D'
Device Dimensions	SCR (μm)	8		15		23		30	
	D_N (μm)	8		15		23		30	
	L_{trig} (nH)	0.38		0.27		0.23		0.2	
	M_{trig} (μm / μm)	100 / 0.2		100 / 0.2		100 / 0.2		100 / 0.2	
	Area (μm x μm)	120 x 150		110 x 140		105 x 135		100 x 130	
	RF-NMOS Emulator	w/o	w/i	w/o	w/i	w/o	w/i	w/o	w/i
Measurement Results	S_{11} at 60 GHz (dB)	-19.1		-18.2		-20.4		-24.6	
	S_{21} at 60 GHz (dB)	-1.24		-1.39		-1.60		-1.84	
	PS HBM ESD Level (kV)		0.75		1.5		2.25		2.75
	PD HBM ESD Level (kV)		1		1.5		2.25		2.75
	NS HBM ESD Level (kV)		0.75		1.5		2.25		3
	ND HBM ESD Level (kV)		0.75		1.5		2.25		3
	PS TLP-Measured It_2 (A)		0.37		0.72		1.39		1.78
	PS VF-TLP-Measured It_2 (A)	1.98	0.96	2.72	1.72	3.08	2.14	3.71	2.21



(a)



(b)

Fig. 5.8. Measurement results of (a) S_{11}-parameters and (b) S_{21}-parameters among the four test circuits with the proposed ESD protection scheme under different device dimensions.

5.3.2. ESD Robustness of Inductor-Triggered SCR

The human-body-model (HBM) ESD pulses are stressed to each test circuit under positive-to-V_{SS} (PS), positive-to-V_{DD} (PD), negative-to-V_{SS} (NS), and negative-to-V_{DD} (ND) ESD stress conditions. The failure criterion is defined as the I-V characteristics seen at RF_{IN} shifting over 30% from its original curve after ESD stressed at every ESD test level. In other words, the leakage current under 1-V bias at RF_{IN} will not increase over 30% if the test circuit is not failed after ESD stresses. The HBM ESD robustness among the four test circuits with the proposed ESD protection designs are listed in Table 5.1. The HBM ESD levels of the

proposed ESD protection circuits A', B', C', and D' can achieve 0.75-kV, 1.5-kV, 2.25-kV, and 2.75-kV, respectively, which are obtained from the lowest levels among PS, PD, NS, and ND ESD tests. The HBM ESD robustness of the test circuits is almost proportional to the sizes of ESD protection devices (SCR and D_N).

To investigate the turn-on behavior and the I-V characteristics in high-current regions of the inductor-triggered SCR, the transmission line pulsing (TLP) system with a 10-ns rise time and a 100-ns pulse width is used. The TLP-measured I-V curves of the ESD protection circuits A', B', C', and D' under positive-to-V_{SS} stress conditions are shown in Fig. 5.9. Once ESD pulses stressed to the test circuits, all SCR devices can be quickly triggered on to discharge ESD currents. The secondary breakdown current (It_2), which indicated the current-handling ability of ESD protection circuit, can also be obtained from the TLP-measured I-V curve. The test circuits A', B', C', and D' can achieve It_2 of 0.37A, 0.72A, 1.39A, and 1.78A, respectively. These second breakdown currents measured by TLP system are summarized in Table 5.1. The turn-on behavior and the It_2 values of the ESD protection circuits can ensure the effective ESD protection capability of the proposed inductor-triggered SCR.

To evaluate the effectiveness of the proposed ESD protection circuits in faster ESD-transient events, another very fast TLP (VF-TLP) system with 0.2-ns rise time and 1-ns pulse width is also used in this study. The VF-TLP system can be used to capture the transient behavior of ESD protection circuits in the time domain of charged-device-model (CDM) ESD event [82]. The VF-TLP-measured It_2 of the ESD protection circuits are also listed in Table 5.1. The tests circuits A', B', C', and D' with the RF-NMOS emulator can achieve VF-TLP-measured It_2 of 0.96A, 1.72A, 2.14A, and 2.21A, respectively. For comparison purpose, the tests circuits A, B, C, and D without the RF-NMOS emulator are also tested by VF-TLP system. They can achieve VF-TLP-measured It_2 of 1.98A, 2.72A, 3.08A, and 3.71A, respectively. The proposed inductor-triggered SCR is fast enough to be turned on under such a fast-transient pulse.

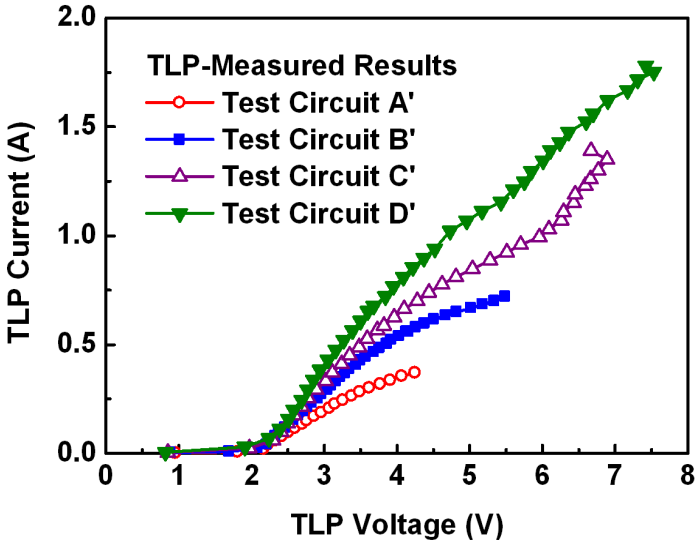


Fig. 5.9. TLP-measured I-V characteristics among the four test circuits with the proposed ESD protection scheme of different device dimensions under positive-to-V_{SS} tests.

5.3.3. Application to 60GHz LNA

One 60GHz LNA is designed in a commercial 65nm CMOS technology for verification purpose. The metal-insulator-metal (MIM) capacitors and polysilicon resistors are available in this process. Fig. 5.10 shows the schematic of the 60GHz LNA with ESD protection circuit of inductor-triggered SCR. In the two-stage LNA design, the cascode configuration is utilized to achieve high gain performance. The common-source and common-gate NMOS transistors are all with 36-μm gate width and 0.06-μm gate length. The input matching is designed for the minimum noise figure. The output matching network is conjugately matched for the maximum gain.

The 60GHz LNA circuits with ESD protection circuits A and D are included in silicon chip. Fig. 5.11 shows a chip photograph of the 60GHz LNA with the ESD protection circuit D. The layout size of this circuit is 400μm x 850μm, including all testing pads and dummy layers. The dummy layers are kept away from the signal paths, so they will not influence the RF signals. In order to verify the RF characteristics and ESD robustness, the stand-alone LNA without RF ESD protection is also fabricated for comparison. All the LNA circuits with and without ESD protection circuits are fabricated on the same wafer for comparison.

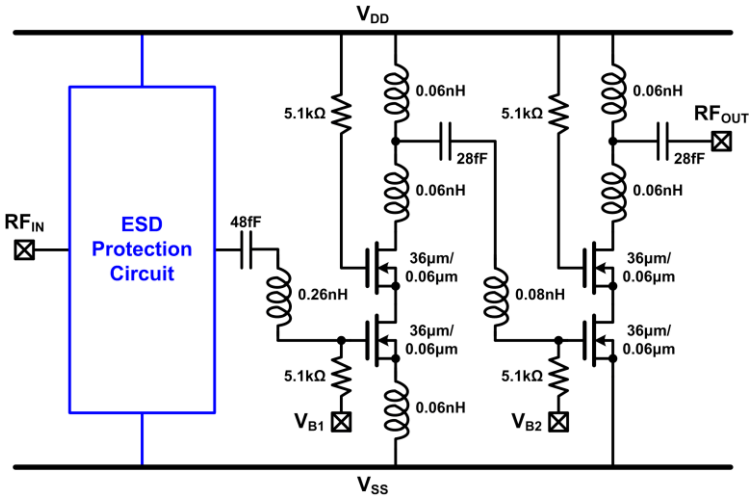


Fig. 5.10. Circuit schematic of 60GHz LNA with ESD protection circuit.

The RF characteristics are measured on wafer through G-S-G microwave probes with 100-μm pitch. The S-parameters are measured by using the Agilent E8361A PNA network analyzer. The short-open-load-thru calibration has been done before the measurements. Each LNA circuit operates with the 1-V V_{DD} supply and draws a total current of 30mA. The used bias voltages V_{B1} and V_{B2} are all 0.7V. The measured S_{11}-parameters and S_{21}-parameters of the LNA circuits are shown in Figs. 5.12(a) and 5.12(b), respectively. With the ESD protection circuits, the peak power-gain frequencies of all LNA circuits are at ~60GHz. The input return losses for all test circuits are greater than 10dB at 60GHz. The power gains at 60GHz are 11.1dB and 10.2dB for two ESD-protected LNA circuits, respectively, which reduced by 1.1dB and 2dB, as compared with the stand-alone LNA of 12.2dB.

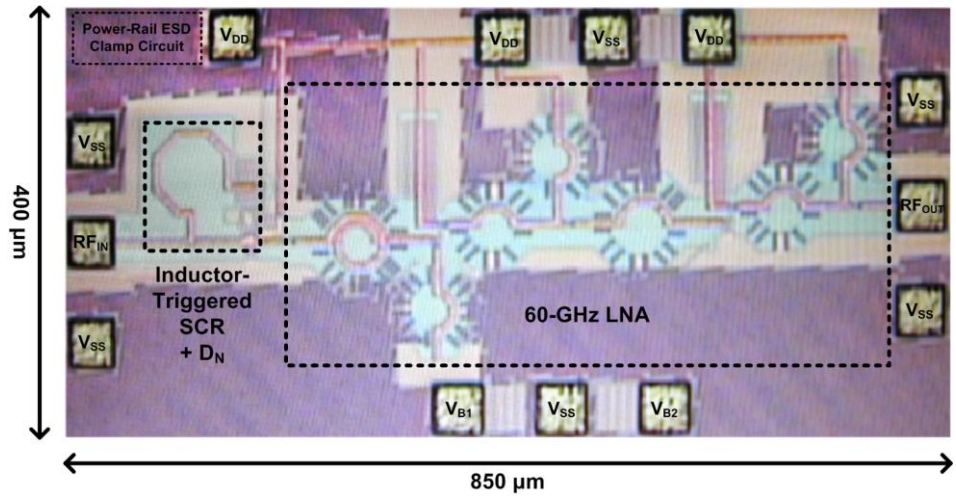
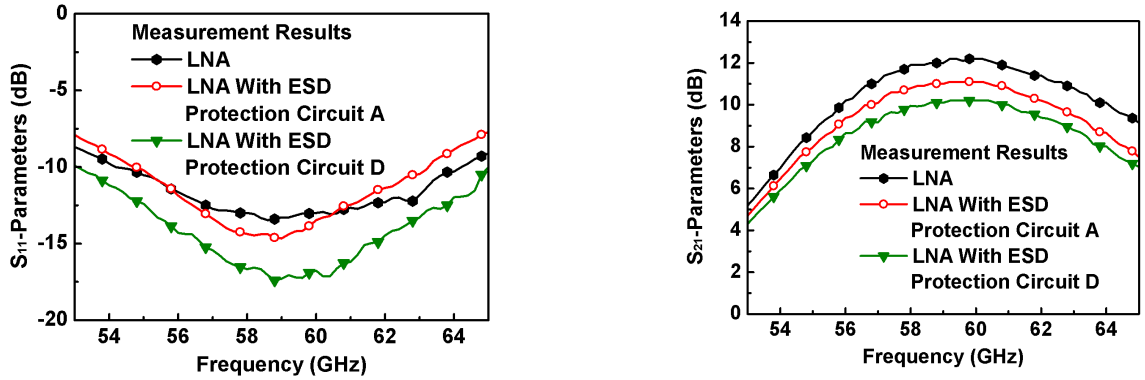


Fig. 5.11. Chip micrograph of 60GHz LNA with ESD protection circuit D.



(a) (b)

Fig. 5.12. Measurement results of (a) S_{11}-parameters and (b) S_{21}-parameters on 60GHz LNA with and without ESD protection circuits.

Table 5.2

Comparison Among 60GHz LNA with and without ESD Protection Designs in CMOS Technologies

LNA	Technology	Gain (dB)	Noise Figure (dB)	HBM ESD Level (kV)	ESD Protection Circuit Area (μm x μm)
Without ESD Protection (Chapter 5)	65nm	12.2	6.5	< 0.1	0
With ESD Protection Circuit A (Chapter 5)	65nm	11.1	7.5	0.5	120 x 150
With ESD Protection Circuit D (Chapter 5)	65nm	10.2	8.6	3	100 x 130
With ESD Protection Diodes and Inductors in Series (Ref. [68])	130nm	20.4	8.6	1.5	400 x 180
With ESD Protection Diodes (Ref. [69])	45nm	23	8.5	1.25	N/A
With ESD Protection Inductor (Ref. [70])	40nm	13	8	4.75	N/A

Under the same bias condition, the noise figures and the output power versus input power of the LNA with and without ESD protection circuits are shown in Figs. 5.13 and 5.14, respectively. The measured noise figures at 60GHz of two ESD-protected LNA circuits are 7.5dB and 8.6dB, respectively, and that of the stand-alone LNA is 6.5 dB, as shown in Table 5.2. The input 1-dB compression point (P_{1dB}) of two ESD-protected LNA circuits are -11 dBm, and that of the stand-alone LNA is -12 dBm.

To compare the ESD protection capability among the LNA with and without ESD

protection circuits, the RF performances of all LNA circuits after ESD stresses are re-measured. All positive-to-V_{SS}, positive-to-V_{DD}, negative-to-V_{SS}, and negative-to-V_{DD} HBM ESD stresses are zapped to RF_{IN} pad of each test circuit. The S_{21}-parameters of three LNA circuits after various ESD stresses are shown in Figs. 5.15(a), 5.15(b), and 5.15(c). The power gain of the stand-alone LNA is severely degraded after 100-V HBM ESD stresses, as seen in Fig. 5.15(a). In contrast, the power gains of the LNA with ESD protection circuit A and that with ESD protection circuit D are still excellent matching after 500-V and 3-kV HBM ESD stresses, respectively, as seen in Figs. 5.15(b) and 5.15(c).

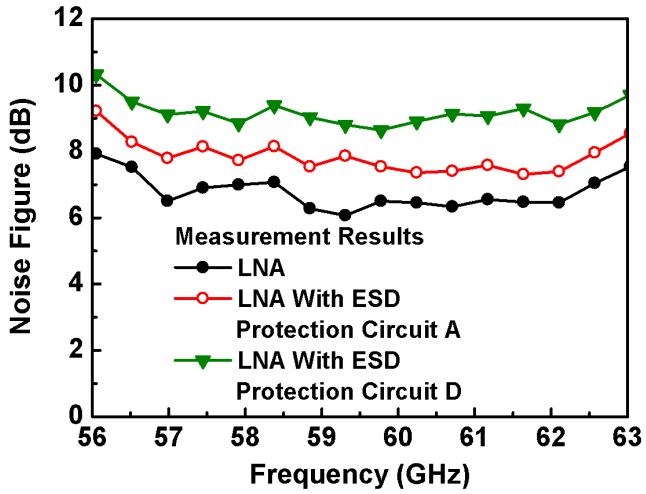


Fig. 5.13. Measurement results of noise figures on 60-GHz LNA with and without ESD protection circuits.

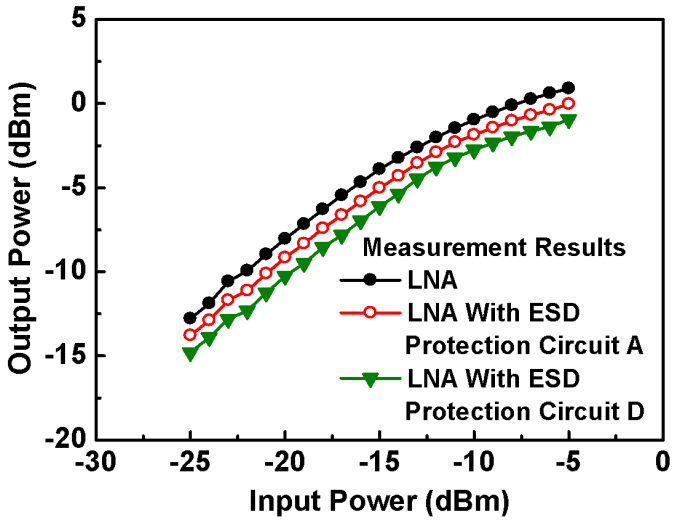
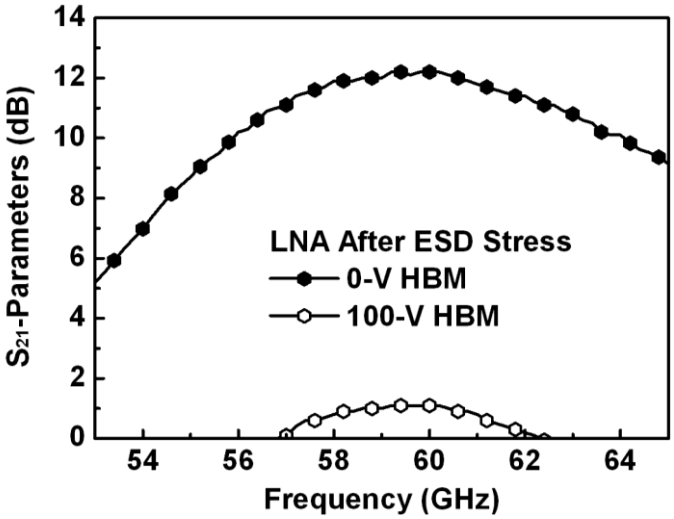
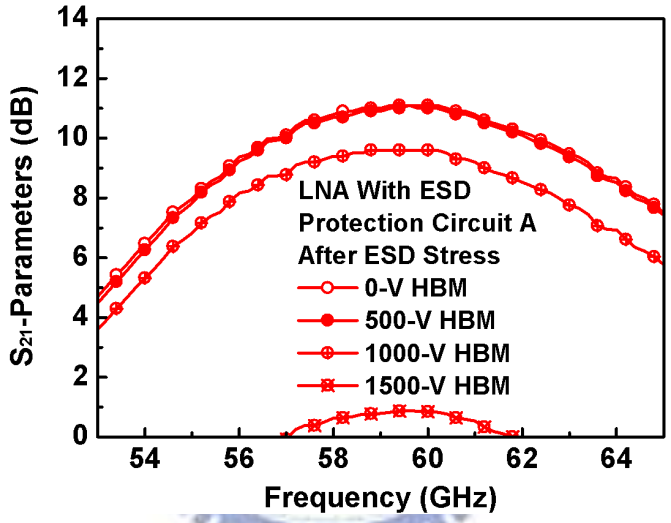


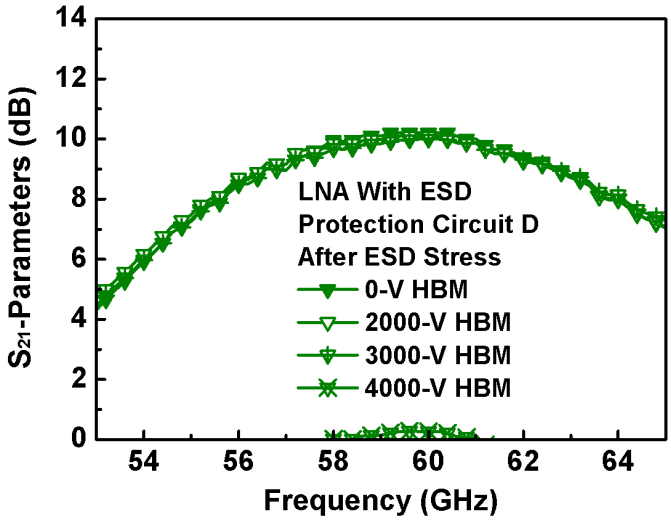
Fig. 5.14. Measurement results of output power versus input power on 60-GHz LNA with and without ESD protection circuits.



(a)



(b)



(c)

Fig. 5.15. Measurement results on S_{21}-parameters of (a) LNA without ESD protection, (b) LNA with ESD protection circuit A, and (c) LNA with ESD protection circuit D, after PS, PD, NS, and ND

HBM ESD stresses.

For comparison, Table 5.2 summarizes and compares the previously reported 60GHz ESD-protected LNA [68]-[70] and the circuits of this chapter. The ESD protection circuit D can provide the required 2-kV HBM ESD robustness with 100×130μm^2 layout area and little RF performance degradation. Moreover, the proposed design has been implemented in cell configuration, which can be directly applied to the 60GHz RF LNA. Therefore, the proposed ESD protection design in this paper is more suitable for RF circuit designer for them to easily apply ESD protection in the 60GHz RF LNA.

5.4. Summary

The new ESD protection scheme with inductor-triggered SCR has been designed, fabricated, and characterized in a 65nm CMOS process. The inductor-triggered SCR is designed to achieve low trigger voltage and high turn-on speed. Moreover, these inductor-triggered SCR can reach the input/output matching with low S_{11}-parameters and high S_{21}-parameters. These ESD protection circuits are developed to support RF circuit designers for them to easily apply ESD protection in the 60GHz RF receiver circuits. Verified in a commercial 65nm CMOS process, the test circuits A, B, C, and D have about 1.2dB, 1.4dB, 1.6dB, and 1.8dB power loss at 60GHz frequency, respectively. Besides, they can sustain 0.75-kV, 1.5-kV, 2.25-kV, and 2.75-kV HBM ESD tests, respectively. The VF-TLP-measured It_2 of these test circuits are also provided, which are 0.96A, 1.72A, 2.14A, and 2.21A, respectively. The test circuits with inductor-triggered SCR have been applied to the 60GHz LNA to confirm the ESD protection ability and to verify the RF performances. The RF performances of the LNA with ESD protection circuit A and that with ESD protection circuit D are still maintained after 500-V and 3-kV HBM ESD tests are performed, respectively. The inductor-triggered SCR can be further applied to other circuit blocks in the RF transceiver without dc blocking capacitor. Therefore, the proposed ESD protection scheme can be widely used to achieve good RF performance and high ESD robustness simultaneously.

Chapter 6

Dual-Band ESD Protection for 24/60 GHz Millimeter-Wave Circuits

To effectively protect the millimeter-wave (MMW) circuits in nanoscale CMOS technology from electrostatic discharge (ESD) damages, a dual-band ESD protection cell for 24/60 GHz ESD protection was presented in this chapter. The proposed ESD protection cell consisted of a diode, a silicon-controlled rectifier (SCR), a PMOS, and two inductors. To verify the dual-band characteristics and ESD robustness, the proposed ESD protection circuit had been applied to a 24/60 GHz low-noise amplifier (LNA). Measurement results showed over 2.75-kV human-body-model (HBM) ESD robustness with little performance degradation on LNA. The proposed dual-band ESD protection cell was suitable for circuit designers for them to easily apply ESD protection in the dual-band MMW circuits.

6.1. Background

A clear trend in wireless applications during recent years has been pushing towards to higher integration and multi-band operation, in order to enable low-cost high-functionality. Millimeter-wave (MMW) circuits become more attractive for many applications such as automotive radar sensors at 24/77 GHz and wireless communications at 24/60 GHz [83], [84]. Several dual-band MMW transceivers operated at these frequency bands have been realized [85], [86]. Nanoscale CMOS technologies have been widely used to implement radio-frequency (RF) and MMW circuits with the advantages of scaling-down feature size, improving high-frequency characteristics, low power consumption, high integration capability, and low cost for mass production. However, the thinner gate oxide in nanoscale CMOS technology seriously degrades the ESD robustness of IC products [66]. Therefore, on-chip ESD protection circuits must be added at all input/output (I/O) pads in ICs [87]-[90]. To support the dual-band MMW applications and to lower the fabrication costs, a dual-band ESD protection cell is needed. Fig. 6.1 presents the dual-band ESD protection circuit which is added to the input (RF_{IN}) pad of the dual-band low-noise amplifier (LNA) against ESD

damages. To minimize the impacts from the dual-band ESD protection circuit on RF performances, the dual-band ESD protection circuit at the input pads should be carefully designed.

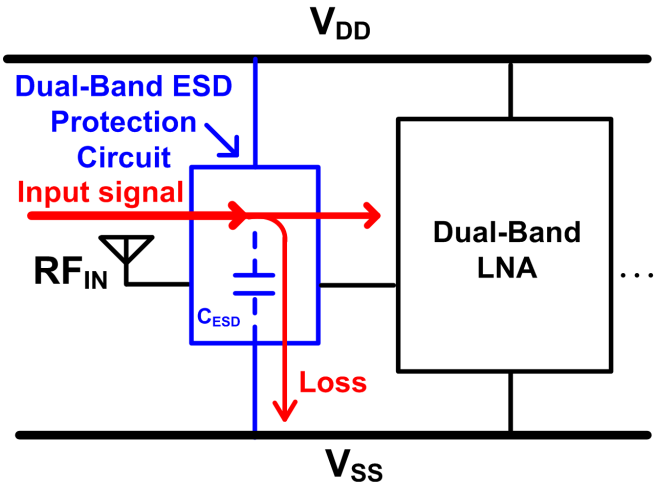


Fig. 6.1. Dual-band ESD protection circuit added to the input (RF_{IN}) pad of dual-band LNA against ESD damages.

ESD protection devices cause the circuit performance degradation with several undesired effects [72]-[73], [91]. The parasitic capacitance (C_{ESD}) of the ESD protection device is one of the most important design considerations for MMW circuits. Conventional ESD protection devices with large dimensions have large parasitic capacitances, which are difficult to be well tolerated in the MMW circuits. The parasitic capacitance will cause signal loss from the pad to ground. Moreover, the parasitic capacitance will change the input matching condition. Besides, adding an ESD protection device to the MMW receiver will degrade the noise figure. As the operating frequencies of MMW circuits are further increased, on-chip ESD protection designs for MMW circuits are more challenging. Among the ESD protection devices, silicon-controlled rectifier (SCR) device has been reported to be useful for RF ESD protection design due to its high ESD robustness within a small layout area and low parasitic capacitance [75]-[77], [87]. Besides, the SCR device can be safely used without latchup danger in advanced CMOS technologies with low supply voltage. The device structure of the SCR device used in RF input (RF_{IN}) pad is illustrated in Fig. 6.2. The SCR path between RF_{IN} and V_{SS} consists of P+, N-well, P-well, and N+. Besides, the parasitic diode path between RF_{IN} and V_{DD} consists of P+ and N-well/N+. However, SCR has some drawbacks, such as higher trigger voltage and slower turn-on speed. To reduce the trigger

voltage of an SCR device, the trigger signal can be sent to enhance the turn-on speed. Some design techniques have been reported to enhance the turn-on efficiency of SCR devices [75]. However, adding a trigger circuit to SCR device also increases the parasitic capacitance seen at the RF_{IN} pad, which is hard to tolerate for MMW circuits. In this chapter, a novel SCR design is proposed for dual-band ESD protection at 24/60 GHz. Such ESD protection circuits have been successfully designed and applied to 24/60 GHz LNA in a 65nm CMOS process.

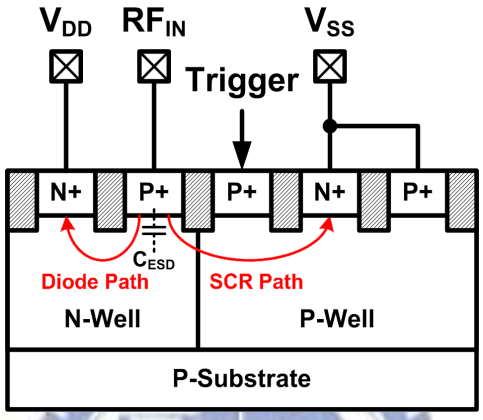


Fig. 6.2. Device cross-sectional view of SCR device used in RF_{IN} pad.

6.2. Proposed Dual-Band ESD Protection Design

The proposed dual-band ESD protection cell is shown in Fig. 6.3, which consists of a diode (D_N), an SCR, a PMOS (M_1), two inductors (L_1 and L_2), and a power-rail ESD clamp circuit. The L_1 is used to provide the trigger path between the RF_{IN} pad and the trigger port of the SCR device under ESD stress conditions. The resistor and capacitor used in the power-rail ESD clamp circuit are used to control the M_1. The M_1 at the trigger path is also turned on under ESD stress conditions. When the trigger signal passes from the RF_{IN} pad to the trigger port of the SCR device, the SCR device can be quickly turned on to discharge the ESD current. Fig. 6.3 also shows the ESD current paths under positive-to-V_{SS} (PS), positive-to-V_{DD} (PD), negative-to-V_{SS} (NS), and negative-to-V_{DD} (ND) ESD stress conditions. During PS ESD stress, ESD current will first pass through the L_1 and M_1 to trigger the SCR device. The major ESD current will be discharged by the SCR device from the RF_{IN} pad to V_{SS}. Under PD ESD stress, the ESD current will be discharged by the parasitic diode path embedded in the SCR device from the RF_{IN} pad to V_{DD}. During NS ESD stress, the ESD current will be discharged by the forward-biased D_N and L_2 from the V_{SS} to RF_{IN} pad. Under

ND ESD stress, the ESD current will be discharged by the power-rail ESD clamp circuit, D_N, and L_2 from V_{DD} to RF_{IN} pad. The proposed dual-band ESD protection scheme in Fig. 6.3 can provide the corresponding current discharging paths with good ESD robustness.

Under normal power-on conditions, the M_1 is turned off to block the steady leakage current path from the RF_{IN} pad to the trigger port of SCR device. Under normal circuit operating conditions, there are two series LC resonators in this circuit. The resonant frequency of series L_1 and C_1 is designed <24GHz, while that of the series L_2 and C_D is designed at 24GHz~60 GHz, where C_1 and C_D denote the capacitances of M_1 and D_N, respectively. As the frequency is higher than the resonant frequency of first series LC resonator and lower than that of second series LC resonator, the equivalent inductance (L_{eq1}) of the first series LC resonator can be expressed as

$$L_{eq1} = L_1 - \frac{1}{\omega^2 C_1} \tag{6.1}$$

and the equivalent capacitance (C_{eq2}) of the second series LC resonator can be expressed as

$$C_{eq2} = \frac{C_D}{1 - \omega^2 L_2 C_D} \tag{6.2}$$

where the ω is the angular frequency. The L_{eq1} can be used to eliminate the C_{eq2} and $C_{ESD,}$ where the C_{ESD} is the parasitic capacitance contributed by the SCR. The resonant frequency of parallel L_{eq1}, $C_{eq2,}$ and C_{ESD}, which is designed to be the first operating frequency (ω_{o1}) of MMW circuit, can be obtained by

$$\omega_{o1} = \frac{1}{\sqrt{L_{eq1}(C_{eq2} + C_{ESD})}} \tag{6.3}$$

Similarly, as the frequency is higher than the resonant frequency of second series LC resonator, the inductance dominated the impedance. The equivalent inductance (L_{eq2}) of second series LC resonator can be expressed as

$$L_{eq2} = L_2 - \frac{1}{\omega^2 C_D} \tag{6.4}$$

The resonant frequency of parallel L_{eq1}, L_{eq2}, and C_{ESD}, which is designed to be the second operating frequency (ω_{o2}) of MMW circuit, can be obtained by

$$\omega_{o2} = \frac{1}{\sqrt{(L_{eq1} // L_{eq2})C_{ESD}}} \tag{6.5}$$

The sizes of SCR and D_N depend on the required ESD robustness, while the size of M_1 depends on the required trigger current. Once the sizes of M_1, SCR, and D_N have been chosen, the required inductors (L_1 and L_2) can be determined through Eq. (6.1) to Eq. (6.5).

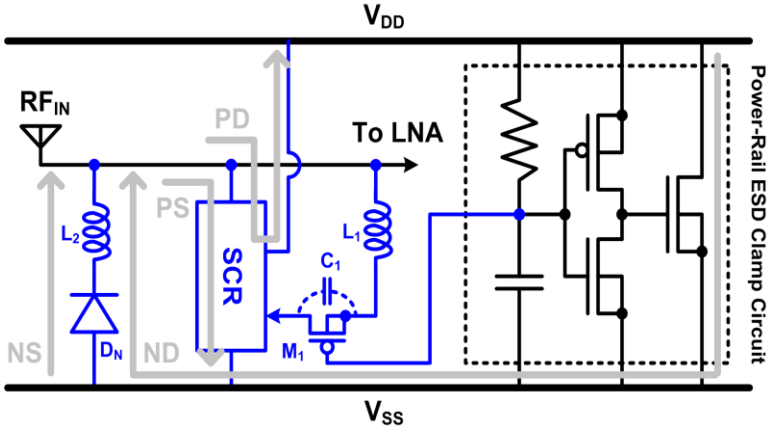


Fig. 6.3. The proposed dual-bad ESD protection scheme for RF_{IN} pad.

6.3. Simulation and Experimental Results of Dual-Band ESD Protection Circuit

6.3.1. Simulation Results of Dual-Band ESD Protection Circuit

The test circuits have been designed and fabricated in a 65nm CMOS process. The test patterns include the test circuits A, B, C, and D. The device dimensions of the test circuits are listed in Table 6.1. The size of SCR device used in the test circuits A, B, C, and D are split as 8μm, 15μm, 23μm, and 30μm, respectively. The size of D_N in test circuits A, B, C, and D are also split as also 8μm, 15μm, 23μm, and 30μm, respectively. The width / length of M_1 in each test circuit is kept at 90μm / 0.2μm. Therefore, the required L_1 (L_2) are 0.58nH (0.38nH), 0.58nH (0.27nH), 0.58nH (0.23nH), and 0.58nH (0.2nH) for the test circuits A, B, C, and D, respectively. Fig. 6.4 shows one chip photograph of test circuit D with cell size of $100\times180\mu m^2$.

The performances of the test circuits are simulated by using the microwave circuit simulator ADS with the selected device dimensions. Since the SCR model is not provided in the given CMOS process, diodes with P+/N-well, N+/P-well, and N-well/P-well junctions are used to simulate the SCR devices. A signal source with 50-Ω impedance drives the port 1 (RF_{IN} pad) of the test circuit, and a 50-Ω load is connected to the port 2 to simulate the LNA. The voltage supply of V_{DD} (V_{SS}) is 1V (0V), and the dc bias of RF_{IN} is 0.5V. The simulated reflection (S_{11}) parameters are shown in Fig. 6.5. These dual-band ESD protection circuits exhibit good input matching (S_{11}-parameters < -10dB) around 24GHz and 60GHz. The transmission (S_{21}) parameters around 24GHz and 60GHz are shown in Figs. 6.6(a) and 6.6(b). At 24GHz (60GHz) frequency, the test circuits A, B, C, and D have about 0.91dB (1.057dB),

1.002dB (1.138dB), 1.107dB (1.261dB), and 1.232dB (1.384dB) power loss, respectively. Although the parasitic capacitance of the ESD protection devices can be resonated out, the losses are still contributed by the parasitic resistance of the SCR and D_N. The performances of the test circuits are simulated by using the microwave circuit simulator ADS with the selected device dimensions. Since the SCR model is not provided in the given CMOS process, diodes with P+/N-well, N+/P-well, and N-well/P-well junctions are used to simulate the SCR devices. A signal source with 50-Ω impedance drives the port 1 (RF_{IN} pad) of the test circuit, and a 50-Ω load is connected to the port 2 to simulate the LNA. The voltage supply of V_{DD} (V_{SS}) is 1V (0V), and the dc bias of RF_{IN} is 0.5V. The simulated reflection (S_{11}) parameters are shown in Fig. 6.5. These dual-band ESD protection circuits exhibit good input matching (S_{11}-parameters < -10dB) around 24GHz and 60GHz. The transmission (S_{21}) parameters around 24GHz and 60GHz are shown in Figs. 6.6(a) and 6.6(b). At 24GHz (60GHz) frequency, the test circuits A, B, C, and D have about 0.91dB (1.057dB), 1.002dB (1.138dB), 1.107dB (1.261dB), and 1.232dB (1.384dB) power loss, respectively. Although the parasitic capacitance of the ESD protection devices can be resonated out, the losses are still contributed by the parasitic resistance of the SCR and D_N.

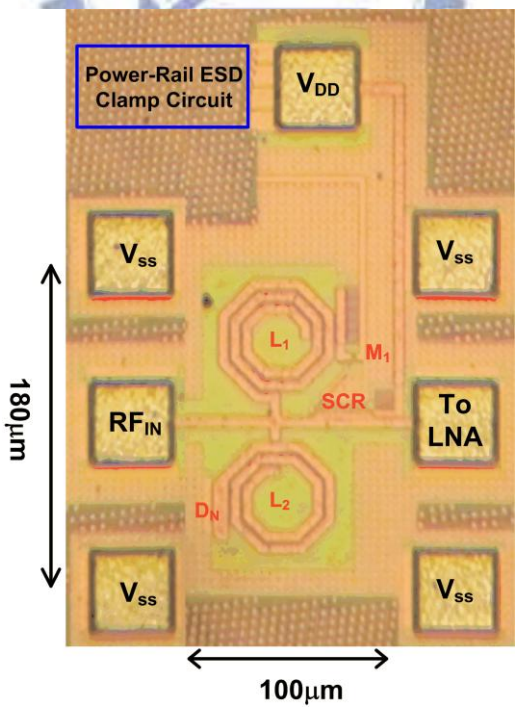


Fig. 6.4. Chip micrograph of test circuit D.

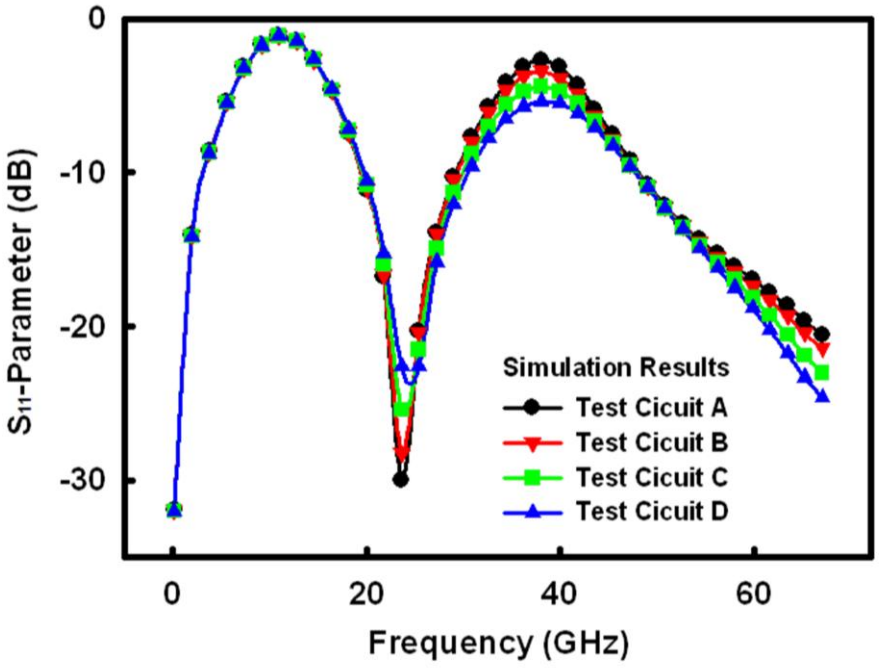
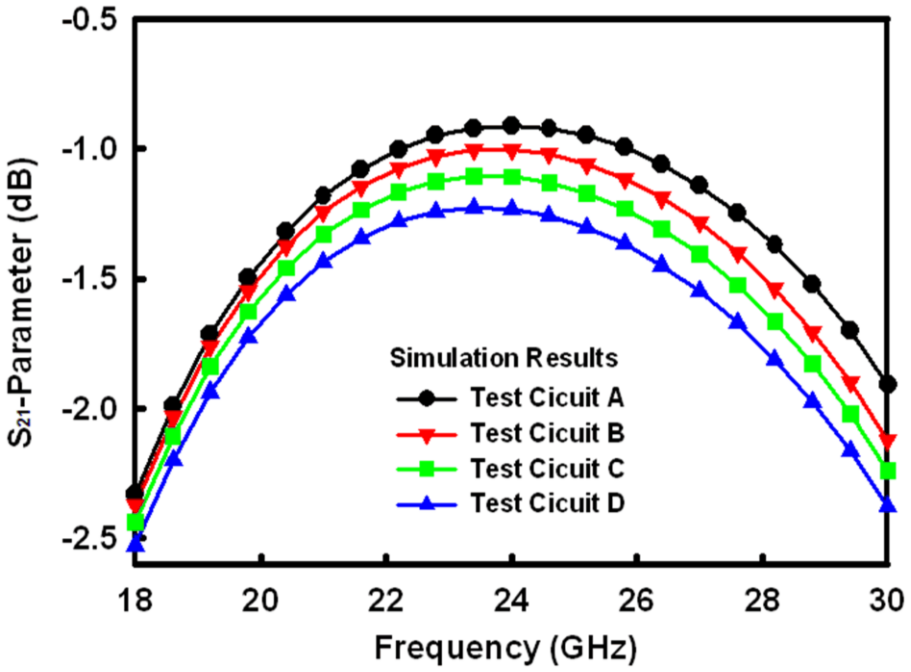
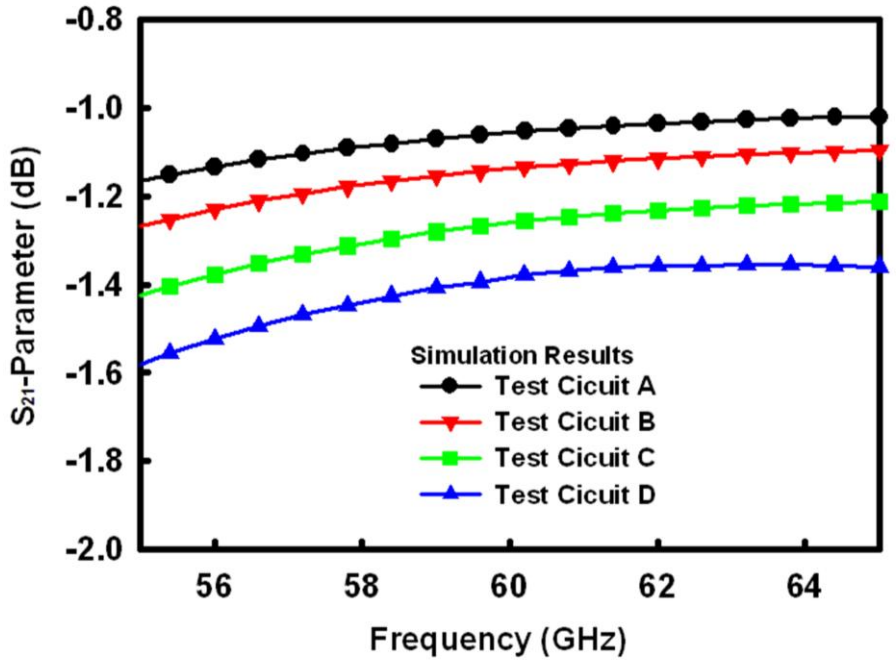


Fig. 6.5. Simulation results of the proposed dual-band ESD protection scheme on S_{11}-parameter.



(a)



(b)

Fig. 6.6. Simulation results of the proposed dual-band ESD protection scheme on S_{21}-parameter around (a) 24GHz and (b) 60GHz.

6.3.2. RF Performance of Dual-Band ESD Protection Circuit

With the on-wafer RF measurement, the S-parameters of these fabricated test circuits have been extracted from 0GHz to 67GHz. The voltage supply of V_{DD} (V_{SS}) is 1V (0V), and the dc bias of RF_{IN} is 0.5V ($V_{DD}/2$). The source and load resistances to the test circuits are kept at 50-Ω. In order to extract the intrinsic characteristics of the test circuits in high frequencies, the parasitic effects of the G-S-G pads have been removed by using de-embedding technique. The measured S_{11}-parameters and S_{21}-parameters versus frequencies among the four test circuits are shown in Figs. 6.7 and 6.8, respectively. As shown in Fig. 6.7, these ESD protection circuits exhibit good input matching (S_{11}-parameters < -15dB) around 24GHz or 60GHz. At 24GHz (60GHz), the test circuits A, B, C, and D have about 1.29dB (1.22dB), 1.26dB (1.28dB), 1.28dB (1.42dB), and 1.35dB (1.57dB) power loss, respectively.

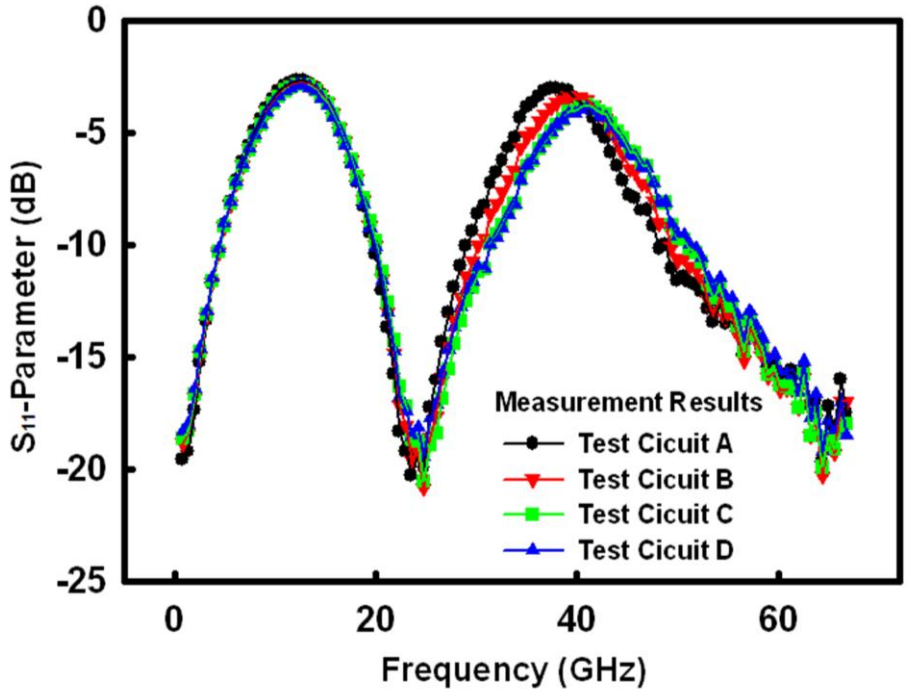


Fig. 6.7. Measurement results of S_{11}-parameters among the four test circuits with the proposed ESD protection scheme under different device dimensions.

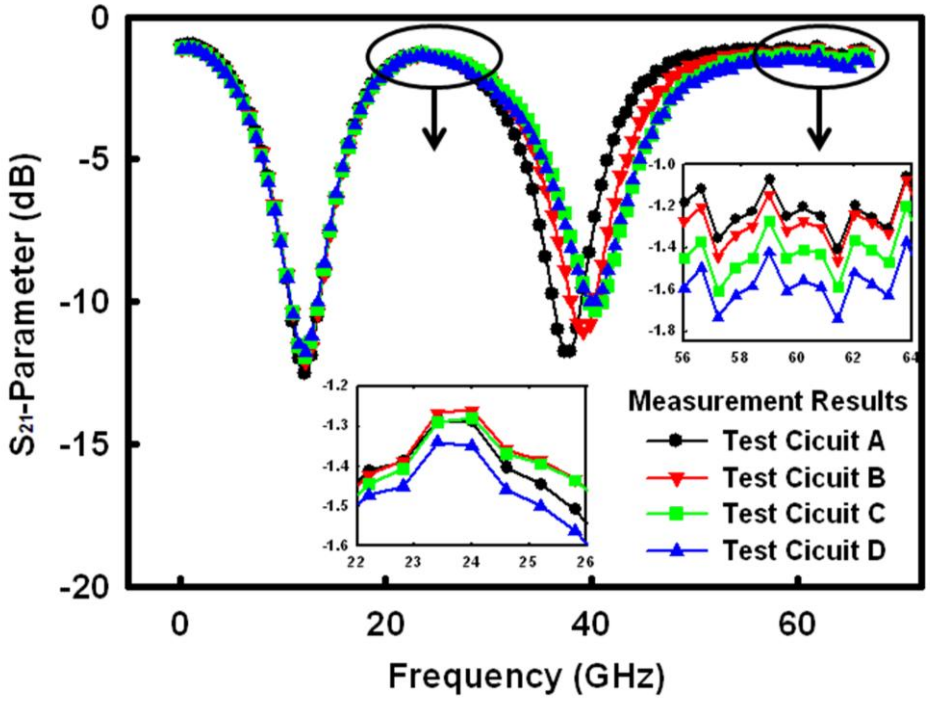


Fig. 6.8. Measurement results of S_{21}-parameters among the four test circuits with the proposed ESD protection scheme under different device dimensions.

Table 6.1

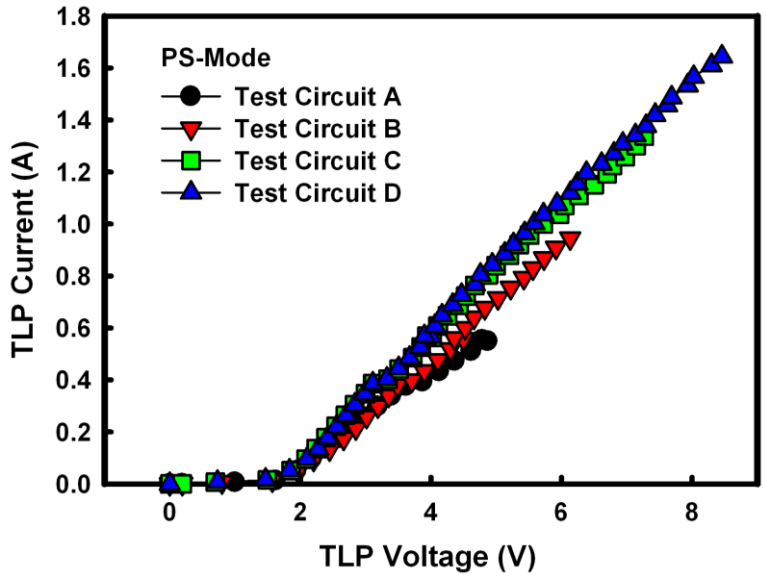
Device Dimensions and Measurement Results of Dual-band ESD Protection Cells

	Test Circuits			
	A	B	C	D
SCR (μm)	8	15	23	30
D_N (μm)	8	15	23	30
L_1 (nH)	0.58	0.58	0.58	0.58
L_2 (nH)	0.35	0.3	0.25	0.21
M_1 (μm / μm)	90/0.2	90/0.2	90/0.2	90/0.2
Area (μm x μm)	100x200	100x190	100x185	100x180
S_{11} at 24 GHz (dB)	-19.0	-19.7	-19.6	-18.5
S_{11} at 60 GHz (dB)	-15.6	-16.3	-16.1	-15.5
S_{21} at 24 GHz (dB)	-1.29	-1.26	-1.28	-1.35
S_{21} at 60 GHz (dB)	-1.22	-1.28	-1.42	-1.57
PS HBM (kV)	0.50	1.25	1.50	2.25
PD HBM (kV)	0.75	1.50	2.25	2.50
NS HBM (kV)	0.75	1.75	2.25	2.25
ND HBM (kV)	0.75	1.25	1.75	2.25

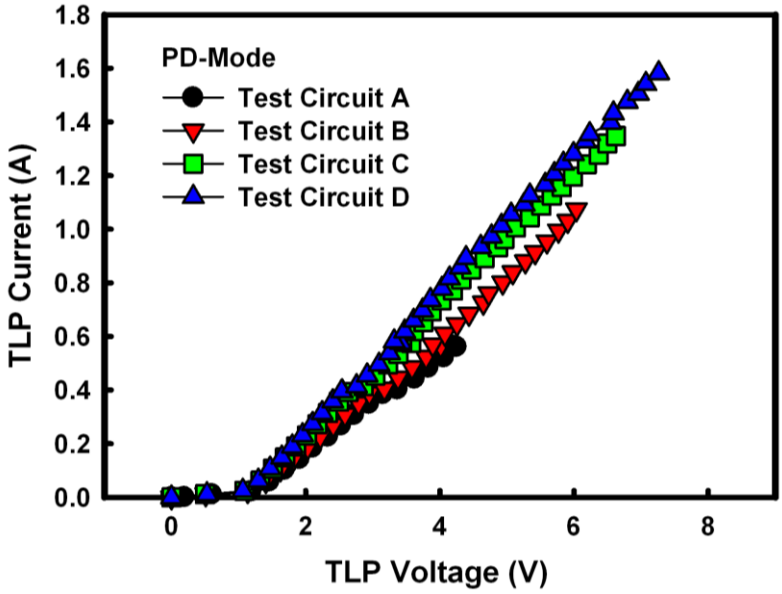
6.3.3. RF Performance of Dual-Band ESD Protection Circuit

The human-body-model (HBM) ESD pulses are stressed to each test circuit under PS, PD, NS, and ND ESD stress conditions. The failure criterion is defined as the I-V

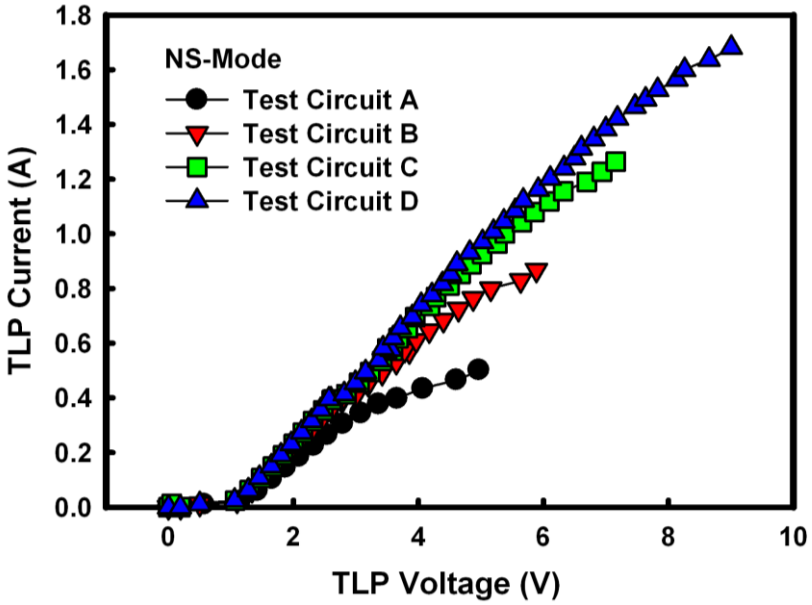
characteristics seen at RF_{IN} shifting over 30% from its original curve after ESD stressed at every ESD test level. The HBM ESD robustness among the four test circuits with the proposed ESD protection designs are listed in Table 6.1. The HBM ESD levels of the proposed ESD protection circuits A, B, C, and D can achieve 0.5-kV, 1.25-kV, 1.5-kV, and 2.25-kV, respectively, which are obtained from the lowest levels among PS, PD, NS, and ND ESD tests. The HBM ESD robustness of the test circuits is almost proportional to the sizes of ESD protection devices.



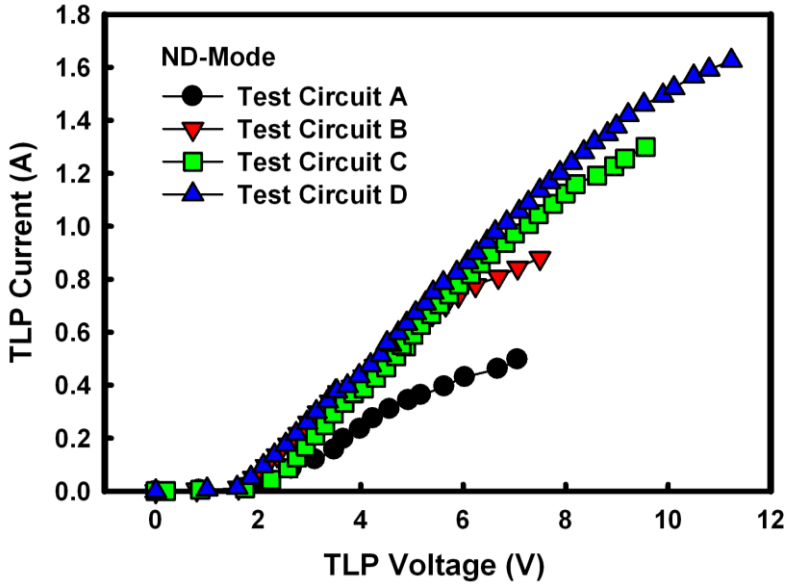
(a)



(b)



(c)



(d)

Fig. 6.9. TLP-measured I-V characteristics among four test circuits with the proposed dual-band ESD protection scheme under (a) PS mode, (b) PD mode, NS mode, and (d) ND mode tests.

The I-V characteristics of the ESD protection cells in high-current regions were characterized by using the transmission line pulsing (TLP) system with 10-ns rise time and 100-ns pulse width [81]. Fig. 6.9 shows the TLP-measured I-V curves of the fabricated ESD protection cells under PS mode, PD mode, NS mode, and ND mode tests, respectively. The secondary breakdown currents (It_2) indicated the current-handling ability of ESD protection cells were obtained from the TLP-measured I-V curves. The secondary breakdown currents

of ESD protection cells are listed in Table 6.2.

Table 6.2

TLP-Measured and VF-TLP-Measured I-V Characteristics among Four Test Circuits

TLP-Measured It_2 (A)	Test Circuits			
	A	B	C	D
PS Mode	0.55	0.94	1.34	1.64
PD Mode	0.57	1.07	1.35	1.58
NS Mode	0.50	0.86	1.30	1.68
ND Mode	0.57	0.88	1.30	1.63
VF-TLP-Measured It_2 (A)	**Test Circuits**			
	A	**B**	**C**	**D**
PS Mode	1.30	1.85	2.3	2.88
PD Mode	1.76	2.24	2.79	3.39
NS Mode	1.78	2.66	3.00	3.50
ND Mode	1.10	1.58	2.06	2.55

To further investigate the effectiveness of the proposed dual-band ESD protection circuit in faster ESD-transient events, another very fast TLP (VF-TLP) system is also used with 0.2-ns rise time and 1-ns pulse width. The VF-TLP system can be used to capture the transient behavior of ESD protection circuits in the time domain of charged-device-model (CDM) ESD event [82]. The VF-TLP-measured It_2 of the proposed circuits are also listed in Table 6.2. The tests circuits A, B, C, and D under PS mode ESD tests can achieve VF-TLP-measured It_2 of 1.3A, 1.85A, 2.3A, and 2.88A, respectively. These results determine that the proposed dual-band ESD protection circuits with inductor-triggered SCR are fast enough to be turned on among fast impulse response.

6.4. 24/60 GHz LNA with Proposed Dual-Band ESD Protection Circuit

One 24/60 GHz dual-band LNA (DBLNA) has been designed and fabricated in a 65nm CMOS technology for verification. The polysilicon resistors and metal-insulator-metal

capacitors are available in this process. Fig. 6.10 shows the circuit schematic of the 24/60 GHz LNA with the proposed dual-band ESD protection circuit. In order to implement 24/60 GHz LNA without applying MOS switches, two LNAs (24GHz and 60GHz) are designed in parallel using single RF_{IN} and RF_{OUT} [92]. Each LNA consists of two-stages and the cascode configuration is applied to achieve high gain performance. Besides, the common-source and common-gate NMOS transistors are all with 56-μm gate width and 0.06-μm gate length. The ESD protection circuits A and D are applied to the 24/60 GHz LNA circuit. The layout size of one circuit is $800\times750\mu m^2$, including all testing pads and dummy layers. The dummy layers are kept away from the signal paths, so they will not influence the RF signals. In order to verify the RF characteristics and ESD robustness, the stand-alone LNA without ESD protection is also fabricated for comparison. All the LNA circuits with and without ESD protection circuits are fabricated on the same wafer for comparison. Fig. 6.11 shows a chip photograph of the 24/60 GHz LNA with the ESD protection circuit D.

The RF characteristics are measured on wafer through G-S-G microwave probes with 100-μm pitch. The short-open-load-thru calibration has been done before the measurements. The gate bias of the designed 24/60 GHz LNA is 0.73V through bias tee at RF_{IN} and total dc power consumption is 88mW under 1-V V_{DD} power supply. The measured S_{11} and S_{21} parameters of the dual-band LNA circuits are shown in Figs. 6.12 and 6.13, respectively. Although the operating frequencies of LNA are shifted to lower frequencies, the ESD protection cells still can provide suitable ESD protection with only slight degradation on RF performances.

To compare the ESD robustness of the DBLNA with and without ESD protection circuits, the results of the HBM ESD stresses are shown in Table 6.3. The DBLNA without ESD protection only sustains a very low ESD protection level (<100V), which is far below the ESD specifications for commercial ICs. The ESD robustness of the DBLNA is substantially improved after inserting the proposed dual-band ESD protection circuit. The enhancement of ESD robustness is significant in that DBLNA with ESD A and ESD D (employing the ESD test circuits A and D) achieve the HBM ESD level of 0.8-kV and 2.75-kV, respectively.

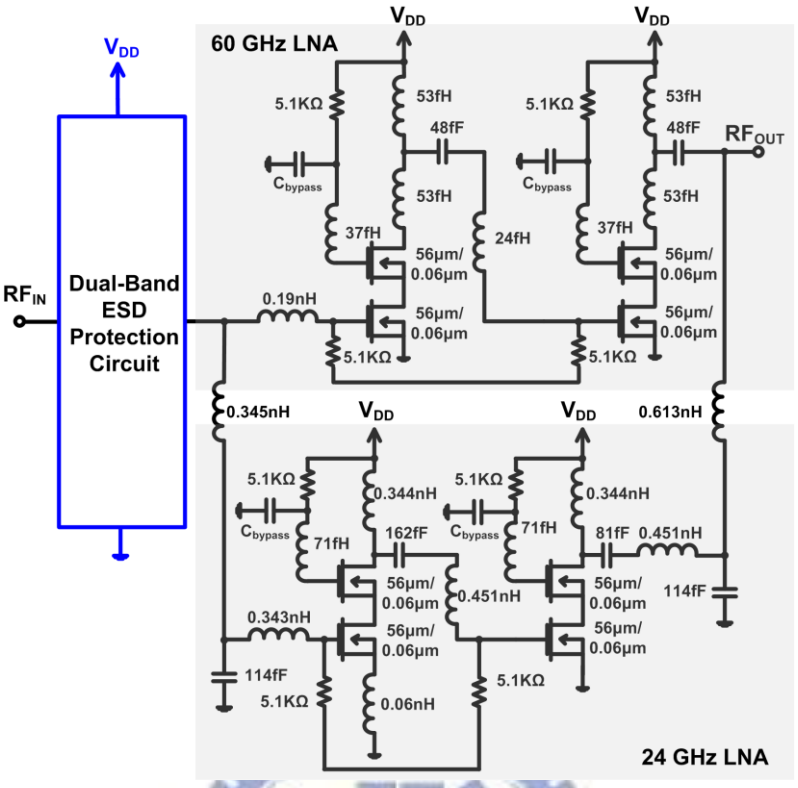


Fig. 6.10. Circuit schematic of 24/60 GHz LNA with dual-band ESD protection circuit.

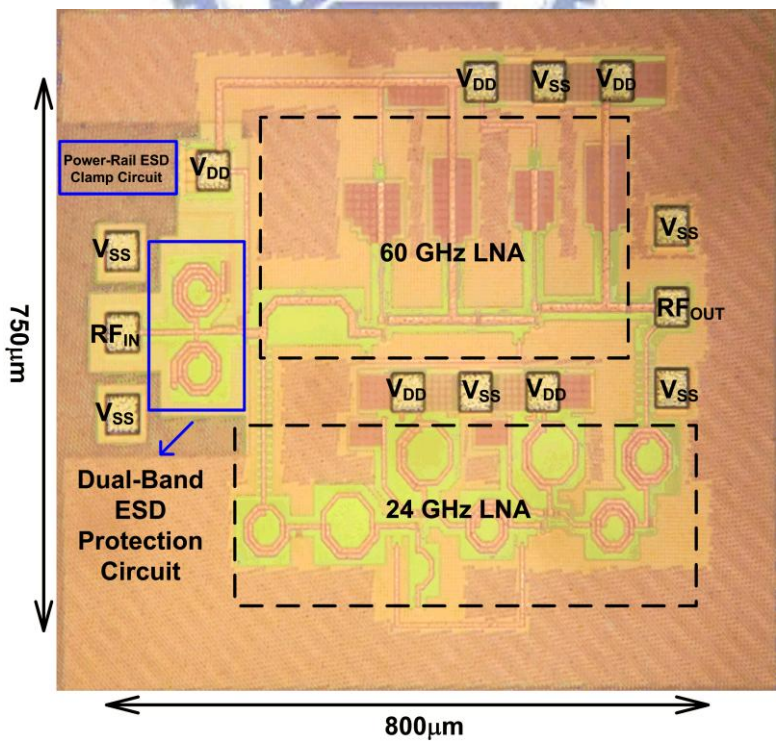


Fig. 6.11. Chip photograph of 24/60 GHz LNA with dual-band ESD protection circuit D.

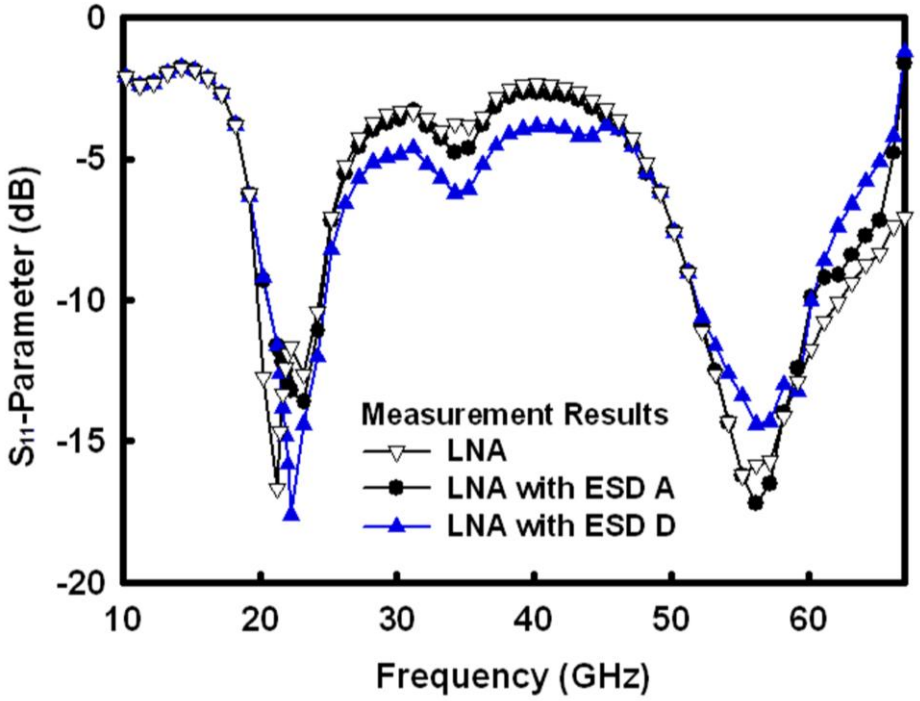


Fig. 6.12. Measurement results of S_{11}-parameters on dual-band LNA with and without ESD protection circuits.

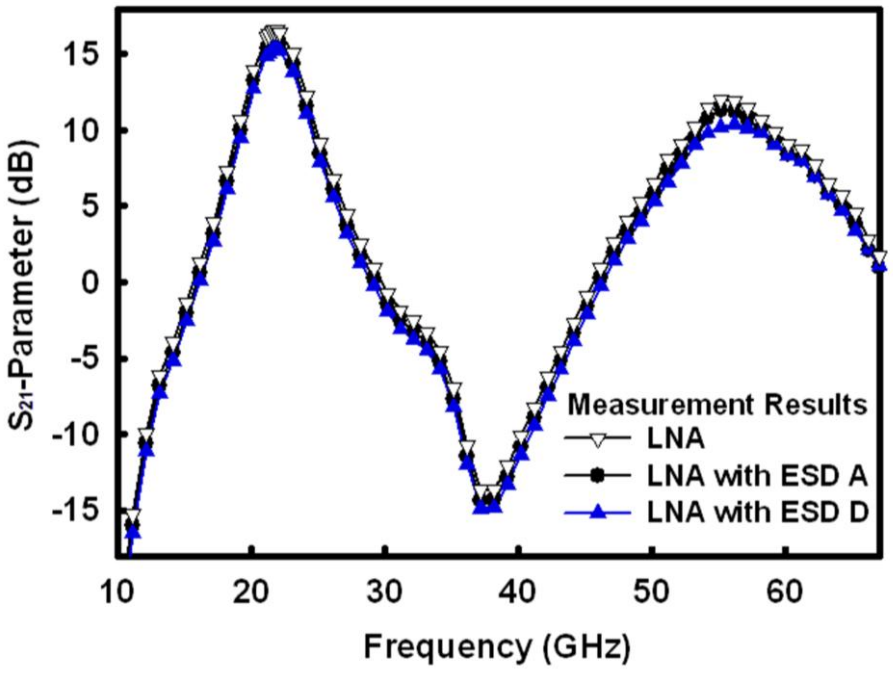


Fig. 6.13. Measurement results of S_{21}-parameters on dual-band LNA with and without ESD protection circuits.

Table 6.3

Test Results of HBM ESD Robustness among DBLNA

HBM ESD Robustness (kV)	Mode			
	PS	PD	NS	ND
DBLNA	< 0.1	< 0.1	< 0.1	< 0.1
DBLNA with ESD A	1	1	0.9	0.8
DBLNA with ESD D	3	3	3	2.75

For failure analysis, Fig. 6.14 shows the chip photograph of ESD zapped DBLNA with the ESD protection circuit D after de-layer procedure. Since the failure location of each zapping mode is concentrated, the red circles are denoted as D_N, SCR, NMOS of 24GHz LNA (NMOS-24GHz), and NMOS of 60GHz LNA (NMOS-60GHz) for scanning electron microscope (SEM) observing. Fig. 6.15 shows the SEM picture of the DBLNA without ESD protection. It has confirmed that the ESD damage, indicated by blue dashed square, is located on the poly-gate with dark and un-continuous marks after the PS-mode HBM ESD stress. Besides, the damage locations of Fig. 6.15(a) are more than those of Fig. 6.15(b), because the ESD current will direct damage the gate oxide which is closer to the RF_{IN} pad.

For the ESD protected DBLNA, Fig. 6.16 shows the failure sites of DBLNA with the proposed dual-band ESD protection circuit D under PS mode, PD mode, and NS mode ESD tests. In PS mode, the input pad is zapped by a positive ESD stress and the V_{SS} pad is grounded. The dominant ESD current will flow through SCR path, as shown in Fig. 6.3, to discharge and the damage site is observed at SCR path and shown in Fig. 6.16(a) with blue dashed square. In PD mode, the input pad is zapped by a positive ESD stress and the V_{DD} pad is grounded. The ESD current will be gathered in the diode path, as shown in Fig. 6.3, and the damage site is inspected at diode and shown in Fig. 6.16(b) with blue dashed square. In NS and ND modes, the input pad is zapped by a negative ESD stress, and the V_{SS} and V_{DD} pad are grounded, respectively. Since the ESD current will be discharged by the forward-biased D_N in NS and ND mode, the damage site is found at D_N and shown in Fig. 6.16(c) with blue dashed square.

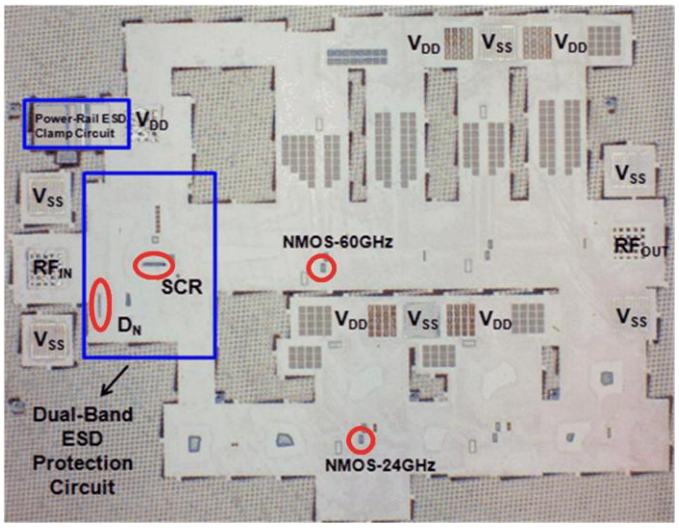
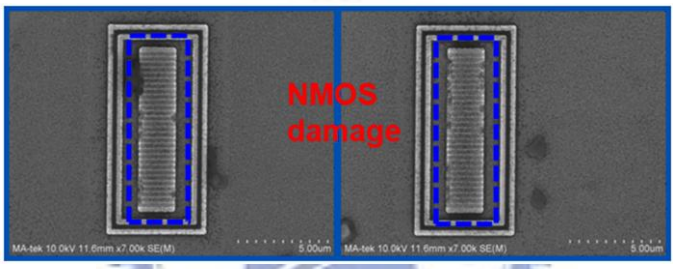
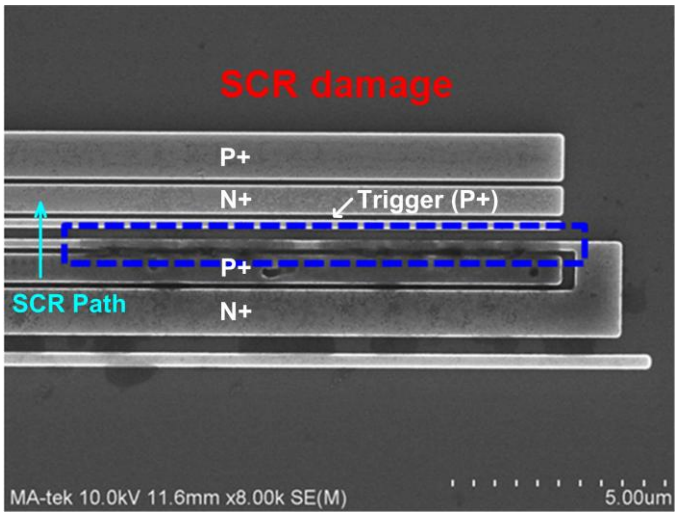


Fig. 6.14. The chip photograph of ESD zapped DBLNA with the ESD protection circuit D after de-layer procedure.

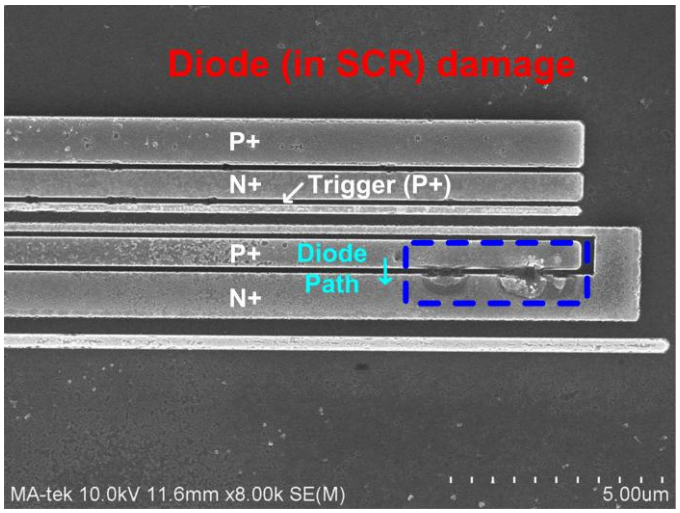


(a) (b)

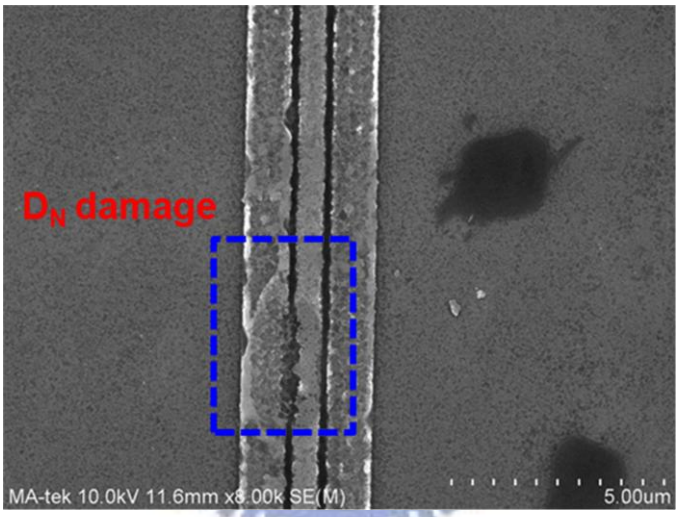
Fig. 6.15. SEM picture of NMOS in (a) 60GHz LNA and (b) 24GHz LNA, of the DBLNA without ESD protection.



(a)



(b)



(c)

Fig. 6.16. The failure sites of DBLNA with the proposed dual-band ESD D under (a) PS mode, (b) PD mode, and (c) NS mode ESD tests.

6.5. Summary

The novel ESD protection cell for 24/60 GHz dual-band applications has been designed, fabricated, and characterized in a 65nm CMOS process. The test circuits A, B, C, and D have about 1.29dB (1.22dB), 1.26dB (1.28dB), 1.28dB (1.42dB), and 1.35dB (1.57dB) power loss at 24GHz (60GHz), respectively. Besides, they can sustain 0.5-kV, 1.5-kV, 2.25-kV, and 2.75-kV HBM ESD tests, respectively. The VF-TLP-measured It_2 of these test circuits are also provided, which are 1.3A, 1.85A, 2.3A, and 2.88A, respectively. The proposed dual-band ESD protection design can be used to achieve good RF performance and ESD robustness simultaneously. The test circuits with the proposed dual-band ESD have been

successfully applied to the 24/60 GHz LNA to verify the circuit performance and confirm the ESD protection ability. Besides, the ESD protection cell can be further designed for other MMW circuits, such as 24/77 GHz applications.

Chapter 7

Conclusions and Future Works

This chapter summarizes the main results and contributions of this dissertation. Suggestions for future research topics in the fields of on-panel circuits design for display panel applications are also provided in this chapter.

7.1. Main Results of This Dissertation

In this dissertation, s several novel designs have been proposed in the aforementioned research topics. Measured results of the integrated panels and fabricated test chips have demonstrated the performance improvement. The achievements of this dissertation have been published or submitted to several international journal and conference papers. Several innovative designs have been applied for patents. The research topics of this dissertation including: (1) integrated gate driver with threshold voltage drop cancellation in amorphous silicon (a-Si) technology, (2) low power gate driver in a-Si technology for narrow bezel panel application, (3) analog pixel memory in low temperature poly silicon (LTPS) technology for low power display, (4) ESD protection design for 60GHz low noise amplifier (LNA) with inductor-triggered silicon-controlled rectifier (SCR) in 65nm CMOS process, and (5) dual-band ESD protection for 24/60 GHz millimeter-wave circuits.

In chapter 2, an integrated gate driver with highly output charging speed has been successfully fabricated in amorphous silicon technology for a 3.8-inch WVGA panel. The output rise time of the proposed integrated gate driver is dramatically reduced about 24.6% by using the threshold voltage drop cancellation method. For panel reliability testing, the decay rate of transmittance brightness for the demonstrated 3.8-inch panel implemented with the new proposed integrated gate drivers represents less than 3.61%, and the contrast ratio shows almost no degradation after the operating of 500 hours under 70℃ and -20℃ conditions. The proposed gate driver is quite appropriate for integration into to the high resolution TFT-LCD panels. In chapter 3, a new gate driver using amorphous silicon TFT technology has been successfully designed and fabricated for TFT-LCD application. The

proposed gate driver utilizes four clock signals and only one output charge/discharge TFT to narrow the pixel size and achieve power reduction about 61%. Besides, the scan direction of the proposed gate driver can be adjusted by switching two control signals to accomplish the bidirectional function and it is as well as demonstrated on 4.5-inch WXGA panel successfully. Therefore, the proposed gate driver is quite appropriate for integration into to the high resolution and low power TFT-LCD panels.

In chapter 4, two proposed analog pixel memory cells for power saving application in TFT-LCDs have been successfully verified in a 3-μm LTPS process. The frame rate to refresh the static image can be reduced from 60Hz to 3.16Hz with the voltage decay at the output only less than 0.1V under the input data varies from 1V to 4V. Experimental results have successfully verified that both of the proposed analog memory cells are suitable for the MIP application of high resolution. Besides, the compensation technique is used to improve the output voltage decay due to the threshold voltage drop.

In chapter 5, the new ESD protection scheme with inductor-triggered SCR has been designed, fabricated, and characterized in a 65nm CMOS process. The inductor-triggered SCR is designed to achieve low trigger voltage and high turn-on speed. These ESD protection circuits are developed to support RF circuit designers for them to easily apply ESD protection in the 60GHz RF receiver circuits. Verified in a commercial 65nm CMOS process, the test circuits A, B, C, and D have about 1.2dB, 1.4dB, 1.6dB, and 1.8dB power loss at 60GHz frequency, respectively. Besides, they can sustain 0.75-kV, 1.5-kV, 2.25-kV, and 2.75-kV HBM ESD tests, respectively. The VF-TLP-measured It_2 of these test circuits are also provided, which are 0.96A, 1.72A, 2.14A, and 2.21A, respectively. The test circuits with inductor-triggered SCR have been applied to the 60GHz LNA to confirm the ESD protection ability and to verify the RF performances. The RF performances of the LNA with ESD protection circuit A and that with ESD protection circuit D are still maintained after 500-V and 3-kV HBM ESD tests are performed, respectively. In chapter 6, the novel ESD protection cell for 24/60 GHz dual-band applications has been designed, fabricated, and characterized in a 65nm CMOS process. The test circuits A, B, C, and D have about 1.29dB (1.22dB), 1.26dB (1.28dB), 1.28dB (1.42dB), and 1.35dB (1.57dB) power loss at 24GHz (60GHz), respectively. Besides, they can sustain 0.5-kV, 1.5-kV, 2.25-kV, and 2.75-kV HBM ESD tests, respectively. The VF-TLP-measured It_2 of these test circuits are also provided, which are 1.3A, 1.85A, 2.3A, and 2.88A, respectively. The proposed dual-band ESD protection design can be used to achieve good RF performance and ESD robustness simultaneously. The test circuits with the

proposed dual-band ESD have been successfully applied to the 24/60 GHz LNA to verify the circuit performance and confirm the ESD protection ability. Besides, the ESD protection cell can be further designed for other MMW circuits, such as 24/77 GHz applications.

7.2. Future Works

For the narrow bezel demands of display devices, gate driver circuit using thin-film-transistor (TFT) has become a main stream for the liquid crystal display (LCD) due to the mature manufacturing, low-cost processing, and reducing of complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs). Nevertheless, the turn off bias of main driving TFT of proposed gate driver circuits is set at zero voltage (V_{GS}=0V) so that the size of TFT for controlling leakage current is rather large. Large size of TFT would increase the power consumption of gate driver circuit, and it is well known that the leakage current of a-Si:H TFT is decreased with decreasing V_{GS} so that the turn off bias of pixel switch is less than 0V (about -5V) to reduce leakage current in the pixel. Future work could focus on the gate driver circuit by employing the negative turn-off biasing, which can reduce the power consumption. Furthermore, the noise reduction circuit of gate driver occupies large layout area due to the capacitor's value (about 1.5~2pF) for each gate line. To further decrease that, the design of sharing noise reduction circuit by adjacent gate driver could be realized in the future for narrow bezel display applications.

The design of memory-in-pixel (MIP) using TFT is as proposed to meet the low power consumption of mobile displays, which provided a low power standby mode for continuous display of static images. However, the size of proposed analog pixel memory is overdesigned in chapter 4, so it should be scaled down for practical application. By scaling down the size, the power of the pixel memory circuit can be reduced. Besides, the proposed analog memory was applied to single pixel and its layout area was large to decrease the aperture ratio of the display panel. Therefore, future designs can aim at sharing multi-pixels with one analog pixel memory to save layout restriction for high resolution displays application.

The designs for RF circuits applied to higher frequency band is a popular topic in advanced CMOS technology. The V band occupied from 40 to 75 GHz frequency band. The V band is primarily used for high capacity and short distance communication systems. To achieve successful ESD protection design for such high-frequency RF circuits, precise modeling of ESD protection devices is necessary. Hence, modeling of ESD protections in such high frequency bands is needed. Besides, in an fully integrate SoC chip with RF

frond-end and baseband circuits, the larger die size for SoC applications and the thinner gate oxide in nanoscale CMOS transistors will become the design concerns. With the larger die size and the thinner gate oxide, nanoscale CMOS ICs are very sensitive to charged-device model (CDM) ESD events. Therefore, the efficient CDM ESD protections should be designed in nanoscale CMOS process. T-coil ESD protection circuits are often used to compensate the parasitic capacitance of ESD protection devices and input circuit for high speed data transmission. Developing distributed T-coil ESD protection circuit for high speed digital circuit will be promising in the near future. (40 Gb/s)

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Publication List

(A) Referred Journal Papers:

[1] P.-T. Liu, and **Li-Wei Chu**, "Innovative voltage driving pixel circuit using organic thin-film transistor for AMOLEDs," *IEEE J. Display Technol.*, vol. 5, no. 6, pp. 224-228, June 2009.

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