國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

奈米互補式金氧半製程下應用於射頻積體電路之靜電放電防護設計

ESD Protection Design for Radio-Frequency Integrated Circuits in Nanoscale CMOS Technology

研 究 生：范美蓮　　(Mei-Lian Fan)

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中華民國一〇三年二月

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碩士論文

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摘要

在現今的積體電路產業中，基於晶片整合度與成本的考量，射頻積體電路 (radio-frequency integrated circuits, RF ICs) 也逐漸傾向於實現在 CMOS 製程中。靜電放電 (electrostatic discharge, ESD) 是積體電路可靠度中最重要的一環，大多數電子產品的故障與損壞均與遭受靜電放電轟擊有關。由於射頻積體電路對於任何額外的寄生效應都相當敏感，因此能應用在射頻積體電路之靜電放電防護設計除了要有好的靜電放電耐受度之外，還必須要能將其寄生效應的影響降至最低。

在本篇論文首先提出了由傳統靜電放電防護設計修改並且無額外增加元件的新靜電放電防護元件設計。此新的設計採用堆疊的二極體 (diode) 並將矽控整流器 (silicon-controlled rectifier, SCR) 內嵌於其中並做為主要靜電放電之路徑。經由佈局優化

能使得新的架構有更低的寄生電阻、低的寄生電容以及高的靜電放電防護能力，更適合做為晶片上的靜電放電防護設計。

本論文進一步將上述的靜電放電防護元件設計成可應用於差動式 (differential) 低雜訊放大器 (low-noise amplifier, LNA) 的靜電放電防護電路。由於在此靜電放電防護電路中，內嵌的矽控整流器是建立於一差動輸入端到另一差動輸入端之間，所以在兩輸入端之間 (pin-to-pin) 的靜電防護能力能夠提升。

此外，本論文進一步將靜電放電防護電路應用在 24 GHz 之低雜訊放大器電路以作驗證。根據量測結果，證明所提出的設計可以有效的提供差動低雜訊放大器電路出色的靜電放電防護能力以及良好的射頻電路性能。

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Abstract

For the consideration of high integration and low cost, radio-frequency integrated circuits (RF ICs) have been fabricated in nanoscale CMOS processes. Electrostatic discharge (ESD), which has become one of the most important reliability issues in IC products, must be taken into consideration during the design phase of all IC products. Since RF ICs are very sensitive to any extra parasitic effect, ESD protection design for RF ICs in nanoscale CMOS processes needs well ESD protection ability and small parasitic effect.

In this thesis, the new ESD protection design which was modified from the conventional ESD protection design without adding any extra device has proposed. The new proposed ESD protection device utilizes stacked diodes with embedded silicon-controlled rectifier (SCR) as main ESD-current-discharging paths. The optimization on layout style of the stacked diodes is more suitable for on-chip ESD protection due to its low turn-on resistance, low parasitic

capacitance, and high ESD robustness.

The proposed ESD protection stacked diodes with embedded SCR has been also developed for the differential low-noise amplifier (LNA). The SCR path was established directly from one differential input pad to the other differential input pad, so the pin-to-pin ESD robustness can be improved.

Besides, this design had been further applied to a 24-GHz LNA in the same CMOS process. Experimental results had shown that the proposed ESD protection design for the differential LNA can achieve excellent ESD robustness and good RF performances.

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首先我要感謝我的指導教授柯明道老師和林群祐老師，柯明道老師的細心指導與耐心鼓勵，無論多忙碌，都孜孜不倦的關心學生的研究狀況，老師在ESD方面深厚的專業知識以及殷切的指導讓我學到了許多東西，而在專業領域之外，老師認真的研究態度、對於論文格式的要求也讓我獲益良多。

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范美蓮

103年2月於竹塹交大

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Chapter 1
Introduction

1.1 Motivation

In recent decades, the requirements of wireless products such as smart phones are overwhelming. Nanoscale CMOS technologies have been used to implement the RF circuits with the advantages of scaling-down feature size, low power consumption, high integration capability, improving high-frequency characteristics, and low cost for mass production [1].

From consumer electronics to mission-critical applications operating under harsh conditions, reliability becomes a key feature for most RF electronics. The electrostatic discharge (ESD) of CMOS ICs becomes the biggest reliability concern. ESD-induced failure results in unbearable energy bursts, either huge transient current or large voltage surge, which can easily damage any integrated RF devices, circuits, and systems [2]. As the IC technology keep scales down, ESD issues become more serious and must be carefully considered. Well-designed ESD protection circuits for all I/O pads in ICs are necessary.

In the RF frontend circuits, the input/output (I/O) pads are usually connected to the gate terminal or silicided drain/source terminal of the metal-oxide-semiconductor field-effect transistor (MOSFET). For an RF IC, the input interface is typically a low-noise amplifier (LNA), and the output interface is typically a power amplifier (PA). Once the RF frontend circuit is damaged by ESD, it cannot be recovered and the RF functionality would be lost. Thus, on-chip ESD protection design must be provided for all I/O pads in RF ICs, such as LNA and PA. Conventional ESD protection design, which consists of a pair of diodes inserted

beside I/O pads and a power-rail ESD clamp circuit can provide whole-chip ESD protection [3]. Unfortunately, such design would cause RF performance degradation of core circuits due to the undesired parasitic effects introduced by those ESD protection devices [4].

While being applied in RF ICs, conventional ESD protection devices with large dimension have good ESD robustness, but their large parasitic capacitances cause signal loss from pads to ground. In particular, the parasitic capacitances also inevitably corrupt the critical input and output matching conditions, which will lead to serious RF IC circuit performance degradation, including almost all circuit specifications. For these reasons, designing effective ESD protection circuits without degrading the RF performance of core circuits has become a great challenge.

Since the parasitic capacitance of ESD protection devices is one of the most important design considerations for RF ICs. Some methods have been developed to mitigate the negative impact caused by the parasitic capacitances. The parasitic capacitances of ESD protection devices can be cancelled out by using inductors and capacitors [5]-[7]. Some ESD protection designs have been developed to fundamentally reduce the parasitic capacitances of the ESD protection devices [4]. Several RF designs considering ESD parasitic effects were reported, which included the ESD-induced parasitic resistance and capacitance into impedance matching designs [8].

Unfortunately, the rapidly increasing operating frequency of RF ICs makes the parasitic capacitances of ESD protection devices be more strictly limited. It is getting harder and harder to meet the desired ESD robustness with such limitation. Consequently, ESD protection designs for extremely high frequency must be necessary. For RF ESD protection designs, silicon-controlled rectifier (SCR) is a useful device. An SCR with proper triggering mechanism has great ESD robustness and low parasitic capacitances within a small layout area. Therefore, carefully designed SCR is expected to be suitable for RF ESD protection [9].

The new ESD protection device and circuit for RF circuit with higher ESD protection level and compact layout area are proposed in this work. Such ESD protection device and circuit have been designed and fabricated in a 65-nm CMOS process. The new proposed ESD protection design utilizes stacked diodes embedded silicon-controlled rectifier (SDSCR) as main ESD-current-discharging paths. The measurement results prove that ESD protection designs provides low turn-on resistance, low parasitic effects, and high ESD robustness.

The proposed ESD protection circuit also has been further applied to the CMOS differential LNA. The 24 GHz CMOS differential LNA which utilize SDSCR and a power-rail ESD clamp circuit as their ESD protection design are presented. The SDSCR and LNA have been designed and fabricated in a 65-nm CMOS process. The measurement results show that SDSCR indeed provides desired ESD robustness for the 24 GHz CMOS LNA.

Besides, for comprehensive investigation of LNA ESD protection methods, an ESD-protected LNA with ESD protection strategy consists of a power-rail ESD clamp circuit has also been designed and verified in a 65-nm CMOS process. According to the measurement results, the proposed ESD protection strategy also provides a good protection for the input gate terminal of the MOSFET of the RF LNA circuit.

1.2 Thesis Organization

Chapter 2 introduces the basic principles and the crucial considerations of RF ESD protection design as well as basics of RF LNA. The issues of RF ESD protection design are investigated.

Chapter 3 shows the design procedure of ESD protection devices for RF circuits. The novel ESD protection design with optimized layout style is proposed. The architecture and simulation results are presented. The measurement results of the RF performances and the

ESD levels of both ESD protection designs, which are fabricated in a 65-nm CMOS process, are summarized. According to the experimental results, the proposed ESD protection design exhibit required ESD levels without additional layout area.

Chapter 4 exhibits an ESD protection circuit design for RF circuit, which are fabricated in a 65-nm CMOS process,. The new proposed ESD protection circuit utilizes stacked diodes embedded silicon-controlled rectifier (SDSCR) as main ESD-current-discharging paths. In addition, comparing with the conventional dual diodes ESD protection circuit, the new proposed ESD protection circuit provides the shortest ESD current path under the pin-to-pin ESD stress. As the result, the new proposed ESD protection circuit is expected to have high pin-to-pin ESD robustness.

Chapter 5 exhibits an application of the proposed ESD protection design to 24-GHz differential LNA. The stacked diodes embedded silicon-controlled rectifier (SDSCR), which is appropriate for differential LNA ESD protection, is proposed. The architecture of the ESD protection design is presented in detail. In addition, a 24 GHz CMOS LNA used to verify the ESD level of the proposed SDSCR is also designed. Both unprotected LNA and ESD-protected LNA are fabricated in a 65-nm CMOS process. The experimental results of RF performances and ESD levels of the unprotected LNA and the ESD-protected LNA are summarized and compared. According to the results, the proposed SDSCR indeed has high ESD protection ability without increasing the layout area.

Chapter 6 is the conclusions of this thesis and the future works on this topic.

Chapter 2

Basics of RF Circuit and ESD Protection

2.1 General Considerations of LNA Design

2.1.1 S-Parameters

To deal with a high-frequency network, conventional method of measuring voltage and current is no longer suitable. Direct measurements under high-frequency conditions usually involve the magnitude and phase of a traveling wave, so the concepts of equivalent voltage, equivalent current, and the related impedance and admittance became abstract. Scattering parameters (S-parameters) with the concepts of reflected, incident, and transmitted waves are more suitable and widely used to describe the characteristics and behaviors of high-frequency networks [10].

Fig. 2.1 shows a two-port network characterized by S-parameters. The S-parameters are defined in

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.1}$$

which can also be represented as

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 \\ b_2 = S_{21}a_1 + S_{22}a_2 \end{cases} \tag{2.2}$$

where a_1 and a_2 represent the incident waves of each port; b_1 and b_2 represent the reflected waves of each port, respectively. Each term in the S-parameters matrix is defined in (2.3).

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{2.3}$$

S_{11} is the reflection coefficient seen at port 1 when port 2 is terminated with a load of 50 Ω; S_{22} is the reflection coefficient seen at port 2 when port 1 is terminated with a load of 50 Ω. S_{21} is the forward gain from port 1 to port 2; S_{12} is the reverse gain from port 2 to port 1.

In high-frequency measurement, S_{11} describes input matching condition, and S_{22} describes output matching condition. S_{21} describes the forward gain from port 1 to port 2, and S_{12} describes the reverse isolation condition.

Fig. 2.1. A two-port network described with S-parameters.

2.1.2 Noise Figure

For receivers, noise is another important concern. In many analog circuits, the signal-to-noise ratio (SNR), defined as the ratio of the signal power to the total noise power. Noise factor is a figure of merit to describe a noisy system [11]. In RF design, on the other hand, even though the ultimate goal is to maximize the SNR for the received and detected

signal, most of the front-end receiver blocks are characterized in terms of their noise figure than the input-referred noise. Noise factor is defined as

$$F = \frac{SNR_i}{SNR_o} \tag{2.4}$$

where SNR_i represents the signal-to-noise ratio measured at input, and SNR_o represents the signal-to-noise ratio measured at output. It is a measure of SNR degradation when signal passes through the described system. A commonly used figure of merit named noise figure (NF) is

$$NF = 10\log F(dB) \tag{2.5}$$

The physical meaning can be realized as

$$NF = \frac{Total\ output\ noise\ power}{Output\ noise\ power\ due\ to\ source\ only} \tag{2.6}$$

Form (2.6), if the described system adds no noise of its own, NF would be zero.

Noise Figure is measure of how much the SNR degrades as the signal passes through a system. If a system has no noise, then $SNR_o = SNR_i$, regardless of the gain. This is because both the input signal and the input noise are amplified (or attenuated) by the same factor and no additional noise is introduced. Form (2.6), if the described system adds no noise of its own, NF would be zero. In reality, the finite noise of a system degrades the SNR, yield $NF > 1$.

Considering a cascade multi-stage system shown in Fig. 2.2, each stage has gain (G) and noise factor (F). The noise factor can be characterized by Friis formula

$$F_{sys} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots \tag{2.7}$$

It is indicial that noise of a multi-stage system is mainly contributed by the first stage. For this reason, LNA, which is the first stage of an RF receiver, needs much consideration on noise.

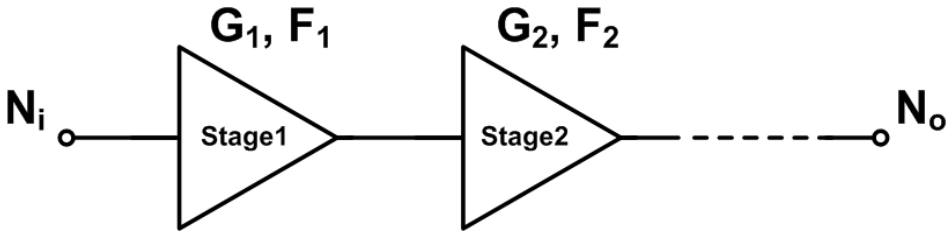


Fig. 2.2. A cascade multi-stage RF system described with gain and noise factor.

2.1.3 Stability

Stability, which can be extracted from S-parameters, is a crucial consideration in RFIC design. To an RF amplifier, it is important to operate stably without going into oscillation under any condition. For unconditionally stable, both input impedance and output impedance cannot be negative resistive. The sufficient and necessary conditions are

$$|\Gamma_S| < 1 \tag{2.8}$$

$$|\Gamma_L| < 1 \tag{2.9}$$

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{2.10}$$

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{11}\Gamma_L} \right| < 1 \tag{2.11}$$

where Γ_S is source reflection coefficient; Γ_L is load reflection coefficient; Γ_{IN} is input reflection coefficient; Γ_{OUT} is output reflection coefficient.

These equations can be further derived to

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.12}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.13}$$

(2.12) and (2.13) can be further derived to

$$b = 1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11}S_{22} - S_{12}S_{21}|^2 > 0 \tag{2.14}$$

(2.12) and (2.14) represents the necessary and sufficient conditions for unconditional stability.

2.1.4 Gain Compression

The small-signal gain of a circuit is usually obtained with the assumption that harmonics are negligible. However, as the signal amplitude increases, the gain begins to vary. In fact, nonlinearity can be viewed as variation of the small-signal gain with the input level. In most circuits of interest, the output is a compressive or saturating function of the input. Ideally, an RF amplifier is considered as a linear amplifier. The power gain remains constant and the relationship between output power and input power is linear. However, the large signal transfer characteristics are different. As input power increases larger and larger, the output power starts to gradually saturate. This makes the linear transfer relationship between input power and output power no longer hold. In RF circuits, this effect is quantified by the "1-dB compression point," defined as the input signal level that causes the small-signal gain to drop by 1 dB. If plotted on a log-log scale as a function of the input level, the output level falls below its ideal value by 1 dB at the 1-dB compression point. At 1-dB gain compression point (P_{1dB}), the power gain is 1 dB smaller than the constant power gain, as shown in Fig. 2.3. IP_{1dB} is the input power at P_{1dB}.

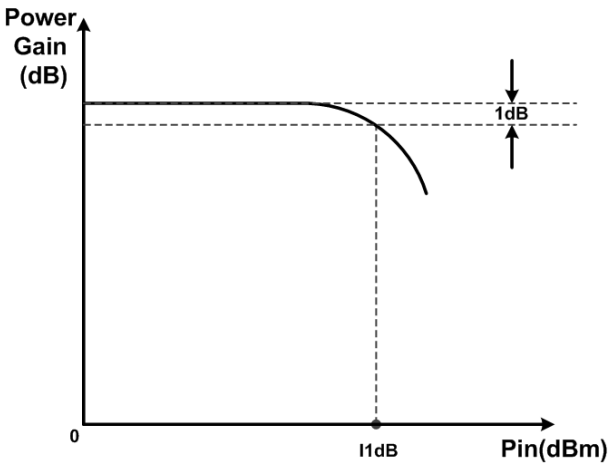


Fig. 2.3. The plots of power gain versus input power.

2.2 Conventional ESD Protection Design

2.2.1 Architecture of Conventional Whole-Chip ESD Protection Design

Fig. 2.4 shows a whole-chip ESD protection design which can provide effective ESD protection for CMOS ICs [3]. The typical design consists of a pair of ESD protection devices inserted beside the I/O pad and a power-rail ESD clamp circuit placed between the V_{DD} and V_{SS} power lines. The pair of ESD protection devices is used to clamp ESD stress and provide ESD discharge paths among I/O pad and power lines. The power-rail ESD clamp circuit is used to clamp the V_{DD}-to-V_{SS} ESD stress and provide an ESD discharge path between V_{DD} and V_{SS} power lines.

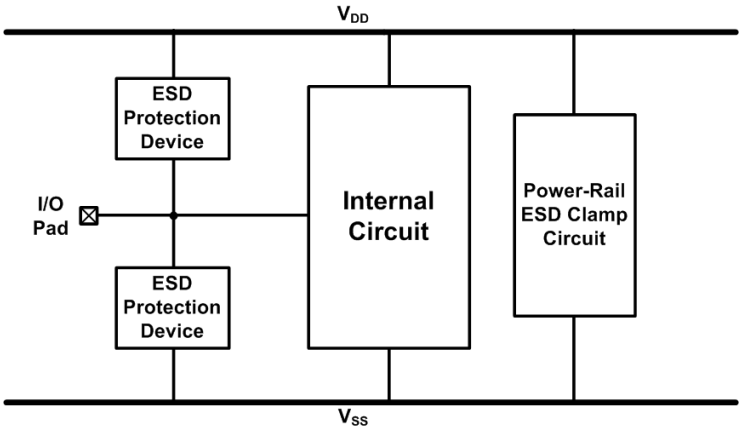


Fig. 2.4. Architecture of whole-chip ESD protection design.

2.2.2 Power-Rail ESD Clamp Circuit and I/O ESD Clamp Device

A typical power-rail ESD clamp circuit, which is shown in Fig. 2.5, consists of an ESD-transient detection circuit and an NMOS (M_{ESD}) used as a V_{DD}-to-V_{SS} ESD clamp device. The ESD-transient detection circuit is expected to detect ESD stress and then turn on the ESD clamp device to provide an ESD discharge path right after ESD events occur, while turn off the ESD clamp device under normal power-on conditions.

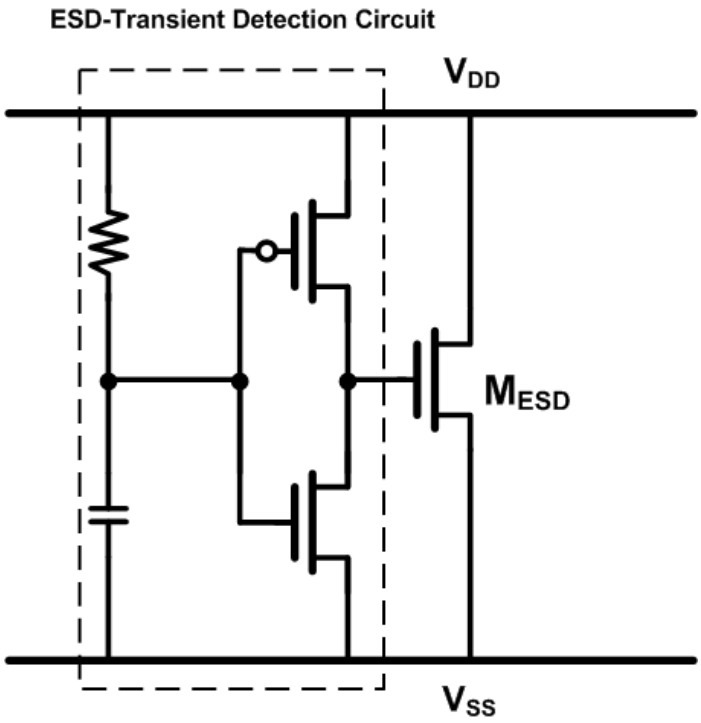


Fig. 2.5. Typical power-rail ESD clamp circuit.

A conventional ESD-transient detection circuit is an RC-detector. Since the pulse rise time of ESD events is on the order of nanosecond but that of the normal power-on events is on the order of millisecond. The RC time constant of the RC-detector should be designed to be on the order of microsecond, so the RC-detector is able to distinguish ESD events from normal power-on events.

M_{ESD} is used as a main ESD clamp device. It provides a low-impedance path for ESD current and clamps the ESD voltage between V_{DD} and V_{SS} power lines when it is triggered on by the ESD-transient detection circuit.

The pair of ESD protection devices inserted beside the I/O pad is expected to provide low-impedance ESD discharge paths among the I/O pad and power lines. A practical solution is a pair of diodes. Diode can endure a large amount of current with small device dimension. Furthermore, diode can clamp the voltage of I/O at about 0.7V when it is forward biased to

discharge ESD current. The low clamping voltage is beneficial to protecting MOS devices used in the internal circuits from being damaged by ESD stress.

In conclusion, a typical and conventional whole-chip ESD protection design is shown in Fig. 2.6. Since this ESD protection design provides proper ESD discharge paths under every ESD zapping mode, inclusive of positive-to-V_{DD} mode (PD-mode), positive-to-V_{SS} mode (PS-mode), negative-to-V_{DD} mode (ND-mode), negative-to-V_{SS} mode (NS-mode), V_{DD}-to-V_{SS} mode, and V_{SS}-to-V_{DD} mode, well ESD robustness is guaranteed. All the ESD discharge paths are shown in Fig. 2.7.

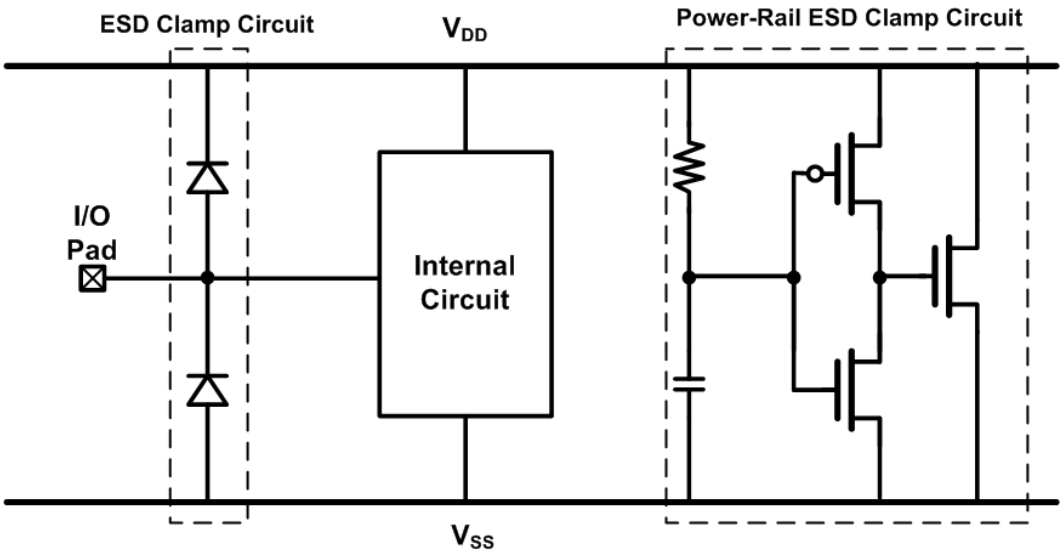
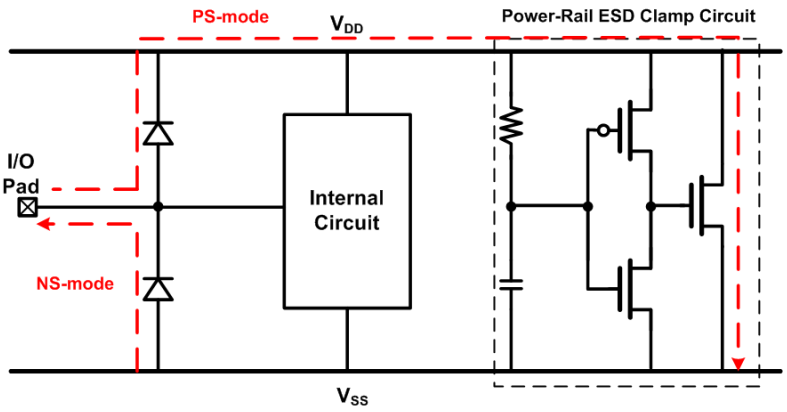
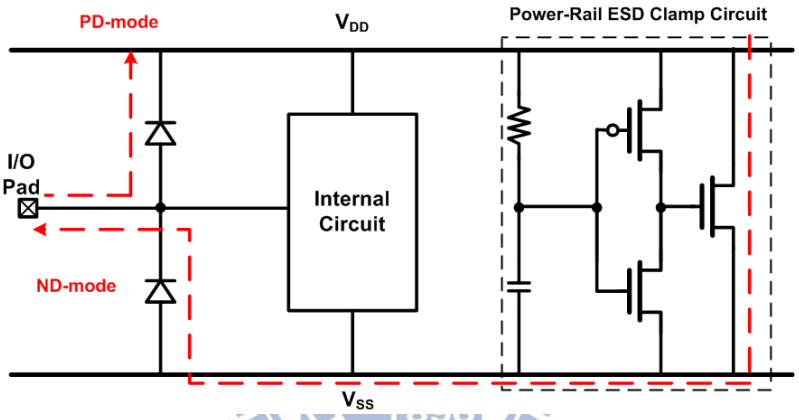


Fig. 2.6. Conventional whole-chip ESD protection design.



(a)



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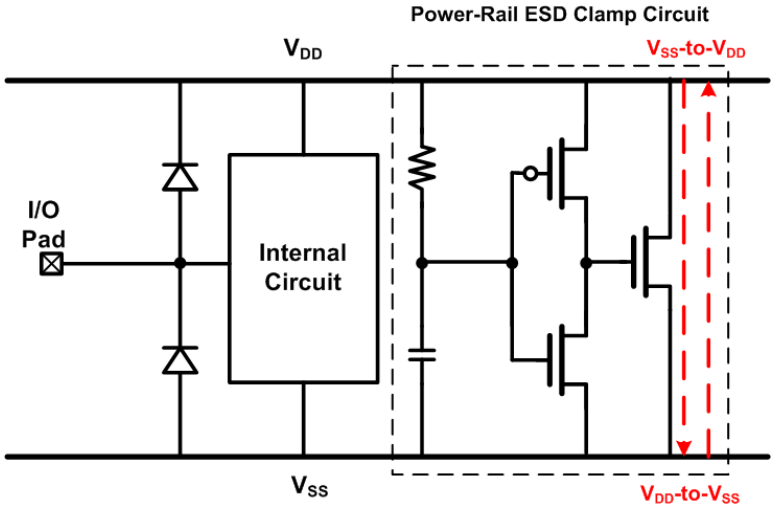


(c)

Fig. 2.7. ESD-discharge paths under (a) PS-mode and NS-mode, (b) PD-mode and ND-mode, and (c) V_{DD}-to-V_{SS} mode and V_{SS}-to-V_{DD} mode.

2.3 Issues of RF ESD Protection Design

2.3.1 Impacts of ESD protection design on RF performance

As discussed in Chapter 1, the performance of radio-frequency (RF) front-end circuits and high-speed input/output (I/O) interface circuits is degraded by the parasitic effects of the electrostatic discharge (ESD) protection devices on the signal path. If the ESD protection device is realized by the PN-junction, MOS transistor, BJT, or silicon-controlled rectifier (SCR), it is capacitive. For the RF front-end circuits, the parasitic capacitance causes signal loss from the I/O pads to the AC ground nodes. Consequently the power gain is lowered and the noise figure is increased. If an inductor is used as the ESD protection device, it exhibits inductive impedance under normal circuit operating conditions. Therefore, the impedance matching conditions are changed. As a result, the center frequency will be shifted if the inductive impedance is not considered in the impedance matching network design. For the high-speed I/O interface circuit, the ESD protection devices are mainly realized with capacitive devices. To mitigate the high-speed performance degradation, the parasitic capacitance of ESD protection devices must be as low as possible.

2.3.2 Conventional RF ESD Protection Design

To overcome these problems, many RF ESD protection design has been developed. One method is trying to cancel or isolate the parasitic capacitances from RF circuits, such as “ESD cancellation” and “ESD isolation”; other method is trying to fundamentally reduce the parasitic capacitances of ESD protection devices in order to minimize the influence on RF performance [2], [12]. Some of these methods will be briefly introduced in this section.

“ESD isolation” is a method to protect RF circuits under ESD events, and “isolate” the parasitic capacitances of ESD protection devices from RF circuits under normal operating

conditions. Well designed “ESD isolation” can provide enough ESD robustness without serious RF performance degradation. The low-capacitance ESD protection design utilizing the impedance isolation technique had been reported [7], [13] – [14]. As shown in Fig. 2.8, the LC-tank which consists of the inductor L_P and the capacitor C_P, is placed between the I/O pad and V_{DD}. Another LC-tank consisting of the inductor L_N and the capacitor C_N is placed between the I/O pad and V_{SS}. The ESD diodes D_P and D_N are used to block the steady leakage current path from V_{DD} to V_{SS} under normal circuit operating conditions. The impedance of LC-tank is infinite when LC-tank operates at its resonant frequency. For this reason, the pair of LC-tanks can be designed to resonate at the operating frequency of the internal RF circuit, and the RF input port will see infinite impedance through ESD clamp devices with the LC-tank, ideally. Therefore, the parasitic effects of ESD protection devices would not influence the RF circuit under normal operating conditions. The resonant frequency of LC-tanks is

$$\omega_0 = \frac{1}{\sqrt{L_P C_P}} = \frac{1}{\sqrt{L_N C_N}} \tag{2.15}$$

The inductances and capacitances of LC-tanks can be chosen with (2.15).

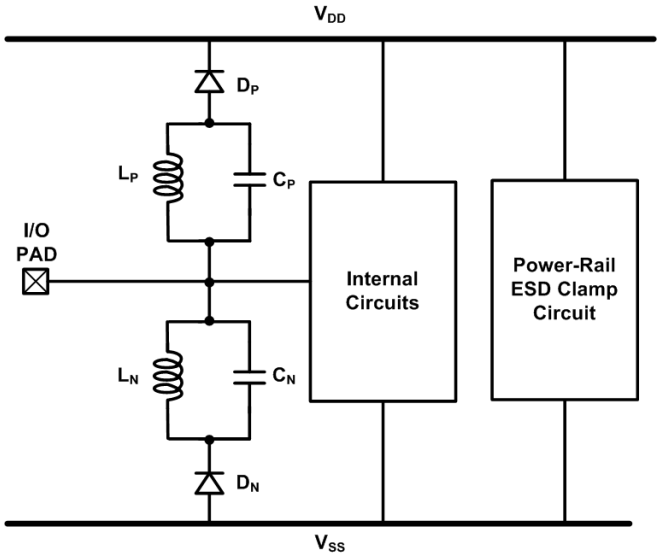


Fig. 2.8. ESD protection design with LC-tanks for RF circuits.

Another method is using series inductor and diode as ESD protection device, as shown in Fig. 2.9 [6]. The diode can be considered as a capacitor because of its parasitic effect. At the resonant frequency, there is a notch where the signal loss is very large, which means that the signal at the notch frequency will be totally lost. However, at frequencies above the resonant frequency, the impedance of the series LC resonator becomes inductive, so the magnitude of impedance increases (which means the signal loss becomes much smaller) with frequency until the self-resonant frequency of the inductor is reached. The resonant frequency of the series inductor and capacitor is the same as (2.15). Choose the resonant frequency of the series inductor and diode far away from the operating frequency of the RF circuit, and therefore the RF input port can see infinite impedance through the series inductor and diode under normal operating conditions. Thus, the parasitic effects of ESD protection devices would not influence the RF circuit. Of course, the diode serves the same function as an ESD clamp device does.

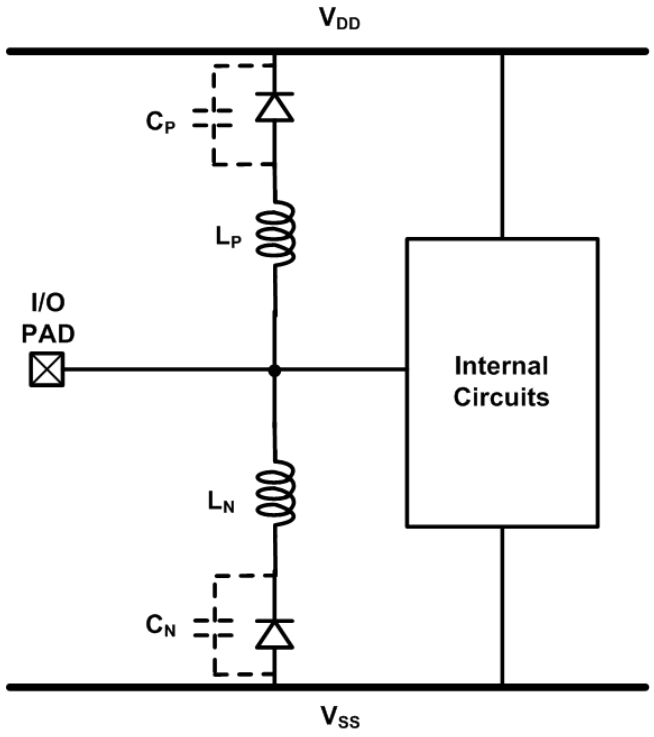


Fig. 2.9. ESD protection design with series diodes and inductors for RF circuits.

"ESD cancellation" is a method to turn ESD protection devices into a part of RF circuit so as to "cancel" the parasitic capacitances introduced by ESD protection device. A commonly used method is considering ESD protection devices as parts of matching network [15]. If an ESD protection device is simply added in front of an RF circuit, the parasitic capacitance of the ESD protection device might change the input matching condition. ESD protection devices can be treated as a part of the impedance matching network. By co-designing the ESD protection circuit and the impedance matching network, large ESD protection devices can be used to achieve high ESD robustness with their parasitic capacitance matched. Fig. 2.10 shows this method. $C_{P,ESD}$ is the parasitic capacitance of an ESD protection device which changes the input matching condition. By adding extra capacitor C_C and inductor L_G, the input impedance of the internal RF circuit can be changed from Zi_1 to Zi_2 of 50Ω. Hiding ESD protection devices in input matching network can cancel the RF performance degradation caused by the parasitic capacitance of ESD protection devices.

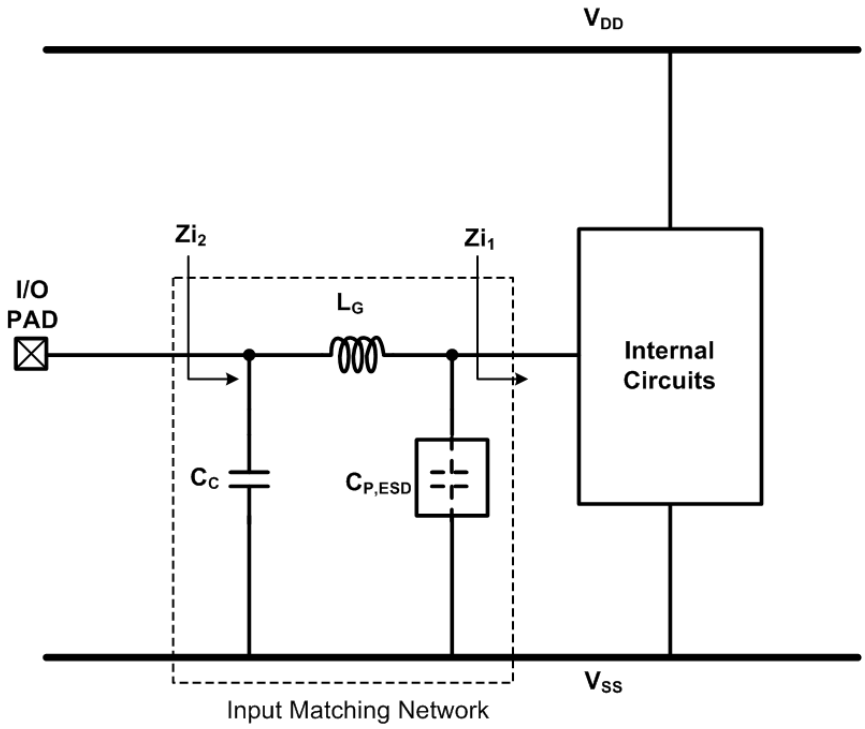


Fig. 2.10. Input matching co-design of RF circuits with ESD protection devices.

In addition, this method can be extended to broadband RF applications [16], as shown in Fig. 2.11. As shown in Fig. 2.11, The ESD protection devices are divided into several sections with decreasing size and are impedance matched by the transmission lines (T-lines) or inductors from the I/O pad to the internal RF circuit. Each ESD protection device is connected to V_{DD} or V_{SS}, which is an equivalent AC ground node. The ESD protection devices are divided into several small devices rather than one large device for broad-band RF performance. For ESD robustness, dividing the ESD protection devices into decreasing size is better than dividing them into equal size, since a larger ESD protection device inserted right beside the I/O pad is beneficial to providing a high-current-tolerant ESD discharge path under ESD events. Z_0 represents the impedance of transmission lines, coplanar waveguides, or inductors which are used to do input matching. This architecture successfully combines ESD protection devices with input matching network, and it can provide enough ESD robustness without serious RF performance degradation.

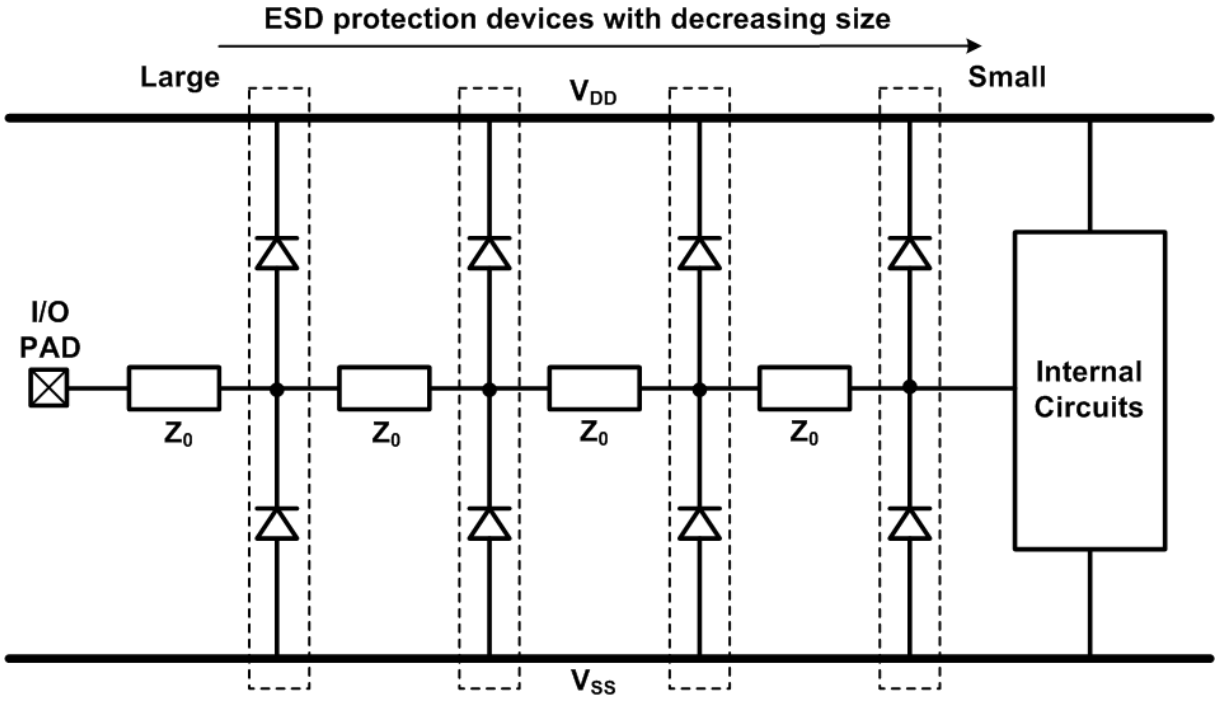


Fig. 2.11. ESD protection devices with decreasing size for broad-band RF circuits.

2.3.3 Conventional Structure of Silicon-Controlled Rectifier

The methods mentioned above are a little complex to RF circuit designers since ESD protection circuits have to be co-designed with RF circuits. Considering ESD protection designs throughout RF design phase needs more effort. Therefore, a more straightforward direction is to fundamentally decrease the parasitic capacitances of ESD protection devices. RF designers can therefore easily add low-C ESD protection devices to RF circuits without complex co-design methodology. To meet these requirements, silicon-controlled rectifier (SCR) can serve. SCR had been demonstrated to be suitable for ESD protection for high-frequency applications, because it has both high ESD robustness and low parasitic capacitance under a small layout area [17]. Layout structures which can reduce the parasitic capacitance of SCR had been investigated [18].

Fig. 2.12 and Fig. 2.13 shows the cross-section view and the equivalent circuit of a typical SCR. The SCR structure consists of P-plus (P+) diffusion, N-well, P-well, and N-plus (N+) diffusion, as shown in Fig. 2.12. This four-layer structure can be regarded as a two-terminal device consists of a lateral Q_{NPN} and a vertical Q_{PNP} bipolar transistor, as shown in Fig. 2.13.

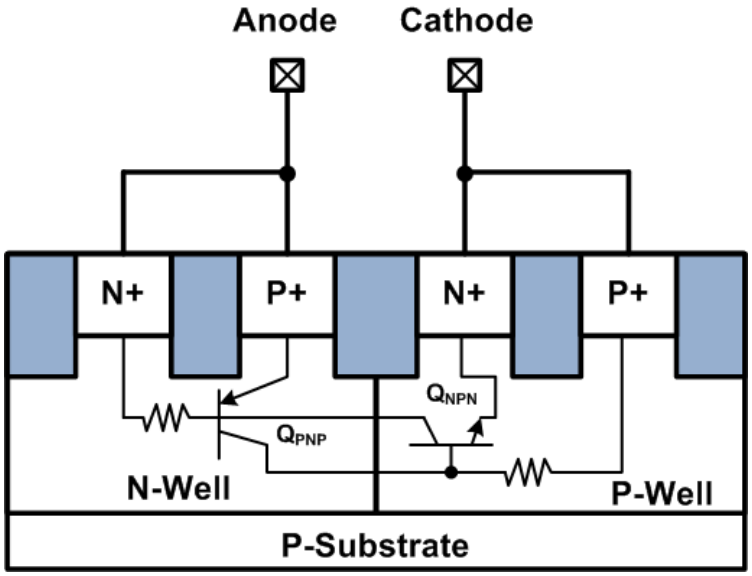


Fig. 2.12. The cross-section view of a typical SCR.

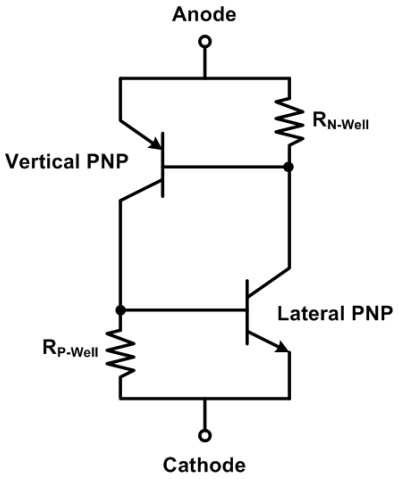


Fig. 2.13. The equivalent circuit of a typical SCR.

The DC I–V characteristics of SCR under ESD stress is shown in Fig. 2.14. Assume that positive ESD stress is applied to the anode of SCR and its cathode is relatively grounded. At the beginning, the voltage applied to the anode is less than the breakdown voltage of the N-well/P-well junction, so SCR acts like an open circuit. When the voltage applied to the anode is greater than the breakdown voltage, avalanche breakdown mechanism starts to work. Hole current flows through the P-well to the P+ diffusion connected to ground, and meanwhile electron current flows through the N-well to the N+ diffusion connected to the anode. Once the voltage drops across the P-well resistor ($R_{P\text{-well}}$) (N-well resistor ($R_{N\text{-well}}$)) is larger than 0.7 V, the parasitic NPN (PNP) transistor will be turned on. Furthermore, the parasitic NPN (PNP) transistor injects electron (hole) current to bias the PNP (NPN) transistor, and then the positive-feedback regenerative mechanism helps SCR to be successfully triggered into its latching state and have a low holding voltage (V_{hold}) ~1.5 V.

Next, assume that negative ESD stress is applied to the anode of SCR and its cathode is relatively grounded. This negative voltage drops across the parasitic diode, which consists of the P-well/N-well junction, in SCR. As long as the parasitic diode is forward biased, ESD current can be discharged and the negative voltage will be clamped at the low cut-in voltage of the parasitic diode.

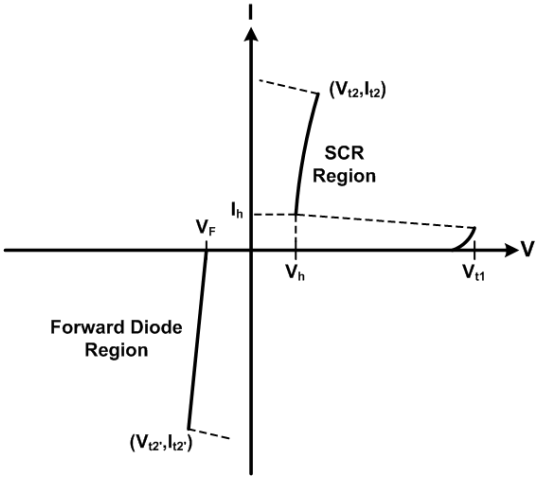
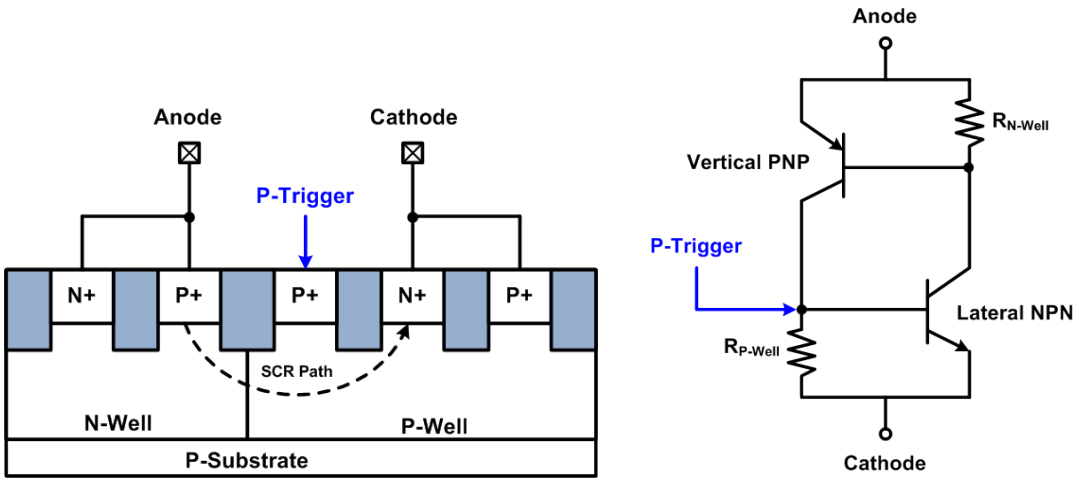


Fig. 2.14. I–V characteristics of SCR device under positive and negative voltage biases.

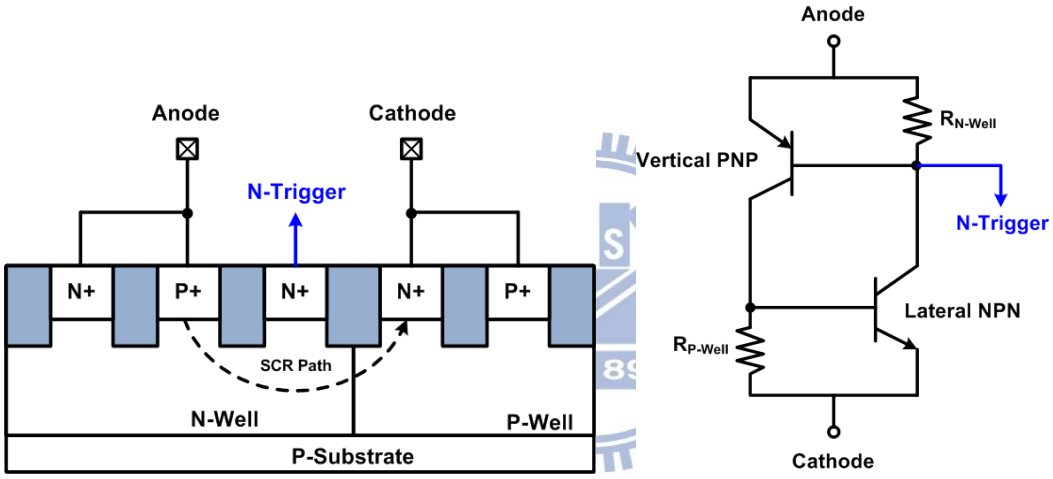
However, SCR has some drawbacks, such as higher trigger voltage and slower turn-on speed. To reduce the trigger voltage of an SCR device, the trigger signal can be sent into the base terminal of NPN BJT to enhance the turn-on speed. With the substrate-triggered technique, the p-type substrate-triggered SCR (P-STSCR) and n-type substrate-triggered SCR (N-STSCR) devices for ESD protection were reported [9]. The cross-sectional view and equivalent circuits of the P-STSCR and N-STSCR are illustrated in Fig. 2.15 and Fig. 2.16, respectively.

SCR provides suitable ESD discharging ability under every ESD stress condition, as described above. It can provide high ESD protection level within a small layout area. A smaller layout area introduces less parasitic capacitance, and therefore is beneficial to RF ESD protection.



(a) (b)

Fig. 2.15. (a) Cross-sectional view of P-STSCR. (b) Equivalent circuit of P-STSCR.



(a) (b)

Fig. 2.16. (a) Cross-sectional view of N-STSCR. (b) Equivalent circuit of N-STSCR.

Chapter 3

Design of ESD Protection Devices for RF Circuits

3.1 Conventional ESD Protection of Stacked Diodes

The conventional double-diode ESD protection scheme has been generally used for gigahertz RF circuits. In order to reduce the parasitic capacitance or provide the large signal swing tolerance, the ESD protection diodes in stacked configuration has also been presented, as shown in Fig. 3.1 and Fig. 3.2 [19]. Although stacked ESD protection devices can reduce the parasitic capacitance and leakage current, the overall turn-on resistance and the voltage across the stacked ESD protection devices during ESD stresses are increased as well, which is adverse to ESD protection. Therefore, a novel stacked diodes to improve ESD robustness is needed for RF applications.

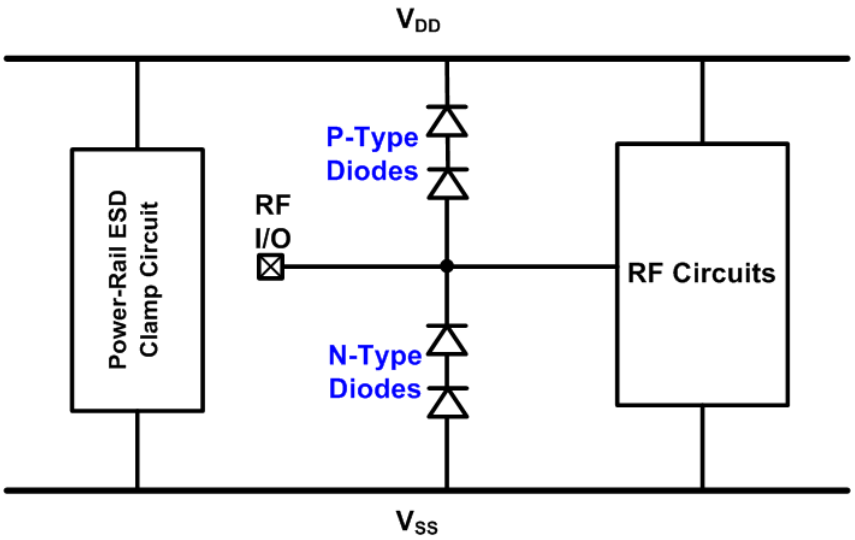
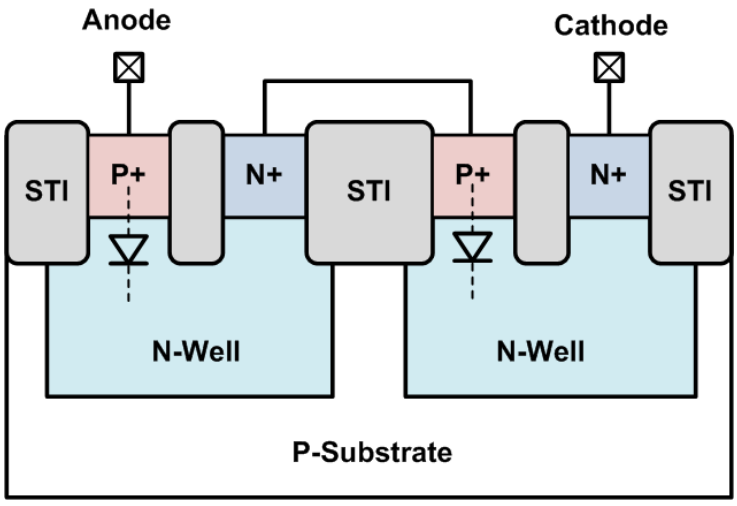
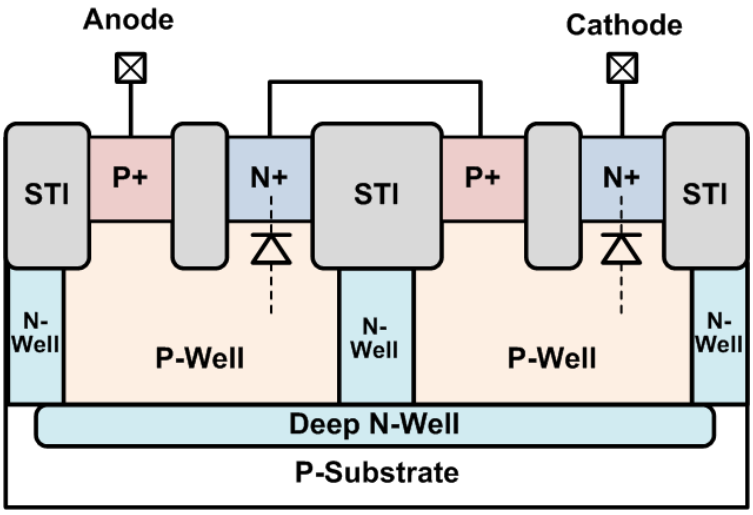


Fig. 3.1. ESD protection design with stacked diodes.



(a)



(b)

Fig. 3.2. Device cross-sectional view of (a) P-type and (b) N-type stacked diodes.

3.2 Novel ESD Protection of Stacked Diodes with Embedded SCR

The novel stacked diodes with embedded silicon controlled rectifier (SCR) are illustrated in Fig. 3.3 and Fig. 3.4. Fig. 3.3 shows the layout top view of the proposed design, and Fig. 3.4 shows the device cross-sectional view. In this work, the novel stacked diodes combines one P+/N-well diode and one P-well/N+ diode. The embedded SCR consists of P+, N-well, P-well, and N+. The deep N-well structure is used to isolate the P-well region from the

common P-substrate. The ESD current path along Q-Q' direction consists the P+/N-well diode and P-well/N+ diode. The ESD current path along R-R' direction consists P+/N-well/P-well/N+ SCR. The width of diode path (T) is defined as the sum of all segments of t in Fig. 3.3, and the width of SCR path (W) is the sum of all segments of w_1 and w_2. The SCR device has been reported to be useful for ESD protection with low turn-on resistance, low parasitic effects, and high ESD robustness. However, the stand-alone SCR device has drawbacks of high turn-on voltage and low turn-on speed. To improve the turn-on speed and reduce the turn-on voltage, the trigger current sent into the base terminal of the PNP and NPN is need. In this design, the diode path also plays the role of trigger circuit of SCR to enhance its turn-on speed [9], [17]. In the beginning of ESD stress, the diode path ((1)-(1')) will turn on first to discharge the initial current, and then the SCR path ((2)-(2')) take over to discharge the main current. Since the primary ESD current is discharged through the SCR path, the distance from anode to cathode of SCR (D) is wished to be minimized to reduce the turn-on resistance.

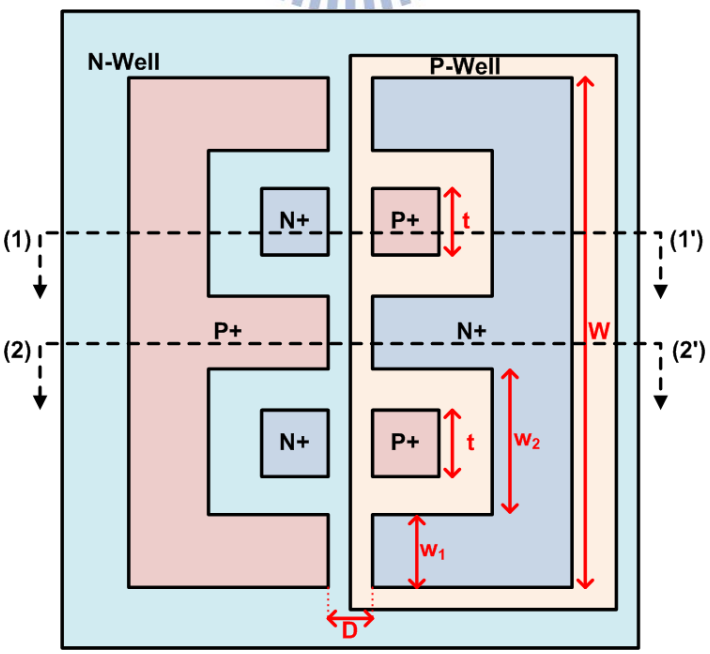
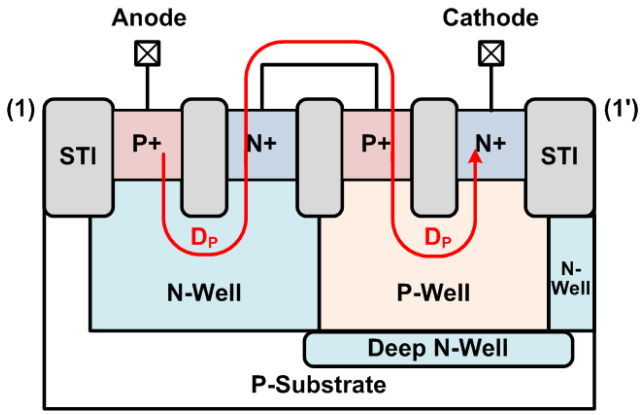
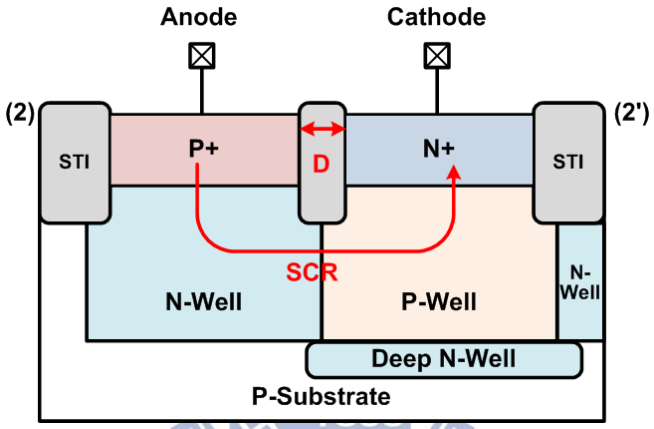


Fig. 3.3. Layout top view of type A novel stacked diodes.



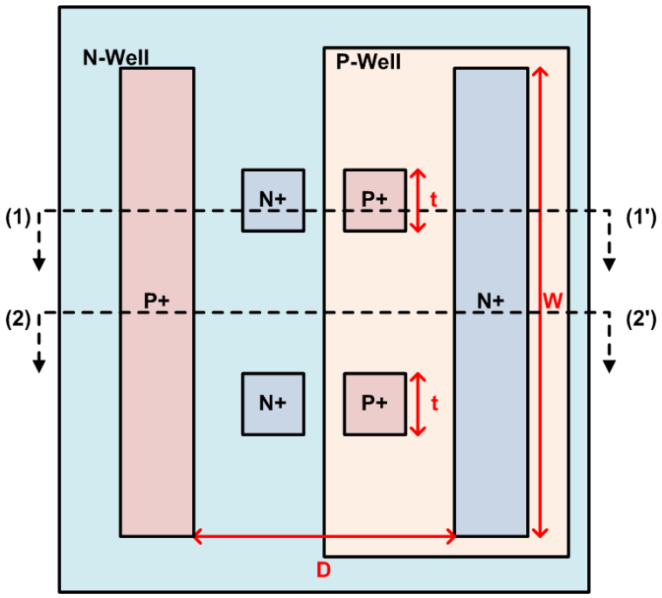
(a)



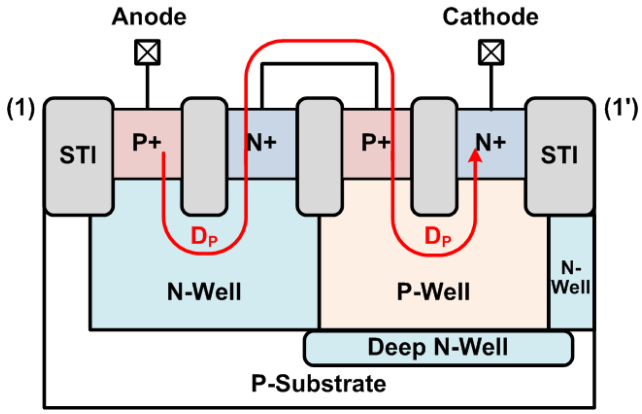
(b)

Fig. 3.4. Cross-sectional view of novel stacked diodes type A along (a) (1)-(1') and (b) (2)-(2').

For comparison purpose, two different layout structures which called type B and type C are also implemented in the same CMOS process. The layout top view and cross-sectional view of these two structures are illustrated in Fig. 3.5 and Fig. 3.6.



(a)



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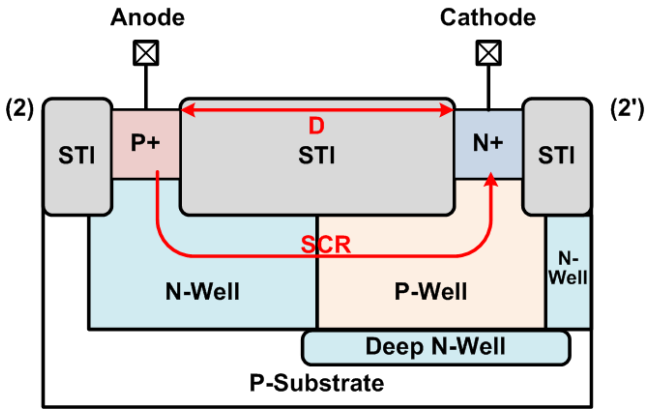
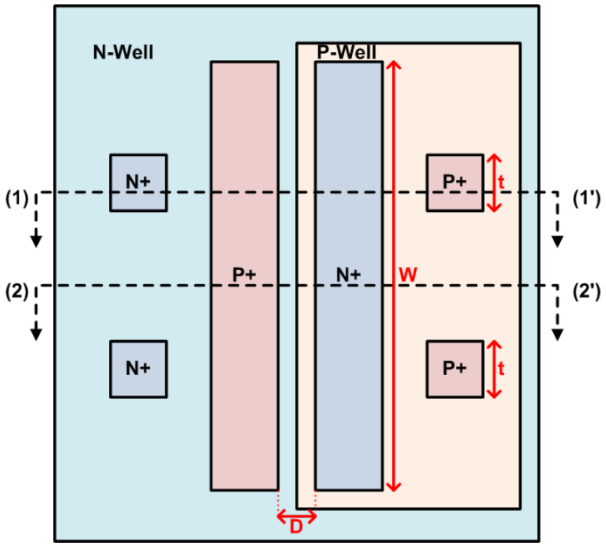
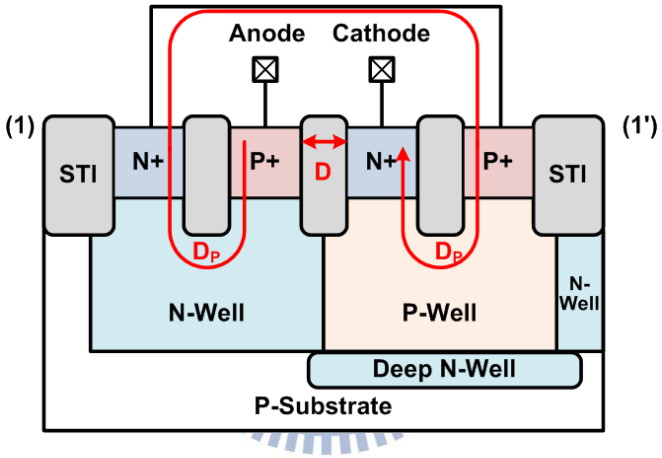


(c)

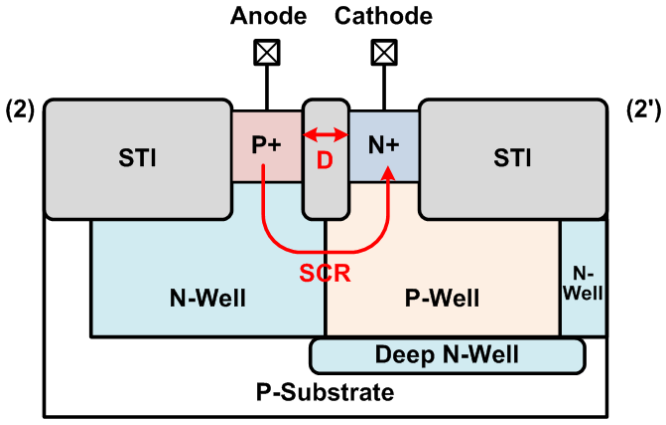
Fig. 3.5. (a) Layout top view and cross-sectional view (b) (1)-(1') and (c) (2)-(2') of novel stacked diodes type B.



(a)



(b)



(c)

Fig. 3.6. (a) Layout top view and cross-sectional view (b) (1)-(1') and (c) (2)-(2') of novel stacked diodes type C.

3.3 Experimental Results

3.3.1 Test Devices

These test devices have been fabricated in a 65-nm salicided CMOS process without using the silicide-blocking mask. The chip photograph of test devices is shown in Fig. 3.7. These test devices are arranged with ground-signal-ground (G-S-G) style in layout to facilitate the on-wafer RF measurement. The widths of the test circuits (W) are arranged as 20μm, 30μm, and 40μm. The widths of diode path (T) of type A are equal to W/2, W/4, or W/8. The widths of diode path (T) of type B and C are selected to be W/4 or W. The distance from anode to cathode of SCR (D) is 0.32μm.

For comparison purpose, the stand-alone P diode, N diode, P stacked diodes, and N stacked diodes with W=40μm are also implemented in 65-nm CMOS process. All these dimensions of test devices are listed in Table I.

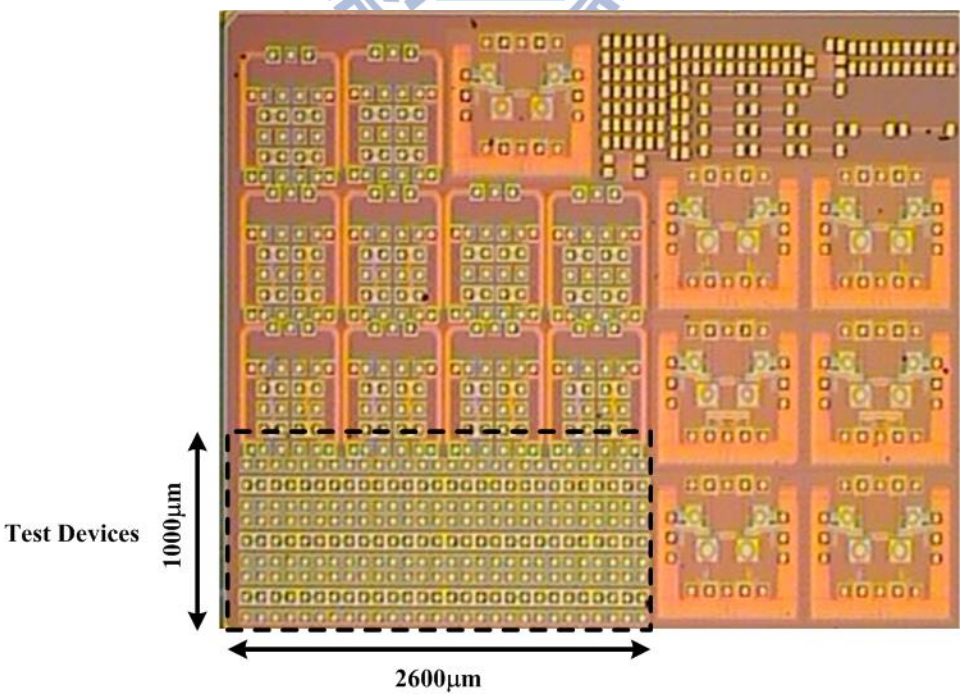


Fig. 3.7. The chip photograph of test devices.

3.3.2 Measured Parasitic Capacitance

With the on-wafer measurement, the two-port S-parameters of the test devices were measured by using the vector network analyzer. The source and load resistances to the test devices are kept at 50 Ω. In order to extract the intrinsic characteristics of the test devices in high frequencies, the parasitic effects of the G-S-G pads have been removed by using the de-embedding technique [20]. The test patterns, one including the DUT and the other excluding the DUT, as shown in Fig. 3.8, were fabricated in the same experimental test chip. The measured Y-parameter of the including-DUT pattern is labeled as Y_{11_meas}, and the measured Y-parameter of the excluding-DUT pattern is labeled as Y_{11_pad}. The intrinsic device characteristics (Y_{11_DUT}) can be obtained by subtracting Y_{11_pad} from Y_{11_meas}. The parasitic capacitance (C_{ESD}) of each test device can be extracted from the S-parameters by using

$$C_{ESD} = \frac{\mathrm{Im}\left(Y_{11\_DUT}\right)}{2\pi f} \tag{3.1}$$

where f is the operating frequency. In fact, the parasitic effects consist of capacitances and resistances. As shown in Fig. 3.9(a), the capacitances exist at P+/N-well (C_{S1}) and N+/P-well (C_{S2}) junctions. The resistances exist in N-well (R_{S1}) and P-well (R_{S2}). Since the capacitances (C_{S1} and C_{S2}) and the resistances (R_{S1} and R_{S2}) are in series, the series capacitance (C_S) can be expressed as (C_{S1}*C_{S2})/(C_{S1}+C_{S2}), and the series resistance (R_S) can be expressed as R_{S1}+R_{S2}. The parasitic capacitance (C_{ESD}), as defined in Fig. 3.9(b), can be calculated by

$$C_{ESD} = \frac{1}{1+\left(2\pi f R_S C_S\right)^2} C_S \tag{3.2}$$

The parasitic capacitance (C_{ESD}) slightly decreased with the increased frequency due to the series parasitic resistance (R_S). Fig. 3.10~13 shows the extracted parasitic capacitances of the test devices from 1 to 30 GHz.

The parasitic capacitances of the novel stacked diodes with w=20μm/30μm/40μm are about 20fF/30fF/40fF. As the Fig. 10 shown, the parasitic capacitances of novel device type A are

slightly increased with the narrower T, which is identical to the narrowed w_2 and the widened w_1. This is perhaps because the total capacitance is dominated by P+/N-well and N+/P-well between two terminals. The source and load resistances to the test circuits were kept at 50 Ω.

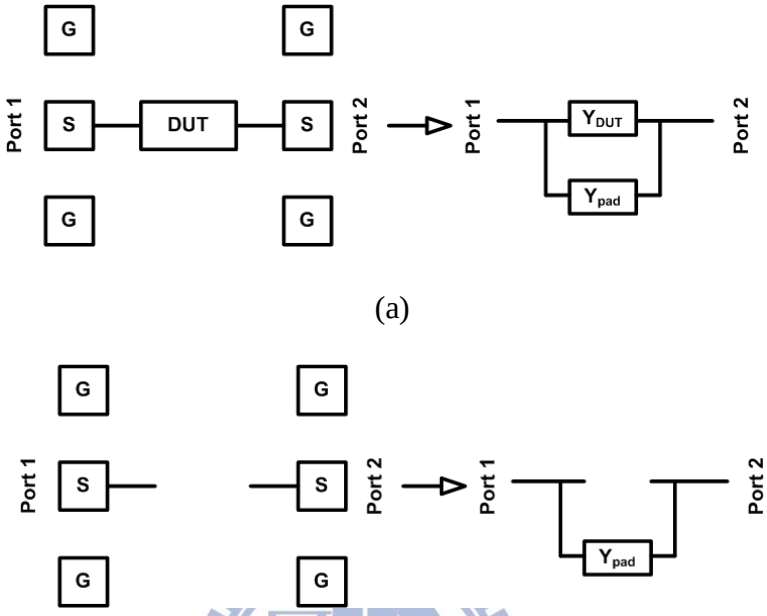


Fig. 3.8. The layout top view with ground-signal-ground (G-S-G) pads and the equivalent model of (a) including-DUT pattern and (b) excluding-DUT pattern.

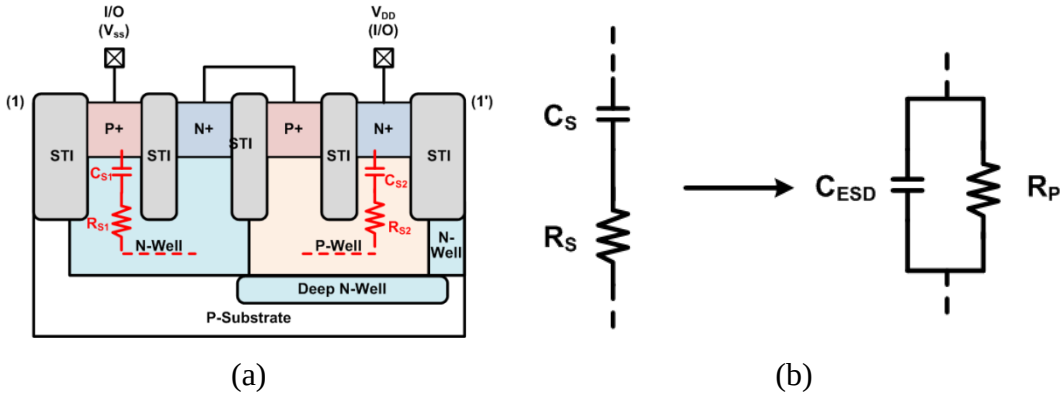
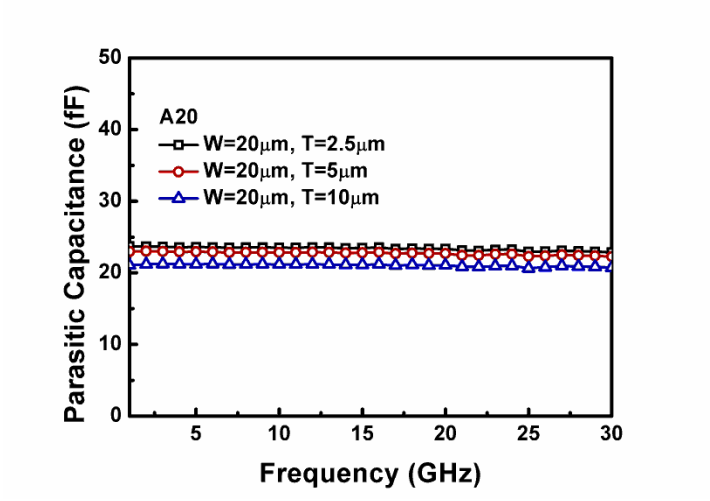
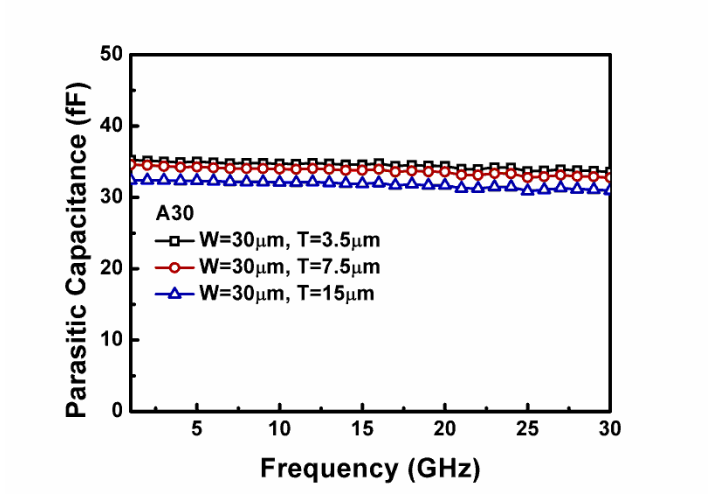


Fig. 3.9. (a) The schematic diagram of parasitic capacitances (C_{S1} and C_{S2}) and parasitic resistances (R_{S1} and R_{S2}) and (b) the equivalent model of measured capacitance C_{ESD}.



(a)



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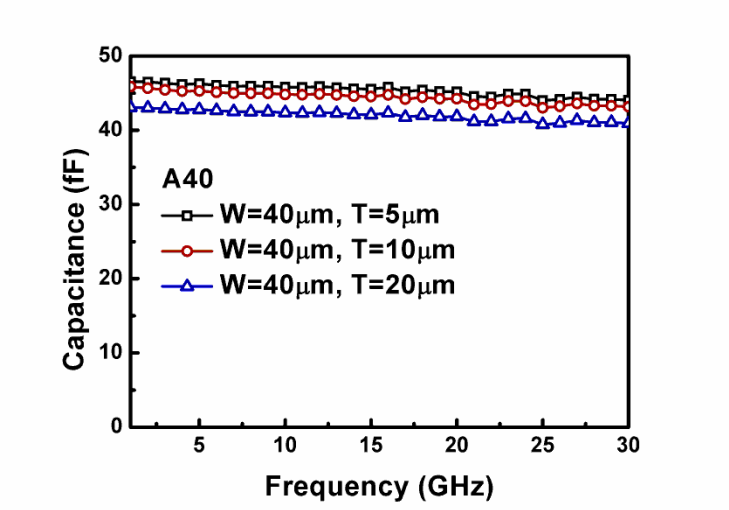
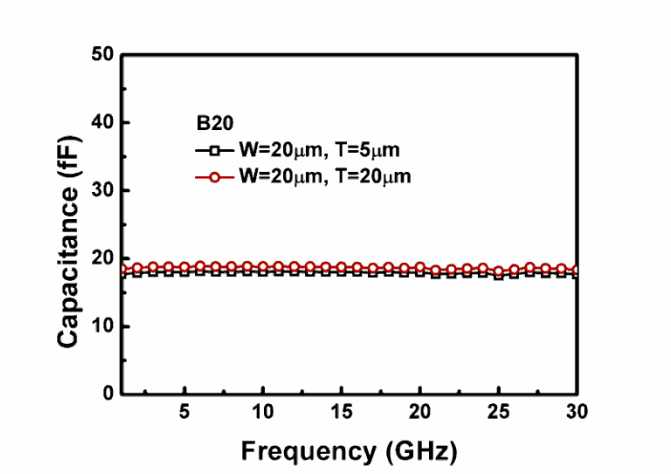
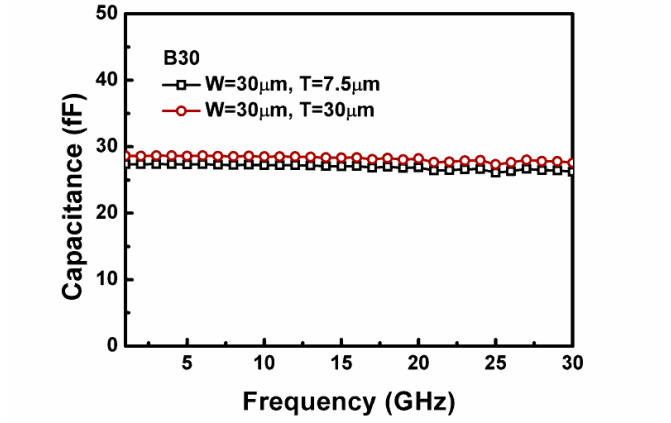


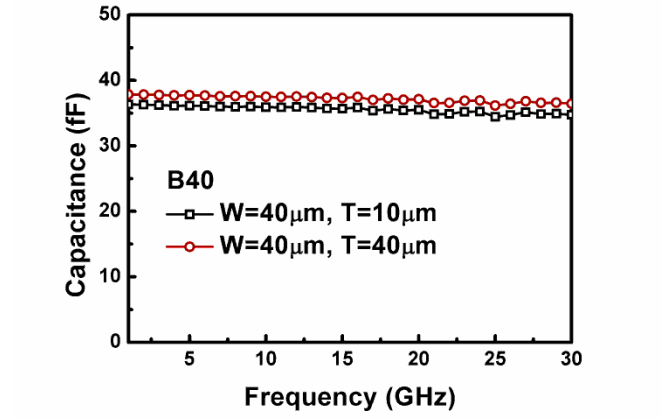
Fig. 3.10. Measured parasitic capacitances of device type A with (a) W=20μm, (b) W=30μm, and (c) W=40μm.



(a)

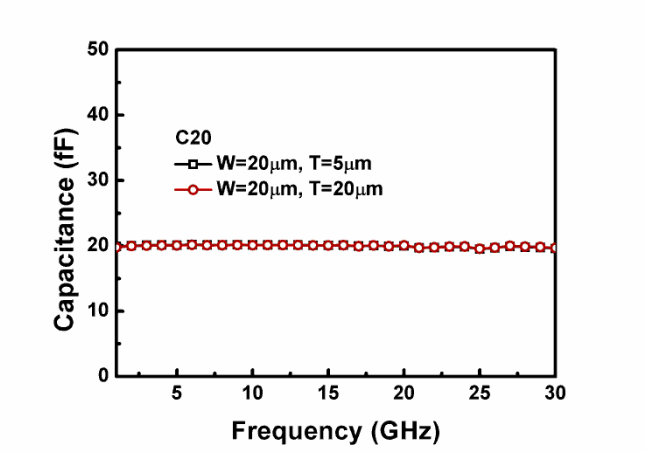


(b)

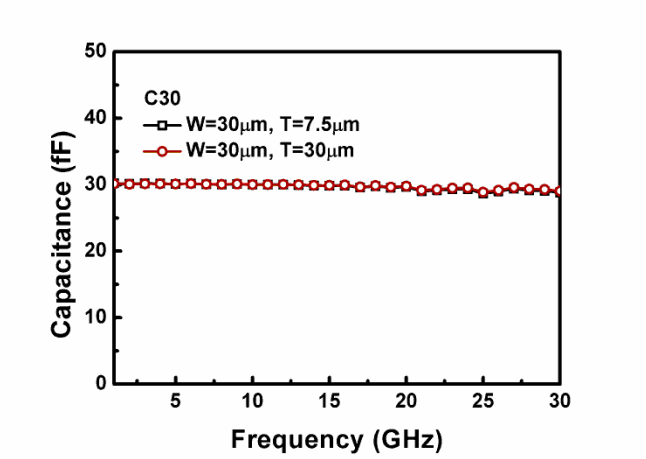


(c)

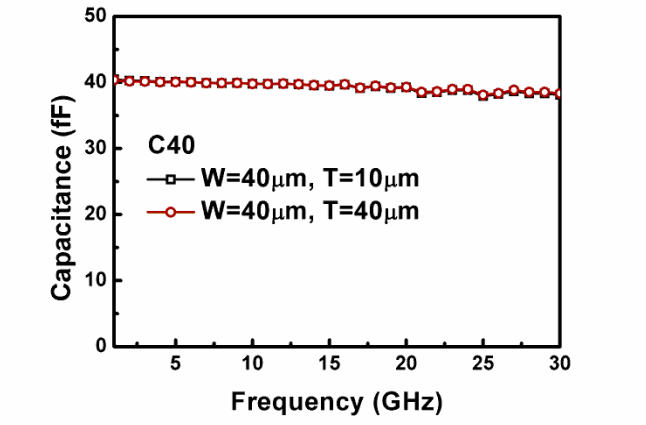
Fig. 3.11. Measured parasitic capacitances of device type B with (a) W=20μm, (b) W=30μm, and (c) W=40μm.



(a)

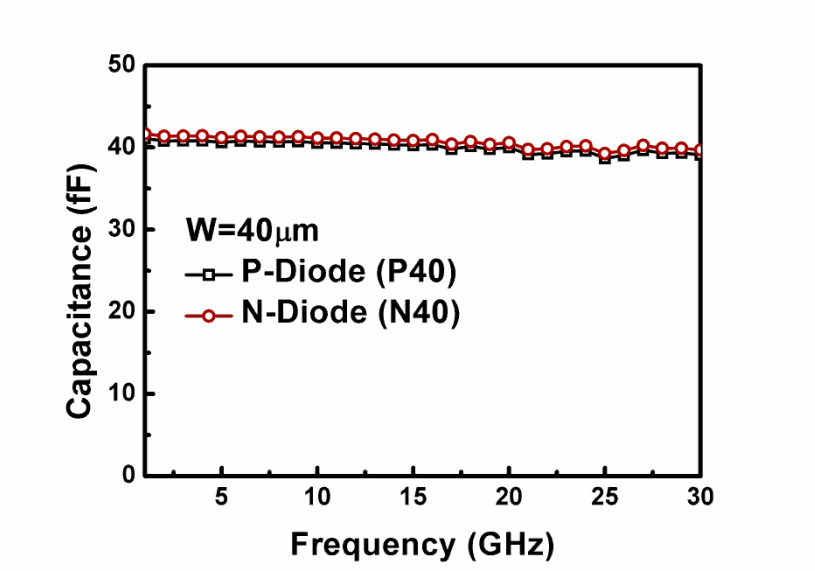


(b)

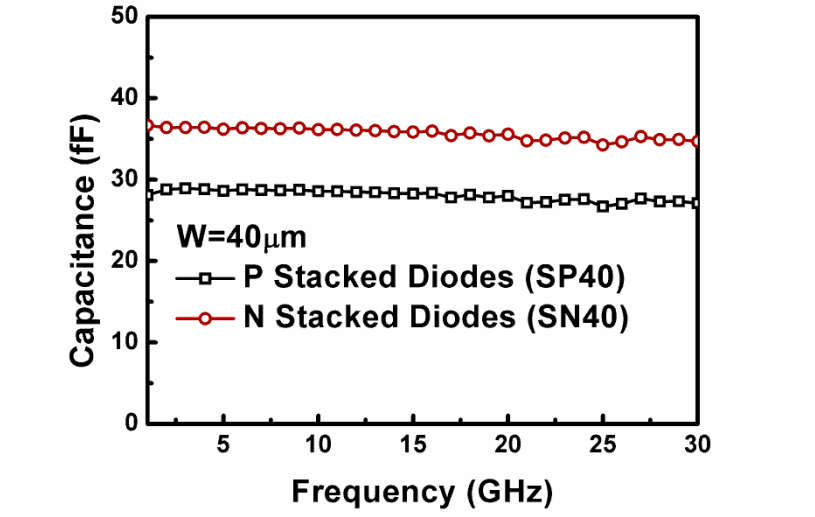


(c)

Fig. 3.12. Measured parasitic capacitances of device type C with (a) W=20μm, (b) W=30μm, and (c) W=40μm.



(a)

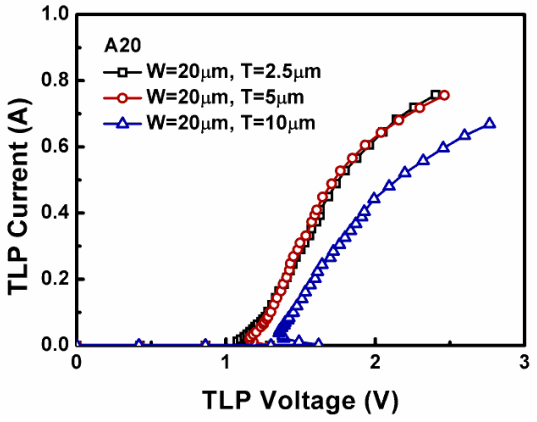


(b)

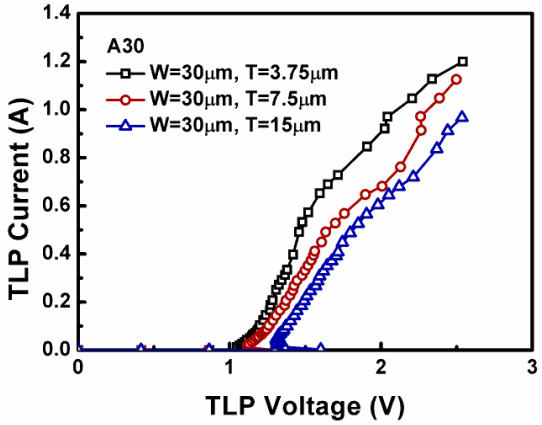
Fig. 3.13. Measured parasitic capacitances of (a) diode and (b) stacked diodes with W=40μm.

3.3.3 Measured ESD Robustness

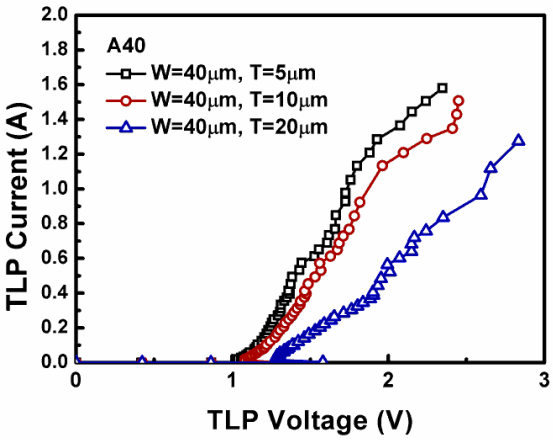
To investigate the turn-on behavior and the I-V characteristics in high-current regions of the ESD protection circuits, the transmission-line-pulsing (TLP) system with 10-ns rise time and 100-ns pulse width is used [21]. The TLP-measured IV characteristics are shown in Fig. 3.14~17. The trigger voltages (V_{t1}) of test devices type A are about 1.3V, type B are about 1.6V, and type C are about 1.5V. Due to the assistance of embedded SCR, the turn-on resistances are significantly reduced. The TLP-measured current compression point (I_{CP}), which is defined as the current level deviates from the linearly extrapolated low-current curve by 20% [22], of the proposed designs type A with w=20μm/30μm/40μm are about 0.7A/1.1A/1.3A. The I_{CP} of the proposed designs are improved, as compared with those of the traditional diode and stacked diodes. To evaluate the effectiveness of the proposed ESD protection circuit in faster ESD-transient events, a very-fast-TLP (VFTLP) system with 0.2-ns rise time and 1-ns pulse width is used in this study. The VFTLP system can be used to capture the transient behavior of ESD protection circuits in the time domain of charged-device-model (CDM) ESD event [23]. The VFTLP measured I–V characteristics of the proposed devices type A are shown in Fig. 3.18. As the width of diode path (T) increased, the turn-on speed of embedded SCR decreased.



(a)

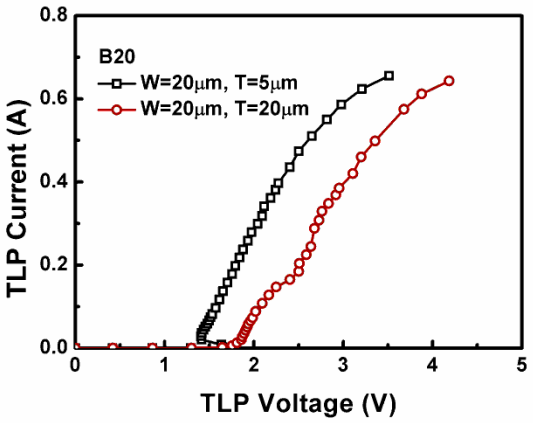


(b)

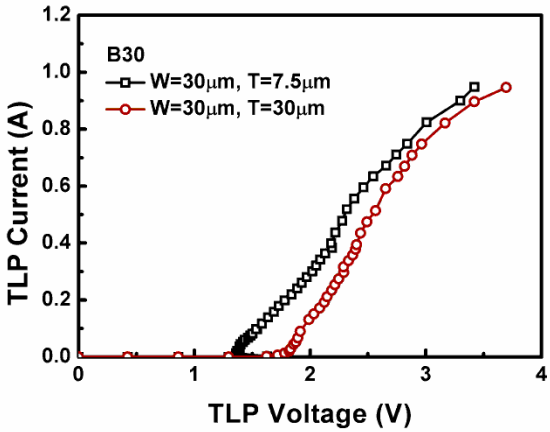


(c)

Fig. 3.14. TLP-measured I-V characteristics of device type A with (a) W=20μm, (b) W=30μm, and (c) W=40μm.



(a)



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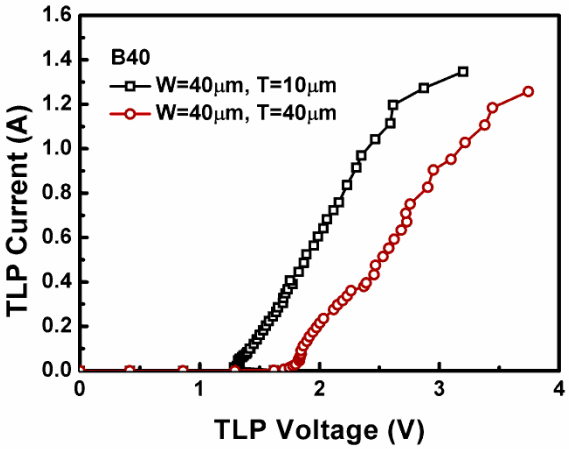
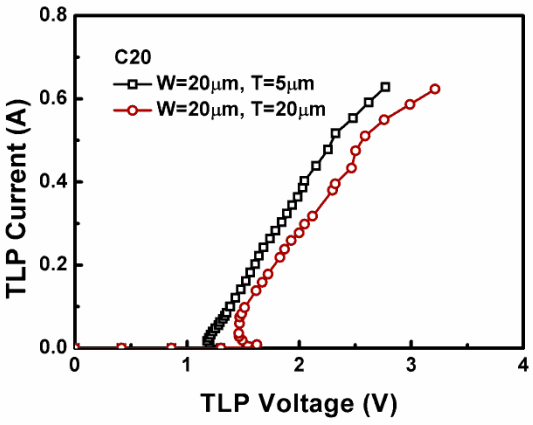
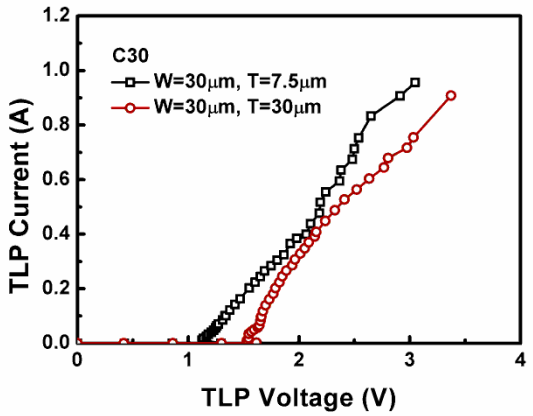


(c)

Fig. 3.15. TLP-measured I-V characteristics of device type B with (a) W=20μm, (b) W=30μm, and (c) W=40μm.



(a)



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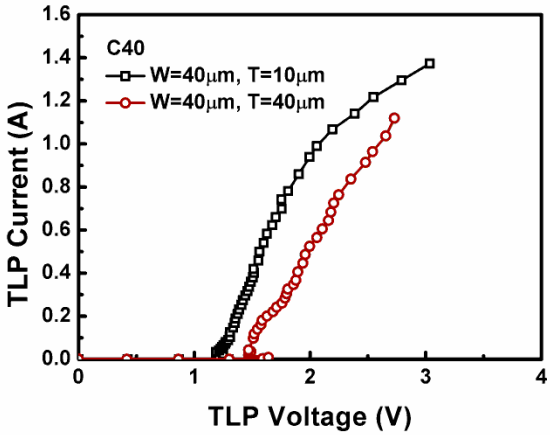
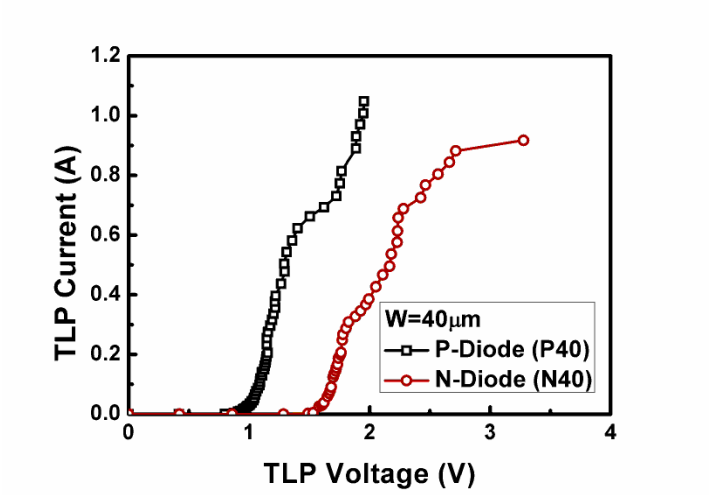
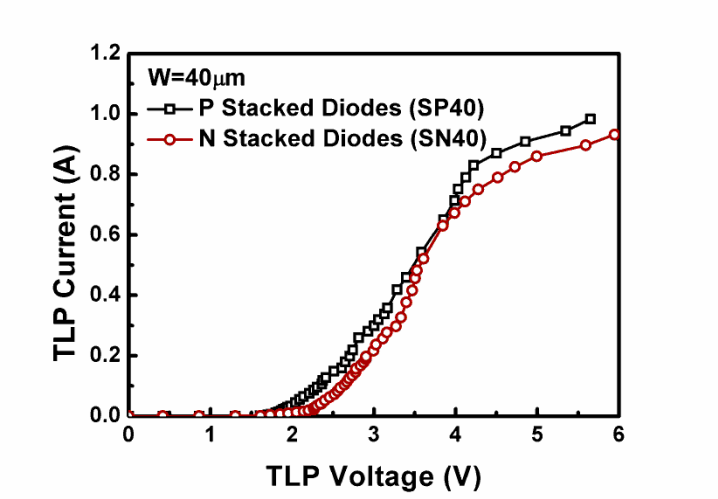


(c)

Fig. 3.16. TLP-measured I-V characteristics of type C device with (a) W=20μm, (b) W=30μm, and (c) W=40μm.

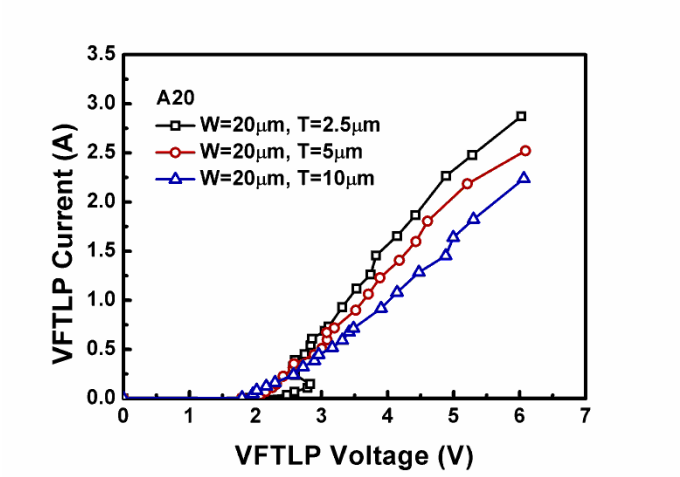


(a)

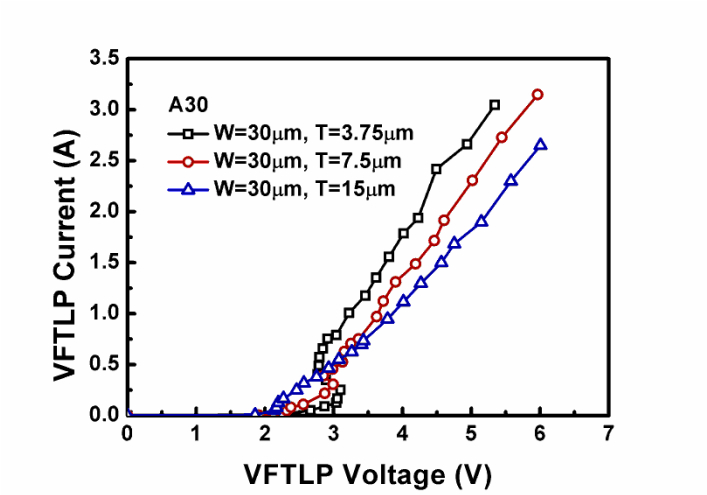


(b)

Fig. 3.17. TLP-measured I-V characteristics of (a) diode and (b) stacked diodes with W=40μm.



(a)



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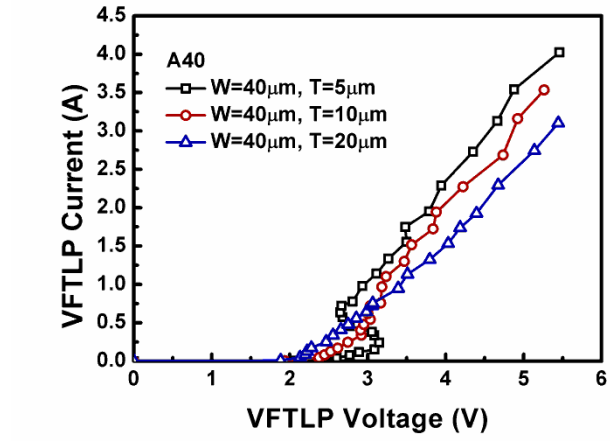


(c)

Fig. 3.18. Very-fast-TLP I-V characteristics of proposed device type A with (a) W=20μm, (b) W=30μm, and (c) W=40μm.

The human-body-model (HBM) ESD robustness of the all test devices are evaluated by the ESD tester. For the proposed design A, the test device A40 with W=40μm and T=5μm can pass 3.5kV HBM ESD robustness. For the proposed design B, the test device B40 with W=40μm and T=10μm can achieve 2kV HBM ESD robustness. For the proposed design C, the test device C40 with W=40μm and T=10μm can achieve 2kV HBM ESD robustness. While the P diode or N diode with the same width can achieve 2.25kV and 2kV HBM ESD robustness, respectively. The P stacked diodes or N stacked diodes with the same width has only 1.5kV HBM ESD robustness. All these measured ESD robustness are listed in Table I.

3.4 Summary

Among the splits of the proposed designs type A, B and C, the test device A40 can achieve 3.5-kV HBM ESD robustness with W=40μm and T=5μm. Since the parasitic capacitance of type B is a little smaller than that of type A, type A can achieve higher ESD robustness. Although the turn-on resistance of type C is a little smaller than that of type A, the parasitic capacitance of type A is a little smaller than that of type C. The ratio of HBM ESD robustness and parasitic capacitance of the test devices are compared in Table I. The novel stacked diodes type A with W=40μm and T=5μm has the best ratio (HBM/C) of 75.4, while the P stacked diodes and N stacked diodes with the same width has only 51.9 and 41.3, respectively.

Therefore, the compact ESD protection circuit for RF circuits can be realized by using the test device type A. The proposed design can easily be used for RF circuits. The novel stacked diodes with embedded SCR has been designed, fabricated, and characterized in a 65-nm CMOS process. The optimization on layout style of stacked diodes with embedded SCR is more suitable for on-chip ESD protection due to its low turn-on resistance, low parasitic capacitance, and high ESD robustness. This layout style can be further extended to the stacked diodes with more diodes.

Table I
Comparisons of Experimental Results Among ESD Protection Devices in Silicon

Test Device	Type	W (μm)	T (μm)	D (μm)	C @ 2.4 GHz (fF)	HBM (kV)	TLP V_{t1} (V)	TLP R_{on} (Ω)	TLP I_{CP} (A)	HBM/C@2.4 GHz(V/fF)
A20	Proposed Design	20	2.5	0.32	23.6	1.75	1.29	1.19	0.72	74.2
			5		23	1.5	1.3	1.24	0.67	65.2
			10		21.2	1.25	1.62	1.62	0.6	59
B20			5	1.02	17.9	1	1.65	2.9	0.66	55.9
			20		18.7	1	1.64	3.6	0.68	53.5
C20			5	0.32	20.1	1	1.3	1.2	0.66	49.8
			20		20	1	1.6	1.52	0.69	50
A30		30	3.75	0.32	35.1	2.5	1.3	1.02	1.2	71.2
			7.5		34.4	2.25	1.3	1.17	1.16	65.4
			15		32.4	2	1.6	1.35	1.16	61.7
B30			7.5	1.02	27.3	1.5	1.63	2.2	0.95	54.9
			30		28.6	1.5	1.62	2.6	1	52.4
C30			7.5	0.32	30.1	1.5	1.3	1.15	1.03	49.8
			30		30	1.5	1.62	2.2	0.96	50
A40		40	5	0.32	46.4	3.5	1.3	0.66	1.66	75.4
			10		45.5	3.25	1.3	0.76	1.62	71.4
			20		42.9	2.75	1.58	1.12	1.45	64.1
B40			10	1.02	36.2	2	1.62	1.2	1.35	55.2
			40		37.8	2	1.62	1.5	1.26	52.9
C40			10	0.32	40.2	2	1.3	0.75	1.37	49.8
			40		40.1	2	1.64	1.06	1.27	49.9
P40	P Diode	40	N/A	N/A	40.8	1.5	0.8	1.08	1.05	36.8
N40	N Diode				41.4	1.5	0.86	1.4	0.92	36.2
SP40	P Stacked Diodes				28.9	1.5	1.61	3.02	0.91	51.9
SN40	N Stacked Diodes				36.3	1.5	1.61	3.14	0.9	41.3

Chapter 4

Design of ESD Protection Circuit for Differential RF Circuits

4.1 Traditional ESD Protection Design for Differential RF LNA

In an RF receiver, the low-noise amplifier (LNA) plays a very important role because it is the first stage in the RF receiver. A differential configuration is used for LNA design because the advantages of common-mode noise-rejection, less sensitivity to substrate noise, supply noise, and bond-wire inductance variation [24]-[26]. In addition, the differential output signals of the differential LNA can be directly connected to the differential inputs of the double balanced mixer [27].

The LNA is usually connected to the external of the RF receiver chip. Therefore, on-chip ESD protection circuits must be added at the first stage of RF receiver. As shown in Fig. 4.1, the ESD protection circuits are added to the input (RF_{IN}) pads of the LNA against ESD damages. Parasitic capacitance of the ESD protection device is one of the most important design considerations for gigahertz differential LNA.

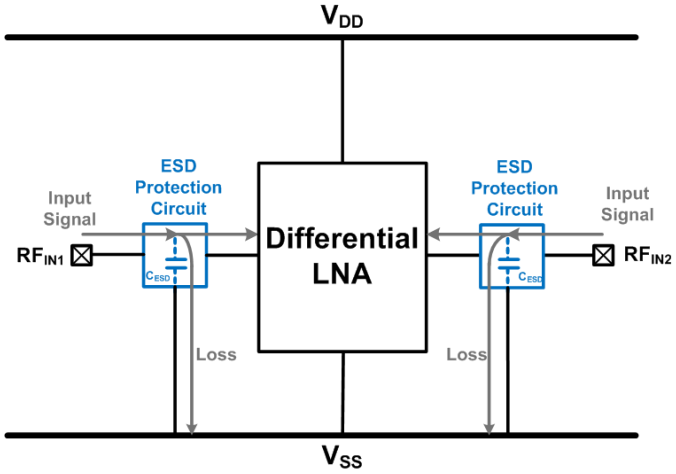
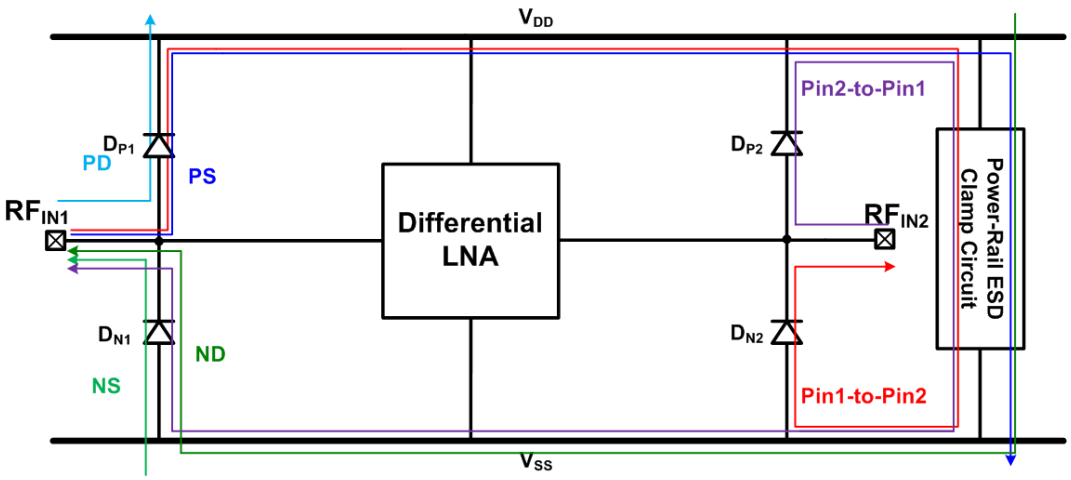
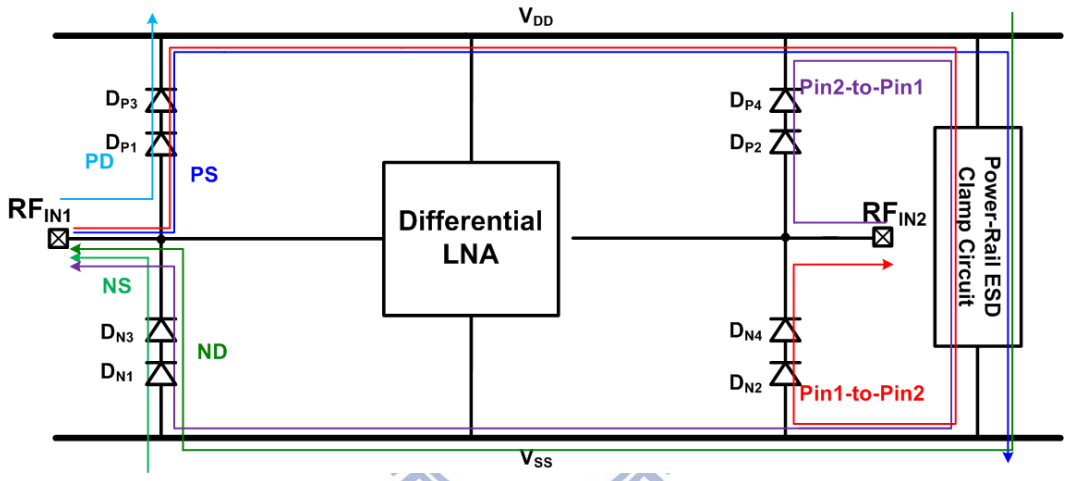


Fig. 4.1. Differential LNA with ESD protection devices.



(a)



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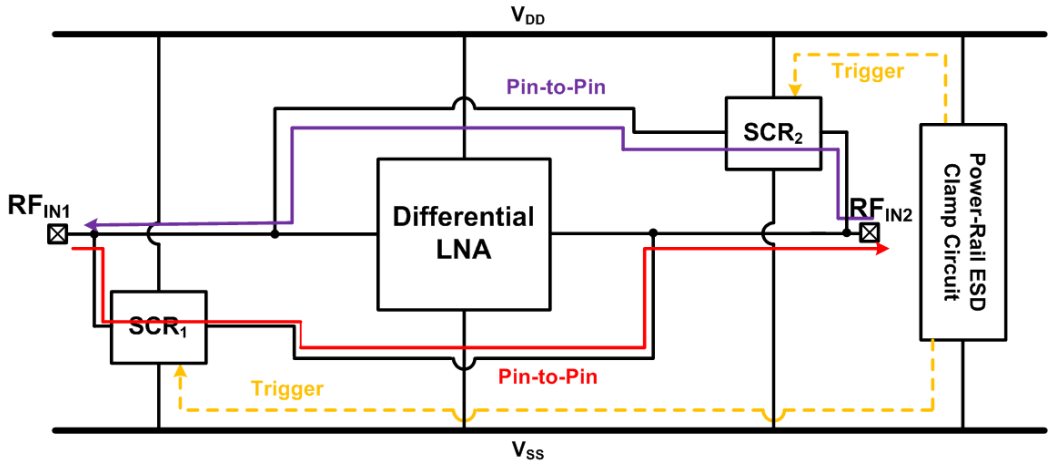


(c)

Fig. 4.2. Differential LNA with conventional ESD protection design of (a) dual diodes, (b) stacked diodes, and (c) cross-coupled SCR.

In the ESD-test standards, there are several ESD-test pin combinations. In addition to the positive-to-V_{DD} (PD), positive-to-V_{SS} (PS), negative-to-V_{DD} (ND), and negative-to-V_{SS} (NS) ESD tests, the pin-to-pin ESD test is also specified to evaluate ESD robustness of the differential input pads. Under the pin-to-pin ESD test, one input pad is stressed with the other input pad relatively grounded, while all the other pads including all V_{DD} and V_{SS} pads are floating [28]. The conventional ESD protection design with dual diodes has been generally used for gigahertz differential LNA [25], as shown in Fig. 4.2(a). The ESD current will be discharged through D_{P1}, V_{DD} bus, power-rail ESD clamp circuit, V_{SS} bus, and D_{N2} under pin1-to-pin2 ESD stresses. Since the pin-to-pin ESD current path is longer than PD, PS, ND, or NS ESD current path, the pin-to-pin ESD stress was the most critical ESD events for the differential input pads. To adapt some applications, the ESD protection design with stacked diodes has also been used [19], as shown in Fig. 4.2(b). As the Fig. 4.2 (a) and Fig. 4.2 (b) shown, the voltage drop across the ESD current path of LNAs with ESD protection can be calculated as

$$V_{ESD,Dual\ Diodes} = V_{D_{P1}} + V_{V_{DD\_Bus}} + V_{Power\_Clamp} + V_{V_{SS\_Bus}} + V_{D_{N2}} \quad (4.1)$$

$$V_{ESD,Stacked\ Diodes} = V_{D_{P1}} + V_{D_{P3}} + V_{V_{DD\_Bus}} + V_{Power\_Clamp} + V_{V_{SS\_Bus}} + V_{D_{N2}} + V_{D_{N4}} \quad (4.2)$$

Since the pin-to-pin ESD current path is even longer in the stacked diodes, the ESD protection design with dual silicon-controlled rectifier (SCR) has been presented to improve the pin-to-pin ESD robustness [29], because the clamping voltage of SCR is much lower than that of diode under ESD stress. To further reduce the voltage drop under pin-to-pin ESD stress, the ESD protection design with cross-coupled SCR has been presented [30], as shown in Fig. 4.2(c). Under pin-to-pin ESD stresses, the ESD current will be discharged through SCR_1 or SCR_2. The voltage drop across the ESD current path of LNAs with cross-coupled

SCR can be calculated as

$$V_{ESD,Cross\_couple\ SCR} = V_{SCR_1}\ or\ V_{SCR_2} \tag{4.3}$$

However, in this design, the trigger circuit of SCR is needed to enhance the turn-on speed of SCR under ESD stress. The cross-coupled SCR and power-rail ESD clamp circuit need to be co-designed; therefore, this ESD protection design may be hard for RF circuit designer to apply ESD protection in the gigahertz differential LNA.

In this work, a novel ESD protection design by using ESD protection diodes with embedded SCR is proposed for effective ESD protection in the gigahertz differential LNA. All the components used in the proposed design are embedded in a compact cell. The proposed ESD protection design is suitable for RF circuit designer for them to easily apply ESD protection in the gigahertz differential LNA.

4.2 Novel ESD Protection Design for Differential RF LNA

The new proposed ESD protection circuit utilizes stacked diodes embedded silicon-controlled rectifier (SCR) as main ESD-current-discharging paths. The proposed ESD protection circuit is shown in Fig. 4.3. The power-rail ESD clamp circuit is also used to provide the ESD paths between V_{DD} and V_{SS}.

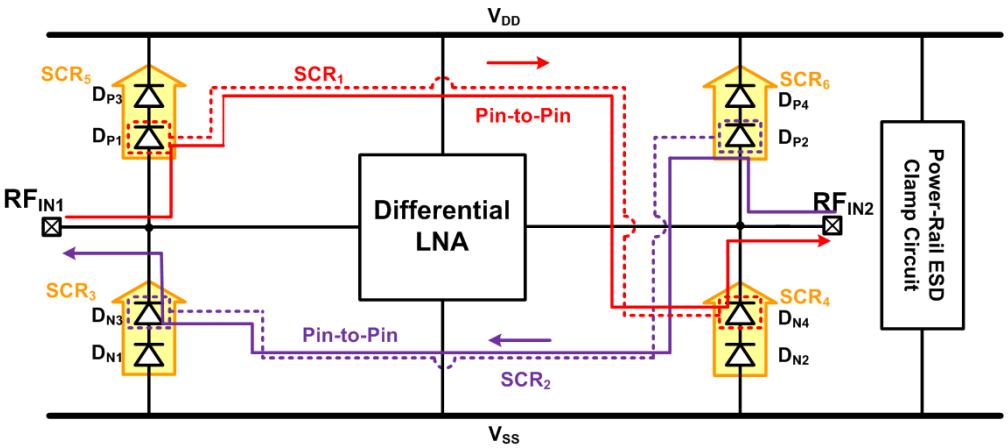


Fig. 4.3. Proposed ESD protection design.

Similar to the ESD protection design with stacked diodes in Fig. 4.2(b), 8 diodes are used in the proposed design. Without adding extra device, the proposed design combines P+/N-well diodes (D_{P1}, D_{P2}, D_{N1}, and D_{N2}) and P-well/N+ diodes (D_{P3}, D_{P4}, D_{N3}, and D_{N4}) to form the embedded P+/N-well/P-well/N+ SCR paths (SCR_3, SCR_4, SCR_5, and SCR_6) by using layout skill.

Besides, by putting D_{P1} and D_{N4} (D_{P2} and D_{N3}) together in layout, another embedded SCR_1 (SCR_2) exists. To implement this design, the layout top view and the device cross-sectional view of the proposed ESD protection design are shown in Figs. 4.4 and Figs. 4.5. The ESD current paths along (1)-(1') direction include D_{P3}, D_{P1}, D_{N4}, D_{N2}, and the parasitic stacked diodes from RF_{IN1} to RF_{IN2}. The ESD current paths along (2)-(2') direction include SCR_5, SCR_1, and SCR_4. Similarly, the ESD current paths along (3)-(3') direction include D_{N1}, D_{N3}, D_{P2}, D_{P4}, and the parasitic stacked diodes from RF_{IN2} to RF_{IN1}, and those along (4)-(4') direction include SCR_3, SCR_2, and SCR_6.

The width of diode path (T) is equal to twice the width of t in Fig. 4.4, and the width of SCR path (W) is the sum of all segments of w_1 and w_2. In the beginning of ESD stress, the diode paths will turn on to discharge the initial currents, and then the SCR paths will take over to discharge the primary currents. The diode path also plays the role of trigger circuit of SCR device to enhance its turn-on speed [9], [17] . Since the primary ESD currents are designed to be discharged through the SCR paths, the distance from anode to cathode of SCR (D) is wished to be minimized. The turn-on resistance of SCR can be lowered by using this layout style.

As positive-to-V_{DD}-mode (PD-mode) ESD stress on RF_{IN1} pad, ESD current will be discharged by the forward-biased stacked diodes (D_{P1} and D_{P3}) with embedded SCR_5. During positive-to-V_{SS}-mode (PS-mode) ESD stress on RF_{IN1} pad, ESD current will be discharged through the D_{P1} and D_{P3} with embedded SCR_5 and the power-rail ESD clamp circuit. As negative-to-V_{SS}-mode (NS-mode) ESD stress on RF_{IN1} pad, ESD current will be discharged

by the D_{N1} and D_{N3} with embedded SCR_3. During negative-to-V_{DD}-mode (ND-mode) ESD stress on RF_{IN1} pad, ESD current will be discharged through the power-rail ESD clamp circuit and the D_{N1} and D_{N3} with embedded SCR_3. As pin-to-pin ESD stress from RF_{IN1} to RF_{IN2}, the ESD current can be discharged by the parasitic stacked diodes with embedded SCR_1. During pin-to-pin ESD stress from RF_{IN2} to RF_{IN1}, the ESD current can be discharged by the other parasitic stacked diodes with embedded SCR_2. As the Fig. 4.3 shown, the voltage drop across the ESD current path of LNAs with ESD protection can be calculated as

$$V_{ESD,Proposed\ Design} = V_{SCR_1}\ or\ V_{SCR_2} \tag{4.4}$$

Comparing with the conventional ESD protection designs, the proposed ESD protection design provides the whole chip ESD protection for all ESD-test pin combinations with lowest clamping voltage without extra trigger circuit. Therefore, the proposed ESD protection design is expected to have better ESD robustness.

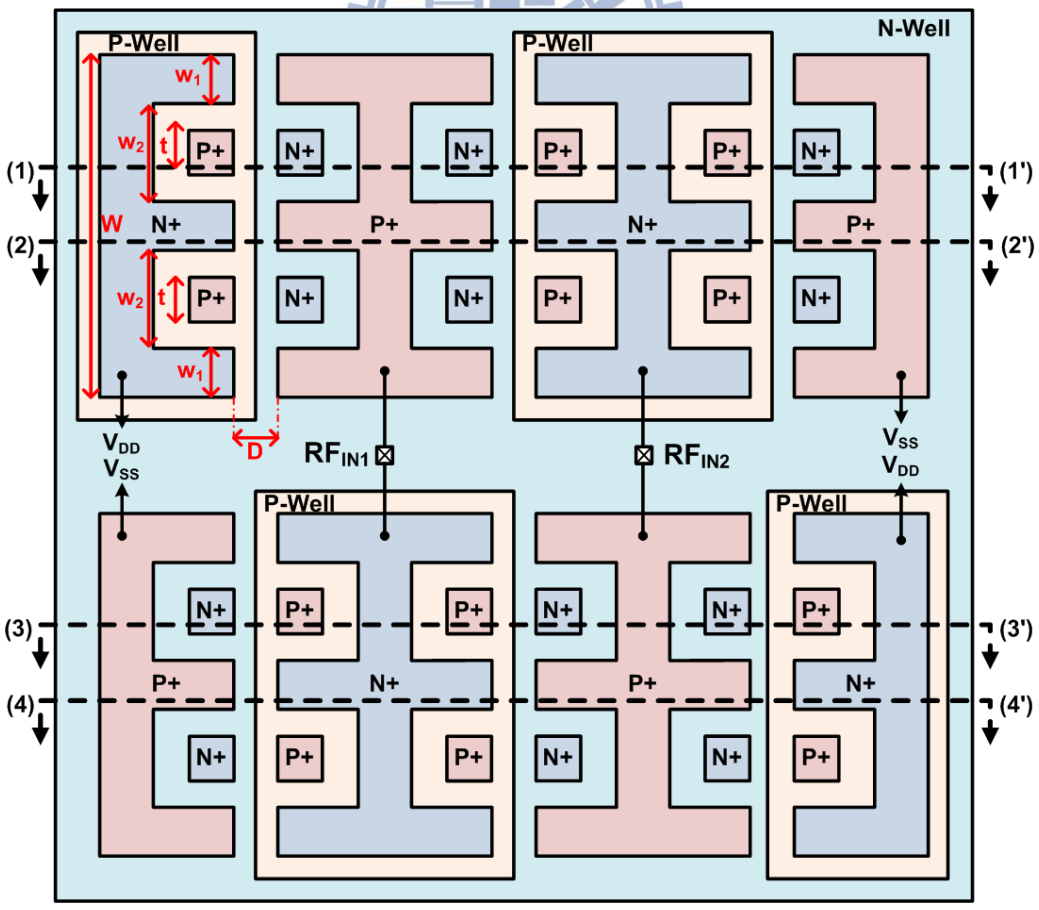
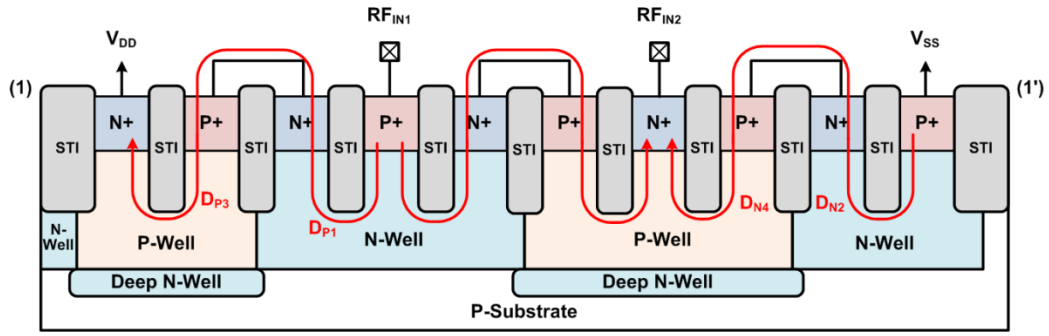
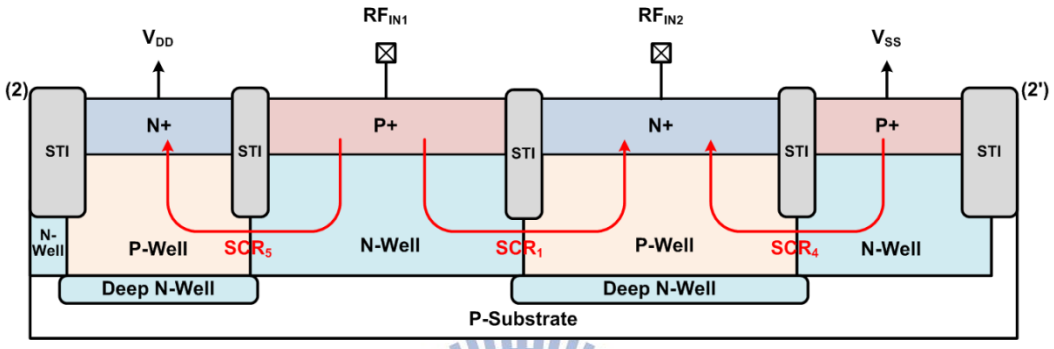


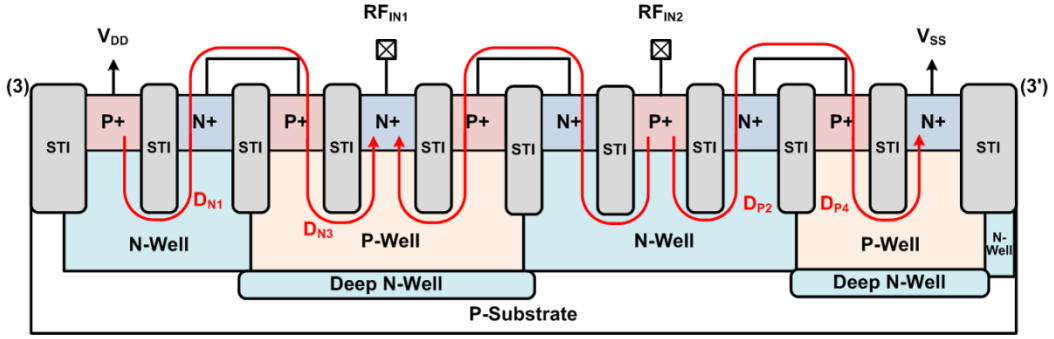
Fig. 4.4. Layout top view of proposed ESD protection design.



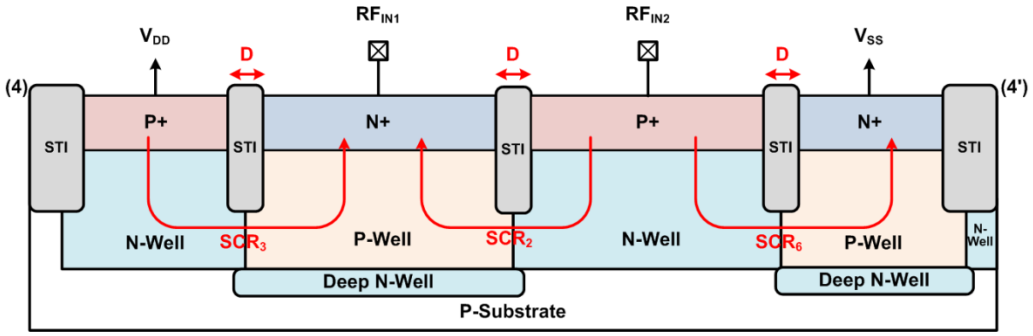
(a)



(b)



(c)



(d)

Fig. 4.5. Cross-sectional view of proposed ESD protection design along (a) (1)-(1'), (b) (2)-(2'), (c) (3)-(3'), and (d) (4)-(4').

4.3 Experimental Results

4.3.1 Test Circuits

To verify the proposed design in silicon chip, a 65-nm CMOS process is used in this work. The width of SCR path (W) is selected to be 40μm, which is estimated to pass 2-kV HBM ESD tests. The widths of diode path (T) of are selected to be W/2, W/4, or W/8. The distance from anode to cathode of SCR (D) is 0.32μm. For comparison purpose, the ESD protection designs with dual diodes and stacked diodes are also implemented in the same 65-nm CMOS process. In each test circuit, the dimensions of diodes and power-rail ESD protection circuits are all identical. The effective circuit of power-rail ESD protection circuit is shown in Fig.4.6. All these dimensions of test circuits are listed in Table I. These test circuits have been fabricated in a 65-nm salicided CMOS process without using the silicide-blocking mask. These test circuits are arranged with ground-signal-ground-signal-ground (G-S-G-S-G) style in layout to facilitate the on-wafer RF measurement. The chip photo of test circuits is shown in Fig. 4.7.

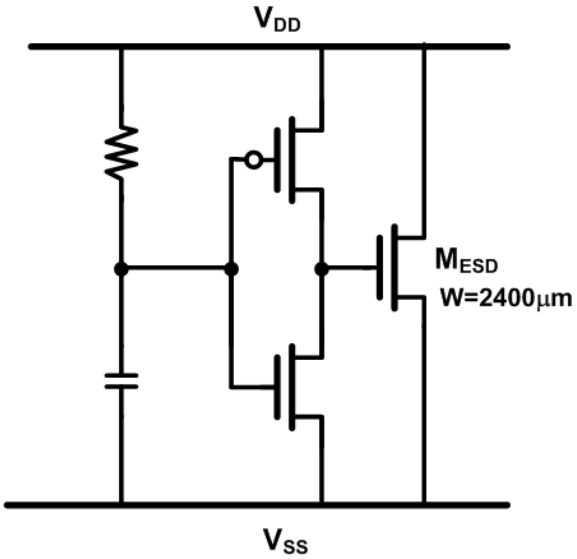


Fig. 4.6. The equivalent circuit of power-rail ESD protection circuit.

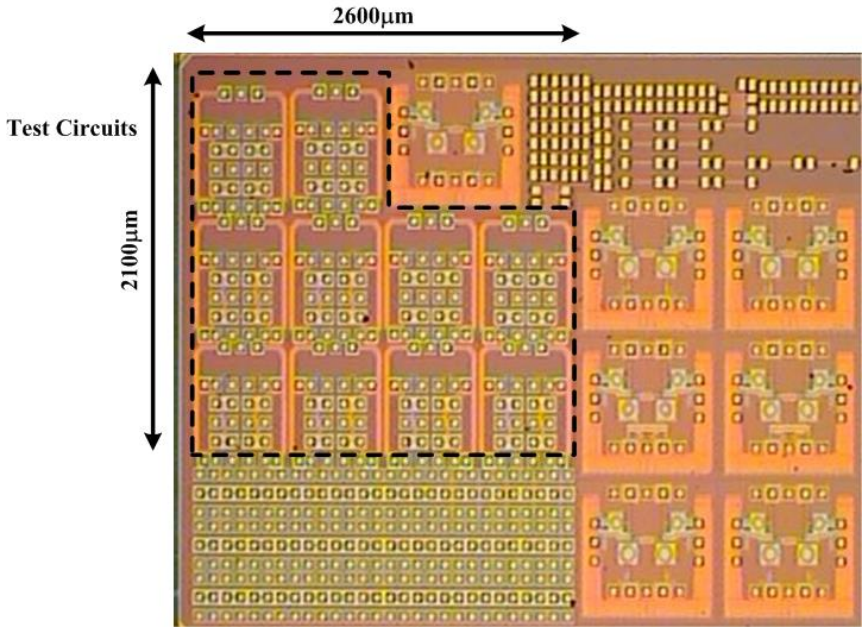


Fig. 4.7. The chip photograph of test circuits.

4.3.2 Measured Parasitic Capacitance

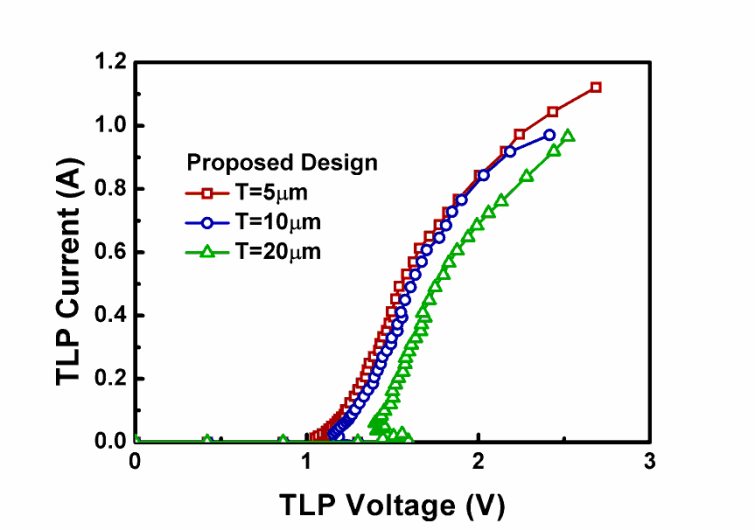
With the on-wafer measurement, the two-port S-parameters of the test devices were measured by using the vector network analyzer. The source and load resistances to the test devices are kept at 50 Ω. In order to extract the intrinsic characteristics of the test devices in high frequencies, the parasitic effects of the G-S-G-S-G pads have been removed by using the de-embedding technique [20]. The parasitic capacitance of each test device can be extracted from the S-parameters.

The intrinsic parasitic capacitance of the proposed design seen at RF_{IN1} or RF_{IN2} is about 120 fF at 24 GHz, as listed in Table I. With the narrower T, which is identical to the narrowed w_2 and the widened w_1, the parasitic capacitances are slightly increased. The parasitic capacitances of the dual diodes and stacked diodes are 122.9 fF and 83.4 fF, respectively. The parasitic capacitance of the proposed design is lower than 200 fF, and the proposed ESD protection design is expected to have much better ESD robustness.

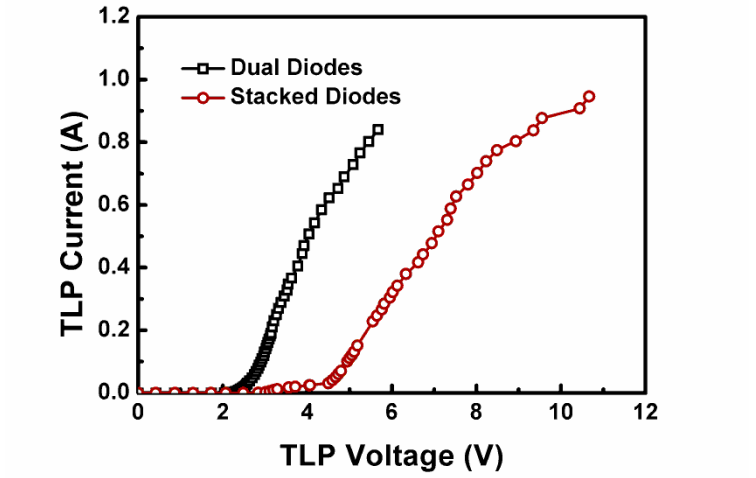
4.3.3 Measured ESD Robustness

To investigate the turn-on behavior and the I-V curve in high-current region of the ESD protection circuit, the transmission-line-pulsing (TLP) system with 10-ns rise time and 100-ns pulse width is used [21]. The TLP-measured I-V characteristics of the ESD protection circuit under pin-to-pin stress are shown in Fig. 4.8. The trigger voltages (V_{t1}) of the proposed designs are 1.3~1.6 V, while those of the dual diodes and stacked diodes are 2.0 V and 2.8 V, respectively. The holding voltage (V_{hold}) of the proposed designs are 1.1~1.4 V, while those of the dual diodes and stacked diodes are 2.4 V and 4.5 V, respectively. Besides, the current compression point (I_{CP}), which is defined as the current level deviates from the linearly extrapolated low-current curve by 20% [22], of the test circuits are also measured. The ICP of the proposed designs are 1.0~1.1 A, while those of the dual diodes and stacked diodes are 0.8 A and 0.9 A, respectively. All TLP-measured I-V characteristics are listed in Table I. The proposed ESD protection design with lower V_{t1}, lower V_{hold}, and higher I_{CP} is more suitable for ESD protection. Moreover, the proposed ESD protection design has the lower clamping voltage which can provide effective ESD protection on the gigahertz differential LNA.

The HBM ESD robustness of the test circuits have been evaluated by the ESD tester. The HBM ESD pulses are stressed to each test circuit under PD, PS, ND, NS, and pin-to-pin ESD stress conditions. The failure criterion is defined as the I-V curve seen between test pads shifting over 30% from its original curve after ESD stressed at every ESD test level. All these measured ESD robustness are listed in Table I. According to the measurement results, the proposed design with W=40μm and T=5μm can pass 2.75kV pin-to-pin HBM ESD test, while the dual diodes and stacked diodes with the same W=40μm can only pass 1.75kV pin-to-pin HBM ESD test.



(a)



(b)

Fig. 4.8. TLP I-V curves of (a) proposed design and (b) conventional designs, under pin-to-pin stress

Table I
Design Parameters and Measurement Results of Test Circuits

Structure	W (μm)	T (μm)	D (μm)	C @ 24 GHz (fF)	PD HBM (kV)	PS HBM (kV)	ND HBM (kV)	NS HBM (kV)	Pin-to-Pin HBM (kV)	Pin-to-Pin TLP V_{t1} (V)	Pin-to-Pin TLP V_{hoid} (V)	Pin-to-Pin TLP I_{CP} (A)
Proposed Design	40	5	0.32	121.5	3	3	3	3	2.75	1.3	1.1	1.1
		10		120.6	2.5	2.75	2.5	2.5	2.5	1.3	1.2	1.0
		20		113.6	2.25	2.25	2.25	2.25	2	1.6	1.4	1.0
Dual Diodes	40	N/A	N/A	122.9	2	2	2	2	1.75	2.0	2.4	0.8
Stacked Diodes	40	N/A	N/A	83.4	2.5	2	2	2	1.75	2.8	4.5	0.9

4.4 Summary

The proposed ESD protection stacked diodes with embedded SCR has been developed for the gigahertz differential LNA. Without adding extra device, this design also includes the trigger circuit of SCR to enhance the turn-on speed. The I_{CP} of the proposed designs are 1.0~1.1 A, while those of the dual diodes and stacked diodes are 0.8 A and 0.9 A, respectively. The proposed ESD protection design has been verified in a 65-nm CMOS process with low parasitic capacitance, low clamping voltage, and high ESD robustness by TLP tests. The HBM ESD robustness of the test circuits have been evaluated by the ESD tester. According to the measurement results, the proposed design with W=40μm and T=5μm can pass 2.75kV pin-to-pin HBM ESD test, while the dual diodes and stacked diodes with the same W=40μm can only pass 1.75kV pin-to-pin HBM ESD test.

Chapter 5

Application of Novel ESD Protection Design to 24-GHz Differential LNA

5.1 Differential LNA

The differential LNA is designed to operate at 24 GHz with V_{DD} supply of 1.2 V. The circuit schematic of the reference LNA without ESD protection is shown in Fig. 5.1. The architecture of common-source inductive degeneration is applied to match the source impedance (50Ω) at resonance. Using the cascode configuration can achieve good isolation between the input and output. Moreover, cascode configuration reduces the Miller effect and provides good stability [31]. The dimensions of the input NMOS transistors were designed according to the compromise between noise figure and power consumption. In order to verify the intrinsic ESD protection capability of the on-chip ESD protection circuits at the input pads, the ac coupling capacitor between the input pad and the gate inductor is not realized in the test chip because the ac coupling capacitor connected to the input pad can block some ESD energy when the input pad is stressed by ESD. The off-chip bias tee is needed to combine the RF input signal and dc bias at the input node during RF performance measurement.

With the deep N-well structure, the P-well (bulk) region of each NMOS transistor can be fully isolated from the common P-substrate, so the source and bulk terminals are connected together to eliminate the body effect. All of the inductors are the on-chip spiral inductors implemented by the top metal layer. The active and passive devices are fully integrated in the silicon chip in 65-nm CMOS process.

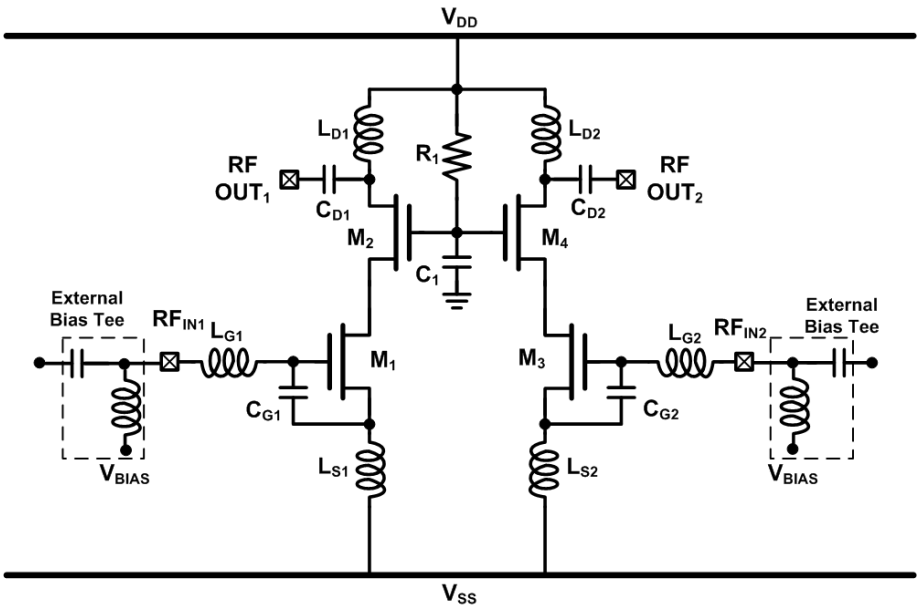


Fig. 5.1. Differential LNA without ESD protection.

The LNA with and without ESD protection circuits have been fabricated in the same 65-nm CMOS process. The proposed ESD protection design with W=40μm and T=10μm is used to protect the RF_{IN1} and RF_{IN2} pads of the differential LNA, as the Fig. 5.2 shown. For comparison purpose, the ESD protection designs with dual diodes and stacked diodes are also used to protect the RF_{IN1} and RF_{IN2} pads of the other test LNA, as the Fig. 5.3 and Fig. 5.4 shown. Fig. 5.5 shows the chip photograph of the ESD-protected LNA. The area of each LNA is 750μm x 800μm, including all pads.

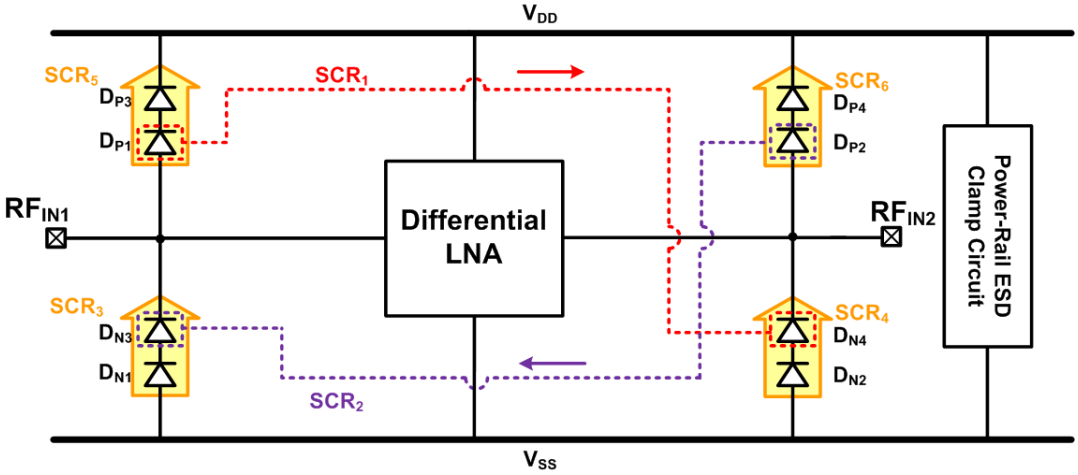


Fig. 5.2. Differential LNA with proposed ESD protection design.

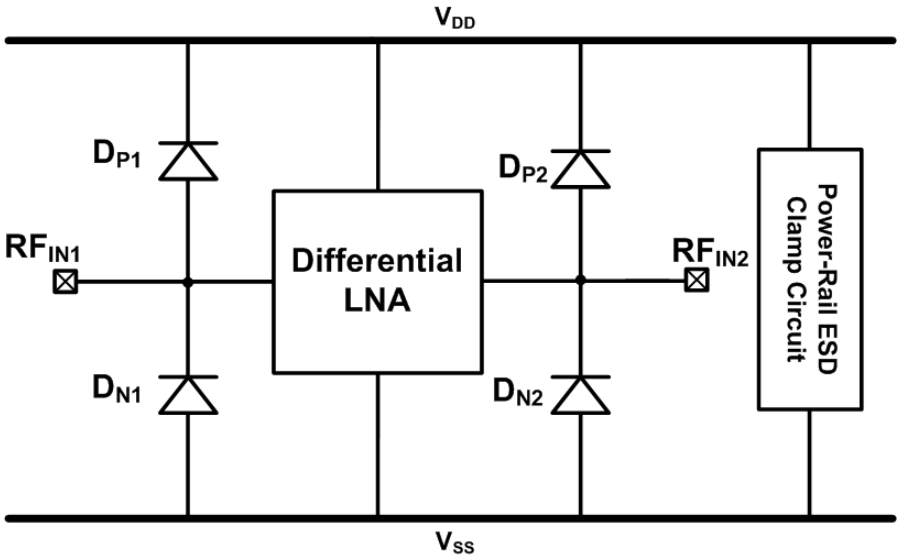


Fig. 5.3. Differential LNA with conventional ESD protection design of dual diodes.

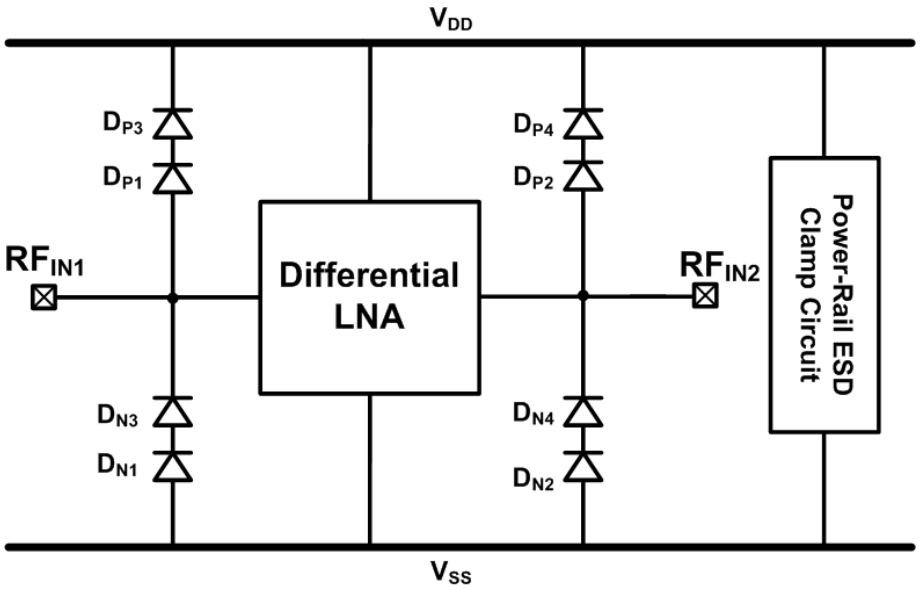


Fig. 5.4. Differential LNA with conventional ESD protection design of stacked diodes.

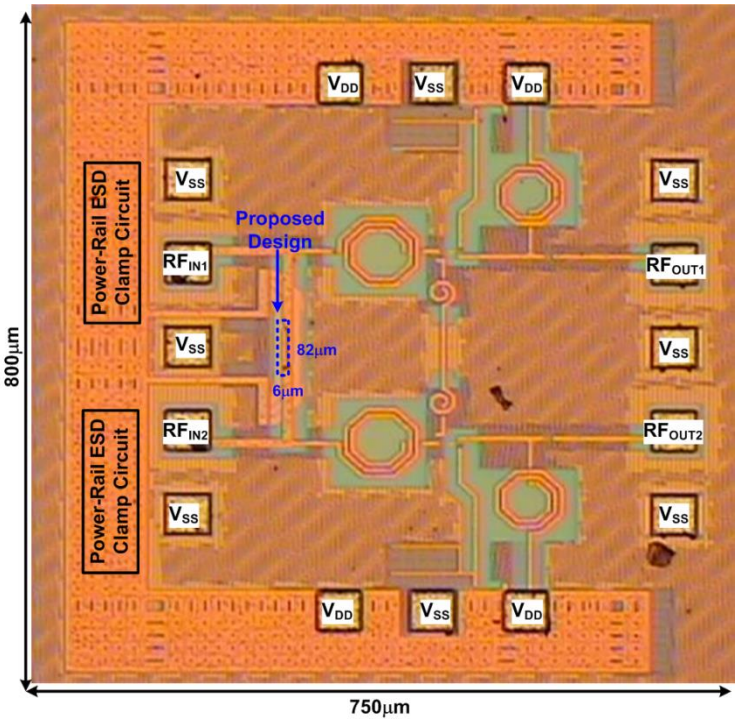


Fig. 5.5. Chip photograph of differential LNA with proposed ESD protection design.

5.2 Experimental Results

To measure the S – parameters of differential LNAs, on-wafer four-port S – parameters measurement with an Agilent E8361A network analyzer performed. The noise figures were measured by using an Agilent N8975A noise figure analyzer with an Agilent 346C noise source.

It is not easy to estimate the RF performance degradation of LNA circuit caused by ESD protection device by purely measuring the parasitic capacitance or S-parameters of ESD protection device. Therefore, full-functional RF testing is needed for ESD-protected LNA circuits to verify the effect caused by ESD protection device before being zapped by ESD stress. To verify the ESD level of ESD-protected LNA circuits, RF function failure, has been demonstrated in [32] that are more suitable and accurate for RF circuits.

RF characteristics are measured on wafer through G-S-G-S-G microwave probes. Each LNA operates with the 1.2-V V_{DD} supply and draws a total current of 18 mA. The used bias

voltage driven through the external bias tee is 0.65 V. The RF performances of all LNA are measured before and after ESD stress. The measured S_{21} parameters and noise figures (NF) of all LNA are shown in Figs. 5.6 ~5.13. The peak gain frequency of the LNA is shifted to about 21 GHz. Before ESD stress, the S_{21} at 21 GHz of LNA without ESD protection, LNA with dual diodes, LNA with stacked diodes, and LNA with proposed design are 12.3 dB, 11.3 dB, 11.1 dB, and 11.5 dB, respectively, and the NF at 21 GHz are 3.1 dB, 3.8 dB, 4.0 dB, and 4.3 dB, respectively.

To verify the ESD protection ability, the RF performances of all LNA after ESD tests are re-measured. All PD, PS, ND, NS, and pin-to-pin modes of HBM ESD stresses are performed to the LNA. The RF performances of the LNA without ESD protection are severely degraded after 500-V pin-to-pin HBM ESD tests, as shown in Figs. 5.6 and Fig. 5.7. The RF performances of the LNA with dual-diode and stacked-diode ESD protections are degraded after 2-kV and 1-kV pin-to-pin HBM ESD tests, respectively, as shown in Figs. 5.8~5.11. In contrast, the RF performances of the LNA with proposed ESD protection design are still excellent matching after 2-kV pin-to-pin HBM ESD stress, as shown in Figs. 5.12 and Fig. 5.13.

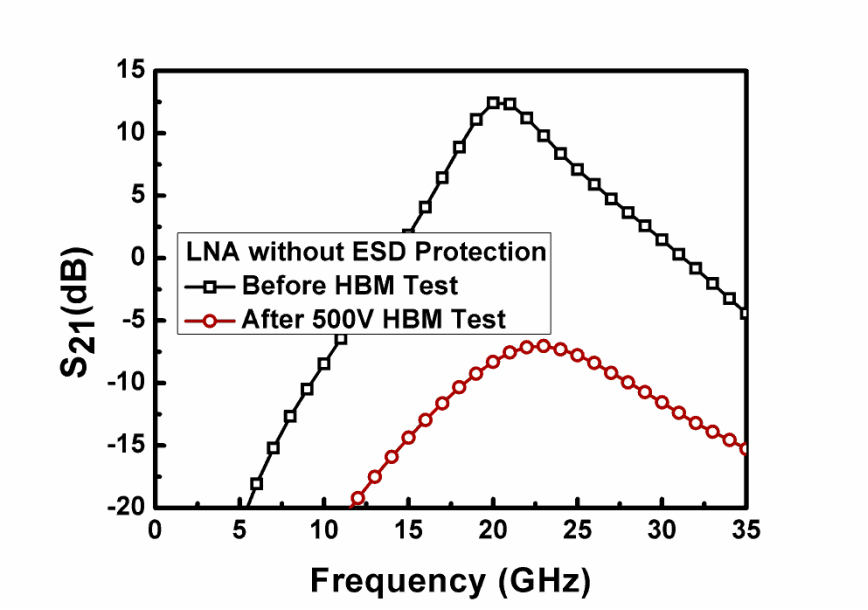


Fig. 5.6. Measured S_{21} of LNA without ESD protection.

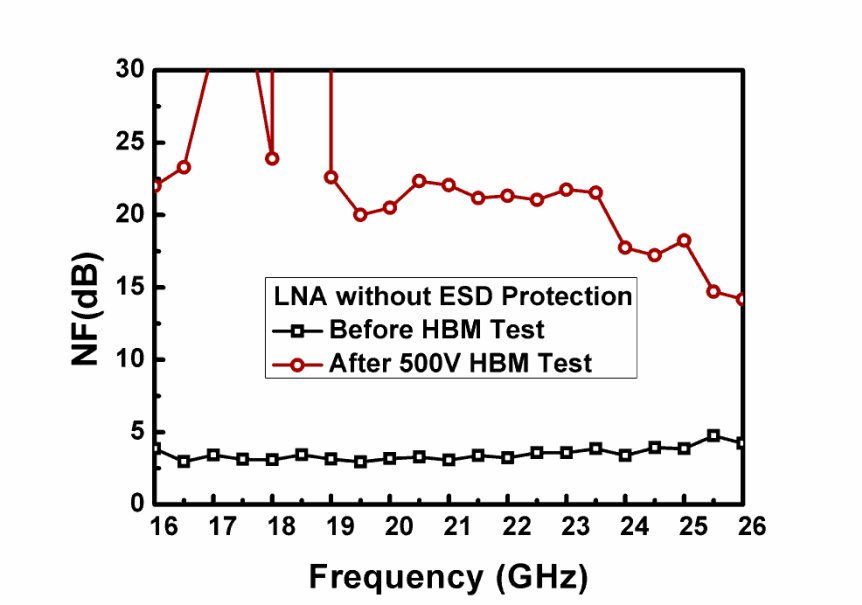


Fig. 5.7. Measured NF of LNA without ESD protection.

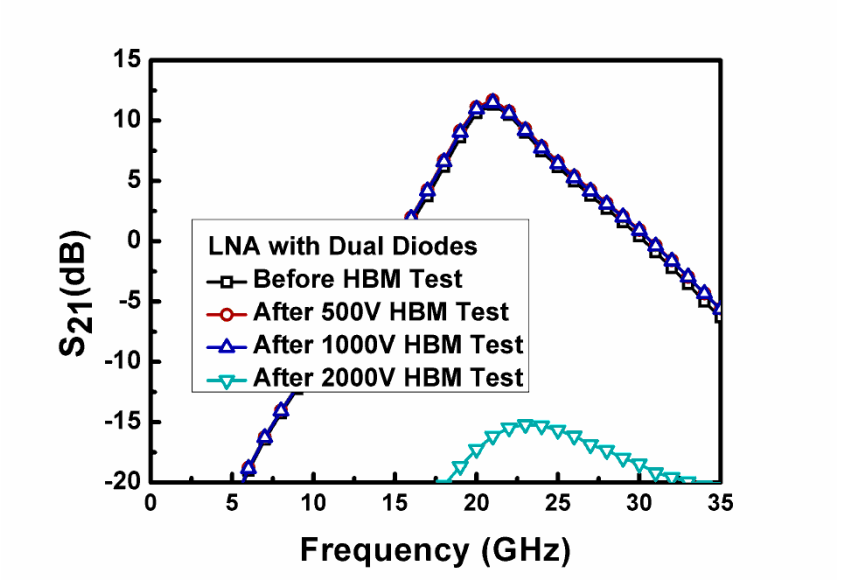


Fig. 5.8. Measured S_{21} of LNA with dual-diode ESD protection.

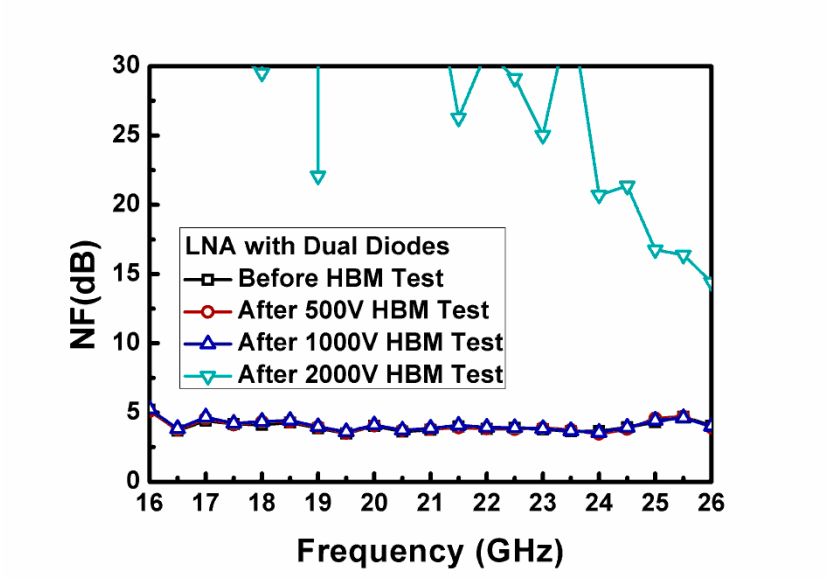


Fig. 5.9. Measured NF of LNA with dual-diode ESD protection.

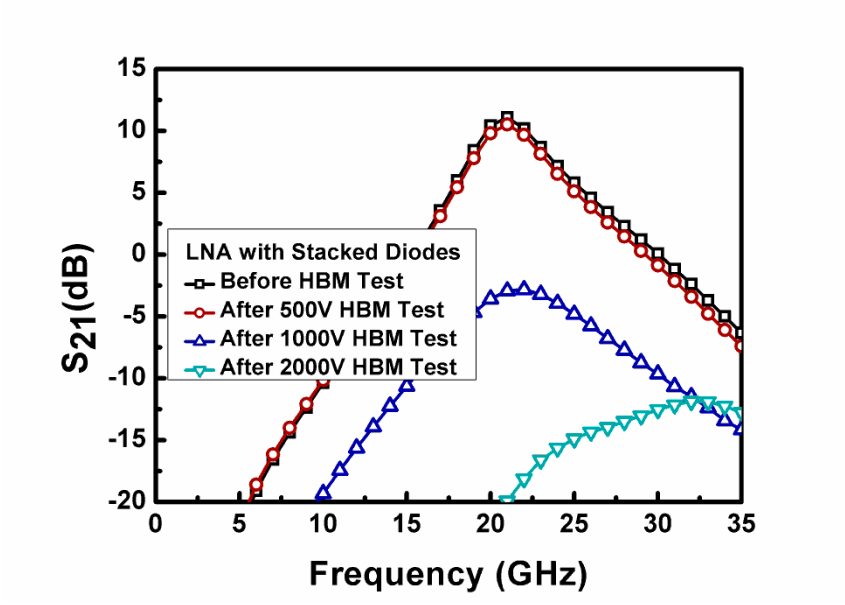


Fig. 5.10. Measured S_{21} of LNA with stacked-diode ESD protection.

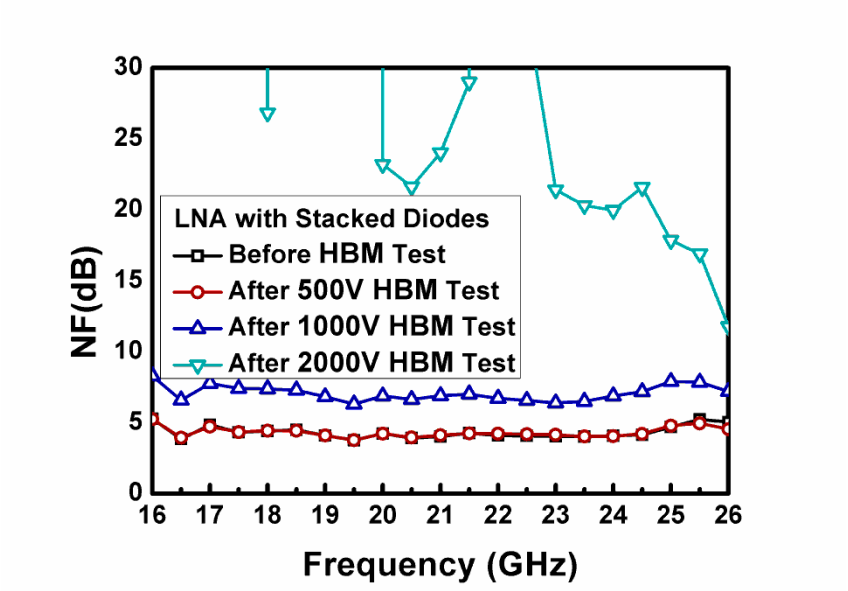


Fig. 5.11. Measured NF of LNA with stacked-diode ESD protection.

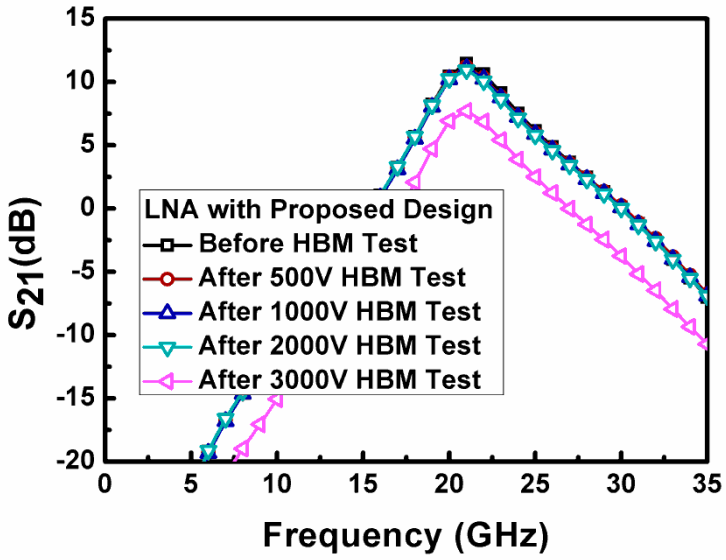


Fig. 5.12. Measured S_{21} of LNA with proposed ESD protection.

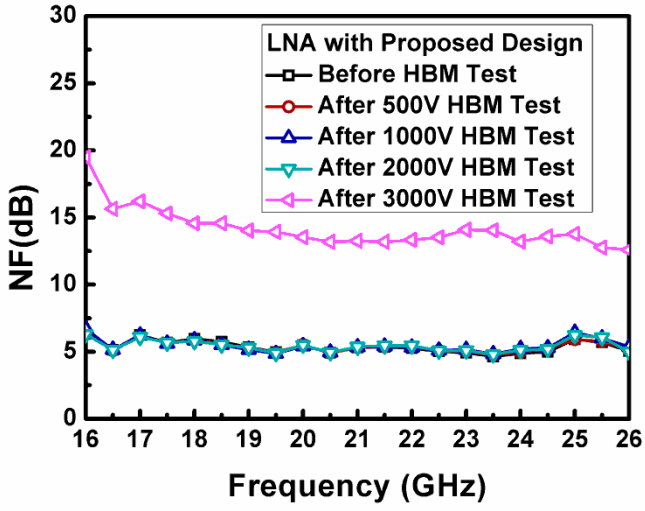


Fig. 5.13. Measured NF of LNA with proposed ESD protection.

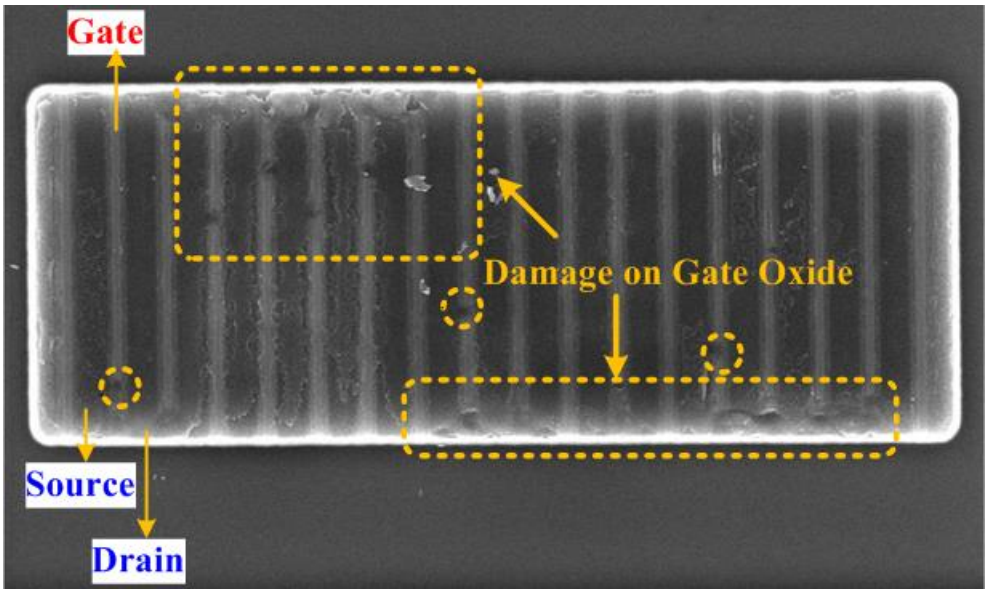
5.3 Failure Analysis

After ESD tests, the LNA with and without ESD protection circuits are analyzed. To investigate the failure mechanism, emission microscope (EMMI) and scanning electron microscope (SEM) can be utilized to find the failure location. The SEM photograph of the LNA without ESD protection after 500-V pin-to-pin HBM ESD tests is shown in Fig. 5.14. The failure points are located at the gates of M_1 and M_3. Fig. 5.15 and Fig. 5.16 show the EMMI pictures of the LNA with dual-diode and stacked-diode ESD protection after 2-kV pin-to-pin HBM ESD tests. Furthermore, the SEM photographs of the LNA with dual-diode and stacked-diode ESD protections after 2-kV pin-to-pin HBM ESD tests are shown in Figs. 5.17 and Fig. 5.18, respectively. The failure points are still located at the gates of M1 or M3. The failure mechanism indicates that the conventional ESD protection design can not effectively clamp the overshooting voltage to protect the gate oxide from damage. This failure mechanism indicates that overshooting voltage across the gate oxide causes damage because

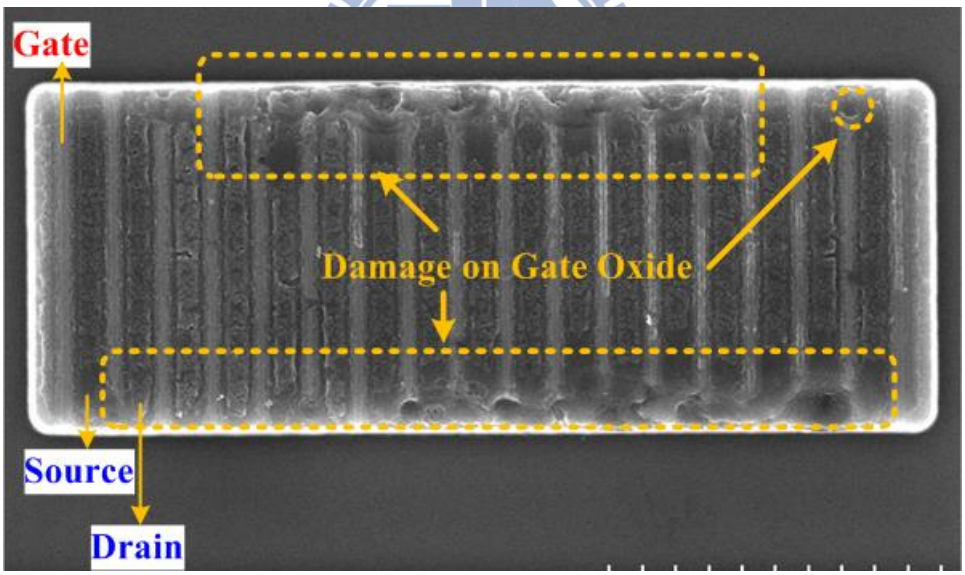
the gate- oxide breakdown voltage is decreasing as the CMOS technology is scaled down.

The SEM photographs of the LNA with proposed ESD protection design after 2-kV pin-to-pin HBM ESD tests is shown in Fig. 5.19. There is no failure found in the LNA with proposed ESD protection design after 3-kV pin-to-pin HBM ESD tests. The EMMI and SEM photographs of the LNA with proposed ESD protection design after 3-kV pin-to-pin HBM ESD test are shown in Fig. 5.20 and Fig. 5.21. After 3-kV pin-to-pin HBM ESD tests, the failure point is located at the embedded SCR_1. This failure mechanism indicates that the failed function of LNA after HBM ESD zapping is caused by the damaged proposed ESD protection design. Since the proposed ESD protection design is damaged earlier than the MOS transistor used in LNA, trigger speed and clamp voltage of the proposed ESD protection design is tolerable to the used MOS transistor when proposed ESD protection design is applied to LNA. Therefore, the proposed ESD protection design has been verified to protect the LNA from ESD damage with 2-kV HBM ESD robustness.

The ESD level of proposed protection design itself becomes crucial. If the ESD level of proposed ESD protection design can be boosted, the ESD level of ESD-protected LNA with proposed ESD protection design would further enhance. One method is to enlarge the width of proposed ESD protection design.



(a)



(b)

Fig. 5.14. SEM photo of (a) M1 and (b) M3, in LNA without ESD protection after 500-V HBM ESD tests.

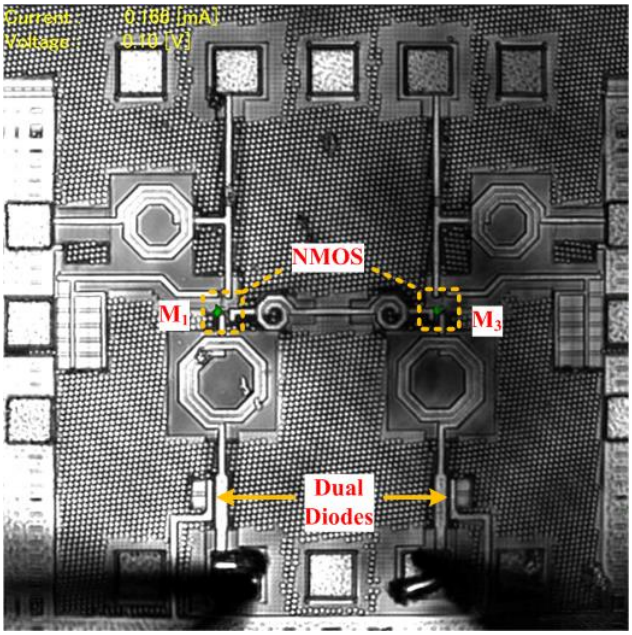


Fig. 5.15. EMMI photo of LNA with dual-diode ESD protection after 2-kV pin-to-pin HBM ESD tests.

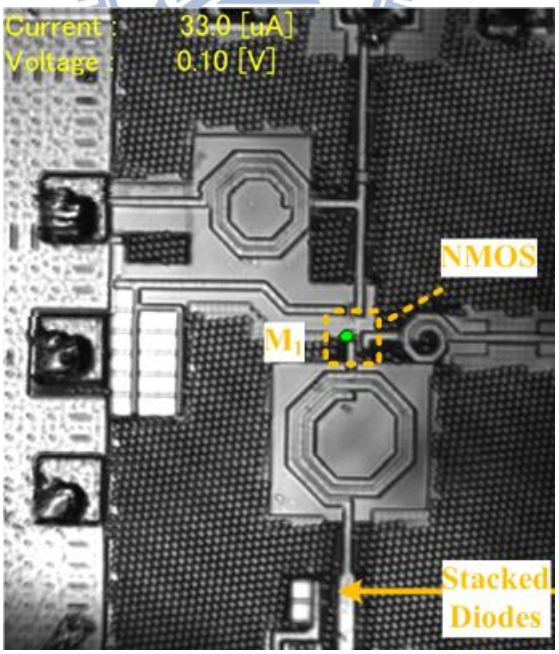


Fig. 5.16. EMMI photo LNA with stacked-diode ESD protection after 2-kV pin-to-pin HBM ESD tests.

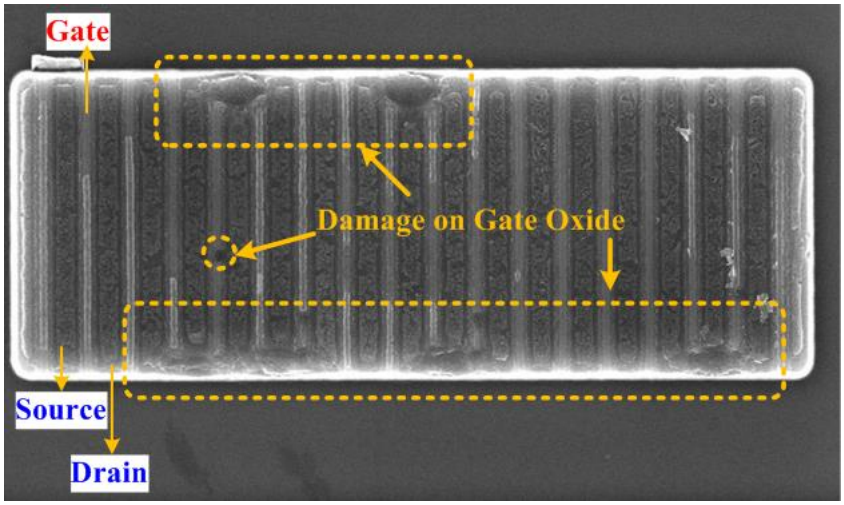


Fig. 5.17. SEM photo of M_1 in LNA with dual-diode ESD protection after 2-kV pin-to-pin HBM ESD tests.

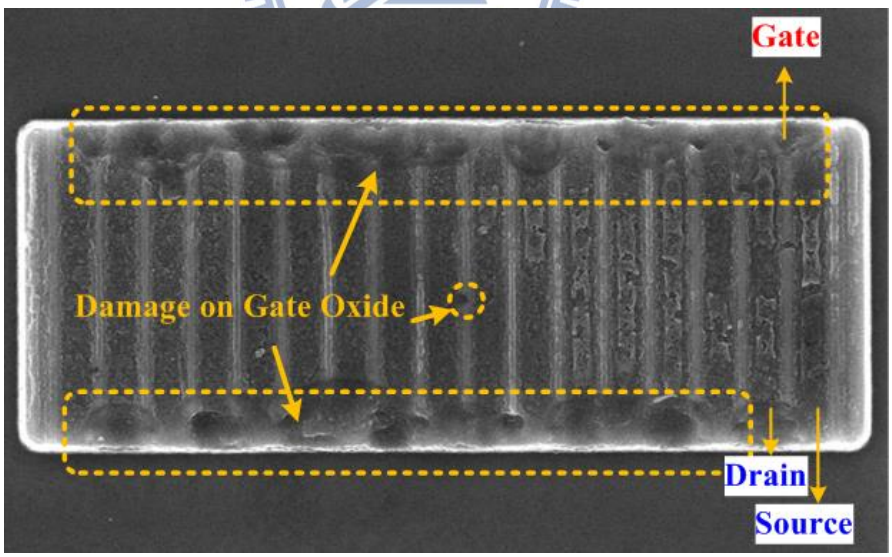


Fig. 5.18. SEM photo of M_3 in LNA with stacked-diode ESD protection after 2-kV pin-to-pin HBM ESD tests.

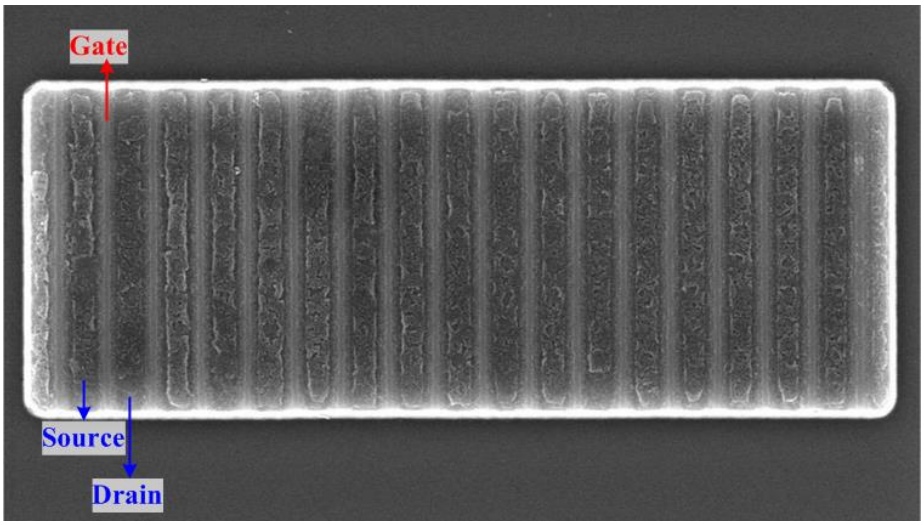


Fig. 5.19. SEM photo of M_1 in LNA with proposed ESD protection after 3-kV pin-to-pin HBM ESD tests.

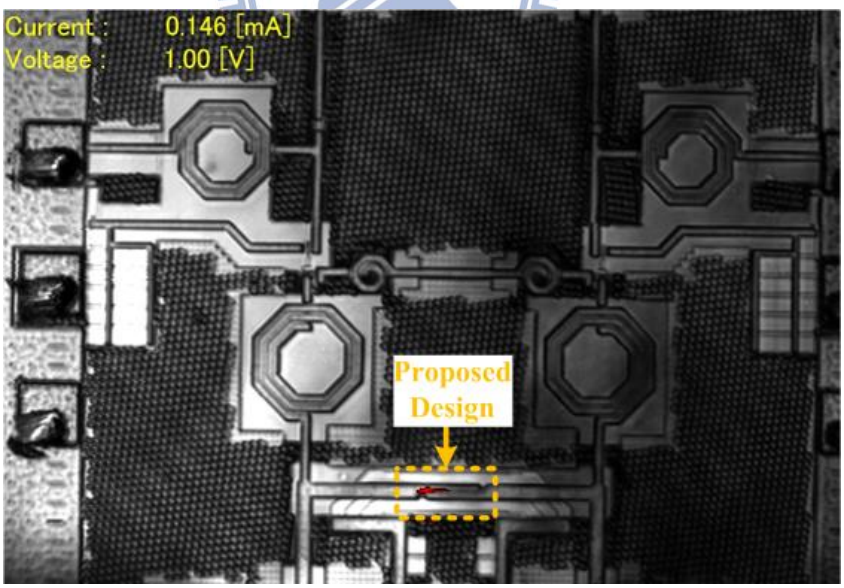


Fig. 5.20. EMMI photo of LNA with proposed ESD protection after 3-kV pin-to-pin HBM ESD tests.

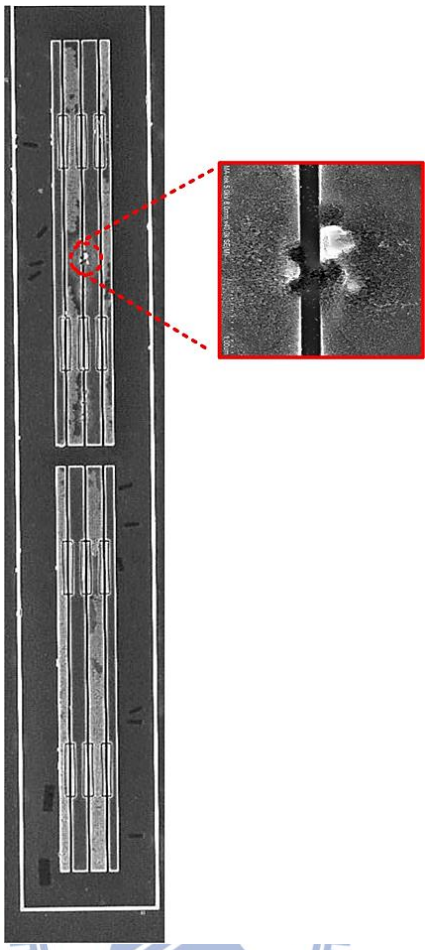


Fig. 5.21. SEM photo of proposed ESD protection design after 3-kV pin-to-pin HBM ESD tests.

5.4 Summary

The proposed ESD protection design with W=40μm, T=10μm, 120.6-fF parasitic capacitance, and 2.5-kV HBM ESD robustness has been applied to a differential LNA. According to the measurement results, the RF performance of the LNA with dual-diode and with stacked-diode ESD protections are degraded after 2-kV and 1-kV pin-to-pin HBM ESD tests, respectively. The RF performances of the LNA with proposed ESD protection design are still excellent matching after 2-kV pin-to-pin HBM ESD stress.

The failure mechanism indicates that the failed function of LNA after HBM ESD zapping is caused by the damaged proposed ESD protection design. The trigger speed and clamp voltage of the proposed ESD protection design is tolerable to the used MOS transistor because the proposed ESD protection design is damaged earlier than the MOS transistor. The failure analyze results verify the RF performances and confirm the ESD protection ability of the proposed ESD protection design. The experimental results reveal the truth that the proposed ESD protection circuit indeed done its work with 2-kV HBM ESD robustness.

Chapter 6

Conclusions and Future Works

6.1 Conclusions

In this thesis, the issues of RF ESD protection design have been presented. The parasitic effects of ESD protection devices may cause signal loss, change input matching conditions, and induce other undesired RF performance degradation. Designing RF ESD protection devices or circuits with good ESD level and less influence on RF performance is quite a challenge. The novel RF ESD protection device and circuit design have been proposed to advance this goal.

The novel ESD protection design of stacked diodes has been designed, fabricated, and characterized in a 65-nm CMOS process. The new proposed ESD protection device utilizes stacked diodes embedded silicon-controlled rectifier (SDSCR) as main ESD-current-discharging paths. According to the measurement results, the novel stacked diodes type A40 with W=40μm and T=5μm has the best ratio of 75.4, while the P stacked diodes and N stacked diodes with the same width has only 51.9 and 41.3, respectively. Therefore, the optimization on layout style of stacked diodes is more suitable for on-chip ESD protection due to its low turn-on resistance, low parasitic capacitance, and high ESD robustness. This layout style can be further extended to the stacked diodes with more diodes.

The proposed ESD protection stacked diodes with embedded SCR has been developed for the gigahertz differential LNA. Without adding extra device, the proposed circuit design combines P+/N-well diodes and P-well/N+ diodes to form the embedded P+/N-well/P-well/N+ SCR paths by using layout skill, and this design also includes the trigger circuit of SCR to enhance the turn-on speed. The I_{CP} of the proposed designs are

1.0~1.1 A, while those of the dual diodes and stacked diodes are 0.8 A and 0.9 A, respectively. The proposed ESD protection design has been verified in a 65-nm CMOS process with low parasitic capacitance, low clamping voltage, and high ESD robustness by TLP tests. The HBM ESD robustness of the test circuits have been evaluated by the ESD tester. The HBM ESD pulses are stressed to each test circuit under PD, PS, ND, NS, and pin-to-pin ESD stress conditions. According to the measurement results, the proposed design with W=40μm and T=5μm can pass 2.75kV pin-to-pin HBM ESD test, while the dual diodes and stacked diodes with the same W=40μm can only pass 1.75kV pin-to-pin HBM ESD test.

Moreover, the proposed ESD protection design with W=40μm, T=10μm, 120.6-fF parasitic capacitance, and 2.5-kV HBM ESD robustness has been successfully applied to a differential LNA. Among the measurement results, the RF performance of the LNA with dual-diode and with stacked-diode ESD protections are degraded after 2-kV and 1-kV pin-to-pin HBM ESD tests, respectively. In contrast, the RF performances of the LNA with proposed ESD protection design are still excellent matching after 2-kV pin-to-pin HBM ESD stress.

The failure mechanism indicates that the failed function of LNA after HBM ESD zapping is caused by the damaged proposed ESD protection design. The proposed ESD protection design with high trigger speed and low clamp voltage is suitable for differential LNA in nanoscale CMOS process. The proposed ESD protection design has been verified to protect the LNA from ESD damage with 2-kV HBM ESD robustness.

6.2 Future Works

The RF circuits realized in CMOS technologies are susceptible to ESD events that may damage the IC products. The ESD protection design for power amplifier (PA) has been reported in [33]. In this thesis, the ESD protection design for LNA has been discussed. The transmit/receive (T/R) switch in the RF front-end circuit, as shown in Fig. 1, may also be stressed by ESD. As yet little is known about the ESD protection design for the T/R switch. Thus, ESD protection design for T/R switch in RF circuits can be further studied in the future.

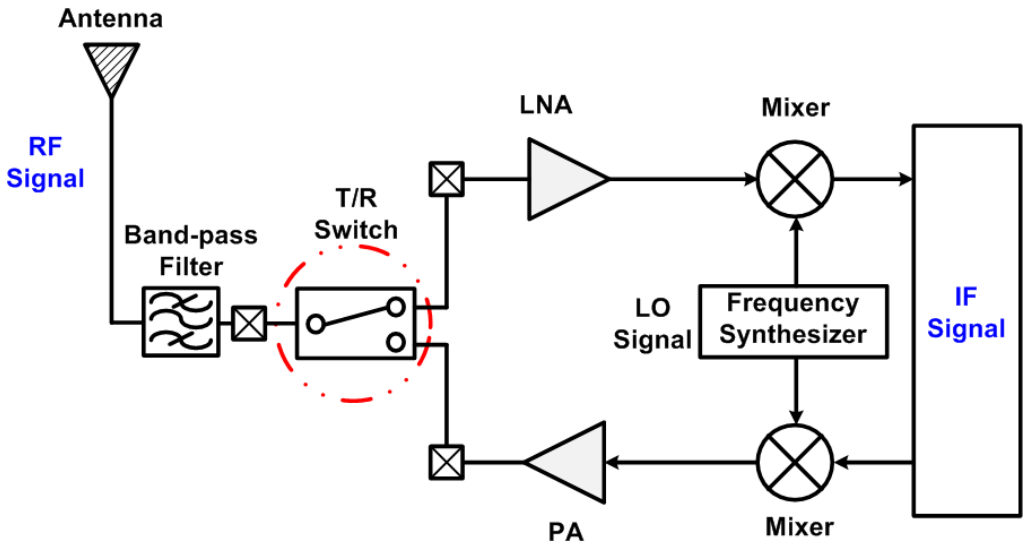


Fig. 6.1. Schematic diagram of T/R switch in RF front-end circuit.

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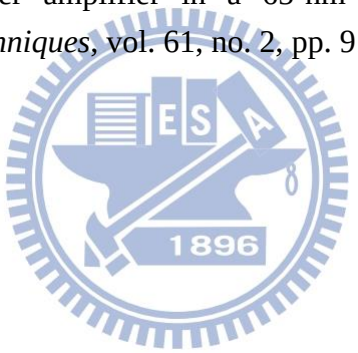

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[1] C.-Y. Lin and **M.-L. Fan**, "Optimization on Layout Style of Diode Stackup for On-Chip ESD Protection," revised to *IEEE Transactions on Device and Materials Reliability*.

[2] C.-Y. Lin and **M.-L. Fan**, "Design of ESD Protection Diodes with Embedded SCR for Differential LNA in a 65-nm CMOS Process," submitted to *IEEE Transactions on Microwave Theory and Techniques*.

(B) International Conference Papers:

[1] C.-Y. Lin, **M.-L. Fan**, M.-D. Ker, L.-W. Chu, J.-C. Tseng, and M.-H. Song, "Improving ESD Robustness of Stacked Diodes with Embedded SCR for RF Applications in 65-nm CMOS," accepted by 2014 *IEEE International Reliability Physics Symposium*.