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博士論文

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ESD Protection Design with TVS (Transient Voltage Suppressor) to Meet System-Level ESD Specifications

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摘要

對於電子產品的可靠度與安全性考量，系統層級靜電放電(electrostatic discharge, ESD)防護設計是絕對必要的。為了承受 IEC 61000-4-2 的接觸或空氣放電能量，電子產品必須在靠近輸出入介面端做靜電放電防護設計。此外，在輸出入端子直接針腳注入(direct pin injection)靜電放電測試已被用來模擬電纜放電(cable discharged event, CDE)對積體電路造成的傷害。同樣是模擬人體帶靜電放電，由於等效電路中的電容與電阻差異，IEC61000-4-2 系統層級靜電放電模型的最大電流比相同測試電壓下之人體放電模式(human-body-model, HBM)的最大電流大了約 5 倍。在測試規範上，基本的 IEC61000-4-2 測試規格是± 8 kV，而基本的 HBM 測試規格是 2 kV，因此要達到基本測試規格，IEC61000-4-2 系統層級靜電放電模型的最大電流比 HBM 的最大電流大了約 20 倍。在積體電路中通常必須設計 HBM 靜電放電防護電路，而針對 IEC61000-4-2 防護，則必須考慮整合在積體電路晶片中或是使用外加的瞬態電壓抑制器(transient voltage suppressor, TVS)來保護系統。

對於系統設計者來說，積體電路晶片中整合系統層級靜電放電防護是有益的。他們不需要再去考慮額外添加 TVS 元件的規格，也不需考慮如何針對靜電放電防護設計印刷電路板的佈局，可以節省系統開發時間，並且對於可攜式電子產品需要縮小印刷電路板的尺寸有所幫助。本論文第二章提出了一個嶄新的 TVS 元件整合在矽基底的 RS232 收發器 IC 之中做 IEC61000-4-2 系統層級靜電放電防護，並且於 0.8 微米 Bipolar CMOS DMOS (BCD)製程中實現並驗證。此防護元件結構為一有高導通電壓(holding voltage, V_h)與導通電流(holding current, I_h)之高壓雙向矽控整流器(Dual Silicon-Controlled-Rectifier, DSCR)。此整合晶片上 TVS 元件的 RS232 收發器 IC 可通過±12 kV IEC61000-4-2 接觸放電測試，並沒有造成任何硬體損壞與電性閂鎖(latch-up)的問題。此外，將此整合晶片上 TVS 元件的 RS232 收發器 IC 應用於筆記型電腦系統上時，可通過±20 kV IEC61000-4-2 接觸放電測試(class B)。

在先進 CMOS 製程或是絕緣層上矽(silicon-on-insulator, SOI)製程中，由於單位面積的靜電放電防護耐受度非常差，若要整合系統層級靜電放電防護於晶片上，需要的矽面積將會非常的大，並不符合成本考量。本論文第三章提出一使用 TVS 晶片與控制器區域網路(controller area network, CAN)收發器整合在單一封裝之設計方法，此設計方法並於高壓 SOI 製程製作 CAN 收發器晶片以及 0.8 微米雙極性電晶體(bipolar)製程製作 TVS 晶片上驗證。本章節並提出計算封裝上接合導線寄生電感的方式，來設計 TVS 元件之箝制電壓(clamping voltage)。此 TVS 晶片與 CAN 收發器晶片共同封裝設計可通過±15 kV IEC61000-4-2 接觸放電測試，並沒有造成任何硬體損壞與電性閂鎖的問題。

為了進一步去除封裝上接合導線寄生電感所造成靜電放電防護能力下降的

問題，本論文第四章提出於三維基體電路(three-dimension integrated circuit, 3D IC)中整合 TVS 晶片與功能晶片之設計方案。此共同封裝設計於三維基體電路之 TVS 晶片與功能晶片可使用不同的製程技術製作來降低製造成本。此外，功能晶片亦可不需設計人體放電模式與機器放電模式(machine-model, MM)之靜電放電防護，而透過共同封裝設計於三維基體電路之 TVS 晶片來做防護，進一步降低成本。

隨著積體電路製程的持續微縮，在現今奈米製程中，晶片之靜電放電防護設計已成為一大挑戰。目前業界已有提出降低靜電放電防護目標規格的建議。然而，降低靜電放電防護目標規格的晶片產品在自動化測試時，若是環境靜電荷控制沒有跟著改善，晶片容易遭受測試機台或是晶片本身所帶之靜電放電轟擊造成損毀。本論文第五章提出一嶄新的測試方法與測試元件，來消除晶片產品在自動化測試時的靜電放電轟擊。此測試方法與測試元件可在不需修改測試機台下避免待測晶片遭受靜電放電損毀。

第六章總結本論文的研究成果，並提出數個接續本論文研究方向的研究題目。本論文所提出的數個針對系統層級之靜電放電防護之新穎設計，已有實驗晶片量測結果以驗證設計之理論，並已發表於國際期刊論文以及提出專利申請。

ESD Protection Design with TVS (Transient Voltage Suppressor) to Meet System-Level ESD Specifications

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Abstract

For reliability and safety concern, system-level electrostatic discharge (ESD) protection to electronic devices is absolutely necessary. The electronic devices must have the ESD protection design nearby the I/O interfaces to against IEC61000-4-2 contact (or air) discharge stress. Moreover, direct pin injection of ESD stress at I/O ports had been used to emulate the cable discharged event (CDE) for the interface integrated circuits (ICs). Due to the difference of capacitor and resistor in the equivalent circuit, the maximum current of system-level ESD in IEC-61000-4-2 is 5 times higher than that of human-body-model (HBM) at the same zapping voltage. The basic specification of IEC-61000-4-2 is ± 8 kV, where the maximum current is around 20 times higher than that of the basic 2 kV HBM specification. In general, on-chip ESD protection design to sustain HBM stress is necessary for the integrated circuit. For the IEC6100-4-2 system-level ESD protection, on-chip ESD protection devices or additional off-chip transient voltage suppressor (TVS) devices are the necessary for

the sufficient protection capability.

The system-level ESD protection by on-chip TVS device embedded in the functional IC has benefits for the system designers. They do not have to take care of the TVS device specification and the PCB layout for ESD protection, which can save developing time and valuable for portable devices with small PCB size. In Chapter 2, a novel on-chip TVS integrated with the silicon-based transceiver IC has been proposed and verified in a 0.8-μm Bipolar CMOS DMOS (BCD) process for IEC 61000-4-2 system-level ESD protection. The structure of on-chip TVS is a high voltage dual silicon-controlled-rectifier (DSCR) with high holding voltage (V_h) and holding current (I_h). The RS232 transceiver IC with proposed on-chip TVS has been evaluated to pass the IEC61000-4-2 contact ±12 kV stress without any hardware damages and latch-up issue. Moreover, the proposed RS232 transceiver IC has been verified to well protect the system over the IEC 61000-4-2 contact ±20 kV stress (class B) in the notebook applications.

The TVS device is much difficult to be embedded with on-chip design in an advanced CMOS or silicon-on-insulator (SOI) process due to the poor ESD robustness per unit silicon area in these processes. The silicon area is unreasonable by cost consideration for the embedded on-chip TVS to bypass IEC61000-4-2 ESD stress. In Chapter 3, a co-packaged methodology using TVS chips and a controller area network (CAN) bus transceiver to ensure IEC 61000-4-2 system-level ESD protection has been proposed. The design methodology is verified in a high-voltage SOI process for CAN transceiver chip and an 0.8-μm bipolar process for TVS chips. The design target of parasitic inductance by bonding wires is calculated to meet the clamping voltage requirement. The CAN bus transceiver IC with TVS chips co-packaged has been evaluated to pass the IEC61000-4-2 contact ±15 kV stress without any hardware

damages and latch-up issues.

To future avoid the degradation of ESD protection capability of the TVS chip by parasitic inductances from bonding wires, a design scheme to integrate TVS devices and functional ICs in three-dimension integrated circuit (3D IC) package is proposed in Chapter 4. The proposed co-packaged design in 3D IC can use different process to fabricate the functional chip and the TVS chip for reducing the fabrication cost. Moreover, the on-chip ESD protection design on functional chip also can be removed since the TVS chip also provide the on-chip HBM and machine-model (MM) ESD protection capability in the 3D IC package.

With the continuous miniaturization of CMOS transistors, ESD protection has become a tough challenge of integrated circuits with the era of advanced nano-scale CMOS technology. A reduction of ESD target levels was proposed for today's on-chip ESD protection design in industry. During the automatic final test for the IC products, the lower on-chip ESD robustness will cause damage of electronic components if the static control technology is not improved. In Chapter 5, the novel test process and devices to eliminate ESD stress during automatic final test of IC products are proposed. The present test method and devices can remove the electrostatic charges causing damage to the tested IC without modifying the tester.

Chapter 6 concludes the main results of this thesis, and suggests several future works in this research field. In this thesis, several novel designs have been verified for system-level ESD protection. These designs also have been published in international journal papers and applied for patents.