國立交通大學電機學院
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博士論文

全金屬矽化物互補式金氧半奈米晶片之靜電放電防護電路設計與實現

DESIGN AND IMPLEMENTATION OF ESD PROTECTION CIRCUITS IN NANOSCALE FULLY SILICIDED CMOS TECHNOLOGY

研 究 生：葉 致 廷 (Chih-Ting Yeh)

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中華民國一〇二年二月

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摘要

隨著互補式金氧半製程的持續發展並微縮至奈米等級，閘極氧化層變得愈來愈薄且擴散區的接面深度變得愈來愈淺，這些製程上的發展導致金氧半場效電晶體的閘極氧化層崩潰電壓下降以及金氧半場效電晶體的閘極漏電流增加。閘極氧化層崩潰電壓的下降會使得金氧半場效電晶體更容易受到靜電放電(Electrostatic Discharge, ESD)的轟擊而受損，因為靜電放電的本質並未隨著金氧半製程的發展而微縮，閘極漏電流的增加會使得靜電放電防護電路裡的金氧半場效電晶體在靜電放電事件與正常電路操作的情況下發生電性功能失常的問題。在可靠度(Reliability)領域中，靜電放電已成為積體電路產品在量產過程中最為重要的問題，對於所有的電子產品在設計階段時就必須謹慎地將靜電放電等問題納入考慮以符合可靠度的各種規範。為了達到全晶片靜電放電防護設計，所有的銲墊(Pad)，包括輸入/輸出(input/output)銲墊以及電源/接地(VDD/VSS)銲墊，皆必須具有靜電放電防護電路以提供有效的靜電放電防護予積體電路。介於輸入/輸出銲墊以及電源/接地銲墊的靜電放電防護元件無可避免地會對射頻(Radio Frequency, RF)與高速電路的訊號路徑產生寄生效應，而這些電路對於寄生效應是非常敏感的，因為過大的寄生效應會造成射頻與高速電路的電路性能嚴重衰減，因此對於應用在射頻與高速電路的靜電放電防護元件之挑戰則是靜電放電防護元件能夠承受最大的靜電放電耐受度並且達到其寄生效應的最小化。此外，介於電源/接地銲墊之間的靜電放電防護電路則可在電源軌線間提供有效的靜電放電防護，雖然電源軌線間靜電放電箝制電路的寄生效應對於內部電路毫無影響，但是金氧半場效電晶體閘極氧化層崩潰電壓的下降以及閘極漏電流的增加仍然大幅提高了靜電放電防護設計上的困難度。另外，積體電路的單位面積製作成本隨著互補式金氧半製程的持續微縮而快速地增加，因此，在佈局面積上具有高度效益的電源軌線間靜電放電箝制電路也是另一個設計上的挑戰。基於以上所提及之設計挑戰，本論文的研究主題包括：(1)適用於射頻與高速輸入/輸出電路的靜電放電防護二極體、(2)不需電容元件之電源軌線間靜電放電箝制電路、(3)具有等效靜電放電偵

測機制的電源軌線間靜電放電箝制電路、(4)具有閘極漏電流與閘極氧化層可靠度之設計考量的電源軌線間靜電放電箝制電路、(5)不需電阻元件之電源軌線間靜電放電箝制電路。

本論文第二章提出可適用於射頻前端與高速輸入/輸出銲墊的新型靜電放電防護二極體元件，其佈局型式分為八角形、四方中空形、八角中空形、多重四方形、以及多重四方中空形。在 90 奈米互補式金氧半製程的實驗結果顯示，相較於長條形與四方形佈局型式的二極體元件在相同的靜電放電耐受度之下可以達到較小的寄生電容，因此射頻前端與高速輸入/輸出電路的訊號衰減程度可以被降低。

在本論文第三章中，不需使用電容元件的新型靜電放電偵測電路已被提出並且驗證在 65 奈米 1.2 伏特的互補式金氧半製程。相較於傳統的 *RC*-based 靜電放電偵測電路，新型設計的佈局面積可縮小超過 54%，具有可調整維持電壓的新型設計在快速電源啟動以及暫態雜訊干擾的情形下擁有非常好的抗誤觸發與抗暫態引起的閂鎖效應之能力。

本論文第四章提出一個以大通道電晶體作為靜電放電箝制元件並且利用大通道電晶體的寄生二極體之電源軌線間靜電放電箝制電路，並且驗證在 65 奈米 1.2 伏特的互補式金氧半製程。利用二極體連接方式的電晶體作為等效電阻以及利用大通道電晶體寄生逆偏二極體作為等效電容，新型的電容耦合以及 *RC*-based 靜電放電偵測機制可不使用實際的電阻與電容元件就能達成，並且相較於傳統的 *RC*-based 靜電放電偵測電路，可顯著地縮小所需之佈局面積達 82%。

本論文第五章提出一個僅使用薄閘極氧化層元件以及使用矽控整流器(Silicon-Controlled Rectifier, SCR)作為靜電放電箝制元件的電源軌線間靜電放電箝制電路，並且驗證在 65 奈米 1 伏特的互補式金氧半製程。藉由降低在靜電放電偵測電路中元件閘極氧化層的跨壓，提出的電源軌線間靜電放電箝制電路可具有低漏電流，此外，藉由佈局的方式還可以將靜電放電偵測電路完全嵌入至矽控整流器元件中。在本章中，一個可操作在 2 倍 VDD 的電源軌線間靜電放電箝制電路也被提出，並且驗證在相同的製程。根據實驗結果，提出的電源軌線間靜電放電箝制電路搭配 50 微米寬的矽控整流器元件在偏壓 1 伏特的正常電路操作與室溫的情形下僅消耗 34.1 奈安培的漏電流。

本論文第六章提出一個僅使用薄閘極氧化層元件、使用矽控整流器作為靜電放電箝制元件、以及不需使用電阻元件的電源軌線間靜電放電箝制電路，並且驗證在 65 奈米 1 伏特的互補式金氧半製程。技巧性地使用閘極漏電流以實現等效電阻，*RC*-based 靜電放電偵測機制可不使用實際的電阻元件就能達成並且顯著地縮小所需之佈局面積。不需電阻元件的電源軌線間靜電放電箝制電路搭配 45 微米寬的矽控整流器在偏壓 1 伏特的正常電路操作與室溫的情形下僅消耗 1.43 奈安培的極低漏電流。

第七章總結本論文的研究成果，並提出數個接續本論文研究方向的研究題目。本論文所提出的各項新型設計，皆已經由實驗晶片進行驗證。本論文已有數篇國際期刊與國際研討會論文發表。

DESIGN AND IMPLEMENTATION OF ESD PROTECTION CIRCUITS IN NANOSCALE FULLY SILICIDED CMOS TECHNOLOGY

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Abstract

As CMOS technology is continuously scaled down to nanoscale, the gate oxide becomes thinner and the diffusion junction depth becomes shallower. These lead to the reduced gate oxide breakdown voltage and increased gate leakage current of MOS transistor. The reduced gate oxide breakdown voltage makes the MOS transistor more vulnerable to electrostatic discharge (ESD) because ESD is not scaled down with the CMOS technology. The gate leakage current makes the MOS transistors in ESD protection circuit malfunction during ESD stresses and normal circuit operating condition. ESD is one of the most important reliability issues for the integrated circuit (IC) during mass production. It must be taken into consideration during the design phase to meet the reliability specifications for all microelectronic products. For whole-chip ESD protection design, all pads, including the input/output (I/O) pads and VDD/VSS pads, are necessary to be implemented with ESD protection circuits to provide effective ESD protection for the IC. The ESD protection devices between the I/O pads and VDD/VSS pads inevitably cause parasitic effects on the signal path of RF front-end and high-speed circuits, which are very sensitive to those parasitic effects. The challenge of ESD protection devices for RF front-end and high-speed circuits is to sustain the highest ESD level and to achieve the smallest parasitic effects. Moreover, the ESD protection circuits between the VDD/VSS pads are necessary to provide ESD protection between the power rails. Although the parasitic effects of power-rail ESD clamp circuit have no impact on the internal circuits, the reduced gate oxide breakdown voltage and increased gate leakage current of MOS transistor greatly increase the difficulty of ESD protection design. In addition, the fabricated cost per unit area of the IC is dramatically increased with the continuously scaled-down CMOS technology. Therefore, the power-rail ESD clamp circuit with high efficiency of layout area is another design challenge. The research topics

based on aforementioned design challenges in this dissertation including: (1) ESD protection diode for RF and high-speed I/O applications, (2) capacitor-less power-rail ESD clamp circuit, (3) power-rail ESD clamp circuit with equivalent ESD-transient detection mechanism, (4) power-rail ESD clamp circuit with considerations of gate leakage current and gate oxide reliability, and (5) resistor-less power-rail ESD clamp circuit.

In Chapter 2, new ESD protection diodes drawn in the octagon, waffle-hollow, octagon-hollow, multi-waffle, and multi-waffle-hollow layout styles are presented in a 90nm CMOS process. The experimental results confirmed that they can achieve smaller parasitic capacitance under the same ESD robustness level as compared to the stripe and waffle diodes. Therefore, the signal degradation of RF and high-speed transmission can be reduced.

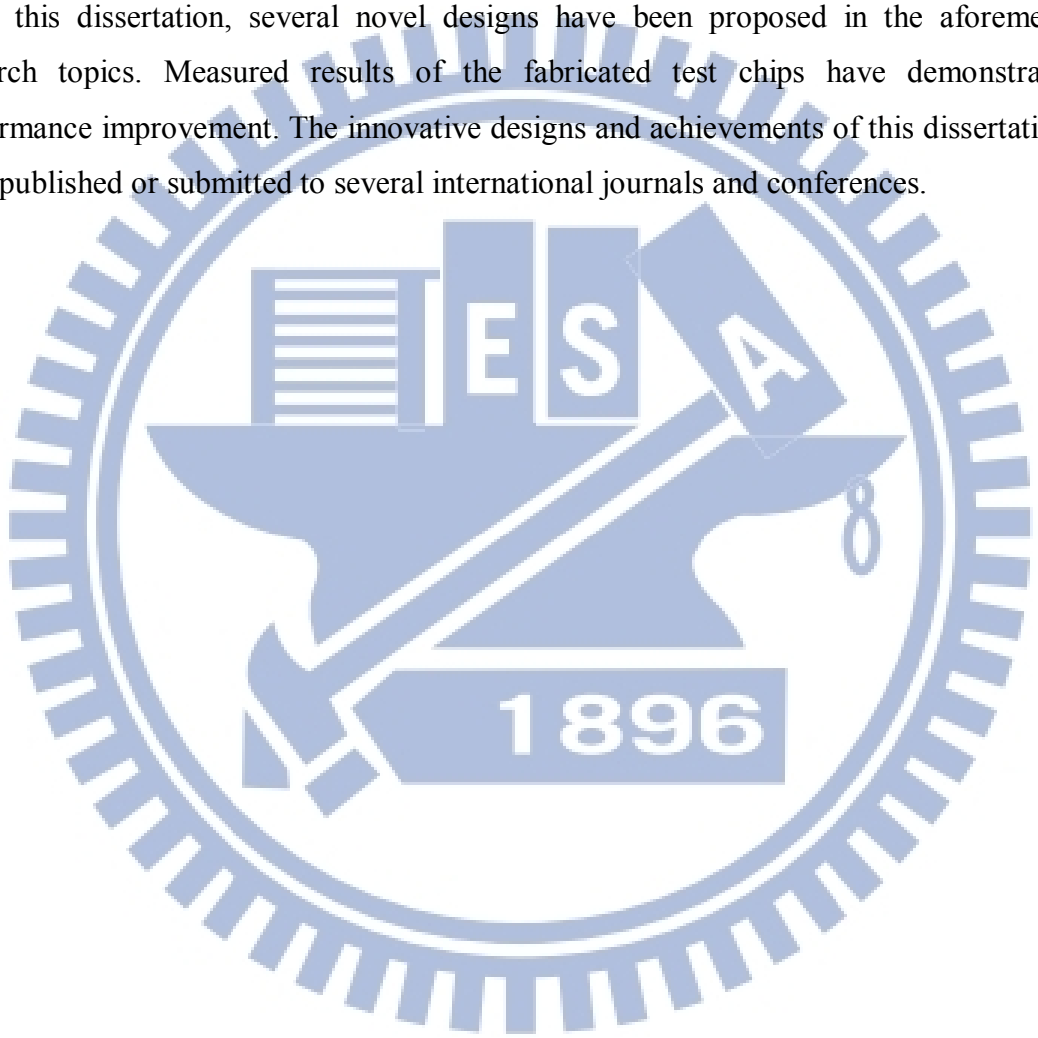
In Chapter 3, a new ESD-transient detection circuit without using the capacitor has been proposed and verified in a 65nm 1.2V CMOS process. The layout area of the new ESD-transient detection circuit can be greatly reduced by more than 54%, as compared to the traditional *RC*-based one. The new ESD-transient detection circuit with adjustable holding voltage has better immunity against mis-trigger and transient-induced latch-on event under the fast power-on and transient noise conditions.

In Chapter 4, a power-rail ESD clamp circuit realized with ESD clamp device drawn in the layout style of BigFET, and with parasitic diode of BigFET, is proposed and verified in a 65nm 1.2V CMOS process. Utilizing the diode-connected MOS transistor as the equivalent large resistor and parasitic reverse-biased diodes of BigFET as the equivalent capacitors, the new *RC*-based and capacitance-coupling ESD-transient detection mechanism can be achieved without using an actual resistor and capacitor to significantly reduce the layout area by ~82%, as compared to the traditional *RC*-based ESD-transient detection circuit.

In Chapter 5, a power-rail ESD clamp circuit realized with only thin gate oxide devices and with SCR as main ESD clamp device has been proposed and verified in a 65nm 1V CMOS process. By reducing the voltage difference across the gate oxide of the devices in the ESD-transient detection circuit, the proposed design can achieve a low standby leakage current. In addition, the ESD-transient detection circuit can be totally embedded in the SCR device by modifying the layout structure. In this chapter, a 2×VDD-tolerant power-rail ESD clamp circuit has also been proposed and verified in the same CMOS process. The proposed design with SCR width of 50μm can achieve a low standby leakage current of 34.1nA at room temperature under the normal circuit operating condition with 1.8V bias.

In Chapter 6, a resistor-less power-rail ESD clamp circuit realized with only thin gate oxide devices, and with SCR as main ESD clamp device, has been proposed and verified in a 65nm 1V CMOS process. Skillfully utilizing the gate leakage current to realize the equivalent resistor, the *RC*-based ESD-transient detection mechanism can be achieved without using an actual resistor. The resistor-less power-rail ESD clamp circuit with SCR width of 45μm can achieve an ultra-low standby leakage current of 1.43nA at room temperature under the normal circuit operating condition with 1V bias.

In this dissertation, several novel designs have been proposed in the aforementioned research topics. Measured results of the fabricated test chips have demonstrated the performance improvement. The innovative designs and achievements of this dissertation have been published or submitted to several international journals and conferences.



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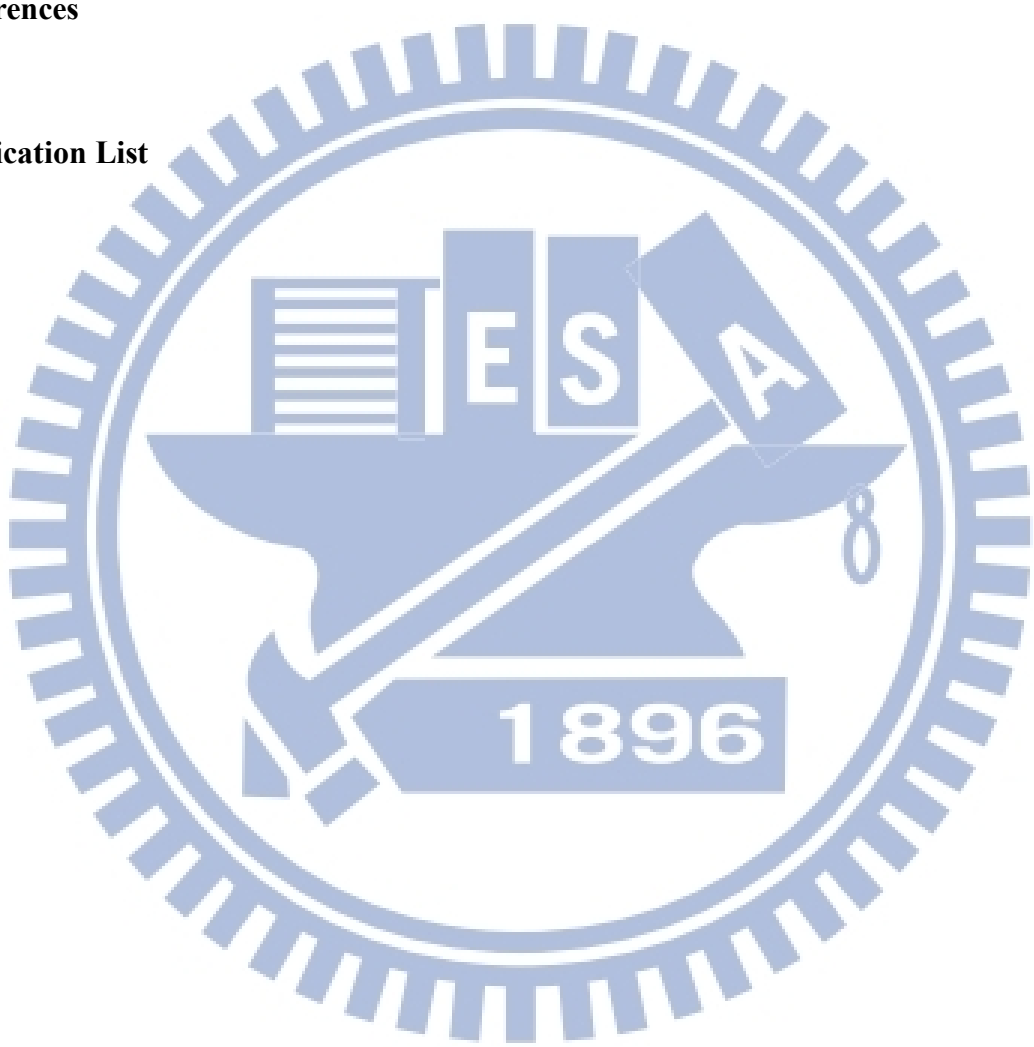

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Chapter 1

Introduction

In this chapter, the background and the organization of this dissertation are discussed. First, the whole-chip electrostatic discharge (ESD) protection designs for on-chip ESD protection in fully silicided complementary metal-oxide-semiconductor (CMOS) processes are introduced. Then, the organization of this dissertation is described.

1.1 Background of Whole-Chip ESD Protection Design

The aggressive scaling of CMOS technology has driven the MOSFET down to sub-100nm scale. ESD has become the main reliability concern on semiconductor products in nanoscale CMOS processes. Generally, the typical ESD specifications for commercial integrated circuit (IC) products are required to be higher than 2kV in human-body-model (HBM) [1] and 200V in machine-model (MM) [2] ESD stresses. HBM and MM ESD tests are used to evaluate the ESD robustness of the IC when the IC is touched by the charged human body or charged machine. The equivalent circuits of HBM and MM ESD tests are shown in Fig. 1.1(a) and (b), respectively. During the HBM ESD test, the charges stored in the capacitor would be discharged into the device under test (DUT) through 1.5kΩ resistor. Similarly, during the MM ESD test, the charges stored in the capacitor would be discharged directly into the DUT. In order to protect the internal circuits against ESD stresses, on-chip ESD protection circuits have to be added between the input/output (I/O) pad and VDD/VSS to provide the desired ESD robustness in CMOS ICs [3]-[5]. Fig. 1.2 shows the concept of whole-chip ESD protection design. The turn-on-efficient power-rail ESD clamp circuit was placed between VDD and VSS power lines to avoid the unexpected ESD damage in the internal circuits [6]-[8]. ESD stresses on an I/O pad with respect to the grounded VDD or VSS have four pin combinations: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode), as shown in Fig. 1.3(a) ~ (d), respectively. For comprehensive ESD verification, the pin-to-pin and VDD-to-VSS ESD stresses had also been specified to verify the whole-chip ESD robustness, as shown in Figs. 1.4 and 1.5, respectively.

The typical on-chip ESD protection scheme with double-diode at I/O pad and the

power-rail ESD clamp circuit is shown in Fig. 1.6 [9]. In Fig. 1.6, the diodes Dp and Dn are placed at input pad and output pad. The Dp is a P+/N-well diode and the Dn can be an N+/P-well diode or an N-well/P-substrate diode. The diodes Dp and Dn are operated under forward-biased condition to provide discharging paths between I/O pad and VDD/VSS. Under positive-to-VDD mode (PD-mode) and negative-to-VSS mode (NS-mode) ESD stresses, ESD current is discharged through the forward-biased diodes Dp and Dn, as shown in Fig. 1.7(a). During positive-to-VSS mode (PS-mode) and negative-to-VDD mode (ND-mode) ESD stresses, the power-rail ESD clamp circuit between VDD and VSS is necessary to provide ESD current discharging path between the power rails [8]. Hence, ESD current can be discharged from I/O pad through the forward-biased diode Dp to VDD, and discharged to the grounded VSS through the turn-on-efficient power-rail ESD clamp circuit during PS-mode ESD stress. Similarly, ESD current can be discharged from VDD through the turn-on-efficient power-rail ESD clamp circuit to VSS, and discharged to I/O pad through the forward-biased diode Dn during ND-mode ESD stress, as shown in Fig. 1.7(b). During pin-to-pin ESD stress, ESD current is discharged from the zapped I/O pad through the forward-biased diode Dp, the power-rail ESD clamp circuit, and the forward-biased diode Dn to the grounded I/O pad, as shown in Fig. 1.7(c). Under VDD-to-VSS ESD stress, ESD current is discharged through the turn-on-efficient power-rail ESD clamp circuit between VDD and VSS. With the turn-on-efficient power-rail ESD clamp circuit, the ESD diodes Dp and Dn can be certainly operated in forward-biased condition during all ESD test modes.

Although the power-rail ESD clamp circuit operated independently between VDD and VSS does not have any parasitic effect on the internal circuits, the parasitic effects of ESD protection devices at the I/O pads inevitably introduce some negative impacts to degrade the circuit performance. For the high-frequency performance, the main parasitic effect of ESD protection devices is the parasitic capacitance. Therefore, the parasitic capacitance of ESD protection device at the RF and high-speed input pad is strictly limited because the input signal is small and sensitive to the shunt parasitic capacitance of ESD protection device. On the contrary, the devices at the RF output stage are implemented with large dimensions to output the signals with large enough signal power. The devices at the RF output stage can also be properly used to protect the RF output pad against ESD stresses. Therefore, ESD protection design with low parasitic capacitance and high ESD robustness for the input pad of the RF receiver is more challenging than that for the output pad of the RF transmitter.

1.2 Organization of This Dissertation

In order to achieve the whole-chip ESD protection design, several new ESD protection diodes with layout modification and power-rail ESD clamp circuits with area and/or leakage efficiency are proposed and verified in this dissertation. This dissertation consists of seven chapters. In chapter 2, the ESD protection diodes for RF and high-speed I/O applications are investigated. The ESD protection diodes are proposed in several new layout styles to improve the ratio of ESD robustness to parasitic capacitance. In chapter 3, capacitor-less power-rail ESD clamp circuit is proposed to reduce the layout area and standby leakage current. In chapter 4, the power-rail ESD clamp circuit with equivalent ESD-transient detection mechanism is proposed to achieve high efficiency of layout area. By using the same concept of ESD-transient detection circuit with positive feedback mechanism proposed in chapter 3, the power-rail ESD clamp circuits with the considerations of gate leakage current and gate oxide reliability are investigated in chapter 5 for core VDD and high-voltage-tolerant applications. In chapter 6, resistor-less power-rail ESD clamp circuit is also proposed to solve the gate leakage current and gate oxide reliability issues by utilizing the gate leakage itself to construct *RC*-based ESD-transient detection mechanism. The outlines of each chapter are summarized below.

In chapter 2, new ESD protection diodes drawn in the octagon, waffle-hollow, octagon-hollow, multi-waffle, and multi-waffle-hollow layout styles to improve the efficiency of ESD current distribution and to reduce the parasitic capacitance for RF front-end and high-speed I/O pads are presented. The experimental results in a 90nm CMOS process confirmed that they can achieve smaller parasitic capacitance under the same ESD robustness level as compared to the stripe and waffle diodes, especially for the diodes drawn in the hollow layout style. Therefore, the signal degradation of RF and high-speed transmission can be reduced due to smaller parasitic capacitance of the new proposed diodes.

The ESD clamp device drawn in the layout style of BigFET has been utilized to effectively enhance the ESD robustness of CMOS ICs. In chapter 3, a new ESD-transient detection circuit without using the capacitor has been proposed and verified in a 65nm 1.2V CMOS process. The layout area of the new ESD-transient detection circuit can be greatly reduced by more than 54%, as compared to the traditional *RC*-based ESD-transient detection circuit. From the experimental results, the new ESD-transient detection circuit with adjustable holding voltage can achieve long enough turn-on duration under ESD stress condition, as well as better immunity against mis-trigger and transient-induced latch-on event under the fast

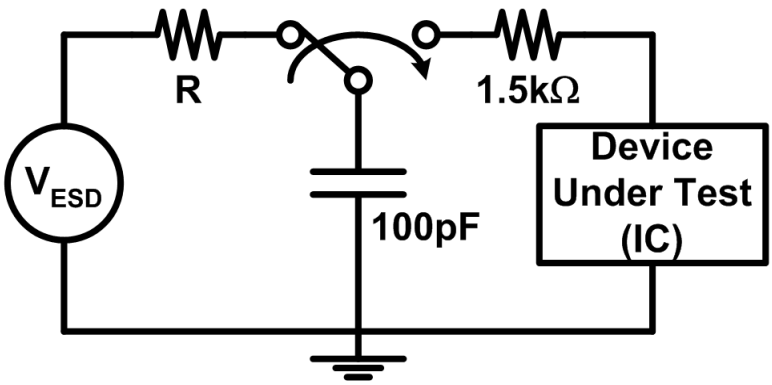
power-on and transient noise conditions.

In chapter 4, a power-rail ESD clamp circuit realized with ESD clamp device drawn in the layout style of BigFET, and with parasitic diode of BigFET as a part of ESD-transient detection mechanism, is proposed and verified in a 65nm 1.2V CMOS process. Utilizing the diode-connected MOS transistor as the equivalent large resistor and parasitic reverse-biased diodes of BigFET as the equivalent capacitors, the new *RC*-based and capacitance-coupling ESD-transient detection mechanism can be achieved without using an actual resistor and capacitor to significantly reduce the layout area by ~82%, as compared to the traditional *RC*-based ESD-transient detection circuit.

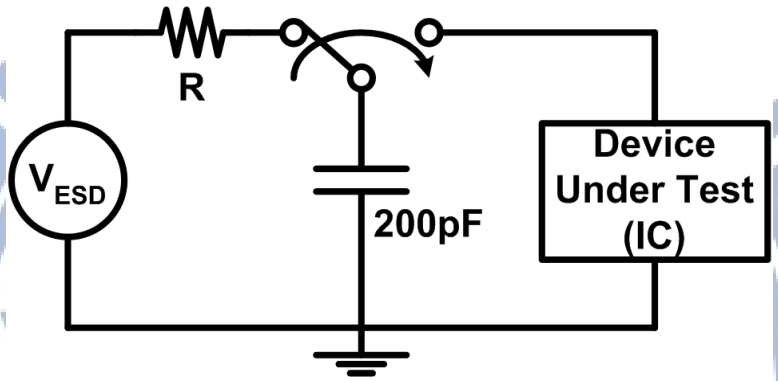
In chapter 5, a power-rail ESD clamp circuit realized with only thin gate oxide devices and with SCR as main ESD clamp device has been proposed and verified in a 65nm 1V CMOS process. By reducing the voltage difference across the gate oxide of the devices in the ESD-transient detection circuit, the proposed power-rail ESD clamp circuit can achieve a low standby leakage current. In addition, the ESD-transient detection circuit can be totally embedded in the SCR device by modifying the layout structure. From the measured results, the proposed power-rail ESD clamp circuit with SCR width of 45μm can achieve 7kV HBM and 350V MM ESD levels, while consuming only a standby leakage current in the order of nano-ampere at room temperature under the normal circuit operating condition with 1V bias. In this chapter, a 2×VDD-tolerant power-rail ESD clamp circuit with only thin gate oxide 1V devices and SCR as main ESD clamp device has also been proposed and verified in the same CMOS process. From the measured results, the proposed design with SCR width of 50μm can achieve 6.5kV HBM, 300V MM ESD levels, and a low standby leakage current of 34.1nA at room temperature under the normal circuit operating condition with 1.8V bias.

In chapter 6, a resistor-less power-rail ESD clamp circuit realized with only thin gate oxide devices, and with SCR as main ESD clamp device, has been proposed and verified in a 65nm 1V CMOS process. Skillfully utilizing the gate leakage current to realize the equivalent resistor in the ESD-transient detection circuit, the *RC*-based ESD-transient detection mechanism can be achieved without using an resistor to significantly reduce the layout area. From the measured results, the resistor-less power-rail ESD clamp circuit with SCR width of 45μm can achieve 5kV HBM, 400V MM ESD levels, and a low standby leakage current of 1.43nA at room temperature under the normal circuit operating condition with 1V bias.

Chapter 7 summarizes the main results of this dissertation. Some suggestions for the future works are also addressed in this chapter.



(a)



(b)

Fig. 1.1 Equivalent circuits of (a) HBM and (b) MM ESD tests.

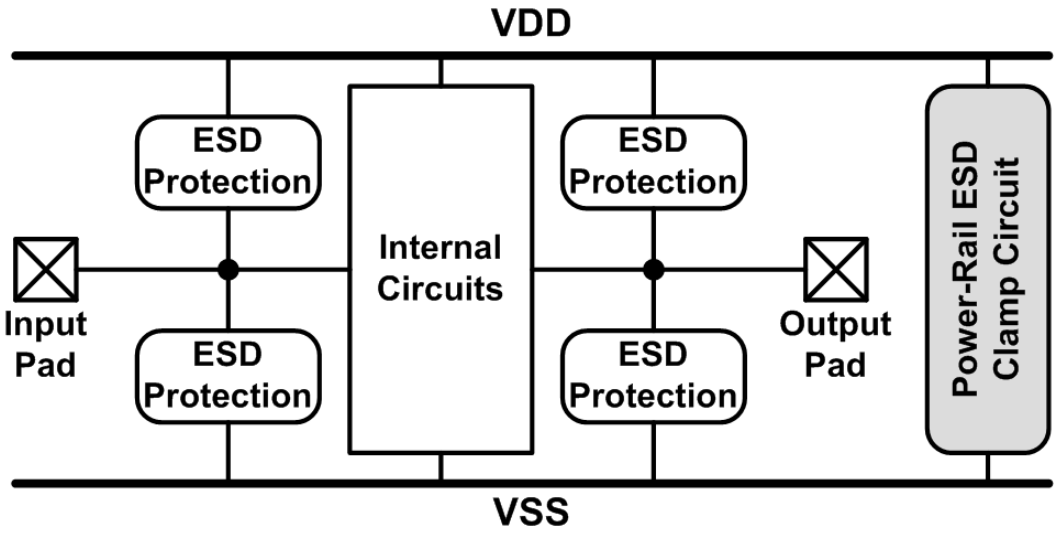


Fig. 1.2 Design concept of whole-chip ESD protection circuits in CMOS ICs.

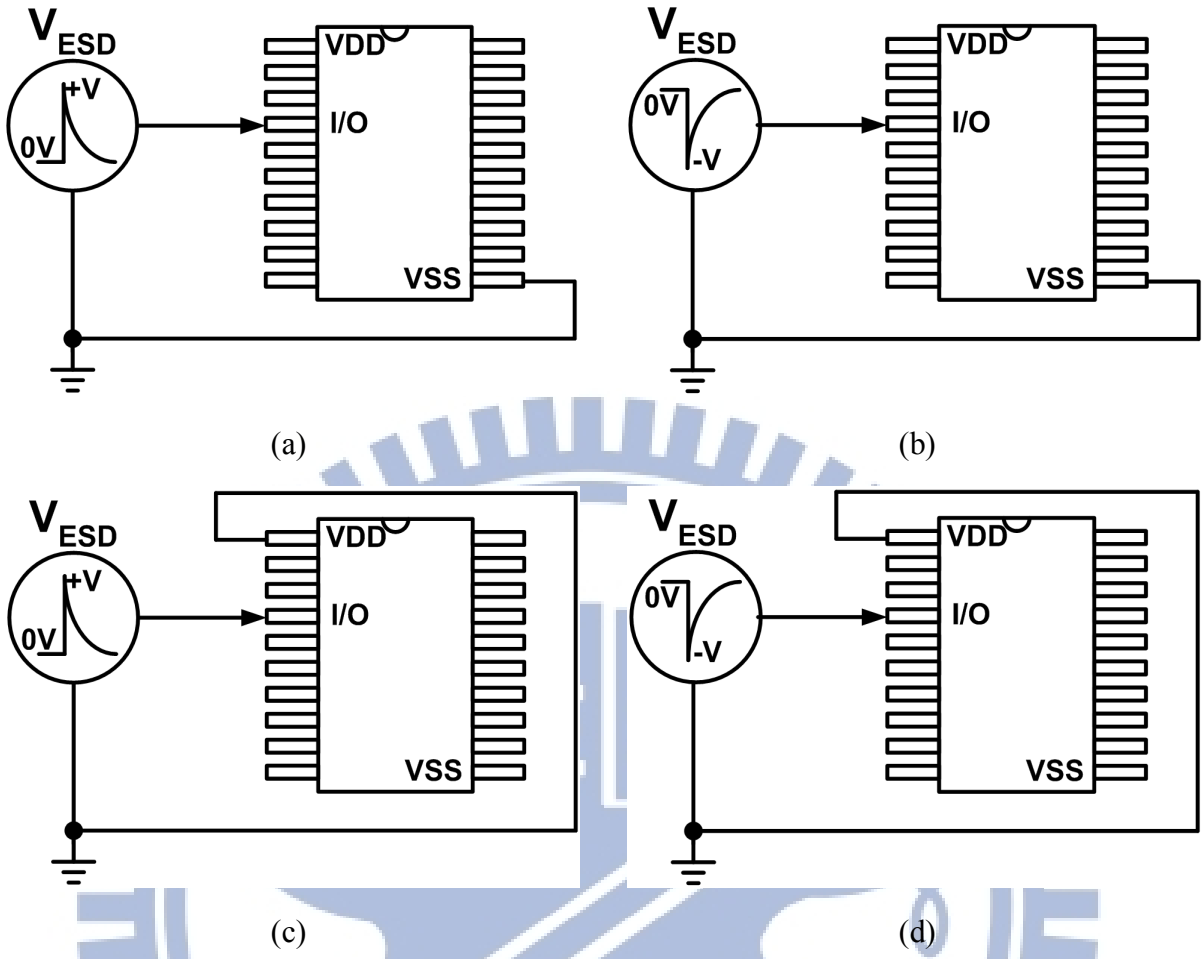


Fig. 1.3 The four pin combinations for ESD test on an IC product: (a) positive-to-VSS (PS-mode), (b) negative-to-VSS (NS-mode), (c) positive-to-VDD (PD-mode), and (d) negative-to-VDD (ND-mode).

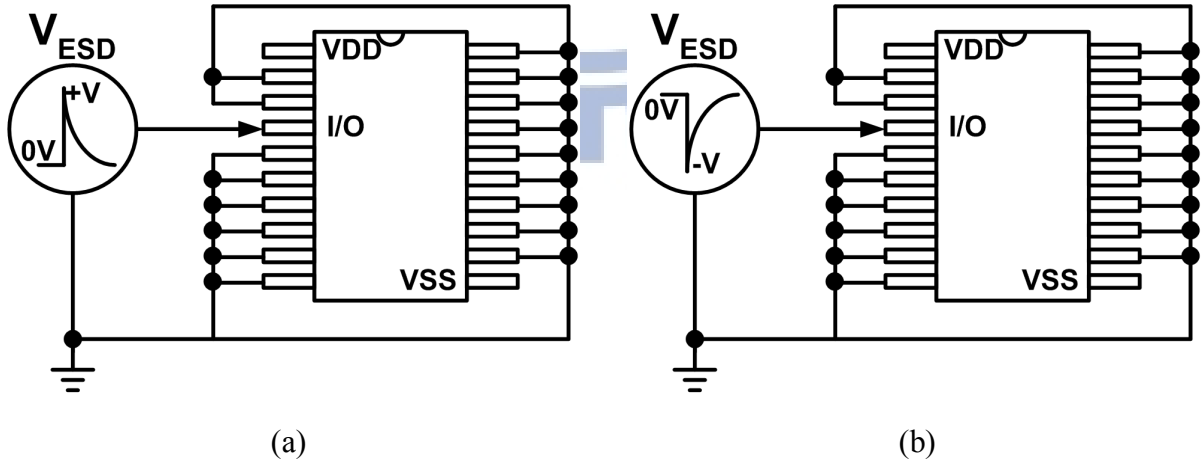
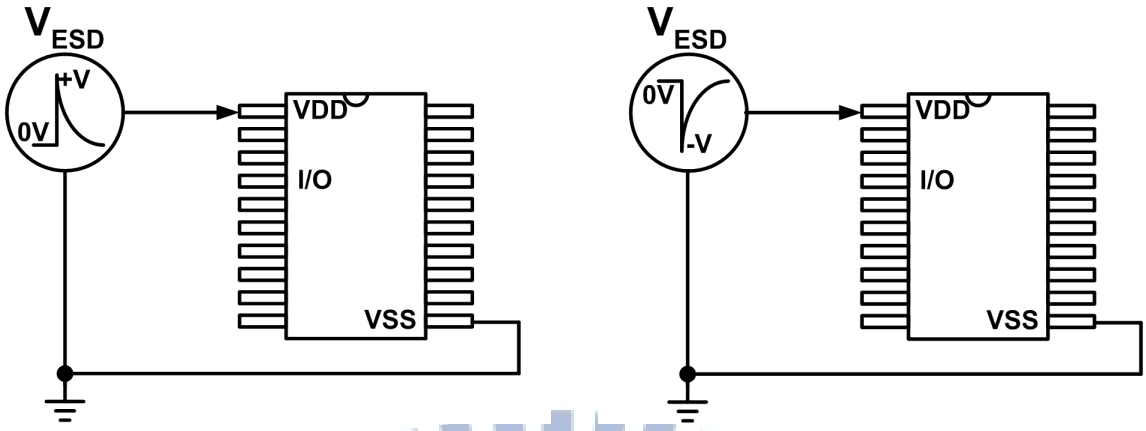


Fig. 1.4 Pin-to-pin ESD tests: (a) positive mode and (b) negative mode.



(a) (b)

Fig. 1.5 VDD-to-VSS ESD tests: (a) positive mode and (b) negative mode.

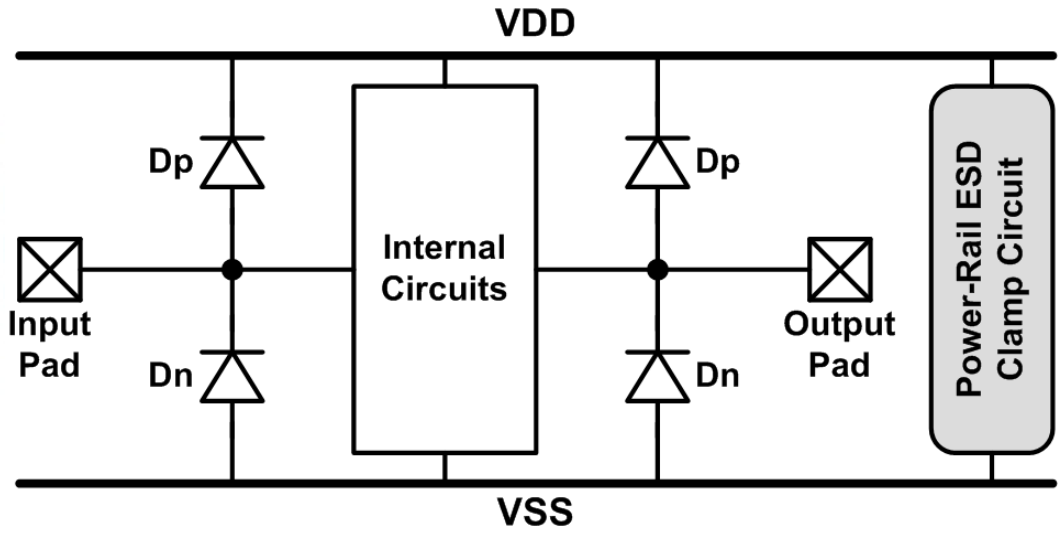
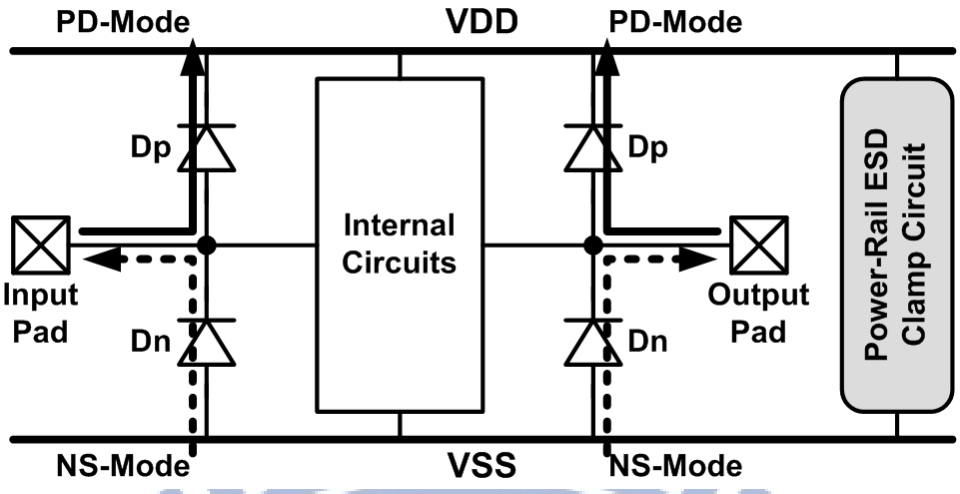
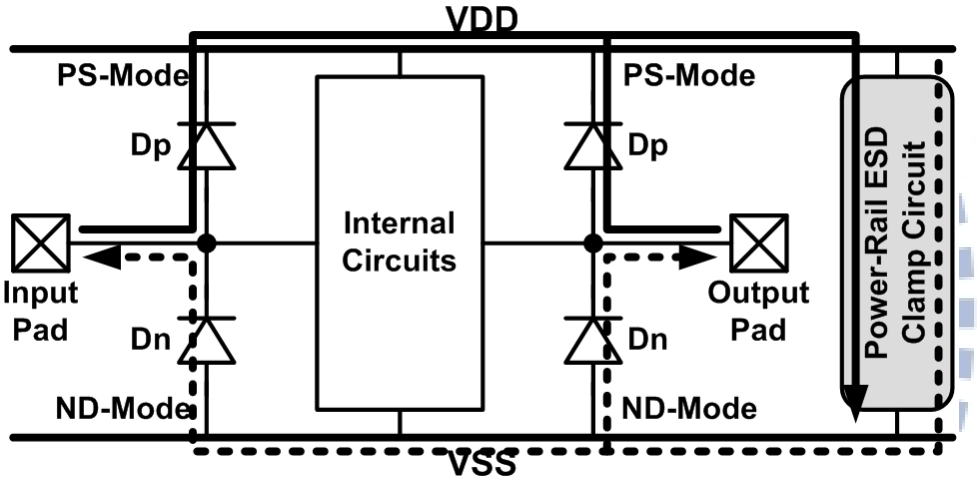


Fig. 1.6 Typical on-chip double-diode ESD protection scheme.



(a)



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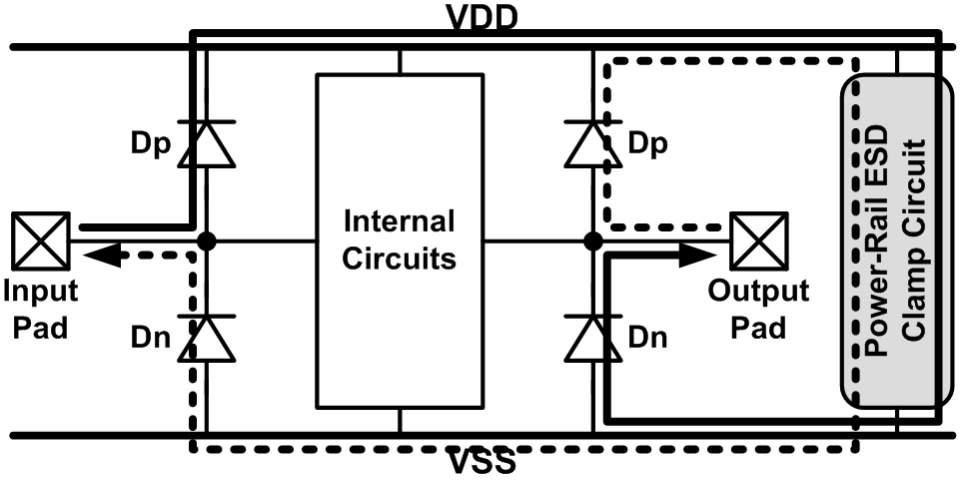


(c)

Fig. 1.7 ESD current discharging paths in the typical double-diode ESD protection scheme under (a) PD-mode, NS-mode, (b) PS-mode, ND-mode, and (c) pin-to-pin ESD stresses.

Chapter 2

ESD Protection Diode for RF and High-Speed I/O Applications

In this chapter, the ESD protection diodes for RF and high-speed I/O applications are presented. The ESD diodes with octagon, waffle-hollow, and octagon-hollow layout styles are investigated in section 2.2, and those with multi-waffle and multi-waffle-hollow layout styles are discussed in section 2.3. All ESD diodes with new proposed layout styles were fabricated in a 90nm CMOS process to achieve high ESD robustness and low parasitic capacitance.

2.1 Background

ESD has become the major concern of reliability for ICs in nanoscale CMOS technology. The thinner gate oxide and shallower diffusion junction seriously degraded the ESD robustness of ICs and raised the difficulty of ESD protection design for ICs implemented in nanoscale CMOS technology [10]-[13]. Furthermore, thinner metal layer and shallower diffusion junction increase the resistance and local heat of the ESD protection devices [14]. In order to sustain the required ESD robustness, such as 2kV in HBM [1] and 200V in MM [2], the on-chip ESD protection devices must be drawn with large enough device dimension. However, the parasitic loading effects of the ESD protection devices with large device dimension will obviously degrade the circuit performance of signal transmission, especially for radio-frequency (RF) front-end and high-speed input/output (I/O) circuits [15], [16]. In order to reduce the circuit performance degradation, the parasitic capacitance (C_{ESD}) of the ESD protection devices must be minimized but the ESD robustness is still kept at the reasonable level [17]. ESD protection designs for RF front-end and high-speed I/O interface circuits must be optimized with consideration of parasitic capacitance and ESD robustness.

A typical on-chip ESD protection scheme for RF front-end or high-speed I/O applications is shown in Fig. 2.1, where two ESD diodes at I/O pad are cooperated with the turn-on-efficient power-rail ESD clamp circuit to discharge ESD current in the forward-biased condition [4], [12], [18]. Through the turn-on-efficient power-rail ESD clamp circuit, the

device dimensions of these two diodes can be significantly shrunk to meet the circuit performance and ESD requirement simultaneously. In order to minimize the parasitic capacitance caused by the ESD protection diodes and to achieve satisfactory ESD robustness, the high frequency characteristics and the ESD levels of the ESD protection diodes in a 90nm CMOS process were evaluated in this work to obtain the dependence of device size on ESD robustness and parasitic capacitance. Furthermore, the layout style of ESD protection diode will also directly affect its ESD robustness and parasitic capacitance.

Under normal circuit operation, the diode is turned off under the reverse-biased condition. Although the diode is turned off, there is still an intrinsic junction capacitance of the diode seen by the signals at the I/O pad. On the other hand, the diode should be turned on to discharge ESD current at forward-biased condition (cooperated with efficient power-rail ESD clamp circuit) under ESD stresses. Therefore, the intrinsic junction capacitance of the diode at reverse-biased condition and the ESD protection capability of the diode at forward-biased condition are the important characteristics to investigate ESD diodes.

The current-handling ability of ESD protection device is usually indicated in terms of its second breakdown current It_2. However, the measured *I-V* curve of the diode, as shown in Fig. 2.2, reveals that the ESD protection diode near the failure level It_2 may not function as an effective voltage clamp due to the series resistances of the diffusion regions [19]. When the current level approaches to It_2, the increased on-resistance (R_{ON}) would result in local heating in the silicon or metal routing. Therefore, the maximum current-handling capability of the diode is suggested to be defined as the current level at which the measured *I-V* curve deviates from its linearly extrapolated value by 20% [20]-[22]. In this work, the current compression point is denoted as I_{CP}, which is used to represent the current-handling capability of the ESD protection diode.

Although the I_{CP} and R_{ON} of the ESD diode can be improved by increasing its device size, this would cause larger C_{ESD} and layout area of the ESD diode. Consequently, in order to determine the efficiency of the ESD diodes with different layout styles for high-speed I/O circuits, the figure of merits (FOMs) of R_{ON}*C_{ESD} and I_{CP}/C_{ESD} will be utilized. It is better for the ESD protection diode to achieve higher I_{CP} and lower C_{ESD} at the specific layout style and device size. In order to further improve the I_{CP}/C_{ESD}, the area of active junction region in ESD protection diode must be minimized to attain low parasitic capacitance, but its junction perimeter must be maximized to enhance the ESD robustness. Moreover, the FOM of V_{HBM}/C_{ESD} can also be an alternative evaluation factor for the ESD diodes because the HBM

levels (V_{HBM}) of the ESD protection diodes are reasonably relative to I_{CP}.

2.2 Octagon, Waffle-Hollow, and Octagon-Hollow Layout Styles

For the N+/P_{sub} diode, the GND and I/O nodes are electrically connected to P+ diffusion and N+ diffusion, respectively. Under normal circuit operation, the diode is kept off due to the reverse-biased condition between the P_{sub} and N+ diffusion regions. Although the diode is turned off, there is still an intrinsic junction capacitance of the diode seen by the signals at the I/O pad. On the other hand, the diode should be turned on to conduct ESD current at forward-biased condition under ESD stresses. Therefore, the junction capacitance of diode at reverse-biased condition and the ESD protection capability of diode at forward-biased condition are the important parameters to be investigated in the following. In this section, the ESD protection diodes realized in stripe, waffle, octagon, waffle-hollow, and octagon-hollow layout styles are fabricated in a 90nm CMOS process and compared with each other. According to the measured results, the ESD protection diodes with octagon and hollow layout styles can successfully boost the I_{CP}/C_{ESD} to make the diodes more profitable to RF front-end and high-speed I/O applications.

2.2.1 Diode with Stripe Layout Style

The device cross-sectional view and layout top view of the ESD protection diodes with stripe layout style are shown in Fig. 2.3, which is the typical layout style to be often implemented in IC products. This typical stripe diode is realized with P+ stripe on both sides of the N+ stripe to give it with twice the conducting perimeter. Moreover, the width of N+ stripe is twice as large as that of each P+ stripe in order to avoid the current crowding at the N+ stripe region. Based on the typical stripe diode, the diodes with the new proposed layout style will be discussed in the following sections to improve the characteristics of diodes for ESD protection and circuit performance. In previous studies [20], [23]-[25], the ESD protection diodes realized in the waffle layout style have been verified to achieve better FOM than that of stripe diodes under careful size optimization, which is suitable to RF front-end and high-speed I/O applications [20], [23].

2.2.2 Diodes with Waffle and Octagon Layout Styles

The device cross-sectional view and layout top view of the ESD protection diodes with waffle and octagon layout styles are shown in Figs. 2.4(a) and (b), respectively. The octagon

layout style is formed from waffle layout style but the four corners are cut off. When the junction area of waffle and octagon diodes is reduced, they can achieve lower parasitic capacitance. Compared to the waffle diode, the junction perimeter and junction area of the octagon diode are simultaneously smaller than those of the waffle diode by 17%. It means that all FOM based on physical characteristics of the waffle and octagon diodes would be totally the same. Fortunately, the risk of damages located at the corner can be reduced by forming octagon layout style because the corner angle of octagon diode is larger than that of waffle diode. Hence, the octagon diode can be supposed to have better ESD level than waffle diode.

2.2.3 Diodes with Waffle-Hollow and Octagon-Hollow Layout Styles

The two new proposed diodes investigated in this study are illustrated in Figs. 2.5(a) and (b), which are called as the waffle-hollow and octagon-hollow layout styles, respectively. Generally, the parasitic capacitance of the diode is proportional to the active junction area and the ESD robustness is related to the active junction perimeter. The purpose of forming the hollow layout is to reduce the active junction area and to keep the active junction perimeter at the same time by removing the N+ central diffusion region. For instance, the cross-sectional view to explain ESD current flows in the diodes with waffle and waffle-hollow layout styles are shown in Figs. 2.6(a) and (b), respectively. According to the device cross-sectional view in Fig. 2.6(a), the ESD current could not uniformly flow through whole N+ active junction region in the waffle diode because the current always tends to flow through the shortest path between two nodes. Therefore, there is only a small part of total ESD current discharging through the N+ central diffusion region, where still contributes parasitic capacitance to RF front-end and high-speed I/O circuits at normal circuit operation. By removing the N+ central diffusion region to form the hollow layout style, the ESD current can be effectively concentrated in restricted region of the diode as shown in Fig. 2.6(b). Consequently, the diodes with hollow layout style can be expected to attain a great reduction of parasitic capacitance without degrading ESD robustness severely at the same time. Similarly, all FOM based on physical characteristics of the waffle-hollow are also the same as those of octagon-hollow diodes.

Based on the waffle layout style studied in previous work [20], [23], the octagon, waffle-hollow, and octagon-hollow layout styles are proposed and fabricated in a 90nm CMOS process to investigate the dependence between ESD robustness and parasitic capacitance on diode layout styles. The important layout parameters of those investigated

diodes are listed in Table 2.1, where the different spacings are also marked in Fig. 2.3, Fig. 2.4, and Fig. 2.5, respectively. It has to be noticed that the dimensions of the stripe diode in this work are not optimum.

2.2.4 Interconnect Routing of the Diodes

To effectively reduce the impact from the parasitic resistance and capacitance of the interconnect routing in the layout of ESD diodes, the arrangement of metal lines to connect the ESD diodes should be considered with the de-embedding calculation. The 3D layout diagram of interconnect routing of the $N+/P_{sub}$ diode is shown in Fig. 2.7(a). The width of metal line from the diode to the bond pad is drawn as large as possible to reduce the parasitic resistance of interconnect routing. With the large width of metal line, the parasitic resistance of interconnect routing (that can be estimated manually with the sheet resistance provided by foundry) can be quite smaller than the on-resistance R_{ON} of the ESD diodes.

About the parasitic capacitance of interconnect routing, the 3D layout diagram of the open pad structure for de-embedding calculation is shown in Fig. 2.7(b). All metal layers are remained except the diodes. With the measured *S*-parameters of the open pad structure, the parasitic capacitance of interconnect routing can be de-embedded to obtain the pure junction capacitance of the ESD diodes.

The different metal routing approaches [20], [23] were not discussed in this work because the diodes are totally symmetric. To diminish the parasitic effects of interconnect routing is emphasized in this work to obtain the pure characteristics of the diodes.

2.2.5 Performance Evaluations

Before implementing the diodes, there is a useful evaluation to imply the goodness of the diodes. This evaluation discussed in the following paragraphs is based on the physical dimensions of diodes listed in Table 2.1.

This important evaluation is the factor of (N+ junction perimeter) / (total N+ junction area). This is the most commonly used evaluation to estimate the diodes, as that illustrated in Fig. 2.8. The N+ junction perimeter is related to ESD robustness and the total N+ junction area is corresponded to parasitic capacitance at normal circuit operation. Undoubtedly, this evaluation is expected to be large to sustain high enough ESD robustness and minimize the degradation of circuit performance for RF front-end and high-speed I/O applications. In Fig. 2.8, the diodes with hollow layout styles obviously have the highest values at the specified

diode size. Moreover, the large-size diodes with hollow layout styles can achieve comparable level to that of small-size diodes with non-hollow layout style. This result inspires us to consider a way not to continuously shrink the diode size to avoid any capacitance penalty from the junction perimeter [17], [20], [23]. Though the diode with stripe layout style has the smallest width, its evaluation is not the highest because the diode with stripe layout style can not give the N+ junction perimeter as much as those of the diodes with other layout styles. The performance evaluation is also listed in Table 2.1.

2.2.6 Experimental Results

The test chips of diodes with the stripe, waffle, and new proposed layout styles have been fabricated in a 90nm CMOS process. These diodes are prepared with the considerations of two-port *S*-parameter measurement, TLP measurement, and HBM ESD level measurement. In this work, each diode structure was tested four times from four separated dice.

2.2.6.1 Parasitic Capacitance

The diode devices are arranged with ground-signal-ground (G-S-G) pads to facilitate on-wafer two-port *S*-parameter measurement. During the *S*-parameter measurement, the P+ and N+ diffusion regions of the diode devices are connected to port 1 and port 2, respectively, and they are both biased at 0V.

In order to extract the characteristics of the intrinsic device at high frequency, the parasitic effects of the pad and the interconnect routing must be de-embedded [26]-[28]. The test structures, one including the DUT and the other excluding the DUT (open pad structure), as shown in Figs. 2.9(a) and (b), were implemented in the same test chip [26], [27]. The Y_{22}-parameter can be obtained from the measured two-port *S*-parameters by

$$Y_{22} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{Z_0\left((1+S_{11})(1+S_{22})-S_{12}S_{21}\right)} \tag{1}$$

where Z_0 is the termination resistance of 50Ω [28]. The measured *Y*-parameter of the including-DUT pattern is labeled as $Y_{22\text{-meas}}$, and the measured *Y*-parameter of the excluding-DUT pattern (open pad structure) is labeled as $Y_{22\text{-open}}$. The intrinsic device characteristics, $Y_{22\text{-DUT}}$, can be obtained by subtracting $Y_{22\text{-open}}$ from $Y_{22\text{-meas}}$. The parasitic capacitance (C_{ESD}) of each diode can be extracted from the $Y_{22\text{-DUT}}$ by

$$C_{ESD} = \frac{\mathrm{Im}(Y_{22-DUT})}{2\pi f} \tag{2}$$

where *f* is the operating frequency. The extracted parasitic capacitances of the fabricated diode devices at 2.5GHz under zero DC bias are listed in Table 2.2 and shown in Fig. 2.10.

From the measured results of the diode devices with stripe, waffle, and octagon layout styles, the extracted parasitic capacitances are obviously proportional to the N+ occupied area. Meanwhile, the reductions of parasitic capacitances can achieve 16%, 26%, and 39% by modifying the diodes in size A, size B, and size C from waffle to waffle-hollow layout styles, respectively. Similarly, it can achieve the reductions of parasitic capacitance of 13%, 25%, and 38% by modifying the diodes from octagon to octagon-hollow layout styles. The reduction of parasitic capacitance is exactly meeting the theoretical calculations. This great reduction of parasitic capacitance is the key factor to significantly improve the FOM of the diodes with hollow layout style.

2.2.6.2 Transmission Line Pulsing (TLP) Measurement

In order to investigate the device behavior during high ESD current stress, TLP generator with a pulse width of 100ns and a rise time of ~2ns is used to measure It_2 of the device [29]. For the ESD protection diode, it is suggested that an appropriate upper-bound current level, I_{CP}, is utilized because the ESD protection diode should never be designed to discharge ESD current near its failure level [20], [23]. By using TLP, the R_{ON}, It_2, and I_{CP} derived from It_2 of the diode devices under positive stresses at the P+ diffusion region with grounded N+ diffusion region are measured and listed in Table 2.2. The R_{ON} and I_{CP} versus the N+ junction perimeter of the diodes are illustrated in Fig. 2.11 and Fig. 2.12, respectively. Apparently, the R_{ON} is decreased and the I_{CP} is increased with the increased N+ junction perimeter.

When the diode is modified from non-hollow to hollow layout style, the drop on I_{CP} of the diode with large device size is greater than that of the diode with small device size. The line current densities, which are the ratio of I_{CP} to N+ junction perimeter, of waffle and octagon diodes are calculated in Table 2.3. The drop percentages of line current density from waffle to waffle-hollow (from octagon to octagon-hollow) are also calculated in Table 2.3. From the measured results and calculations, the waffle (or octagon) diode with large device size has larger line current density and larger drop percentage of line current density while modified to waffle-hollow (or octagon-hollow) diode. This implies that the ESD discharging current of waffle (or octagon) diode with large device size would flow more deeply through the N+ central diffusion region because waffle (or octagon) diode with large device size has more contacts at N+ diffusion region to cause a small equivalent resistance at cathode. With more

detailed explanation and illustration, the simulations can give a clear perspective. Figs. 2.13(a) and (b) are the current vector plots of the diode in small size and large size, respectively. For convenience, the anode is set along the entire edge of the diode and the cathode is set along the right half of the top surface of the diode. When the diode is drawn in small size, the fewer contacts at junction area make the current crowded into the nearest corner of the electrode. On the contrary, there are more contacts at junction area for the diode drawn in large size as shown in Fig. 2.13(b). The current crowding behavior experienced in Fig. 2.13(a) has diminished and the current can be distributed through the entire electrode more widely. Based on the simulation results and the measured results of line current density, the ESD discharging current through the diode in large size is expected to flow more deeply through the N+ central diffusion region. Therefore, the diode in large device size has larger reduction of I_{CP} when the diode with non-hollow layout style is modified to hollow layout style.

According to the measured results, the reductions of I_{CP} are 2.4%, 6.2%, and 14.8% for the waffle diodes in size A, size B, and size C, respectively. Also, they are 1.2%, 4.4%, and 10.6% for the octagon diodes in size A, size B, and size C, respectively. Compared with the reductions of parasitic capacitance, the removed N+ central diffusion region is originally flowed by a small part of total ESD discharging current. Consequently, removing the N+ central diffusion region of the diodes can greatly reduce the parasitic capacitance without degrading the ESD protection capability.

2.2.6.3 ESD Robustness

The HBM ESD robustness of the fabricated diodes is also listed in Table 2.2. The relationship between the HBM ESD level (V_{HBM}) and the It_2 based on the measured results in this work is about

$$V_{HBM} \approx (1800 + R_{ON}) \times It_2 \tag{3}$$

where R_{ON} is the turn-on resistance of the diode. The HBM ESD levels of all ESD protection diodes are within the range of 1.4-3.5kV, except the stripe diode.

2.2.7 FOM Comparison and Discussion

The FOM (I_{CP}/C_{ESD}, V_{HBM}/C_{ESD}, and $R_{ON}\times C_{ESD}$) of the diode devices are listed in Table 2.2 and illustrated in Figs. 2.14-2.16. The most important FOM, I_{CP}/C_{ESD}, among the diodes is illustrated in Fig. 2.14. The trend of I_{CP}/C_{ESD} is apparently increasing from non-hollow to hollow layout style due to the reduction of parasitic capacitance, and the results exactly meet

the expectation of layout design. Because the HBM ESD level is directly proportional to It_2, the trend of V_{HBM}/C_{ESD} illustrated in Fig. 2.15 is quite similar to that in Fig. 2.14. According to the experimental results of diodes with different layout styles, the diodes with hollow layout styles can apparently achieve higher ESD robustness under the same parasitic capacitance. For instance, the measured results clearly demonstrate that the I_{CP}/C_{ESD} of waffle-hollow (or octagon-hollow) diode in size C is better than that of waffle (or octagon) diode in size B. These two diodes actually have the same total N+ junction area, but the N+ junction perimeter of waffle-hollow (or octagon-hollow) diode in size C is obviously larger. This feature reveals that the diodes with waffle-hollow (or octagon-hollow) layout styles can attain higher I_{CP} than those with waffle (octagon) layout styles under the same total N+ junction area to achieve better I_{CP}/C_{ESD}. Besides, the I_{CP}/C_{ESD} can also be slightly improved from waffle (or waffle-hollow) diode to octagon (or octagon-hollow) diode due to the relaxation of current distribution located at the smoother corners.

The I_{CP}/C_{ESD} values of waffle-hollow and octagon-hollow diodes in size B and size C can achieve almost the same level as that of waffle diode in size A. It represents that the diode with hollow layout style in large size still can sustain I_{CP} as high as that of the diode with waffle layout style in small size under the same parasitic capacitance. As a result, the waffle-hollow and octagon-hollow diodes in large size can perform as well as the waffle diode in small size under careful layout optimization.

From TLP *I-V* measurement and the results in Fig. 2.12, R_{ON} can be reduced by increasing the N+ junction perimeter of the ESD diodes, but this action also increases the parasitic capacitance of the ESD diodes simultaneously due to the increased N+ junction area. For ESD protection purpose, the R_{ON} of the ESD diode is expected to be as small as better to effectively clamp the voltage. The C_{ESD} is also highly demanded to be as small as better to avoid the RF circuits' performance degradation. Therefore, the $R_{ON}\times C_{ESD}$ is another useful justification to the diodes, as shown in Fig. 2.16. The $R_{ON}\times C_{ESD}$ value of the stripe diode is too large, that is hard to be implemented for high-performance RF and high-speed I/O interface applications. For the diodes with hollow layout styles, such values can be reduced to the range from 23 to 34 (Ω-fF), which is much smaller than that of the stripe diode. Moreover, the $R_{ON}\times C_{ESD}$ value of the waffle-hollow and octagon-hollow diodes in large size can also be comparable to that of waffle and octagon diodes with small size.

Although the waffle diode in small size theoretically has larger ratio of N+ junction perimeter to N+ junction area, carefully optimizing the size of waffle diode is still required to

avoid any capacitance penalty from junction perimeter [20], [23]. Therefore, it is not necessary to simply shrink the device size of waffle diode to achieve high value of I_{CP}/C_{ESD} and low value of $R_{ON}\times C_{ESD}$. In this work, it has been verified that there are two methods, forming octagon and hollow layout styles, to effectively improve the I_{CP}/C_{ESD} and $R_{ON}\times C_{ESD}$ of the diodes.

2.3 Multi-Waffle and Multi-Waffle-Hollow Layout Styles

The STI-bound $N+/P_{sub}$ and $P+/N_{well}$ ESD protection diodes fabricated in a 90nm CMOS technology were investigated in this section. The evaluations of ESD protection diodes with stripe and waffle layout styles in previous works [20], [21], [23] are briefly reviewed. Two new layout styles are proposed to effectively improve the FOMs of ESD protection diodes. The key design variables are the P-N junction dimensions and layout styles. Experimental results of the ESD protection diodes have confirmed that the new layout styles can successfully improve $R_{ON}*C_{ESD}$ and I_{CP}/C_{ESD} of the diodes. Compared to the prior arts, the diodes drawn with the new proposed layout styles are adequate for high-speed I/O applications. It should be noted that, for applications other than gigahertz frequency and high-speed I/O circuits, the C_{ESD} of the ESD diode may not be the major concern of the design. Instead, the ESD protection diode might be optimized based on different performance evaluation, such as layout area (A_{Layout}). Therefore, the FOM of I_{CP}/A_{Layout} presented in this section also gives another perspective factor on the tradeoffs between diode dimensions and layout styles.

2.3.1 Diodes with Stripe and Waffle Layout Styles

Under forward-biased condition, the perimeter of the P-N junction in ESD diode primarily provides electrical conduction path [22]. It implies that the bottom plate of the P-N junction in ESD diode mainly contributes the C_{ESD}. Therefore, the FOMs, especially for I_{CP}/C_{ESD}, should be enhanced by maximizing the junction perimeter and minimizing the junction area.

The top view of the STI-bound $N+/P_{sub}$ ESD diode with stripe layout style is shown in Fig. 2.17, which is the typical layout style often implemented in IC products. This typical stripe diode is realized by P+ stripe with both sides of the N+ stripe to give it with twice the electrical conduction path. Because the dimension H is much smaller than L, these two short sides of N+ stripe do little to improve electrical conduction. For the stripe diode, the ratio of junction perimeter to junction area for N+ strip diffusion region can be expressed as

$$\frac{Junction\ \ Perimeter}{Junction\ \ Area} = \frac{2 \cdot L}{H \cdot L} = \frac{2}{H} \tag{4}$$

Another STI-bound N+/P_{sub} ESD protection diode with waffle layout style is shown in Fig. 2.18(a). The waffle diode has been studied in the previous works [24], [25], [30]. The N+ diffusion region is surrounded by a P+ diffusion region. In order to obtain different current-handling capability of the diode, multiple waffle diodes can be joined in parallel to form an array structure. A similar waffle structure can be implemented for P+/N_{well} diode, as shown in Fig. 2.18(b). For the waffle diode, the ratio of junction perimeter to junction area can be expressed as

$$\frac{Junction\ \ Perimeter}{Junction\ \ Area} = \frac{4 \cdot H}{H \cdot H} = \frac{4}{H} \tag{5}$$

which is twice as large as that for the stripe diode in (4). These evaluations imply that a waffle diode may potentially outperform a stripe diode.

In the previous works [20], [21], [23], the ESD protection diodes with the waffle layout style have been verified to achieve better FOMs than that of stripe diodes under careful size optimization. In addition, the diodes with waffle-hollow, octagon, and octagon-hollow layout styles have been proposed in the previous work [21] to further improve the FOMs of the waffle diode. Because the junction perimeter and the junction area of the octagon (octagon-hollow) diode are simultaneously smaller than those of the waffle (waffle-hollow) diode by 17%, the measured FOMs of the octagon (octagon-hollow) diode are only slightly better than those of the waffle (waffle-hollow) diode. However, the FOMs of the diodes with hollow layout style are significantly improved because the useless junction area is removed to reduce the parasitic capacitance. In this work, the new multi-waffle layout style based on waffle layout style is proposed. The multi-waffle diode with the increased junction perimeter and the reduced junction area is supposed to have better FOMs than that of waffle diode. Based on the same concept of hollow layout style in [21], the new multi-waffle-hollow layout style based on multi-waffle layout style is also proposed to further enhance the FOMs for high-speed I/O applications.

2.3.2 Diodes with Multi-Waffle and Multi-Waffle-Hollow Layout Styles

The layout top view of the N+/P_{sub} [30] and P+/N_{well} ESD protection diodes with multi-waffle layout style are shown in Figs. 2.19(a) and (b), respectively. The multi-waffle layout style is modified from waffle layout style. The P+ (N+) diffusion region extends into the N+ (P+) diffusion region from four sides for N+/P_{sub} (P+/N_{well}) diodes. The junction area

can be theoretically reduced by a factor of 44%. Besides, the junction perimeter can also be increased by a factor of 67% at the same time. It implies that the ratio of junction perimeter to junction area for the multi-waffle diode can be given by

$$\frac{Junction\ \ Perimeter}{Junction\ \ Area} = \frac{5 \cdot (4 \cdot H/3)}{5 \cdot (H/3)^2} = \frac{12}{H} \tag{6}$$

which is triple of that in (5). This suggests that the multi-waffle layout style can be another good method to reduce C_{ESD} of ESD diode for high-speed I/O applications.

It should be noted that the risk of damages located at the corner might be elevated because the corner number of multi-waffle diode is more than that of waffle diode. Moreover, the uniformity issue of discharging current would be emerged in real multi-waffle diode. However, the multi-waffle diode can still be supposed to have better FOMs than those of waffle diode due to great reduction of junction area and great raise of junction perimeter.

The other new layout style for ESD diode is illustrated in Fig. 2.20, which is called as the multi-waffle-hollow layout style. The multi-waffle-hollow layout style is modified from the multi-waffle layout style by removing the N+ (P+) central diffusion region of $N+/P_{sub}$ ($P+/N_{well}$) diodes. The purpose is to further reduce the junction area and to keep the junction perimeter at the same time. For instance, the cross-sectional view to explain ESD current flows in the $N+/P_{sub}$ diodes with hollow and non-hollow layout styles are shown in Figs. 2.6(a) and (b), respectively. For the non-hollow layout style shown in Fig. 2.6(a), the ESD current could not be uniformly discharged through the whole N+ diffusion region because the current always tends to flow through the shortest path between two nodes. The ESD discharging current did not flow through the N+ central diffusion region, where still contributes C_{ESD} at normal circuit operation. To form the hollow layout style as shown in Fig. 2.6(b), the N+ central diffusion region is removed to directly reduce the junction area of the diode. The ESD discharging current can be effectively concentrated in the remaining N+ diffusion region of the diode. Therefore, the ratio of junction perimeter to junction area for the multi-waffle-hollow diode can be theoretically expressed by

$$\frac{Junction\ \ Perimeter}{Junction\ \ Area} = \frac{5 \cdot (4 \cdot H/3)}{5 \cdot (H/3)^2 - 5 \cdot (S)^2} = \frac{12}{H - \dfrac{(3 \cdot S)^2}{H}} \tag{7}$$

where the junction perimeter is assumed to be the same as that of multi-waffle layout style and the symbol *S* represents the width of removed central diffusion region. The ratio in (7) is

always larger than that in (6) for multi-waffle diode. Therefore, the multi-waffle-hollow diode can be expected to further reduce the C_{ESD} and to keep the ESD robustness at the same time.

In this work, the ESD diodes with multi-waffle and multi-waffle-hollow layout styles are drawn and fabricated in a 90nm CMOS process to investigate their corresponding FOMs. The major layout parameters of those N+/P_{sub} and P+/N_{well} diodes are listed in Table 2.4, where the different spacings are also marked in Figs. 2.18-2.20.

2.3.3 Performance Evaluations

Before implementing the diodes, there is a useful evaluation to imply the goodness of ESD diodes. This important evaluation is the ratio of (junction perimeter) / (junction area), which has been calculated in (4) ~ (7) for different layout styles. Undoubtedly, the high evaluation value suggests that the ESD diodes can sustain high ESD robustness with low C_{ESD} to minimize the degradation of circuit performance for high-speed I/O applications. The evaluation values for the diodes investigated in this work are listed in Table 2.4 and illustrated in Fig. 2.21. According to the theoretical calculations, the diode in small size obviously has larger evaluation value at the given layout style. It can also be noted that the diodes in large size with the two new modified layout styles can achieve comparable level to that of small-size diodes with waffle layout style. This result reveals that not to continuously shrink the diode size but to implement the diode with new modified layout styles can be a good choice for avoiding the penalty, such as parasitic sidewall capacitance from the junction perimeter and local heat distribution [20], [23].

2.3.4 Experimental Results

The test chips of STI-bound N+/P_{sub} and P+/N_{well} diodes with the original waffle and two new modified layout styles have been fabricated in a 90nm CMOS process. These diodes are prepared with the consideration of two-port *S*-parameter measurement, TLP measurement, and HBM ESD robustness measurement. In this work, each diode structure was tested four times from four separated dice.

2.3.4.1 Parasitic Capacitance

The extracted C_{ESD} of the fabricated N+/P_{sub} (P+/N_{well}) diodes from 4 to 5GHz under zero DC bias are listed in Table 2.5 (2.6) and compared in Fig. 2.22. From the measured results of the diodes with waffle, multi-waffle, and multi-waffle-hollow layout styles, the extracted

parasitic capacitances of the diodes in large dimension are practically proportional to the junction area. It can be observed that the extracted parasitic capacitances of waffle diodes in small size are higher than expected values due to parasitic sidewall capacitances. When the diodes are modified from waffle to multi-waffle and multi-waffle-hollow layout styles, the junction area is purposely decreased and the junction perimeter is increased. The contribution of parasitic sidewall capacitance induced by increased junction perimeter would be gradually emerged. Therefore, the measured C_{ESD} trend lines of multi-waffle and multi-waffle-hollow diodes in Figs. 2.22(a) and (b) are a little higher than that of waffle diode. Besides, it can be also observed that the measured C_{ESD} of multi-waffle-hollow diode in size C is slightly larger than that of multi-waffle diode in size C due to the effect of parasitic sidewall capacitance. Compared to the $N+/P_{sub}$ ($P+/N_{well}$) waffle diodes in size C ~ size E, the C_{ESD} can be reduced 33%, 34%, and 36% (44%, 38%, and 37%) for the $N+/P_{sub}$ ($P+/N_{well}$) multi-waffle diodes, respectively. Similarly, they can be reduced 32%, 39%, and 46% (43%, 46%, and 47%) for the $N+/P_{sub}$ ($P+/N_{well}$) multi-waffle-hollow diodes. These great reductions of C_{ESD} are the major factors to significantly improve the FOMs of the diodes with new layout styles.

2.3.4.2 TLP Measurement

The R_{ON} and current compression point (I_{CP}) of the fabricated STI-bound diodes under forward-biased condition were characterized by the TLP system. The current level I_{CP} is utilized for comparison. By using TLP system, the R_{ON} and I_{CP} of the $N+/P_{sub}$ and $P+/N_{well}$ diodes under forward-biased condition are extracted and listed in Table 2.5 and Table 2.6, respectively. The R_{ON} versus the junction perimeter of the $N+/P_{sub}$ and $P+/N_{well}$ diodes with different layout styles are illustrated in Figs. 2.23(a) and (b), respectively. Apparently, the R_{ON} is decreased with the increased junction perimeter.

The I_{CP} versus the junction perimeter of the $N+/P_{sub}$ and $P+/N_{well}$ diodes with different layout styles are illustrated in Figs. 2.24(a) and (b), respectively. The junction perimeter of multi-waffle diode is purposely increased 67% to be larger than that of waffle diode. But the I_{CP} is not increased as much as the theoretical expectation when the diode is modified from waffle to multi-waffle layout style. This is caused by non-uniformity of the ESD discharging current. Besides, the increased corners of multi-waffle diode also increase the risk of damages at the corners. However, the C_{ESD} can be greatly reduced by removing the N+ (P+) diffusion region of the $N+/P_{sub}$ ($P+/N_{well}$) diode. Consequently, the FOMs can still be expected to be further improved by modifying the diode from waffle to multi-waffle and multi-waffle-hollow

layout styles.

The line current densities, which are the ratio of I_{CP} to junction perimeter, of multi-waffle and multi-waffle-hollow diodes are calculated in Table 2.7. The reduction percentages of line current density from multi-waffle to multi-waffle-hollow layout style are also calculated in Table 2.7. When the diode is modified from multi-waffle to multi-waffle-hollow layout style, the reduction on I_{CP} of the diode in large device size is greater than that of the diode in small device size. This implies that the ESD discharging current of multi-waffle diode in large device size would flow more deeply through the central diffusion region because the multi-waffle diode in large device size has more contacts at diffusion region to cause a small equivalent resistance at cathode.

2.3.4.3 ESD Robustness

The HBM ESD robustness of the ESD diode is measured by KeyTek ZapMaster with the test method standard [31]. The ESD diodes are tested from 0.1kV to 8kV with the step 0.1kV under forward-biased condition and the results are also listed in Table 2.5 and Table 2.6. The V_{HBM} versus the N+ (P+) junction perimeter of the N+/P_{sub} (P+/N_{well}) diodes with different layout styles are shown in Fig. 2.25. The trend in Fig. 2.25 is quite similar to Fig. 2.24.

2.3.5 FOM Comparison and Discussion

The FOMs (R_{ON}*C_{ESD}, I_{CP}/C_{ESD}, V_{HBM}/C_{ESD}, and I_{CP}/A_{Layout}) of the ESD diodes in a 90nm COM technology are listed in Table 2.5 and Table 2.6. According to TLP *I-V* measured results in Fig. 2.23, R_{ON} can be reduced by increasing the junction perimeter, but the junction area of the ESD diodes would be increased simultaneously. The R_{ON} of the ESD diode is expected to be small to effectively clamp the voltage. The C_{ESD} is also highly demanded to be small to minimize the degradation of circuit performance. Therefore, the R_{ON}*C_{ESD} is a useful justification to the ESD diodes. The exact values of R_{ON}*C_{ESD} of the N+/P_{sub} and P+/N_{well} diodes with different layout styles are illustrated in Figs. 2.26(a) and (b). In Fig. 2.26, the R_{ON}*C_{ESD} values of the diodes with new modified layout styles in size C can be comparable to that of waffle diodes in small size.

The most important FOM of I_{CP}/C_{ESD} should be expected to be high to sufficiently sustain the ESD stresses. The exact values of I_{CP}/C_{ESD} of the N+/P_{sub} and P+/N_{well} diodes with different layout styles are shown in Figs. 2.27(a) and (b). For the waffle diodes in size A and size B, the I_{CP}/C_{ESD} values are not improved as high as that of theoretical expectation. The

main reason is that the effects of parasitic sidewall capacitance and the local heat dissipation are getting serious when the dimension of the diode is shrunk. However, the I_{CP}/C_{ESD} values of the diodes at given size can be greatly improved from the waffle to the new layout styles in order to avoid the penalty when continuously shrinking the diode size. Moreover, the trend of V_{HBM}/C_{ESD} illustrated in Fig. 2.28 is quite similar to that in Fig. 2.27 because the HBM ESD level is highly related to It_2. Taking the multi-waffle diode in size C and waffle diode in size A for comparison, the I_{CP}/C_{ESD} and the V_{HBM}/C_{ESD} values of multi-waffle $N+/P_{sub}$ ($P+/N_{well}$) diode are only smaller than those of waffle diode about 15% and 11% (29% and 8%), respectively. Overall, I_{CP}/C_{ESD} and V_{HBM}/C_{ESD} values of $P+/N_{well}$ diodes are better than those of $N+/P_{sub}$ diodes. It was found that the $P+/N_{well}$ diodes have both a higher I_{CP} and a lower C_{ESD} than their $N+/P_{sub}$ diode counterparts. The higher I_{CP} may be caused by the turn-on parasitic vertical PNP bipolar transistor [20]. The lower parasitic capacitance is most likely due to the different N_{well} and P_{sub} doping concentrations. Besides, $R_{ON}*C_{ESD}$ values of $P+/N_{well}$ diodes are also slightly lower than those of $N+/P_{sub}$ diodes due to the smaller C_{ESD}.

Another design concern for the circuit applications is layout area (A_{Layout}). In advanced CMOS technology, the fabrication cost per die area is getting higher and higher. Therefore, the biggest concern of some ESD designers might be to save the layout area of the protection circuit but to sustain required ESD robustness. The values of I_{CP}/A_{Layout} of the $N+/P_{sub}$ and $P+/N_{well}$ diodes with different layout styles are shown in Figs. 2.29(a) and (b), respectively. The value of I_{CP}/A_{Layout} is supposed to be large to meet the requirements of layout area efficiency for a given ESD robustness. For the diodes with new modified layout styles, the values of I_{CP}/A_{Layout} are within the range from 17 to 19mA/μm^2 for $N+/P_{sub}$ diodes and 18 to 21mA/μm^2 for $P+/N_{well}$ diodes. The I_{CP}/A_{Layout} value of the waffle diode in size A is obviously the smallest among all ESD diodes. Taking the multi-waffle diode in size C and waffle diode in size A for comparison, the I_{CP}/A_{Layout} value of multi-waffle $N+/P_{sub}$ ($P+/N_{well}$) diode are higher than that of waffle diode about 66% (59%). It implies that the effect of local heat dissipation is truly getting serious to degrade the current-handling capability when the diode size is getting small.

Although the waffle diodes in size A and size B theoretically have larger ratio of junction perimeter to total junction area as shown in Fig. 2.21, the size of waffle diode is still required to be carefully optimized. The penalties of parasitic sidewall capacitance and significant reduction on I_{CP} due to local heat dissipation for the waffle diode in small size are emerged. Therefore, it should not to simply shrink the device size of waffle diode for achieving better

FOMs. Based on the FOMs illustrated in Figs. 2.26-2.29, the characteristics of the diodes in large size can be improved to the level of waffle diodes in small size by adequately modifying the layout style. Overall, the diodes with new modified layout styles are superior to those waffle diodes in small size for implementing to the high-speed I/O circuits with the consideration of layout area.

2.4 Summary

In section 2.2, the new proposed diodes with octagon and hollow layout styles have been successfully verified in a 90nm CMOS process. The layout optimization is the essential element to minimize the parasitic capacitance and to improve ESD robustness of the ESD protection diodes for RF front-end and high-speed I/O applications. As compared to the diodes with stripe and waffle layout style, the new proposed diodes with hollow layout styles have been demonstrated to significantly improve ESD robustness under the same parasitic capacitance. Therefore, the proposed waffle-hollow and octagon-hollow diodes are more suitable to be implemented to RF front-end and high-speed I/O circuits.

In section 2.3, the ESD diodes with multi-waffle and multi-waffle-hollow layout styles have also been successfully verified in a 90nm CMOS technology. They are characterized in terms of some FOMs (R_{ON}*C_{ESD}, I_{CP}/C_{ESD}, V_{HBM}/C_{ESD}, and I_{CP}/A_{Layout}) to evaluate the suitability for high-speed I/O applications. It is expected that the FOMs of the ESD diode can be improved by maximizing the ratio of junction perimeter to junction area. However, it is found that the FOMs of waffle diodes with continuously shrinking size would be limited due to emerged parasitic sidewall capacitance and local heat dissipation in small layout area. As a result, the FOMs of waffle diodes will not be further improved by simply shrinking the diode size to maximize the ratio of junction perimeter to total junction area.

The new proposed diodes with multi-waffle and multi-waffle-hollow layout styles have been demonstrated. The new proposed diodes in large size can avoid the penalty of local heat distribution. The reduction of junction area by using new layout styles is the key factor to significantly improve the FOMs of the ESD diodes. As compared to the FOMs of waffle diodes, it reveals that the FOMs values of the large size diodes can be enhanced by modifying the layout styles. Therefore, the proposed multi-waffle and multi-waffle-hollow diodes are also adequate to be implemented to high-speed I/O applications with small layout area.

Table 2.1

Device Dimensions and Previous Evaluation Values of Diodes under Different Layout Styles

Layout Style	Stripe	Waffle			Octagon			Waffle-hollow			Octagon-hollow		
Size	D	A	B	C	A	B	C	A	B	C	A	B	C
Sizes of Device (μm)	W=1 G=0.5 H=2 L=40	W=1 G=0.5 H=3	W=1 G=0.5 H=4	W=1 G=0.5 H=5	W=1 G=0.5 H=3	W=1 G=0.5 H=4	W=1 G=0.5 H=5	W=1 G=0.5 H=3 S=1	W=1 G=0.5 H=4 S=2	W=1 G=0.5 H=5 S=3	W=1 G=0.5 H=3 S=1	W=1 G=0.5 H=4 S=2	W=1 G=0.5 H=5 S=3
N+ Junction Perimeter (μm)	80	24	32	40	19.92	26.56	33.20	24	32	40	19.92	26.56	33.20
Total N+ Junction Area (μm^2)	80	18	32	50	14.94	26.56	41.50	16	24	32	13.28	19.92	26.56
N+ Junction Perimeter / Total N+ Junction Area	1.00	1.33	1.00	0.80	1.33	1.00	0.80	1.50	1.33	1.25	1.50	1.33	1.25

Table 2.2

Measured Results and FOM of Diode Devices with Different Layout Styles

Layout Style	Stripe	Waffle			Octagon			Waffle-hollow			Octagon-hollow		
Size	D	A	B	C	A	B	C	A	B	C	A	B	C
C_{ESD} (fF)	83.71	16.70	31.18	47.64	13.65	26.44	41.39	13.92	22.95	28.95	11.85	19.89	25.61
It_2 (A)	3.338	0.948	1.418	1.851	0.861	1.241	1.636	0.944	1.281	1.639	0.840	1.178	1.481
I_{CP} (A)	2.873	0.755	1.192	1.675	0.664	1.026	1.434	0.737	1.118	1.428	0.656	0.981	1.282
V_{HBM} (kV)	6.6	1.7	2.6	3.5	1.4	2.2	2.9	1.7	2.3	3.1	1.4	2.0	2.7
R_{ON} (Ω)	0.885	1.690	1.280	1.024	1.912	1.460	1.156	1.693	1.314	1.093	1.967	1.509	1.299
I_{CP} / C_{ESD} (mA/fF)	34.32	45.21	38.23	35.16	48.64	38.80	34.65	52.95	48.71	49.33	55.36	49.32	50.06
V_{HBM} / C_{ESD} (V/fF)	78.84	101.8	83.39	73.47	102.6	83.21	70.07	122.1	100.2	107.1	118.1	100.6	105.4
R_{ON} × C_{ESD} (Ω-fF)	74.08	28.22	39.91	48.78	26.10	38.60	47.85	23.57	30.16	31.64	23.31	30.01	33.27

Table 2.3

Line Current Density of Diode Devices from Waffle (Octagon) to Waffle-Hollow (Octagon-Hollow)

Layout Style	From Waffle to Waffle-hollow						From Octagon to Octagon-hollow					
Size	A	A	B	B	C	C	A	A	B	B	C	C
I_{CP} (A)	0.755	0.737	1.192	1.118	1.675	1.428	0.664	0.656	1.026	0.981	1.434	1.282
N+ Junction Perimeter (μm)	24	24	32	32	40	40	19.92	19.92	26.56	26.56	33.20	33.20
Line Current Density (mA/μm)	31.46	30.71	37.25	34.94	41.88	35.70	33.33	32.93	38.63	36.94	43.19	38.61
Drop Percentage of Line Current Density (%)	2.38		6.20		14.76		1.20		4.37		10.60	

Table 2.4

Device Characteristics and Previous Evaluation Items of Diodes with Different Layout Styles

Layout Style	Size	Dimensions of Device (μm)	Array	Junction Perimeter (μm)	Junction Area (μm^2)	Layout Area, A_{Layout} (μm^2)	Junction Perimeter / Junction Area
Waffle	A	W=0.22, H=0.56, G=0.34	5x1	11.2	1.57	14.11	7.13
	B	W=0.22, H=1.12, G=0.34	5x1	22.4	6.27	25.09	3.57
	C	W=0.22, H=3.36, G=0.34	5x1	67.2	56.45	100.35	1.19
	D	W=0.22, H=4.20, G=0.34	5x1	84.0	88.20	141.51	0.95
	E	W=0.22, H=5.04, G=0.34	5x1	100.8	127.01	189.73	0.79
Multi-waffle	C	W=0.22, H=3.36, G=0.34	5x1	112.0	31.36	100.35	3.57
	D	W=0.22, H=4.20, G=0.34	5x1	140.0	49.00	141.51	2.86
	E	W=0.22, H=5.04, G=0.34	5x1	168.0	70.56	189.73	2.38
Multi-waffle-hollow	C	W=0.22, H=3.36, S=0.34, G=0.34	5x1	112.0	28.47	100.35	3.93
	D	W=0.22, H=4.20, S=0.62, G=0.34	5x1	140.0	39.39	141.51	3.55
	E	W=0.22, H=5.04, S=0.90, G=0.34	5x1	168.0	50.31	189.73	3.34

Table 2.5

Measured Results and Figures-of-Merit of $N+/P_{sub}$ Diodes with Different Layout Styles

Layout Style	Size	C_{ESD} (fF)	I_{CP} (A)	R_{ON} (Ω)	I_{t2} (A)	V_{HBM} (kV)	$R_{ON}*C_{ESD}$ (Ω-fF)	I_{CP}/C_{ESD} (mA/fF)	V_{HBM}/C_{ESD} (V/fF)	I_{CP}/A_{Layout} (mA/μm²)
Waffle	A	2.84	0.158	10.148	0.178	0.3	28.82	55.63	105.63	11.20
	B	8.01	0.416	3.980	0.476	0.8	31.88	51.94	99.88	16.58
	C	59.44	2.100	0.871	2.361	3.8	51.77	35.33	63.93	20.93
	D	88.00	2.777	0.738	2.890	4.8	64.94	31.56	54.55	19.62
	E	123.09	3.328	0.694	3.536	5.5	85.42	27.04	44.68	17.54
Multi-waffle	C	39.56	1.862	0.819	2.252	3.7	32.40	47.07	93.53	18.56
	D	58.02	2.722	0.699	3.096	5.1	40.56	46.91	87.90	19.24
	E	78.76	3.561	0.601	3.902	6.5	47.33	45.21	82.53	18.77
Multi-waffle-hollow	C	40.51	1.790	0.821	2.229	3.6	33.26	44.19	88.87	17.84
	D	53.31	2.531	0.709	3.017	5.0	37.80	47.48	93.79	17.89
	E	66.03	3.258	0.620	3.752	6.2	40.94	49.34	93.90	17.17

Table 2.6

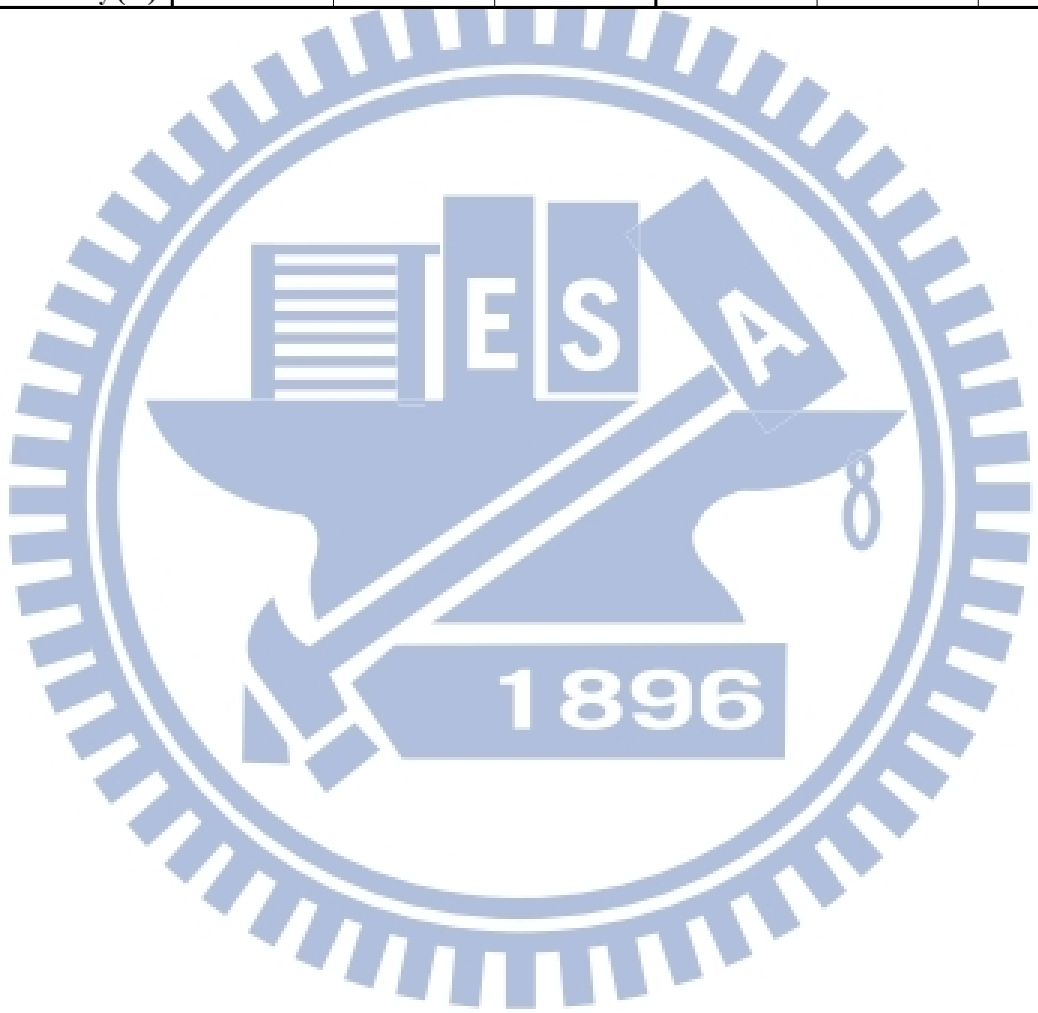
Measured Results and Figures-of-Merit of $P+/N_{well}$ Diodes with Different Layout Styles

Layout Style	Size	C_{ESD} (fF)	I_{CP} (A)	R_{ON} (Ω)	I_{t2} (A)	V_{HBM} (kV)	$R_{ON}*C_{ESD}$ (Ω-fF)	I_{CP}/C_{ESD} (mA/fF)	V_{HBM}/C_{ESD} (V/fF)	I_{CP}/A_{Layout} (mA/μm²)
Waffle	A	2.84	0.158	10.148	0.178	0.3	28.82	55.63	105.63	11.20
	B	8.01	0.416	3.980	0.476	0.8	31.88	51.94	99.88	16.58
	C	59.44	2.100	0.871	2.361	3.8	51.77	35.33	63.93	20.93
	D	88.00	2.777	0.738	2.890	4.8	64.94	31.56	54.55	19.62
	E	123.09	3.328	0.694	3.536	5.5	85.42	27.04	44.68	17.54
Multi-waffle	C	39.56	1.862	0.819	2.252	3.7	32.40	47.07	93.53	18.56
	D	58.02	2.722	0.699	3.096	5.1	40.56	46.91	87.90	19.24
	E	78.76	3.561	0.601	3.902	6.5	47.33	45.21	82.53	18.77
Multi-waffle-hollow	C	40.51	1.790	0.821	2.229	3.6	33.26	44.19	88.87	17.84
	D	53.31	2.531	0.709	3.017	5.0	37.80	47.48	93.79	17.89
	E	66.03	3.258	0.620	3.752	6.2	40.94	49.34	93.90	17.17

Table 2.7

Line Current Density of Diode Devices from Multi-Waffle to Multi-Waffle-Hollow

Layout Style	**From Multi-waffle to Multi-waffle-hollow**											
Diode	**$N+/P_{sub}$**						**$P+/N_{well}$**					
Size	**C**	**C**	**D**	**D**	**E**	**E**	**C**	**C**	**D**	**D**	**E**	**E**
I_{CP} (A)	1.862	1.790	2.722	2.531	3.561	3.258	2.083	2.053	2.835	2.773	3.512	3.364
Junction Perimeter (μm)	112.0	112.0	140.0	140.0	168.0	168.0	112.0	112.0	140.0	140.0	168.0	168.0
Line Current Density (mA/μm)	16.63	15.98	19.44	18.08	21.20	19.39	18.60	18.33	20.25	19.81	20.90	20.02
Reduction Percentage of Line Current Density (%)	3.91		7.00		8.54		1.45		2.17		4.21	



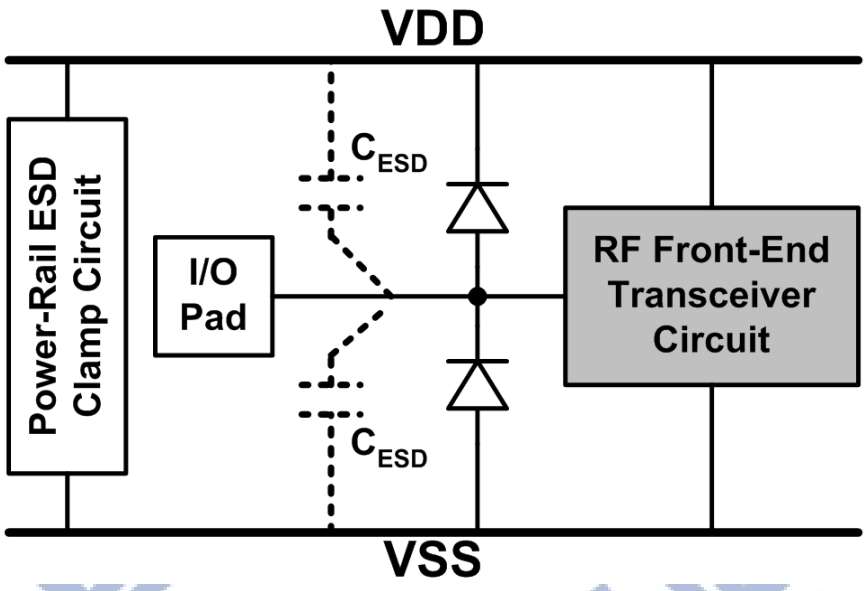


Fig. 2.1 Typical ESD protection scheme with double diodes for RF front-end or high-speed I/O applications.

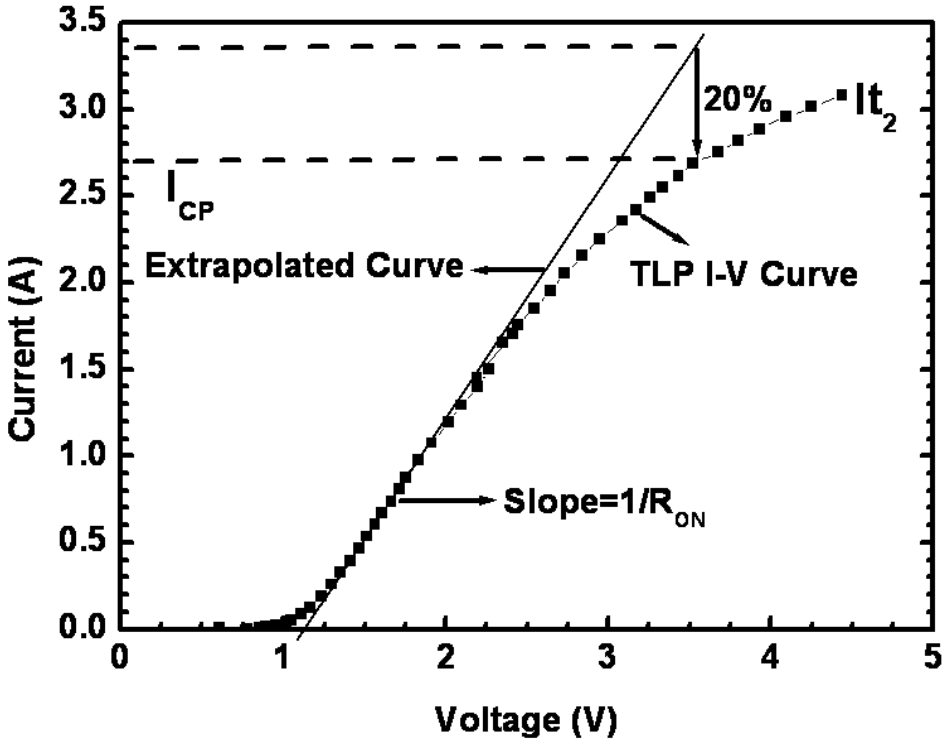


Fig. 2.2 The measured TLP *I-V* curve of the ESD protection diode. The current compression point (I_{CP}) is defined as the current level at which the measured *I-V* curve deviates from its linearly extrapolated value by 20%.

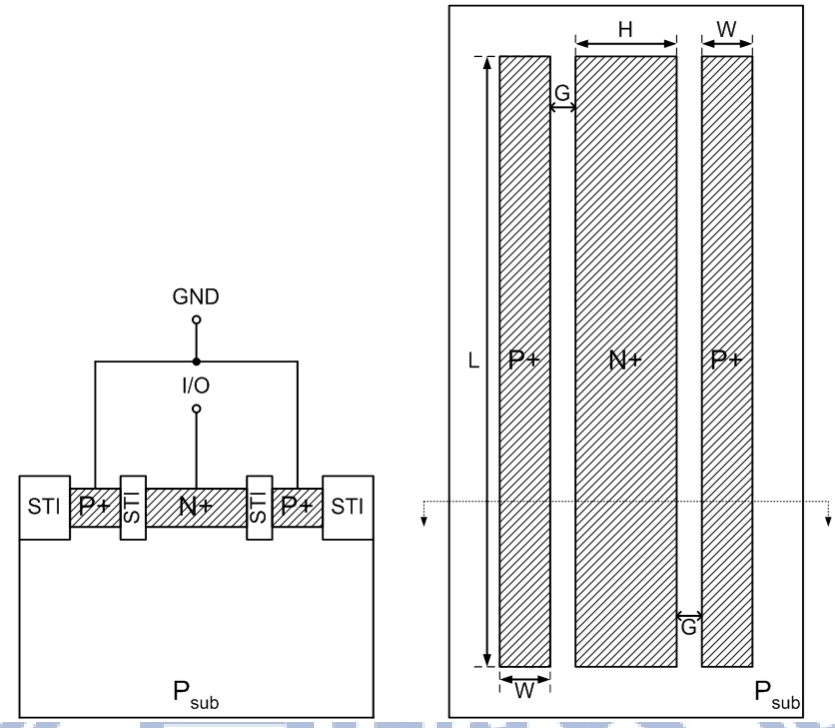
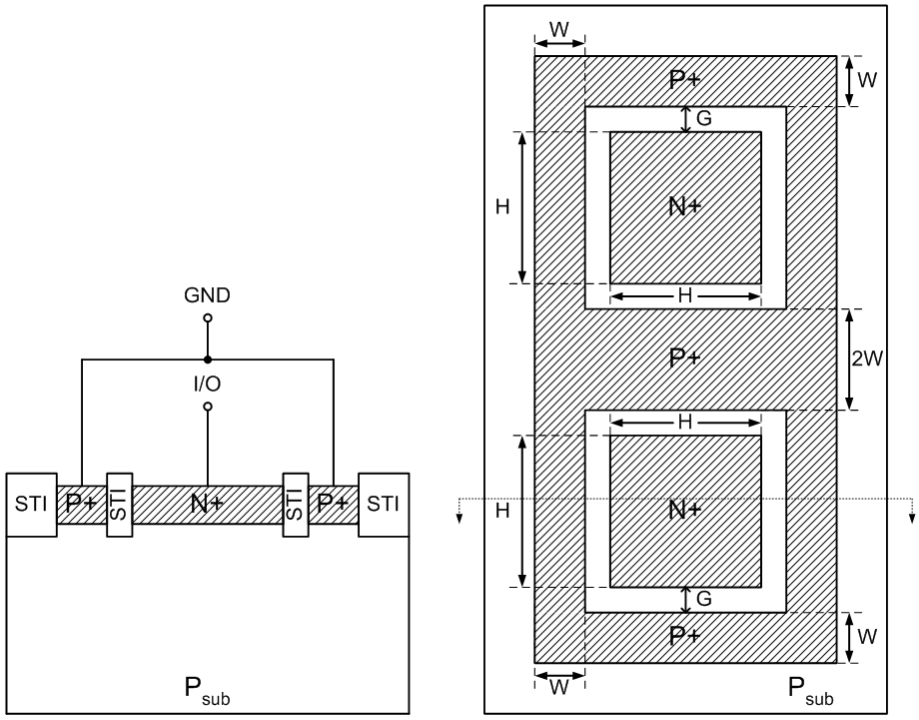
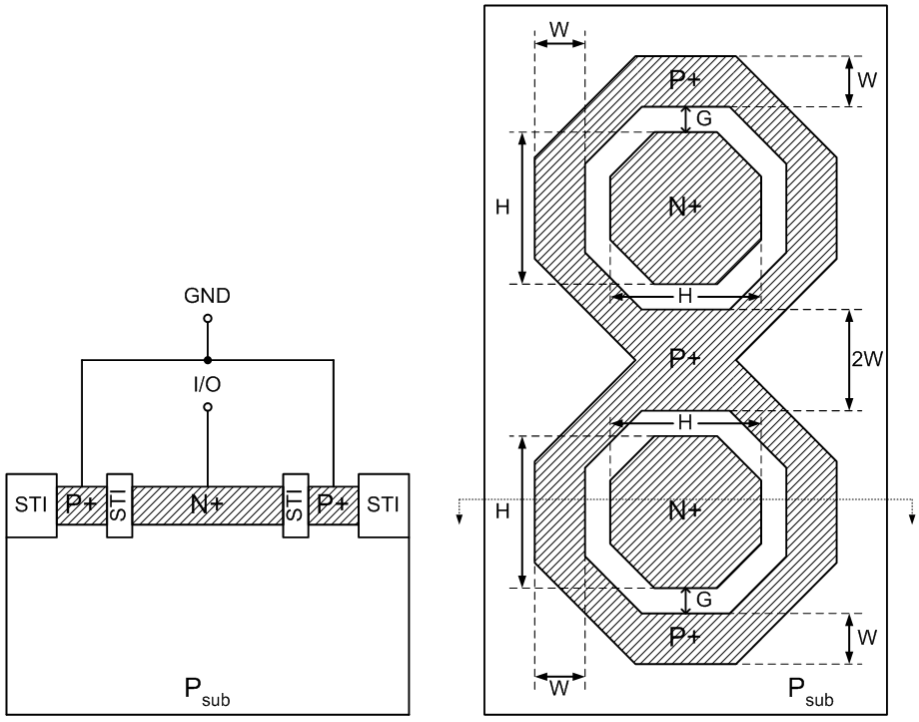


Fig. 2.3 Device cross-sectional view and layout top view of the ESD protection diode with typical stripe layout style.

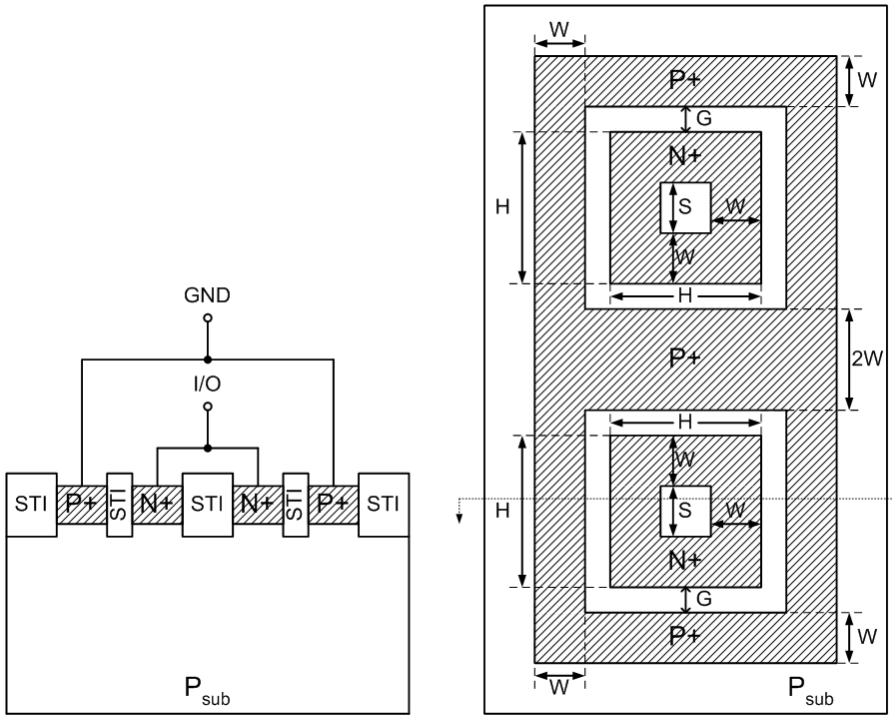


(a)

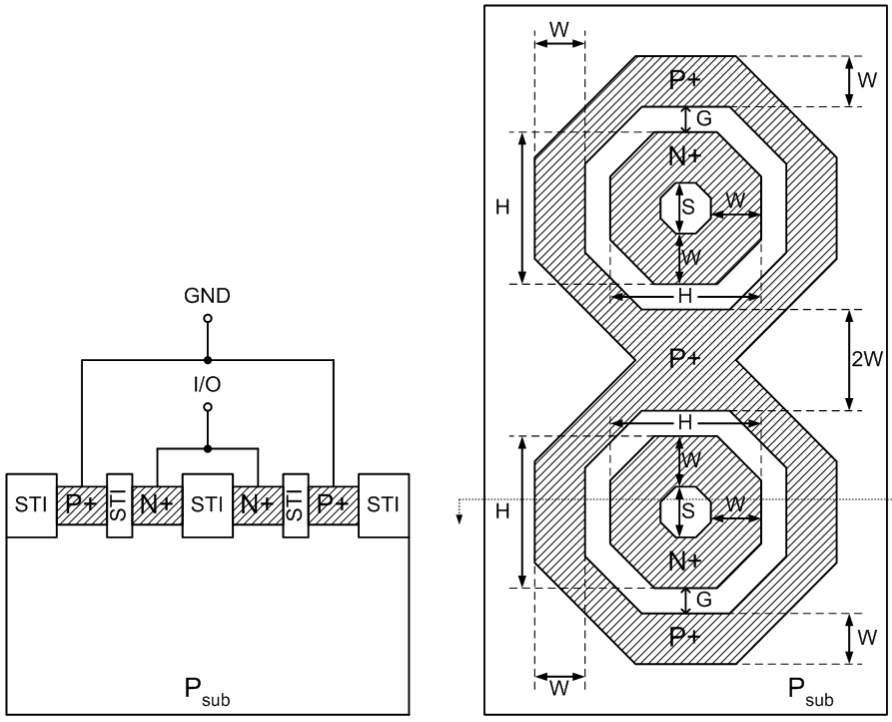


(b)

Fig. 2.4 Device cross-sectional view and layout top view of the ESD protection diodes with (a) waffle layout style and (b) octagon layout style.

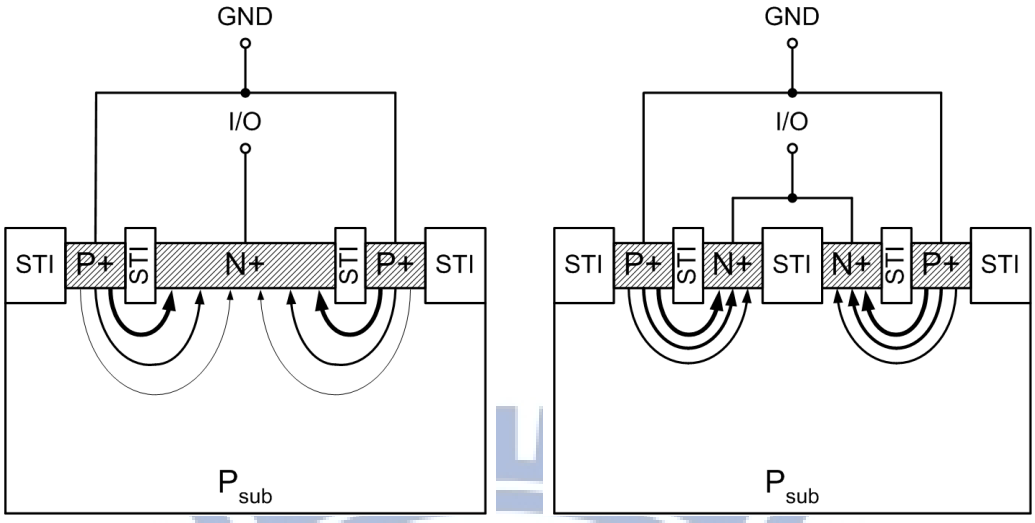


(a)



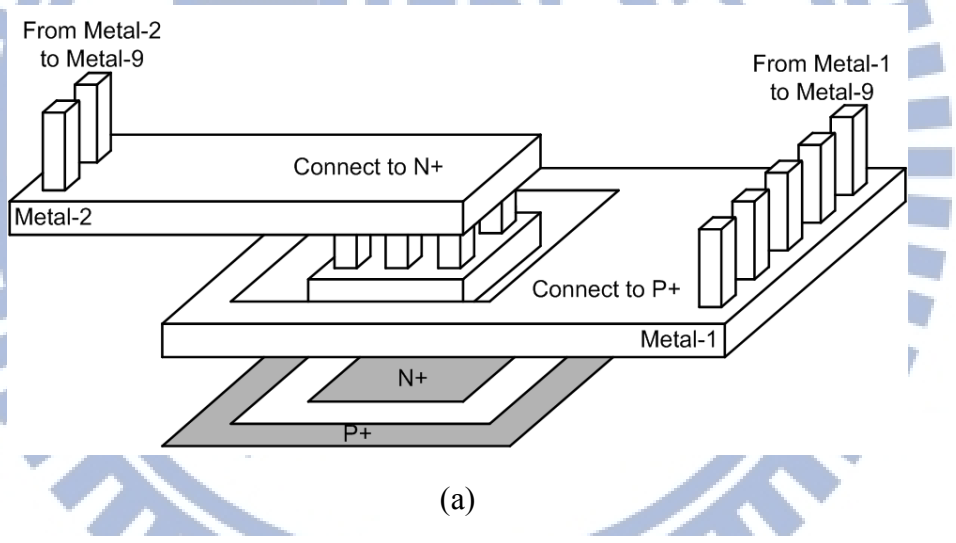
(b)

Fig. 2.5 Device cross-sectional view and layout top view of the ESD protection diodes with (a) waffle-hollow layout style and (b) octagon-hollow layout style. The center region is drawn with the STI region to effectively reduce the parasitic capacitance.

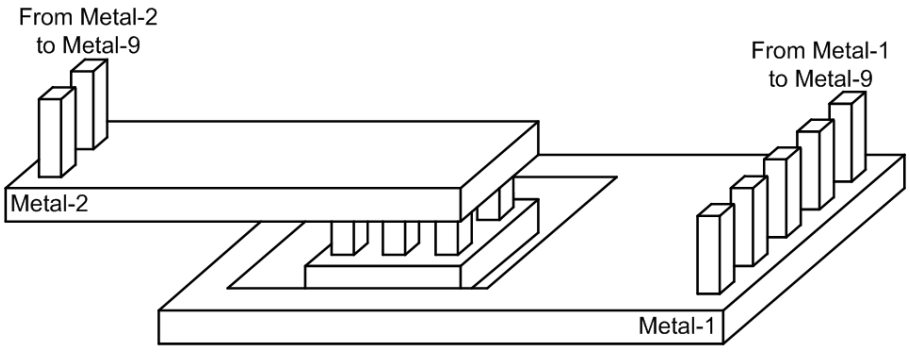


(a) (b)

Fig. 2.6 Device cross-sectional view to explain ESD current flows in the diodes with (a) waffle layout style and (b) waffle-hollow layout style.



(a)



(b)

Fig. 2.7 The 3D views of metal layer arrangement for (a) interconnect routing of N+/P_{sub} diodes, and (b) the corresponding open pad structure.

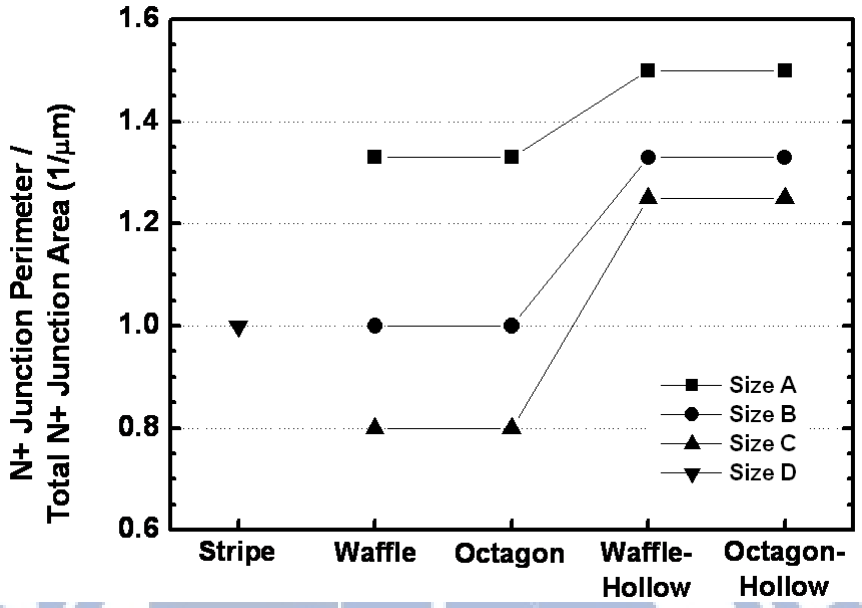
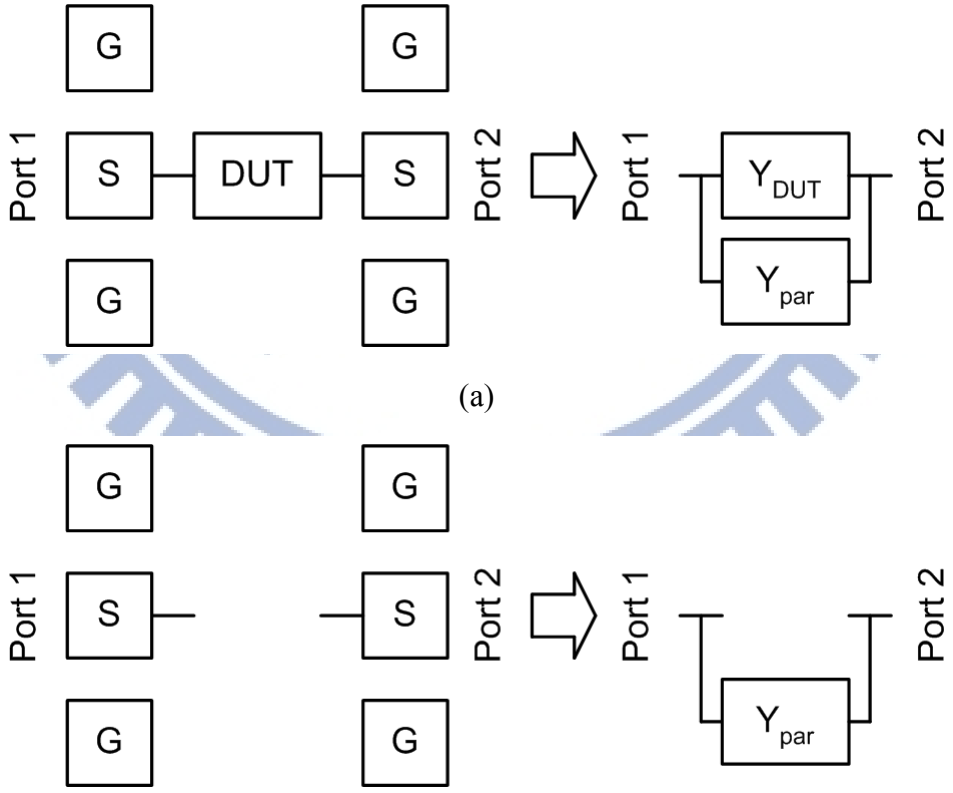


Fig. 2.8 The performance evaluations with the factors of N+ junction perimeter / total N+ junction area under different diode layout styles.



(a)

(b)

Fig. 2.9 Layout top views for de-embedded calculation to extract the parasitic capacitance of the fabricated ESD diodes with (a) including-DUT pattern and (b) excluding-DUT pattern.

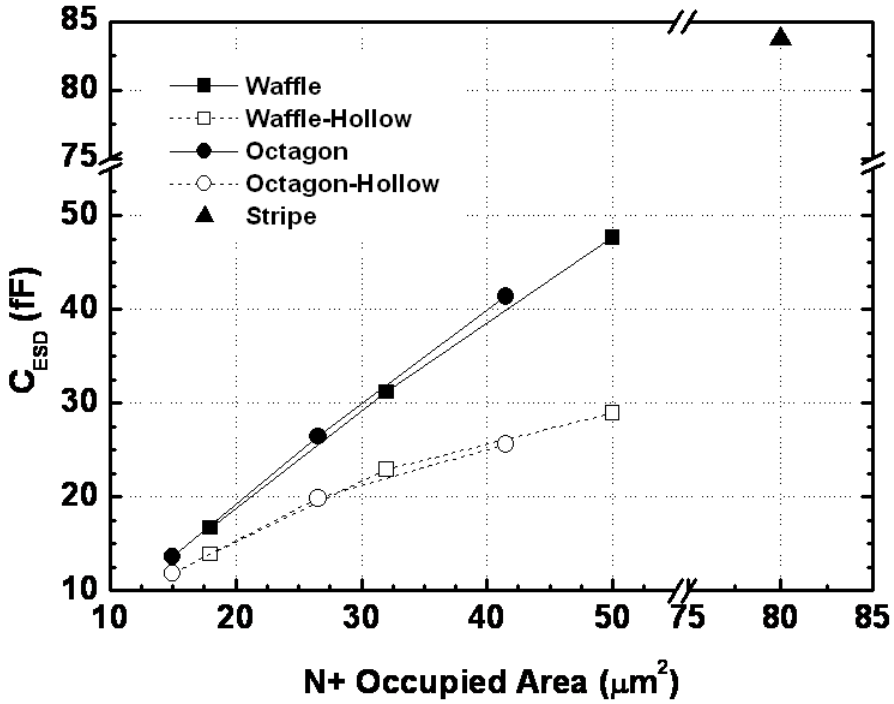


Fig. 2.10 Dependence of C_{ESD} extracted from *S*-parameter at 2.5GHz under zero DC bias on the N+ occupied area of diode devices with different layout styles.

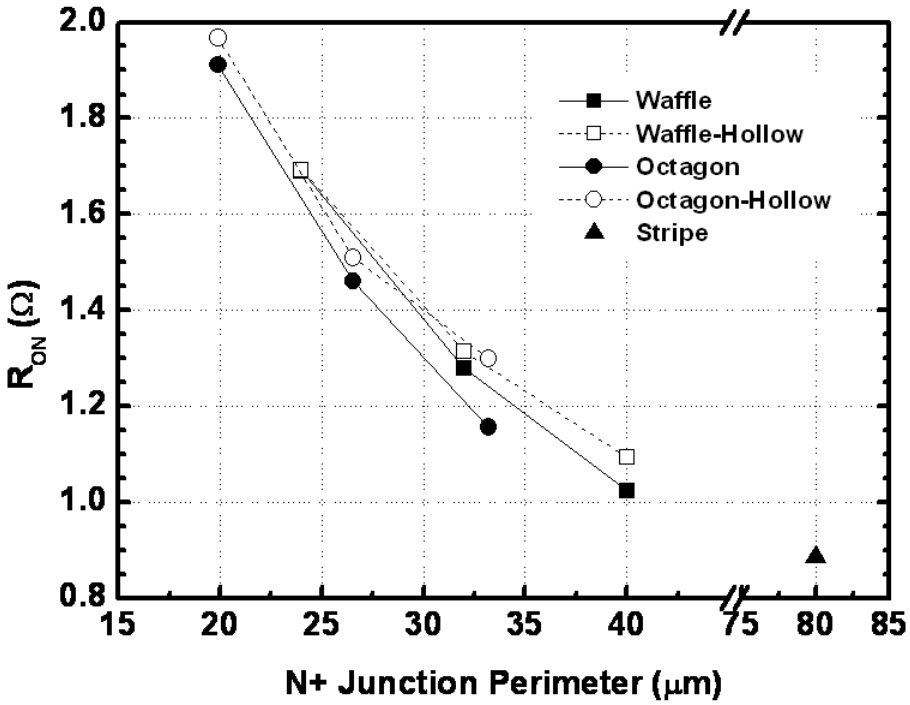


Fig. 2.11 Dependence of TLP-measured R_{ON} on the N+ junction perimeter of diode devices with different layout styles.

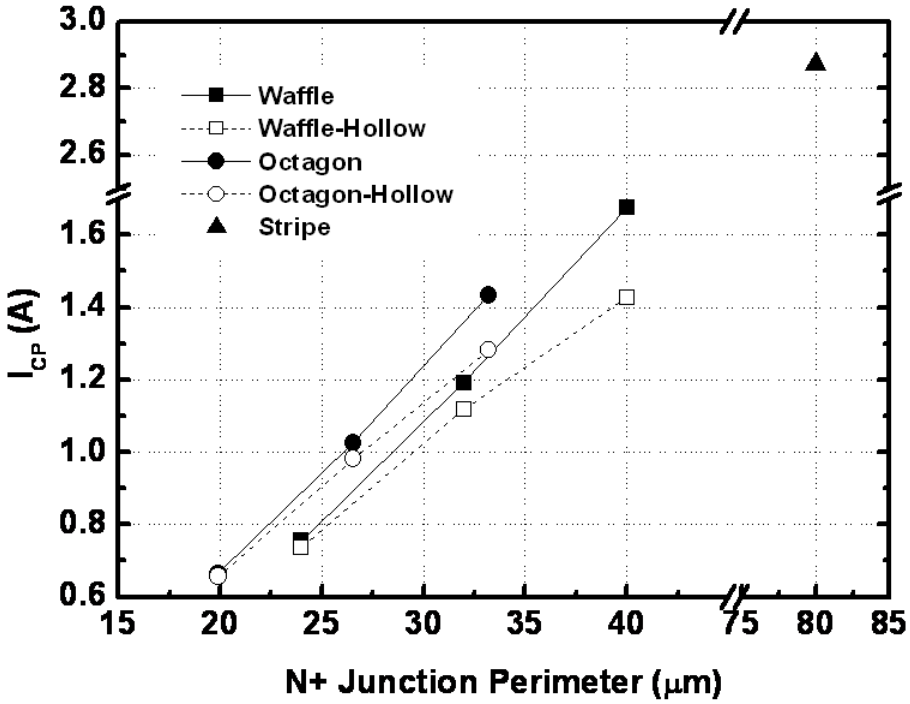
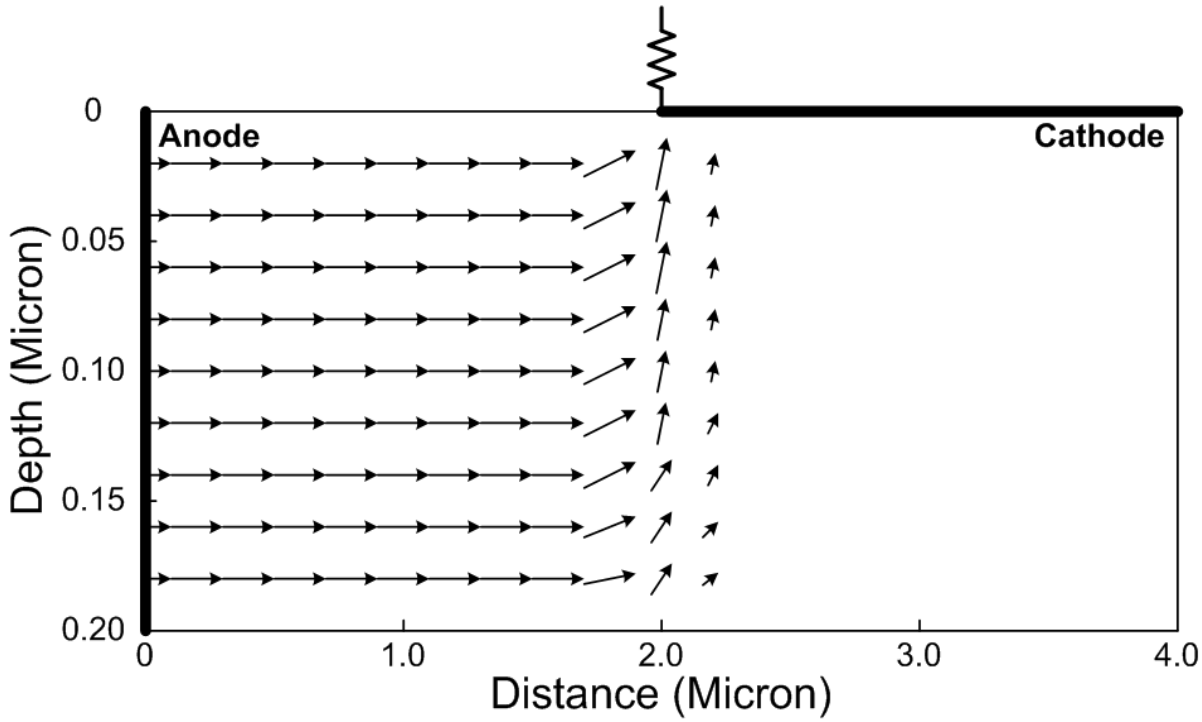
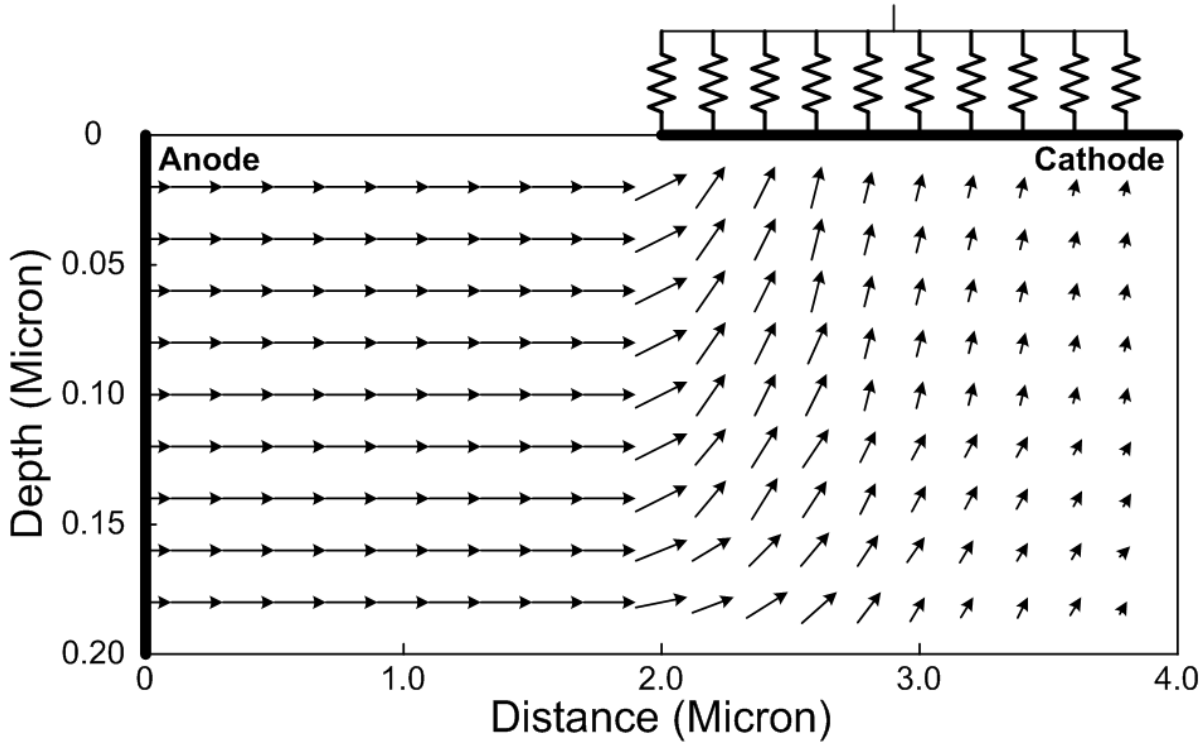


Fig. 2.12 Dependence of TLP-measured I_{CP} on the N+ junction perimeter of diode devices with different layout styles.



(a)



(b)

Fig. 2.13 The simulated vectors of ESD discharging current along the cross section of waffle diode with a (a) small, and (b) large, device size.

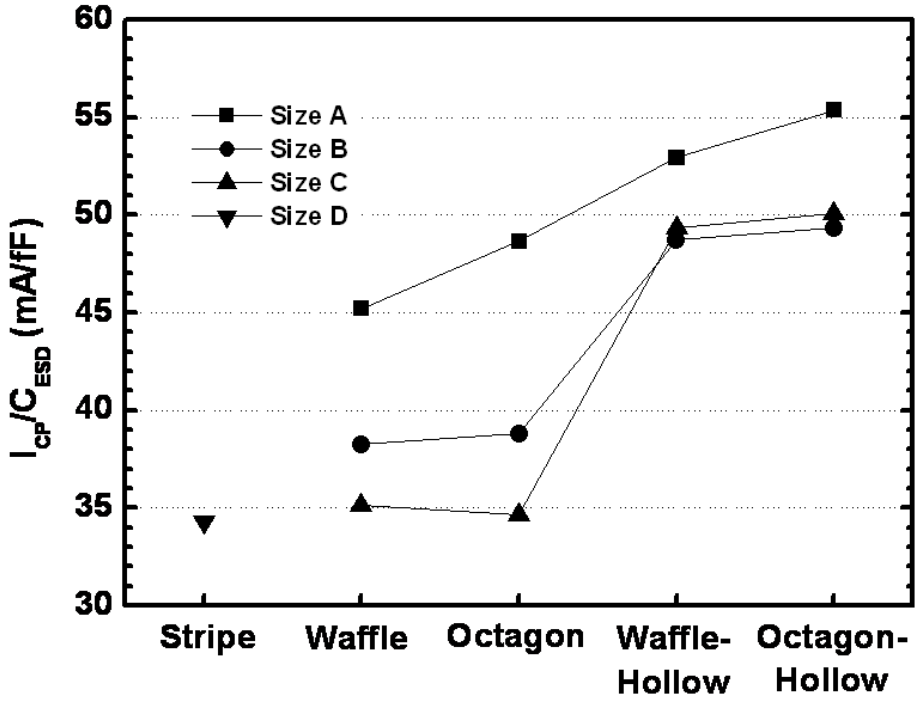


Fig. 2.14 The (I_{CP}/C_{ESD}) FOM of ESD protection diodes with different layout styles.

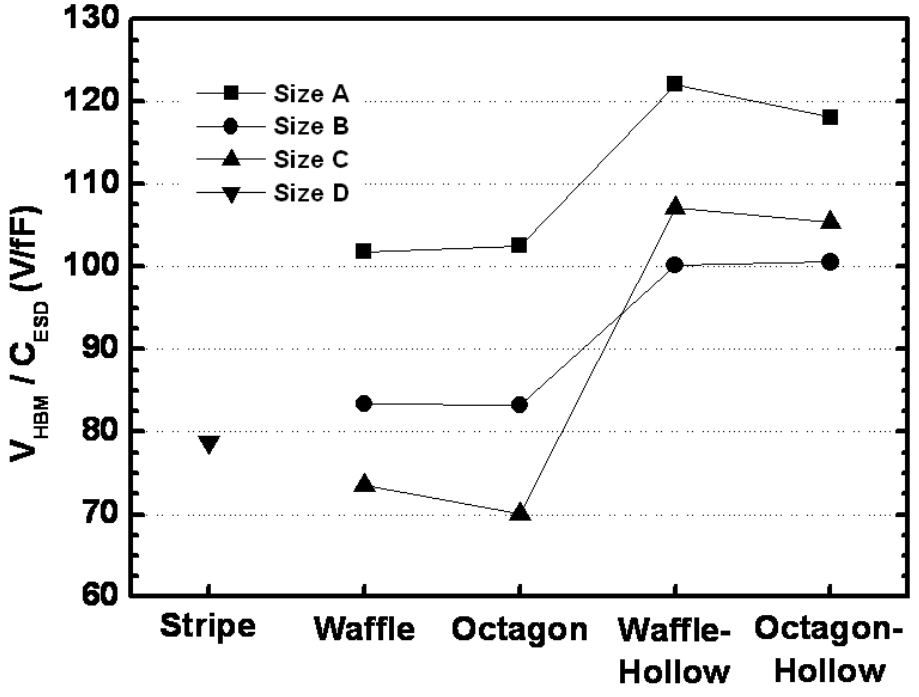


Fig. 2.15 The (V_{HBM}/C_{ESD}) FOM of ESD protection diodes with different layout styles.

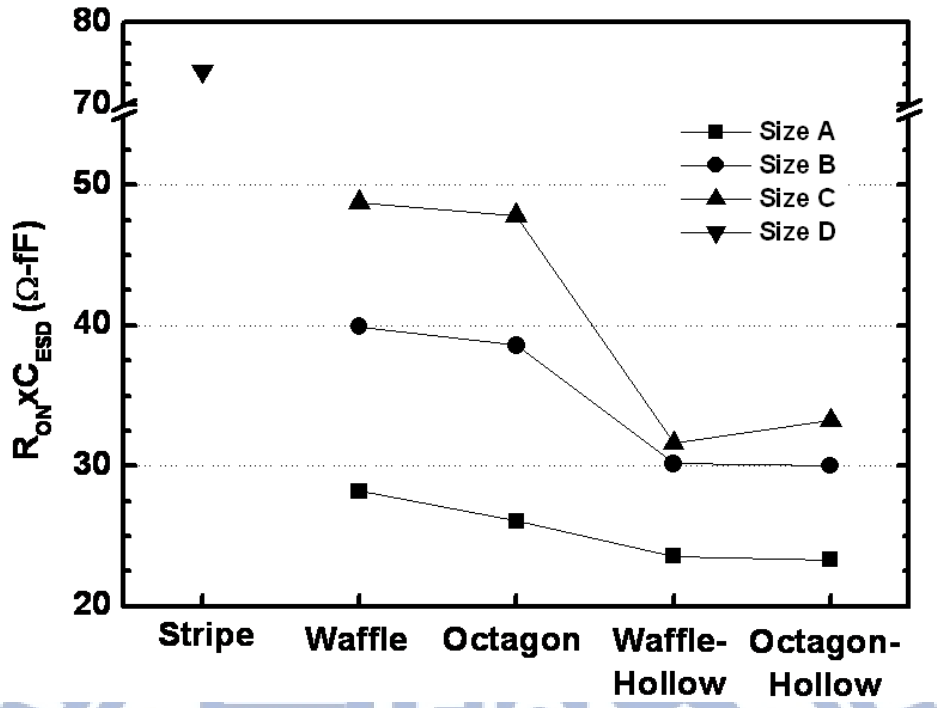


Fig. 2.16 The (R_{ON}×C_{ESD}) FOM of ESD protection diodes with different layout styles.

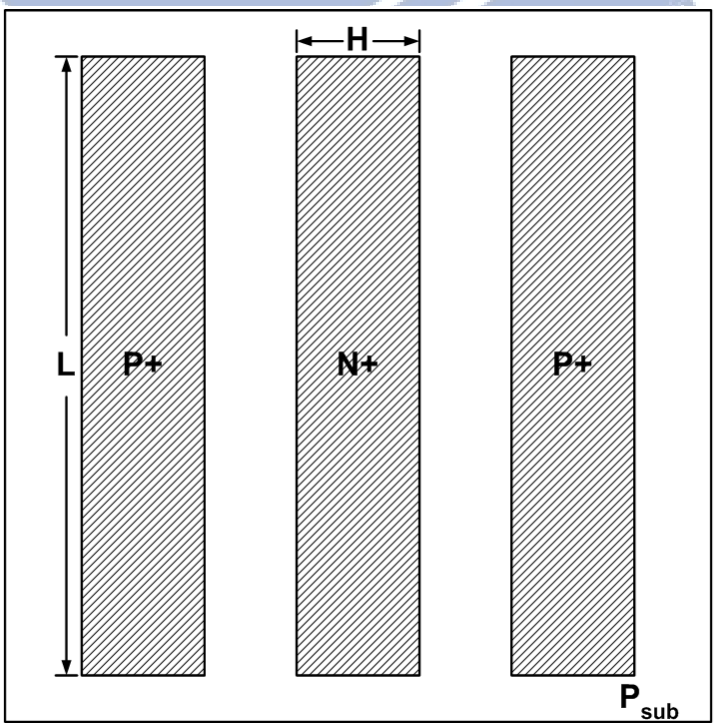
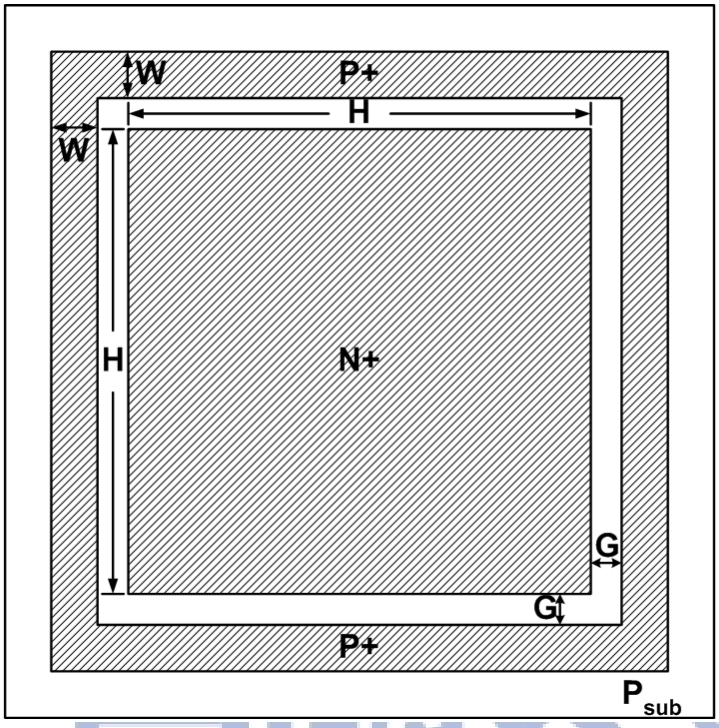
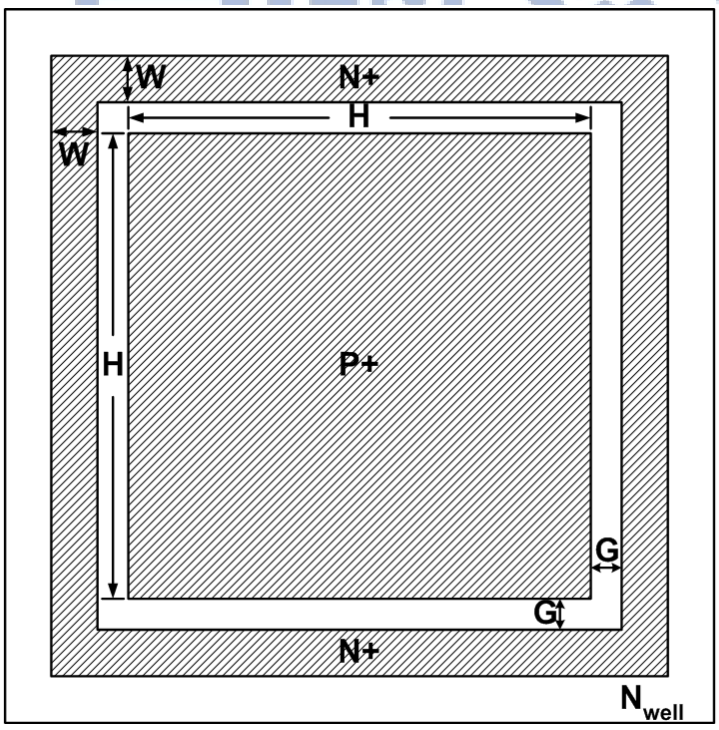


Fig. 2.17 STI-bound N+/P_{sub} ESD protection diode with typical stripe layout style. The major current conduction path of the stripe diode occurs along the length (L) of the diode.

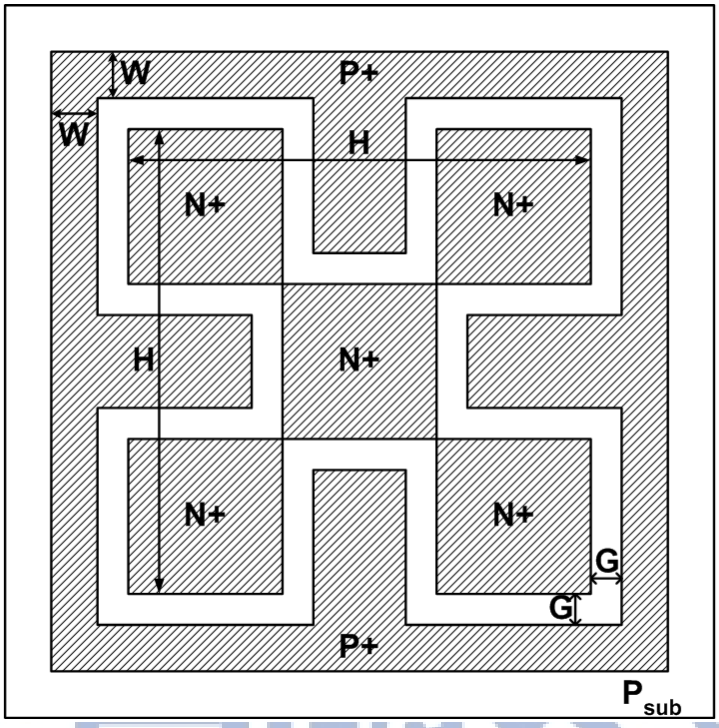


(a)

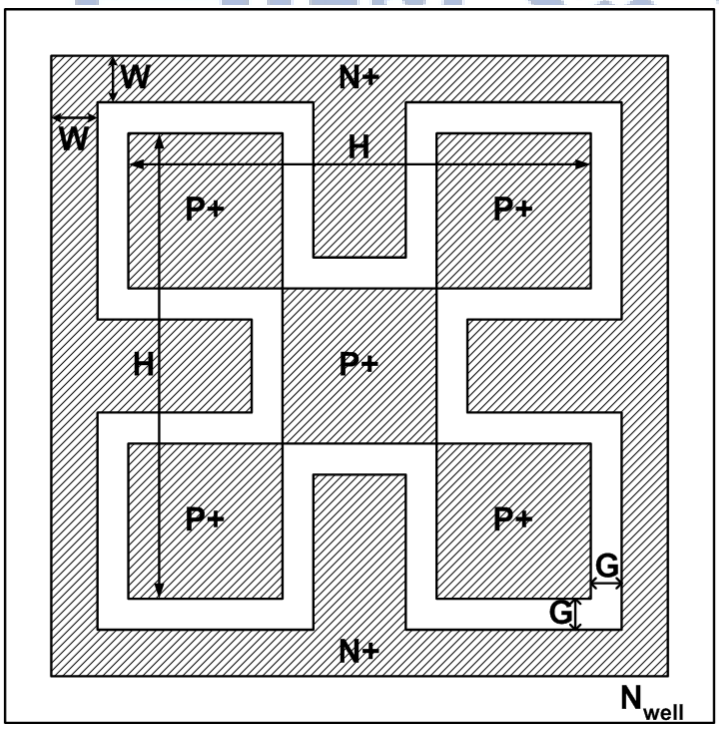


(b)

Fig. 2.18 Layout top view of the STI-bound (a) N+/P_{sub} ESD protection diode and (b) P+/N_{well} ESD protection diode with waffle layout style.

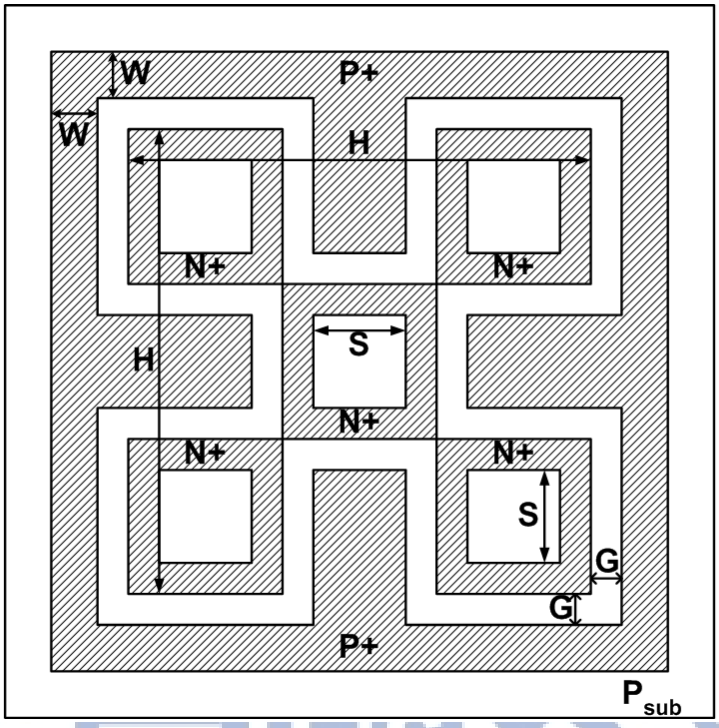


(a)

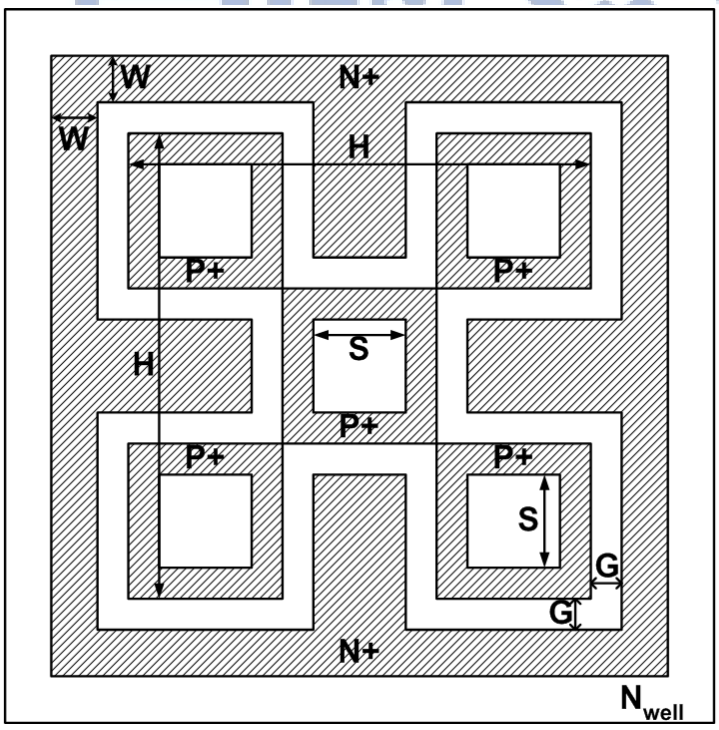


(b)

Fig. 2.19 Layout top view of the STI-bound (a) N+/P_{sub} ESD protection diode and (b) P+/N_{well} ESD protection diode with multi-waffle layout style.



(a)



(b)

Fig. 2.20 Layout top view of the STI-bound (a) N+/P_{sub} ESD protection diode and (b) P+/N_{well} ESD protection diode with multi-waffle-hollow layout style. The N+ (P+) center diffusion region of N+/P_{sub} (P+/N_{well}) diode with multi-waffle-hollow layout style is removed to reduce the parasitic capacitance.

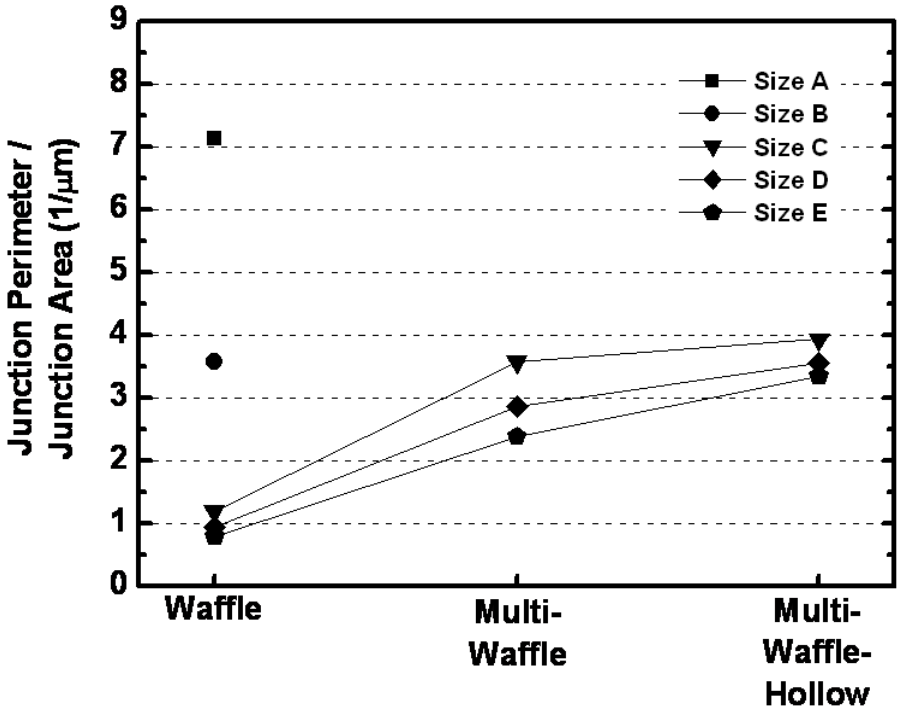
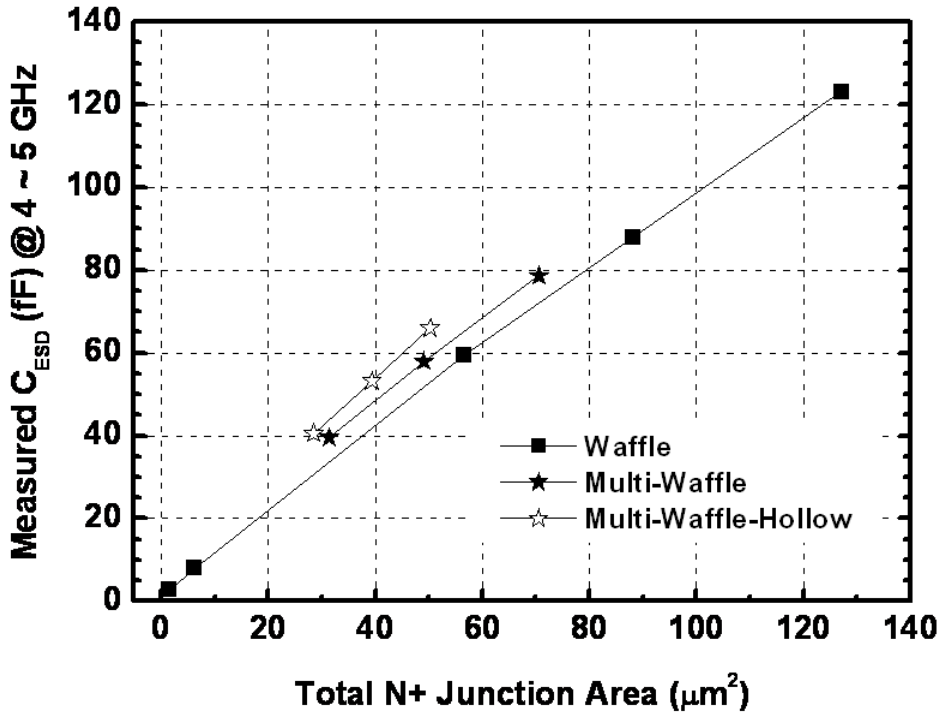
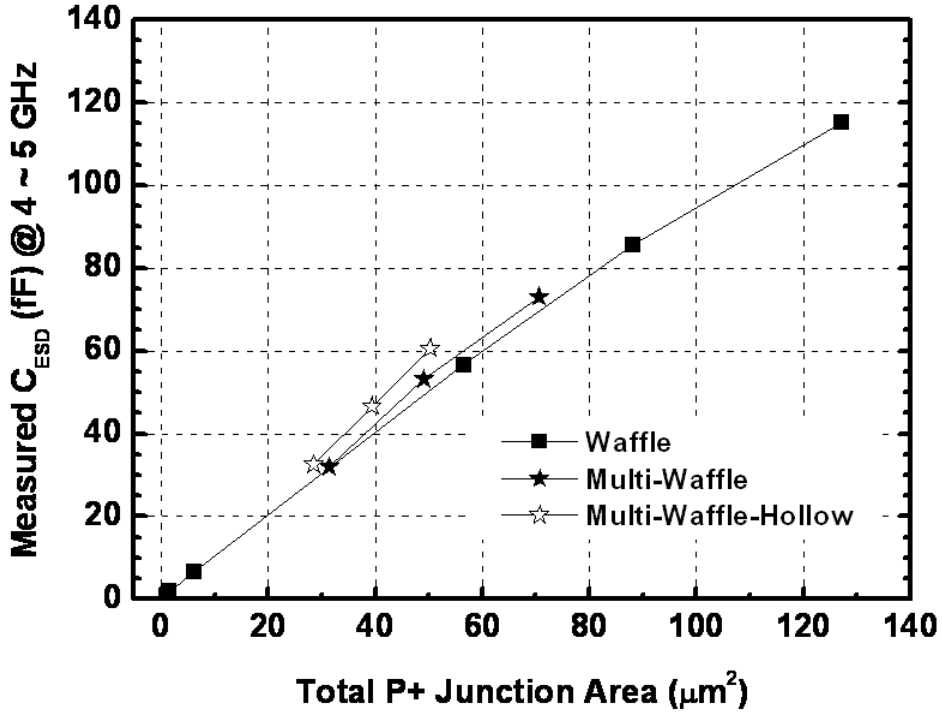


Fig. 2.21 The performance evaluations with the ratio of (junction perimeter) / (junction area) under different layout styles.

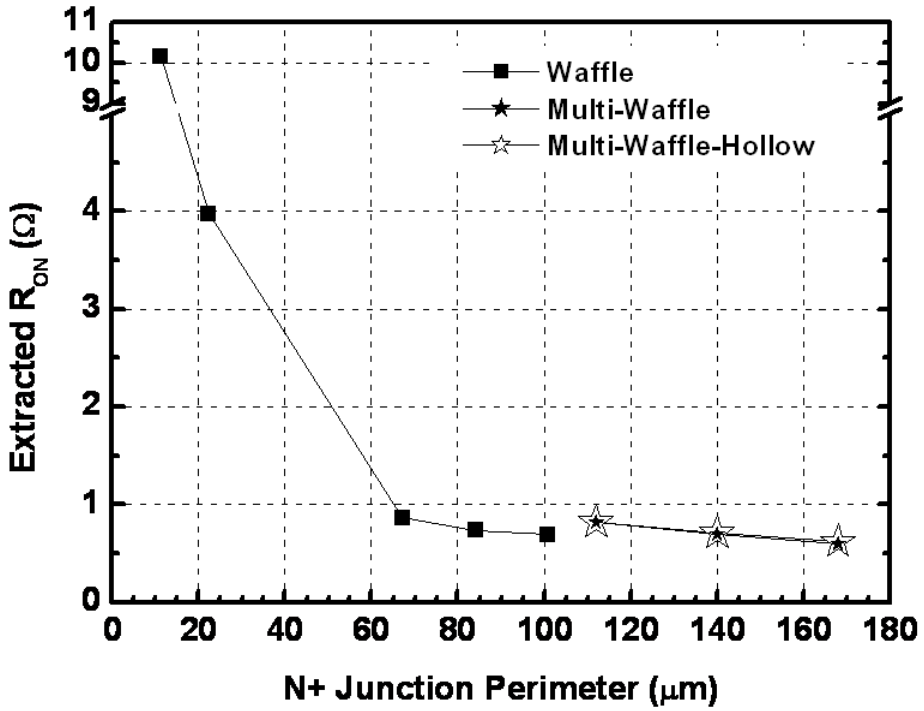


(a)

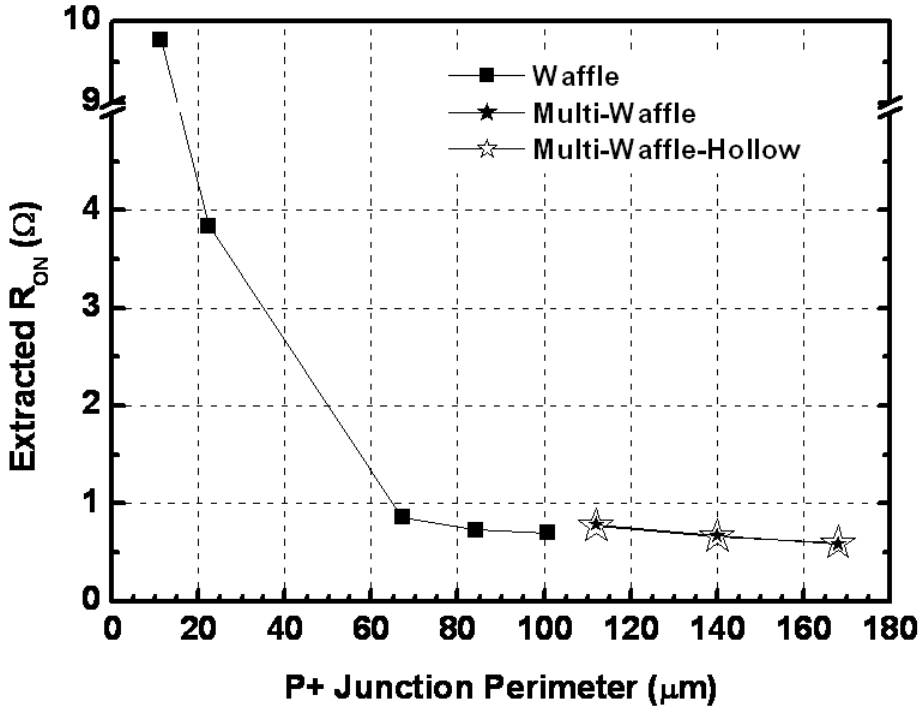


(b)

Fig. 2.22 Dependence of measured C_{ESD} extracted from *S*-parameter from 4 to 5GHz under zero DC bias on the (a) total N+ junction area of N+/P_{sub} diodes and (b) total P+ junction area of P+/N_{well} diodes with different layout styles.

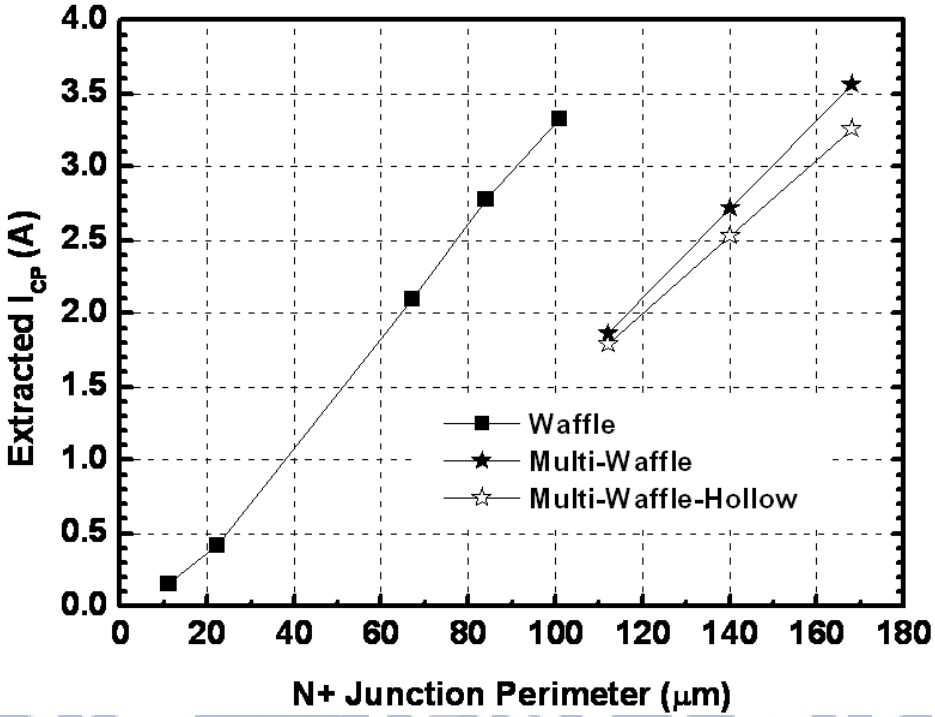


(a)

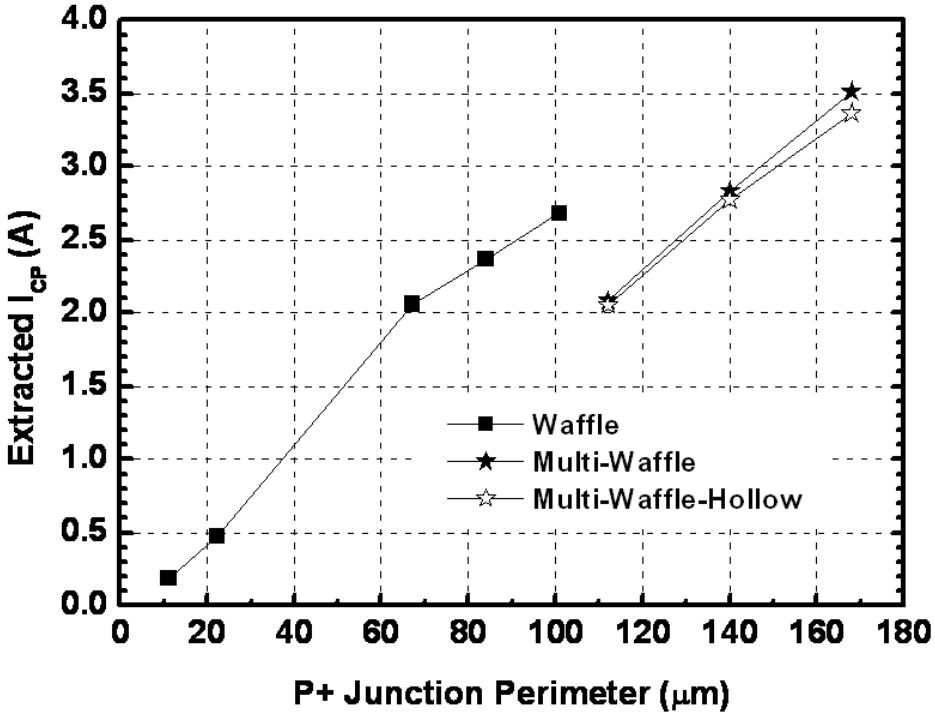


(b)

Fig. 2.23 Dependence of extracted on-resistance R_{ON} on the (a) N+ junction perimeter of $N+/P_{sub}$ diodes and (b) P+ junction perimeter of $P+/N_{well}$ diodes with different layout styles.

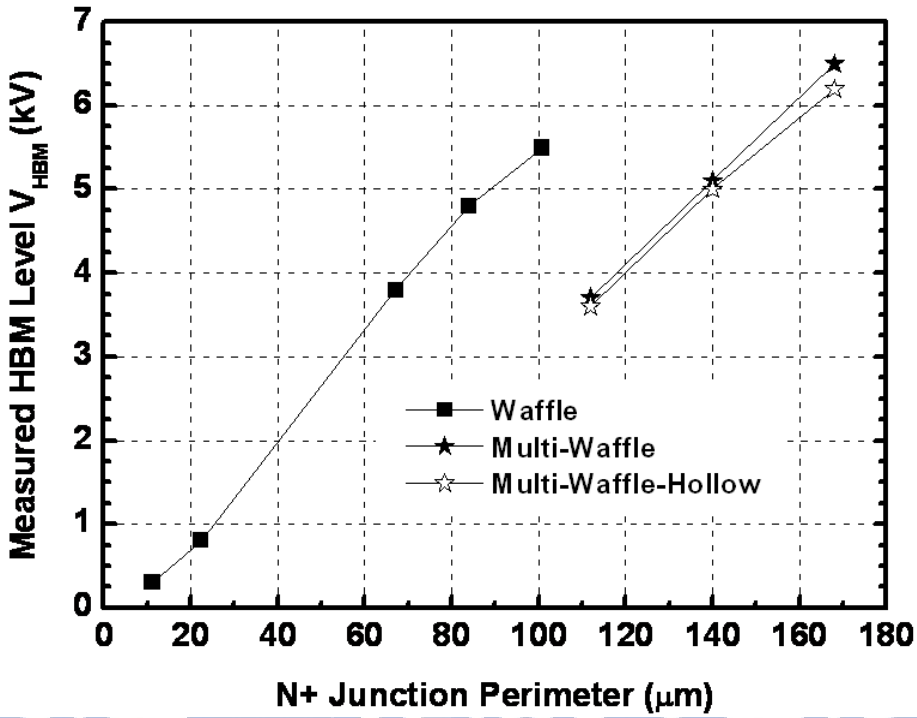


(a)

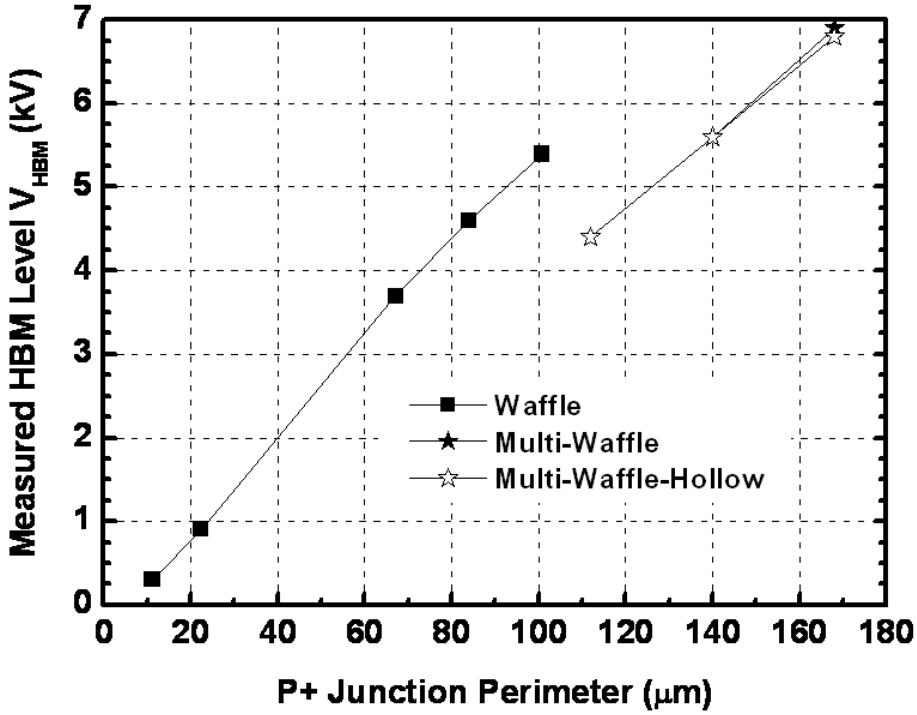


(b)

Fig. 2.24 Dependence of extracted current compression point I_{CP} on the (a) N+ junction perimeter of N+/P_{sub} diodes and (b) P+ junction perimeter of P+/N_{well} diodes with different layout styles.

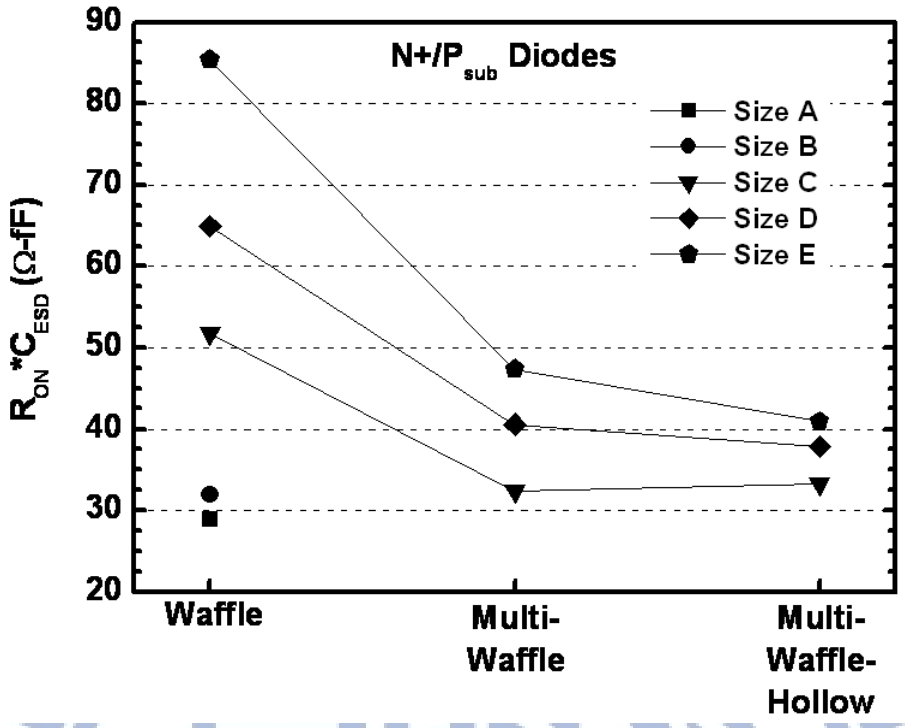


(a)

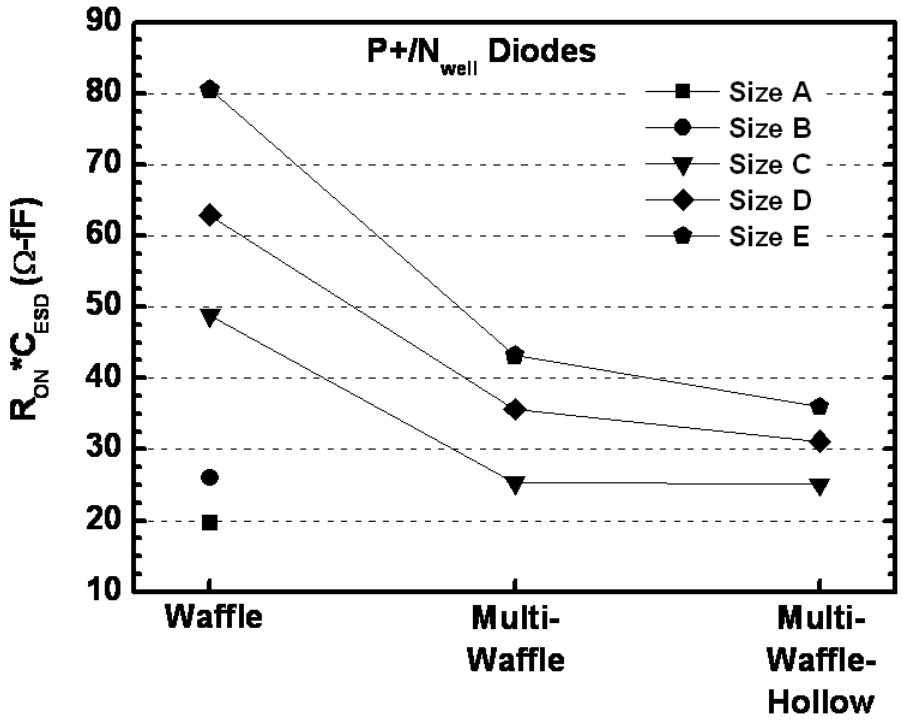


(b)

Fig. 2.25 Dependence of measured HBM level V_{HBM} on the (a) N+ junction perimeter of $N+/P_{sub}$ diodes and (b) P+ junction perimeter of $P+/N_{well}$ diodes with different layout styles.

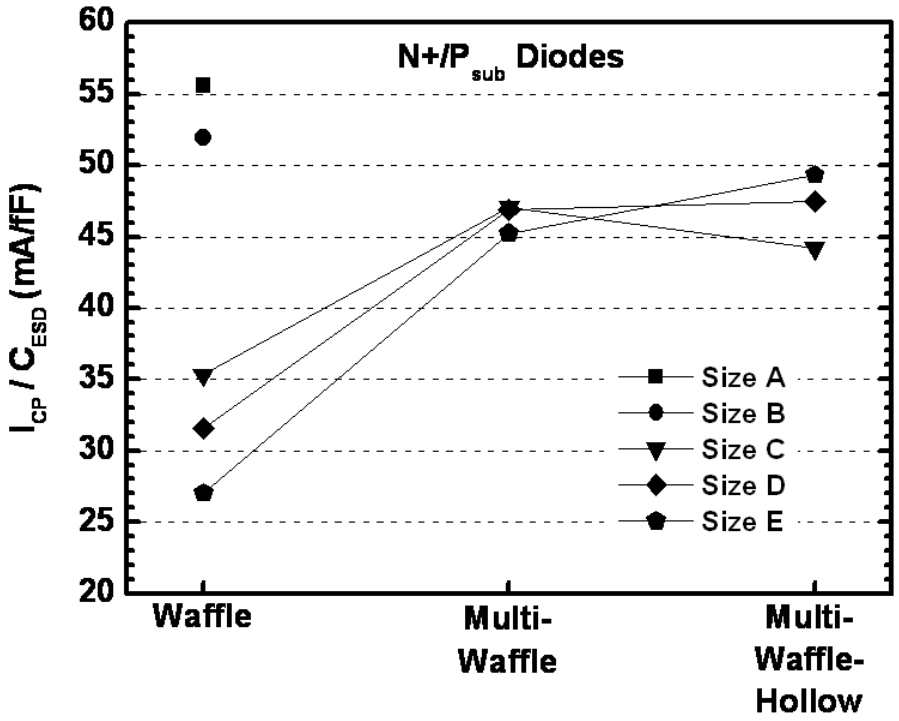


(a)

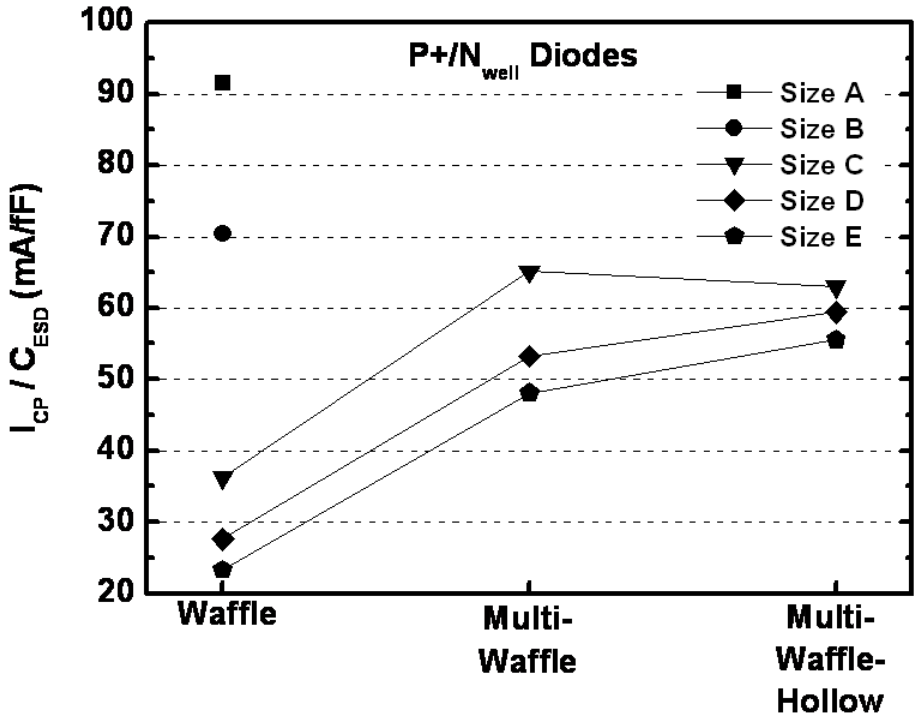


(b)

Fig. 2.26 The exact values of $R_{ON}*C_{ESD}$ of the (a) $N+/P_{sub}$ diodes and (b) $P+/N_{well}$ diodes with different layout styles.

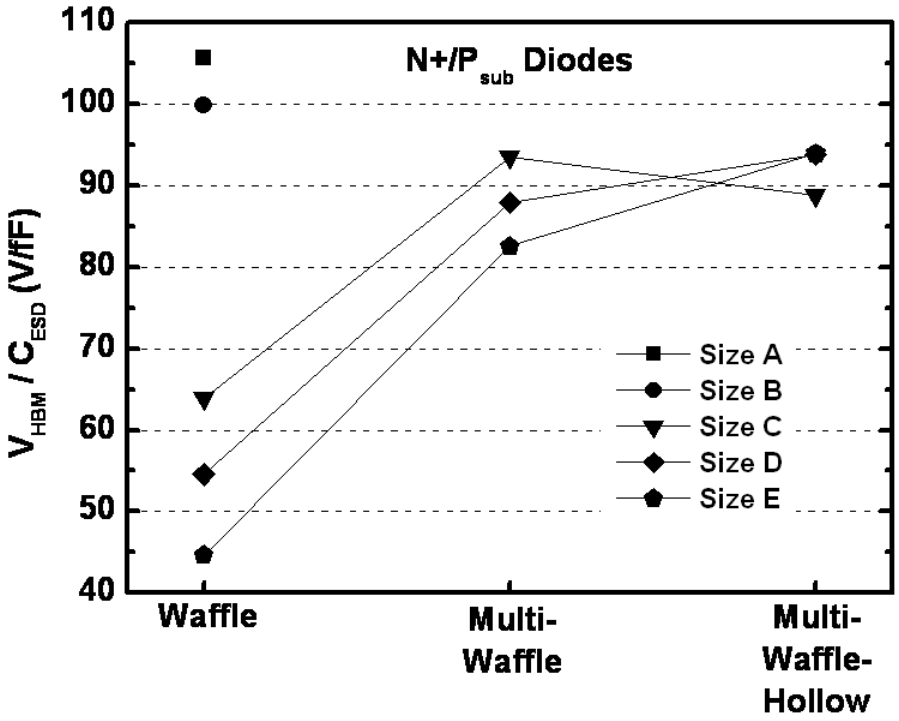


(a)

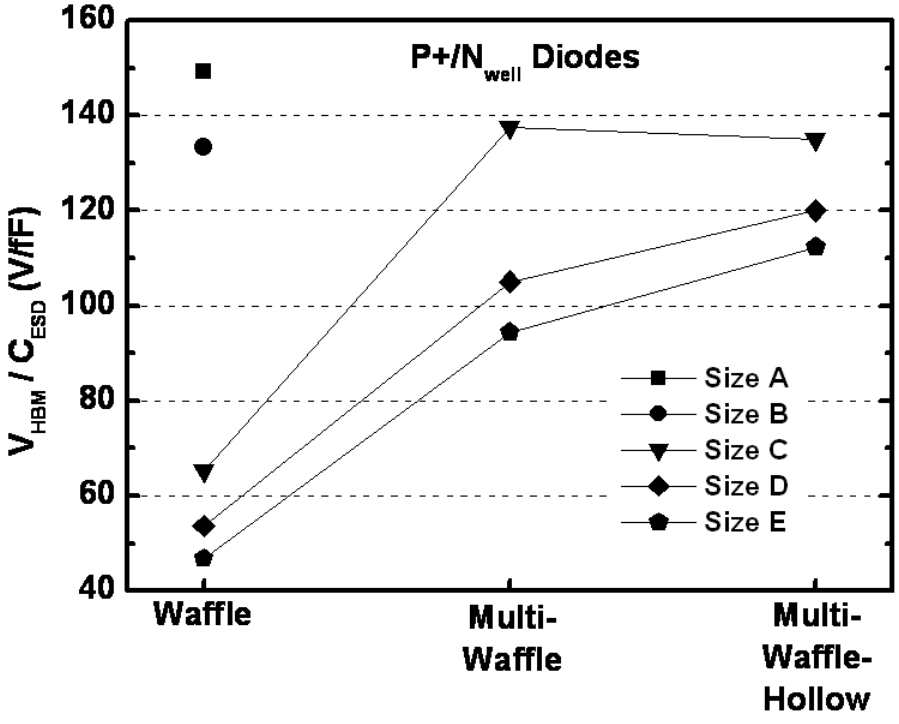


(b)

Fig. 2.27 The exact values of I_{CP}/C_{ESD} of the (a) N+/P_{sub} diodes and (b) P+/N_{well} diodes with different layout styles.

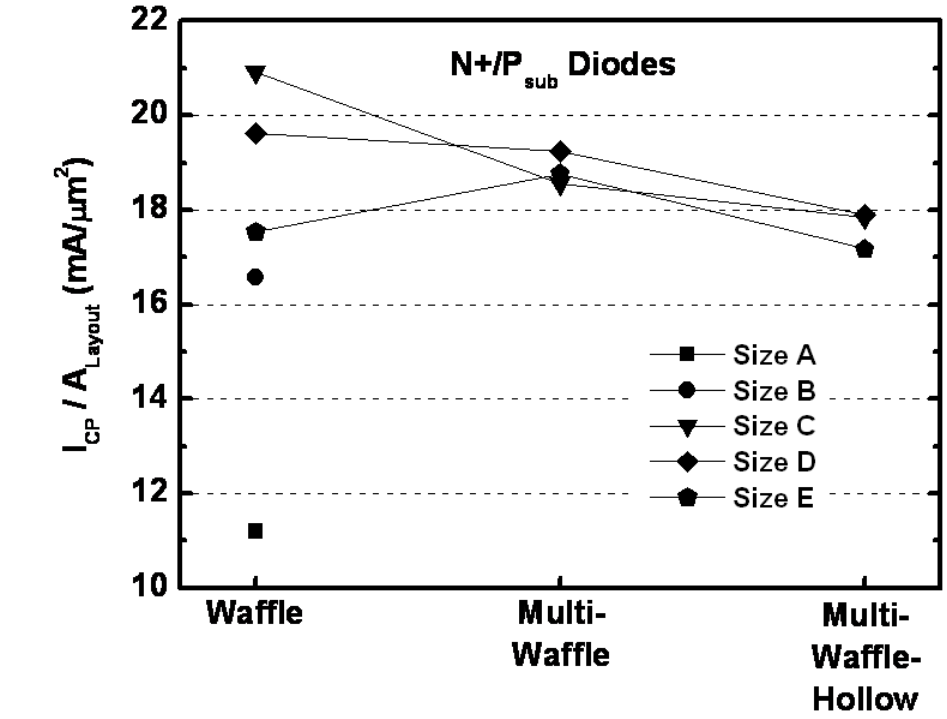


(a)

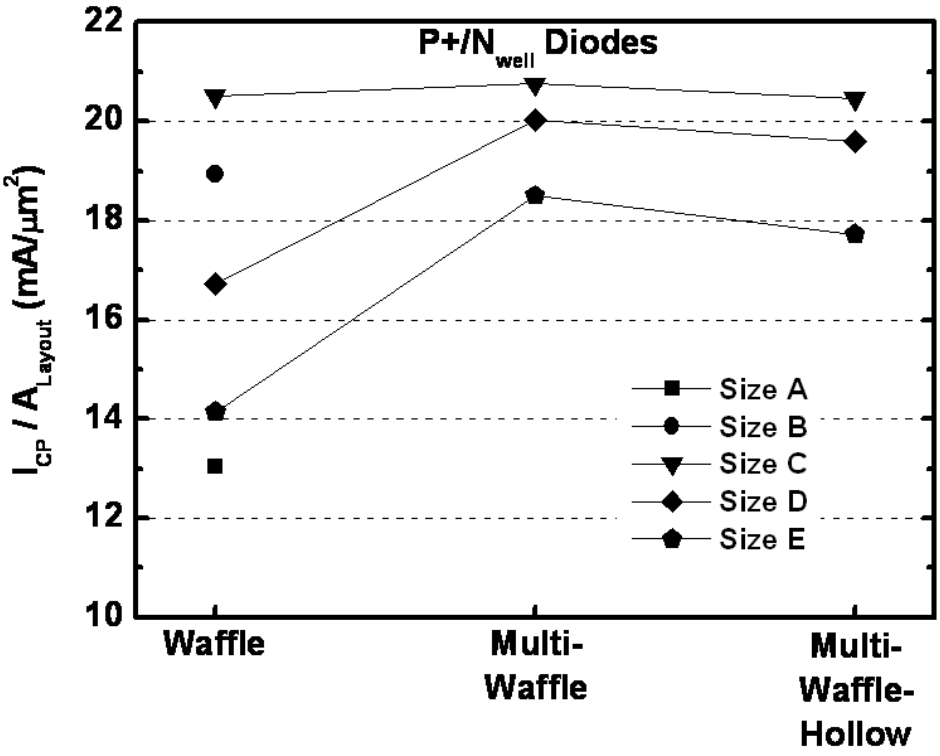


(b)

Fig. 2.28 The FOM V_{HBM}/C_{ESD} of the (a) $N+/P_{sub}$ diodes and (b) $P+/N_{well}$ diodes with different layout styles.



(a)



(b)

Fig. 2.29 The FOM I_{CP}/A_{Layout} of the (a) $N+/P_{sub}$ diodes and (b) $P+/N_{well}$ diodes with different layout styles.

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Chapter 3

Capacitor-Less Design of Power-Rail ESD Clamp Circuit

In this chapter, the capacitor-less design of power-rail ESD clamp circuits are presented. The power-rail ESD clamp circuit with ESD clamp nMOS transistor is investigated in section 3.2, and that with ESD clamp pMOS transistor is discussed in section 3.3. All power-rail ESD clamp circuit with traditional *RC*-based and new proposed designs were fabricated in a 65nm 1.2V fully silicided CMOS process.

3.1 Background

With the continuously scaled-down CMOS technology, ESD protection has become the major concern of reliability for ICs in nanoscale CMOS technology. The nanoscale device with thinner gate oxide and shallower diffusion junction depth seriously degraded the ESD robustness of ICs and raised the difficulty of ESD protection design for ICs implemented in nanoscale CMOS technology [4], [11]. In order to sustain the required ESD robustness, such as 2kV in HBM [1] and 200V in MM [2], the power-rail ESD clamp circuit is an important element to achieve whole-chip ESD protection for ICs [8], [32]. The power-rail ESD clamp circuit is vital for ESD protection under V_{DD}-to-V_{SS} (or V_{SS}-to-V_{DD}) ESD stress, as well as different ESD stress conditions from the input/output to V_{DD}/V_{SS}, including positive-to-V_{SS} mode (PS-mode), negative-to-V_{SS} mode (NS-mode), positive-to-V_{DD} mode (PD-mode), and negative-to-V_{DD} mode (ND-mode), which are illustrated in Figs. 3.1(a) and (b). Therefore, the power-rail ESD clamp circuit can provide efficient protection to the internal circuits of IC products.

In advanced nanoscale CMOS technology, the ESD clamp device drawn in the layout style of big field-effect transistor (BigFET) had demonstrated excellent ESD protection performance [33]-[38]. In these power-rail ESD clamp circuits, the ESD clamp devices can discharge a large ESD current by the inversion channel layer without snapback operation of the parasitic BJT [39]-[42]. The typical power-rail ESD clamp circuit, which was shown in Fig. 3.2 with *RC*-based ESD-transient detection circuit and a controlling circuit, commands the ESD clamp device to turn on under ESD stress conditions and to turn off under normal

circuit operation conditions. Practically, there are two different circuit skills, the *RC*-delay technique [33]-[36] and the capacitance-coupling design [37], [38], to realize the ESD-transient detection circuit in the power-rail ESD clamp circuit. The turn-on duration of the ESD clamp nMOS transistor is mainly controlled by the *RC*-time constant of the *RC*-based ESD-transient detection circuit [33]-[36]. Consequently, the *RC*-time constant would be designed large enough about several hundreds nanosecond to keep the ESD clamp nMOS transistor at "ON" state under the ESD stress condition. However, the extended *RC*-time constant of the ESD-transient detection circuit suffers not only the larger layout area from the resistance and capacitance but also the mis-triggering of the ESD clamp nMOS transistor under fast power-on application [34].

In previous studies [33], [34], [37], [38], they demonstrated the power-rail ESD clamp circuits with feedback circuit methods to extend the turn-on duration by using a small *RC*-time constant. However, the feedback circuit designs would suffer the latch-on issue under the fast power-on or the electrical fast transient (EFT) conditions [43]. Moreover, some circuit designs, such as on-time control circuits [33] and multi-*RC*-triggered circuits [35], had also been used to extend the turn-on duration without the latch-on issue. However, those previous circuits are more complicated with large silicon layout area including the requested resistances and capacitances in the ESD-transient detection circuits.

3.2 Power-Rail ESD Clamp Circuit with ESD Clamp nMOS Transistor

In this section, a new capacitor-less ESD-transient detection circuit, which is combined with the parasitic capacitance of the ESD clamp nMOS transistor drawn in BigFET layout style, has been proposed and verified in 65nm 1.2V CMOS technology. This new design adopts the feedback circuit in cascode structure to achieve desired function for controlling the ESD clamp nMOS transistor. According to the experimental measured results, the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit has revealed a much better performance than that of the traditional *RC*-based power-rail ESD clamp circuit.

3.2.1 ESD-Transient Detection Circuit Scheme

The capacitor-less ESD-transient detection circuits with different number of diodes in series are illustrated in Fig. 3.3. The proposed power-rail ESD clamp circuit in Fig. 3.3(a)

consists of the ESD-transient detection circuit with feedback technique, which are realized by two transistors (M_n and M_p) and two resistors (R_n and R_p), and the ESD clamp nMOS transistor (M_{clamp}) drawn in BigFET layout style. These two resistors are realized by N-well resistors with shallow trench isolation (STI). In Fig. 3.3(a), the gate terminal of ESD clamp nMOS transistor is linked to the output of the ESD-transient detection circuit. The circuit is connected in a cascode structure (R_n with M_n, and M_p with R_p) to construct the ESD-transient detection circuit with positive-feedback mechanism, which can command the ESD clamp nMOS transistor at "ON" or "OFF" state.

To overcome the transient-induced latch-on issue, the ESD-transient detection circuit is added with one or two diodes in series to adjust its holding voltage, as shown in Figs. 3.3(b) and (c), respectively. The anode of the diode is connected to the gate terminal of M_p transistor, and its cathode is connected to the drain terminal of M_n transistor. With such a modification, the holding voltage of the power-rail ESD clamp circuit can be adjusted by the number of added diodes.

Verified in the test chips, the ESD clamp nMOS transistor is drawn in BigFET layout style without silicide blocking in a 65nm 1.2V CMOS process. Compared with the power-rail ESD clamp circuit with the traditional *RC*-based ESD-transient detection circuit, the layout area of the new proposed ESD-transient detection circuit is much smaller, as illustrated in Figs. 3.4(a) ~ (d). The dimension of M_{clamp} in all circuits verified in the silicon test chips is kept the same of 2000μm/0.1μm. According to the layout area of the new proposed power-rail ESD clamp circuits, the cell height of the whole power-rail ESD clamp circuit is reduced by 30%, and the layout area of the ESD-transient detection circuit is reduced by 54.5%.

3.2.2 Operation Principles

The most important feature of the new proposed power-rail ESD clamp circuit is no need of additional capacitor. Because the ESD clamp nMOS transistor is drawn in BigFET layout style without silicide blocking, a large gate-to-drain, gate-to-source, and gate-to-body parasitic capacitors (C_{gd}, C_{gs}, and C_{gb}) essentially exist in the ESD clamp nMOS transistor. Sufficiently utilizing these parasitic capacitors with the resistor (R_p) to realize capacitance-coupling mechanism, no additional capacitor is needed in this design. In Fig. 3.3(a), during the positive V_{DD}-to-V_{SS} ESD stress condition, the voltage of node A will be simultaneously elevated toward a positive voltage through the coupling effect from the parasitic capacitors of the ESD clamp nMOS transistor. The elevated voltage of node A can

not hold for a long time because the resistor (R_p) connected to V_{SS} would pull down the voltage of node A. Therefore, the nMOS transistor (M_n) is designed to immediately start the ESD-transient detection circuit with positive feedback mechanism when the voltage of node A is elevated. The turned-on nMOS transistor (M_n) makes the voltage of node B low enough to turn on the pMOS transistor (M_p) due to the voltage drop on the resistor (R_n). Therefore, the feedback loop of the ESD-transient detection circuit is started entirely, and the voltage of node A is continuously elevated to the voltage level at V_{DD} line by the turned-on pMOS transistor (M_p) during the ESD stress transition. Finally, the ESD clamp nMOS transistor is turned on to discharge ESD current. A 3V voltage pulse with a rise time of 5ns was applied to the V_{DD} node while the V_{SS} node was grounded to simulate the fast-rising edge of the HBM ESD event, as illustrated in Fig. 3.5. The simulation results clearly demonstrate that the voltage at node A can be elevated to the voltage level at V_{DD}. However, the voltage at node A in the *RC*-based power-rail ESD clamp circuit is elevated to the voltage level higher than the threshold voltage of ~0.58V for only the first period of ~300ns. The design parameters, including the device sizes of each transistor and resistor, are listed in Table 3.1. On the other hand, the parasitic drain-substrate diode in the ESD clamp nMOS transistor can provide a low impedance path under the negative V_{DD}-to-V_{SS} ESD stress.

With the proposed power-rail ESD clamp circuit in Fig. 3.3, the gain (G) of the coupling effect composed of C_{gd}, C_{gs}, C_{gb}, and R_p can be expressed as

$$G = \frac{V_A}{V_{DD}} = \left| \frac{\left(\frac{1}{R_p} + j\omega\left(C_{gs} + C_{gb}\right) \right)^{-1}}{\frac{1}{j\omega C_{gd}} + \left(\frac{1}{R_p} + j\omega\left(C_{gs} + C_{gb}\right) \right)^{-1}} \right| \quad (1)$$

According to the design parameters of the proposed power-rail ESD clamp circuit, the gain with $C_{gd} \fallingdotseq C_{gs}$=0.43pF, C_{gb}=0.39pF, R_p=20kΩ, and signal frequency of 50MHz derived from 5ns fast-rising edge of the voltage pulse, would be 0.34. Therefore, the voltage of node A is determined by the gain of the coupling structure. As shown in Fig. 3.6, the coupling voltage at node A is exactly equal to 0.34V_{DD} before the ESD-transient detection circuit is turned on. When the sub-threshold current of the M_n can produce enough voltage drop on R_n to further turn on the M_p, the voltage at node A would be elevated quickly to the voltage level at V_{DD}. In Fig. 3.6, it can be observed that the voltage of node A is elevated to 0.41V and then raised quickly because the ESD-transient detection circuit is turned on. Consequently, the ESD clamp nMOS transistor is turned on by the ESD-transient detection circuit with positive

feedback mechanism. The gain expression in eq. (1) of the coupling structure has been successfully verified by the simulation.

According to eq. (1), the most critical device is the R_p to quickly drive the M_n into sub-threshold region during the pulse rising period. Therefore, the R_p is chosen to be 20kΩ to make the gain of the coupling structure and the layout area of R_p optimal. The R_n resistance of 40kΩ is determined to produce enough voltage drop on R_n to further turn on the M_p as long as there is sub-threshold current of a few tens micro-ampere flowing through the R_n. Consequently, the ESD-transient detection circuit with positive feedback mechanism can be successfully initiated.

According to the design window of the ESD protection circuit for avoiding the latch-on issue, the holding voltage (V_h) of the ESD protection circuit is an important index to exceed the normal circuit operation voltage V_{DD}. The holding voltage of the proposed power-rail ESD clamp circuit can be indicated as

$$\begin{aligned} V_h &= V_{ds(M_n)} + nV_{ON(Diode)} + V_{gs(M_p)} \\ &= V_{ds(M_n)}\Big|_{I_{ds}=V_{THP}/R_n} + nV_{ON(Diode)} + V_{THP} \end{aligned} \tag{2}$$

where n and V_{ON} are the number and the turn-on voltage of the diode, respectively. For the pMOS threshold voltage of 0.58V and R_n resistance of 40kΩ, the I_{ds} current flowing through the M_n transistor is only about 14.5μA. Based on the device parameters and simulation results, the V_{ds} of M_n transistor is only a few milli-volt and the V_{ON} of diode is about 0.67V. Therefore, the V_h in the expression (2) can be re-expressed as below due to minor V_{ds} compared to V_{ON} and V_{THP}.

$$V_h \approx nV_{ON(Diode)} + V_{THP} \tag{3}$$

For the new proposed power-rail ESD clamp circuit in Fig. 3.3(a), the V_h would be only 0.58V due to zero diode in the ESD-transient detection circuit. It would be a high risk to apply the structure in Fig. 3.3(a) to the circuit with 1.2V operation voltage. However, the V_h can be theoretically adjusted to 1.25V and 1.92V for the new proposed structures in Figs. 3.3(b) and (c), respectively. By adding the diodes in the ESD-transient detection circuit, the new proposed power-rail ESD clamp circuit with adjustable holding voltage can be safely applied to protect any internal circuits from the transient-induced latch-on event.

Under the normal V_{DD} power-on condition, the gain of the coupling structure is 1.35×10^{-5} for a 1.2V power-on voltage pulse with a rise time of 1ms. Such a slow-rising power-on

voltage will not induce a high enough coupling voltage at node A to initiate the ESD-transient detection circuit. When the power-on voltage pulse has a rise time of 100ns, the gain of the coupling structure is only 0.13, which is also too small to initiate the ESD-transient detection circuit. Even though the power-rail ESD clamp circuit encounters a fast-rising power-on voltage with the order of nanoseconds, the voltage level of node A and node B can be kept at ground and V_{DD}, respectively, due to the design with adjustable holding voltage. Therefore, the new proposed power-rail ESD clamp circuit can have excellent immunity against mis-trigger under the fast power-on conditions.

3.2.3 Experimental Results

The test chips of power-rail ESD clamp circuits with the traditional *RC*-based and the new proposed ESD-transient detection circuits have been fabricated in a 65nm 1.2V CMOS process, as shown in Figs. 3.7(a) and (b). These circuits are prepared for standby leakage current measurement, TLP measurement, turn-on verification measurement, and transient-induced latch-up (TLU) measurement.

3.2.3.1 Standby Leakage Current

The DC *I-V* characteristics of the power-rail ESD clamp circuits are measured by HP4155 from 0V to 1.2V with the voltage step of 10mV. The leakage currents of the power-rail ESD clamp circuits at 1.2V normal V_{DD} operation voltage can be observed clearly in Fig. 3.8. The leakage current of the *RC*-based power-rail ESD clamp circuit is 86.9nA. However, the new proposed power-rail ESD clamp circuits have the leakage currents of the range from 50.2nA to 55.3nA, and the leakage current of the ESD clamp nMOS transistor (M_{clamp}) is about 49.2nA. This implies that the leakage currents of the *RC*-based and the new proposed ESD-transient detection circuits are 37.7nA and 6.1nA, respectively. The leakage current of the new proposed ESD-transient detection circuit is extremely reduced by 83.8% because the device sizes of M_n and M_p transistors are greatly shrunk. Therefore, the new proposed power-rail ESD clamp circuit with lower leakage current is more adequate for the portable product applications, which strongly demand the low standby current.

3.2.3.2 TLP Measurement and ESD Robustness

In order to investigate the circuit behavior during high ESD current stress, TLP generator with a pulse width of 100ns and a rise time of ~2ns is used to measure the *RC*-based and the

new proposed power-rail ESD clamp circuits [29]. The measured results, as illustrated in Fig. 3.9(a), demonstrate that there are no obvious differences among the curves at the voltage level higher than 4V because the ESD clamp nMOS transistors in all power-rail ESD clamp circuits are drawn with the same device dimension and layout style. The second breakdown currents (It_2) of these four power-rail ESD clamp circuits are all around 5.44A.

The V_h of the new proposed ESD-transient detection circuits with zero, one, and two diodes are 0.51V, 1.22V, and 1.95V, respectively, as shown in Fig. 3.9(b). These measured V_h are very close to the theoretical V_h of 0.58V, 1.25V, and 1.92V calculated in section 3.2.2. The adjustable holding voltage by modifying the number of diodes in the ESD-transient detection circuit has been successfully verified by the TLP *I-V* measurement.

Table 3.2 shows the HBM [1] and MM [2] ESD robustness of these four power-rail ESD clamp circuits. The HBM and MM ESD robustness of all power-rail ESD clamp circuits are over 8kV and 450V, respectively. It is obvious that the characteristics (It_2, HBM, and MM ESD levels) of all power-rail ESD clamp circuits are the same due to the same device dimension and layout style of the ESD clamp nMOS transistors.

3.2.3.3 Turn-On Verification

In order to observe the turn-on efficiency of the power-rail ESD clamp circuits, a 3V ESD-transient-like voltage pulse with 5ns rise time is applied to the V_{DD} power line with the grounded V_{SS}. The voltage pulse with a rise time of 5ns is utilized to simulate the fast-rising edge of the HBM ESD event [1]. The ESD-transient-like voltage pulse will be coupled to the gate terminal of the M_n transistor in the proposed ESD-transient detection circuit, and then the proposed ESD-transient detection circuit with positive feedback mechanism will be started up. Consequently, the M_{clamp} transistor is triggered on. The turn-on verifications of the voltage waveform on V_{DD} power line under ESD-like stress condition are shown in Fig. 3.10(a).

In Fig. 3.10(a), the voltage waveform of the *RC*-based design rises as the time is increased. On the contrary, the voltage waveforms of the new proposed designs can be clamped to a specific voltage level during the whole pulse width due to the positive feedback mechanism of the ESD-transient detection circuit. Therefore, the new proposed ESD-transient detection circuit can efficiently extend the turn-on duration of the ESD clamp nMOS transistor under ESD stress conditions.

For power-on condition, the voltage usually has a rise time in the order of milliseconds. According to this feature, the coupling voltage at node A is not enough to start up the

ESD-transient detection circuit, and the ESD clamp nMOS transistor will be kept at "OFF" state. However, some previous studies [33]-[36], [43] have demonstrated that the power-rail ESD clamp circuits with *RC*-based ESD-transient detection circuits and feedback mechanism were easily mis-triggered into the latch-on state under the fast power-on condition. The new proposed power-rail ESD clamp circuits have been applied with 1.2V voltage pulse with 25ns rise time to investigate their immunity against mis-trigger, as shown in Fig. 3.10(b). The voltage waveforms of the new proposed power-rail ESD clamp circuits are not degraded under the fast power-on condition. Even though the rise time of fast power-on voltage is shorter than 25ns, the new proposed power-rail ESD clamp circuits with adjustable holding voltage can still perform high immunity against mis-trigger. On the contrary, the *RC*-based power-rail ESD clamp circuit dramatically suffered the mis-trigger under the fast power-on condition, and it spends about 300ns to return back the normal operation voltage level.

In addition, the turn-on verification with the power line noise at normal operation is another useful justification for the latch-on concerns. The transient noise with 3V voltage level and a rise time of 5ns is purposely added to V_{DD} power line with 1.2V operation voltage. As shown in Figs. 3.11(a) ~ (c), the new proposed ESD-transient detection circuit with zero diode is the only circuit to suffer the latch-on issue because its holding voltage is much lower than the 1.2V operation voltage. However, the holding voltage of the new proposed ESD-transient detection circuit can be adjusted by adding the diodes. Therefore, the ESD-transient detection circuits with positive feedback mechanism and the adjustable holding voltage can be free to latch-on issue. Since the feedback mechanism is not used in the *RC*-based power-rail ESD clamp circuit, the latch-on event is not occurred.

3.2.3.4 Transient-Induced Latch-Up (TLU) Measurement

The transient-induced latch-up (TLU) measurement has been used to investigate the susceptibility of device under test (DUT) to the noise transient or glitch on the power lines under normal circuit operation condition. The TLU measurement setup with bipolar trigger waveform can accurately simulate the practical system-level ESD event [44]. The setup for TLU measurement is shown in Fig. 3.12 [44], [45]. The charging voltage (V_{charge}) has positive ($V_{charge} > 0$) and negative ($V_{charge} < 0$) polarities. The positive (negative) V_{charge} can generate the positive-going (negative-going) bipolar trigger noise into the power pins of the DUT. A 200pF capacitor is employed as the charging capacitor. The supply voltage of 1.2V is used as V_{DD} and the noise trigger source is directly connected to DUT through the relay in the

measurement setup. The current-limiting resistance of 4.7Ω is used to avoid electrical overstress (EOS) damage in the DUT under a high-current latch-on state. The voltage and current waveforms of the DUT at V_{DD} node after TLU measurement are monitored by the oscilloscope.

The measured V_{DD} and I_{DD} transient responses of the traditional *RC*-based power-rail ESD clamp circuit under the TLU measurement with V_{charge} of +1kV and -1kV are shown in Figs. 3.13(a) and (b), respectively. In Fig. 3.13, the latch-on event is not occurred because the feedback mechanism is not used in the *RC*-based power-rail ESD clamp circuit. Due to the holding voltage lower than V_{DD}, the new proposed power-rail ESD clamp circuit with zero diode suffered the latch-on issue under TLU measurement for V_{charge} of +3V and -2V, as shown in Fig. 3.14. The measured results of the new proposed power-rail ESD clamp circuits with the diodes under the TLU measurement with V_{charge} of +1kV and -1kV are also shown in Fig. 3.15. In Fig. 3.15, the new proposed power-rail ESD clamp circuits with adjustable holding voltage can successfully overcome transient-induced latch-on issue. The TLU levels (the minimum V_{charge} to induce the latch-on on V_{DD}) among the four power-rail ESD clamp circuits are listed in Table 3.3.

3.3 Power-Rail ESD Clamp Circuit with ESD Clamp pMOS Transistor

Besides, low standby leakage of the power-rail ESD clamp circuit is highly demanded by the hand-held, portable, and battery powered products. In advanced CMOS technology, the leakage current of nMOS was often larger than that of pMOS in the same device dimension. Therefore, pMOS is suggested to be used as ESD clamp device [38].

In this section, the parasitic capacitance of the ESD clamp pMOS transistor drawn in BigFET layout style is used as a part of ESD-transient detection circuit. This new design has also been verified in a 65nm 1.2V CMOS technology. From the measured results, the proposed power-rail ESD clamp circuit has features of area efficiency, low leakage current, and high immunity against mis-trigger.

3.3.1 ESD-Transient Detection Circuit Scheme

The new proposed power-rail ESD clamp circuit is illustrated in Fig. 3.16. The ESD-transient detection circuit consists of two transistors (M_n and M_p), two resistors (R_n and

R_p), and diode string. The pMOS transistor drawn in BigFET layout style (M_{clamp}) is used as ESD clamp device. The gate terminal of M_{clamp} is linked to the output of the ESD-transient detection circuit, which can command M_{clamp} at "ON" or "OFF" state.

In Fig. 3.16, the diode string in ESD-transient detection circuit is used to adjust the holding voltage to overcome the transient-induced latch-on issue. In this work, the ESD-transient detection circuits with zero, one, and two diodes were investigated in silicon chip. The measured results reveal that the holding voltage of the power-rail ESD clamp circuit can be adjusted by modifying the number of the diodes in the ESD-transient detection circuit. In addition, the new proposed power-rail ESD clamp circuit can be totally turned off after power-on transition because the nodes A and B are kept at V_{DD} and V_{SS} through the resistors R_n and R_p, respectively.

Verified in the test chip, the ESD clamp pMOS transistor is drawn in BigFET layout style without silicide blocking in a 65nm 1.2V CMOS process. Compared with the power-rail ESD clamp circuit with the traditional *RC*-based ESD-transient detection circuit, the layout area of the new proposed ESD-transient detection circuit is much smaller, as illustrated in Figs. 3.17(a) ~ (d). The dimension of M_{clamp} in all circuits verified in the silicon test chip is kept the same of 2000μm/0.1μm. According to the layout area of the new proposed power-rail ESD clamp circuits, the cell height of the whole power-rail ESD clamp circuit is reduced by 30%, and the layout area of the ESD-transient detection circuit is reduced by 54.5%.

3.3.2 Operation Principles

The ESD clamp pMOS transistor is drawn in BigFET without silicide blocking. Large C_{gd}, C_{gs}, and C_{gb} parasitic capacitors essentially exist in the ESD clamp pMOS transistor. These parasitic capacitors and the resistor R_n can be used to realize capacitance-coupling mechanism. In Fig. 3.16, the gain (G) of the coupling effect caused by C_{gd}, C_{gs}, C_{gb}, and R_n during the positive V_{DD}-to-V_{SS} ESD stress condition can be expressed as

$$G = \frac{V_A}{V_{DD}} = \left| \frac{\dfrac{1}{j\omega C_{gd}}}{\dfrac{1}{j\omega C_{gd}} + \left(\dfrac{1}{R_n} + j\omega \left(C_{gs} + C_{gb} \right) \right)^{-1}} \right| \tag{4}$$

According to the device sizes used in this work, the gain is 0.64 with $C_{gd} \fallingdotseq C_{gs}$=0.44pF, C_{gb}=0.35pF, R_n=40kΩ, and signal frequency of 50MHz derived from 5ns fast-rising edge of

the ESD voltage pulse.

A 3V voltage pulse with a rise time of 5ns is applied to the V_{DD} node while the V_{SS} node was grounded to simulate the fast-rising edge of the HBM ESD event, as shown in Fig. 3.18(a). The coupling voltage at node A (V_A) of the proposed circuit is exactly equal to $0.64V_{DD}$ before the ESD-transient detection circuit is turned on. When the voltage difference between V_{DD} and V_A is getting larger, the sub-threshold current of M_p can produce enough voltage difference on R_p to further turn on M_n, the V_A will be quickly pulled down to the ground level to trigger on the ESD clamp pMOS transistor. In Fig. 3.18(b), the pulled-down V_A of the proposed circuit can be kept at low voltage level during whole voltage pulse duration. However, the V_A in the traditional *RC*-based power-rail ESD clamp circuit is elevated to the voltage level higher than the nMOS threshold voltage of ~0.58V for only the first period of ~300ns. The design parameters, including the device sizes of each transistor and resistor, are listed in Table 3.4.

According to the design window of the ESD protection circuit for avoiding the latch-on issue, the V_h of the ESD protection circuit is an important index to exceed the normal circuit operation voltage V_{DD}. The holding voltage of the proposed power-rail ESD clamp circuit can be indicated as

$$\begin{aligned} V_h &= V_{ds(M_p)} + nV_{ON(Diode)} + V_{gs(M_n)} \\ &= V_{ds(M_p)}\Big|_{I_{ds}=V_{THN}/R_p} + nV_{ON(Diode)} + V_{THN} \\ &\approx nV_{ON(Diode)} + V_{THN}, \end{aligned} \tag{5}$$

where n and V_{ON} are the number and the turn-on voltage of the diode, respectively. Based on the simulation results, the V_h can be represented as the summation of V_{ON} (0.71V) and V_{THN} (0.58V) due to minor V_{ds} (~ few milli-volt).

For the new proposed power-rail ESD clamp circuit with zero diode in Fig. 3.16, the V_h would be only 0.58V. It would be a high risk to apply this structure to the circuit with 1.2V operation voltage. However, the V_h can be theoretically adjusted to 1.29V and 2.00V by adding the diodes in the ESD-transient detection circuit. The new proposed power-rail ESD clamp circuit with adjustable holding voltage can be safely applied to protect any internal circuits from the transient-induced latch-on event.

3.3.3 Experimental Results

The test chip to verify the proposed power-rail ESD clamp circuit has been fabricated in a 65nm 1.2V CMOS process. As shown in Figs. 3.19(a) and (b), the layout area of the proposed ESD-transient detection circuit is reduced by 54.5% from that of traditional *RC*-based one.

3.3.3.1 Standby Leakage Current

The leakage currents of the power-rail ESD clamp circuits at 1.2V normal circuit operation voltage are shown in Fig. 3.20. The leakage current of the traditional *RC*-based power-rail ESD clamp circuit is 86.9nA at room temperature. However, the proposed power-rail ESD clamp circuits with different numbers of diodes have the leakage currents in the range of 15nA to 17nA. The leakage current of the proposed power-rail ESD clamp circuit is largely reduced by 80.4% due to ESD clamp pMOS transistor. Therefore, the proposed power-rail ESD clamp circuit with lower leakage current is more adequate for the portable products, which highly require low standby leakage current.

3.3.3.2 TLP Measurement and ESD Robustness

As shown in Fig. 3.21(a), there are no differences among the curves higher than 3.5V because the device sizes of M_{clamp} in all proposed power-rail ESD clamp circuits are the same. The It_2 of the traditional *RC*-based and the proposed power-rail ESD clamp circuits are 5.44A and 5.01A, respectively.

The measured holding voltages of the proposed ESD-transient detection circuits with zero, one, and two diodes are 0.56V, 1.25V, and 2.12V, respectively, as shown in Fig. 3.21(b). They are very close to the theoretical ones of 0.58V, 1.29V, and 2.00V calculated from (5). The ESD-transient detection circuit with the adjustable holding voltage has been successfully verified, which can be safely applied to protect any internal circuits from the transient-induced latch-on event.

Table 3.5 shows the HBM and MM ESD robustness of these four power-rail ESD clamp circuits. The HBM ESD robustness of all power-rail ESD clamp circuits are over 8kV. The MM ESD robustness of the traditional *RC*-based and the proposed power-rail ESD clamp circuits are 450V and 350V, respectively.

3.3.3.3 Turn-On Verification

For the turn-on verification, a 3V voltage pulse with 5ns rise time to simulate the rising

transition of HBM ESD event is applied to the V_{DD} power line with the grounded V_{SS}. In Fig. 3.22(a), the voltage waveform of the traditional *RC*-based design rises as the time increases. On the contrary, the voltage waveforms of the proposed designs with different numbers of diodes are clamped to the specific voltage levels during the whole pulse duration due to the positive feedback mechanism in the proposed ESD-transient detection circuit.

For the fast power-on condition, a voltage pulse with 1.2V and 2ns rise time is applied in this work. As shown in Fig. 3.22(b), the voltage waveforms of the proposed power-rail ESD clamp circuits with one and two diodes are not degraded. The proposed power-rail ESD clamp circuits have high immunity against mis-trigger due to adjustable holding voltage. On the contrary, the *RC*-based power-rail ESD clamp circuit dramatically suffers the mis-trigger, which spends about 300ns to return back the normal circuit operation voltage level of 1.2V, as shown in Fig. 3.22(b).

In addition, the transient noise with 3V voltage level and a rise time of 5ns is purposely added to V_{DD} power line with 1.2V operation voltage. As shown in Figs. 3.23(a) ~ (c), the new proposed ESD-transient detection circuit with zero diode is the only circuit to suffer the latch-on issue because its holding voltage is much lower than the 1.2V operation voltage. However, the holding voltage of the new proposed ESD-transient detection circuit can be adjusted by adding the diodes. Therefore, the ESD-transient detection circuits with positive feedback mechanism and the adjustable holding voltage can be free to latch-on issue. Since the feedback mechanism was not used in the traditional *RC*-based power-rail ESD clamp circuit, the latch-on event was not occurred in such a measurement.

3.3.3.4 TLU Measurement

The measured V_{DD} and I_{DD} transient responses of the traditional *RC*-based power-rail ESD clamp circuit under the TLU measurement with V_{charge} of +1kV and -1kV are shown in Figs. 3.24(a) and (b), respectively. In Fig. 3.24, the latch-on event is not occurred because the feedback mechanism is not used in the *RC*-based power-rail ESD clamp circuit. Due to the holding voltage lower than V_{DD}, the new proposed power-rail ESD clamp circuit with zero diode suffered the latch-on issue under TLU measurement for V_{charge} of +3V and -2V, as shown in Figs. 3.25(a) and (b). The measured results of the new proposed power-rail ESD clamp circuits with the diodes under the TLU measurement with V_{charge} of +1kV and -1kV are also shown in Figs. 3.26(a) and (b). In Fig. 3.26, the new proposed power-rail ESD clamp circuits with adjustable holding voltage can successfully overcome transient-induced latch-on

issue. The TLU levels (the minimum V_{charge} to induce the latch-on on V_{DD}) among the four power-rail ESD clamp circuits are listed in Table 3.6.

3.4 Summary

The new capacitor-less power-rail ESD clamp circuits with adjustable holding voltage have been proposed and successfully verified in a 65nm 1.2V CMOS technology. The new proposed ESD-transient detection circuit adopts the capacitance-coupling mechanism to command the ESD clamp nMOS or pMOS transistors. According to the measured results, the capacitor-less power-rail ESD clamp circuits with adjustable holding voltage demonstrate excellent immunity against mis-trigger under the fast power-on condition, and also perform no latch-on issue under power noise and TLU measurement. Moreover, the new proposed capacitor-less ESD-transient detection circuits are also area-efficient, which save layout area by more than 54.5% compared with the traditional *RC*-based ESD-transient detection circuit. For the proposed power-rail ESD clamp circuit with ESD clamp pMOS transistor, it is also efficient in standby leakage to save leakage current by more than 80.4%, compared with the traditional *RC*-based ESD-transient detection circuit.

Table 3.1

Design Parameters of the Power-Rail ESD Clamp Circuits with ESD Clamp nMOS Transistor

Design Parameters	*RC*-Based ESD Clamp Circuit	New Proposed ESD Clamp Circuit
Capacitor	64 μm / 2 μm (W/L)	none
Resistor (Ω)	R = 113k	R_n = 40k ; R_p = 20k
PMOS Transistor (M_p)	184 μm / 60 nm	24 μm / 60 nm
NMOS Transistor (M_n)	36 μm / 60 nm	12 μm / 60 nm
ESD Clamp NMOS Transistor (M_{clamp})	2000 μm / 100 nm	2000 μm / 100 nm
Diode (D_n)	none	0.057 μm^2

Table 3.2

Measured Results of Second Breakdown Current and ESD Levels of Four Power-Rail ESD Clamp Circuits

Power-Rail ESD Clamp Circuits	It_2 (A)	HBM Level (kV)	MM Level (V)
Traditional *RC*-Based	5.44	> 8	450
New Proposed with 0 Diode	5.44	> 8	450
New Proposed with 1 Diode	5.44	> 8	450
New Proposed with 2 Diodes	5.44	> 8	450

Table 3.3

Comparison on TLU Levels among Four Power-Rail ESD Clamp Circuits

Power-Rail ESD Clamp Circuits	Positive TLU Level	Negative TLU Level
Traditional *RC*-Based	Over +1kV	Over -1kV
New Proposed with 0 Diode	+3V	-2V
New Proposed with 1 Diode	Over +1kV	Over -1kV
New Proposed with 2 Diodes	Over +1kV	Over -1kV

Table 3.4

Design Parameters of the Power-Rail ESD Clamp Circuits with ESD Clamp pMOS Transistor

Design Parameters	*RC*-Based ESD Clamp Circuit (nMOS)	New Proposed ESD Clamp Circuit (pMOS)
Capacitor	64 μm / 2 μm (W/L)	none
Resistor (Ω)	R = 113k	R_n = 40k ; R_p = 20k
PMOS Transistor (M_p)	184 μm / 60 nm	24 μm / 60 nm
NMOS Transistor (M_n)	36 μm / 60 nm	12 μm / 60 nm
ESD Clamp NMOS Transistor (M_{clamp})	2000 μm / 100 nm	2000 μm / 100 nm
Diode (D_n)	none	0.057 μm^2

Table 3.5

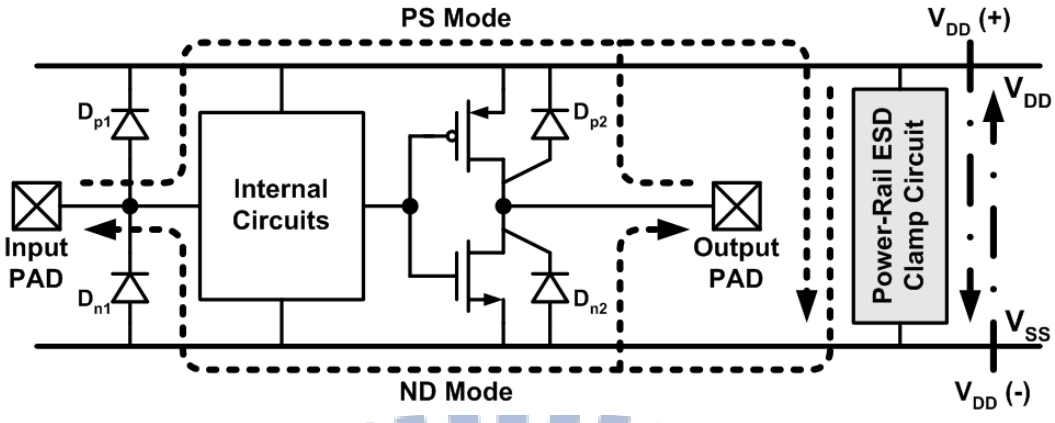
Measured Results of Second Breakdown Current and ESD Levels of Four Power-Rail ESD Clamp Circuits

Power-Rail ESD Clamp Circuits	It_2 (A)	HBM Level (kV)	MM Level (V)
Traditional *RC*-Based	5.44	> 8	450
New Proposed with 0 Diode	5.01	> 8	350
New Proposed with 1 Diode	5.01	> 8	350
New Proposed with 2 Diodes	5.01	> 8	350

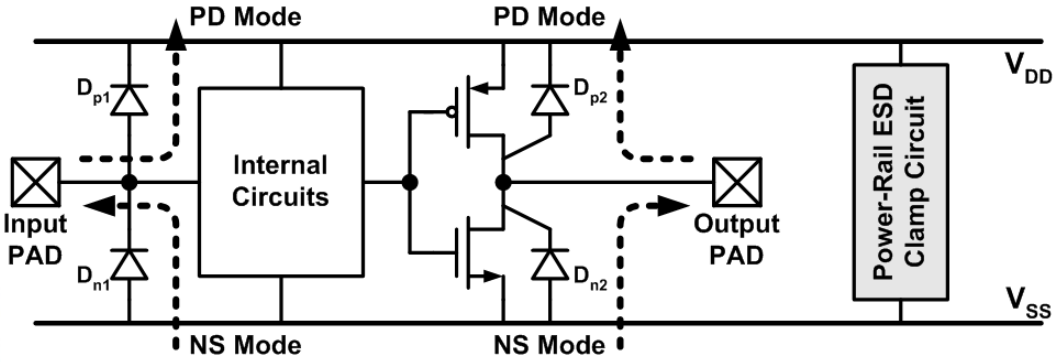
Table 3.6

Comparison on TLU Levels among Four Power-Rail ESD Clamp Circuits

Power-Rail ESD Clamp Circuits	Positive TLU Level	Negative TLU Level
Traditional *RC*-Based	Over +1kV	Over -1kV
New Proposed with 0 Diode	+3V	-2V
New Proposed with 1 Diode	Over +1kV	Over -1kV
New Proposed with 2 Diodes	Over +1kV	Over -1kV



(a)



(b)

Fig. 3.1 Typical on-chip ESD protection design with active power-rail ESD clamp circuit under (a) PS-mode / ND-mode, and (b) PD-mode / NS-mode, ESD stress conditions.

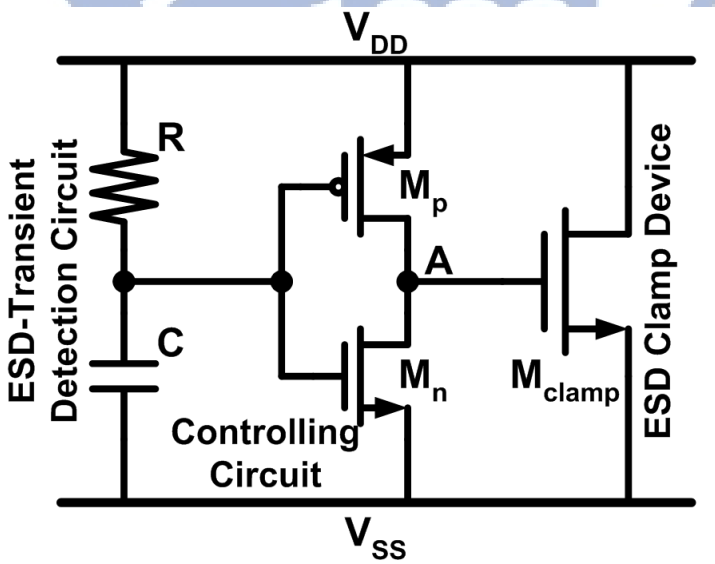
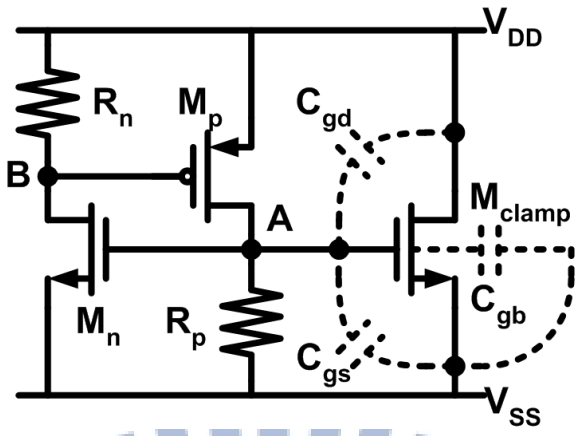
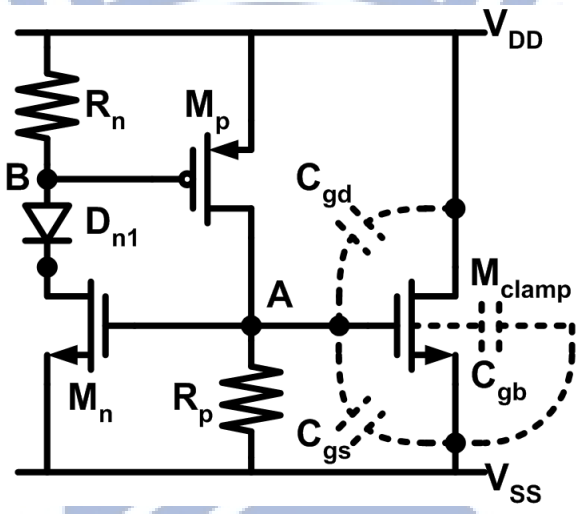


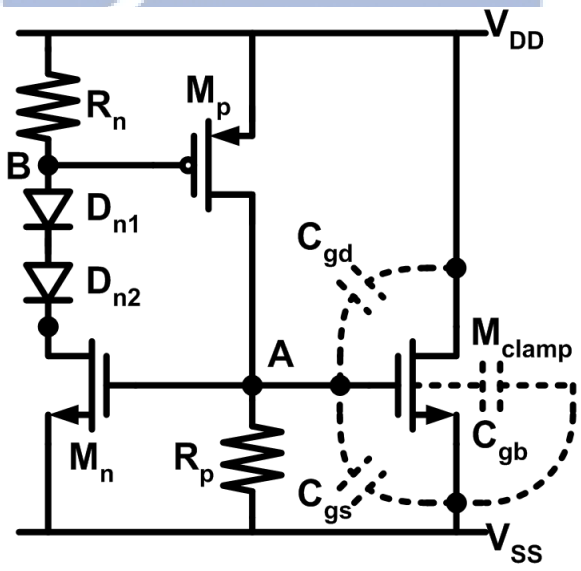
Fig. 3.2 Typical implementation of the *RC*-based power-rail ESD clamp circuit with ESD-transient detection circuit, controlling circuit, and ESD clamp device.



(a)

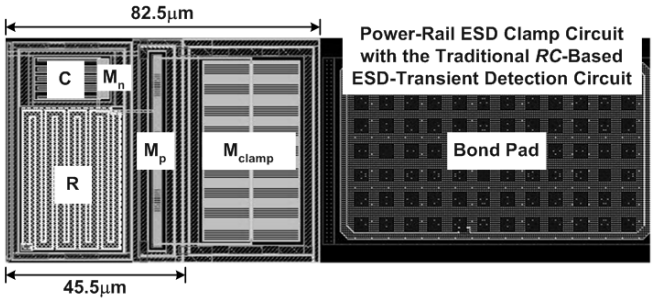


(b)

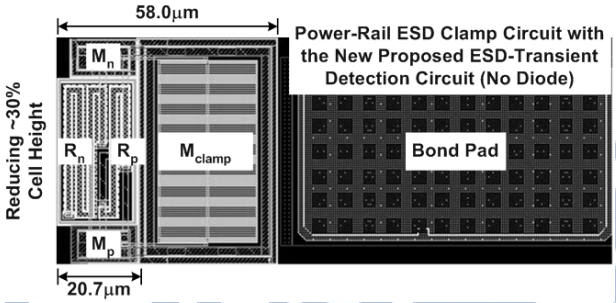


(c)

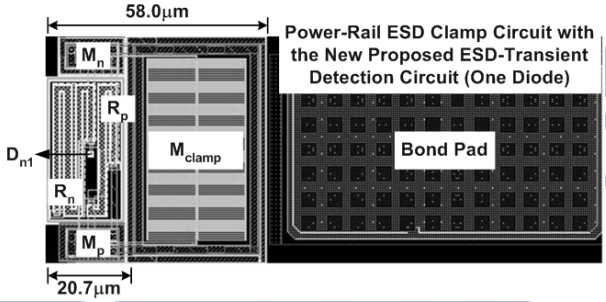
Fig. 3.3 New proposed power-rail ESD clamp circuits with ESD clamp nMOS transistor. There are (a) zero diode, (b) one diode, and (c) two diodes used in the ESD-transient detection circuit, respectively.



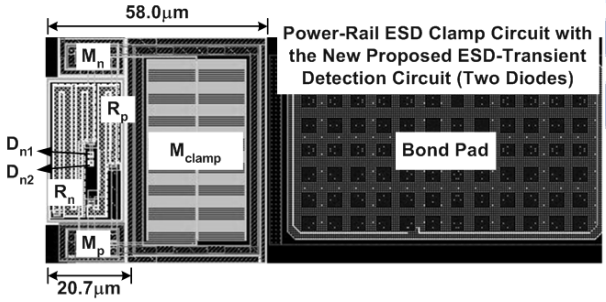
(a)



(b)



(c)



(d)

Fig. 3.4 Comparison on the layout areas among the four power-rail ESD clamp circuits. The ESD clamp nMOS transistor M_{clamp} is drawn in a BigFET layout style with the same W/L=2000μm/0.1μm, which is triggered by (a) the traditional *RC*-based ESD-transient detection circuit, (b) the proposed ESD-transient detection circuit with no diode, (c) the proposed ESD-transient detection circuit with one diode, and (d) the proposed ESD-transient detection circuit with two diodes.

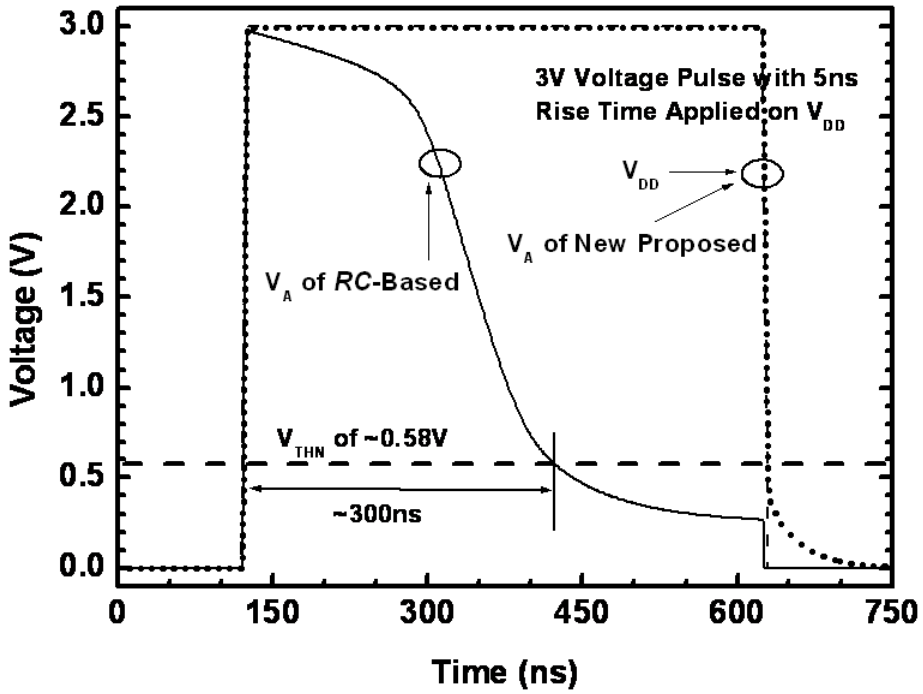


Fig. 3.5 ESD-like simulation results of the voltage at the gate terminal of the ESD clamp nMOS transistor controlled by the *RC*-based and the new proposed ESD-transient detection circuit.

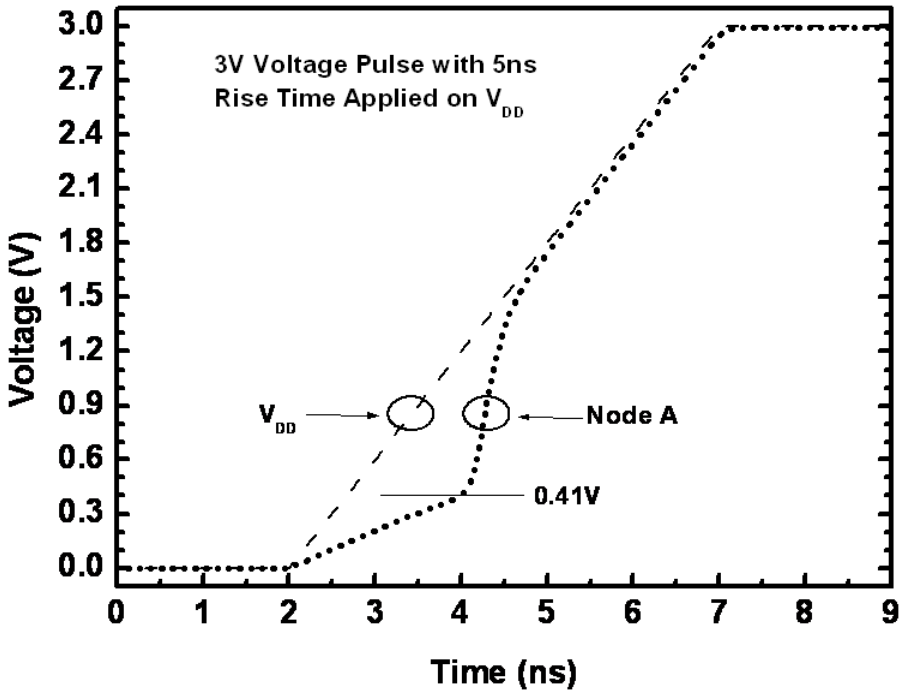
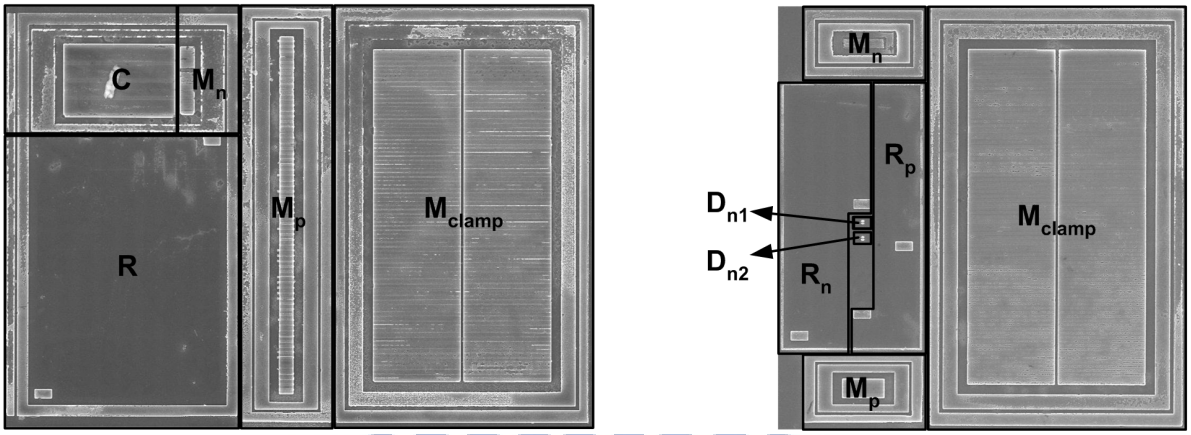


Fig. 3.6 The simulation results of the voltage transient on V_{DD} and node A for new proposed power-rail ESD clamp circuit with ESD clamp nMOS transistor. The 3V ESD-like voltage pulse with 5ns rise time is applied on V_{DD}.



(a) (b)

Fig. 3.7 Chip microphotographs of the fabricated power-rail ESD clamp circuit, realized with (a) the traditional *RC*-based ESD-transient detection circuit and (b) the proposed ESD-transient detection circuit with two diodes.

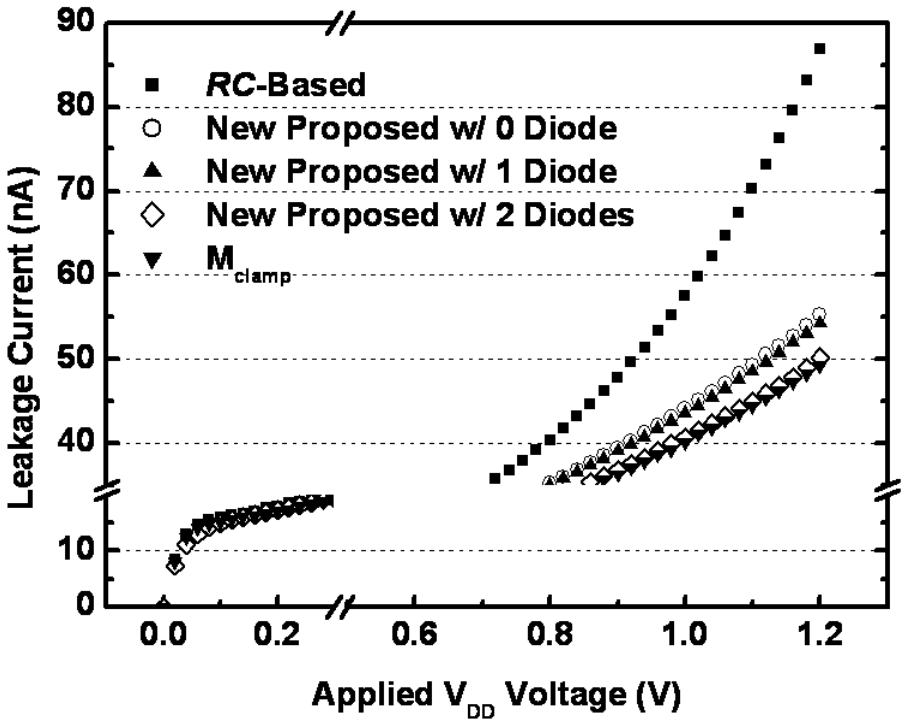
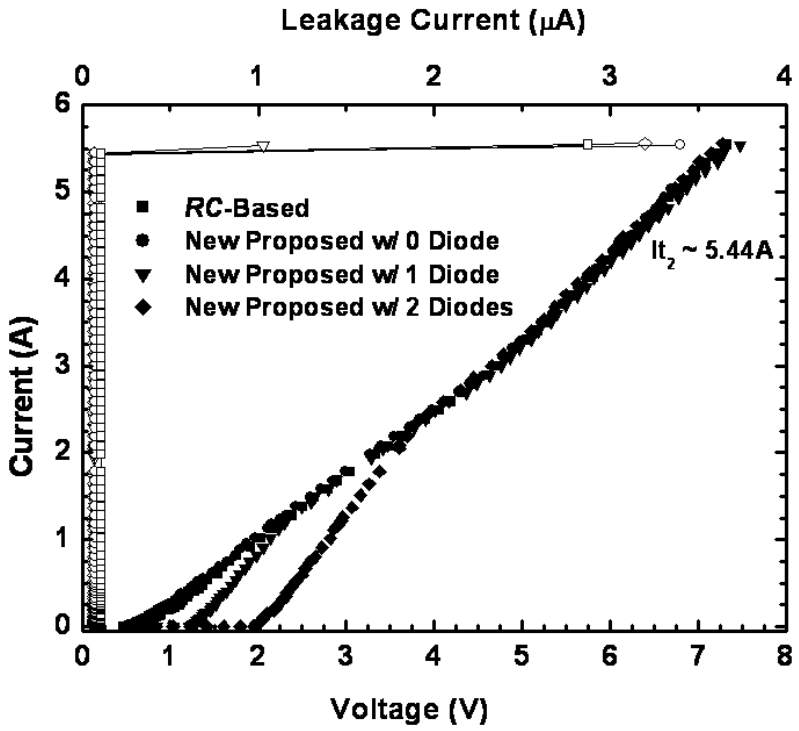
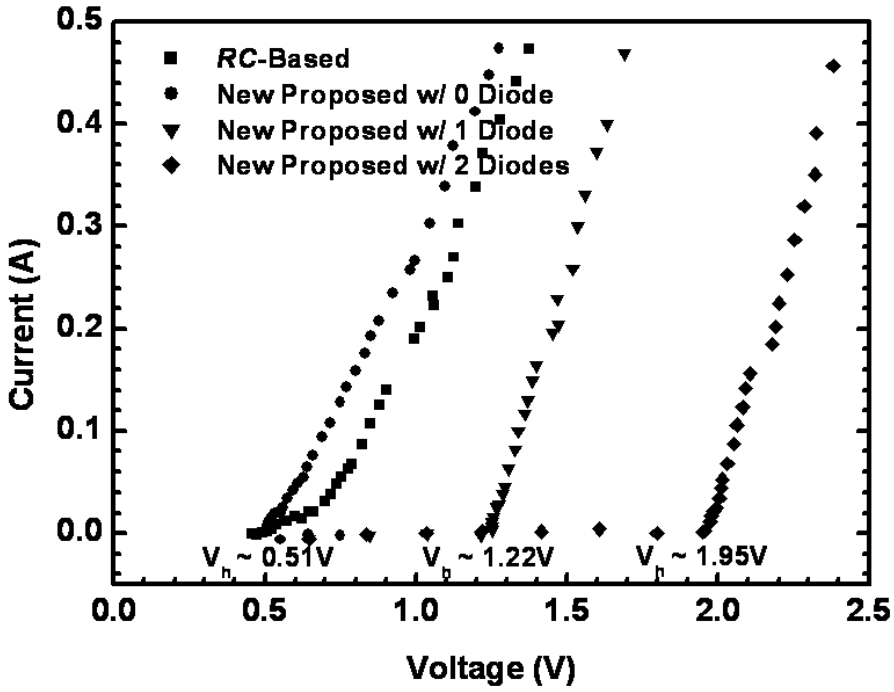


Fig. 3.8 The measured standby leakage current of the *RC*-based power-rail ESD clamp circuit, the new proposed power-rail ESD clamp circuits, and the single ESD clamp nMOS transistor.

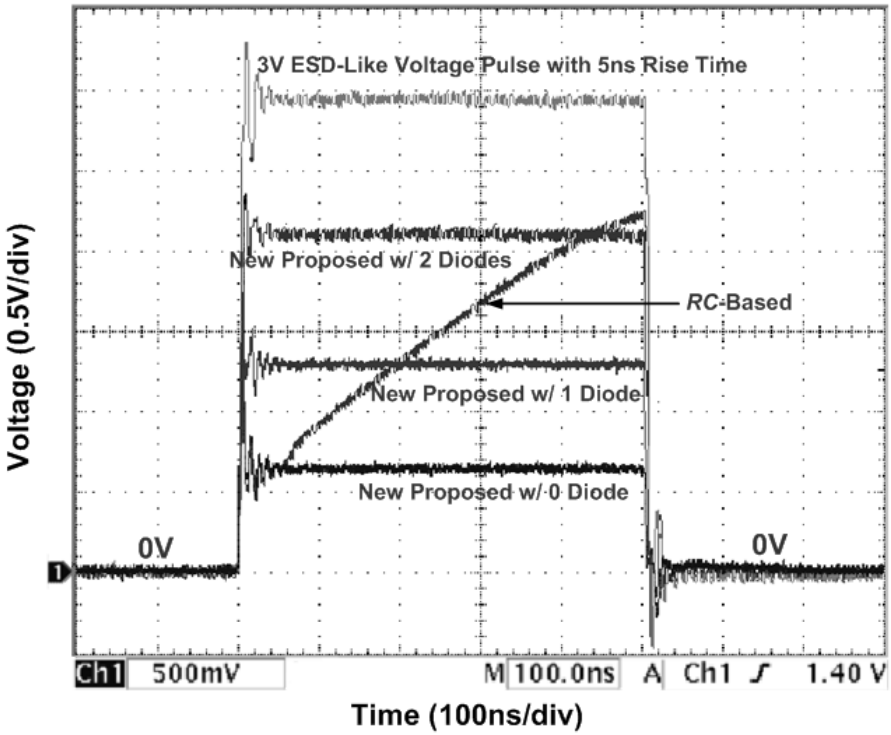


(a)

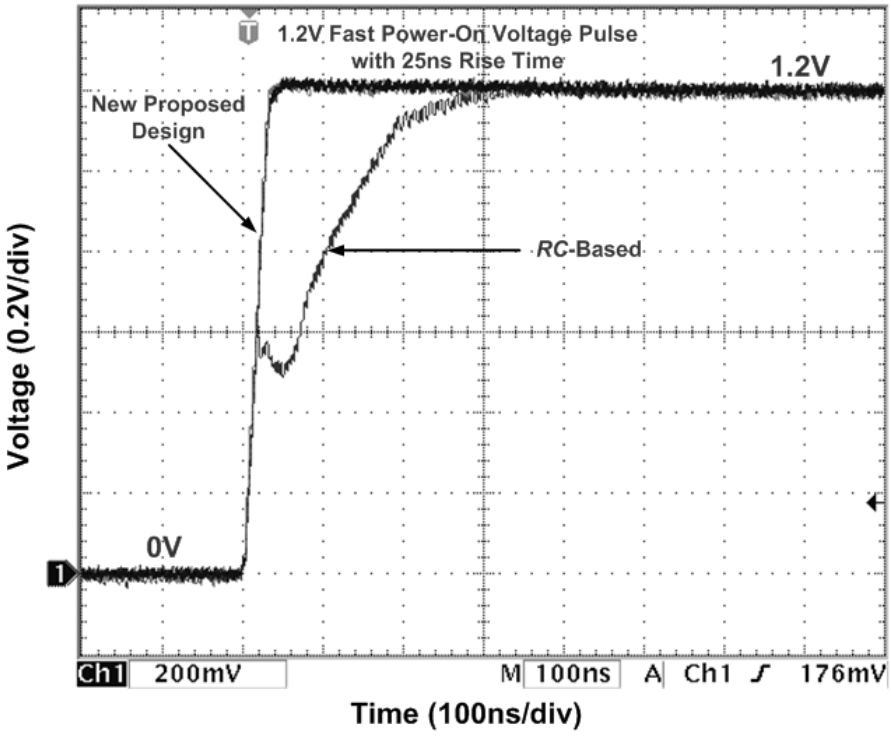


(b)

Fig. 3.9 TLP measured *I-V* curves of (a) the power-rail ESD clamp circuits with the *RC*-based, the new proposed ESD-transient detection circuit, and (b) the zoom-in illustration for the holding voltages (V_h).

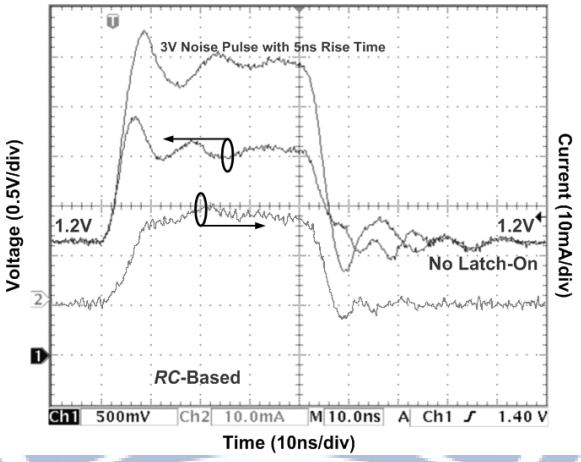


(a)

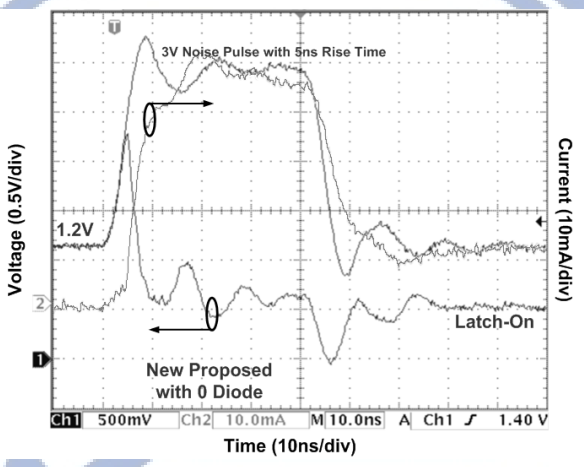


(b)

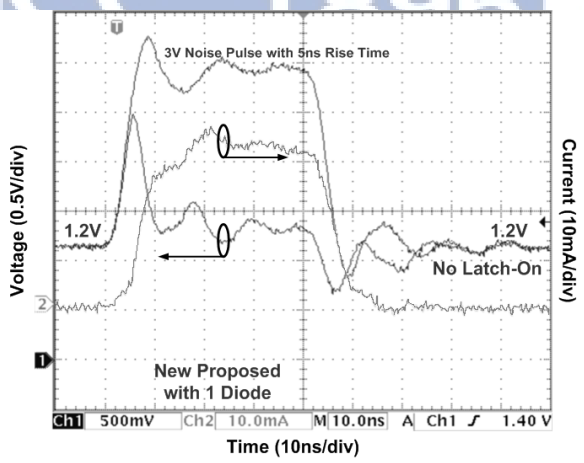
Fig. 3.10 The voltage waveforms under (a) ESD-transient-like condition with 3V voltage pulse and 5ns rise time, (b) fast power-on condition with 1.2V voltage pulse and 25ns rise time.



(a)



(b)



(c)

Fig. 3.11 The measured voltage and current waveforms of power-rail ESD clamp circuit, realized with (a) the traditional *RC*-based ESD-transient detection circuit, (b) the proposed ESD-transient detection circuit with no diode, and (c) the proposed ESD-transient detection circuit with one diode, under transient noise condition.

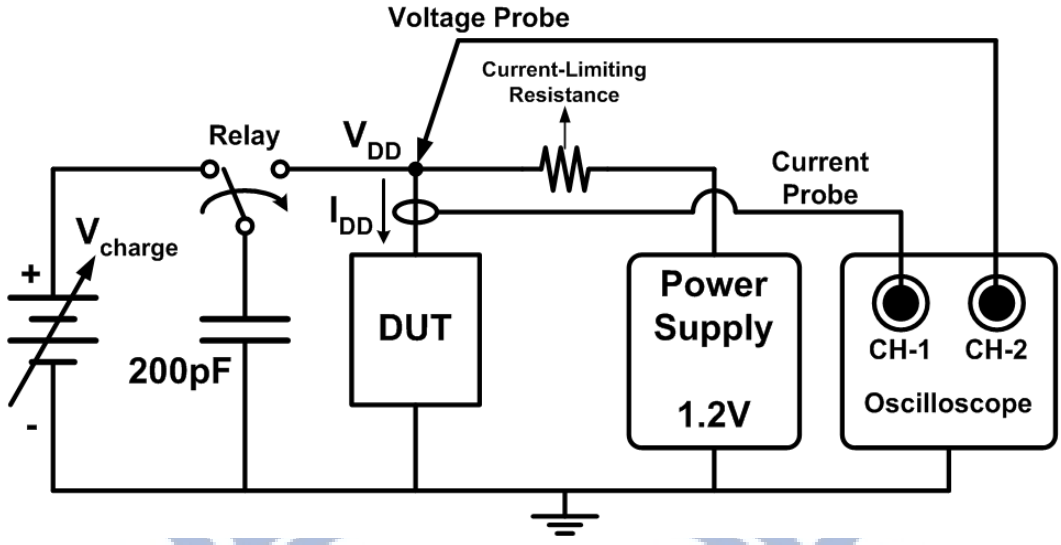
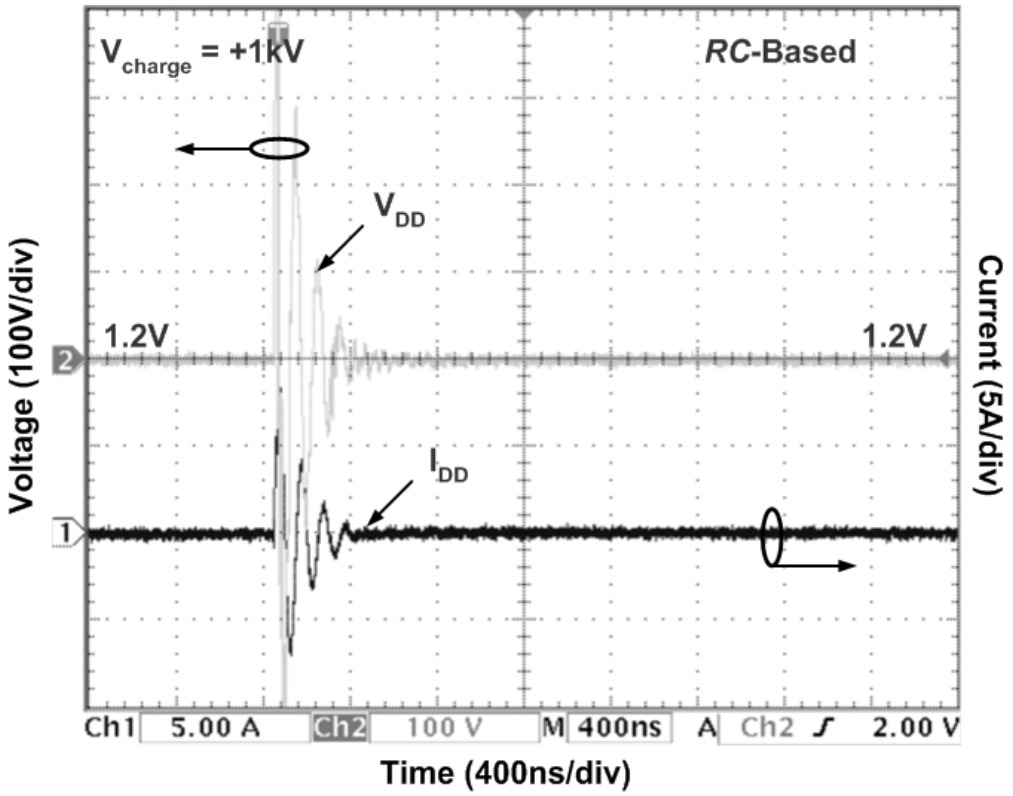
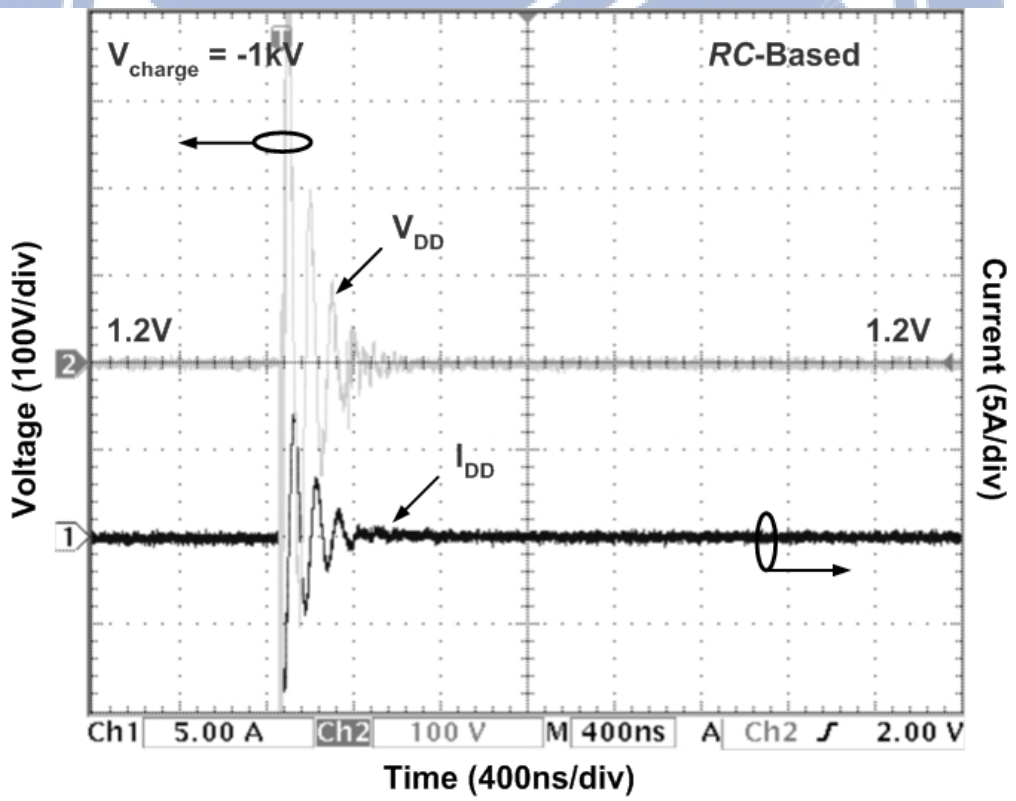


Fig. 3.12 The setup for transient-induced latch-up (TLU) measurement [44], [45].

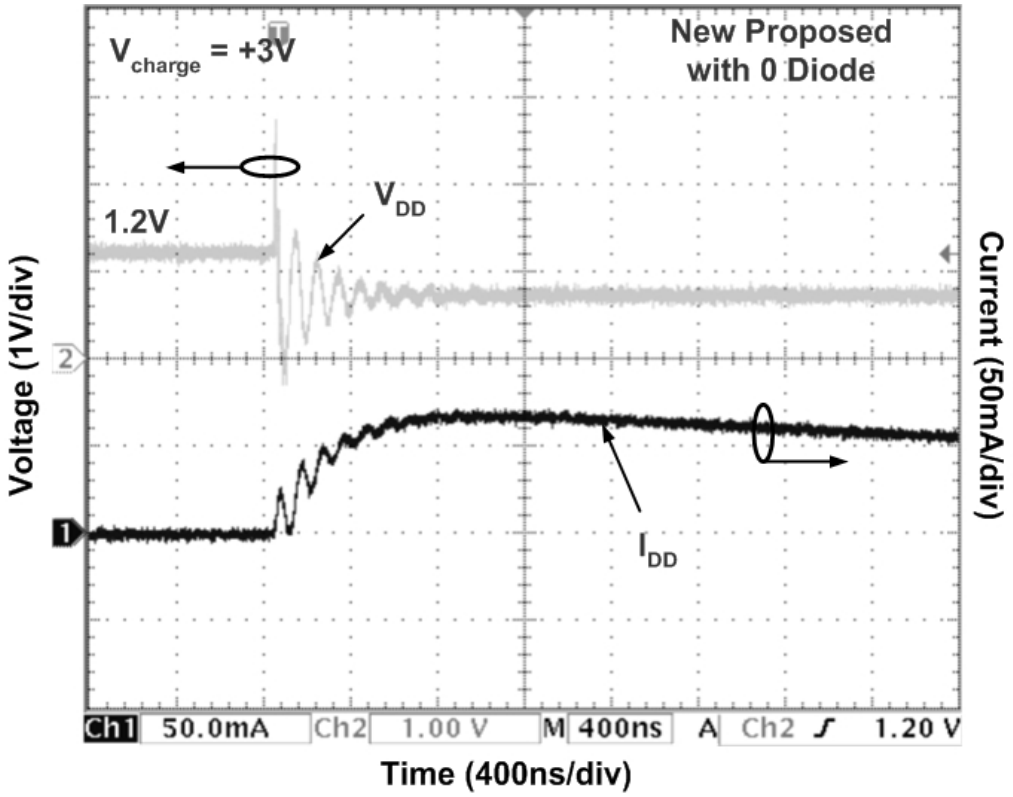


(a)

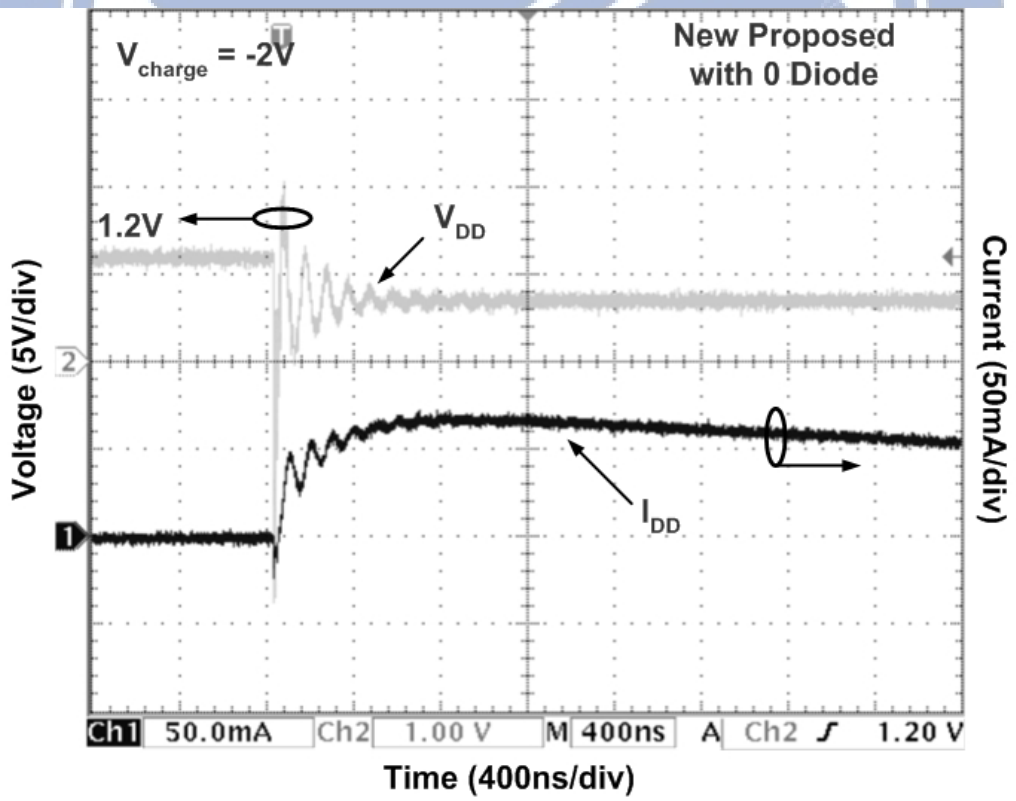


(b)

Fig. 3.13 Measured V_{DD} and I_{DD} waveforms on the traditional *RC*-based power-rail ESD clamp circuit under TLU measurement with V_{charge} of (a) +1kV and (b) -1kV.

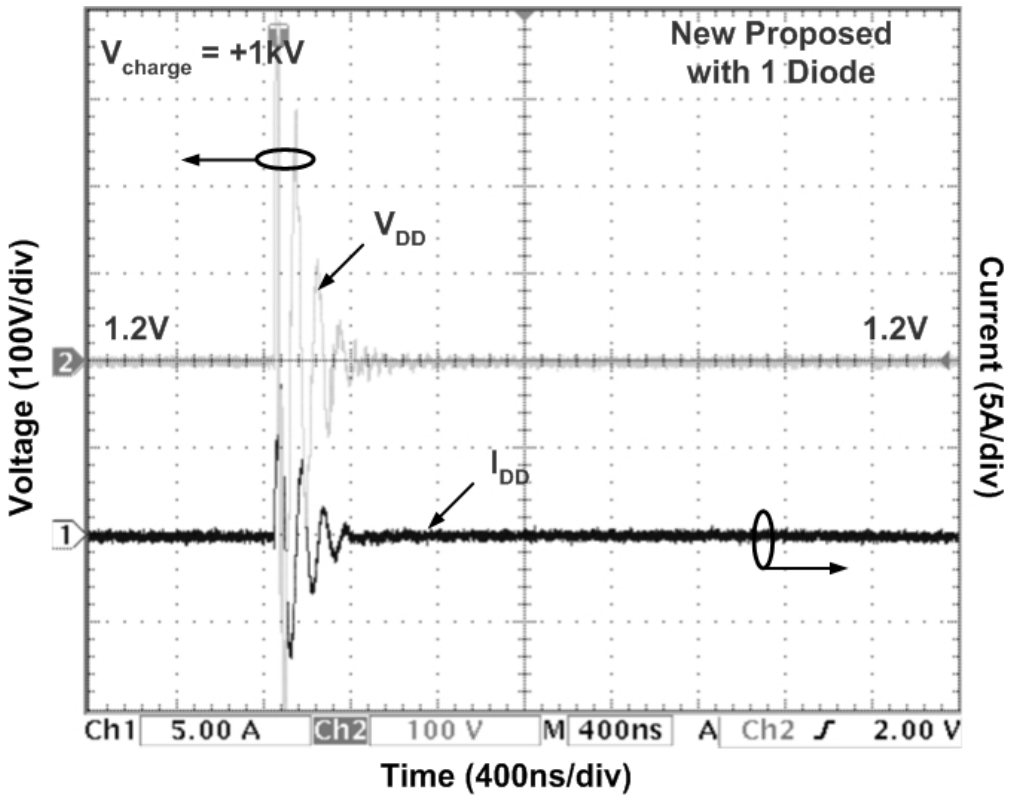


(a)

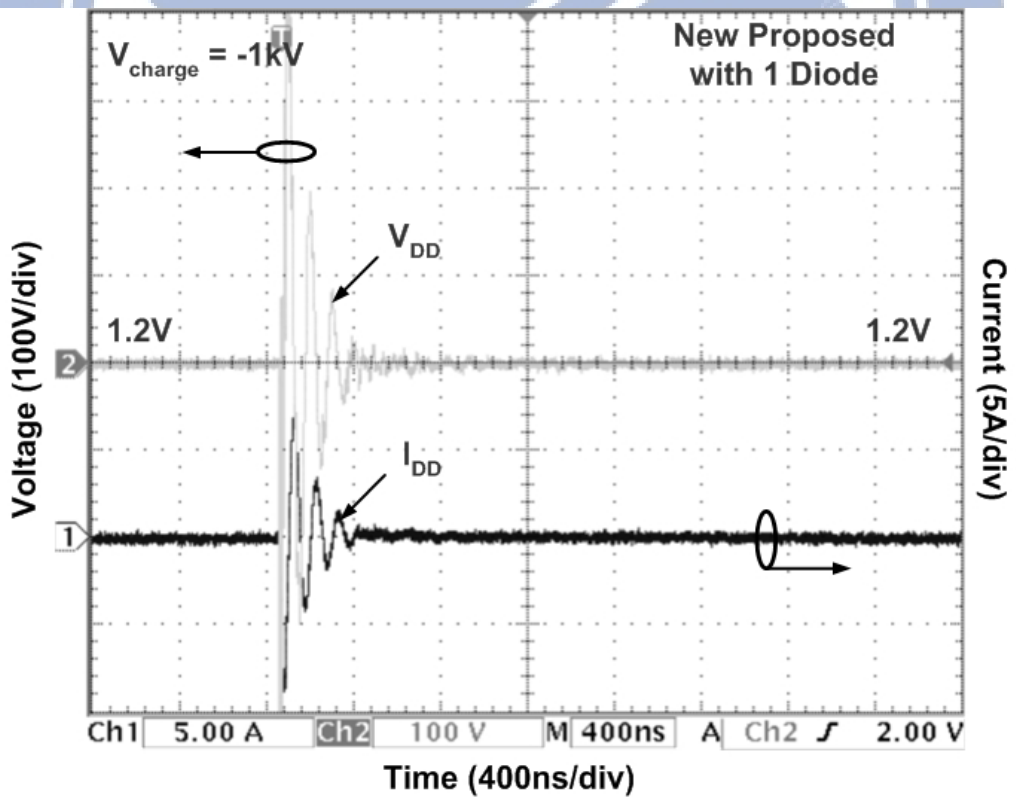


(b)

Fig. 3.14 Measured V_{DD} and I_{DD} waveforms on the new proposed power-rail ESD clamp circuit with no diode under TLU measurement with V_{charge} of (a) +3V and (b) -2V.



(a)



(b)

Fig. 3.15 Measured V_{DD} and I_{DD} waveforms on the new proposed power-rail ESD clamp circuit with one diode under TLU measurement with V_{charge} of (a) +1kV and (b) -1kV.

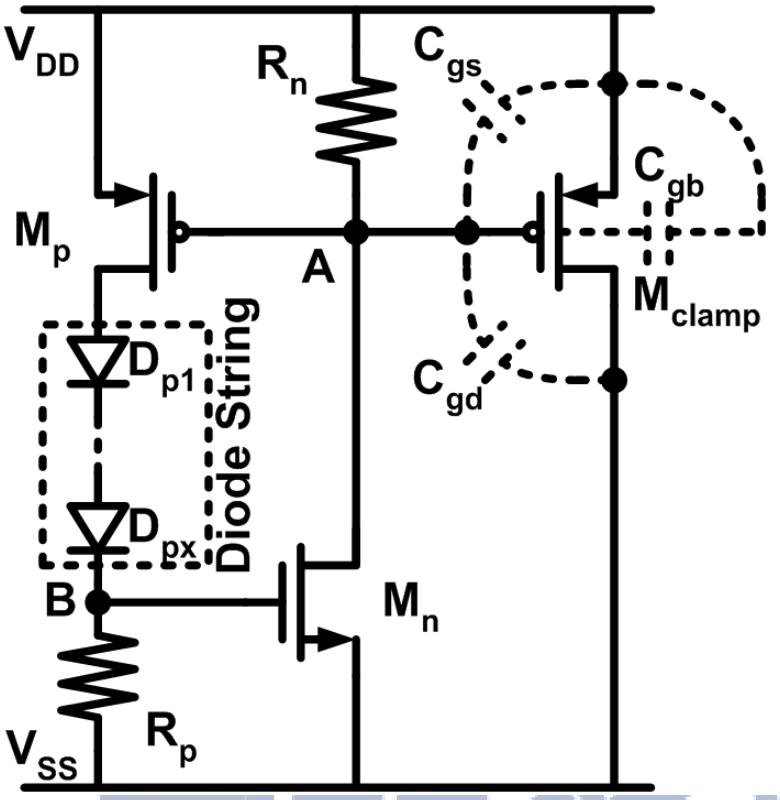
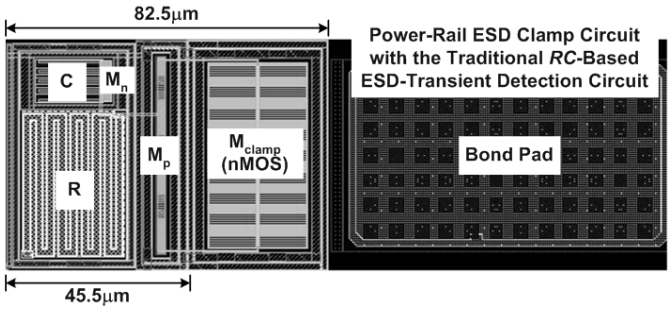
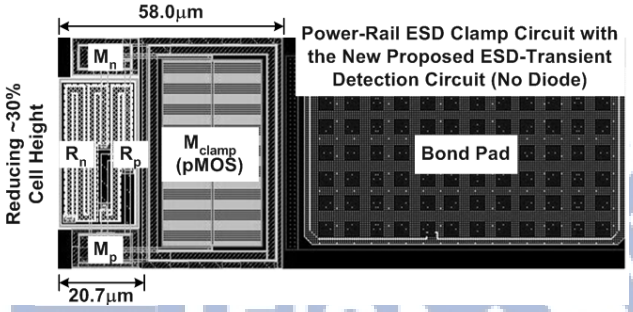


Fig. 3.16 New proposed power-rail ESD clamp circuit with ESD clamp pMOS transistor and diode string in the ESD-transient detection circuit.



(a)



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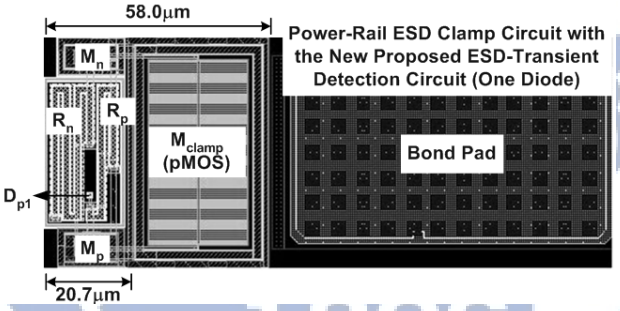
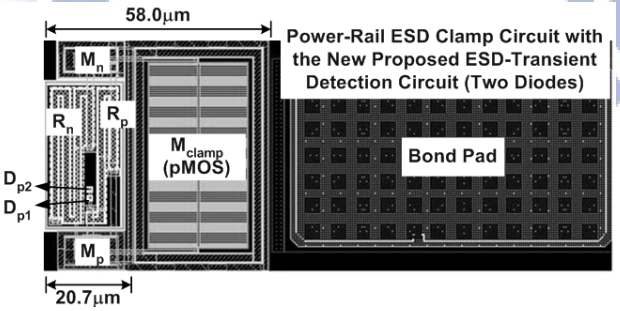
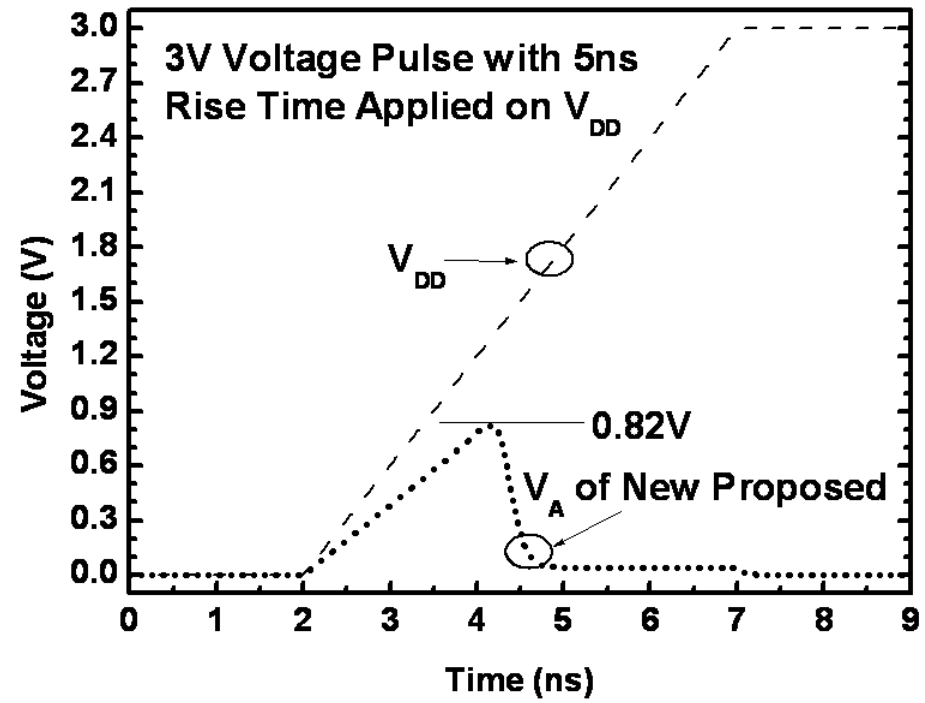


(c)

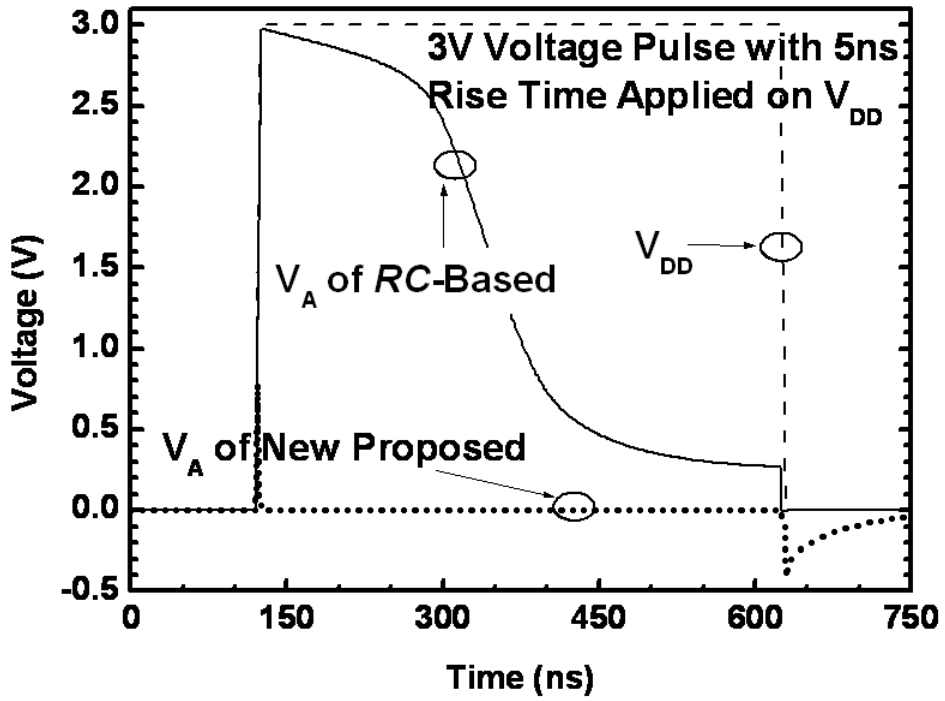


(d)

Fig. 3.17 Comparison on the layout areas among the four power-rail ESD clamp circuits. The M_{clamp} is drawn in a BigFET layout style with the same W/L=2000μm/0.1μm, which is triggered by (a) the traditional *RC*-based ESD-transient detection circuit, (b) the proposed ESD-transient detection circuit with no diode, (c) the proposed ESD-transient detection circuit with one diode, and (d) the proposed ESD-transient detection circuit with two diodes.



(a)



(b)

Fig. 3.18 The simulation results of the voltage transient on V_{DD} and node A under a 3V voltage pulse with a rise time of 5ns. (a) The voltage waveforms in the period of rising transition, and (b) the voltage waveforms during the whole voltage pulse of 500ns.

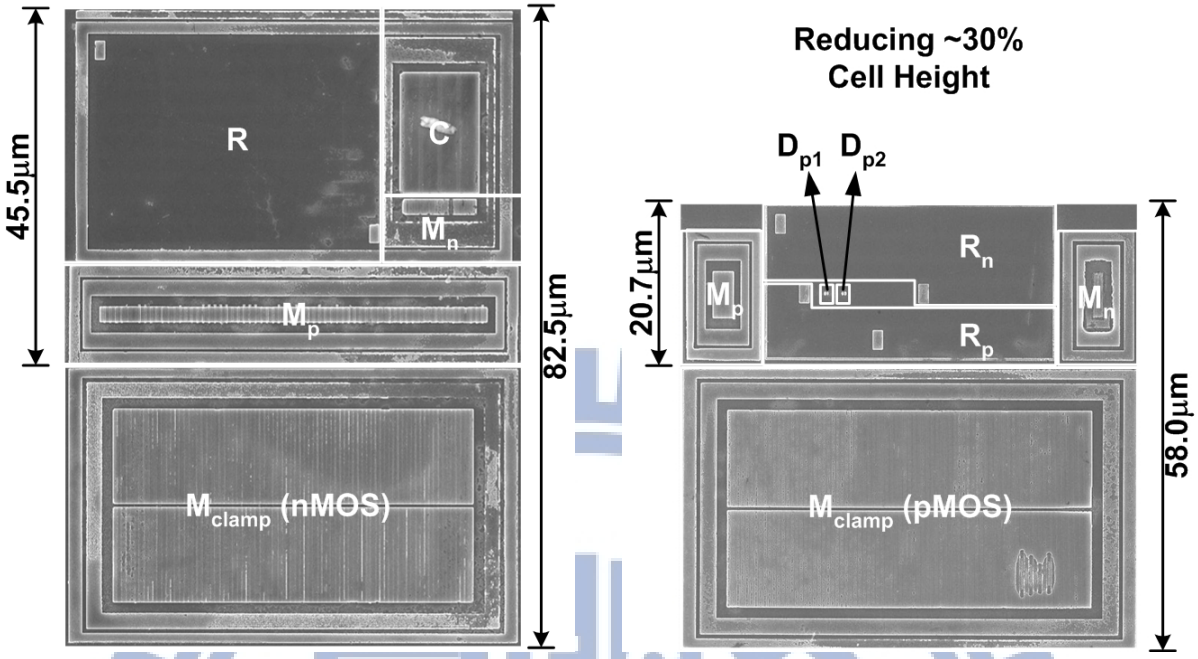


Fig. 3.19 Chip microphotographs of (a) the traditional *RC*-based power-rail ESD clamp circuit and (b) the proposed power-rail ESD clamp circuit with two diodes in its ESD-transient detection circuit.

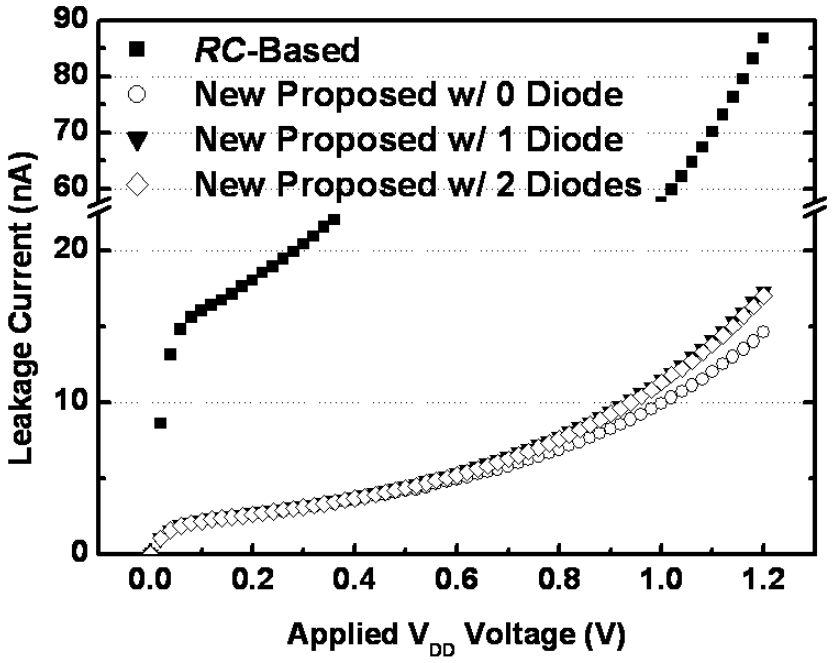
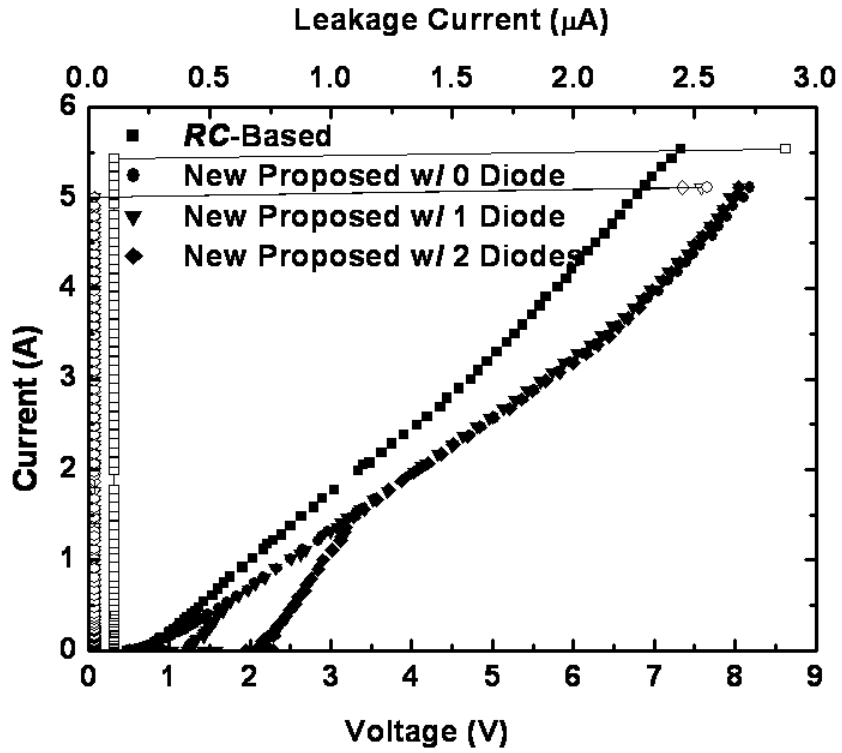
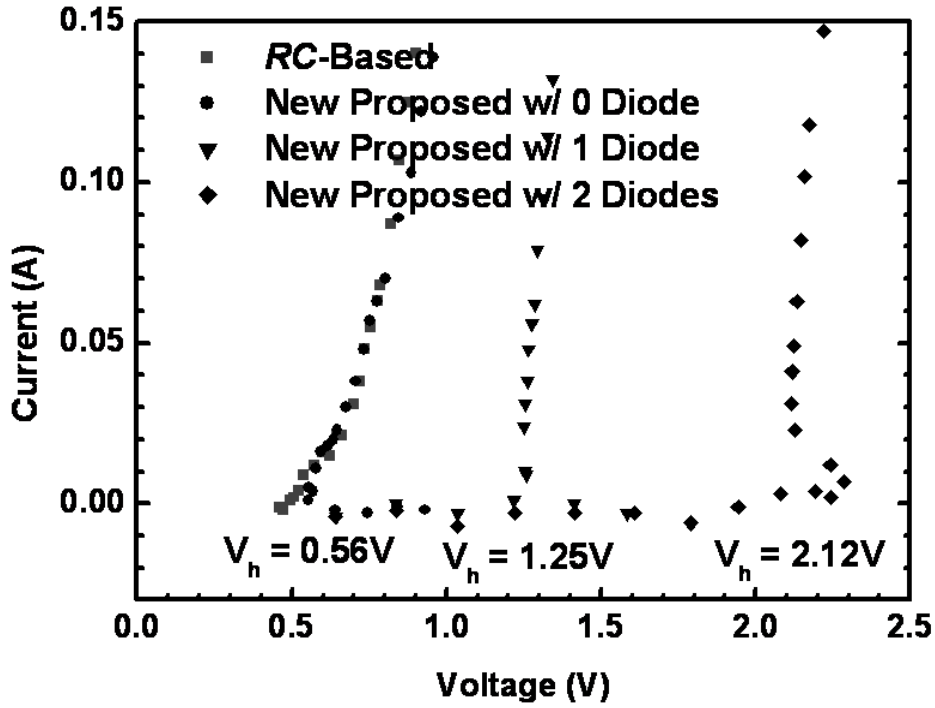


Fig. 3.20 The measured standby leakage current of the traditional *RC*-based and the proposed power-rail ESD clamp circuits at room temperature.

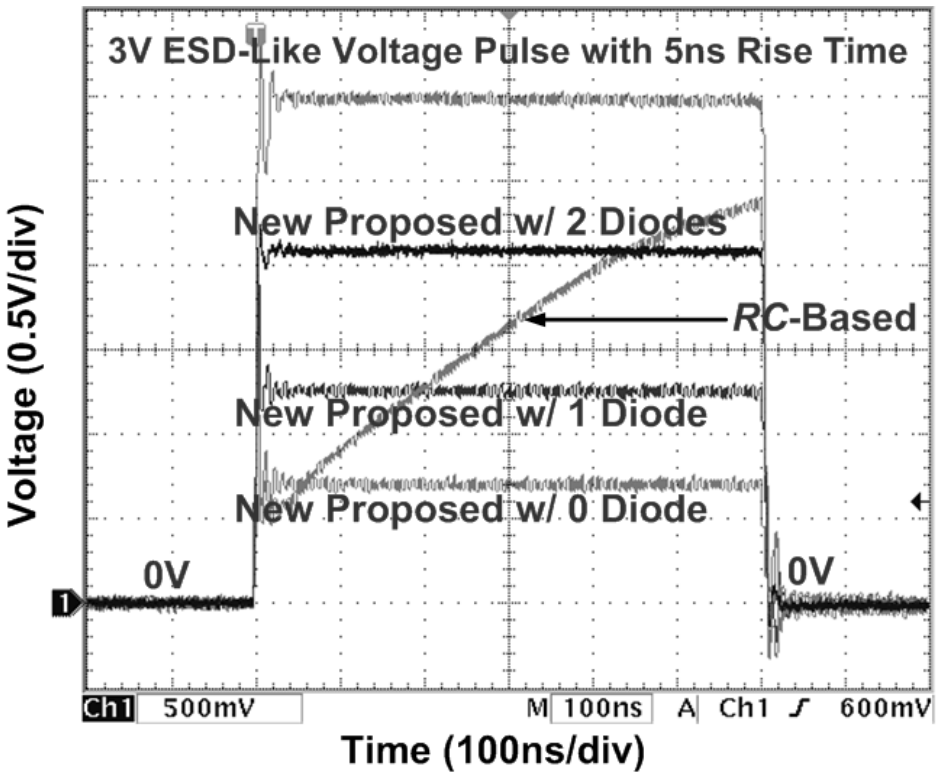


(a)

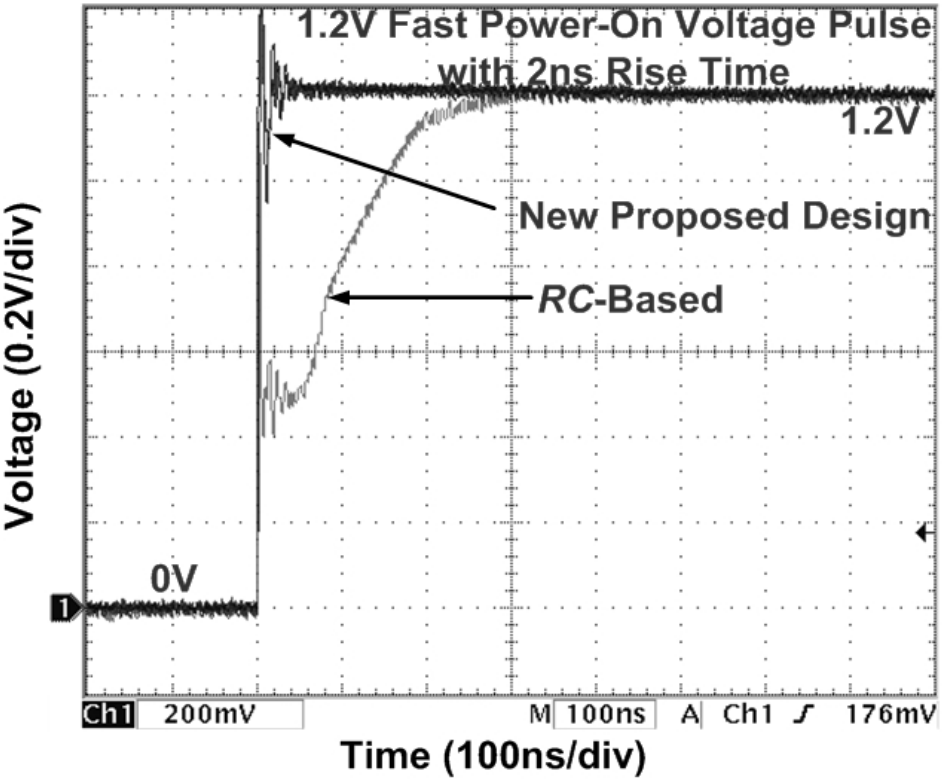


(b)

Fig. 3.21 TLP measured *I-V* curves of (a) the power-rail ESD clamp circuits and (b) the zoomed-in illustration for the holding voltages.

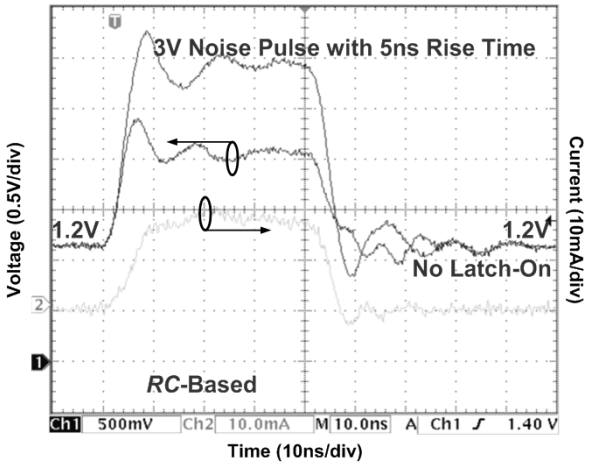


(a)

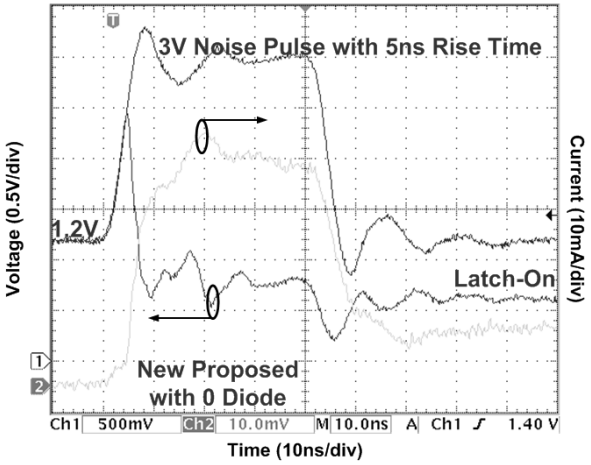


(b)

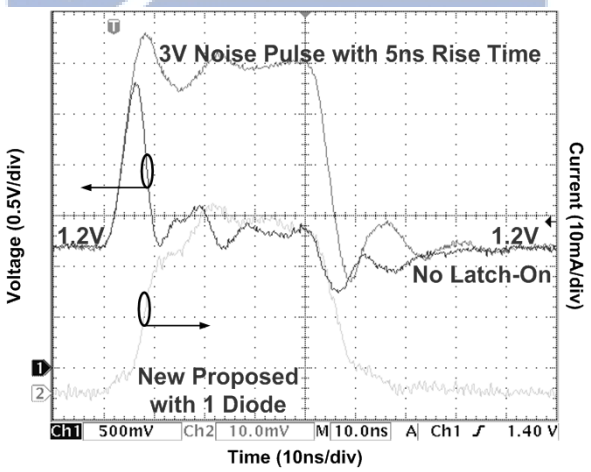
Fig. 3.22 The voltage waveforms monitored on the power-rail ESD clamp circuits under (a) ESD-transient-like condition and (b) fast power-on condition.



(a)

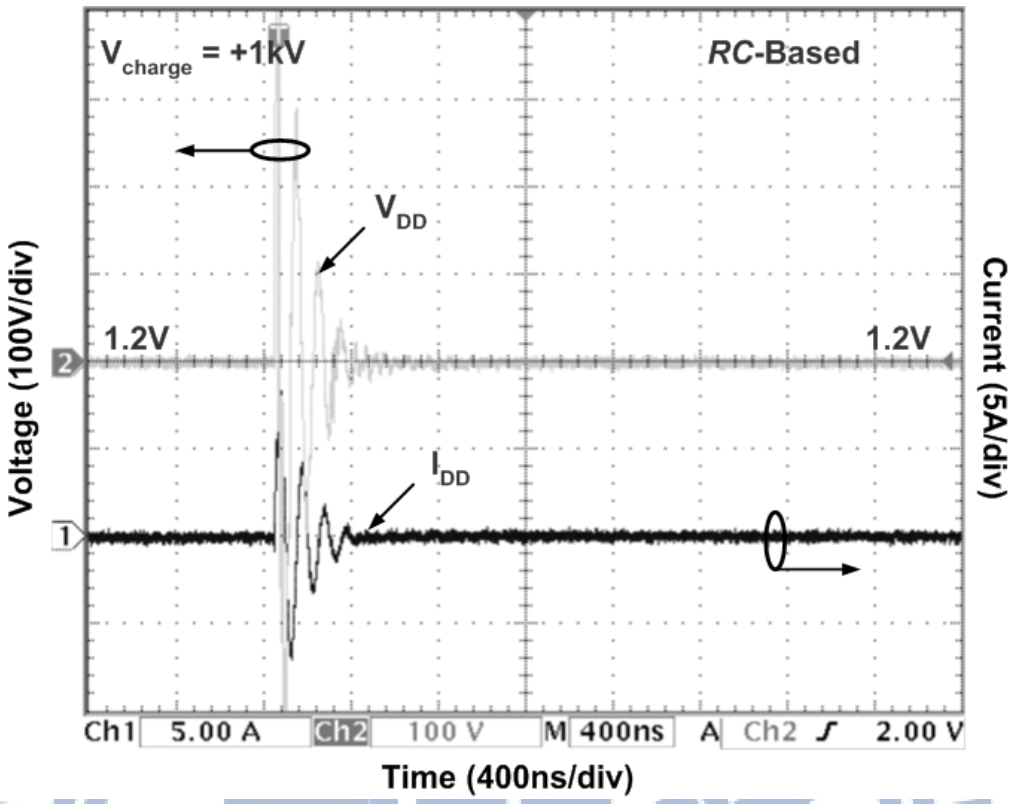


(b)

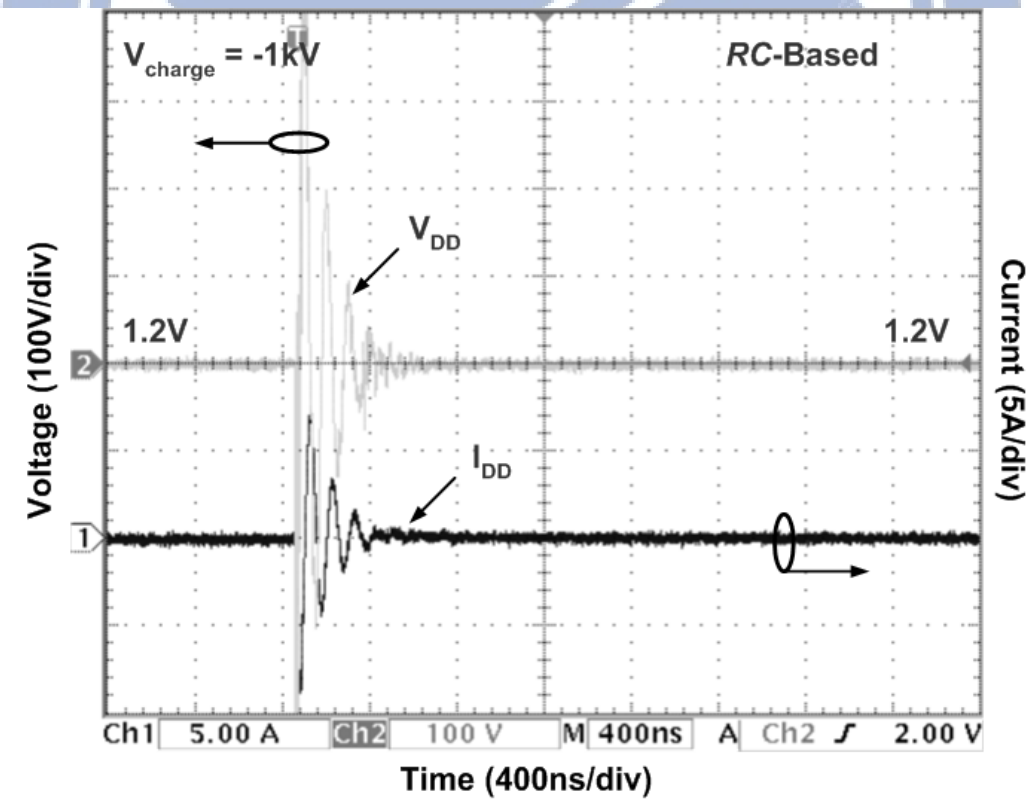


(c)

Fig. 3.23 The measured voltage and current waveforms of power-rail ESD clamp circuit, realized with (a) the traditional *RC*-based ESD-transient detection circuit, (b) the proposed ESD-transient detection circuit with no diode, and (c) the proposed ESD-transient detection circuit with one diode, under transient noise condition with 3V overshooting on 1.2V V_{DD}.

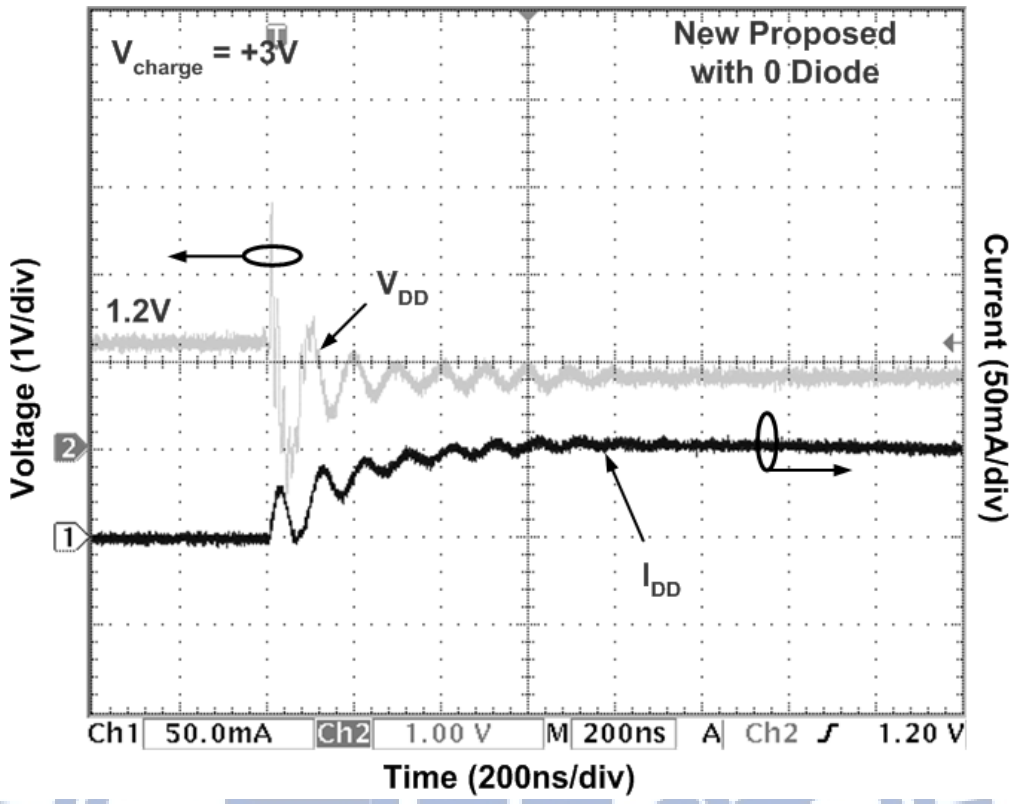


(a)

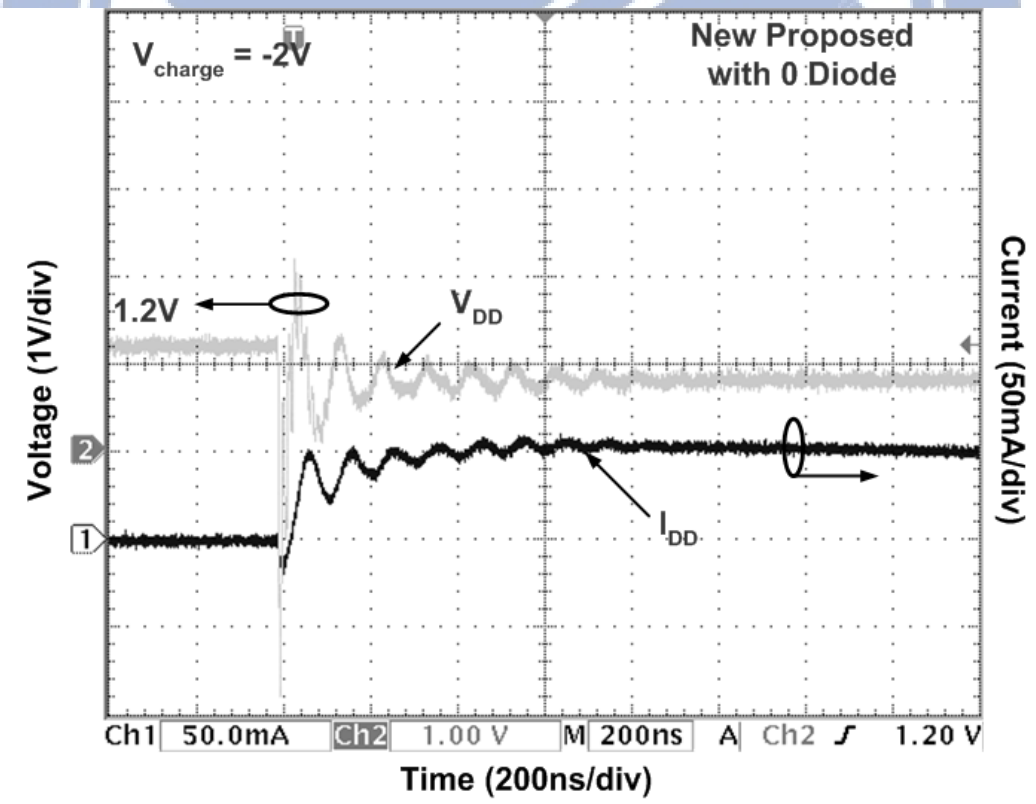


(b)

Fig. 3.24 Measured V_{DD} and I_{DD} waveforms on the traditional *RC*-based power-rail ESD clamp circuit under TLU measurement with V_{charge} of (a) +1kV and (b) -1kV.

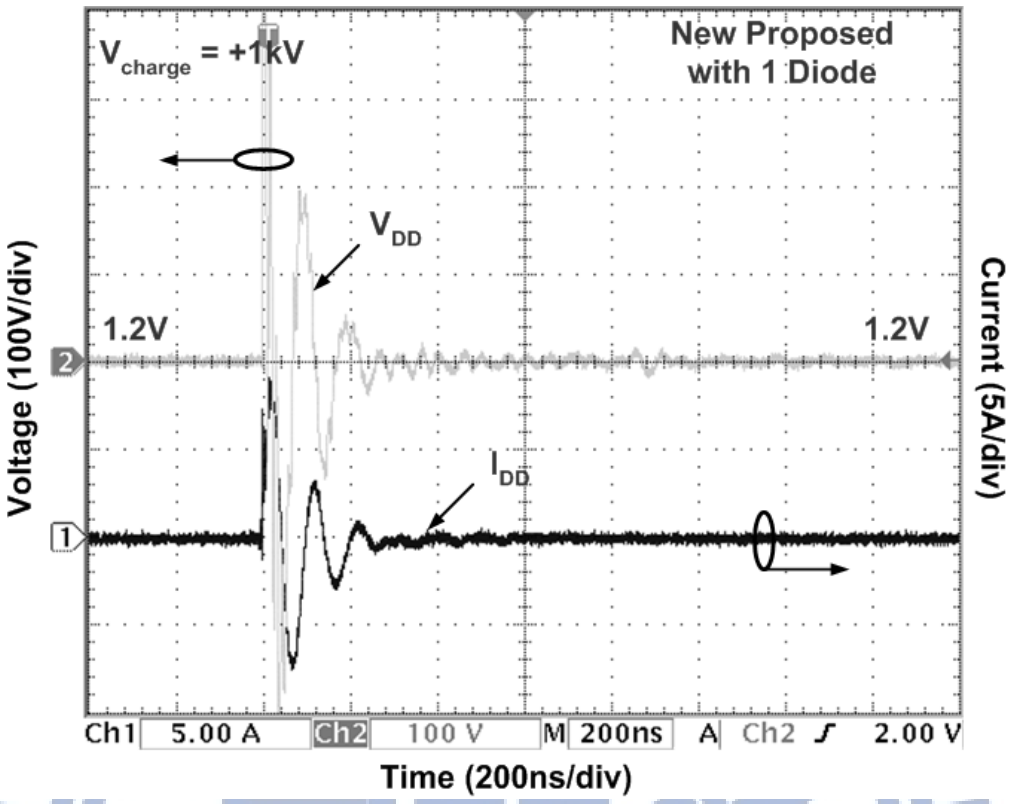


(a)

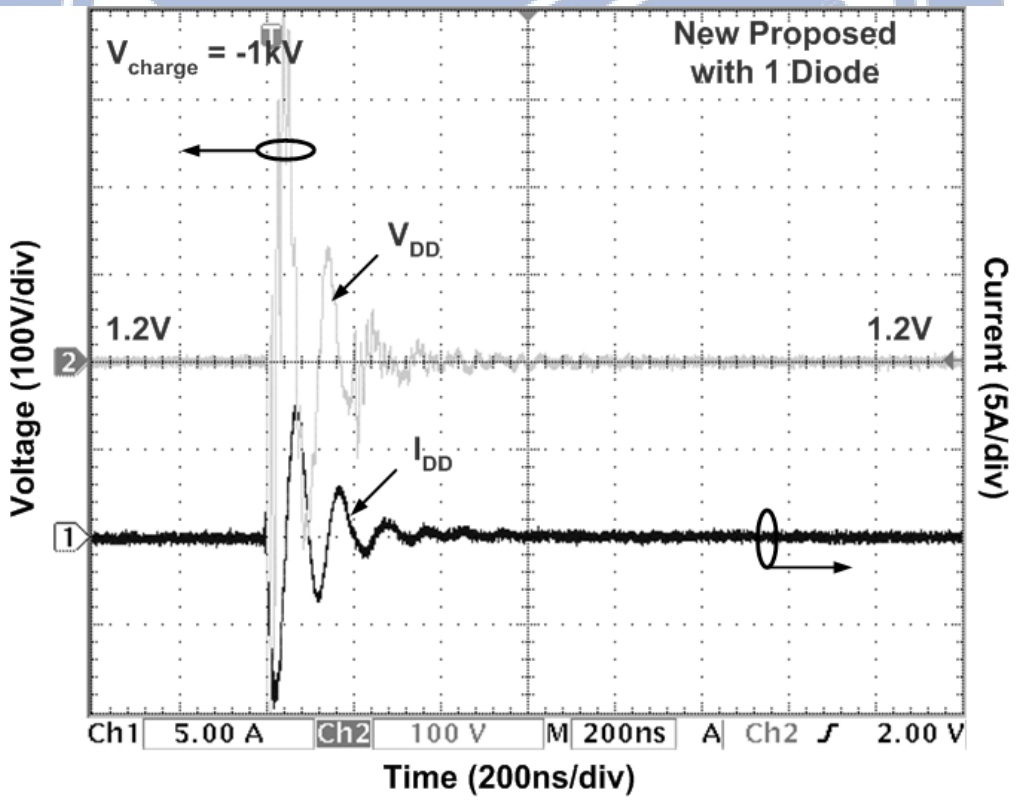


(b)

Fig. 3.25 Measured V_{DD} and I_{DD} waveforms on the new proposed power-rail ESD clamp circuit with no diode under TLU measurement with V_{charge} of (a) +3V and (b) -2V.



(a)



(b)

Fig. 3.26 Measured V_{DD} and I_{DD} waveforms on the new proposed power-rail ESD clamp circuit with one diode under TLU measurement with V_{charge} of (a) +1kV and (b) -1kV.

Chapter 4

Power-Rail ESD Clamp Circuit with Equivalent ESD-Transient Detection Mechanism

In this chapter, the power-rail ESD clamp circuits with equivalent ESD-transient detection mechanisms are presented. The conventional power-rail ESD clamp circuits with traditional *RC*-based design, smaller capacitance design, and capacitor-less design, are discussed in section 4.2. The power-rail ESD clamp circuit with equivalent capacitance-coupling detection mechanism is investigated in section 4.3, and the power-rail ESD clamp circuit with equivalent *RC*-based detection mechanism is discussed in section 4.4. All power-rail ESD clamp circuit were fabricated in a 65nm 1.2V fully silicided CMOS process.

4.1 Background

In advanced nanoscale CMOS technology, the ESD clamp device drawn in the layout style of BigFET had demonstrated excellent ESD protection performance [33]-[38]. In these power-rail ESD clamp circuits, the ESD clamp devices can discharge a large ESD current by the inversion channel layer without snapback operation of the parasitic BJT [39]-[42]. Practically, there are two different circuit skills, the *RC* delay technique [33]-[35] and the capacitance-coupling design [36]-[38], to realize the ESD-transient detection circuit in the power-rail ESD clamp circuit. The turn-on duration of the ESD clamp device is mainly controlled by the *RC* time constant of the *RC*-based ESD-transient detection circuit [33]-[35]. Therefore, the *RC* time constant would be designed large enough about several hundreds nanosecond to keep the ESD clamp device at “ON” state under the ESD stress condition. However, the extended *RC* time constant of the ESD-transient detection circuit suffers not only the larger layout area from the resistance and capacitance but also the mis-trigger of the ESD clamp device under fast power-on application [34]. In previous studies [33], [34], [37], [38], they demonstrated the power-rail ESD clamp circuits with feedback circuit methods to extend the turn-on duration by using a small *RC* time constant. However, the feedback circuit designs would suffer the latch-on issue under the fast power-on or the electrical fast transient

(EFT) conditions [46]. Moreover, some circuit designs, such as on-time control circuits [33] and multi-*RC*-triggered circuits [35], had also been used to extend the turn-on duration without the latch-on issue. However, those previous circuits are more complicated with large silicon layout area including the requested resistances and capacitances in the ESD-transient detection circuits.

4.2 Prior Arts of Power-Rail ESD Clamp Circuit

4.2.1 Traditional RC-Based Power-Rail ESD Clamp Circuit

The traditional *RC*-based power-rail ESD clamp circuit was widely used to protect the core circuits [8], as shown in Fig. 4.1. The *RC*-based ESD-transient detection circuit commands the ESD clamp nMOS transistor to turn on under ESD stress condition and to turn off under normal circuit operating condition. The turn-on time of the ESD clamp nMOS transistor can be adjusted by the *RC* time constant of the *RC*-based ESD-transient detection circuit to meet the half-energy discharging time of the HBM ESD event [1]. To meet the aforementioned requirements, the *RC* time constant of the *RC*-based ESD-transient detection circuit is designed about 0.1-1μs to achieve the desired operations.

4.2.2 Power-Rail ESD Clamp Circuit with Smaller Capacitance

A power-rail ESD clamp circuit with smaller capacitance that adopts the capacitance-coupling mechanism has been shown in Fig. 4.2 [36]. The smaller capacitor implemented in this work is MOS capacitor. The cascode nMOS transistors (Mnc1 and Mnc2) operated at the saturation region are used as a large resistor and combined with the smaller capacitor to construct a capacitance-coupling network. Under ESD stress condition, the potential of node A will be synchronously elevated toward a positive voltage potential by capacitance coupling of the smaller capacitor. Then, the gate terminal of the ESD clamp nMOS transistor will be promptly charged toward the positive voltage potential. Under normal circuit operating condition, the potential of node A will actually be kept at VSS through the high resistance path of the cascode nMOS transistors. Therefore, the ESD clamp nMOS transistor will be kept at the OFF state under normal circuit operating condition.

4.2.3 Capacitor-Less Design of Power-Rail ESD Clamp Circuit

The capacitor-less design of power-rail ESD clamp circuit with ESD clamp nMOS transistor has been proposed, as shown in Fig. 4.3(a) [47]. The large parasitic capacitances

(Cgd, Cgs, and Cgb) of M_{ESD} and resistor Rp can be used to form capacitance-coupling mechanism to control M_{ESD} under different operation conditions. The diode string in the ESD-transient detection circuit is used to adjust the holding voltage of the power-rail ESD clamp circuit to avoid from the transient-induced latch-on event [45].

The capacitor-less design of power-rail ESD clamp circuit with ESD clamp pMOS transistor was also proposed to protect the core circuits [48], as shown in Fig. 4.3(b). The large parasitic capacitances (Cgd, Cgs, and Cgb) of the ESD clamp pMOS transistor and the resistor Rn can be used to realize capacitance-coupling mechanism in the power-rail ESD clamp circuit. Under ESD stress condition, the voltage of node A will be quickly pulled down to the ground level to turn on the ESD clamp pMOS transistor. The diode string in the ESD-transient detection circuit is used to adjust the holding voltage of the power-rail ESD clamp circuit to avoid from the transient-induced latch-on event [45]. Under normal circuit operating condition, the power-rail ESD clamp circuit can be totally turned off because the voltages of nodes A and B are kept at VDD and VSS through the resistors Rn and Rp, respectively.

The device dimensions of the traditional *RC*-based design [8], the smaller capacitance design [36], and the capacitor-less designs [47], [48] fabricated in a 65nm 1.2V CMOS process are listed in Table 4.1. The device dimension of ESD clamp transistor M_{ESD} in all power-rail ESD clamp circuits verified in the silicon test chip is kept the same of 2000μm/100nm.

4.3 ESD Clamp Circuit with Equivalent Capacitance-Coupling Detection Mechanism

In this section, an ESD-transient detection circuit, which is combined with the parasitic diode of the ESD clamp nMOS transistor drawn in BigFET layout style, has been proposed and verified in a 65nm 1.2V CMOS process. The new proposed power-rail ESD clamp circuit has features of low leakage current, high immunity against mis-trigger, and high efficiency of layout area.

4.3.1 Circuit Schematic

The circuit schematic and cross-sectional view of the new proposed power-rail ESD clamp circuit with M_{ESD} drawn in BigFET layout style are shown in Figs. 4.4(a) and (b), respectively.

In Fig. 4.4(a), the body of M_{ESD} is not directly connected to VSS but to diode-connected Mnd and input node of controlling circuit, which is composed of two transistors (Mp and Mn) and two resistors (Rp and Rn). However, the body of M_{ESD} can be still biased to VSS through the parasitic p-substrate resistor Rsub due to P+ pickup elsewhere, as shown in Fig. 4.4(b).

There is a large-area reverse-biased diode Ddb existed in the drain and body of M_{ESD}. The other one exists in the body of M_{ESD} and the Nwell guard ring. These two parasitic diodes are used as the equivalent capacitors. The diode-connected Mnd and parasitic p-substrate resistor Rsub are used as the equivalent large resistors. Hence, an equivalent capacitance-coupling network is constructed without using an actual capacitor and resistor to greatly reduce the layout area.

4.3.2 Operation Mechanism under ESD Transition

When a positive fast transient ESD-like voltage is applied to VDD, the node Psub will be elevated by equivalent capacitance-coupling mechanism. Thus Mn can be quickly turned on and the controlling circuit can output a voltage level equal to that on VDD power line to command M_{ESD} at ON state. In order to simulate the fast transient edge of the HBM ESD event before the breakdown on the internal devices, a 4V voltage pulse with a rise time of 10ns is applied to VDD, as shown in Fig. 4.5 with the device sizes listed in Table 4.2 (adopting M_{ESD} width of 2000μm).

During this ESD-like transition, the voltage of node Psub is increased by capacitance-coupling network. Although the voltage of node Psub is nearly kept at the value of turn-on voltage of the parasitic diode Dsb, such a turn-on voltage is still larger than the threshold voltage of Mn to activate the controlling circuit. Therefore, the voltage of node Nb is quickly pulled up to the voltage level on VDD power line in ~4ns. Then, M_{ESD} can be successfully turned on to discharge the ESD current from VDD to VSS.

4.3.3 Experimental Results

The test chips of power-rail ESD clamp circuits had been fabricated in a 65nm 1.2V CMOS process. As shown in Figs. 4.6(a) ~ (d), the layout area of the proposed ESD-transient detection circuit is reduced by ~82% than that of traditional *RC*-based one.

4.3.3.1 Standby Leakage Current

The leakage current of the *RC*-based power-rail ESD clamp circuit is 88.66nA as listed in

Table 4.3. The leakage currents of the proposed power-rail ESD clamp circuits at 1.2V normal operation voltage are shown in Fig. 4.7. The proposed power-rail ESD clamp circuits have the leakage currents of the range from 30nA to 48nA, which is greatly reduced by ~46% compared with traditional *RC*-based one. Therefore, the proposed power-rail ESD clamp circuit with lower leakage current is more adequate for the portable product, which highly requires low standby current.

4.3.3.2 TLP Measurement and ESD Robustness

The TLP generator with a pulse width of 100ns and a rise time of ~2ns is used to measure the power-rail ESD clamp circuits [29]. The measured TLP *I-V* curves of the prior arts are shown in Fig. 4.8(a). The It2 of the prior arts with M_{ESD} width of 2000μm are both 5.34A. As shown in Fig. 4.8(b), the It2 of the new proposed power-rail ESD clamp circuit can achieve the same level of 5.39A. To observe the beginning of conduction in Fig. 4.8(b), the zoom-in illustration of TLP *I-V* curves is shown in Fig. 4.8(c). The curves of different Mnd widths both have the same Vt1 of ~2.9V because Rsub has a much smaller resistance than that of diode-connected Mnd. It is verified that capacitance-coupling network is mainly consisted by Ddb and Rsub. Overall, the measured holding voltages are ~2V, which is higher than the normal circuit operation voltage VDD of 1.2V. Therefore, the proposed power-rail ESD clamp circuits are free to latch-on issue for safely applying in 1.2V applications. In addition, the measured HBM (MM) ESD levels of all fabricated power-rail ESD clamp circuits with the M_{ESD} width of 2000μm are over ±8kV (+650V and -750V).

4.3.3.3 Turn-On Verification

A TLP voltage pulse with a rise time of ~2ns and a pulse height of 4V is applied to the VDD power line with the VSS grounded, as shown in Fig. 4.9(a). The applied 4V voltage pulse can be quickly clamped down to a lower voltage level of ~2.28V with the discharging current of ~32mA. The M_{ESD} can be successfully turned on to provide a low impedance path from VDD to VSS to discharge ESD current.

For the fast power-on condition, a voltage pulse with 1.2V and 20ns rise time is applied, as shown in Fig. 4.9(b). The measured voltage waveform is totally not degraded. Therefore, the proposed power-rail ESD clamp circuit has high immunity against mis-trigger.

4.4 ESD Clamp Circuit with Equivalent *RC*-Based Detection Mechanism

Low standby leakage of the power-rail ESD clamp circuit is highly demanded by the hand-held, portable, and battery powered products [38]. In advanced CMOS technology, the leakage current of nMOS was often larger than that of pMOS in the same device dimension. Besides, pMOS used as ESD clamp device has become important for low voltage and mixed voltage supply in deep submicron CMOS products [49], [50]. Hence, pMOS is suggested to be used as the ESD clamp device.

In this section, an ultra-area-efficient ESD-transient detection circuit, which is combined with the parasitic diode of the ESD clamp pMOS transistor drawn in BigFET layout style, has been proposed and verified in a 65nm 1.2V CMOS process. From the measured results, the new proposed power-rail ESD clamp circuit can achieve excellent electrical performances with greatly reduced layout area.

4.4.1 Circuit Schematic

The circuit schematic and the cross-sectional view of the new proposed ESD-transient detection circuit with the ESD clamp pMOS transistor drawn in BigFET layout style are shown in Figs. 4.10(a) and (b), respectively. In Fig. 4.10(a), the body of ESD clamp pMOS transistor is not connected to VDD but to the diode-connected pMOS transistor Mpd and the input node of the controlling circuit, which is composed of two transistors (Mp and Mn) and two resistors (Rp and Rn). The output node of the controlling circuit is connected to the gate of ESD clamp pMOS transistor to command the ESD clamp pMOS transistor at "ON" or "OFF" state. As shown in Fig. 4.10(b), there is a large-area reverse-biased diode existed in the body and the drain of ESD clamp pMOS transistor. The other one exists in the body of ESD clamp pMOS transistor and the P+ pickup. These two parasitic diodes are used as the equivalent capacitors and the diode-connected pMOS transistor Mpd is used as the equivalent resistor. Therefore, an equivalent *RC*-based ESD-transient detection mechanism is constructed without using an actual resistor and capacitor to significantly reduce the layout area.

4.4.2 Operation Principles

4.4.2.1 Normal Power-On Transition

Under the normal circuit operating condition, the body voltage of ESD clamp pMOS

transistor (Nwell in Fig. 4.10(a)) can be biased toward VDD through the diode-connected transistor Mpd. The diode-connected transistor Mpd acts as an equivalent large resistor to charge the Nwell node toward VDD. Then, the controlling circuit can output a voltage level of VDD to command the ESD clamp pMOS transistor at "OFF" state.

With the SPICE parameters provided from foundry and the device sizes listed in Table 4.4 (adopting M_{ESD} width of 2000μm), the simulated voltage waveforms and the leakage current of the proposed power-rail ESD clamp circuit during the normal power-on transition are shown in Fig. 4.11(a). In Fig. 4.11(a), the voltage of node Nwell can be smoothly charged to the voltage level near VDD through the diode-connected transistor Mpd. When the width of Mpd is 4μm (20μm), the voltage of node Nwell is charged to 1.130V (1.164V). At the same time, the body current of M_{ESD} is 238pA (354pA). This body current is obviously not provided by the parasitic forward-biased diode Dsb of ESD clamp pMOS transistor as shown in Fig. 4.11(b) because the forward-biased current is only in the order of femto-ampere (fA). On the contrary, the drain current of Mpd with 4μm (20μm) width is 238pA (354pA) when it dissipates ~69mV (~35mV) voltage drop. Mpd with smaller width would cause larger voltage drop to provide drain current. As a result, Mp would not be completely turned off to induce more leakage current. Therefore, the simulated total standby leakage current is 45nA (31nA) for Mpd width of 4μm (20μm) when VDD is raised up to 1.2V with a rise time of 1ms.

4.4.2.2 ESD Transition

When a positive fast transient ESD-like voltage is applied to VDD with VSS grounded, the *RC* time constant keeps the node Nwell at a relatively low voltage level as compared with that on VDD power line. The *RC* time constant is consisted by the equivalent resistor implemented by diode-connected transistor Mpd, and the equivalent capacitors from parasitic diodes of Nwell/Psub and Nwell/drain junctions. Consequently, Mp can be quickly turned on and the controlling circuit can output a voltage level of VSS to command the ESD clamp pMOS transistor at "ON" state.

In order to simulate the fast transient edge of the HBM ESD event before the breakdown on the internal devices, a 4V voltage pulse with a rise time of 10ns is applied to VDD. The simulated voltage waveforms of the new proposed power-rail ESD clamp circuit during such an ESD-like transition are illustrated in Fig. 4.12. During this ESD-like transition, the voltage of node Nwell is increased much slower than that on the VDD power line due to *RC* time constant at node Nwell. The voltage difference between the VDD power line and node Nwell

is nearly kept at the value of turn-on voltage of the diode Dsb. However, such a turn-on voltage of the diode Dsb is still larger than the threshold voltage of Mp to activate the controlling circuit. Therefore, the voltage level of node Nb is successfully pulled down to the VSS level in about 4ns. Therefore, the ESD clamp pMOS transistor can be fully turned on to discharge the ESD current from VDD to VSS.

In Fig. 4.12, the voltages of node Nwell are slightly different under different Mpd width. The equivalent resistance of Mpd with smaller width is larger than that of Mpd with larger width. As a result, the voltage of node Nwell under smaller Mpd width would be slightly lower due to larger *RC* time constant. Besides, the body and the source of ESD clamp pMOS transistor are not connected together. It will induce the body effect of MOSFET to influence the conduction behavior of ESD clamp pMOS transistor. This phenomenon will be observed and discussed in the following experimental results.

4.4.3 Experimental Results

The test chips of power-rail ESD clamp circuits with the traditional *RC*-based, smaller capacitance, capacitor-less, and new proposed ultra-area-efficient ESD-transient detection circuits have been fabricated in a 65nm 1.2V CMOS process, as shown in Figs. 4.13(a) ~ (d). The dimension of M_{ESD} in all circuits verified in the silicon test chip is kept 2000μm/100nm. Compared with the power-rail ESD clamp circuit with the traditional *RC*-based ESD-transient detection circuit, the layout area of the whole new proposed power-rail ESD clamp circuit is reduced by ~46%, and the layout area of the ultra-area-efficient ESD-transient detection circuit is reduced by ~82%. These circuits are prepared for leakage measurement, ESD robustness and TLP measurement, very fast TLP (VF-TLP) measurement, and turn-on verification.

4.4.3.1 Standby Leakage Current

The leakage currents of the fabricated power-rail ESD clamp circuits are measured by HP4155 from 0V to 1.2V with the voltage step of 20mV at 25°C, as shown in Fig. 4.14(a) for the prior art designs and in 4.14(b) for the new proposed design. The leakage currents of the traditional *RC*-based design and the smaller capacitance design are 88.66nA and 85.22nA at room temperature, respectively. At the same device width of 2000μm, the leakage current of the capacitor-less design can be reduced to only 12.97nA due to ESD clamp pMOS transistor. For the new proposed design, the leakage current is 23.35nA for Mpd width of 20μm.

Because the body node of ESD clamp pMOS transistor is not fully biased to VDD, the transistor Mp would not be fully turned off to increase the total leakage current (as shown in Fig. 4.11(a)). Although the leakage current of the new proposed design is slightly larger than that of the capacitor-less design, it is still reduced by ~74%, compared with that of traditional *RC*-based design. The measured standby leakage currents of the fabricated power-rail ESD clamp circuits under 1.2V bias at different temperatures are also listed in Table 4.5. At higher temperatures, it can be observed that the increasing percentage of leakage current of the new proposed design is much better than those of the prior art designs.

4.4.3.2 TLP Measurement and ESD Robustness

The TLP generator with a pulse width of 100ns and a rise time of ~2ns is used to measure the fabricated power-rail ESD clamp circuits [29]. The measured TLP *I-V* curves of the prior arts are shown in Fig. 4.15. The It2 of the traditional *RC*-based and the smaller capacitance designs of the power-rail ESD clamp circuits with M_{ESD} width of 2000μm are both 5.31A. However, the It2 of the capacitor-less design of the power-rail ESD clamp circuit is 4.83A due to ESD clamp pMOS transistor. As shown in Fig. 4.16(a), the It2 of the new proposed power-rail ESD clamp circuit can achieve the same level as that of capacitor-less design at the specific M_{ESD} width. To observe the beginning of conduction in Fig. 4.16(a), the zoom-in illustration of TLP *I-V* curves is shown in Fig. 4.16(b). The curves of different Mpd widths start to rise at different voltage level due to the body effect of ESD clamp pMOS transistor. For the Mpd width of 4μm, the body effect is worse and the threshold voltage of ESD clamp pMOS transistor would be smaller. As a result, the TLP *I-V* curves for the Mpd width of 4μm rise at lower voltage level of ~1.3V (It is ~1.8V for the Mpd width of 20μm). In addition, the DC *I-V* curves of the ultra-area-efficient designs are measured (using TEK370 curve tracer) by applying a voltage sweep on the VDD power line to verify the dependence on the body effect of ESD clamp pMOS transistor and the holding voltage of the new proposed power-rail ESD clamp circuit. In Fig 4.16(c), the circuit with the Mpd width of 4μm surely has lower holding voltage of ~1.76V due to more serious body effect and it is high to ~1.95V for the Mpd width of 20μm when the width of ESD clamp pMOS transistor is kept at 2000μm. Overall, the measured holding voltages are all higher than the normal circuit operation voltage VDD of 1.2V no matter what kind of measurement is taken. Therefore, the proposed power-rail ESD clamp circuits are free to latchup issue for safely applying in 1.2V applications [51], [52].

The measured HBM and MM ESD levels of the fabricated power-rail ESD clamp circuits under positive and negative VDD-to-VSS ESD stresses are listed in Table 4.6. The measured HBM (MM) ESD level of the ESD clamp pMOS transistor with the width of 2000μm is over ±8kV (+500V and -700V). Overall, the measured HBM and MM ESD levels of the proposed power-rail ESD clamp circuits are well proportional to the width of ESD clamp pMOS transistor.

Charged-device model (CDM) is also an important ESD testing standard for ICs. In order to investigate the turn-on behavior of the new proposed designs under CDM-like fast transient condition, the very fast TLP (VF-TLP) with a pulse width of 10ns and a rise time of 200ps is used to measure the new proposed power-rail ESD clamp circuits. The measured VF-TLP *I-V* curves of the power-rail ESD clamp circuits with different M_{ESD} widths are shown in Fig. 4.17, where the width of Mpd is kept at 20μm. In Fig. 4.17, the new proposed power-rail ESD clamp circuits can be successfully activated to achieve higher It2 than those measured by TLP measurement due to the shorter pulse width of VF-TLP. In addition, the measured It2 from VF-TLP are also well proportional to the width of ESD clamp pMOS transistor.

4.4.3.3 Turn-On Verification

For normal power-on condition, the voltage pulse usually has a rise time in the order of milliseconds. As shown in Fig. 4.18(a), the measured voltage on VDD power line successfully rises up to 1.2V in 1ms without any degradation and the measured current is near zero. However, some previous studies [36], [46] have demonstrated that the power-rail ESD clamp circuits with *RC*-based ESD-transient detection circuits were easily mis-triggered or into the latch-on state under the fast power-on condition. The new proposed power-rail ESD clamp circuit has also been applied with 1.2V voltage pulse with 20ns rise time to investigate the immunity against mis-trigger under the fast power-on condition, as shown in Fig. 4.18(b). The measured voltage on VDD power line still can rise up to 1.2V with tiny deviation in the beginning period of ~5ns. However, the measured current waveform is smooth at the level near zero. Therefore, the new proposed power-rail ESD clamp circuit can be still free from the mis-trigger issues.

The transient voltage with a pulse height of 4V and a rise time of 10ns is applied to the VDD power line with 1.2V normal operation voltage to verify the latch-on issue. As shown in Fig. 4.19(a), the transient voltage pulse can activate the ESD-transient detection circuit to command the ESD clamp pMOS transistor at ON state. The applied 4V voltage pulse is

clamped down to a lower voltage level of ~2.2V by the new proposed power-rail ESD clamp circuit with discharging current of ~35mA. After the transient, the voltage on VDD power line is back to 1.2V operation voltage and the current is almost zero.

In order to observe the transient behavior of the proposed power-rail ESD clamp circuit, a TLP voltage pulse with a rise time of ~2ns and a pulse height of 4V is applied to the VDD power line with the VSS grounded. The TLP voltage pulse can quickly initiate the new proposed power-rail ESD clamp circuit. The measured voltage and current waveforms in time domain on VDD power line under 4V voltage pulse are shown in Fig. 4.19(b). The applied 4V voltage pulse can be quickly clamped down to a lower voltage level of ~1.71V by the new proposed power-rail ESD clamp circuit with the discharging current of ~45mA. When the TLP voltage pulse height is increased, the new proposed power-rail ESD clamp circuit can discharge more current. The turned-on ESD clamp pMOS transistor can provide a low impedance path from VDD to VSS to discharge ESD current and clamp down the voltage level. Overall, the new proposed ultra-area-efficient ESD-transient detection circuit can be successfully activated by the voltage pulse with fast transient edge to turn on the ESD clamp pMOS transistor.

4.5 Summary

The new proposed ESD-transient detection circuit with equivalent capacitance-coupling and equivalent *RC*-based ESD-transient detection mechanism has been proposed and successfully verified in a 65nm 1.2V CMOS technology. According to the measured results, the proposed power-rail ESD clamp circuit has good ESD robustness and excellent immunity against the transient-induced latch-on or mis-trigger issues and good proportionality between the width of ESD clamp device and the ESD robustness. Moreover, the proposed ESD-transient detection circuit saves the layout area by ~82% compared with the traditional *RC*-based ESD-transient detection circuit. The new proposed power-rail ESD clamp circuit is an excellent circuit solution to achieve effective and efficient on-chip ESD protection in advanced nanoscale CMOS technologies.

Table 4.1

Device Dimension of Prior Arts of Power-Rail ESD Clamp Circuit

Device Dimension	Traditional *RC*-Based Design [8]	Smaller Capacitance Design [36]	Capacitor-Less Design [47], [48]
Capacitor (Mc)	64μm / 2μm (W/L)	8μm / 60nm	None
Resistor (Ω)	R = 165.3k	R = 1.8k	Rn = 40k ; Rp = 20k
pMOS Transistor (Mp)	184μm / 60nm	184μm / 60nm	24μm / 60nm
nMOS Transistor (Mn)	36μm / 60nm	36μm / 60nm	12μm / 60nm
Diodes (Dp1 and Dp2)	None	None	0.057μm^2
Mnc1, Mnc2, and Mns	None	Mnc1 = 8μm / 60nm Mnc2 = 8μm / 60nm Mns = 60μm / 60nm	None
ESD Clamp Transistor (M_{ESD})	2000μm / 100nm (nMOS)	2000μm / 100nm (nMOS)	2000μm / 100nm (nMOS & pMOS)

Table 4.2

Device Sizes of Proposed Power-Rail ESD Clamp Circuit with ESD Clamp nMOS Transistor

Device Dimension	Ultra-Area-Efficient Power-Rail ESD Clamp Circuit					
Resistor (Ω)	Rn = 3.6k ; Rp = 6k					
MOS Transistors	Mn = 20μm / 60nm ; Mp = 24μm / 60nm					
Mnd	60μm / 60nm			12μm / 60nm		
ESD Clamp nMOS Transistor (M_{ESD})	2000μm / 100nm	1600μm / 100nm	1200μm / 100nm	2000μm / 100nm	1600μm / 100nm	1200μm / 100nm

Table 4.3

Leakage Currents of the Power-Rail ESD Clamp Circuits

Leakage @ 1.2V	Traditional *RC*-Based [8]	Smaller Capacitance [36]	Capacitor-Less Design [47]		
			2000μm	1600μm	1200μm
25°C	88.66nA	85.22nA	42.39nA	33.34nA	25.28nA
75°C	0.71μA	0.78μA	0.48μA	0.40μA	0.32μA
125°C	4.74μA	4.83μA	3.80μA	3.07μA	2.38μA

Leakage @ 1.2V	Ultra-Area-Efficient Design					
	Mnd Width = 60μm			Mnd Width = 12μm		
M_{ESD} Width	2000μm	1600μm	1200μm	2000μm	1600μm	1200μm
25°C	48.32nA	38.18nA	31.29nA	46.57nA	38.06nA	30.00nA
75°C	0.53μA	0.43μA	0.33μA	0.53μA	0.43μA	0.33μA
125°C	3.56μA	2.79μA	2.24μA	3.42μA	2.75μA	2.10μA

Table 4.4

Device Sizes of Proposed Power-Rail ESD Clamp Circuit with ESD Clamp pMOS Transistor

Device Dimension	Ultra-Area-Efficient Power-Rail ESD Clamp Circuit					
Resistor (Ω)	Rn = 3.6k ; Rp = 6k					
MOS Transistors	Mn = 20μm / 60nm ; Mp = 24μm / 60nm					
Diode-Connected Transistor (Mpd)	4μm / 60nm			20μm / 60nm		
ESD Clamp pMOS Transistor (M_{ESD})	2000μm / 100nm	1600μm / 100nm	1200μm / 100nm	2000μm / 100nm	1600μm / 100nm	1200μm / 100nm

Table 4.5

Leakage Currents of the Power-Rail ESD Clamp Circuits

Leakage @ 1.2V	Traditional *RC*-Based [8]	Smaller Capacitance [36]	Capacitor-Less Design [48]		
M_{ESD} Width	2000μm (nMOS)	2000μm (nMOS)	2000μm	1600μm	1200μm
25°C	88.66nA	85.22nA	12.97nA	10.91nA	8.40nA
75°C	0.71μA	0.78μA	0.15μA	0.13μA	0.11μA
125°C	4.74μA	4.83μA	1.37μA	1.09μA	0.82μA

Leakage @ 1.2V	Ultra-Area-Efficient Design					
	Mpd Width = 4μm			Mpd Width = 20μm		
M_{ESD} Width	2000μm	1600μm	1200μm	2000μm	1600μm	1200μm
25°C	49.46nA	38.92nA	29.88nA	23.35nA	21.29nA	19.67nA
75°C	0.34μA	0.26μA	0.22μA	0.22μA	0.19μA	0.15μA
125°C	2.06μA	1.59μA	1.28μA	1.43μA	1.21μA	0.91μA

Table 4.6

ESD Robustness of Fabricated Power-Rail ESD Clamp Circuits

ESD Robustness	Traditional *RC*-Based [8]	Smaller Capacitance [36]	Capacitor-Less Design [48]		
M_{ESD} Width	2000μm (nMOS)	2000μm (nMOS)	2000μm	1600μm	1200μm
It2 (A)	5.31	5.30	4.83	4.05	3.14
HBM (kV)	> ± 8	> ± 8	> ± 8	> ± 8	> ± 8
MM (V)	+ 650 - 750	+ 650 - 750	+ 500 - 700	+ 400 - 600	+ 300 - 450

ESD Robustness	Ultra-Area-Efficient Design					
	Mpd Width = 4μm			Mpd Width = 20μm		
M_{ESD} Width	2000μm	1600μm	1200μm	2000μm	1600μm	1200μm
It2 (A)	4.96	3.92	3.00	4.95	3.98	3.06
HBM (kV)	> ± 8	> ± 8	> ± 8	> ± 8	> ± 8	> ± 8
MM (V)	+ 500 - 700	+ 400 - 600	+ 300 - 450	+ 500 - 700	+ 400 - 600	+ 350 - 450

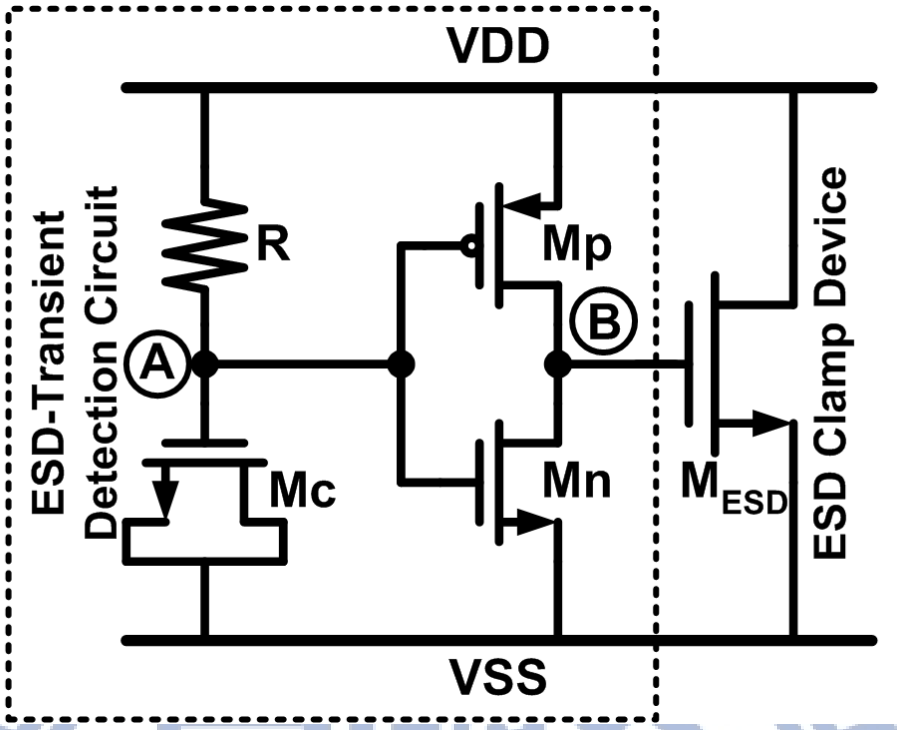


Fig. 4.1 Traditional *RC*-based power-rail ESD clamp circuit with ESD-transient detection circuit and ESD clamp nMOS transistor [8].

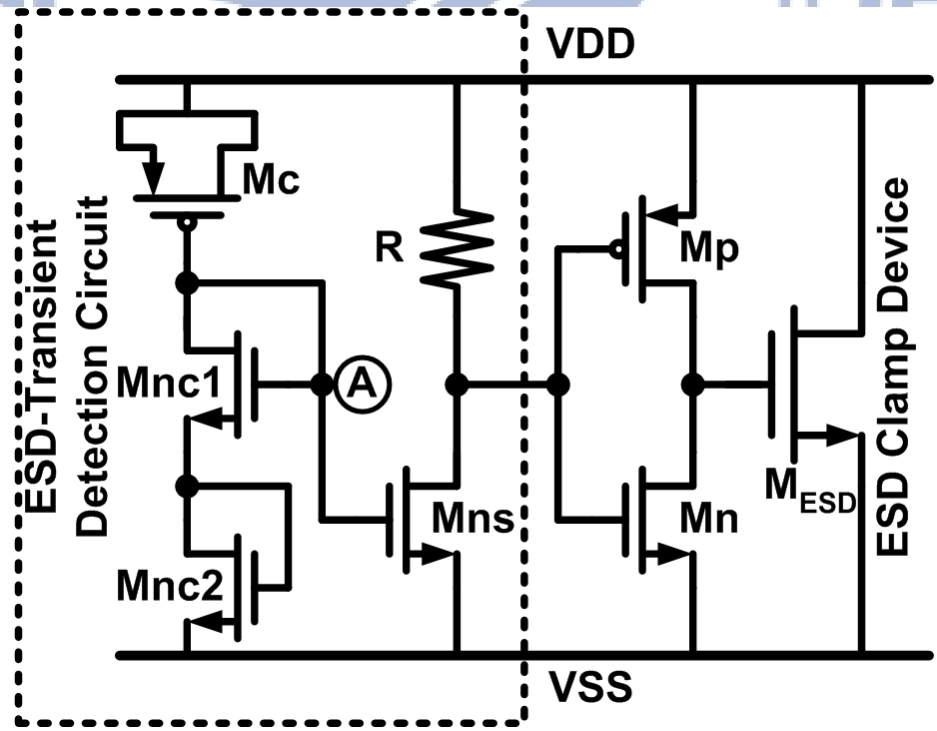
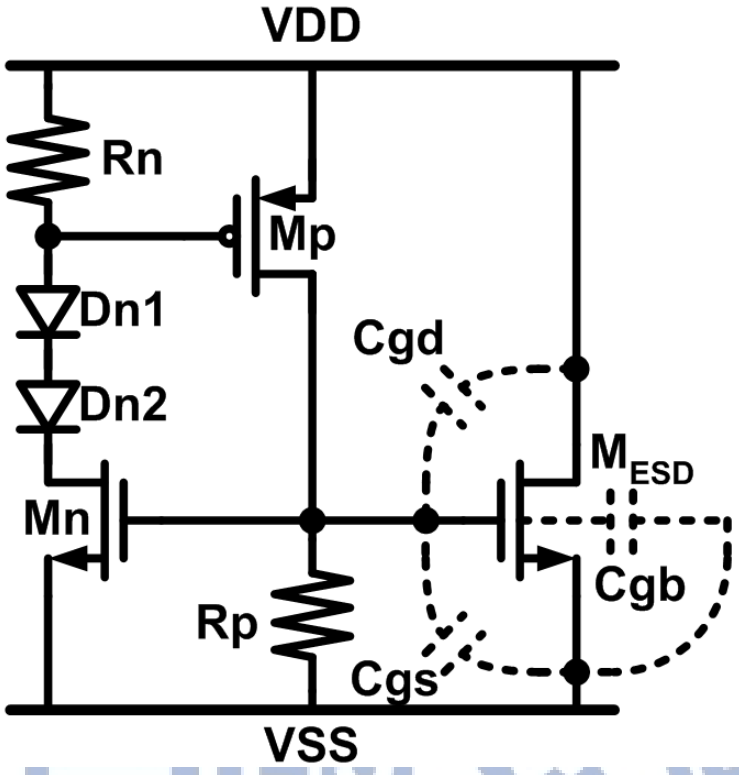
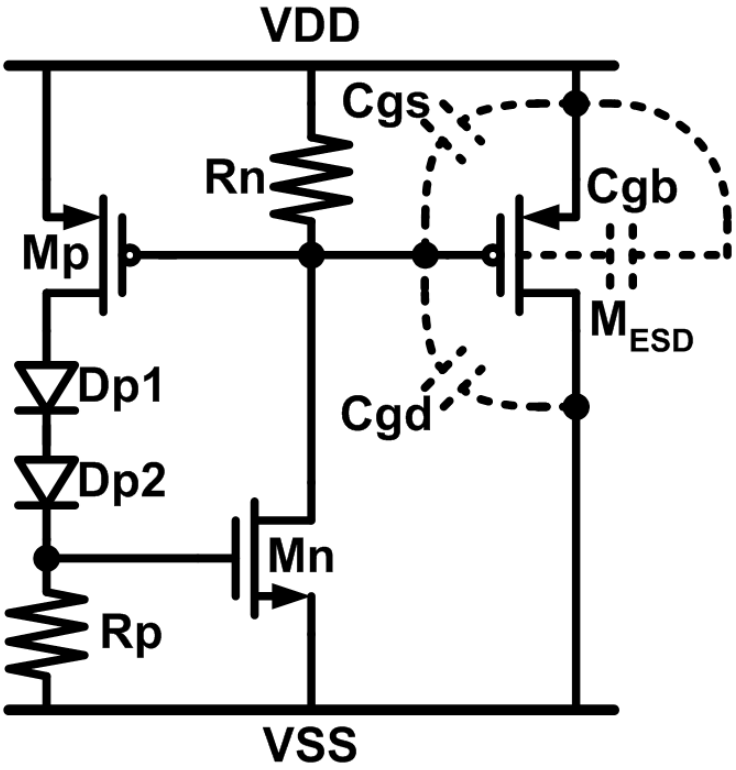


Fig. 4.2 Power-rail ESD clamp circuit with smaller capacitance in ESD-transient detection circuit [36].



(a)



(b)

Fig. 4.3 Capacitor-less power-rail ESD clamp circuit with (a) ESD clamp nMOS transistor [47] and (b) ESD clamp pMOS transistor [48].

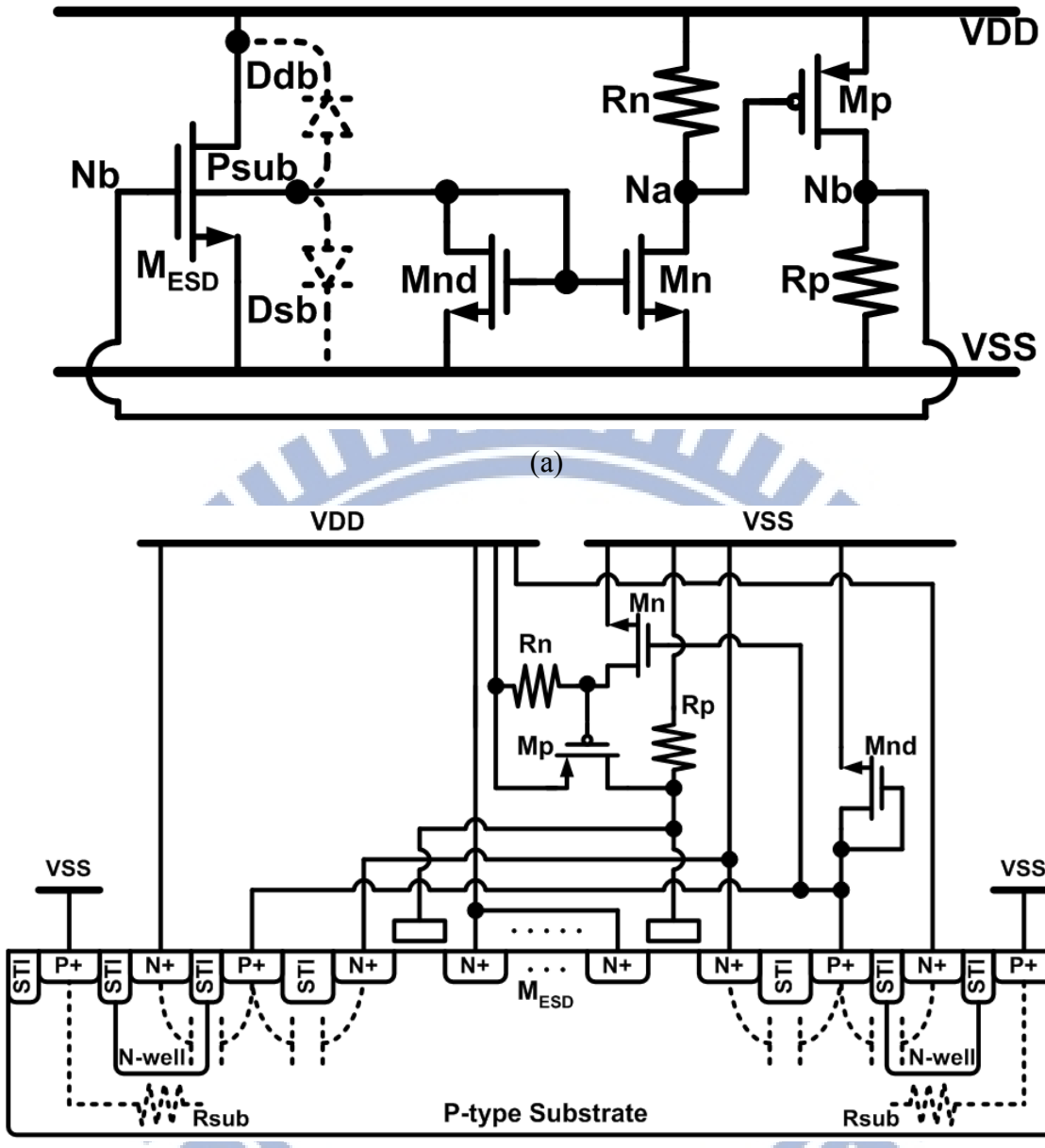


Fig. 4.4 The (a) circuit schematic and the (b) cross-sectional view of the new proposed power-rail ESD clamp circuit with ESD clamp nMOS transistor.

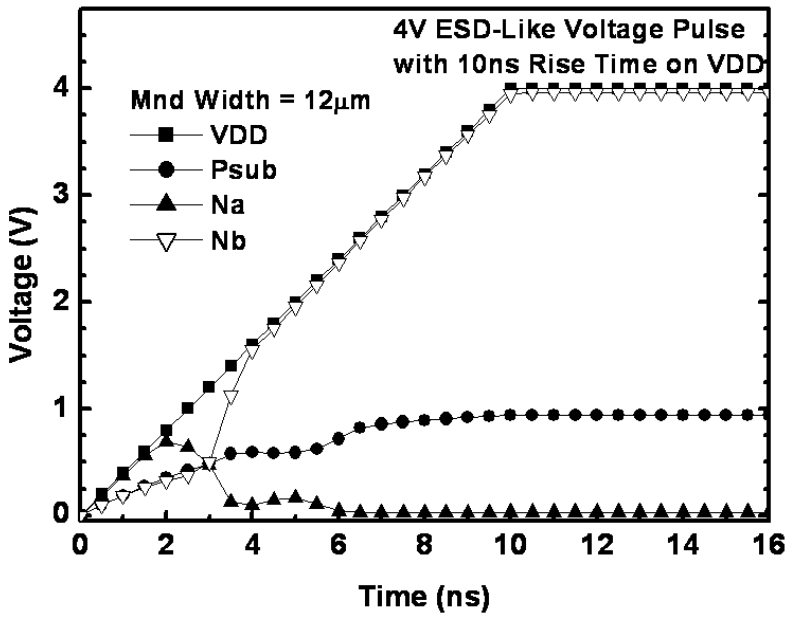


Fig. 4.5 Simulated voltage waveforms of the new proposed power-rail ESD clamp circuit with ESD clamp nMOS transistor under the ESD-like transition.

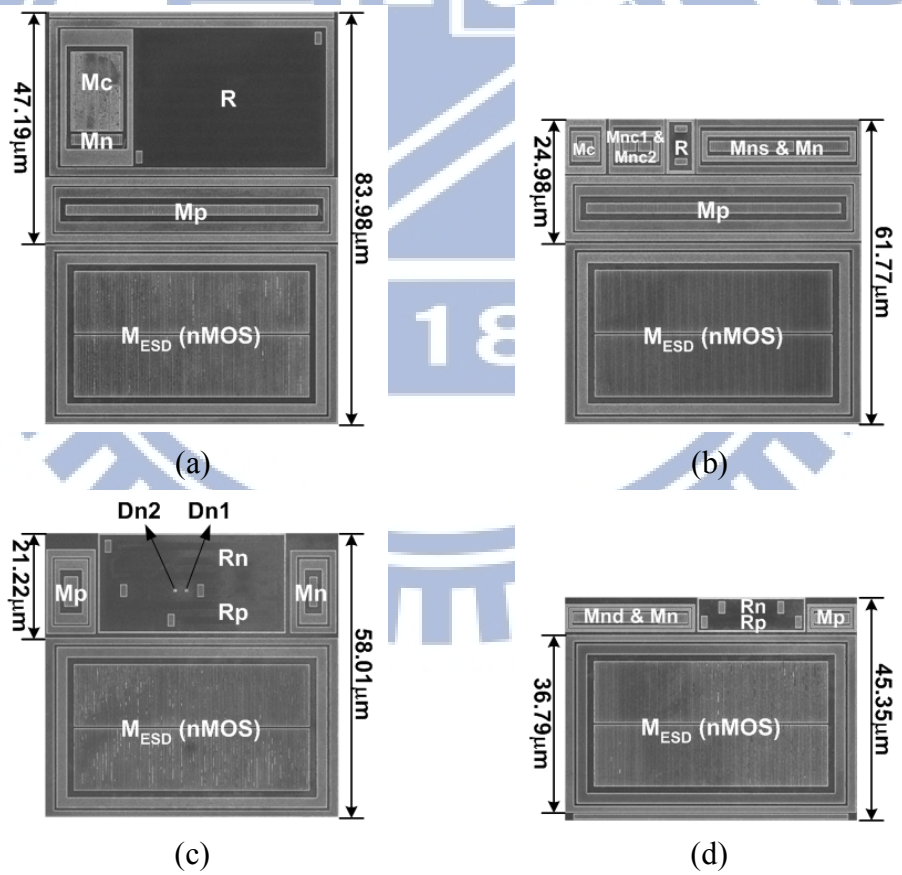


Fig. 4.6 Chip microphotograph of the (a) traditional *RC*-based, (b) smaller capacitance, (c) capacitor-less, and (d) new proposed power-rail ESD clamp circuits with ESD clamp nMOS transistor.

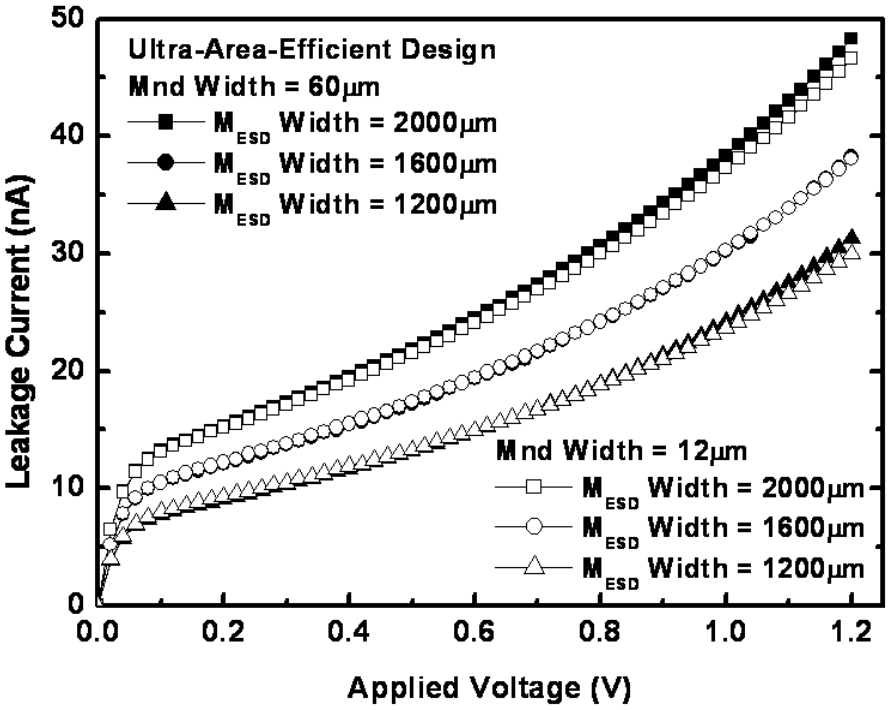
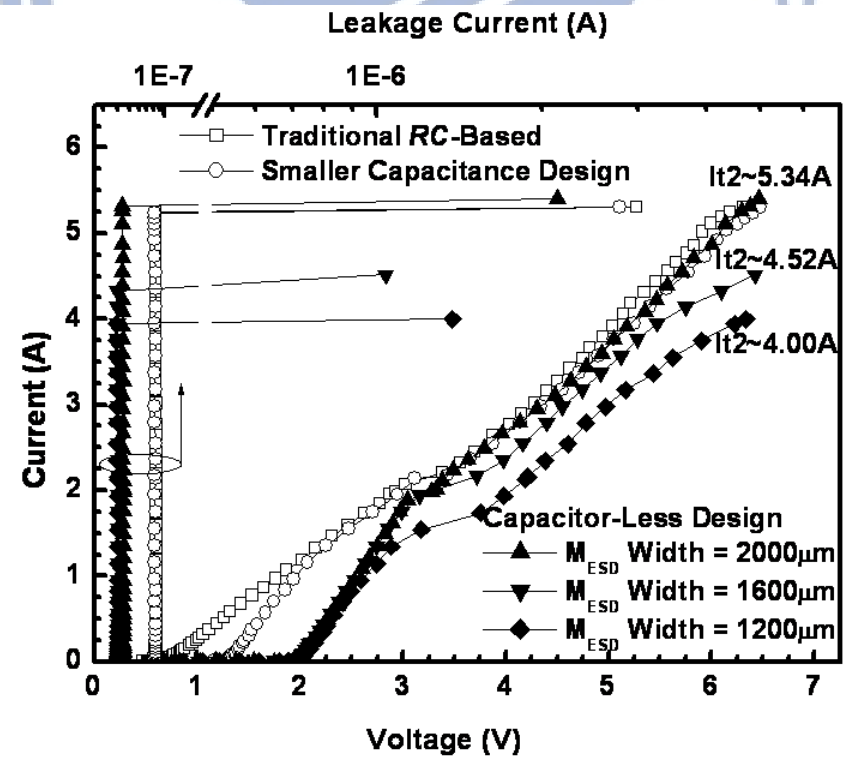
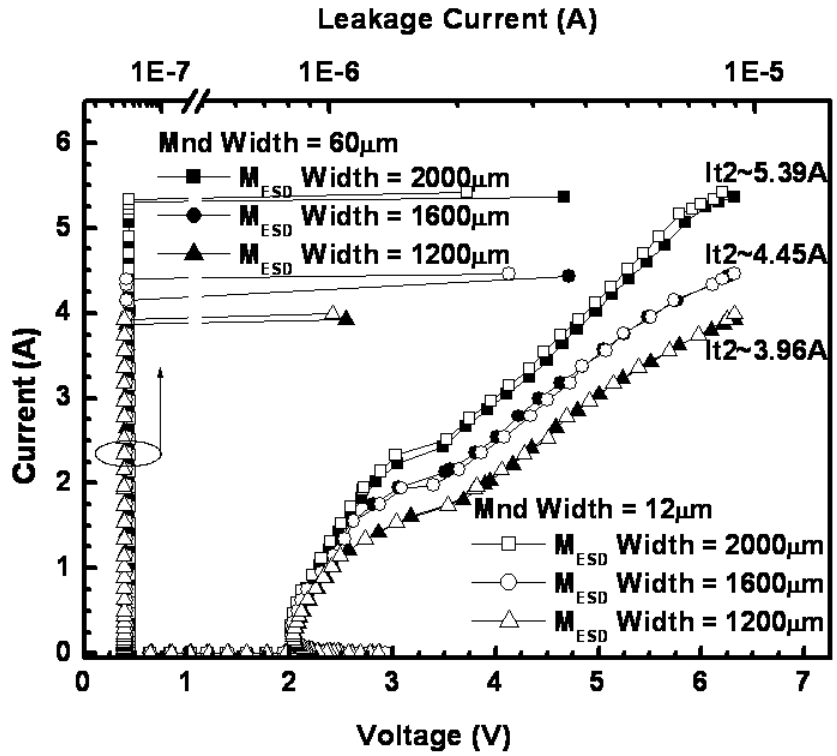


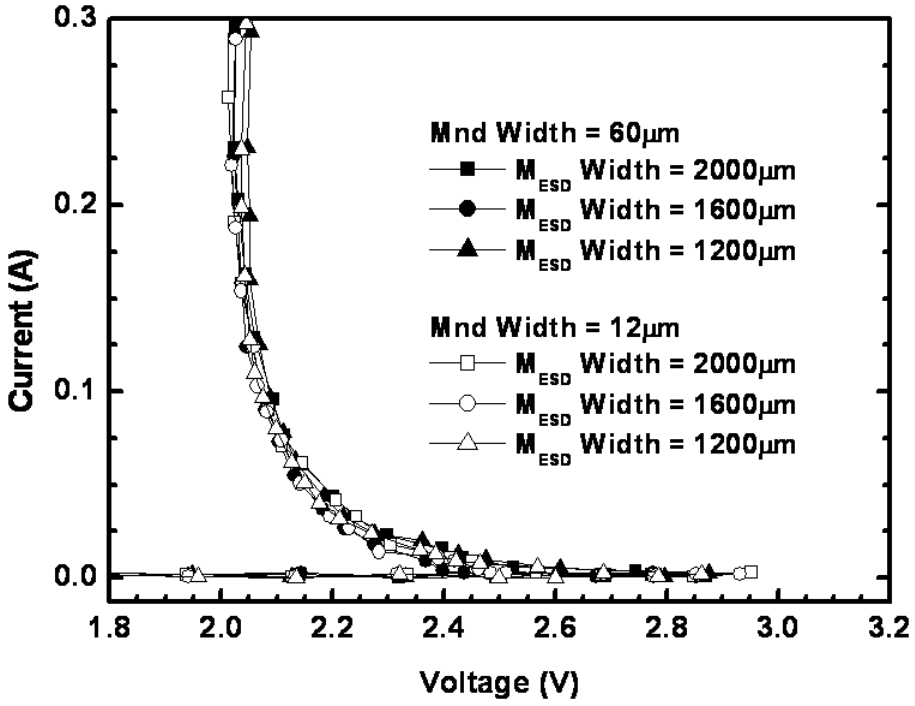
Fig. 4.7 The measured standby leakage currents of the new proposed power-rail ESD clamp circuits with ESD clamp nMOS transistor.



(a)

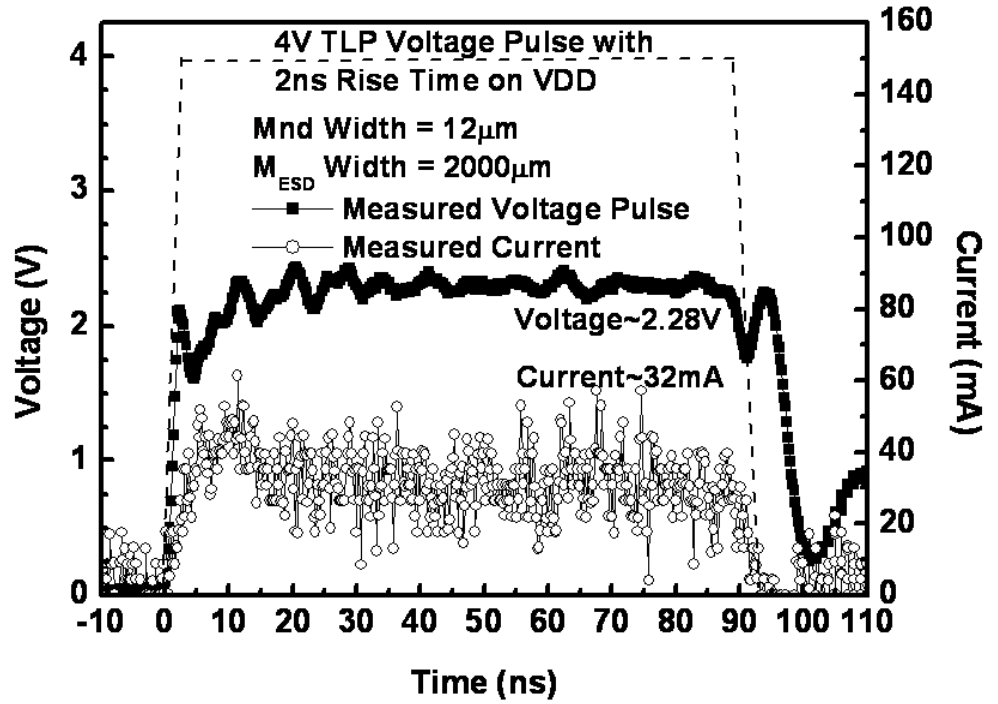


(b)

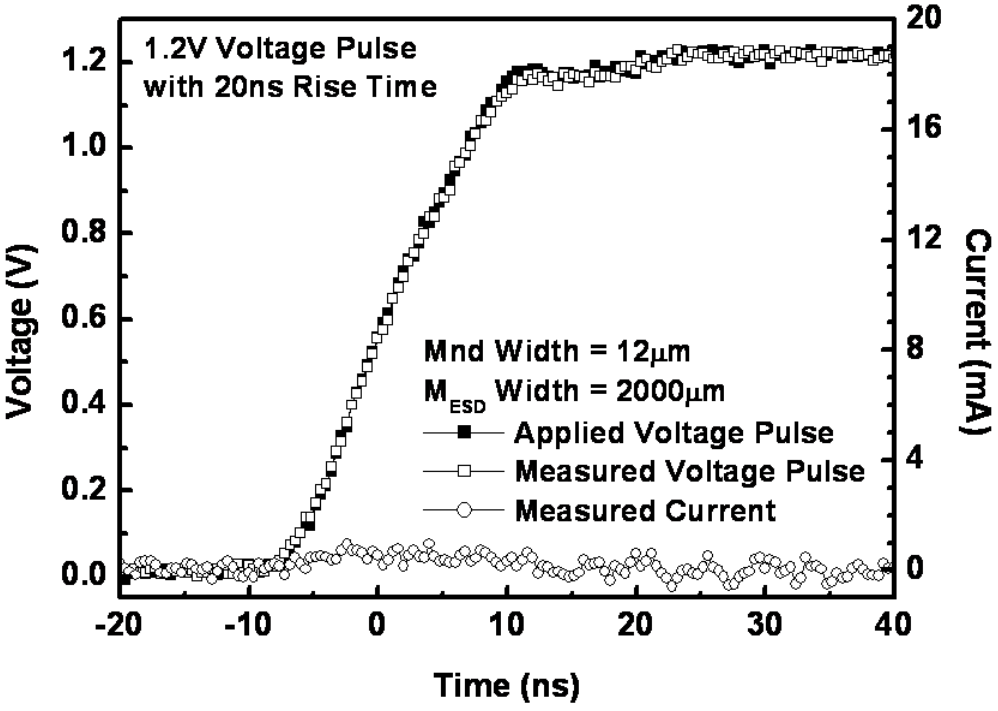


(c)

Fig. 4.8 Measured TLP *I-V* curves of the (a) prior arts, (b) new proposed design with ESD clamp nMOS transistor, and (c) the zoom-in illustration of (b).

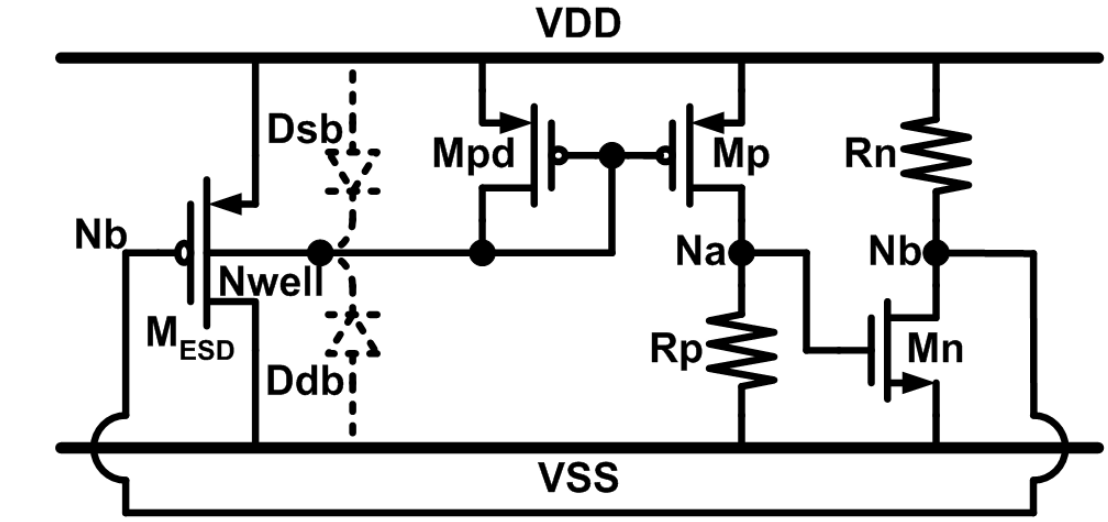


(a)

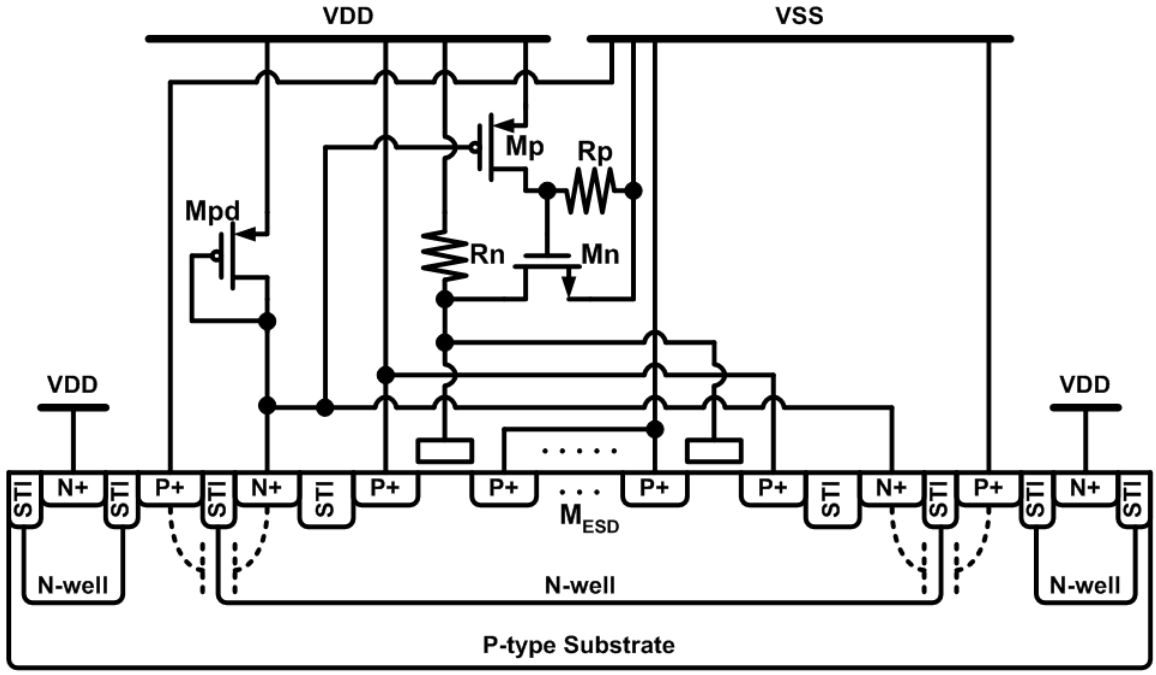


(b)

Fig. 4.9 The voltage waveforms under (a) TLP transition with 4V voltage pulse and (b) fast power-on transition.

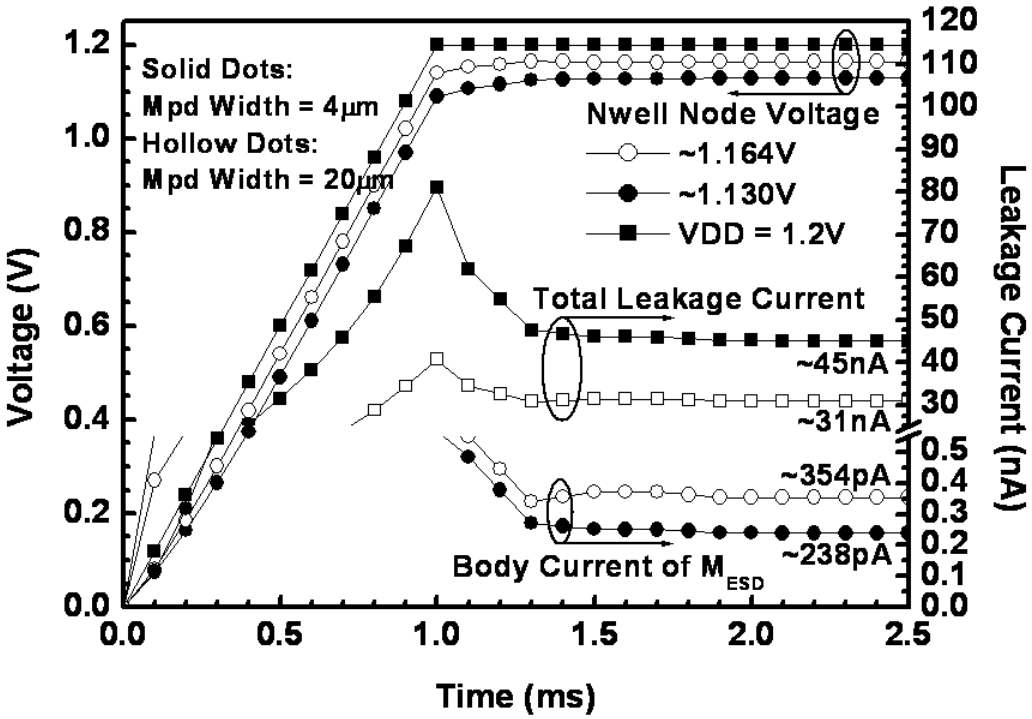


(a)

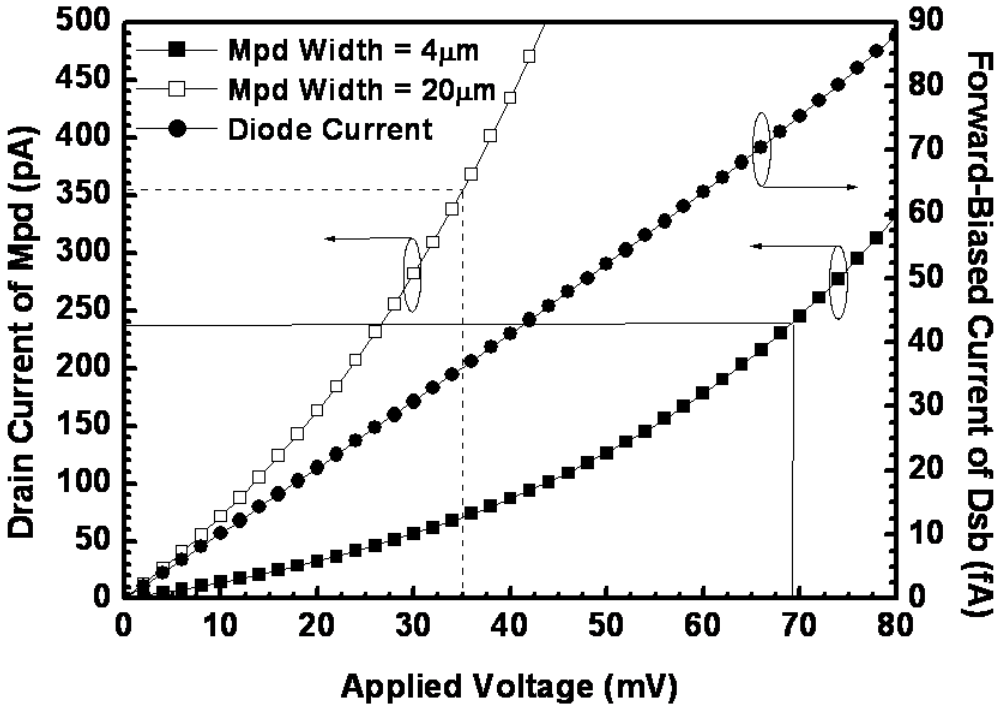


(b)

Fig. 4.10 The (a) circuit schematic and the (b) cross-sectional view of the new proposed ESD-transient detection circuit with ESD clamp pMOS transistor.



(a)



(b)

Fig. 4.11 Simulated voltage waveforms on the nodes and the leakage currents of the (a) proposed power-rail ESD clamp circuit with ESD clamp pMOS transistor under the normal power-on transition and (b) diode-connected transistor Mpd and forward-biased diode Dsb.

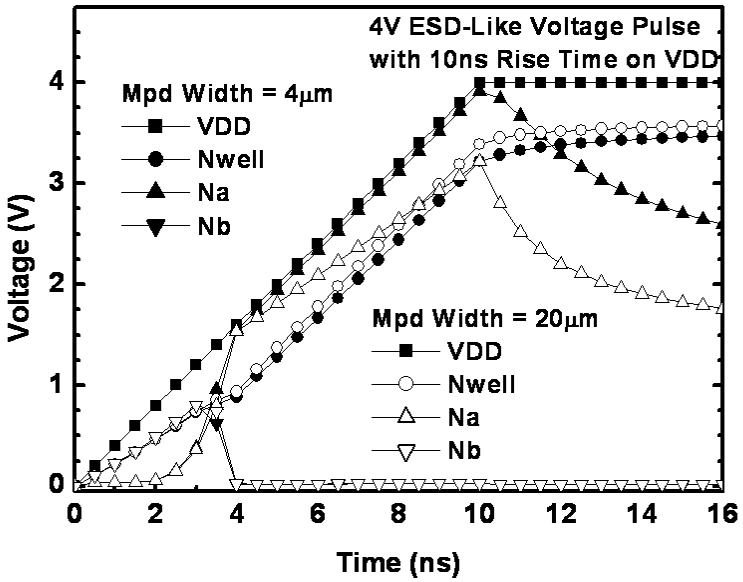


Fig. 4.12 Simulated voltage waveforms on the nodes of the new proposed power-rail ESD clamp circuit with ESD clamp pMOS transistor under the ESD-like transition.

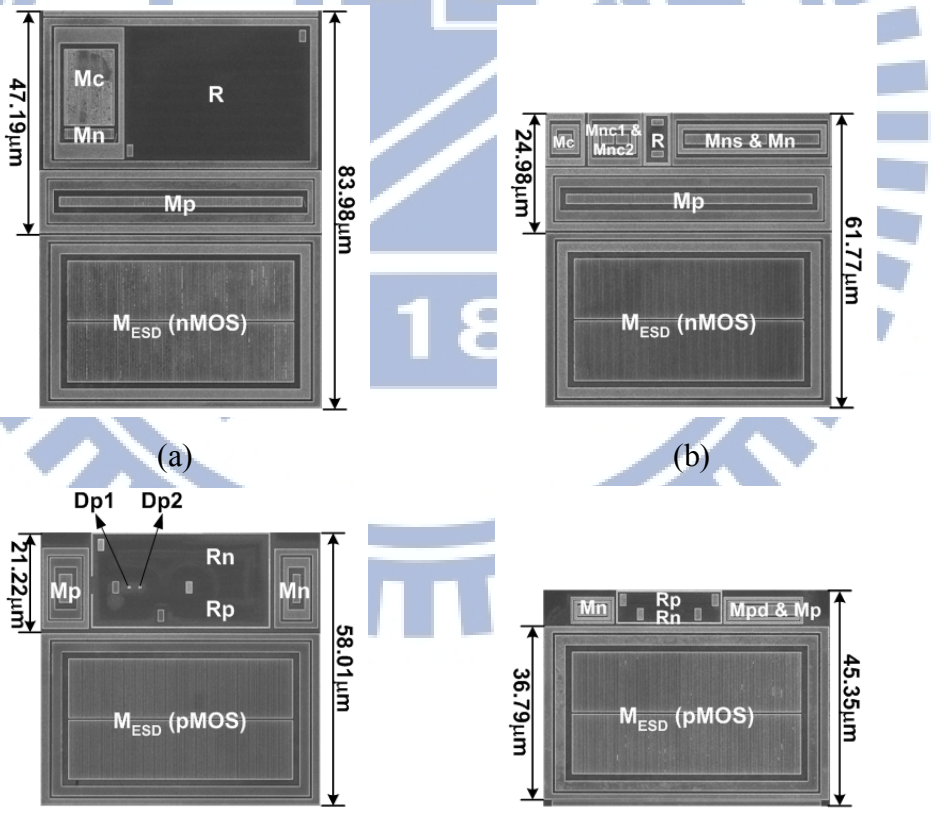
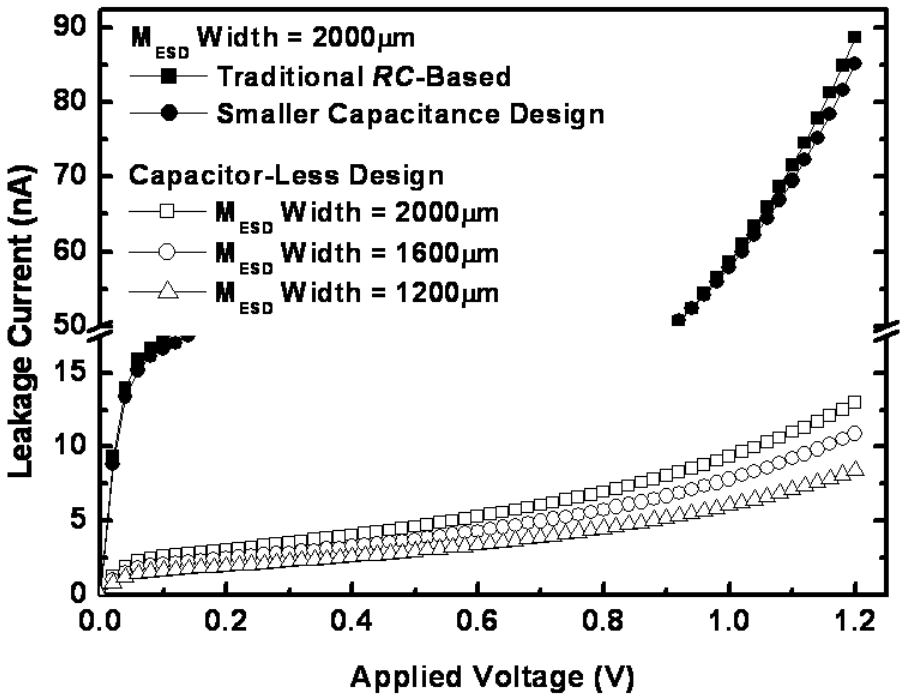
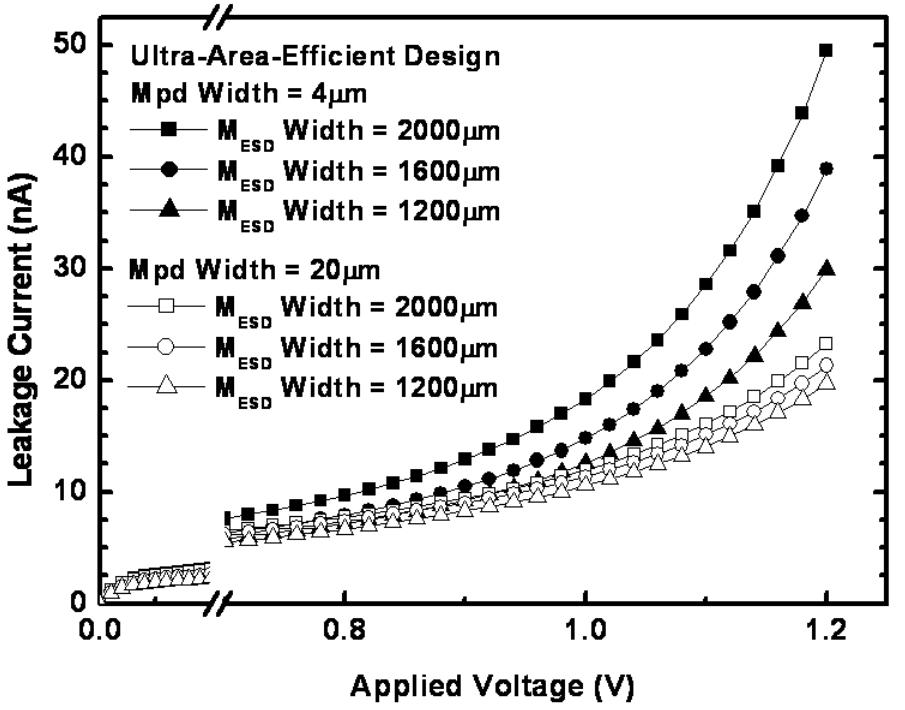


Fig. 4.13 Chip microphotograph of the fabricated power-rail ESD clamp circuits with the (a) traditional *RC*-based, (b) smaller capacitance, (c) capacitor-less, and (d) new proposed ultra-area-efficient ESD-transient detection circuits with ESD clamp pMOS transistor.



(a)



(b)

Fig. 4.14 The measured standby leakage currents of the fabricated power-rail ESD clamp circuits with (a) prior art designs and (b) new proposed design with ESD clamp pMOS transistor.

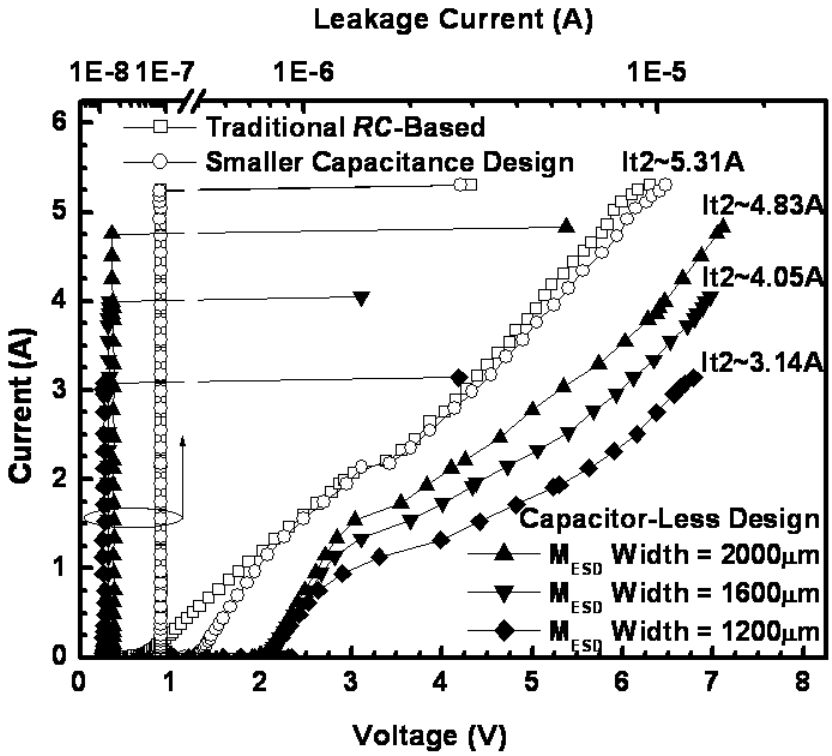
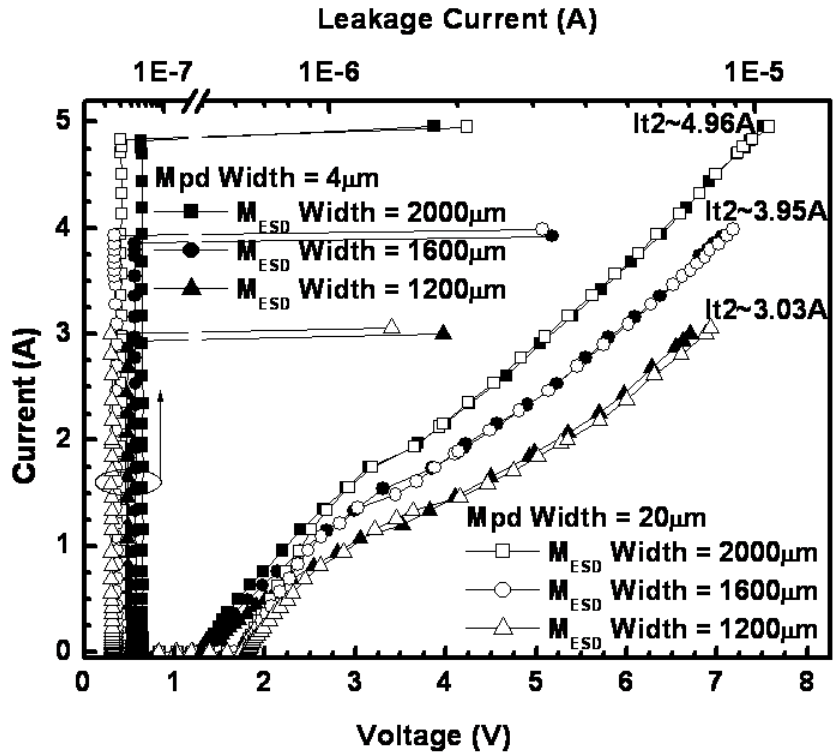
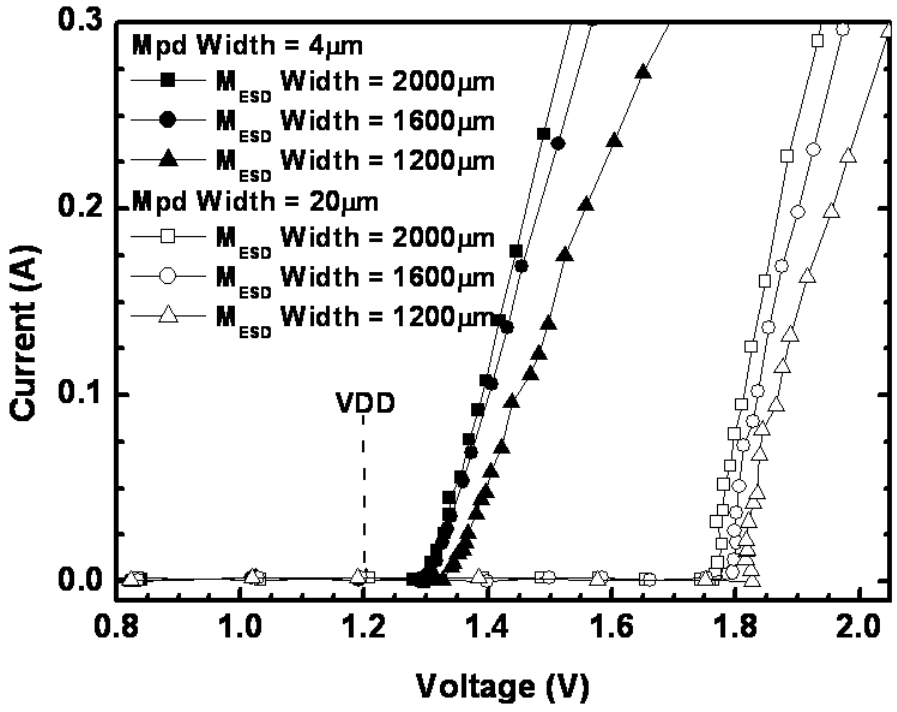


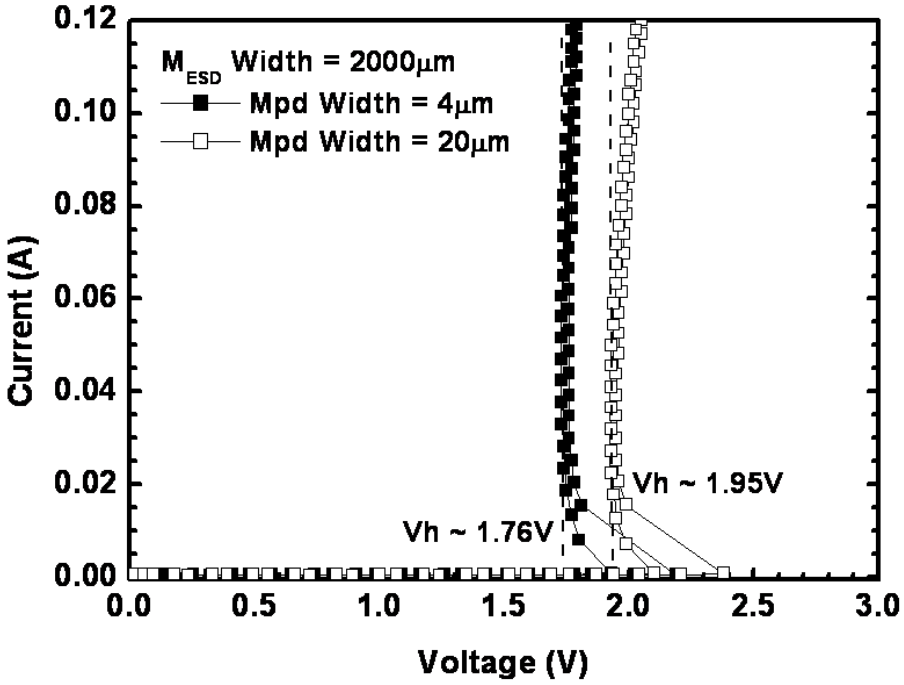
Fig. 4.15 TLP measured I-V curves of the power-rail ESD clamp circuits with the traditional *RC*-based and the smaller capacitance designs.


Leakage Current (A)
1E-7
1E-6
1E-5
It2~4.96A
It2~3.95A
It2~3.03A
Mpd Width = 4μm
M_ESD Width = 2000μm
M_ESD Width = 1600μm
M_ESD Width = 1200μm
Mpd Width = 20μm
M_ESD Width = 2000μm
M_ESD Width = 1600μm
M_ESD Width = 1200μm
Current (A)
Voltage (V)

(a)


Mpd Width = 4μm
M_ESD Width = 2000μm
M_ESD Width = 1600μm
M_ESD Width = 1200μm
Mpd Width = 20μm
M_ESD Width = 2000μm
M_ESD Width = 1600μm
M_ESD Width = 1200μm
VDD
Current (A)
Voltage (V)

(b)



(c)

Fig. 4.16 Measured *I-V* curves of the new proposed power-rail ESD clamp circuits under (a) the TLP measurement, (b) the zoom-in illustration of TLP *I-V* curves for observing the holding voltages, and (c) the DC *I-V* measurement by curve tracer.

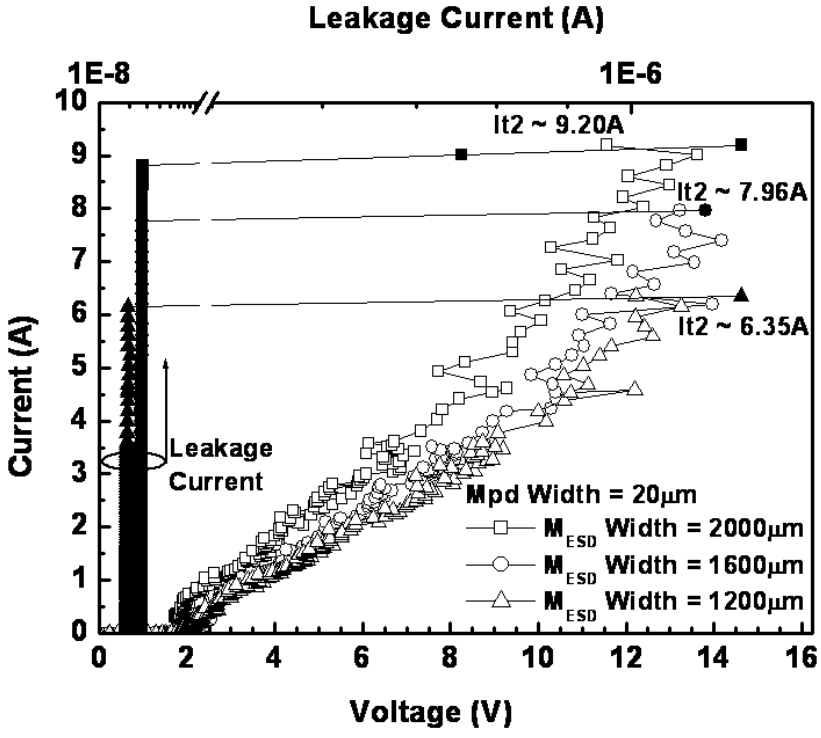
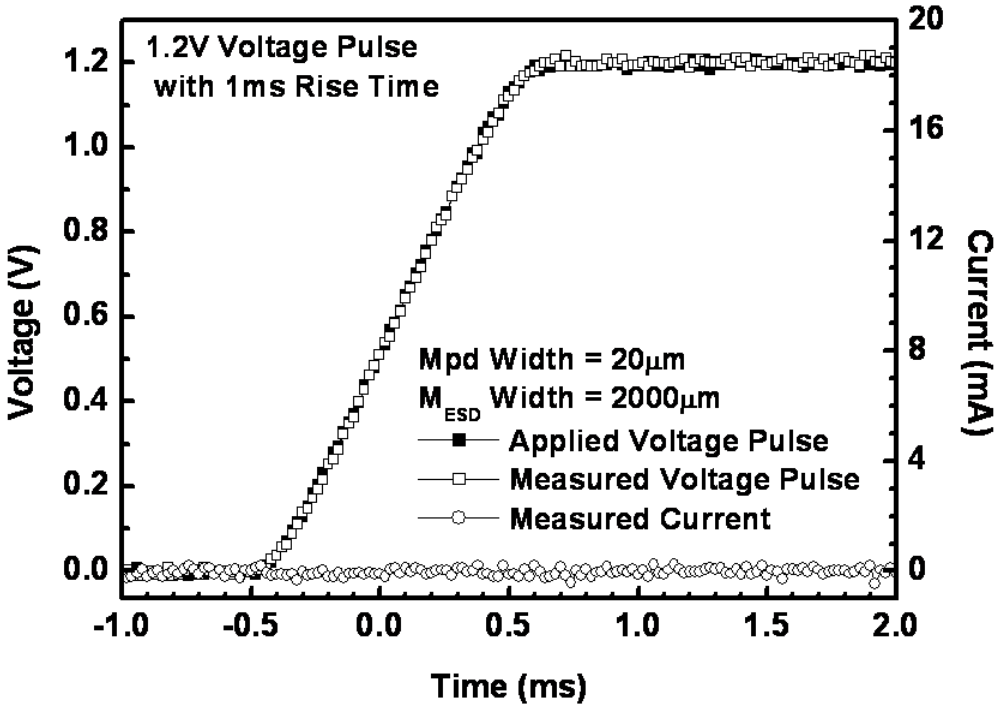
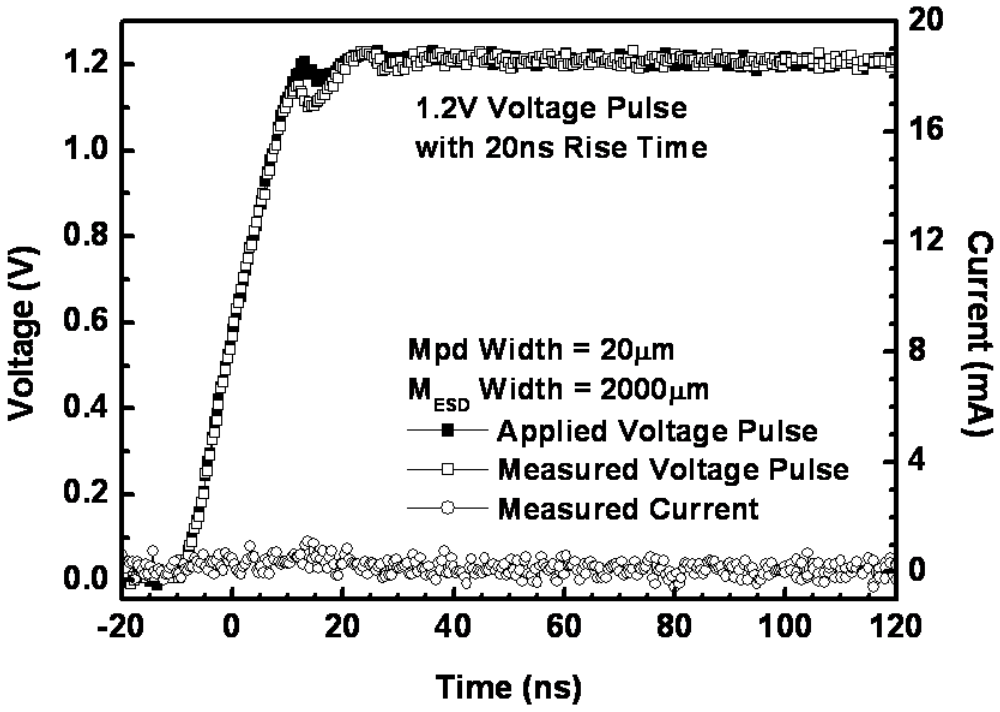


Fig. 4.17 VF-TLP measured *I-V* curves of the ultra-area-efficient power-rail ESD clamp circuits with Mpd width of 20μm under positive VDD-to-VSS ESD stress.

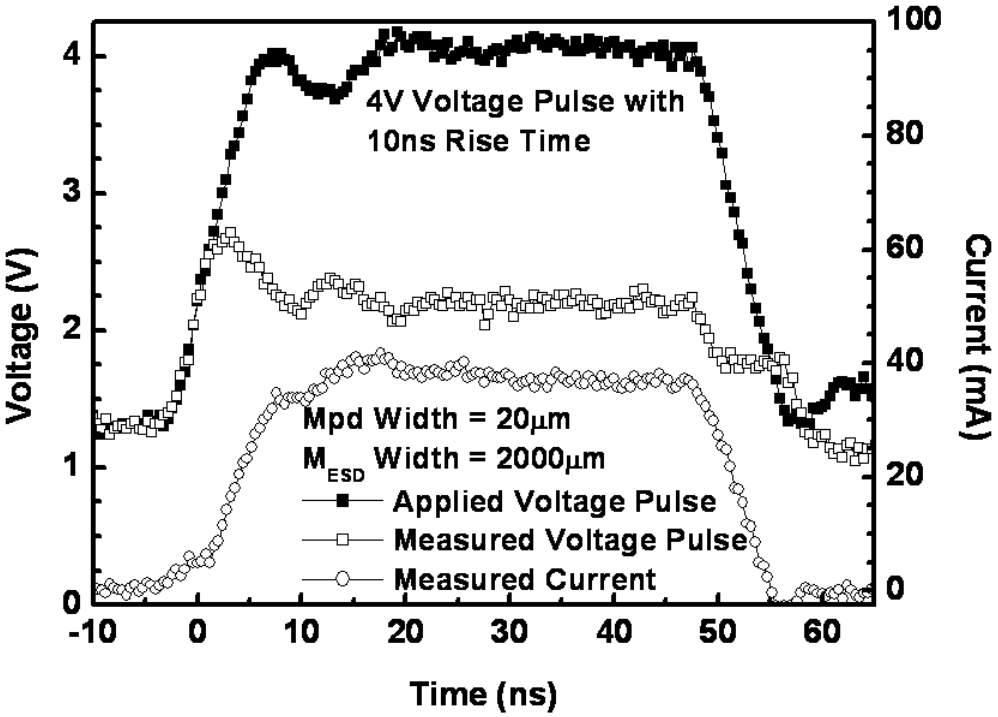


(a)

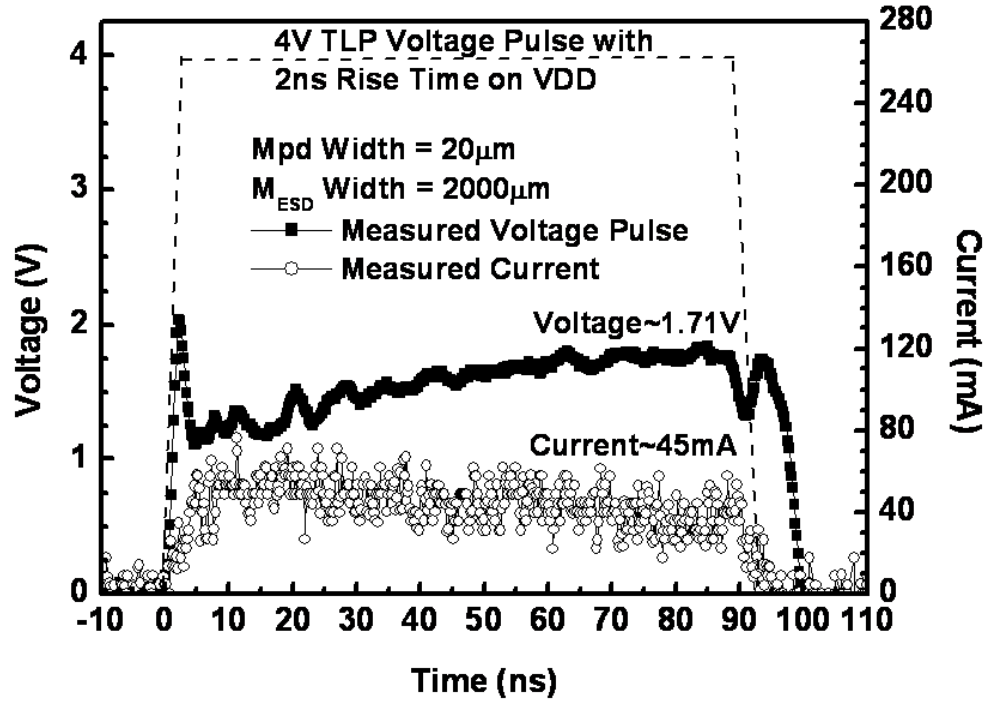


(b)

Fig. 4.18 The measured transient voltage and current waveforms of the ultra-area-efficient power-rail ESD clamp circuit under the 1.2V power-on transition with the rise time of (a) 1ms and (b) 20ns.



(a)



(b)

Fig. 4.19 Measured voltage and current waveforms of the new proposed power-rail ESD clamp circuit with ultra-area-efficient ESD-transient detection circuit under (a) transient noise condition and (b) TLP transition with 4V voltage pulse.

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Chapter 5

Power-Rail ESD Clamp Circuit with Considerations of Gate Leakage Current and Gate Oxide Reliability

In this chapter, the power-rail ESD clamp circuits with considerations of gate leakage current and gate oxide reliability are presented. First, the gate leakage current issue in conventional power-rail ESD clamp circuits is discussed in section 5.2. The power-rail ESD clamp circuit for 1×VDD applications is investigated in section 5.3, and high-voltage-tolerant power-rail ESD clamp circuit is discussed in section 5.4. All power-rail ESD clamp circuit were fabricated in a 65nm 1V fully silicided CMOS process.

5.1 Background

With the continuously scaled-down CMOS technology, the thickness of the gate oxide has been scaled down to only ~2nm. Such a thin gate oxide in nanometer CMOS technology would result in intolerable overall leakage current of the ICs due to the gate leakage current [53], [54]. Although the high-K/metal-gate materials can be used to reduce the equivalent oxide thickness (EOT) and the gate leakage current in nanoscale CMOS technology [55], [56], the 90nm, 65nm, and 45nm CMOS technologies still suffer the gate leakage issue because the high-K/metal-gate materials were not yet included into these processes supported by some foundries. Although the gate leakage can be reduced by directly using thick gate oxide devices, it has some limitations for the system-on-chip (SoC) with mixed-voltage I/O interfaces [57]. Without the thick gate oxide devices in low voltage process, the process steps can be reduced, the fabrication yield can be increased, and the chip cost can be lowered. Recently, some works were reported on how to reduce the gate leakage current by circuit technique for saving total power consumption in advanced CMOS technologies [58], [59].

The gate current of MOSFET is directly dependent on the poly-gate area and the gate oxide thickness, which has been modeled in BSIM4 MOSFET model [60]. Based on the corresponding SPICE parameters provided from foundry, the gate current flowing through an nMOS capacitor with W/L of 5μm/5μm under 1V bias is as large as 1.61μA (217nA) in 65nm

(90nm) CMOS technology. The simulated voltage-dependent gate leakage currents of the nMOS capacitors are shown in Fig. 5.1, where the gate leakage issue in 65nm CMOS technology is obviously worse than that in 90nm CMOS technology.

Recently, some designs of the low-leakage power-rail ESD clamp circuit in nanometer CMOS technologies were revealed [32], [61], [62]. In [32], the gate current was utilized to bias the ESD detection circuit and to reduce the voltage difference across the gates of the MOS capacitors. In [61], the *RC*-based ESD detection circuit and the feedback control inverter were used to avoid the direct leakage path through the MOS capacitor. In [62], the ESD detection circuit consisted of the *RC* timer, inverters, and feedback pMOS. The feedback pMOS could lower the voltage drop across the *RC* timer to reduce the gate-leakage current of the MOS capacitor.

In addition, the SoC has become popular because the number of transistors in a chip is aggressively increasing with the continuously progressed CMOS technology. The gate oxide thickness has been shrunk to improve circuit operating speed for such SoC applications. The power supply voltage has also been scaled down to reduce power consumption. For SoC integration, the I/O circuits with low-voltage devices may receive or drive high-voltage signals to communicate with other ICs in a microelectronic system. However, the nanoscale device with thinner gate oxide and shallower diffusion junction depth arises several serious problems when it is implemented in the I/O circuits with mixed-voltage interfaces [63]. These problems include the gate oxide reliability [64]-[66] and the undesirable leakage current paths [32], [61], [67]. Therefore, the chip-to-chip mixed-voltage I/O interfaces are required in the microelectronic systems with different power supply voltages [63], [68], [69].

In order to solve the gate oxide reliability issue without using the additional thick gate-oxide devices in the ESD protection circuit for the mixed-voltage I/O interfaces, the high-voltage-tolerant configurations had been widely used for mixed-voltage I/O circuits to reduce the process complexity and fabrication cost [70]-[73]. For [70] and [71], the substrate-triggered circuit, which is composed of the two pMOS devices, is controlled by the two *RC*-based detection circuits. In [72] and [73], the diode-connected pMOS are used as the voltage divider to bias the ESD detection circuit. However, those prior designs [70]-[73] did not consider the gate leakage current if such circuits were further implemented in nanometer CMOS processes. In nanometer CMOS technologies, the gate leakage current must be considered during circuit design. Therefore, some design strategies on high-voltage-tolerant power-rail ESD clamp circuit were also revealed to reduce the standby leakage current in

nanometer CMOS technologies [62], [74].

5.2 Gate Leakage Current in the Conventional Power-Rail ESD Clamp Circuits

5.2.1 Traditional RC-Based Power-Rail ESD Clamp Circuit

The traditional *RC*-based power-rail ESD clamp circuit with a large-sized ESD clamp device was traditionally used to protect the core circuits [8], as shown in the inset of Fig. 5.2. The simulated voltages on the nodes of the traditional *RC*-based power-rail ESD clamp circuit and the gate current of the MOS capacitor Mc are shown in Fig. 5.2, under the normal power-on condition with a rise time of 1ms in a 65nm 1V CMOS process. The dimensions of R, Mc, Mp, Mn, and M_{ESD} are 165.3kΩ, 64μm/2μm, 184μm/60nm, 36μm/60nm, and 2000μm/0.1μm, respectively. From the simulated results in Fig. 5.2, the gate current of Mc is 1.65μA when VDD is raised up to 1V. The voltage level on node A is about 0.72V due to the voltage drop across R. Therefore, a leakage current path is generated from VDD through the inverter (Mp and Mn) to VSS. Consequently, the main ESD clamp device M_{ESD} operating in the sub-threshold region will cause more leakage current under the normal circuit operating condition.

5.2.2 Capacitor-Less Design of Power-Rail ESD Clamp Circuit

Based on the concept of capacitor-less design [47], a SCR clamp with dual-base ESD detection driver was proposed to save area [75]. The SCR used as ESD clamp device can reduce leakage current. However, the gate leakage issue of the dual-base ESD detection driver in advanced nanoscale CMOS process should be further considered.

The capacitor-less design of power-rail ESD clamp circuit with a large-sized ESD clamp device was proposed to protect the core circuits [47], as shown in the inset of Fig. 5.3. The simulated voltages on the nodes of the capacitor-less design of power-rail ESD clamp circuit under the normal power-on condition with a rise time of 1ms in a 65nm 1V CMOS process are shown in Fig. 5.3. The gate and drain currents of M_{ESD} are also shown in Fig. 5.3. The dimensions of Rp, Rn, Mp, Mn, and M_{ESD} are 20kΩ, 40kΩ, 24μm/60nm, 12μm/60nm, and 2000μm/0.1μm, respectively. The P+ junction area of the diode Dn is 0.057μm^2. From the simulated results in Fig. 5.3, the gate current of M_{ESD} is 1.69μA when VDD is raised up to 1V. The voltage drop across Rp mainly induced by the gate current of M_{ESD} is about 55mV, which

is not enough to turn Mn on. Therefore, the ESD detection circuit can be almost turned off. However, there is still a leakage current path from VDD through the main ESD clamp device M_{ESD} to VSS. As shown in Fig. 5.3, the drain current of M_{ESD} is as large as 11.79μA and is the major source of the total standby leakage current.

The measured standby leakage currents of the traditional *RC*-based and the capacitor-less power-rail ESD clamp circuits in a 65nm 1V CMOS process at room temperature are shown in Fig. 5.4. The voltage of VDD power line is from 0V to 1V with the voltage step of 20mV. When VDD is 1V, the measured standby leakage currents of the *RC*-based and the capacitor-less power-rail ESD clamp circuits at room temperature are 760.42μA and 12.86μA, respectively. The standby leakage currents of the traditional *RC*-based and the capacitor-less power-rail ESD clamp circuit under different temperatures are also listed in Table 5.1. Based on the measured results in Fig. 5.4 and Table 5.1, MOS transistor, which is drawn with large device dimension as the ESD clamp device, is too leaky for the portable products requiring for low power consumption.

5.3 Power-Rail ESD Clamp Circuit for 1×VDD Applications

In this section, a new power-rail ESD clamp circuit with low standby leakage current and area efficiency is proposed and successfully verified in a 65nm 1V CMOS technology. By using the new proposed circuit solution, the standby leakage current of the proposed power-rail ESD clamp circuit can be significantly reduced to the order of nano-ampere under the normal circuit operating condition with 1V bias. In addition, an area-efficient SCR clamp device with embedded ESD-transient detection circuit is also proposed. The modification of layout structure not only saves the total layout area but improves the discharging efficiency for ESD current. At the same time, the standby leakage current of the proposed layout structure can be still in the order of nano-ampere under the normal circuit operating condition with 1V bias.

5.3.1 Design Concept of ESD-Transient Detection Circuit

The new proposed power-rail ESD clamp circuits of low standby leakage are shown in Figs. 5.5(a) and (b), respectively, with p-type and n-type triggered silicon-controlled rectifier (SCR) devices as the main ESD clamp devices. The SCR device [76] used as the main ESD clamp device can avoid the gate leakage current issue due to no poly-gate structure inside the SCR device. However, the SCR device has some disadvantages, such as the slow turn-on

speed and the high triggered voltage. Therefore, the ESD detection circuit is necessary to improve the turn-on speed of the SCR device under ESD stress condition. The new proposed ESD detection circuit is designed with considerations of the gate leakage current and the gate oxide reliability. By inserting the diode in the ESD detection circuit, the voltage differences across the gate oxide of the nMOS and pMOS transistors can be intentionally reduced. Therefore, the gate leakage current of the nMOS and pMOS transistors in the ESD detection circuit can be well controlled to minimize the total standby leakage current.

In the proposed ESD detection circuit of Fig. 5.5(a), the pMOS Mp is used to generate the trigger current into the trigger node (node C in Fig. 5.5(a)) of the p-type triggered SCR device during the ESD stress event. Under the normal circuit operating condition, the Mp is kept off and the trigger node is kept at VSS through the parasitic p-substrate resistor Rsub. Therefore, the p-type triggered SCR device is turned off during the normal circuit operating condition.

The *RC*-based ESD-transient detection mechanism is realized by the Rn and the junction capacitance of the reverse-biased diode Dc, which can distinguish the ESD stress event from the normal power-on condition. Compared to the thin gate oxide of MOS in the traditional *RC* circuit, the reverse-biased diode Dc used as capacitor to realize the *RC* time constant in the proposed ESD detection circuit can be free from the gate leakage current issue. The inserted diodes, Dn and Dp, in the ESD detection circuit are used to reduce the voltage differences across the gate oxide of the transistors Mp and Mn in the ESD-transient detection circuit. Therefore, the leakage current and gate oxide reliability of Mp and Mn can be safely relieved.

Similarly, the complementary type of the proposed ESD detection circuit is shown in Fig. 5.5(b) to trigger the n-type triggered SCR device. In Fig. 5.5(b), the Rp is used to keep the node C at VSS under the normal circuit operating condition. The additional diode Dt is used to block the connection between the Rn and the parasitic n-well resistor Rwell in the SCR device for not affecting the *RC* time constant at node A. In this complementary type of ESD detection circuit, the nMOS Mn is used to conduct the trigger current from the trigger node (the anode of Dt) of the n-type triggered SCR device under the ESD stress event.

The new proposed power-rail ESD clamp circuits have been fabricated in a 65nm 1V CMOS process. All devices in the proposed design are 1V fully-silicided devices, including the SCR device. For p-type and n-type triggered designs, the widths of SCR devices are split with 30, 40, and 50μm to verify the corresponding ESD robustness. The device dimension of Mp (Mn) in the ESD-transient detection circuit can be adjusted to provide different trigger currents for turning on the p-type (n-type) triggered SCR devices. Therefore, the gate widths

of Mp and Mn are split with 40, 60, 80μm to investigate the turn-on efficiency of the proposed power-rail ESD clamp circuit, as listed in Table 5.2.

5.3.2 Silicon-Controlled Rectifier (SCR) Embedded into ESD-Transient Detection Circuit

The cross-sectional view of the proposed area-efficient power-rail ESD clamp circuit with embedded ESD-transient detection circuit is shown in Fig. 5.6. The main concept of layout modification is to sufficiently utilize parasitic or existing elements in the ESD-transient detection circuit. By following this main concept, the layout area of new proposed design can be greatly saved due to no use of additional resistors and capacitors.

In Fig. 5.6, the source of Mp (Mn) in ESD-transient detection circuit is skillfully used as the anode (cathode) of one of the SCR path. The resistors (Rwell and Rsub) connected to the gate of Mp and Mn are implemented by parasitic resistor in N-well and P-substrate, respectively. The *RC*-based ESD-transient detection mechanism is realized by the Rwell and the reverse-biased diode Dc, which is implemented by the Nwell/P-substrate junction of the surrounding guardring. The inserted diodes, Dn and Dp, in ESD-transient detection circuit are intentionally placed between the P+ pickup regions and the cathodes of SCR paths. This arrangement can increase the parasitic resistance of Rsub and the holding voltage of SCR device can be reduced in response to increased value of Rsub. Additional N+ region connected to VDD is inserted to form a diode Dr to provide a forward-biased discharging path from VSS-to-VDD during the ESD stress event.

For comparison, the widths of SCR devices in the proposed power-rail ESD clamp circuit in Fig. 5.5(a) are designed with 25, 35, and 45μm to verify the corresponding ESD robustness. The width of Mp is kept at 35μm for single finger with the variance in finger number of 1, 2, and 4. The device dimensions of the other devices, including Rn, Dc, Dp, Dn, and Mn, are fixed as listed in Table 5.3.

For the power-rail ESD clamp circuit with embedded ESD-transient detection circuit in this work, the widths of SCR devices are also split with 25, 35, and 45μm. The width of Mp and Mn is varied in response to the width of SCR device due to embedded feature of layout structure. Therefore, the width of Mp and Mn would be 25, 35, and 45μm for single finger with the variance in finger number of 1, 2, and 4. For simplicity, the dimensions of Dp and Dn are also varied in response to the width of SCR device as listed in Table 5.3. The reverse-biased diode Dc is provided by the surrounding N+ guardring.

5.3.3 Operation Mechanism

5.3.3.1 Normal Power-On Transition

Under the normal circuit operating condition with VDD of 1V and grounded VSS, the gate voltage of Mp (node A in Fig. 5.5) is biased at 1V through the resistor Rn in the new proposed ESD detection circuit. The gate voltage of Mn (node C) is simultaneously biased at 0V through the parasitic p-substrate resistor Rsub (the resistor Rp) in the p-type (n-type) triggered design. Because Mp (Mn) is kept off, no trigger current is generated into (conducted from) the trigger node of the p-type (n-type) triggered SCR device. By inserting the diodes, Dp and Dn, in the ESD-transient detection circuit, the voltages at node B and node D can be clamped to the desired higher or lower voltage levels. Therefore, the drain-to-gate and drain-to-source voltages of Mp and Mn can be far less than 1V to further reduce the standby leakage current.

By using the SPICE parameters provided from foundry and the design dimensions listed in Table 5.2, the simulated voltage waveforms and the leakage current of the proposed ESD detection circuit during the normal power-on transition are shown in Fig. 5.7, where VDD is raising from 0V to 1V with a rise time of 1ms. From the simulation results in Fig. 5.7, the voltage differences across the gate-to-drain, gate-to-source, and drain-to-source terminals of all transistors in the proposed ESD-transient detection circuit are only about 0.5V. Because the Mp (Mn) with the device dimension of 40μm/0.12μm is used to trigger the p-type (n-type) triggered SCR device on during the ESD stress event and the pMOS Mp has smaller gate leakage current as comparing to that of nMOS Mn in the same 65nm 1V CMOS process, the simulated leakage current of the ESD-transient detection circuit is around 13.9nA (42.6nA) for the p-type (n-type) triggered design as shown in Fig. 5.7.

5.3.3.2 ESD Transition

When a positive fast-transient ESD-like voltage is applied to VDD with grounded VSS, the *RC* time delay keeps the node A at a relatively low voltage level as compared with that at VDD. Mp can be quickly turned on to generate the trigger current into the trigger node (node C) of the p-type triggered SCR device in Figs. 5.5(a) and 5.6. The turned-on Mp can also elevate the voltage level at the node C to further turn Mn on. When Mn is turned on, the trigger current can be conducted from the trigger node (node A) of the n-type triggered SCR device in Figs. 5.5(b) and 5.6.

To simulate the fast-transient edge of the HBM ESD event [1] before the breakdown on the internal devices to be protected, a 5V voltage pulse with a rise time of 10ns is applied to VDD.

The simulated transient voltage and the trigger current of the ESD detection circuit during such an ESD-like transition are illustrated in Fig. 5.8. According to the simulation results, Mp (Mn) can be successfully turned on to generate (conduct) the trigger current for the p-type (n-type) triggered design. Finally, the SCR device is fully turned on to discharge the ESD current from VDD to VSS.

5.3.4 Experimental Results

The proposed power-rail ESD clamp circuits have been fabricated in a 65nm fully silicided CMOS process by using only 1V devices. The microphotograph of the fabricated power-rail ESD clamp circuits with the SCR device of 40μm in width are shown in Fig. 5.9(a) for p-type triggered design and Fig. 5.9(b) for n-type one. The microphotograph of the embedded ESD-transient detection circuit design with the SCR device of 35μm in width is shown in Fig. 5.10(a), and the p-type triggered design discussed in Fig. 5.5(a) is shown in Fig. 5.10(b).

5.3.4.1 TLP Measurement and ESD Robustness

In order to investigate the protection performance of the power-rail ESD clamp circuit during the ESD stress events, the TLP generator [29] with a pulse width of 100ns and a rise time of ~2ns is used to measure the It2 of the fabricated power-rail ESD clamp circuits. The TLP measured *I-V* curves of the fabricated power-rail ESD clamp circuits with different SCR widths are shown in Fig. 5.11 for the p-type and n-type triggered designs at room temperature. The power-rail ESD clamp circuit with p-type (n-type) triggered SCR widths of 30, 40, and 50μm can achieve the It2 values of 2.07, 2.65, and 3.33A (2.08, 2.65, and 3.32A), respectively. The trigger voltage of the fabricated power-rail ESD clamp circuit with different Mp (Mn) widths is shown in Fig. 5.12. As shown in Fig. 5.12, the trigger voltage can be obviously reduced when the Mp (or Mn) width is increased. Therefore, the turn-on speed of the SCR device can be properly adjusted by the dimension of Mp or Mn to meet different application requirements. In addition, the holding voltages (Vh) of the p-type and n-type triggered designs are around ~2V. The fabricated power-rail ESD clamp circuits with Vh higher than VDD of 1V are free to latchup issue for 1V applications [51], [52].

The HBM and MM ESD levels of the fabricated power-rail ESD clamp circuit under positive VDD-to-VSS ESD stress are listed in Table 5.4. The HBM and MM ESD levels of the proposed power-rail ESD clamp circuits are also only related to the width of SCR device. The other TLP measured characteristics of fabricated power-rail ESD clamp circuit are also

listed in Table 5.4.

The TLP measured *I-V* curves of the power-rail ESD clamp circuits are shown in Fig. 5.13 for the p-type triggered design and in Fig. 5.14 for the embedded ESD-transient detection circuit. In these two figures, the It2 of embedded ESD-transient detection circuit is 1.63 times the value of p-type triggered design with given SCR width because the embedded ESD-transient detection circuit can provide two SCR discharging paths. For the Vh in the zoom-in illustration, it has been lowered from 1.92V to 1.46V due to larger Rsub and Rwell in the embedded ESD-transient detection circuit. ESD clamp circuit with lower Vh has better ESD protection capability and the Vh of embedded ESD-transient detection circuit is still higher than VDD of 1V to be free from latchup issue [52].

The HBM and MM ESD levels of the fabricated power-rail ESD clamp circuits with embedded ESD-transient detection circuit under positive VDD-to-VSS ESD stress are listed in Table 5.5. From the measured results, the HBM and MM ESD levels of the proposed embedded ESD-transient detection circuit are about 1.4~1.6 times the values of p-type triggered design with given SCR width.

The trigger voltages (Vt1) of the fabricated power-rail ESD clamp circuits with different SCR widths are shown in Fig. 5.15 and also listed Table 5.5. In Fig. 5.15, Vt1 can be obviously reduced when the finger number of Mp and Mn is increased to provide larger trigger current into SCR device. Overall, the turn-on speed of the SCR device can be properly adjusted by the dimension of Mp or Mn to meet different application requirements.

To avoid the latchup issue, the Vh of ESD protection circuit with SCR device must be designed greater than the maximum voltage level of VDD. The DC *I-V* curves of the proposed layout structures are measured (using Tek370 curve tracer) by applying a voltage sweep on the VDD pin. The dependence of Vh of the embedded ESD-transient detection circuit under different temperatures is illustrated in Fig. 5.16. In Fig. 5.16, the Vh slightly reduces when the temperature is increased because the current gain (β) of the parasitic bipolar transistor in the SCR device is increased with the increase of temperature. The Vh of the proposed layout structure at temperature of 100^{o}C is 1.31V, which is still greater than VDD of 1V. The measured results have verified that the proposed layout structure can be safely applied in 1V CMOS ICs without latchup issue.

5.3.4.2 Standby Leakage Current

The leakage current of the fabricated power-rail ESD clamp circuits are measured by

HP4155 from 0V to 1V with the voltage step of 20mV as shown in Fig. 5.17. In Fig. 5.17, the standby leakage currents of the power-rail ESD clamp circuits with SCR widths of 30, 40, and 50μm are similar, because the leakage current in the SCR device is quite small. When the device dimension of Mp (Mn) increases from 40μm/0.12μm to 80μm/0.12μm, the standby leakage current of the power-rail ESD clamp circuit with p-type (n-type) triggered SCR of 50μm increases from 16.4nA to 24.8nA (42.9nA to 84.3nA) at 25°C under 1V bias. The standby leakage currents of the fabricated power-rail ESD clamp circuits at room temperature are reduced to the order of nano-ampere only, because the gate oxide leakage is successfully relieved by inserting the diodes in the ESD-transient detection circuit. The n-type triggered design has largest standby leakage current because the nMOS Mn has larger gate leakage current as comparing to that of pMOS at the same device size in 65nm CMOS process. Increasing the device dimension of Mp (Mn) results in a larger standby leakage current under the normal circuit operating condition, but at the same time it can increase the trigger current to improve the turn-on speed of the triggered SCR device with a reduced trigger voltage (as shown in Fig. 5.12 and Table 5.4). The measured results of the standby leakage current at 1V normal operating voltage under different temperatures are also listed in Table 5.6.

The leakage currents of the fabricated power-rail ESD clamp circuits with embedded ESD-transient detection circuit are shown in Fig. 5.18. At 1V operating voltage, the leakage currents of the embedded ESD-transient detection circuits are slightly greater than those of p-type triggered designs under the room temperature because there are larger widths of Mn in embedded ESD-transient detection circuit. The nMOS transistor always contributes larger leakage current than that of pMOS transistor at the same device size. However, the leakage currents of proposed embedded ESD-transient detection circuits are still in the order of nano-ampere. The measured standby leakage currents at 1V operating voltage under different temperatures are listed in Table 5.7.

5.3.4.3 Turn-On Verification

In order to observe the turn-on behavior of the fabricated power-rail ESD clamp circuits, a TLP voltage pulse with a rise time of ~2ns and a pulse height of 20V is applied to the VDD power line with the grounded VSS. The TLP voltage pulse will start the ESD-transient detection circuit to generate the trigger current to trigger on the SCR device. The triggered-on SCR device can provide a low impedance path from VDD to VSS to discharge ESD current. When the TLP voltage pulse height of 20V is applied to VDD, the p-type (n-type) triggered

SCR can be fully turned on to be a low impedance path and the voltage across the clamp circuit is clamped to only 2.5V in Fig. 5.19(a) (2.2V in Fig. 5.19(b)). However, the power-rail ESD clamp circuit with embedded ESD-transient detection circuit can also be activated to clamp the voltage down to the lower level of 1.84V (2.08V) for SCR width in 45μm (25μm) due to two SCR discharging paths, as shown in Fig. 5.19(c).

Charged device model (CDM) is also an important ESD testing standard for ICs. In order to investigate the turn-on behavior of the proposed designs under CDM-like fast transient condition, the very fast TLP (VF-TLP) with a pulse width of 10ns and a rise time of 200ps is used to measure the fabricated power-rail ESD clamp circuits. The VF-TLP measured *I-V* curves of the power-rail ESD clamp circuits with different SCR widths are shown in Fig. 5.20 for the n-type triggered SCR, where the device dimension of Mn is kept at 80μm/0.12μm. In Fig. 5.20, the power-rail ESD clamp circuit with n-type triggered SCR widths of 50μm can achieve the It2 value of 5.73A (3.33A) for VF-TLP (TLP) measurement. It can be observed that the SCR device with larger device width has smaller turn-on resistance to effectively discharge ESD current.

5.4 High-Voltage-Tolerant Power-Rail ESD Clamp Circuit

In this section, a new low-leakage 2×VDD-tolerant power-rail ESD clamp circuit realized with only thin gate oxide devices for mixed-voltage I/O applications is proposed and verified in a 65nm 1V CMOS technology. The proposed design implements the ESD detection circuit with the feature of low leakage current and the consideration of 2×VDD voltage tolerance for mixed-voltage I/O applications. According to the experimental results, the standby leakage current of the proposed 2×VDD-tolerant power-rail ESD clamp circuit has been significantly reduced to the order of nano-ampere under the normal circuit operating condition.

5.4.1 Design Concept of ESD-Transient Detection Circuit

In order to receive the input signals with 2×VDD voltage level, the traditional ESD protection design with direct diode connection from the I/O pad to the power line of 1×VDD is inappropriate. The ESD protection scheme with ESD bus and high-voltage-tolerant ESD clamp circuit for the IC with mixed-voltage I/O interfaces has been reported [71]. The ESD protection scheme for high-voltage-tolerant mixed-voltage I/O buffer is shown in Fig. 5.21, which is realized with the ESD diodes, ESD bus, 1×VDD ESD clamp circuit, and the high-voltage-tolerant ESD clamp circuit.

As a positive ESD stress zapping at the I/O pad with grounded VSS, the ESD current can be discharged through diode Dp to the ESD bus and then through the high-voltage-tolerant ESD clamp circuit to VSS. When a positive ESD stress zapping at the I/O pad with grounded VDD, the ESD current can be discharged through diode Dp, ESD bus, high-voltage-tolerant ESD clamp circuit, VSS line, and the 1×VDD ESD clamp circuit. When a negative ESD stress zapping at the I/O pad with grounded VSS, the ESD current can be discharged through the diode Dn in forward-biased condition. When a negative ESD stress zapping at the I/O pad with grounded VDD, the ESD current can be discharged through the diode Dn to the VSS line and then through the 1×VDD ESD clamp circuit to VDD. Therefore, the four modes of ESD test at the I/O pad with the relatively grounded VDD or VSS in the mixed-voltage I/O buffer can be well protected by this ESD protection scheme.

The proposed 2×VDD-tolerant power-rail ESD clamp circuits with p-type and n-type substrate-triggered SCR devices [76] as the main ESD clamp devices are shown in Figs. 5.22(a) and (b), respectively. The cross-sectional views of p-type and n-type substrate-triggered SCR devices are illustrated in Figs. 5.23(a) and (b), respectively. The SCR device without the poly-gate structure has very small leakage current. The ESD-transient detection circuit is necessary to improve the turn-on speed of the substrate-triggered SCR device under ESD stress condition. Therefore, the proposed ESD detection circuit with only thin gate oxide 1V devices for 2×VDD-tolerant applications has to be designed with considerations of gate current and gate oxide reliability. The main design concept on the ESD-transient detection circuit is to reduce the voltage drop across the gate oxide. By following this main design concept, the gate leakage currents of the nMOS and pMOS in the ESD-transient detection circuit can be well controlled to minimize the total standby leakage current.

In the proposed ESD-transient detection circuit of Fig. 5.22(a), the pMOS Mp is used to generate the substrate-triggered current into the trigger node (node C in Fig. 5.22(a)) of the SCR device during the ESD stress event. Under the normal circuit operating condition, the Mp is kept off and the trigger node is kept at VSS through the parasitic p-substrate resistor Rsub. Therefore, the p-type substrate-triggered SCR device is turned off during the normal circuit operating condition. The *RC*-based ESD-transient detection mechanism is realized by the Rn and the capacitance of the reverse-biased diode Dc, which can distinguish the ESD stress event from the normal power-on condition. Using the reverse-biased diode Dc as capacitor to realize the *RC* time constant in the ESD-transient detection circuit can

significantly reduce the gate leakage current through the thin gate oxide of MOS in the traditional *RC* circuit. The cascode diode D_{SCR} is used to increase the total holding voltage of the ESD clamp device to avoid the transient-induced latchup issue. Other diodes, Dn1, Dn2, Dp1, and Dp2, are used to reduce the voltage drop across the gate oxide of the devices in the ESD-transient detection circuit. Therefore, the leakage currents of Mp (Mn) from source terminal to gate and drain terminals (from drain terminal to gate and source terminals) can be reduced.

Similarly, the reverse type of the proposed ESD detection circuit is shown in Fig. 5.22(b) to trigger the n-type substrate-triggered SCR device. In Fig. 5.22(b), the Rp is used to keep the node C at VSS under the normal circuit operating condition. The additional diode Dt is used to block the connection between the Rn and the parasitic n-well resistor Rwell in the SCR device for not affecting the *RC* time constant at node A. In this reverse-type ESD detection circuit, the nMOS Mn is used to conduct the triggered current from the trigger node (the anode of Dt) of the n-type substrate-triggered SCR device under the ESD stress event.

5.4.2 Operation Principles

5.4.2.1 Normal Power-On Transition

During the normal circuit operating condition with VDD_H of 1.8V and grounded VSS, the gate voltage of Mp (node A) is biased at 1.8V through the resistor Rn in the new proposed ESD-transient detection circuit. The gate voltage of Mn (node C) is simultaneously biased at 0V through the p-substrate resistor Rsub (the resistor Rp) in the new proposed ESD-transient detection circuit with p-type (n-type) substrate-triggered SCR device. Because Mp (Mn) is turned off, no trigger current is generated into (conducted from) the trigger node of the p-type (n-type) substrate-triggered SCR device. By inserting the diode strings into the ESD-transient detection circuit, the voltages at node B and node D can be clamped to some desired levels. Therefore, the drain-to-gate and drain-to-source voltages of Mp and Mn can be less than 1V to effectively reduce the standby leakage current. With such a bias design, all 1V devices in the proposed ESD-transient detection circuit are free from the gate oxide reliability issue under the normal circuit operating condition.

By using the SPICE parameters provided from foundry and the device dimensions listed in Table 5.8, the simulated voltage waveforms of the proposed ESD-transient detection circuit during the normal power-on transition are shown in Fig. 5.24. VDD_H is powered on from 0V to 1.8V with a rise time of 1ms. From the simulation results in Figs. 5.24(a) and (b), the

voltage drops across the gate-to-drain, gate-to-source, and drain-to-source terminals of all devices in the proposed ESD-transient detection circuit do not exceed the 1×VDD 1V range. Therefore, the proposed ESD-transient detection circuit is verified without suffering the gate oxide reliability issue under the normal circuit operating condition.

5.4.2.2 ESD Transition

When a positive ESD-like transient voltage is applied to VDD_H with grounded VSS, the *RC* time delay keeps the node A at a relatively low voltage level as compared with that at VDD_H. Mp can be quickly turned on to generate the trigger current into the trigger node (node C) of the p-type substrate-triggered SCR device in Fig. 5.22(a). For the n-type substrate-triggered SCR device in Fig. 5.22(b), the turned-on Mp can elevate the voltage level at the node C to further turn Mn on. When Mn is turned on, the trigger current is conducted from the trigger node (the anode of Dt) of the n-type substrate-triggered SCR device.

In order to simulate the transient edge of the HBM ESD event [1] before the breakdown on the ESD protection devices, a 5V voltage pulse with a rise time of 10ns is applied to VDD_H. The simulated transient voltage and the trigger current of the ESD detection circuit during the ESD transition are illustrated in Fig. 5.25. According to the simulation results, Mp (Mn) can be successfully turned on to generate (conduct) the trigger current for the p-type (n-type) substrate-triggered SCR device. Finally, the SCR device can be turned on to discharge the ESD current from VDD_H to VSS.

5.4.3 Experimental Results

The new proposed 2×VDD-tolerant power-rail ESD clamp circuits have been fabricated in a 65nm fully silicided CMOS process by using only 1V devices, as shown in Fig. 5.26. The widths of SCR devices in the power-rail ESD clamp circuit are split with 30, 40, and 50μm to verify the corresponding ESD robustness. In order to keep the same cross-section area of the ESD discharging path to avoid the ESD failure location occurring at D_{SCR}, the junction widths of the cascode diode D_{SCR} are also split with 30, 40, and 50μm at the same time.

5.4.3.1 Standby Leakage Current

The DC *I-V* characteristics of the fabricated 2×VDD-tolerant power-rail ESD clamp circuits are measured by HP4155 from 0V to 1.8V with the voltage step of 10mV, as shown in Fig. 5.27. At 1.8V normal operating voltage, the leakage currents of the proposed

2×VDD-tolerant power-rail ESD clamp circuits with p-type (n-type) substrate-triggered SCR devices are 32.7, 33.1, and 34.1nA (100.6, 101.4, and 103.7nA) for the SCR widths of 30, 40, and 50μm, respectively, at the room temperature. The proposed ESD-transient detection circuit for n-type substrate-triggered SCR device has larger leakage current due to the intrinsic characteristics of nMOS Mn with larger gate leakage current as comparing to pMOS. Based on the measured results in Fig. 5.27, the SCR devices obviously contribute very small part to the total leakage current. In addition, the leakage current of the ESD-transient detection circuit is reduced to the order of nano-ampere because the gate oxide leakage has been successfully eased by inserting the diode strings. The measured results of leakage current at 1.8V normal operating voltage under different temperatures are listed in Table 5.9.

5.4.3.2 TLP Measurement and ESD Robustness

The TLP measured results of the fabricated 2×VDD-tolerant power-rail ESD clamp circuits with SCR devices of different widths are shown in Fig. 5.28(a) for the p-type substrate-triggered SCR and in Fig. 5.28(b) for the n-type substrate-triggered SCR. The ESD clamp circuit with p-type (n-type) substrate-triggered SCR width of 40μm can achieve the It2 value of 2.68A (2.75A). In Fig. 5.28, the TLP-measured *I-V* curves have no snapback phenomenon and start to rise up after 2.1V. Because the voltage level of VDD_H under the normal circuit operating condition is 1.8V, the proposed 2×VDD-tolerant power-rail ESD clamp circuit can be free from the latchup issue.

The It2, HBM ESD levels, and MM ESD levels of the fabricated 2×VDD-tolerant power-rail ESD clamp circuits are listed in Table 5.10. The HBM (MM) ESD levels of the p-type substrate-triggered SCR with widths of 30, 40, 50μm are 3.5, 5.0, and 6.5kV (150, 250, 300V), respectively. The HBM and MM ESD levels of n-type substrate-triggered SCR are the same with those of p-type substrate-triggered SCR devices due to the same SCR widths.

5.4.3.3 Turn-On Verification

In order to observe the turn-on efficiency of the proposed power-rail ESD clamp circuits, a ESD-like voltage pulse with a rise time of 10ns and a pulse height of 5V is applied to the VDD_H power line with the grounded VSS to simulate the rising edge of a positive-to-VSS HBM ESD pulse. The ESD-like voltage pulse will start the ESD detection circuit to trigger on the SCR device. The triggered-on SCR device can provide a low impedance path from VDD_H to VSS. The measured voltage waveforms on VDD_H power line under ESD-like

stress condition are shown in Fig. 5.29(a) with the p-type substrate-triggered SCR device and in Fig. 5.29(b) with the n-type substrate-triggered SCR device. In Fig. 5.29, the applied 5V voltage pulse is quickly clamped down to a low voltage level of ~2.4V by the proposed ESD clamp circuit. The turn-on time is ~5ns, which is estimated from the maximum voltage peak to the clamped low voltage level in Fig. 5.29. According to the measured voltage waveforms, the proposed 2×VDD-tolerant power-rail ESD clamp circuits during the ESD stress event have been successfully verified with high turn-on efficiency.

4.5 Summary

New design of power-rail ESD clamp circuit to achieve low standby leakage current and area efficiency has been proposed and successfully verified in a 65nm 1V fully-silicided CMOS technology. The new proposed ESD-transient detection circuit is realized with only 1V devices without suffering the gate leakage issue. According to the measured results, the proposed power-rail ESD clamp circuit with the consideration of gate leakage current demonstrates a low standby leakage current of only 16.4nA under 1V bias at 25°C. In addition, with the layout design of embedded ESD-transient detection circuit, the power-rail ESD clamp circuit can save over 16% layout area with better ESD discharging capabilities of It2, HBM, and MM ESD levels, which are 1.6 times the values of p-type triggered design. Overall, the proposed power-rail ESD clamp circuit performs excellent turn-on efficiency due to low trigger voltage. The proposed power-rail ESD clamp circuit with low standby leakage current and high area efficiency is an excellent on-chip ESD protection solution in advanced nanoscale CMOS technologies without latchup issue.

New designs of 2×VDD-tolerant power-rail ESD clamp circuits with low standby leakage current have also been proposed and successfully verified in a 65nm 1V fully-silicided CMOS technology. The new proposed ESD-transient detection circuit is realized with only 1V devices without suffering the gate oxide reliability issue under 1.8V (2×VDD) applications. According to the measured results, the proposed 2×VDD-tolerant power-rail ESD clamp circuits with the consideration of gate leakage current demonstrate a very small standby leakage current of only 34.1nA for the p-type substrate-triggered SCR device with a width of 50μm and 103.7nA for the n-type one under 1.8V bias at 25°C. Moreover, the proposed power-rail ESD clamp circuits also perform excellent turn-on efficiency. The new proposed 2×VDD-tolerant power-rail ESD clamp circuit with low standby leakage current is a superior design technique for on-chip ESD protection in the mixed-voltage I/O interfaces.

Table 5.1

Leakage Currents of the Conventional Power-Rail ESD Clamp Circuits under Different Temperatures at 1V in a 65nm CMOS Process

Standby Leakage Current at 1V Normal Operating Voltage	Traditional *RC*-Base Power-Rail ESD Clamp Circuit	Capacitor-Less Design of Power-Rail ESD Clamp Circuit [47]
25°C	760.42μA	12.86μA
50°C	12.62mA	1.19mA
100°C	85.02mA	71.65mA

Table 5.2

Design Parameters of the Proposed Power-Rail ESD Clamp Circuits

Design Parameters	P-Type Triggered Design			N-Type Triggered Design		
Rp (Ω)	None			1.9k		
Rn (Ω)	25k			25k		
Dc (μm^2)	156.75			156.75		
Dt (μm^2)	None			24.40		
Dp (μm^2)	24.40			1.14		
Dn (μm^2)	1.14			24.40		
Mp (W/L) (μm)	40, 60, 80 / 0.12			4 / 0.12		
Mn (W/L) (μm)	8 / 0.12			40, 60, 80 / 0.12		
Widths of SCR (μm)	30	40	50	30	40	50

Table 5.3

Device Dimension of the Proposed Power-Rail ESD Clamp Circuits and Embedded ESD-Transient Detection Circuit

New Proposed Power-Rail ESD Clamp Circuit in Fig. 5.5(a)									
Rn (kΩ)	25.33								
Dc (μm^2)	156.74								
Dp & Dn (μm^2)	14 & 1.15								
Mn Width (μm)	8								
SCR Width (μm)	25			35			45		
Mp Width (μm)	35	70	140	35	70	140	35	70	140
Power-Rail ESD Clamp Circuit with Embedded ESD-Transient Detection Circuit									
Dc	N+ Guardring								
Dp & Dn (μm^2)	10			14			18		
SCR Width (μm)	25			35			45		
Mp and Mn Width (μm)	25	50	100	35	70	140	45	90	180

Table 5.4

TLP Measured Results and ESD Robustness of the Fabricated Power-Rail ESD Clamp Circuit

P-Type Triggered Design									
SCR Width (μm)	30			40			50		
Mp Width (μm)	40	60	80	40	60	80	40	60	80
Vt1 (V)	3.49	2.97	2.79	3.79	3.23	2.95	3.95	3.38	3.15
It2 (A)	2.08	2.08	2.07	2.64	2.64	2.65	3.30	3.35	3.33
HBM (kV)	3.5	3.5	3.5	5.0	5.0	5.0	6.5	6.5	6.5
MM (V)	150	150	150	250	250	250	300	300	300
N-Type Triggered Design									
Mn Width (μm)	40	60	80	40	60	80	40	60	80
Vt1 (V)	3.70	3.51	3.42	3.98	3.69	3.56	4.16	3.77	3.62
It2 (A)	2.08	2.08	2.08	2.64	2.64	2.65	3.29	3.32	3.32
HBM (kV)	3.5	3.5	3.5	5.0	5.0	5.0	6.5	6.5	6.5
MM (V)	150	150	150	250	250	250	300	300	300

Table 5.5

TLP Measured Characteristics and ESD Robustness of the Power-Rail ESD Clamp Circuits with P-Type Triggered Design and Embedded ESD-Transient Detection Circuit Design

Power-Rail ESD Clamp Circuit with P-Type Triggered Design									
SCR Width (μm)	25			35			45		
Mp Width (μm)	35	70	140	35	70	140	35	70	140
Vt1 (V)	3.25	2.67	2.45	3.54	2.82	2.54	3.65	2.86	2.58
It2 (A)	1.53	1.55	1.56	2.13	2.15	2.16	2.76	2.76	2.78
HBM (kV)	3	3	3	4	4	4	5	5	5
MM (V)	150	150	150	200	200	200	250	250	250
Power-Rail ESD Clamp Circuit with Embedded ESD-Transient Detection Circuit									
SCR Width (μm)	25			35			45		
Mp & Mn Width (μm)	25	50	100	35	70	140	45	90	180
Vt1 (V)	3.74	3.09	2.50	2.70	2.52	2.14	2.51	2.34	2.02
It2 (A)	2.53	2.55	2.55	3.43	3.52	3.53	4.58	4.54	4.52
HBM (kV)	4	4	4	5.5	5.5	5.5	7	7	7
MM (V)	200	200	200	300	300	300	350	350	350

Table 5.6

Measured Leakage Currents of the Fabricated Power-Rail ESD Clamp Circuits under Different Temperatures at 1V

P-Type Triggered Design									
SCR Width (μm)	30			40			50		
Mp Width (μm)	40	60	80	40	60	80	40	60	80
25°C	15.6nA	19.4nA	23.3nA	16.2nA	19.5nA	24.2nA	16.4nA	20.2nA	24.8nA
125°C	0.67μA	0.78μA	0.88μA	0.68μA	0.80μA	0.89μA	0.69μA	0.81μA	0.91μA
N-Type Triggered Design									
Mn Width (μm)	40	60	80	40	60	80	40	60	80
25°C	41.0nA	59.0nA	82.5nA	42.1nA	60.2nA	83.9nA	42.9nA	63.7nA	84.3nA
125°C	2.03μA	2.75μA	3.34μA	2.05μA	2.77μA	3.35μA	2.06μA	2.79μA	3.36μA

Table 5.7

Leakage Currents of Power-Rail ESD Clamp Circuits with P-Type Triggered Design and Embedded ESD-Transient Detection Circuit Design under 1V Bias at Different Temperatures

Power-Rail ESD Clamp Circuit with P-Type Triggered Design									
SCR Width	25μm			35μm			45μm		
Mp Width	35μm	70μm	140μm	35μm	70μm	140μm	35μm	70μm	140μm
25°C	11.05nA	18.08nA	30.78nA	11.54nA	18.36nA	31.11nA	12.16nA	18.83nA	31.15nA
50°C	23.50nA	43.72nA	81.87nA	23.79nA	44.08nA	82.76nA	24.06nA	43.72nA	83.03nA
100°C	0.27μA	0.37μA	0.57μA	0.27μA	0.37μA	0.58μA	0.27μA	0.37μA	0.58μA
Power-Rail ESD Clamp Circuit with Embedded ESD-Transient Detection Circuit									
SCR Width	25μm			35μm			45μm		
Mp & Mn Width	25μm	50μm	100μm	35μm	70μm	140μm	45μm	90μm	180μm
25°C	28.85nA	58.52nA	124.9nA	38.46nA	83.81nA	175.7nA	50.58nA	108.2nA	231.7nA
50°C	0.08μA	0.19μA	0.40μA	0.12μA	0.27μA	0.57μA	0.16μA	0.36μA	0.76μA
100°C	0.59μA	1.23μA	2.53μA	0.82μA	1.74μA	3.53μA	1.05μA	2.21μA	4.66μA

Table 5.8

Design Parameters of the Proposed 2×VDD-Tolerant Power-Rail ESD Clamp Circuits

Design Parameters	P-Type Substrate-Triggered			N-Type Substrate-Triggered		
Rp (Ω)	None			1.9k		
Rn (Ω)	25k			25k		
Mp (W/L)	40μm / 0.12μm			4μm / 0.12μm		
Mn (W/L)	8μm / 0.12μm			40μm / 0.12μm		
Dp1 & Dp2 (μm^2)	24.40			1.14		
Dn1 & Dn2 (μm^2)	1.14			24.40		
Dc (μm^2)	156.75			156.75		
Dt (μm^2)	None			24.40		
D_{SCR} (μm^2)	30×3	40×3	50×3	30×3	40×3	50×3
Widths of SCR (μm)	30	40	50	30	40	50

Table 5.9

Leakage Currents of the Proposed 2×VDD-Tolerant Power-Rail ESD Clamp Circuits at 1.8V

Standby Leakage Current at 1.8V Normal Operating Voltage	P-Type Substrate-Triggered			N-Type Substrate-Triggered		
	SCR Width (μm)			SCR Width (μm)		
	30	40	50	30	40	50
25°C	32.7nA	33.1nA	34.1nA	100.6nA	101.4nA	103.7nA
125°C	1.35μA	1.36μA	1.38μA	4.72μA	4.73μA	4.74μA

Table 5.10

ESD Robustness of the Proposed 2×VDD-Tolerant Power-Rail ESD Clamp Circuits

	P-Type Substrate-Triggered			N-Type Substrate-Triggered		
	SCR Width (μm)			SCR Width (μm)		
	30	40	50	30	40	50
It2 (A)	2.05	2.68	3.29	2.11	2.75	3.34
HBM ESD Level (kV)	3.5	5.0	6.5	3.5	5.0	6.5
MM ESD Level (V)	150	250	300	150	250	300

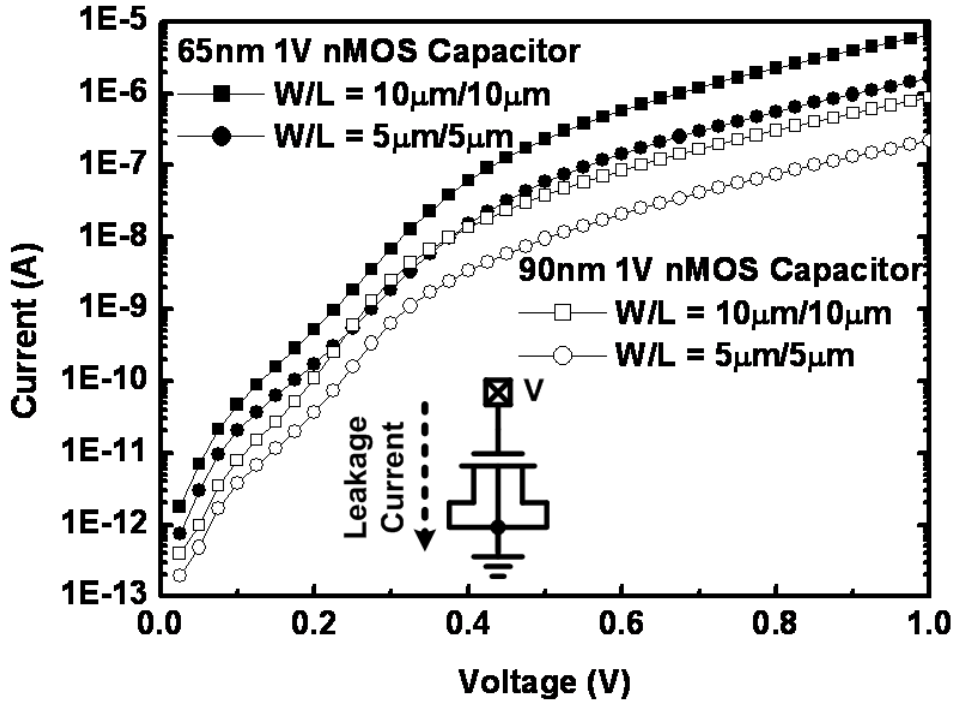


Fig. 5.1 Simulated gate currents of the nMOS capacitors in 65nm and 90nm CMOS technologies.

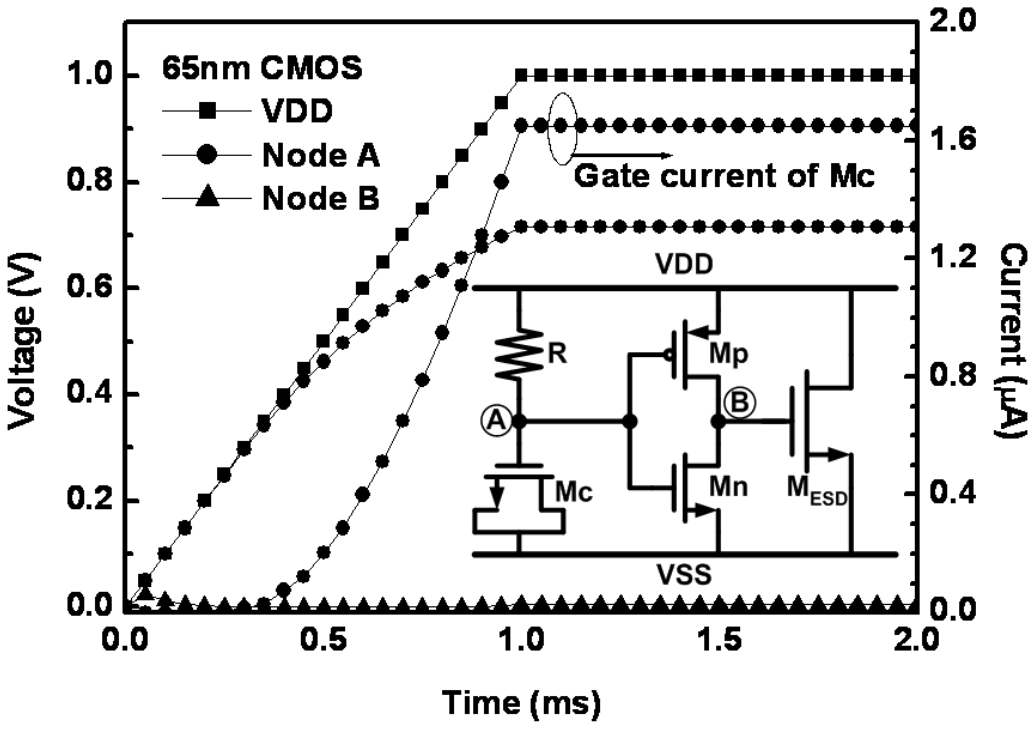


Fig. 5.2 Simulated node voltages of the traditional *RC*-based power-rail ESD clamp circuit [8] and the gate current flowing through the MOS capacitor Mc under the normal power-on condition with a rise time of 1ms in a 65nm CMOS process.

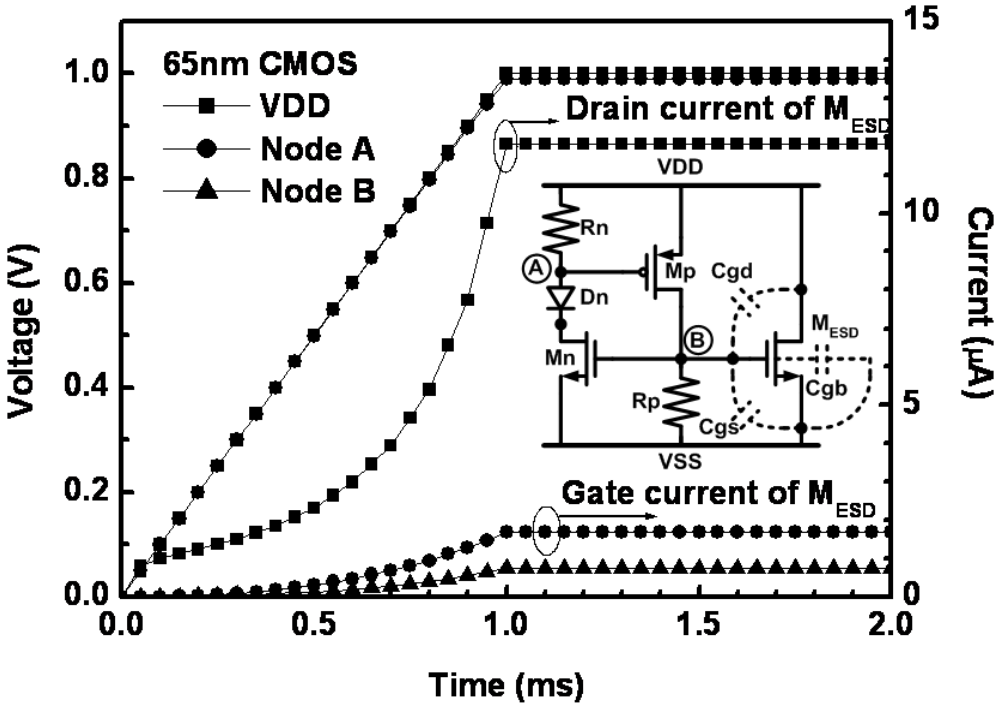


Fig. 5.3 Simulated node voltages of the capacitor-less power-rail ESD clamp circuit [47], the drain current, and the gate current flowing through the clamp device M_{ESD} under the normal power-on transition.

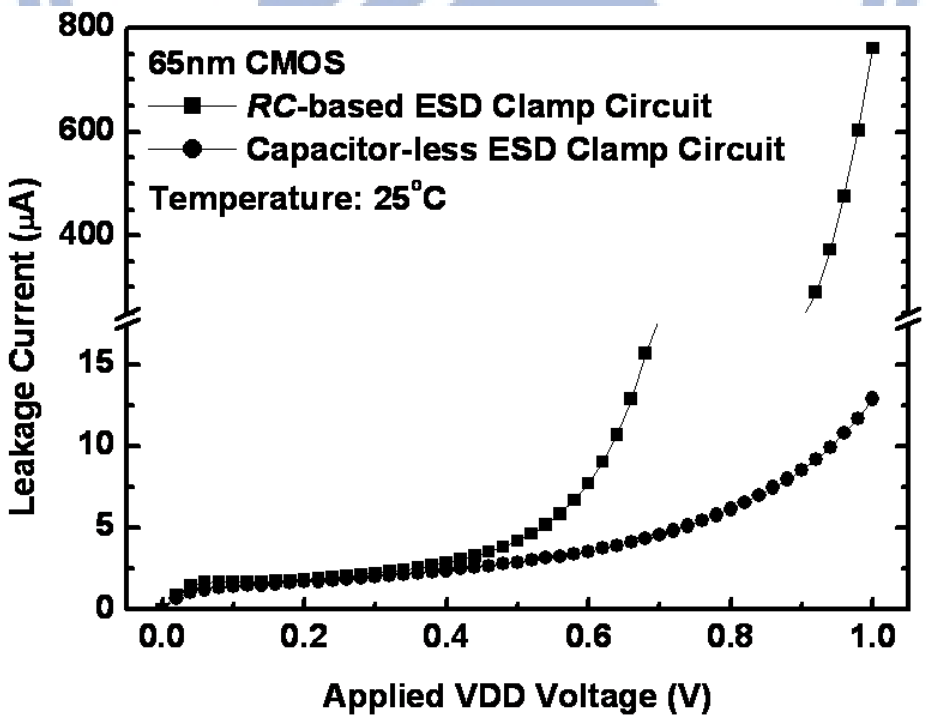
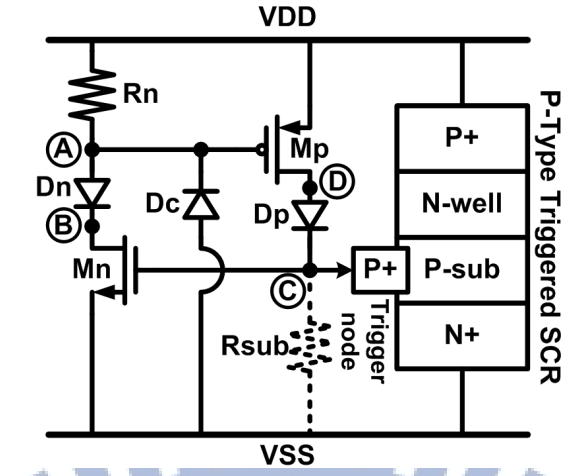
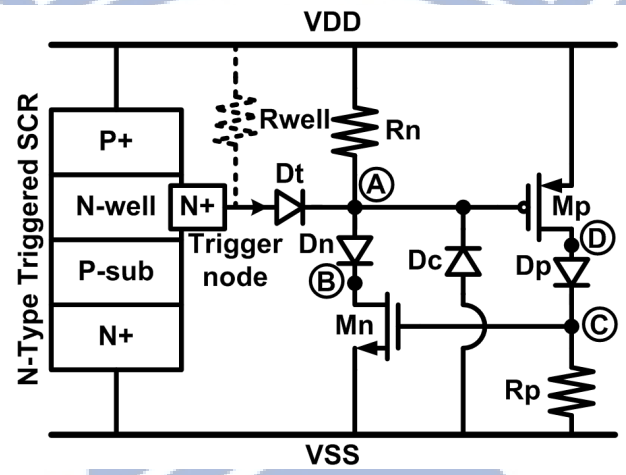


Fig. 5.4 The measured standby leakage currents of the traditional *RC*-based and the capacitor-less power-rail ESD clamp circuits.



(a)



(b)

Fig. 5.5 The proposed low standby leakage power-rail ESD clamp circuits with (a) the p-type triggered SCR device, (b) the n-type triggered SCR device, as the ESD clamp devices.

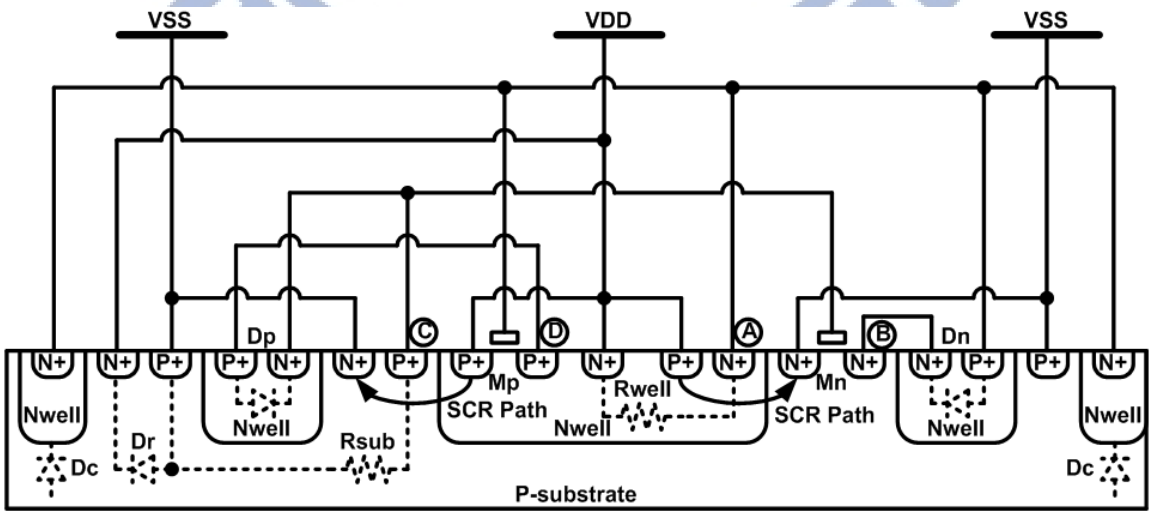
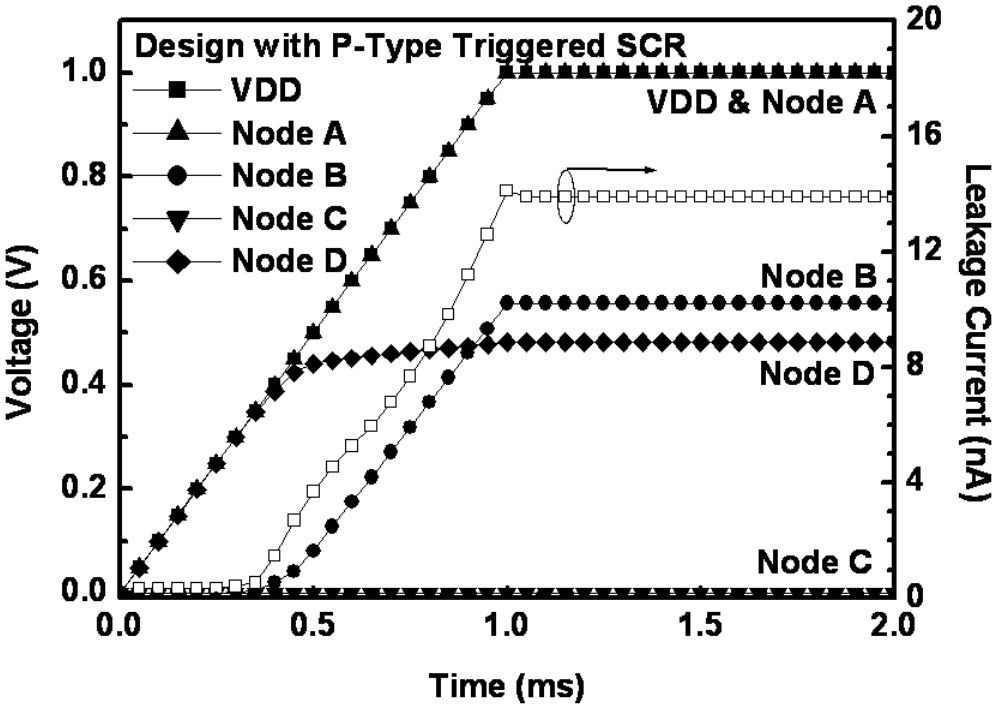
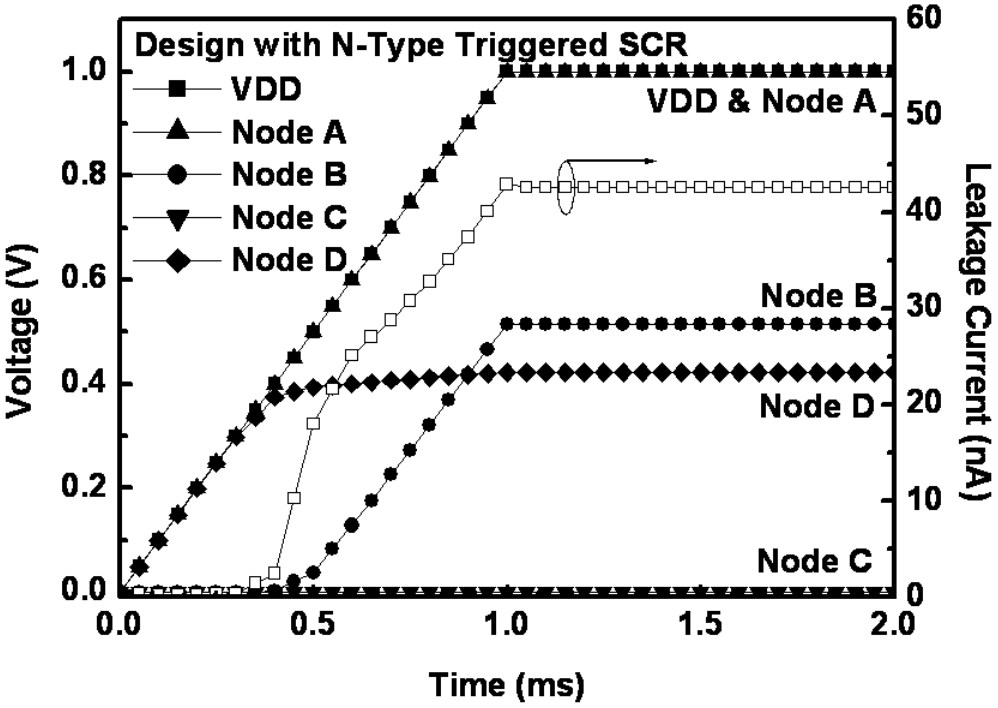


Fig. 5.6 Cross-sectional view of the proposed power-rail ESD clamp circuit with embedded ESD-transient detection circuit.

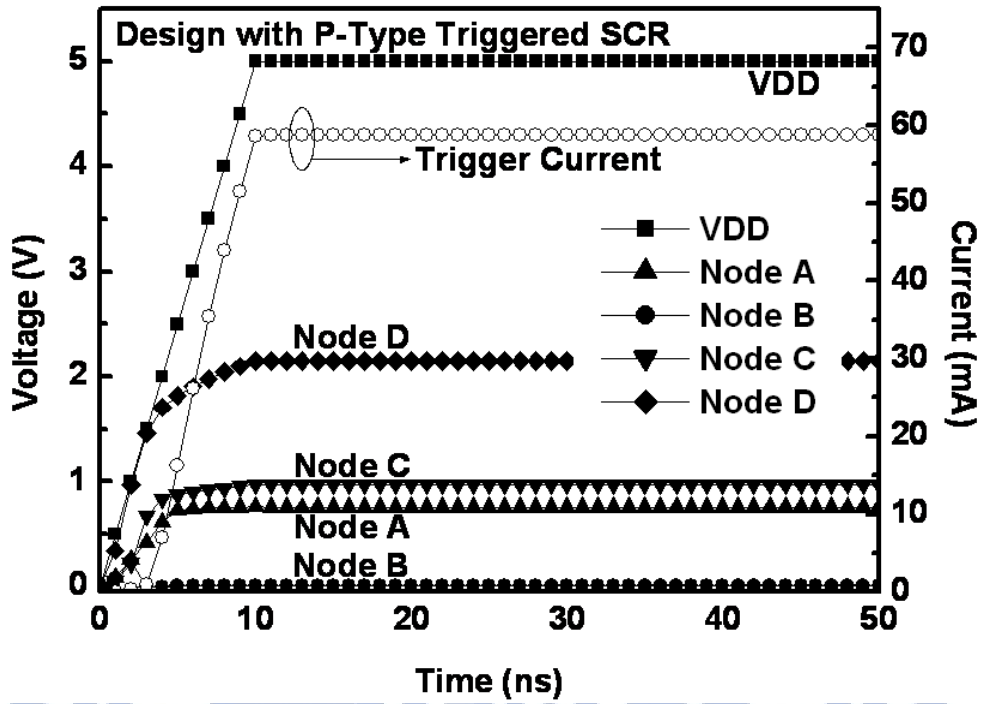


(a)

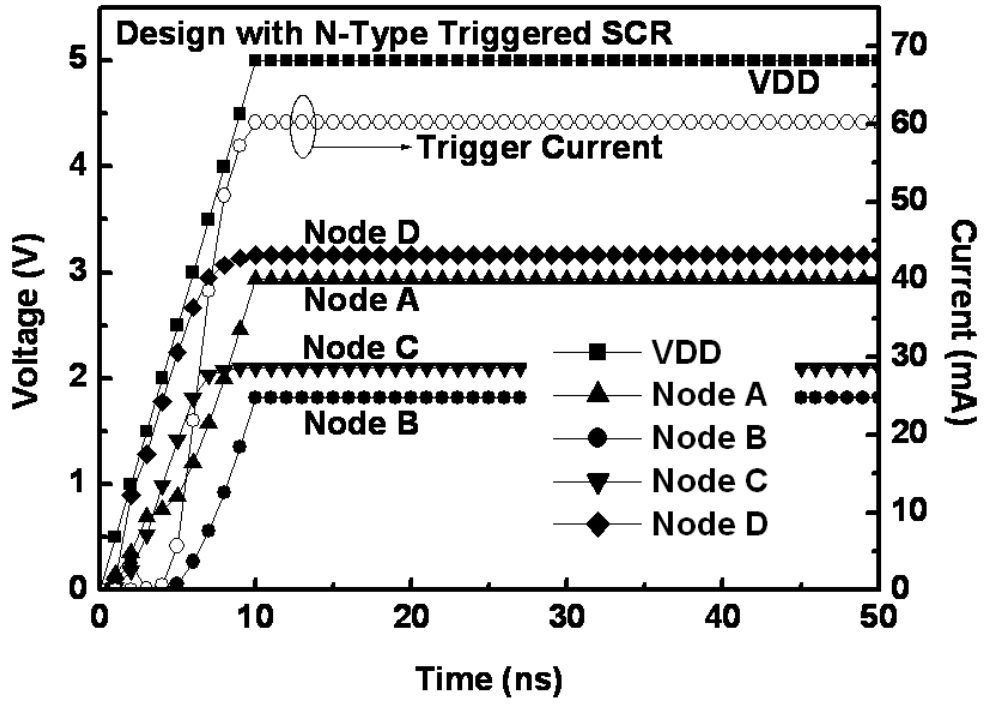


(b)

Fig. 5.7 Simulated voltage waveforms on the nodes and the leakage current of the ESD-transient detection circuit with (a) the p-type, and (b) the n-type, triggered SCR devices in 65nm 1V CMOS process under the normal power-on transition.

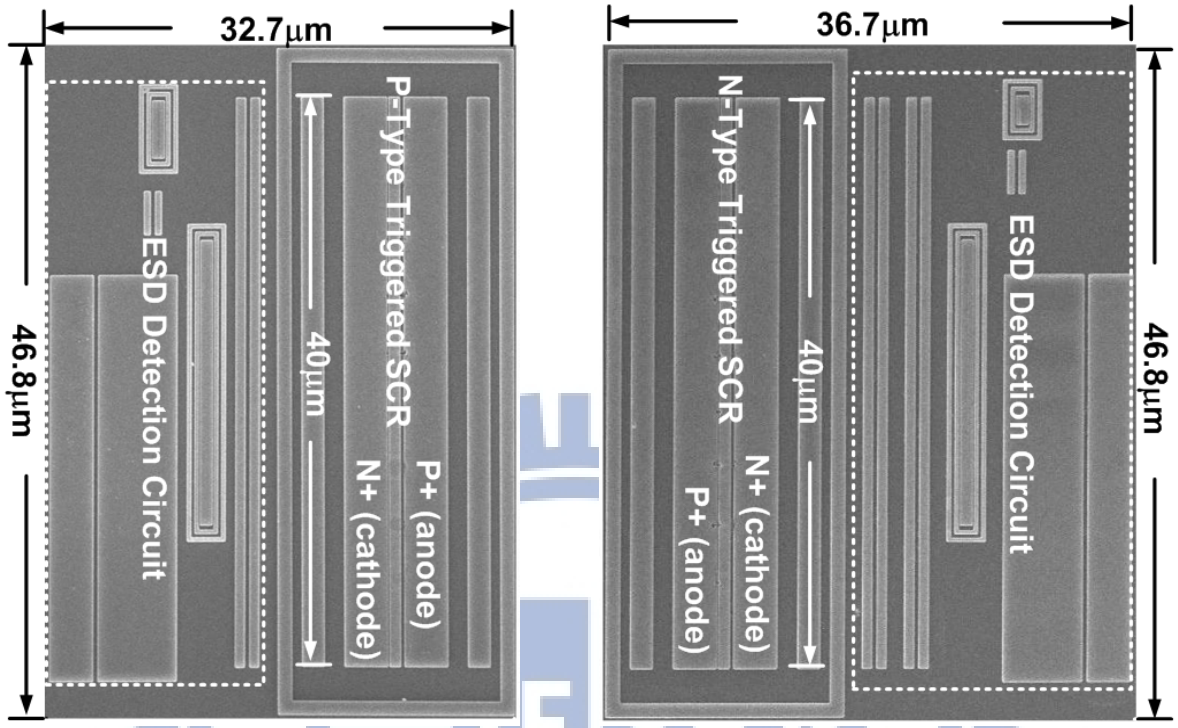


(a)



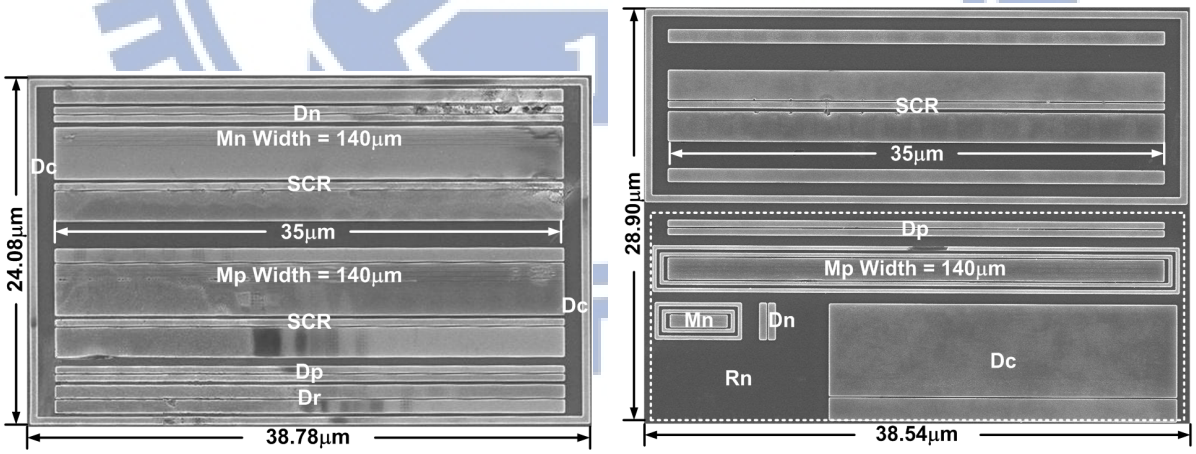
(b)

Fig. 5.8 Simulated voltages on the nodes and the trigger current of the ESD-transient detection circuit with (a) the p-type, and (b) the n-type, triggered SCR devices in 65nm 1V CMOS process under the ESD-like transition.



(a) (b)

Fig. 5.9 The microphotograph of the fabricated power-rail ESD clamp circuits with (a) the p-type triggered SCR and (b) the n-type triggered SCR, as the ESD clamp devices.



(a) (b)

Fig. 5.10 The microphotograph of the fabricated power-rail ESD clamp circuit with the SCR device of 35μm in width. (a) Embedded ESD-transient detection circuit design and (b) the p-type triggered design.

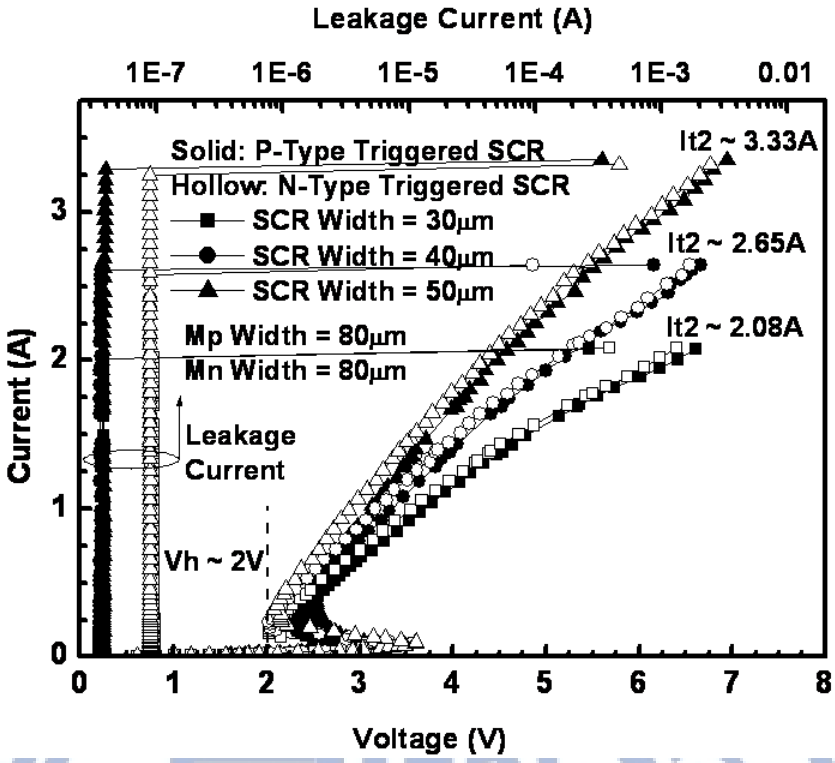


Fig. 5.11 TLP measured *I-V* curves of the fabricated power-rail ESD clamp circuits with the SCR devices of different widths under positive VDD-to-VSS ESD stress for the p-type and n-type triggered SCR designs.

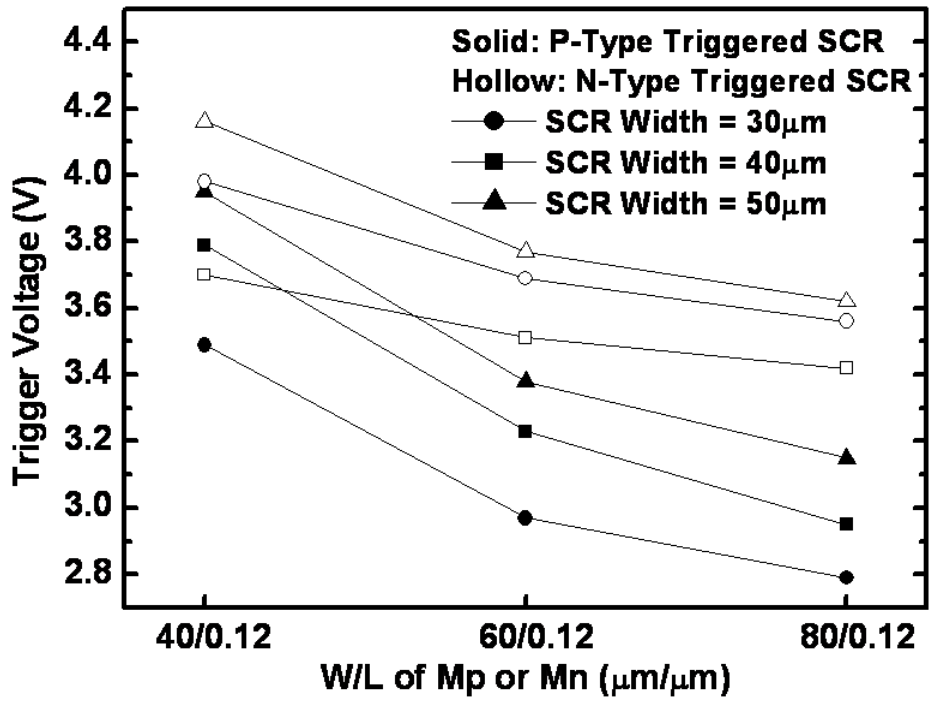
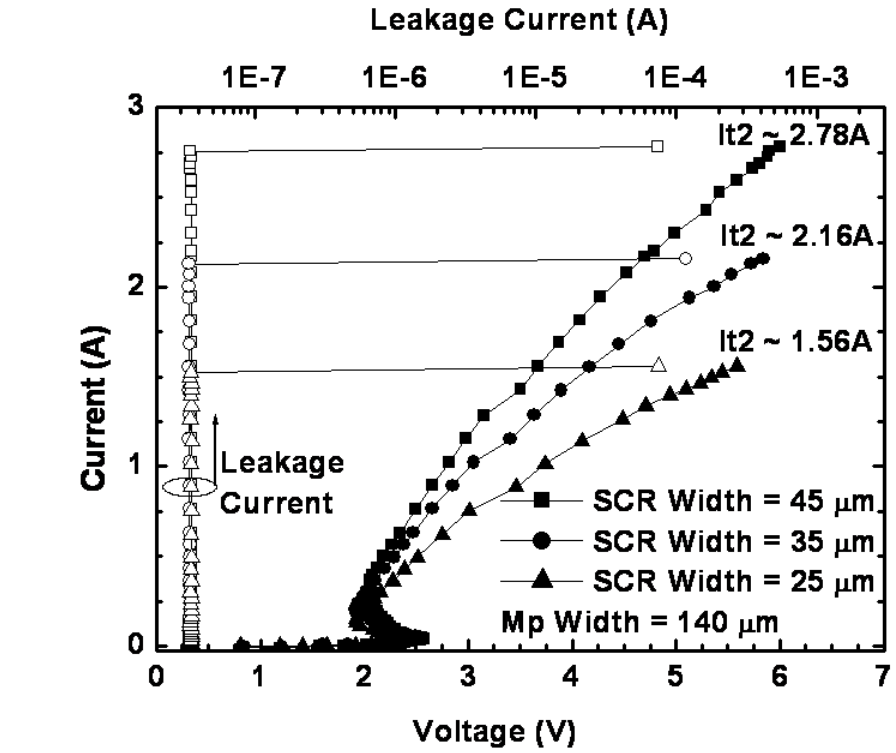
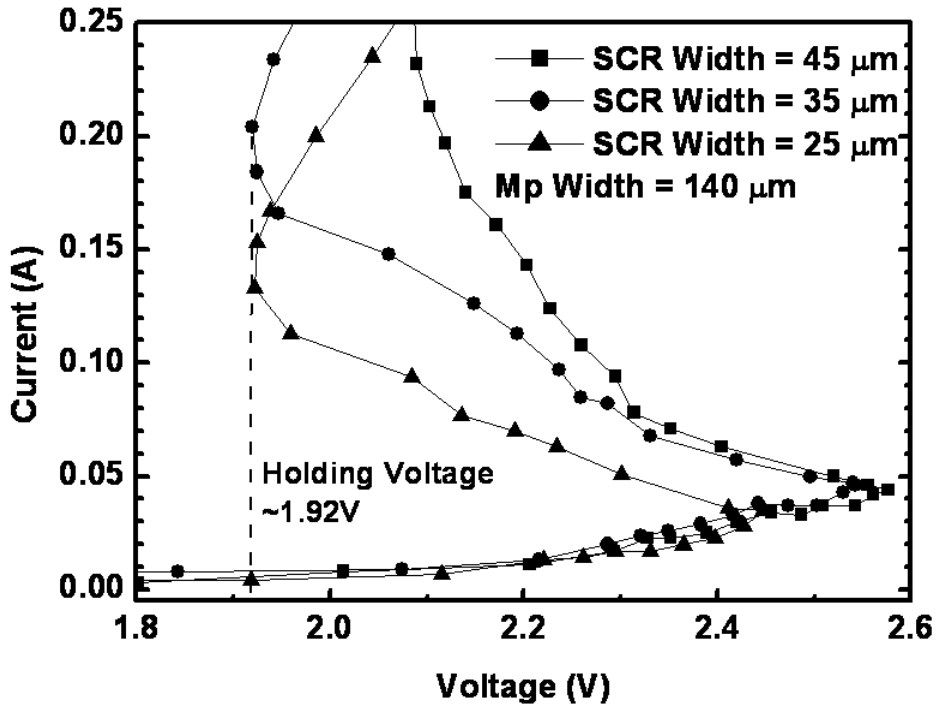


Fig. 5.12 TLP measured trigger voltage of the p-type and n-type triggered design with different width of Mp, Mn, and SCR device.

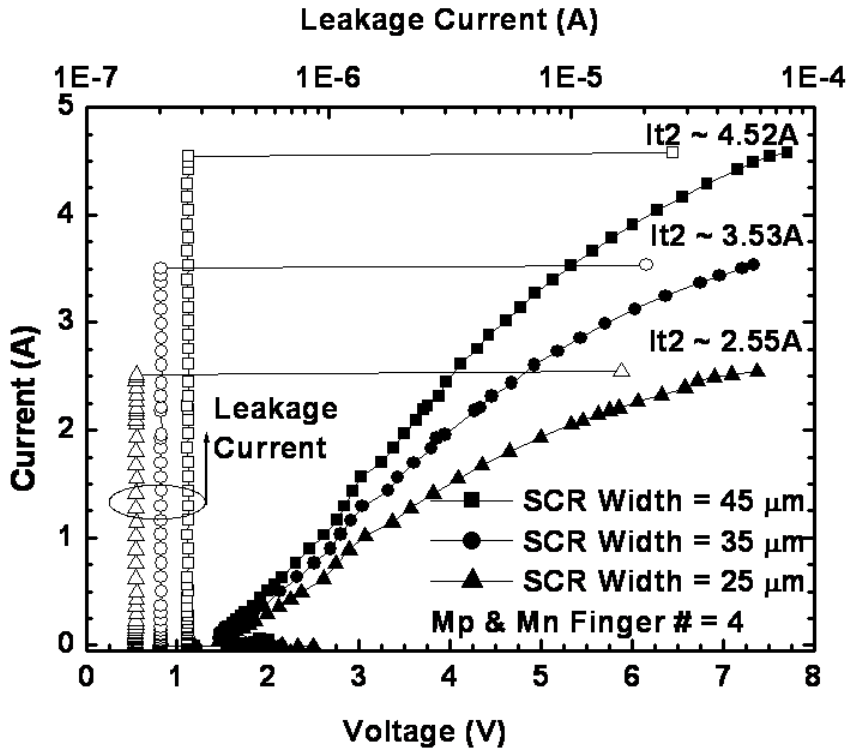


(a)

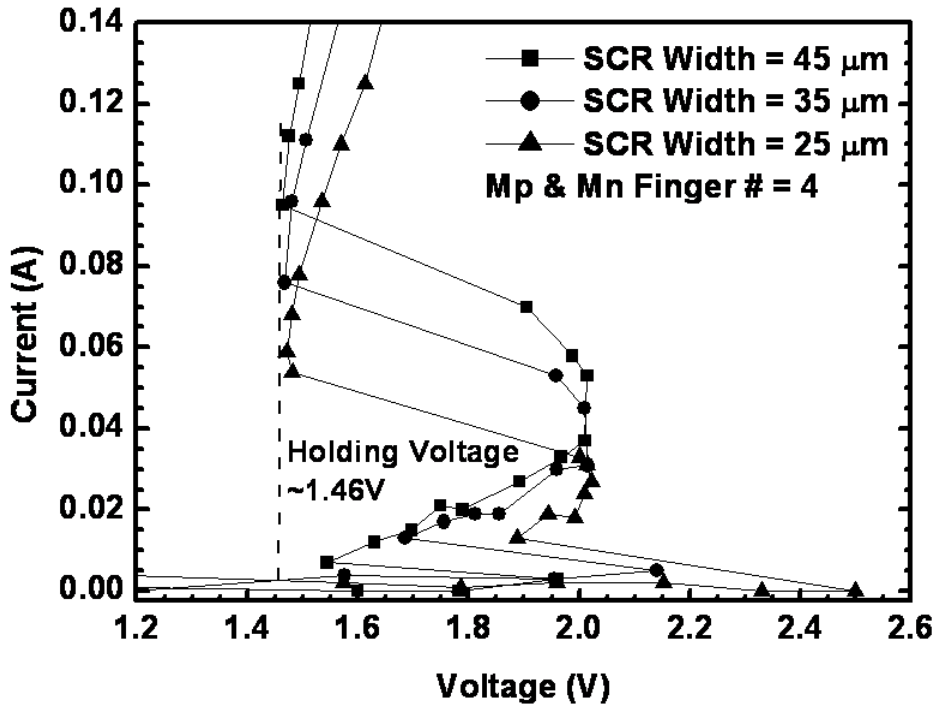


(b)

Fig. 5.13 TLP measured curves of (a) the p-type triggered design with different SCR widths and (b) the zoom-in illustration for the holding voltage (Vh).



(a)



(b)

Fig. 5.14 TLP measured curves of (a) the embedded ESD-transient detection circuit with different SCR widths and (b) the zoom-in illustration for the holding voltage (Vh).

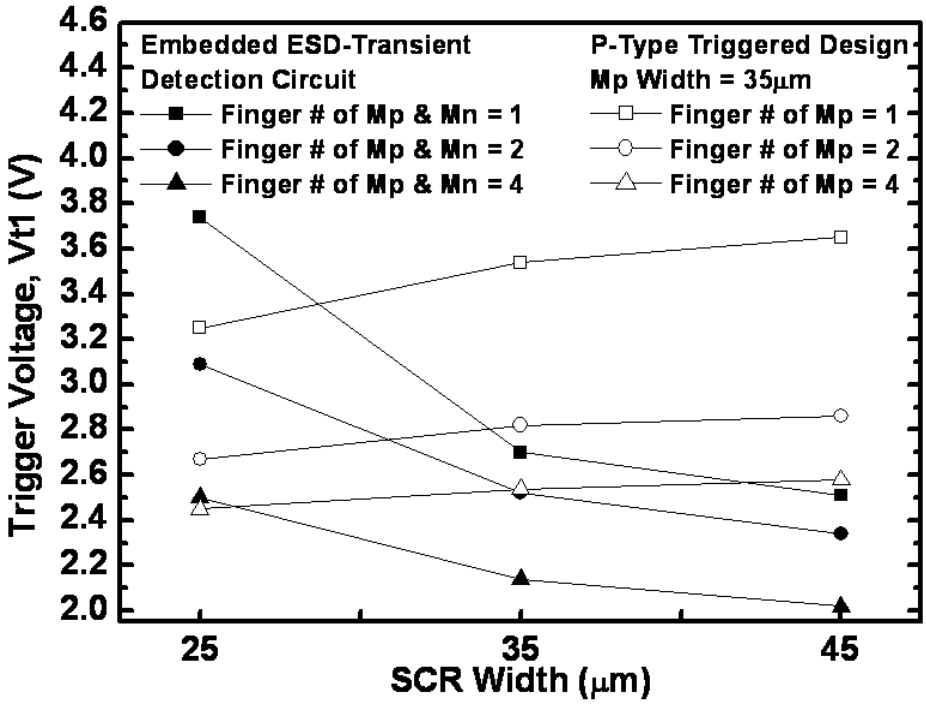


Fig. 5.15 The dependence of the TLP measured trigger voltages on the device dimensions of SCR.

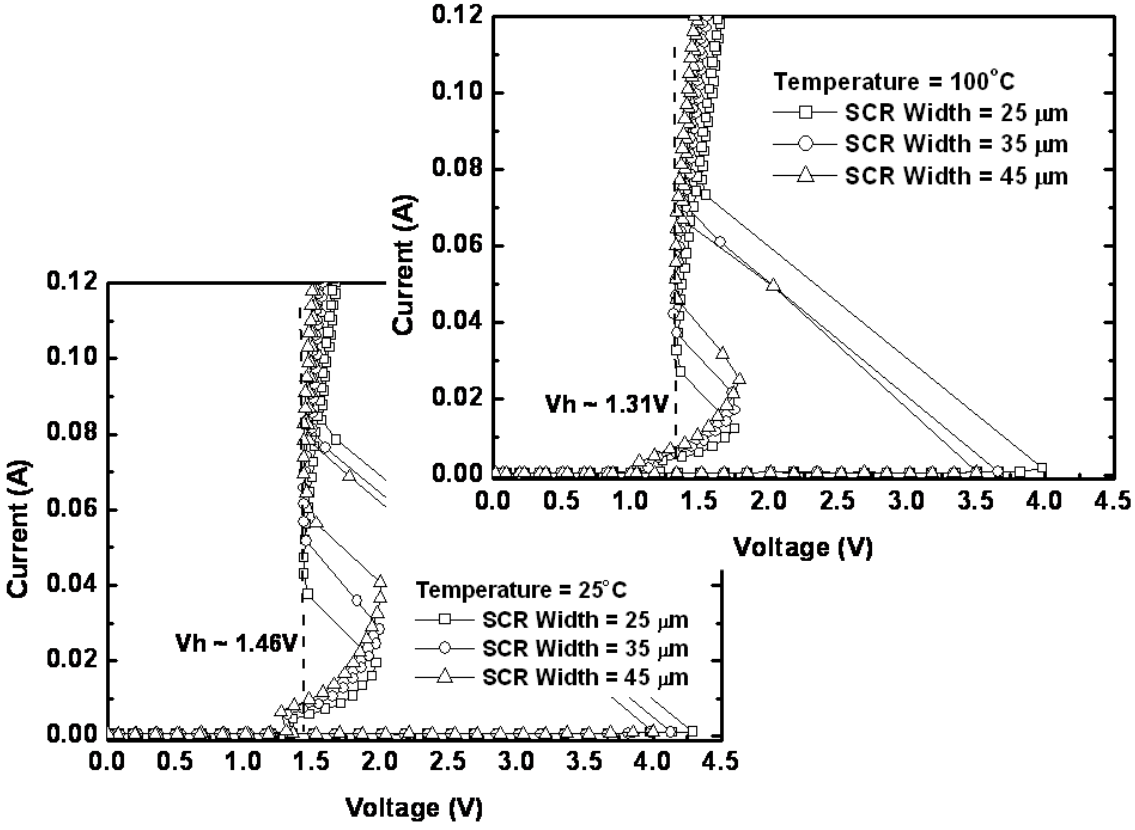


Fig. 5.16 Measured DC *I-V* Characteristics of the embedded ESD-transient detection circuit at different temperatures.

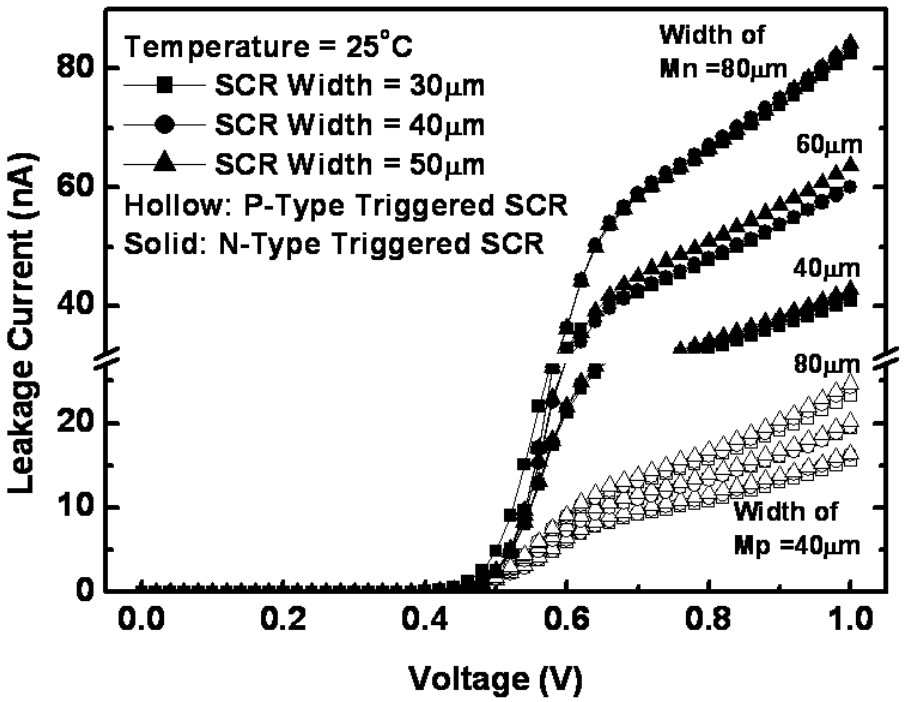


Fig. 5.17 The measured DC *I-V* curves of the fabricated power-rail ESD clamp circuits with SCR devices of different widths.

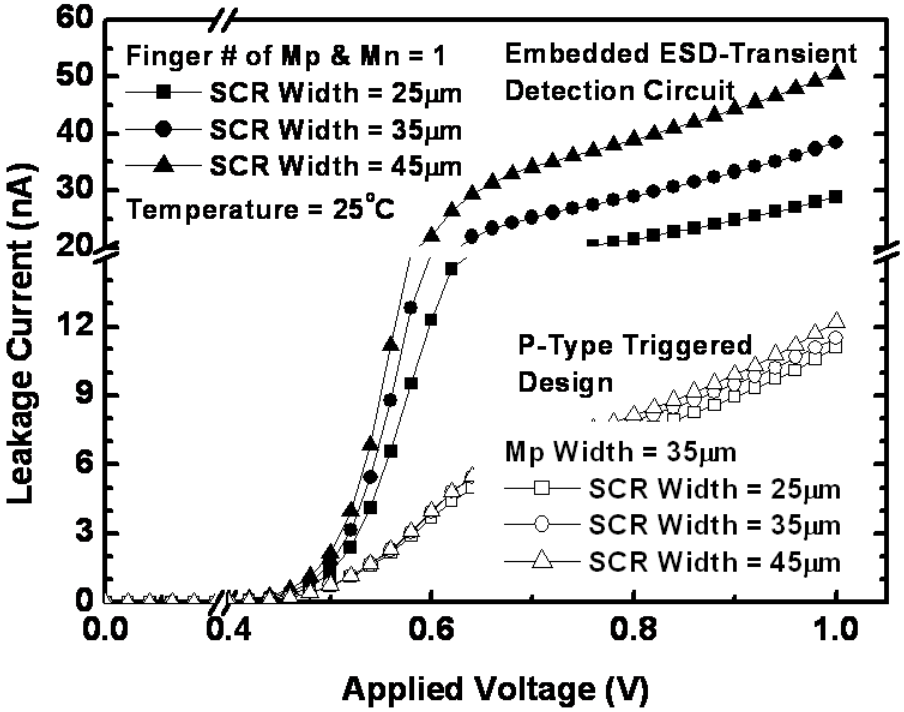
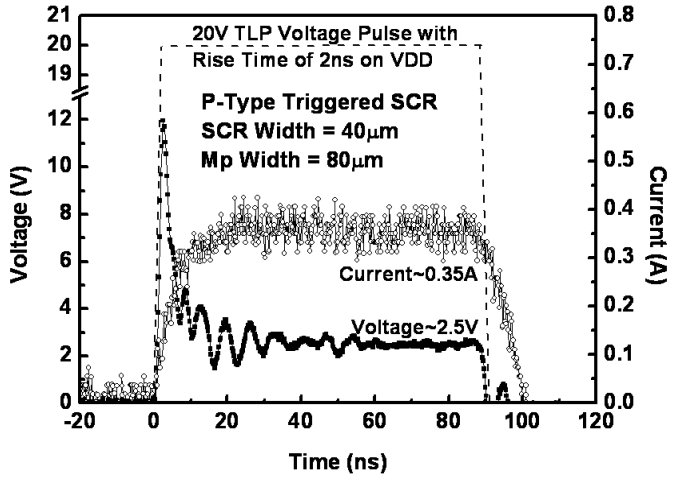
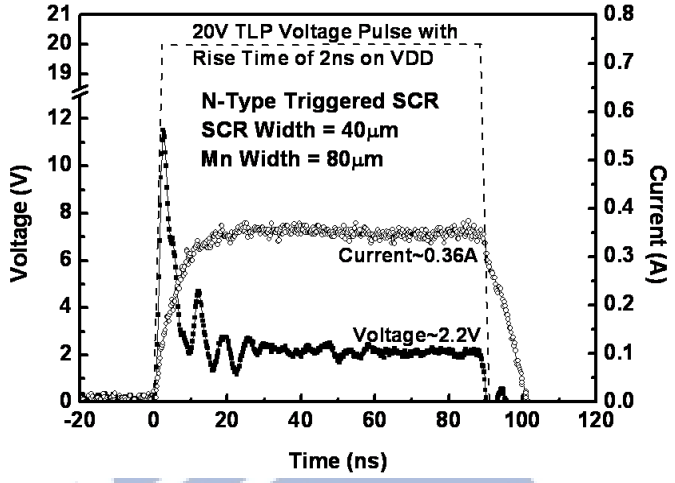


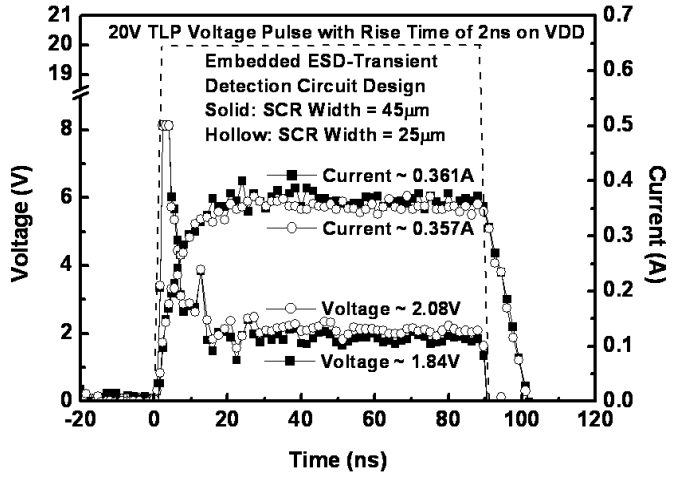
Fig. 5.18 The measured leakage currents of the power-rail ESD clamp circuits with different SCR widths for p-type triggered design and embedded ESD-transient detection circuit design.



(a)



(b)



(c)

Fig. 5.19 Measured voltage and current waveforms of the fabricated power-rail ESD clamp circuits with the SCR devices under TLP transition with different voltage pulse height, (a) the p-type triggered SCR, (b) the n-type triggered SCR, and (d) the embedded ESD-transient detection circuit design.

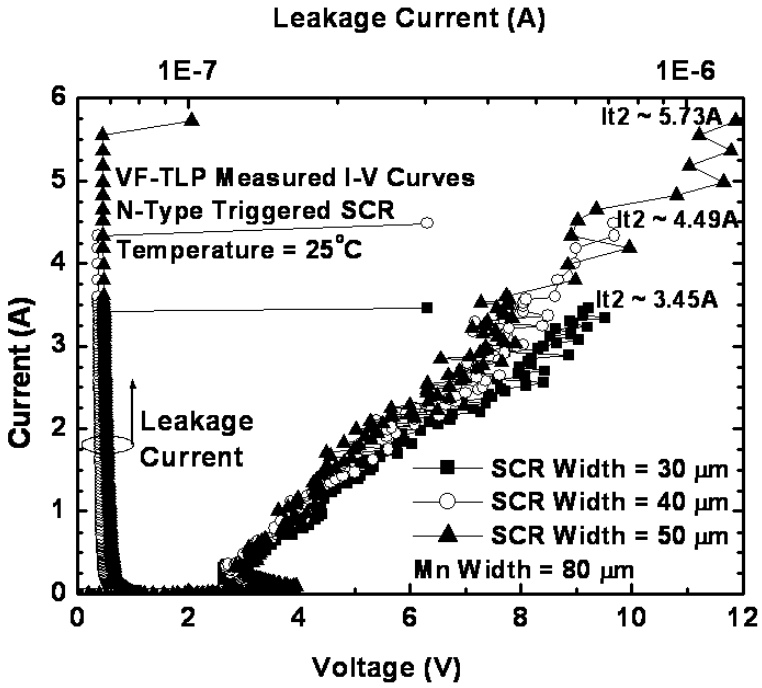


Fig. 5.20 VF-TLP measured *I-V* curves of the fabricated power-rail ESD clamp circuits with the n-type triggered SCR device of different widths under positive VDD-to-VSS ESD stress. The VF-TLP is with a pulse width of 10ns and a rise time of 200ps.

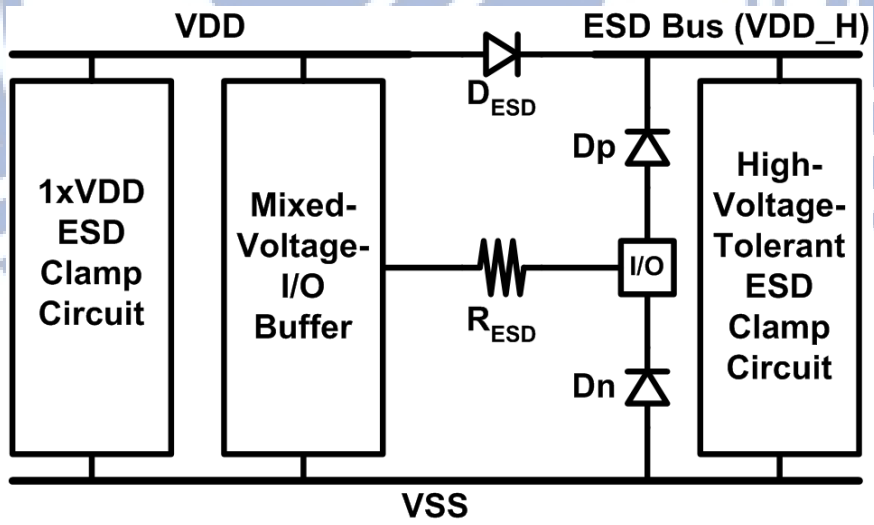
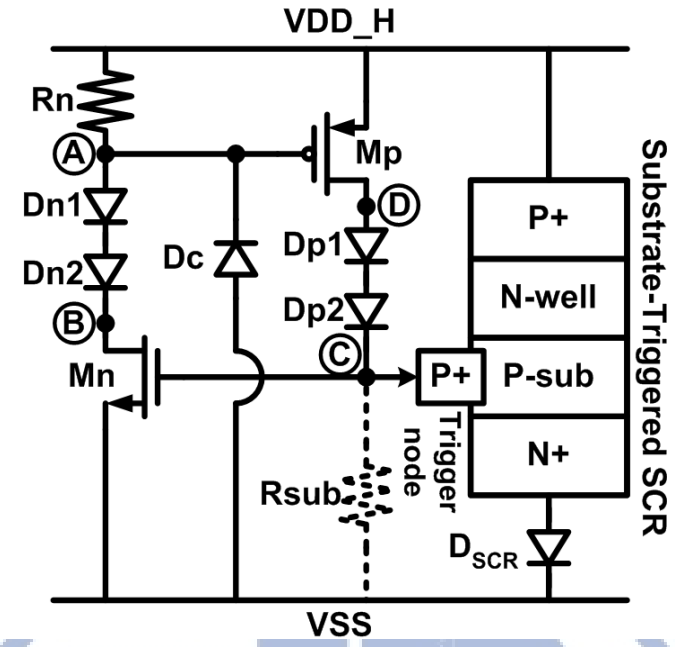
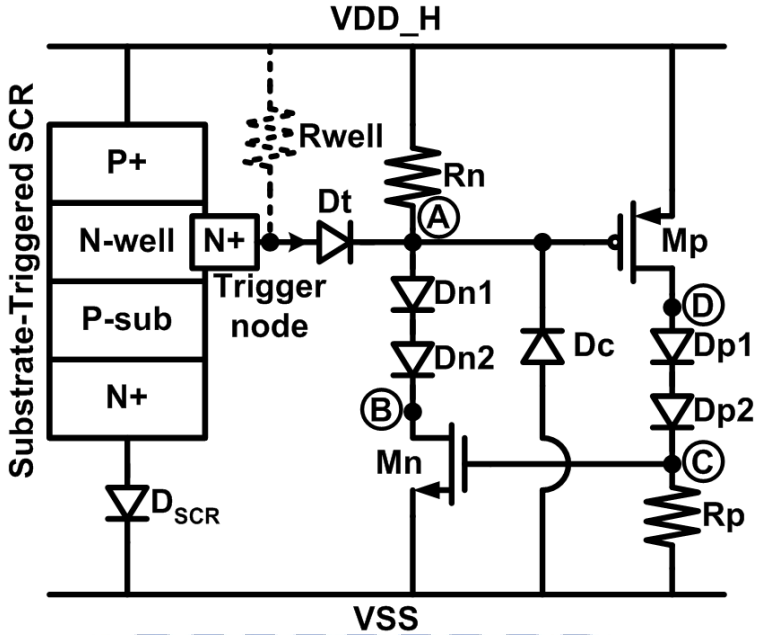


Fig. 5.21 ESD protection scheme with on-chip ESD bus for high-voltage-tolerant mixed-voltage I/O buffer.

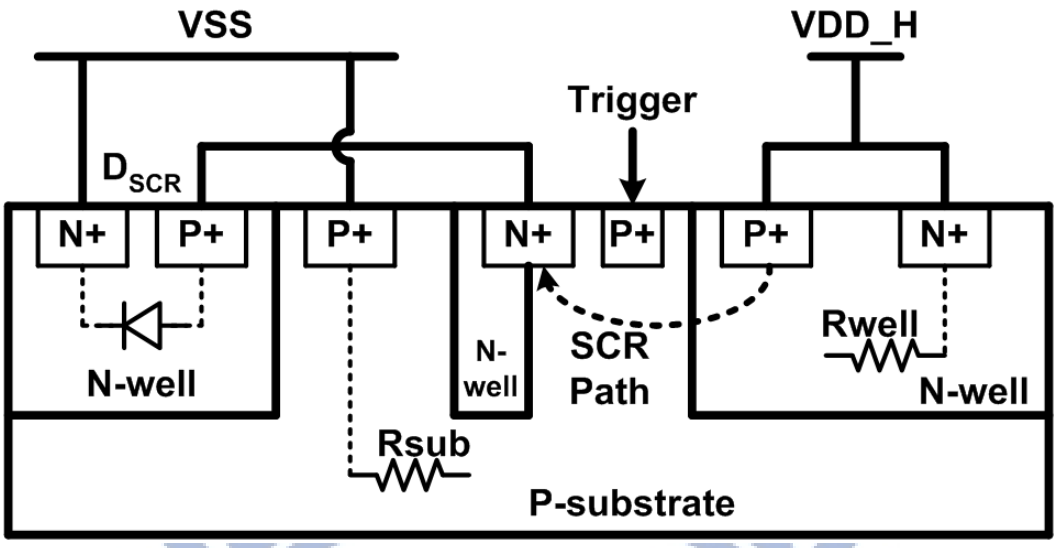


(a)

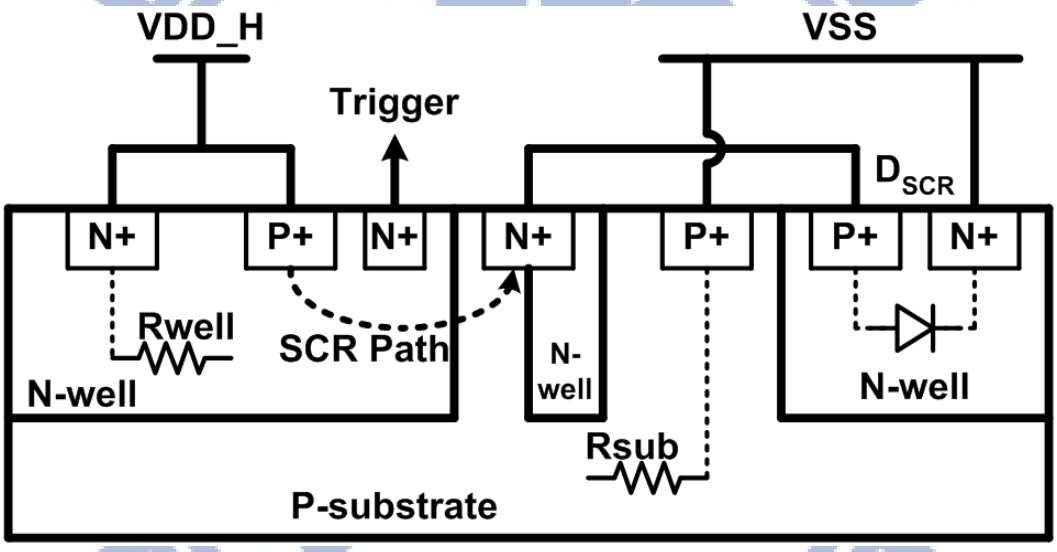


(b)

Fig. 5.22 The proposed low-leakage 2×VDD-tolerant power-rail ESD clamp circuits with the (a) p-type and the (b) n-type triggered SCR as the ESD clamp devices.

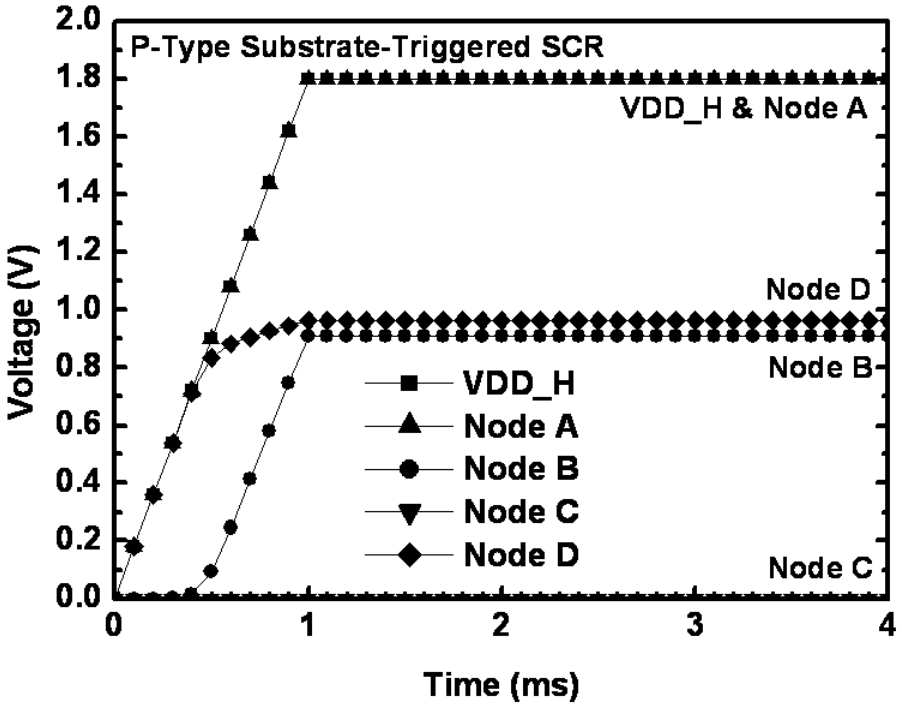


(a)

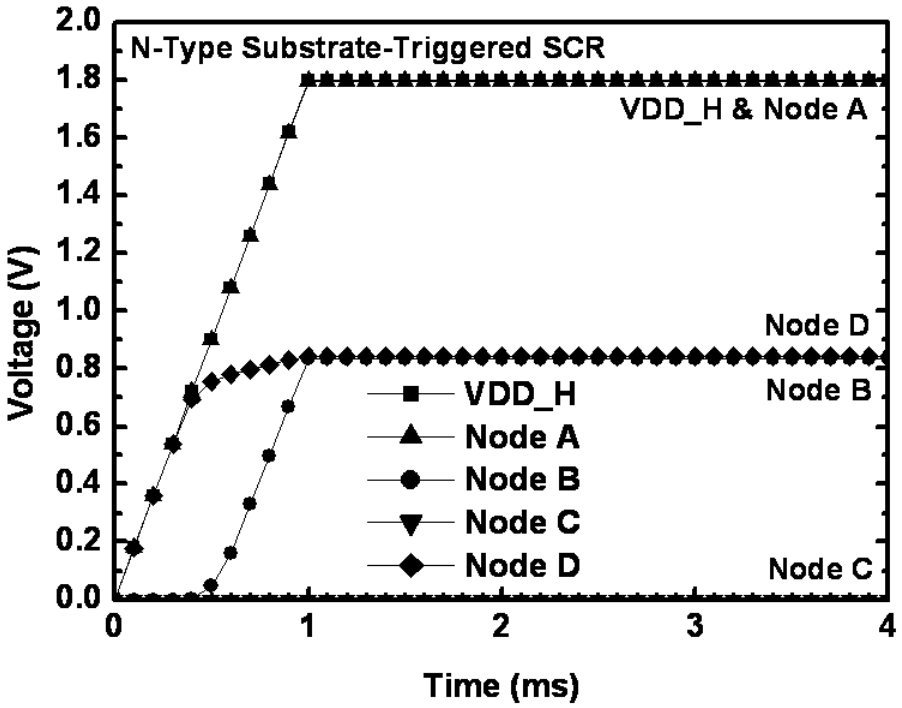


(b)

Fig. 5.23 Cross-sectional view of the ESD clamp devices composed of the (a) p-type and the (b) n-type triggered SCR devices with the cascode diode D_{SCR}.

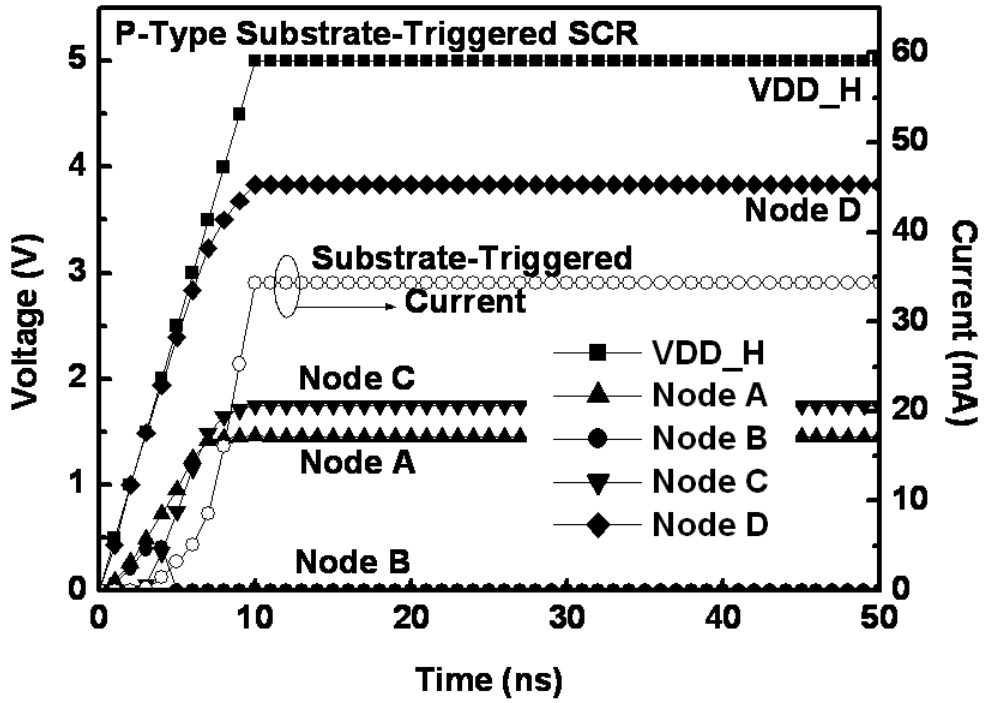


(a)

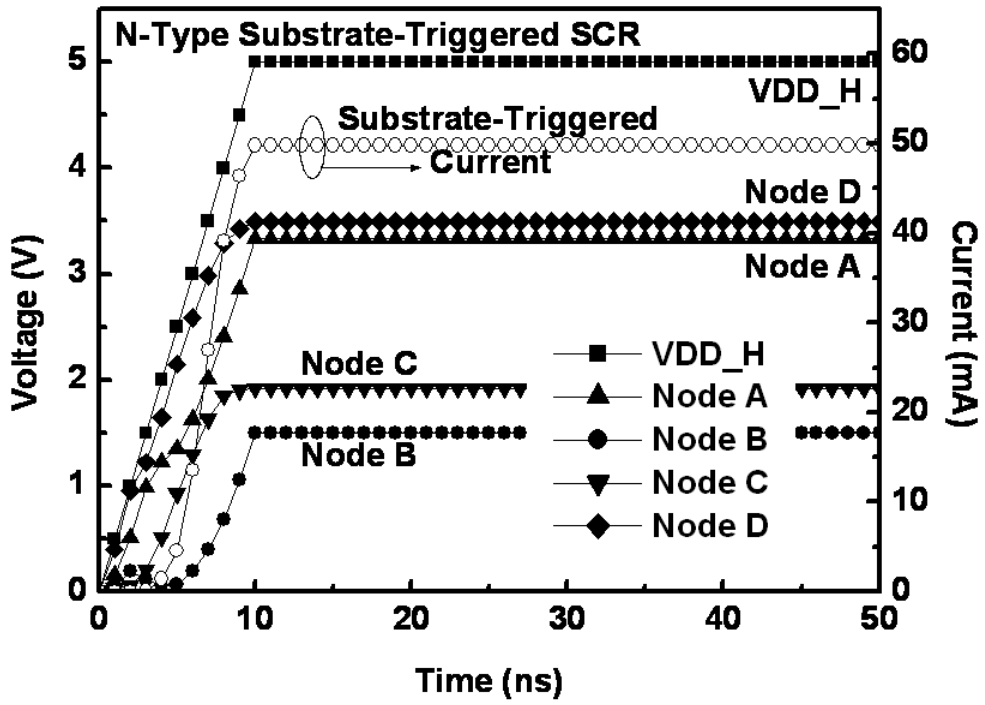


(b)

Fig. 5.24 HSPICE-simulated voltages at the nodes of the ESD-transient detection circuit with (a) the p-type, and (b) the n-type, substrate-triggered SCR devices in 65nm CMOS process under the normal power-on condition with VDD_H of 1.8V and a rise time of 1ms.

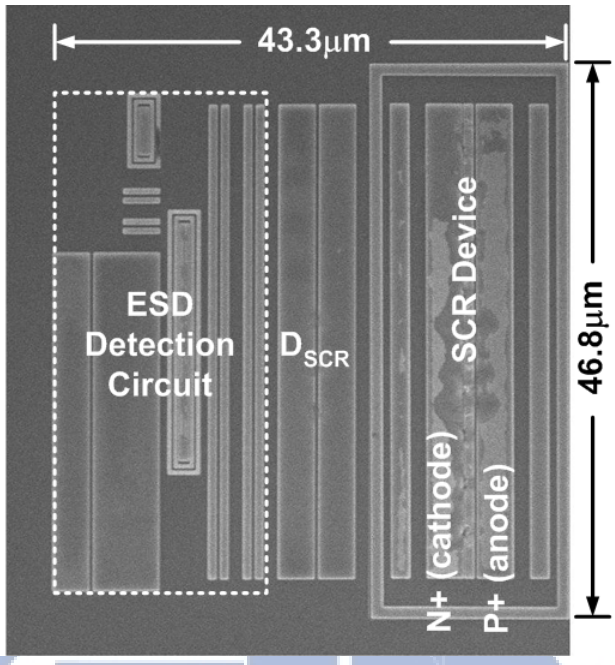


(a)

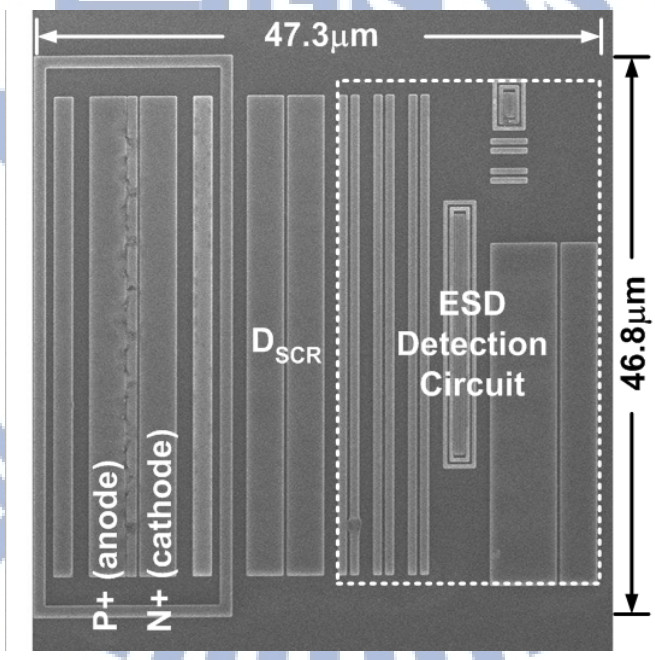


(b)

Fig. 5.25 HSPICE-simulated voltages at all nodes and the trigger current of the ESD-transient detection circuit with (a) the p-type, and (b) the n-type, substrate-triggered SCR devices in 65nm CMOS process under the ESD-like transition condition with VDD_H raising from 0V to 5V and a rise time of 10ns.

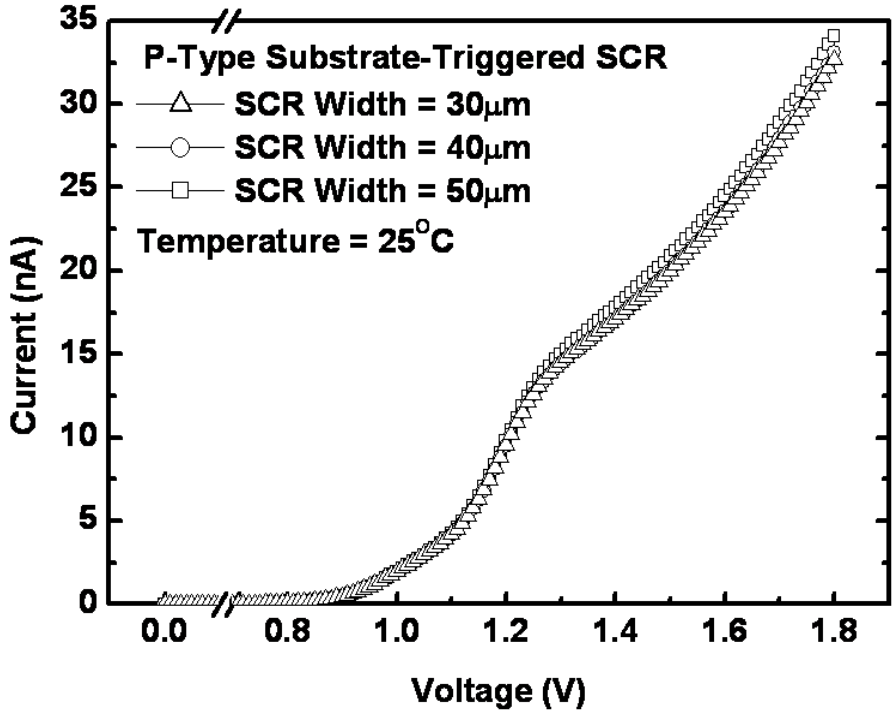


(a)

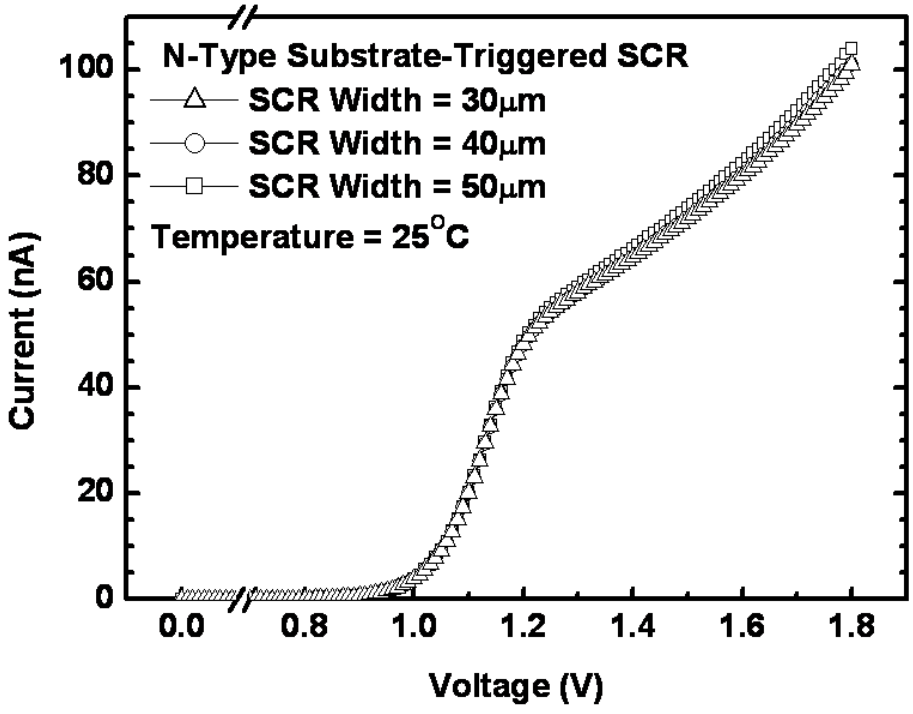


(b)

Fig. 5.26 The proposed 2×VDD-tolerant power-rail ESD clamp circuits with the (a) p-type and the (b) n-type substrate-triggered SCR devices, where the SCR is drawn with a width of 40μm.

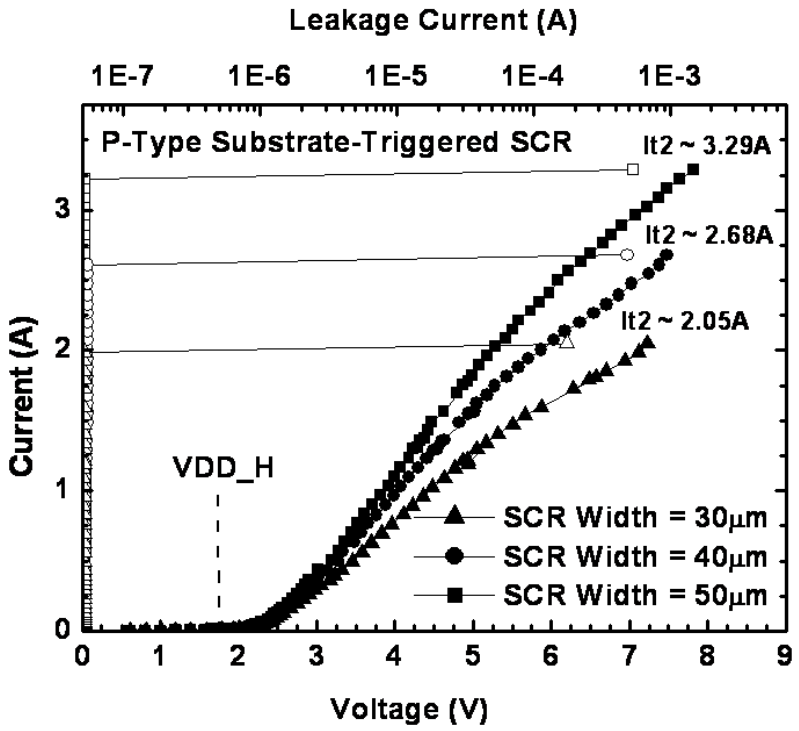


(a)

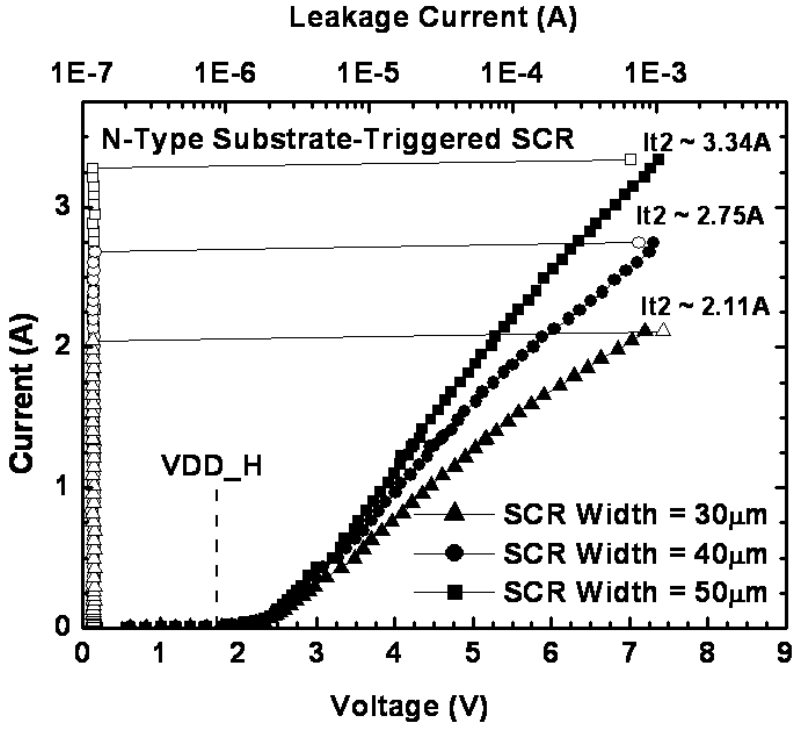


(b)

Fig. 5.27 The measured DC *I-V* curves of the fabricated 2×VDD-tolerant power-rail ESD clamp circuits with (a) the p-type and (b) the n-type substrate-triggered SCR devices in 65nm CMOS process.

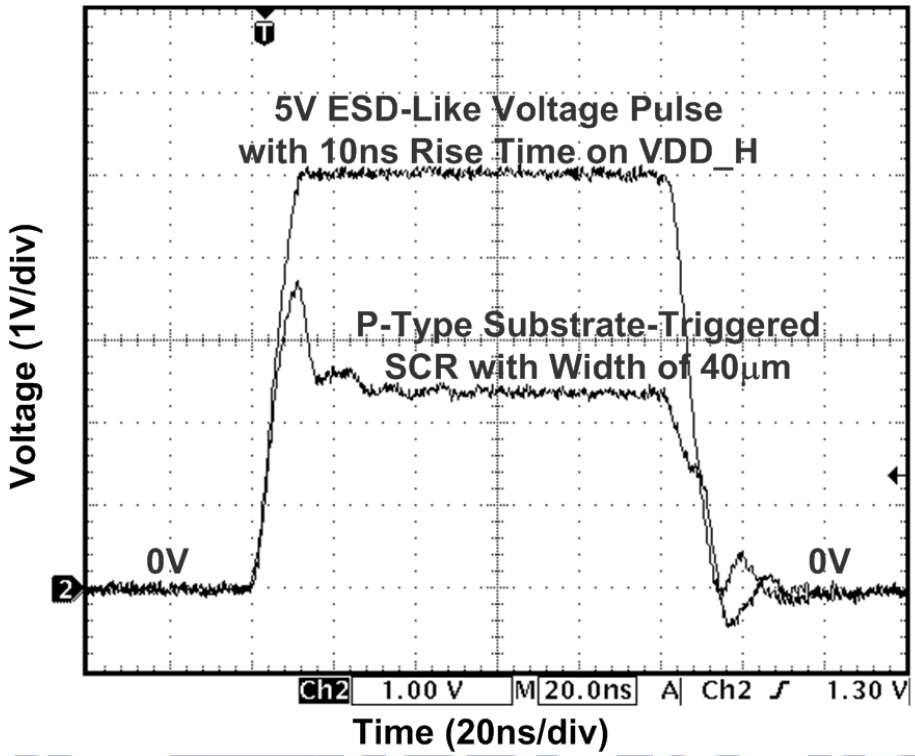


(a)

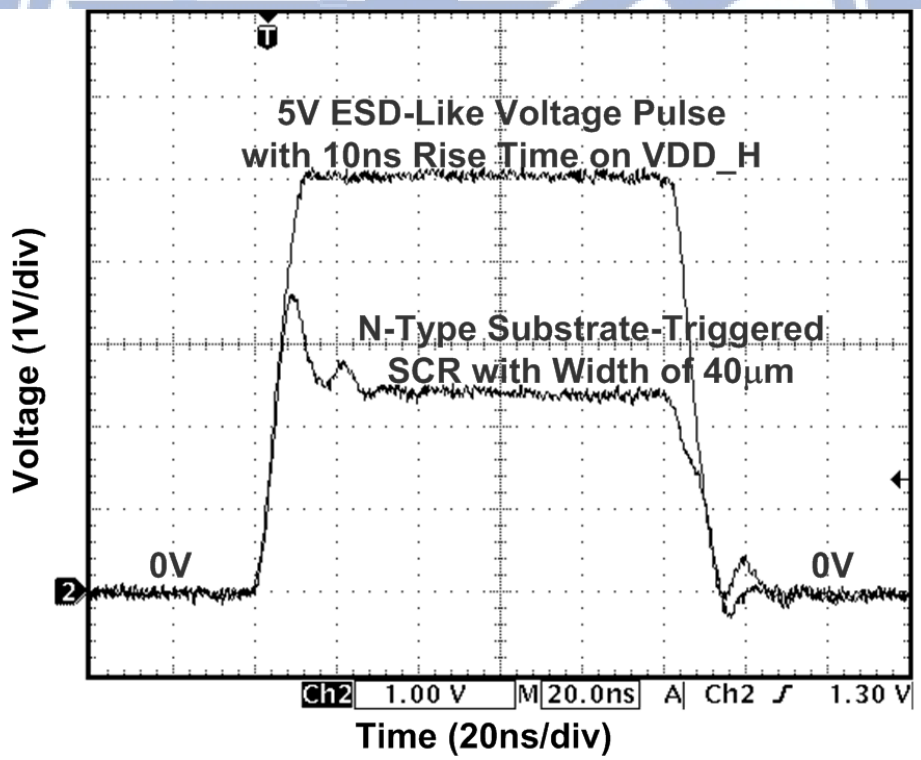


(b)

Fig. 5.28 TLP measured *I-V* curves of the 2×VDD-tolerant power-rail ESD clamp circuit with (a) the p-type and (b) the n-type substrate-triggered SCR devices.



(a)



(b)

Fig. 5.29 Measured voltage waveforms of the fabricated 2×VDD-tolerant ESD clamp circuit with (a) the p-type and (b) the n-type substrate-triggered SCR devices under ESD-like condition with 5V voltage pulse and 10ns rise time.

Chapter 6

Resistor-Less Design of Power-Rail ESD Clamp Circuit

In this chapter, the resistor-less design of power-rail ESD clamp circuit with considerations of gate leakage current and gate oxide reliability are presented. First, the gate leakage current issue in conventional power-rail ESD clamp circuits is discussed in section 6.2. The new proposed resistor-less design of power-rail ESD clamp circuit is investigated in section 6.3. The power-rail ESD clamp circuit with new proposed design was fabricated in a 65nm 1V fully silicided CMOS process.

6.1 Background

In nanoscale CMOS technology, the gate oxide thickness has been scaled down to several nanometers. Such a thin gate oxide causes the gate-tunneling issue more serious [53], [54]. The gate leakage current of MOSFET is directly dependent on the poly-gate area and the gate oxide thickness, which has been investigated and modeled in the BSIM4 MOSFET model [60], [77]. For on-chip ESD protection, the ESD clamp device drawn in the layout style of BigFET had demonstrated excellent ESD protection performance [33]-[38]. However, the ESD clamp device with BigFET layout style is not adequate for low power consumption anymore in the nanoscale CMOS technology because the BigFET of large device dimension with thin gate oxide would lead to intolerable gate leakage current. Therefore, the ESD-transient detection circuit has to be designed with the consideration of gate leakage issue. Recently, the low-leakage power-rail ESD clamp circuit in nanometer CMOS technologies had been revealed [32], [62], [78]. In [32], the gate current was utilized to bias the ESD detection circuit and to reduce the voltage drop across the MOS capacitors. In [62], the ESD detection circuit consisted of the *RC* timer, inverters, and feedback pMOS, where the feedback pMOS used to lower the voltage drop across the *RC* timer and therefore to reduce the gate leakage current of the MOS capacitor. In [78], the *RC*-based ESD detection circuit with the feedback control inverter was used to avoid the direct leakage path through the MOS capacitor. However, those previous circuits were more complicated with large layout area to implement the ESD detection circuits.

6.2 Gate Leakage Current in the Conventional Power-Rail ESD Clamp Circuits

6.2.1 Traditional RC-Based Power-Rail ESD Clamp Circuit

The *RC*-based power-rail ESD clamp circuit was traditionally used to protect the core circuits [8], as shown in the inset of Fig. 6.1. Under the normal circuit operating condition, the MOS capacitor Mc with a large poly-gate area would induce a large gate leakage current from node A to VSS in nanometer CMOS technology. A voltage drop across the resistor R is generated, and therefore the pMOS Mp cannot be completely turned off. The voltage of node B would be elevated to a level higher than VSS due to the non-turned-off pMOS Mp. Finally, the main ESD clamp device (M_{ESD}) drawn with large device dimension operated in the sub-threshold region will further generate a huge leakage current from VDD to VSS under the normal circuit operating condition.

The simulated voltages on the nodes of the traditional *RC*-based power-rail ESD clamp circuit and the gate current of the MOS capacitor Mc under the normal power-on condition with a rise time of 1ms in a 65nm 1V CMOS process are shown in Fig. 6.1. The dimensions of R, Mc, Mp, Mn, and M_{ESD} are 165.3kΩ, 64μm/2μm, 184mμ/60nm, 36μm/60nm, and 2000μm/0.1μm, respectively. In Fig. 6.1, the gate leakage current of Mc is 1.65μA and the voltage of node A is only 0.72V when VDD is raised up to 1V. Therefore, a leakage current path is generated from VDD through the inverter (Mp and Mn) to VSS. Consequently, the main ESD clamp device M_{ESD} operated in the sub-threshold region will contribute another leakage current of 0.98μA under the normal circuit operating condition.

6.2.2 Capacitor-Less Design of Power-Rail ESD Clamp Circuit

The capacitor-less design of power-rail ESD clamp circuit was also proposed to protect the core circuits [47], as shown in the inset of Fig. 6.2. Under the normal circuit operating condition, the ESD clamp device M_{ESD} drawn with large device dimension will induce a large gate current from drain terminal to node B and the sub-threshold channel current in M_{ESD} from drain to source in nanometer CMOS technology. The voltage drop across the resistor Rp can be designed smaller to keep the nMOS Mn in the off state, and therefore the pMOS Mp can be virtually turned off. Consequently, the ESD-transient detection circuit can be almost turned off. However, the M_{ESD} drawn with large device dimension always contributes a large standby leakage current under the normal circuit operating condition.

The simulated voltages on the nodes of the capacitor-less power-rail ESD clamp circuit under the normal power-on condition with a rise time of 1ms in a 65nm 1V CMOS process are shown in Fig. 6.2. The gate and drain currents of M_{ESD} are also shown in Fig. 6.2. The dimensions of Rp, Rn, Mp, Mn, and M_{ESD} are 20kΩ, 40kΩ, 24μm/60nm, 12μm/60nm, and 2000μm/0.1μm, respectively. The P+ junction areas of diode Dn1 and Dn2 are both 0.057μm^2. In Fig. 6.2, the gate current of M_{ESD} is 1.70μA and the voltage of node B is 0.05V when VDD is raised up to 1V. The voltage of node B is not enough to turn Mn on. Therefore, the voltage drop across Rn is only about 2mV, and the ESD-transient detection circuit can be almost turned off. However, there is still a leakage current path from VDD through the M_{ESD} to VSS. As shown in Fig. 6.2, the drain current of M_{ESD} is as large as 9.83μA, which is the major source of the total standby leakage current.

The device dimensions and the total layout areas of the traditional *RC*-based and the capacitor-less power-rail ESD clamp circuits fabricated in a 65nm 1V CMOS process are listed in Table 6.1. The measured standby leakage currents at room temperature are shown in Fig. 6.3. The applied voltage on VDD is from 0V to 1V with the voltage step of 20mV. When VDD is 1V, the measured standby leakage currents of the *RC*-based and the capacitor-less power-rail ESD clamp circuits are 760.42μA and 10.48μA, respectively. The standby leakage currents of the traditional *RC*-based and the capacitor-less power-rail ESD clamp circuits under different temperatures are also listed in Table 6.2. We can observe that MOS transistor drawn with large device dimension as the ESD clamp device would be too leaky in nanometer CMOS technology, which is not suitable for the portable products with the requirement of low power consumption.

6.3 Resistor-Less Design of ESD-Transient Detection Circuit

In this section, a new resistor-less design of ESD-transient detection circuit realized with the gate leakage current is proposed and successfully verified in a 65nm 1V CMOS technology. The proposed ESD-transient detection circuit realized with only core devices can be accurately activated to generate the trigger current to the ESD clamp device. According to the experimentally measured results, the standby leakage current of the proposed power-rail ESD clamp circuit can be significantly reduced to a few nano-ampere under the normal circuit operating condition with 1V bias.

6.3.1 Circuit Schematic

The resistor-less design of power-rail ESD clamp circuit is shown in Fig. 6.4 with the p-type triggered SCR device as the main ESD clamp device. The SCR device [76] adopted as the main ESD clamp device can avoid the gate leakage current issue due to no poly-gate structure inside the SCR device. However, the ESD-transient detection circuit is necessary to enhance the turn-on speed of the SCR device under ESD stress condition. The new proposed ESD-transient detection circuit is designed with considerations of the gate leakage current and the gate oxide reliability. By inserting the diode in the ESD-transient detection circuit, the voltage differences across the gate oxide of the pMOS transistor can be intentionally reduced. By using the gate leakage current of the pMOS transistor, the induced equivalent resistors can be a part of ESD-transient detection mechanism. Therefore, the gate leakage current of the pMOS transistor can be well utilized to achieve the resistor-less design of ESD-transient detection circuit.

The *RC*-based ESD-transient detection mechanism is realized by the equivalent resistors (Rgs and Rgd) of Mp and the junction capacitance of the reverse-biased diode Dc, which can distinguish the ESD stress event from the normal power-on condition. In Fig. 6.4, the pMOS Mp is mainly used to generate the trigger current into the trigger node (node C in Fig. 6.4) of the p-type triggered SCR device during the ESD stress event. Comparing to the thin gate oxide of MOS-capacitor in the traditional *RC* circuit, the Dc used as capacitor in the proposed ESD-transient detection circuit to realize the *RC* time constant can be free from the gate leakage current issue. The inserted diodes, Dp1 and Dp2, in the ESD-transient detection circuit are used to reduce the voltage differences across the gate oxide of Mp. Therefore, the total leakage current and gate oxide reliability of Mp can be safely relieved.

6.3.2 Operation Mechanism

6.3.2.1 Normal Power-On Transition

Under the normal circuit operating condition, the gate voltage of Mp (node A in Fig. 6.4) is biased at VDD through the resistors Rgs and Rgd induced by the gate leakage current. The cathode of Dp2 (node C) is simultaneously biased at VSS through the parasitic p-substrate resistor Rsub in the p-type triggered SCR device. Because Mp is kept off, no trigger current is generated into the trigger node of the p-type triggered SCR device. Inserting two diodes (Dp1 and Dp2) in the ESD-transient detection circuit is to raise up the voltage of node B at the voltage level near to VDD. Therefore, all terminals of Mp are almost at the same voltage level

of VDD to reduce its gate leakage current.

With the SPICE parameters provided from foundry and the device sizes listed in Table 6.3 (adopting Mp width of 140μm), the simulated voltage waveforms and the leakage current of the proposed ESD-transient detection circuit during the normal power-on transition are shown in Fig. 6.5. In Fig. 6.5, the voltage of node A is successfully charged to the voltage level of VDD due to the gate leakage current. Therefore, the Mp is completely turned off and the simulated standby leakage current of the proposed ESD-transient detection circuit is only 1.53nA when VDD is raised up to 1V.

6.3.2.2 ESD Transition

When a positive fast-transient ESD-like voltage is applied to VDD with VSS grounded, the *RC* time delay keeps the node A at a relatively low voltage level as compared with that at VDD. The *RC* time delay is consisted by the equivalent resistors, which are induced by gate leakage currents of Mp, and the reverse-biased diode Dc. Consequently, Mp can be quickly triggered to generate the trigger current into the node C of the p-type triggered SCR device.

In order to simulate the fast transient edge of the HBM ESD event [1] before the breakdown on the internal devices, a 4V voltage pulse with a rise time of 10ns is applied to VDD. The simulated transient voltage and the trigger current of the ESD-transient detection circuit during such an ESD-like transition are illustrated in Fig. 6.6. Mp is successfully turned on to generate the trigger current of ~41mA into the p-type triggered SCR device. Therefore, the SCR device can be fully triggered on to discharge the ESD current from VDD to VSS.

According to the simulated results in Fig. 6.6, the voltages across the source-to-gate and drain-to-gate (ΔVsg and ΔVdg) in time domain are plotted in Fig. 6.7(a). The corresponding gate leakage currents of source-to-gate and drain-to-gate (Isg and Idg) in time domain are drawn in Fig. 6.7(b). The gate leakage currents are in the order of nano-ampere. By using the Ohm's Law, the equivalent resistances (Rgs=ΔVsg/Isg and Rgd=ΔVdg/Idg) can be extracted from the voltage differences and the corresponding gate leakage currents, as shown in Fig. 6.7(c). During the ESD-like transition, the minimum values of Rgs and Rgd are 2.35MΩ and 6.43MΩ, respectively. With these large intrinsic equivalent resistors induced by the gate leakage currents of Mp, the *RC* time delay can be achieved by adopting reverse-biased diode Dc in small size to reduce the layout area of the proposed ESD-transient detection circuit.

6.3.3 Experimental Results

The resistor-less power-rail ESD clamp circuits with different device sizes have been fabricated in a 65nm 1V CMOS process as shown in Fig. 6.8. All devices in the proposed design are 1V fully-silicided devices, including the SCR device. The total layout area of the proposed power-rail ESD clamp circuit with SCR width of 45μm is 21.63×48.60μm^2. The widths of SCR devices are split with 25, 35, and 45μm to verify the corresponding ESD robustness. The gate widths of Mp are split with 35, 70, 140μm to investigate the trigger voltage of the proposed power-rail ESD clamp circuit. These power-rail ESD clamp circuits are prepared for the measurements of DC *I-V*, TLP and ESD test, and transient behavior.

6.3.3.1 TLP Measurement and ESD Robustness

The TLP generator with a pulse width of 100ns and a rise time of ~2ns is used in this measurement [29]. The TLP measured *I-V* curves of the new proposed power-rail ESD clamp circuits with different SCR widths are shown in Fig. 6.9, where the device dimension of Mp is kept at 140μm/0.12μm. The power-rail ESD clamp circuit with SCR widths of 25μm, 35μm, and 45μm can achieve the It2 values of 1.48A, 2.14A, and 2.74A, respectively. The It2 and the trigger voltage of the power-rail ESD clamp circuit with different SCR widths and different Mp widths are listed in Table 6.4. As seen in Table 6.4, the It2 of the proposed power-rail ESD clamp circuit is proportional to the width of SCR device. The trigger voltages of the proposed power-rail ESD clamp circuits are compared in Fig. 6.10. As shown in Fig. 6.10, the trigger voltage can be obviously reduced by increasing the Mp width to generate larger trigger current. In addition, the SCR device with small width also has lower trigger voltage due to larger parasitic p-substrate resistor Rsub. Therefore, the turn-on speed of the SCR device can be properly adjusted by the dimension of Mp. In Fig 6.9, the holding voltages of the SCR devices are ~2V, which is higher than the VDD of 1V under the normal circuit operation conditions. Therefore, the proposed power-rail ESD clamp circuits are free to latchup issue for 1V applications [51], [52].

The measured HBM and MM ESD levels of the proposed power-rail ESD clamp circuit under positive VDD-to-VSS ESD stress are also listed in Table 6.4. The measured HBM (MM) ESD levels of the SCR with the widths of 25, 35, and 45μm are 3, 4, and 5kV (200, 300, and 400V), respectively. The measured HBM and MM ESD levels of the proposed power-rail ESD clamp circuits are also proportional to the width of SCR device.

In nanoscale CMOS process, the application of automotive electronics is increasingly

important for driving safety. In order to meet high reliability need of automotive electronics, typically 8kV HBM ESD level [79], the device width of SCR can be appropriately enlarged. Because the SCR can be uniformly triggered by the trigger current generated from independent ESD-transient detection circuit, the measured It2 and ESD levels as shown in Table 6.4 are well proportional to the SCR width. Therefore, the proposed power-rail ESD clamp circuit with enlarged SCR device width can sustain high enough HBM ESD level to meet the application requirement of automotive electronics.

6.3.3.2 Standby Leakage Current

The DC *I-V* curves of the fabricated power-rail ESD clamp circuits are measured by HP4155 from 0V to 1V with the voltage step of 20mV at 25°C, as shown in Fig. 6.11 and listed in Table 6.4. In Fig. 6.11, the standby leakage current of the power-rail ESD clamp circuit with SCR width of 45μm increases from 1.13nA to 1.43nA under 1V bias when the width of Mp increases from 35μm to 140μm. In Table 6.4, the standby leakage currents of the power-rail ESD clamp circuits with SCR widths of 25, 35, and 45μm are similar, because the leakage current in the SCR device is quite small. The measured standby leakage currents of the fabricated power-rail ESD clamp circuits under 1V bias at 50°C and 100°C are also listed in Table 6.4. The standby leakage currents of the fabricated power-rail ESD clamp circuits are reduced to the order of nano-ampere because the voltage drop across the gate oxide of Mp is significantly reduced by inserting the reverse-biased diode Dc and the diodes (Dp1 and Dp2) in the ESD-transient detection circuit. Although increasing the width of Mp causes a slightly increased standby leakage current under the normal circuit operating condition, it can increase the trigger current to improve the turn-on speed of the SCR device with a reduced trigger voltage (as shown in Fig. 6.10).

6.3.3.3 Turn-On Verification

For normal power-on condition, the voltage pulse usually has a rise time in the order of milliseconds. As shown in Fig. 6.12(a), the measured voltage on VDD power line rises up to 1V and the measured current is near zero. However, some previous studies [36], [46] have demonstrated that the power-rail ESD clamp circuits with *RC*-based ESD detection circuits were easily mis-triggered or into the latch-on state under the fast power-on condition. The new proposed power-rail ESD clamp circuits have been applied with 1V voltage pulse with 20ns rise time to investigate the immunity against mis-trigger, as shown in Fig. 6.12(b). The

measured voltage on VDD power line is not degraded under the fast power-on condition. The measured current waveform is also smooth at the level near zero. The inserted two diodes (Dp1 and Dp2) in ESD detection circuit can ensure that there would not be any on-current flowing through themselves from VDD to VSS. Therefore, the resistor-less power-rail ESD clamp circuit is free from the transient-induced latch-on or mis-trigger issues.

The transient voltage with a pulse height of 4V and a rise time of 10ns is applied to the VDD power line with 1V operation voltage to verify any latch-on issue. As shown in Fig. 6.13, the transient voltage pulse will activate the ESD-transient detection circuit to generate the trigger current of ~14mA. The applied 4V voltage pulse is clamped down to a lower voltage level of ~3.3V by the proposed power-rail ESD clamp circuit. After the transient, the voltage on VDD power line is back to 1V operation voltage and the current is almost zero.

In order to observe the transient behavior of the proposed ESD-transient detection circuit, a TLP voltage pulse with a rise time of ~2ns and a pulse height of 4V is applied to the VDD power line with the VSS grounded. The TLP voltage pulse will initiate the ESD-transient detection circuit to generate the trigger current to trigger on the SCR device. The measured voltage and current waveforms in time domain on VDD power line under 4V voltage pulse are shown in Fig. 6.14. The applied 4V voltage pulse can be quickly clamped down to a lower voltage level of ~3.0V by the proposed ESD-transient detection circuit with the trigger current of ~20mA. When the TLP voltage pulse height is increased, the proposed ESD-transient detection circuit can generate more trigger current into the SCR device. The triggered-on SCR device can provide a low impedance path from VDD to VSS to discharge ESD current and clamp down the voltage level. Overall, the proposed ESD-transient detection circuit can be successfully activated by the fast-transient voltage pulse to trigger on the SCR device.

6.4 Summary

Resistor-less design of ESD-transient detection circuit to achieve ultra-low standby leakage current and small layout area has been proposed and successfully verified in a 65nm 1V fully-silicided CMOS technology. The proposed ESD-transient detection circuit is realized with only 1V devices without suffering the gate leakage issue. According to the measured results, the proposed power-rail ESD clamp circuit demonstrates an ultra-low standby leakage current of only 1.43nA under 1V bias at 25^{o}C, where the device dimension of Mp is drawn as 140μm/0.12μm. Moreover, the proposed power-rail ESD clamp circuit has excellent immunity against the transient-induced latch-on or mis-trigger issues. The proposed

resistor-less power-rail ESD clamp circuit is an excellent circuit solution to achieve effective and efficient on-chip ESD protection in advanced nanoscale CMOS technologies.

Table 6.1

Device Dimensions of the Conventional Power-Rail ESD Clamp Circuits

Device	Traditional RC-Based Power-Rail ESD Clamp Circuit	Capacitor-Less Design of Power-Rail ESD Clamp Circuit [47]
Capacitor (Mc)	64μm / 2μm (W/L)	none
Resistor (Ω)	R = 165.3k	Rn = 40k ; Rp = 20k
PMOS Transistor (Mp)	184μm / 60nm	24μm / 60nm
NMOS Transistor (Mn)	36μm / 60nm	12μm / 60nm
ESD Clamp NMOS Transistor (M_{ESD})	2000μm / 100nm	2000μm / 100nm
Diodes (Dn1 and Dn2)	none	0.057μm^2

Table 6.2

Leakage Currents of the Conventional Power-Rail ESD Clamp Circuits under Different Temperatures at 1V in a 65nm CMOS Process

Standby Leakage Current at 1V Normal Operating Voltage	Traditional RC-Based Power-Rail ESD Clamp Circuit	Capacitor-Less Design of Power-Rail ESD Clamp Circuit [47]
25°C	760.42μA	10.48μA
50°C	12.62mA	32.24μA
100°C	85.02mA	360.48μA

Table 6.3

Design Parameters of the Resistor-Less Design of Power-Rail ESD Clamp Circuit

Device	Size								
Dp1 and Dp2 (μm^2)	14								
Dc (μm^2)	52.13			54.79			60.13		
Mp Width (μm)	35			70			140		
SCR Width (μm)	25	35	45	25	35	45	25	35	45

Table 6.4

Measured Results of the Resistor-Less Design of Power-Rail ESD Clamp Circuits

Mp Width (μm)		35			70			140		
SCR Width (μm)		25	35	45	25	35	45	25	35	45
It2		1.48A	2.17A	2.74A	1.48A	2.11A	2.71A	1.48A	2.14A	2.74A
Trigger Voltage		4.26V	4.71V	5.17V	3.79V	4.02V	4.26V	3.60V	3.75V	3.86V
HBM ESD Level		3kV	4kV	5kV	3kV	4kV	5kV	3kV	4kV	5kV
MM ESD Level		200V	300V	400V	200V	300V	400V	200V	300V	400V
Leakage Current (@ 1V)	25°C	1.12nA	1.12nA	1.13nA	1.31nA	1.31nA	1.32nA	1.43nA	1.43nA	1.43nA
	50°C	6.69nA	6.80nA	6.84nA	8.18nA	8.48nA	8.65nA	12.13nA	12.55nA	12.62nA
	100°C	0.19μA	0.19μA	0.19μA	0.26μA	0.26μA	0.26μA	0.33μA	0.33μA	0.33μA

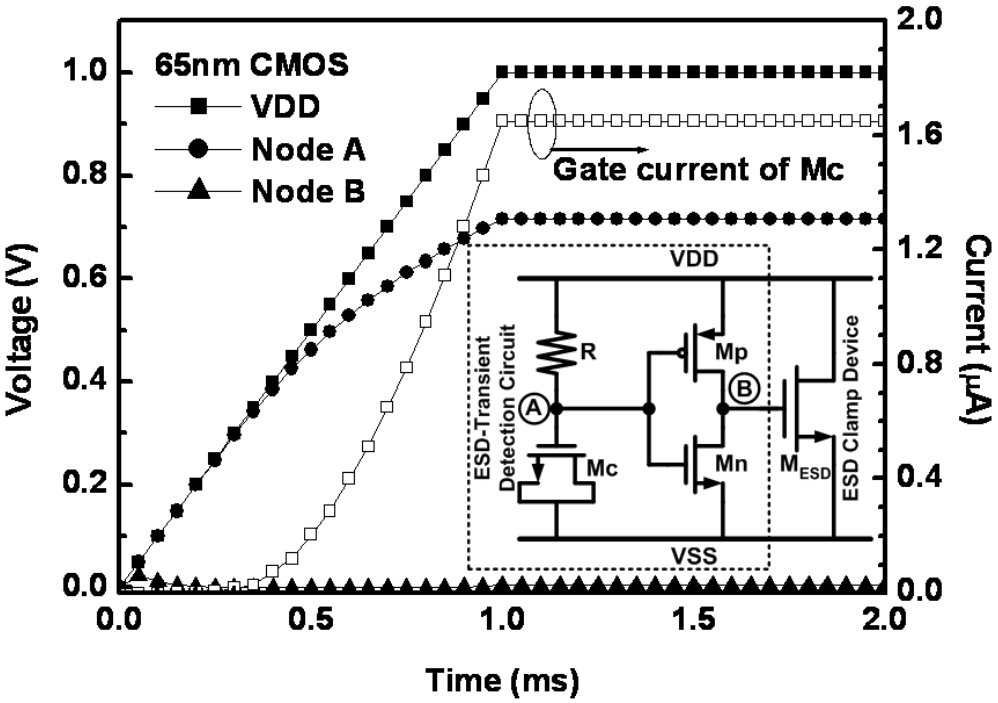


Fig. 6.1 The simulated voltages on the nodes of the traditional *RC*-based power-rail ESD clamp circuit [8] and the gate current flowing through the MOS capacitor Mc under the normal power-on condition with a rise time of 1ms in a 65nm CMOS process.

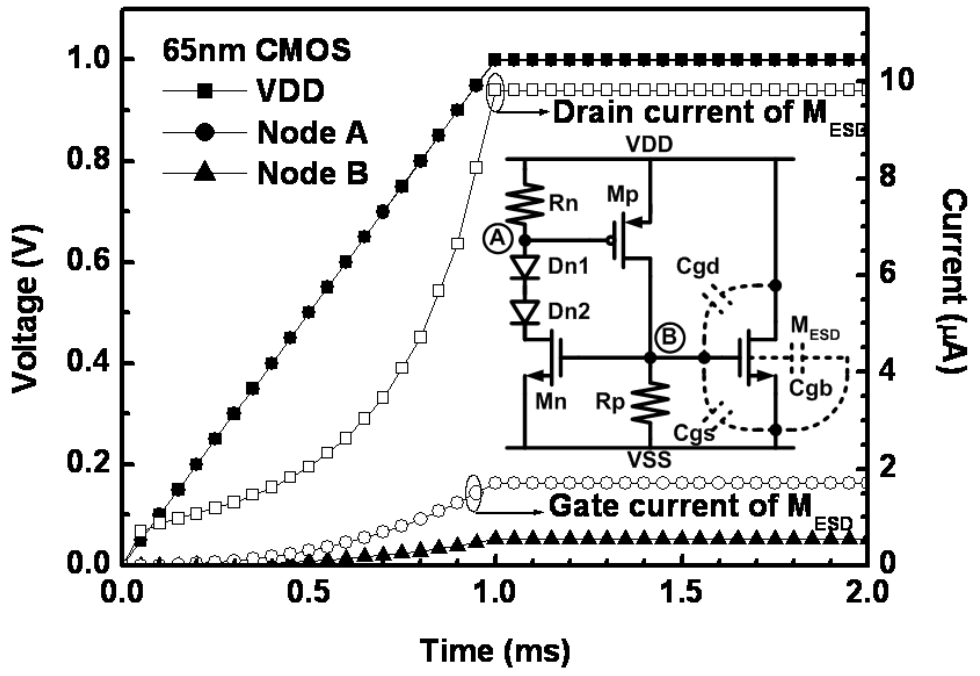


Fig. 6.2 The simulated voltages on the nodes of the capacitor-less power-rail ESD clamp circuit [47], the drain current, and the gate current flowing through the ESD clamp device M_{ESD} under the normal power-on transition.

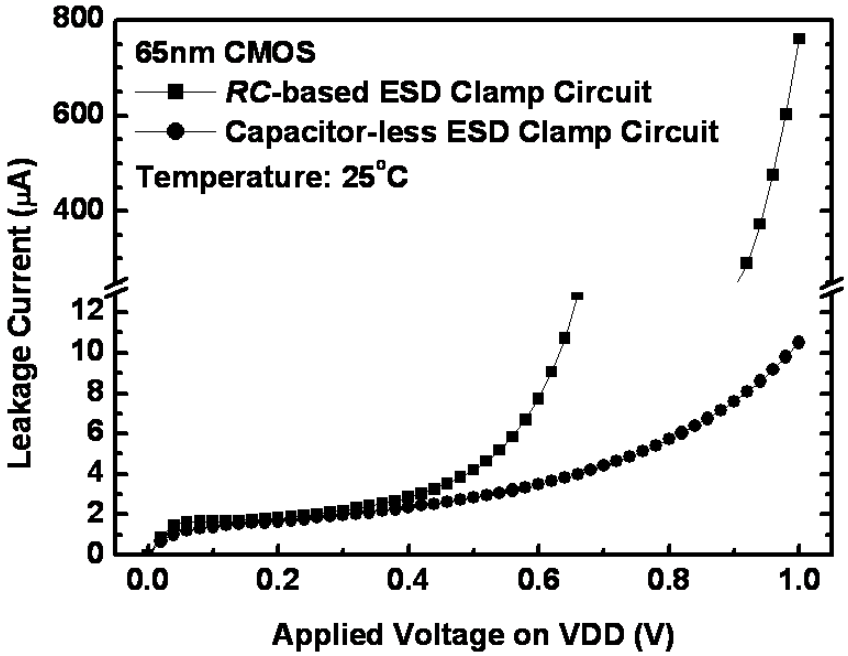


Fig. 6.3 The measured standby leakage currents of the traditional *RC*-based and the capacitor-less power-rail ESD clamp circuits.

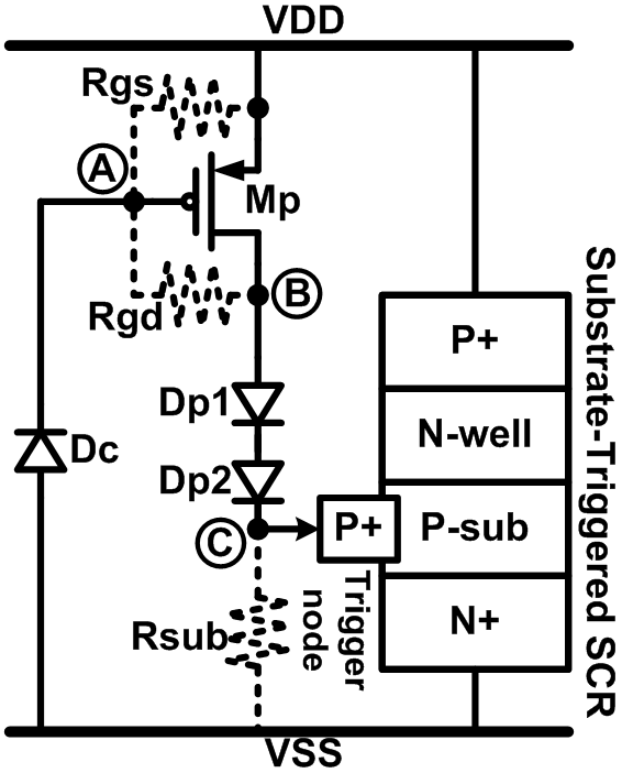


Fig. 6.4 The proposed resistor-less ESD detection circuit with the p-type substrate-triggered SCR device as the ESD clamp device.

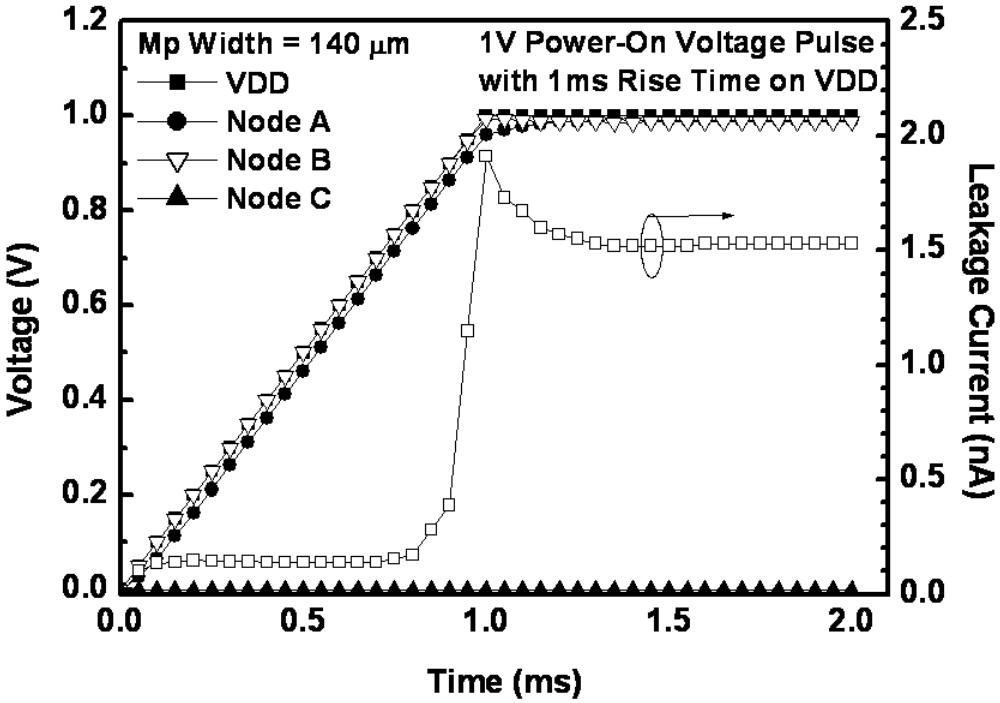


Fig. 6.5 Simulated voltage waveforms on the nodes and the leakage current of the proposed ESD-transient detection circuit under the normal power-on transition with VDD of 1V and a rise time of 1ms in 65nm 1V CMOS process.

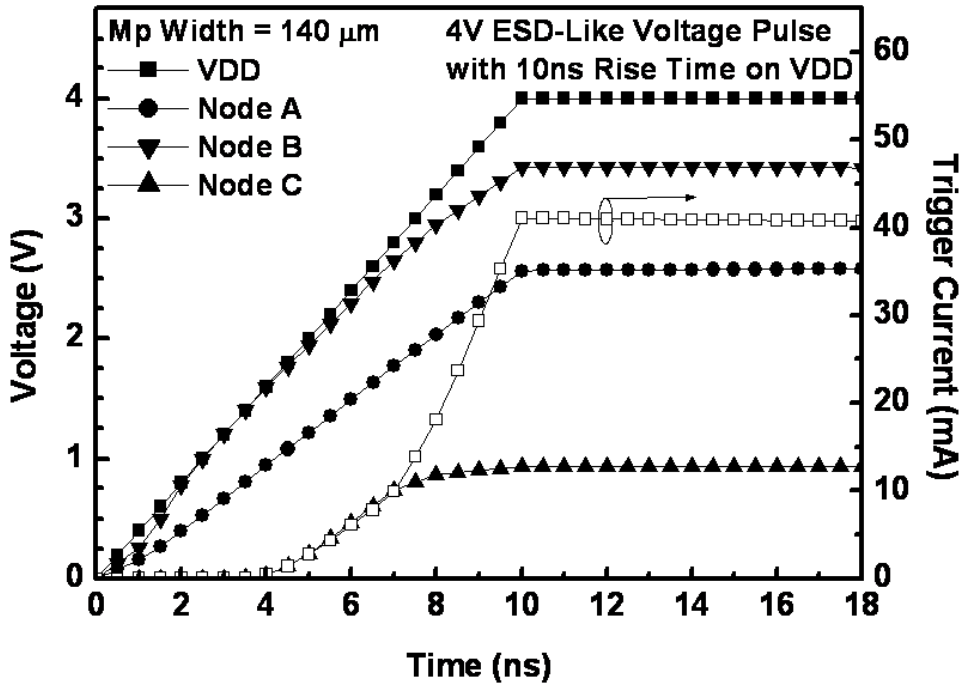
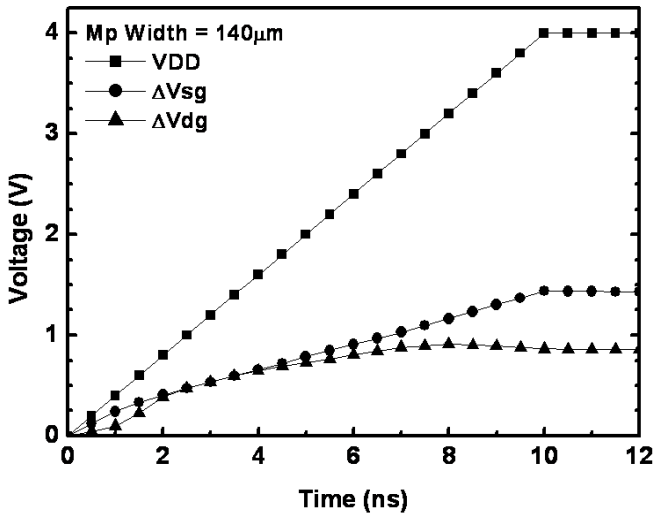
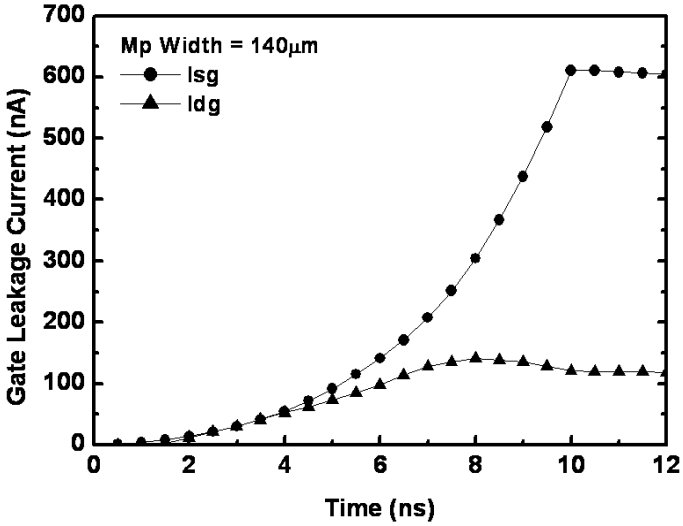


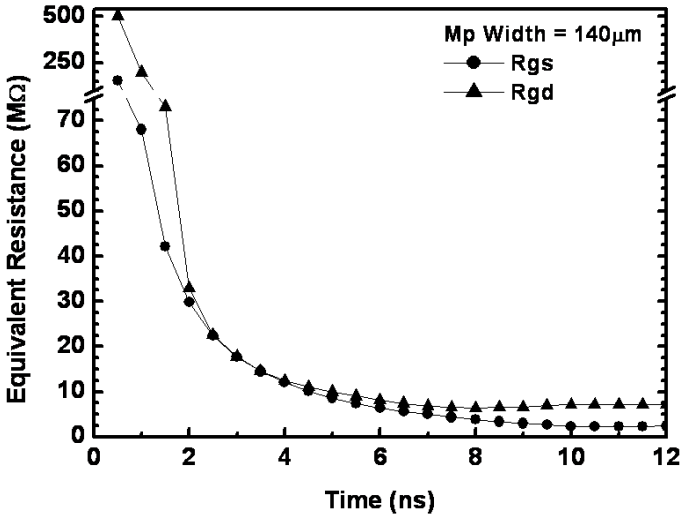
Fig. 6.6 Simulated voltage waveforms on the nodes and the trigger current of the proposed ESD-transient detection circuit under the ESD-like transition with VDD of 4V and a rise time of 10ns in 65nm 1V CMOS process.



(a)



(b)



(c)

Fig. 6.7 Simulated values of (a) ΔVsg, ΔVdg, (b) Isg, Idg, and (c) the extracted equivalent resistances of Rgs and Rgd under the ESD-like transition.

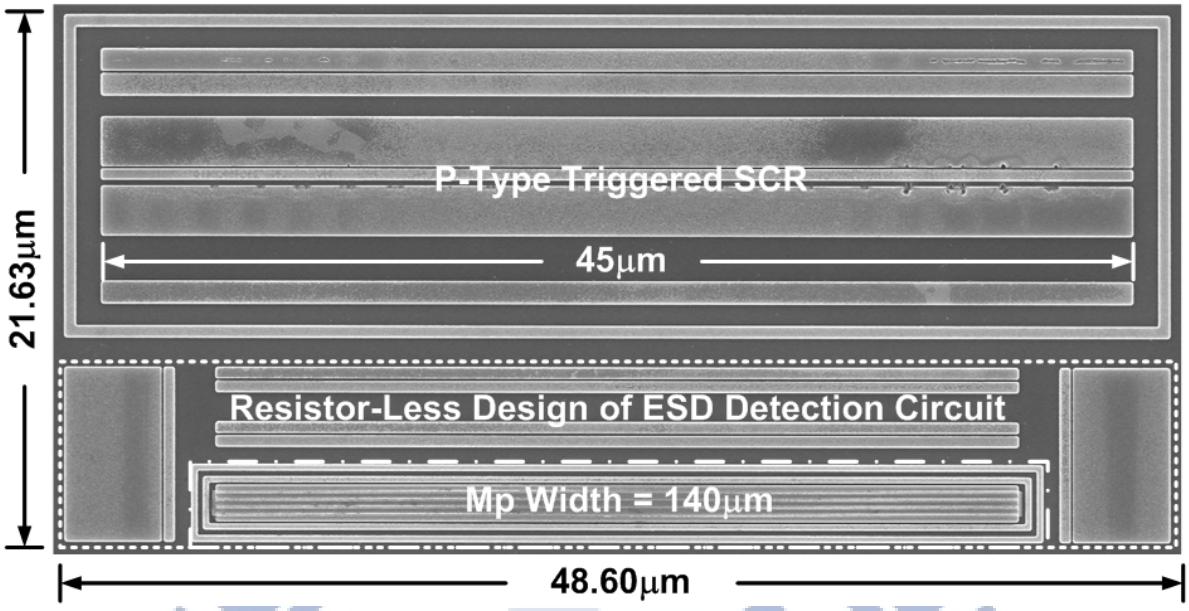


Fig. 6.8 Chip microphotograph of the fabricated power-rail ESD clamp circuit realized with the resistor-less design of ESD-transient detection circuit.

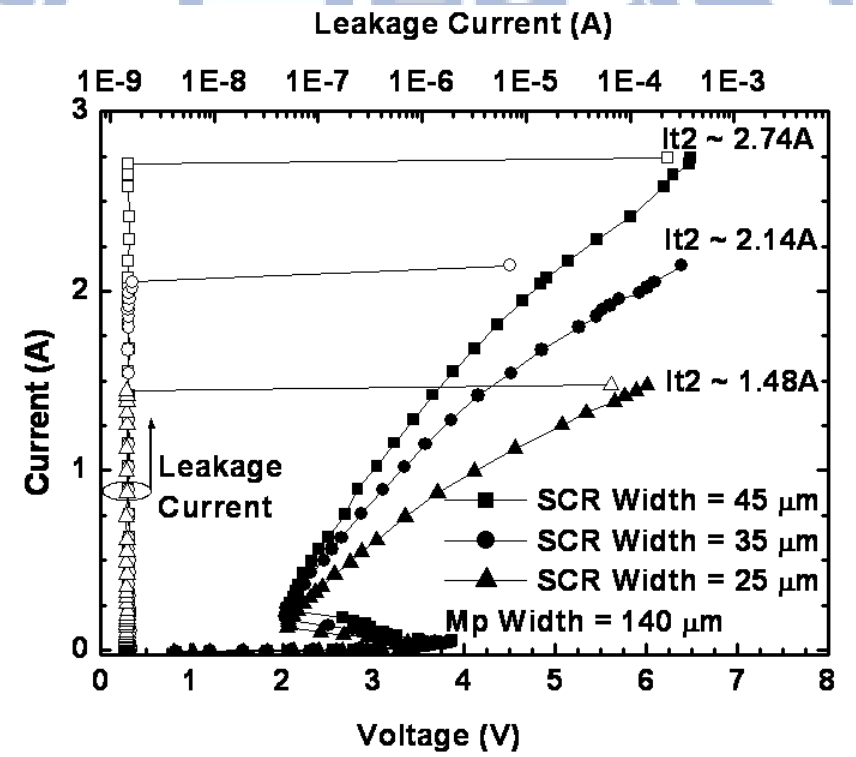


Fig. 6.9 TLP measured *I-V* curves of the power-rail ESD clamp circuits with the resistor-less design of ESD detection circuit.

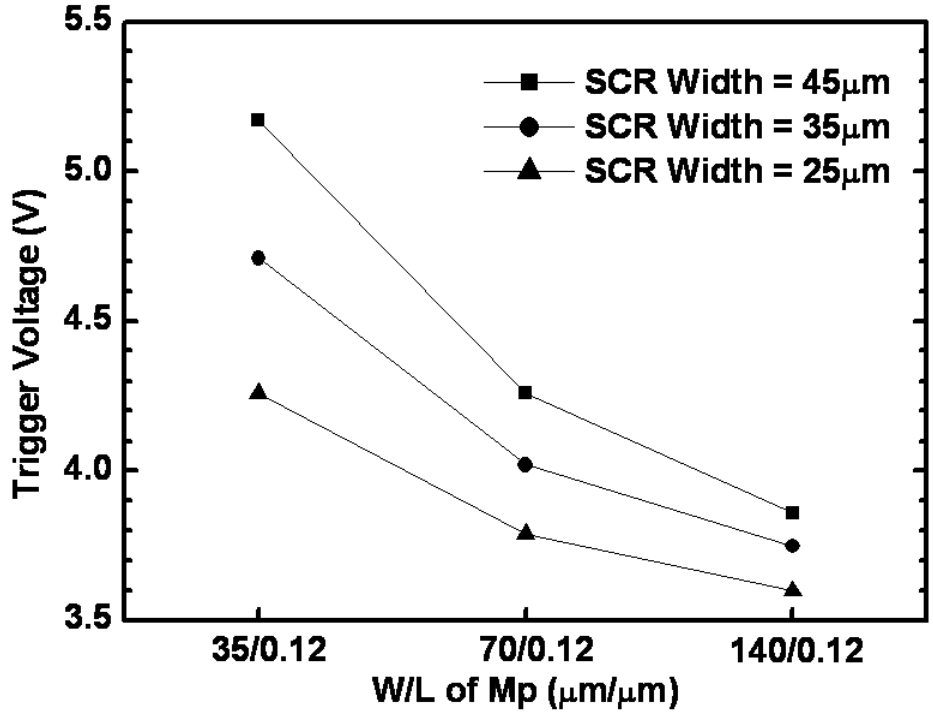


Fig. 6.10 The dependence of the TLP measured trigger voltages on the device dimension of Mp.

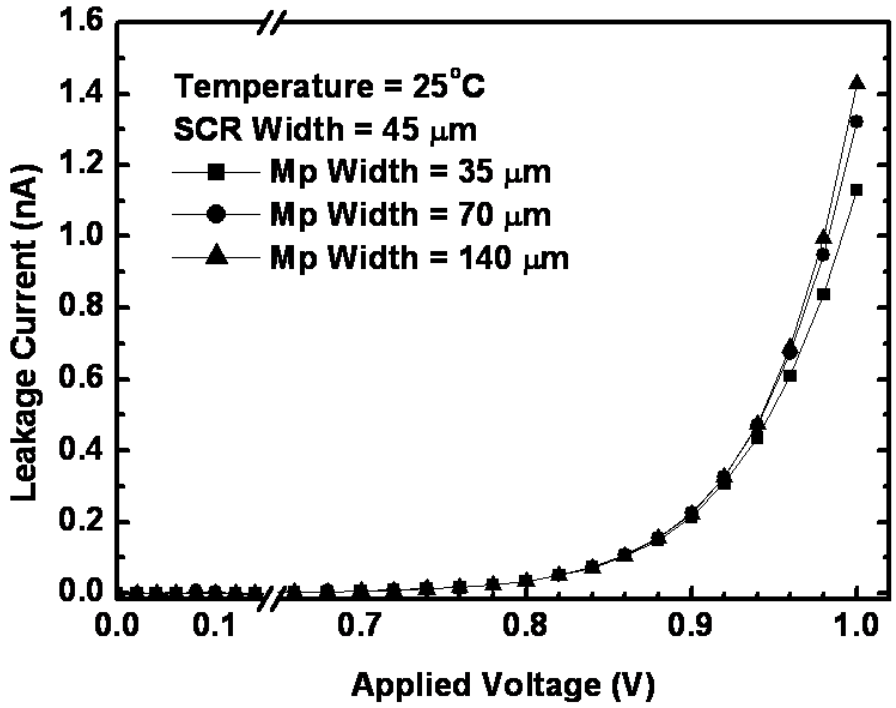
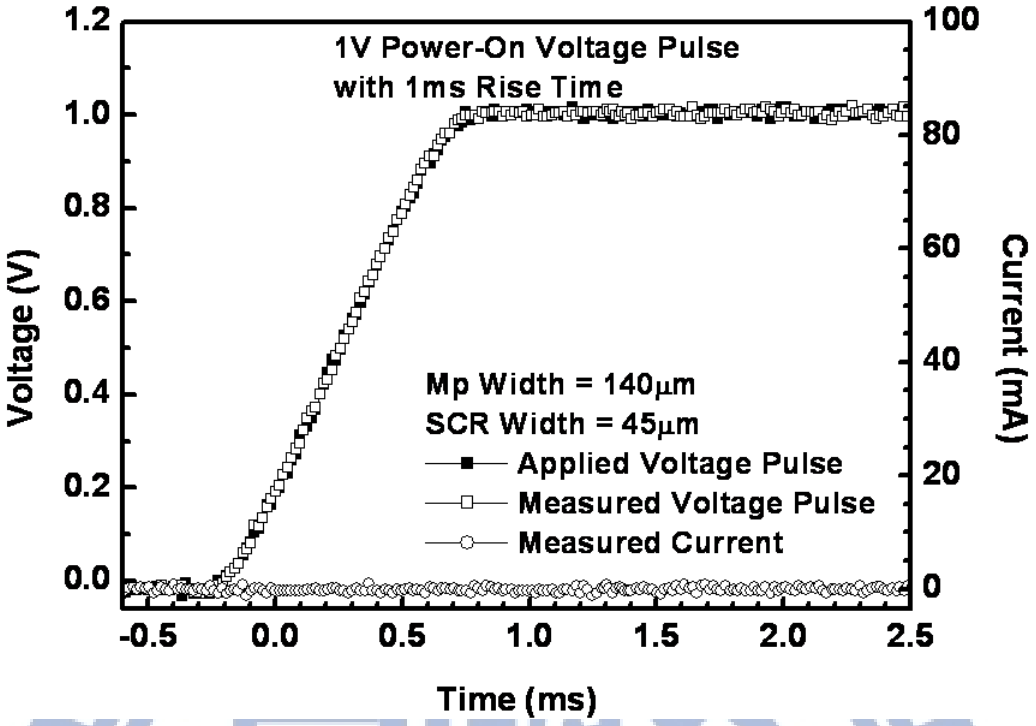
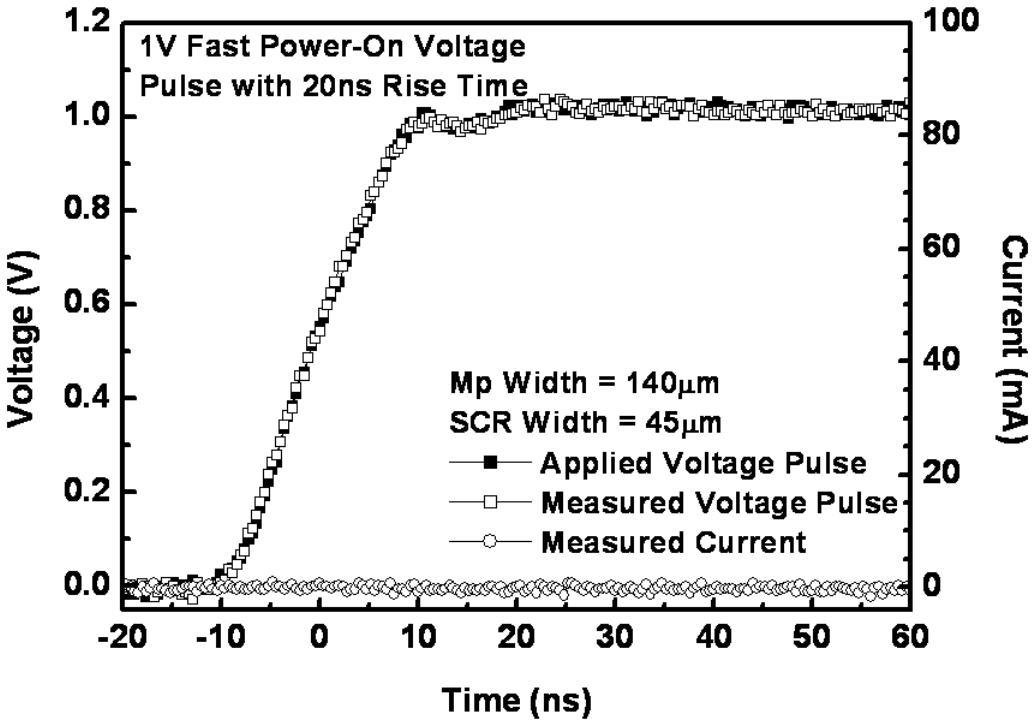


Fig. 6.11 The measured DC *I-V* curves of the fabricated resistor-less power-rail ESD clamp circuits with different widths of Mp at room temperature.



(a)



(b)

Fig. 6.12 The measured voltage and current waveforms of the fabricated resistor-less power-rail ESD clamp circuit under the 1V power-on transitions with the rise time of (a) 1ms and (b) 20ns.

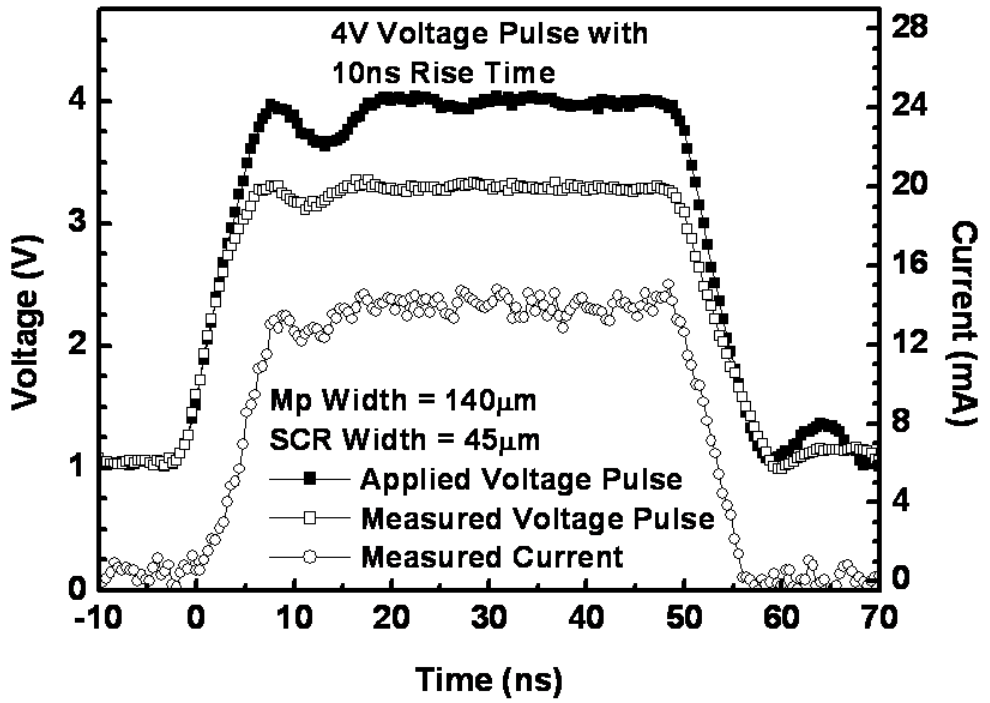


Fig. 6.13 Measured voltage and current waveforms of the resistor-less power-rail ESD clamp circuit under transient noise condition.

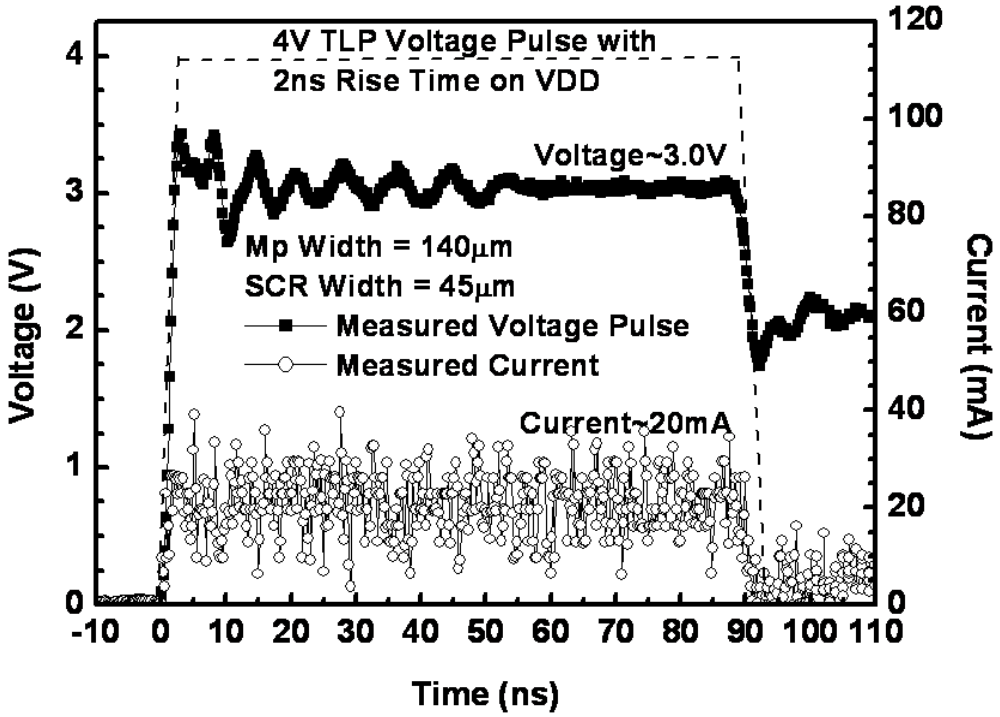


Fig. 6.14 Measured voltage and current waveforms of the resistor-less power-rail ESD clamp circuit under TLP transition with 4V voltage pulse.

Chapter 7

Conclusions and Future Works

This chapter summarizes the main results and contributions of this dissertation. Future works for the fields of power-rail ESD clamp circuits for whole-chip ESD protection design in fully silicided CMOS process are also provided in this chapter.

7.1 Main Contributions of This Dissertation

In this dissertation, many novel power-rail ESD clamp circuits and ESD protection diodes have been developed in nanoscale CMOS technology for whole-chip ESD protection design. Each of the ESD protection circuits has been successfully verified in the test chips. The contributions of each chapter in this dissertation are presented in the following.

In Chapter 2, the new proposed diodes with octagon, waffle-hollow, octagon-hollow, multi-waffle, and multi-waffle-hollow layout styles have been demonstrated. The new proposed diodes in large size can avoid the penalty of local heat distribution. The reduction of junction area by using new modified layout styles is the key factor to significantly improve the FOMs of the ESD diodes. As compared to the FOMs of waffle diodes, it reveals that the FOMs values of the large size diodes can be enhanced by modifying the layout styles. Therefore, the diodes with proposed layout styles are adequate to be implemented to high-speed I/O applications with small layout area.

In Chapter 3, the capacitor-less power-rail ESD clamp circuits with adjustable holding voltage have been proposed and successfully verified in a 65nm 1.2V CMOS technology. The new proposed ESD-transient detection circuit adopts the capacitance-coupling mechanism to command the ESD clamp nMOS or pMOS transistors. According to the measured results, the capacitor-less power-rail ESD clamp circuits with adjustable holding voltage demonstrate excellent immunity against mis-trigger under the fast power-on condition, and also perform no latch-on issue under power noise and TLU measurement. Moreover, the new proposed capacitor-less ESD-transient detection circuits are also area-efficient, which save layout area by more than 54.5% compared with the traditional *RC*-based ESD-transient detection circuit. For the proposed power-rail ESD clamp circuit with ESD clamp pMOS transistor, it is also

efficient in standby leakage to save leakage current by more than 80.4%, compared with the traditional *RC*-based ESD-transient detection circuit.

In Chapter 4, the new proposed ESD-transient detection circuits with equivalent capacitance-coupling and equivalent *RC*-based ESD-transient detection mechanisms have been proposed and successfully verified in a 65nm 1.2V CMOS technology. According to the measured results, the proposed power-rail ESD clamp circuit has good ESD robustness and excellent immunity against the transient-induced latch-on or mis-trigger issues and good proportionality between the width of ESD clamp device and the ESD robustness. Moreover, the proposed ESD-transient detection circuit saves the layout area by ~82% compared with the traditional *RC*-based ESD-transient detection circuit. The new proposed power-rail ESD clamp circuit is an excellent circuit solution to achieve effective and efficient on-chip ESD protection in advanced nanoscale CMOS technologies.

In Chapter 5, new design of power-rail ESD clamp circuit to achieve low standby leakage current and area efficiency has been proposed and successfully verified in a 65nm 1V fully-silicided CMOS technology. The new proposed ESD-transient detection circuit is realized with only 1V devices without suffering the gate leakage issue. According to the measured results, the proposed power-rail ESD clamp circuit with the consideration of gate leakage current demonstrates a low standby leakage current of only 16.4nA under 1V bias at 25^{o}C. In addition, the power-rail ESD clamp circuit with embedded ESD-transient detection circuit can save over 16% layout area with better ESD discharging capabilities of It2, HBM, and MM ESD levels, which are 1.6 times the values of p-type triggered design. Overall, the proposed power-rail ESD clamp circuit performs excellent turn-on efficiency due to low trigger voltage. The proposed power-rail ESD clamp circuit with low standby leakage current and high area efficiency is an excellent on-chip ESD protection solution in advanced nanoscale CMOS technologies without latchup issue. Another designs of 2×VDD-tolerant power-rail ESD clamp circuits with low standby leakage current have also been proposed and successfully verified in a 65nm 1V fully-silicided CMOS technology. The new proposed ESD-transient detection circuit is realized with only 1V devices without suffering the gate oxide reliability issue under 1.8V (2×VDD) applications. According to the measured results, the proposed 2×VDD-tolerant power-rail ESD clamp circuits with the consideration of gate leakage current demonstrate a very small standby leakage current in the order of nano-ampere under 1.8V bias at 25^{o}C. Moreover, the proposed power-rail ESD clamp circuits also perform excellent turn-on efficiency. The new proposed 2×VDD-tolerant power-rail ESD clamp circuit

with low standby leakage current is a superior design technique for on-chip ESD protection in the mixed-voltage I/O interfaces.

In Chapter 6, resistor-less design of ESD-transient detection circuit to achieve ultra-low standby leakage current and small layout area has been proposed and successfully verified in a 1V 65nm fully-silicided CMOS technology. The proposed ESD-transient detection circuit is realized with only 1V devices without suffering the gate leakage issue. According to the measured results, the proposed power-rail ESD clamp circuit demonstrates an ultra-low standby leakage current of only 1.43nA under 1V bias at 25^{o}C, where the device dimension of Mp is drawn as 140μm/0.12μm. Moreover, the proposed power-rail ESD clamp circuit has excellent immunity against the transient-induced latch-on or mis-trigger issues. The proposed resistor-less power-rail ESD clamp circuit is an excellent circuit solution to achieve effective and efficient on-chip ESD protection in advanced nanoscale CMOS technologies.

Overall, the comparisons of several circuit characteristics are listed in Table 7.1 for 65nm LP 1.2V CMOS process and in Table 7.2 for 65nm GP 1V CMOS process. In Table 7.1, the capacitor-less design and equivalent ESD-transient detection mechanism design are compared with traditional *RC*-based design [8] and small capacitance design [36]. The proposed designs have advantages of layout area and leakage current. In addition, the proposed designs also have the feature of adjustable holding voltage to avoid mis-trigger and transient-induced latch-on issues. In Table 7.2, the embedded SCR design and resistor-less design are compared with the prior arts [32], [78]. Because there is a serious gate leakage issue in 65nm GP 1V CMOS process, the ESD clamp devices in all discussed circuits are substrate-triggered SCR. As long as the holding voltage of SCR is higher than the normal circuit operation voltage VDD, all circuits would not suffer from mis-trigger and transient-induced latchup issues. However, the new proposed designs still have advantages of ESD robustness improvement and leakage current.

7.2 Future Works

With the continuously scaling CMOS technology, the thickness of gate oxide layer becomes thinner and thinner. The gate leakage current will absolutely be a serious issue for the hand-held and portable electronic products, which highly require low power consumption. In addition, the power-rail ESD clamp circuit is a key element for whole-chip ESD protection design during the ESD stresses. However, the power-rail ESD clamp circuit should not be activated during normal circuit operating condition. Therefore, the design of power-rail ESD

clamp circuit with low standby leakage current in advanced nanoscale CMOS process is still a continuously interesting research topic to be focused. In this field, the gate leakage current of MOSFET and gate oxide reliability must be considered carefully during the design phase.

In advanced CMOS technology below 40nm, there are some structures presented, such as high-K/metal gate and FinFET, to solve gate leakage issue and improve the control capability of gate electrode. However, the ESD design issues of such a novel process are still largely unknown and need to be solved urgently.

For SoC applications, the power supply voltage may exceed the original VDD of the process to drive a high-voltage output signal. Therefore, it is required to design the high-voltage-tolerant power-rail ESD clamp circuit with low-voltage devices but without suffering the gate leakage current and gate oxide reliability issues. In this field, the standby leakage current of the high-voltage-tolerant power-rail ESD clamp circuit is an important concern, especially when the IC is operated at high temperature condition.

In addition, the fabrication cost per layout area of ICs is incredibly increasing with the scaling CMOS technology. The power-rail ESD clamp circuit with small layout area is another continuous research topic to be achieved. Particularly, the small layout area design is very suitable to pre-bonding functional test of 3D IC. During the fabrication of 3D IC, every tier needs to do functional test before stacking. Therefore, there is a high risk to damage the core circuit in the specific tier during functional test. Consequently, the basic ESD protection design is necessary to provide ESD protection at every probing pad. However, those ESD protection circuit in the tier will not be used anymore when the 3D IC is completely stacked. As a result, the requirements of ESD protection design for pre-bonding pad in 3D IC are small layout area and high enough ESD robustness.

Table 7.1

Comparison on Circuit Characteristics in 65nm LP 1.2V CMOS Process

65nm LP 1.2V CMOS Process				
Power-Rail ESD Clamp Circuit	Traditional *RC*-Based [8]	Smaller Capacitance [36]	Capacitor-Less Design	Equivalent ESD Detection Mechanism
Layout Area	★☆☆☆☆	★★☆☆☆	★★★☆☆	★★★★★
Leakage	★☆☆☆☆	★☆☆☆☆	★★★★☆	★★★☆☆
ESD Levels	★★★★☆	★★★★☆	★★★★☆	★★★★☆
Mis-trigger	YES	NO	NO	NO

Table 7.2

Comparison on Circuit Characteristics in 65nm GP 1V CMOS Process

65nm GP 1V CMOS Process				
Power-Rail ESD Clamp Circuit	Prior Art [32]	Prior Art [78]	Embedded SCR Design	Resistor-Less Design
Layout Area	★★★★★	★★★☆☆	★★★★☆	★★★★★
Leakage	★★★☆☆	★★★☆☆	★★★☆☆	★★★★★
ESD Levels	★★★★☆	★★★★☆	★★★★★	★★★★☆
Mis-trigger	NO	NO	NO	NO

E
S
A
1896

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Design and Implementation of ESD Protection Circuits in Nanoscale Fully Silicided CMOS Technology

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Publication List

(A) Referred Journal Papers:

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