國立交通大學

電子工程學系 電子研究所

博 士 論 文

提升積體電路栓鎖防疫能力之設計方法與實現

DESIGN AND IMPLEMENTATION TO IMPROVE LATCHUP IMMUNITY OF CMOS INTEGRATED CIRCUITS

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中 華 民 國 一0四 年 二 月

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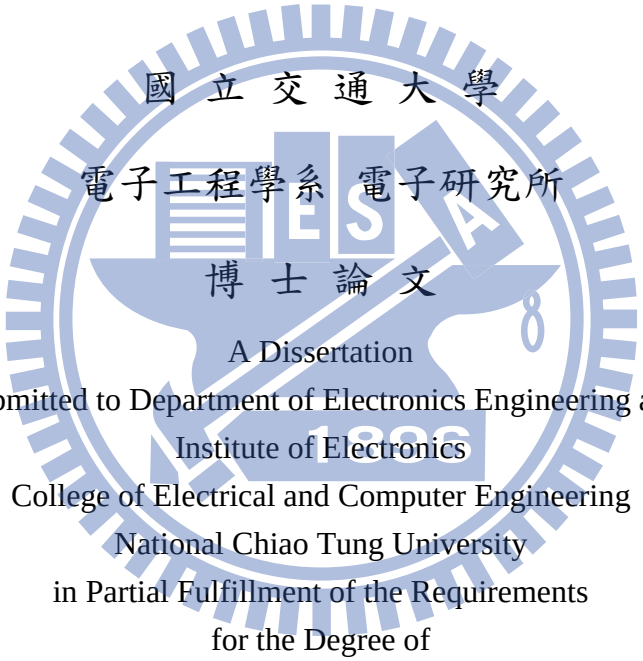

國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

A Dissertation

Submitted to Department of Electronics Engineering and

Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy

in

Electronics Engineering

Feb. 2015

Hsinchu, Taiwan, Republic of China

中華民國一０四年 二 月

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摘要

閂鎖效應(Latchup)是 CMOS 積體電路(IC)產品的設計上一項常見的問題，嚴重時可導致晶片損毀無法正常工作。此效應來源於晶片內部寄生的 P-N-P-N 結構，當受到外加電壓或電流刺激觸發，導通了此寄生結構，引發大電流產生，接面或路徑上的連接與金屬佈線都可能因為大電流損壞或因過熱形成開路或電源對地短路現象進而影響電路正常工作。另外，為了避免靜電放電轟擊對積體電路造成威脅與破壞，所有與外界接觸的輸出/輸入銲墊 (Pad) 皆須搭配相關的靜電放電防護設計。因此在積體電路產品中，皆必須於量產時通過 JEDEC 針對這些項目規範的測試以及 IC 壽命的測試，以確保提供給客戶的產品有一定的可靠度與足夠的耐用年限。

當積體電路應用於高壓環境，例如在相關交流轉直流轉換器(AC-DC converter)或直流轉直流 (DC-DC converter)轉換器等功率積體電路(Power IC)的設計上，元件本身需具備在積體電路正常操作時需要有與可能遇到的端點(閘極,汲極,源極,基極)對應壓差的耐受度。接面間的電壓也需小於接面間的崩潰電壓。考量到規格上規範的高壓電壓範圍，必須選取合適的製程和元件。然而在降低面積的因素下，低壓的元件和相關高低壓介面緩衝電路仍會被使用。在這樣的背景下，電路實體佈局和元件受外界刺激誤導通造成的過度電性應力的失效均須更加注意。

在本論文中，研究主題為避免閂鎖效應測試影響造成的過度電性應力失

效及提高電路對外界閂鎖效應刺激抵抗能力的設計，論文的章節包含：(1)實體布局考量和電路解法以避免在高壓積體電路設計中因閂鎖效應測試引發的過度電性應力失效。(2)透過對應補償電流抑制外界刺激引發閂鎖效應的防護設計。(3) 主動式防護環以及相關的電路實體實施例。

在第二章中，本論文提出了一個高壓積體電路產品研發上遇到的因閂鎖效應測試造成的過度電性應力損壞的實例。透過更佳的佈局方式與額外的保護電路，使原先因負閂鎖刺激電流測試引發不預期的過度電性應力的損壞可以成功的被避免。改良後的設計於 0.6 微米 40 伏高壓 BCD (Bipolar CMOS DMOS)製程實現，並通過 500-mA 的負閂鎖電流測試，避免掉原設計所遭遇的過度電性應力損壞的問題。新提出的解決方法可應用於高壓積體產品設計上以符合工業界對量產產品的要求與規範。

在第三章中，本論文提出了一個靠提供補償電流以對抗閂鎖測試電流刺激提高對閂鎖效應耐受度的方法。透過新增加的接面產生的寄生雙極性場效電晶體元件，閂鎖測試電流刺激可以被感測以導通 ESD 元件並降低外在刺激的影響程度。新提出的設計和傳統的單防護環設計一起在 0.5 微米 5 伏製程被實現，實驗結果驗證確實有改善的效果。

本論文第四章提出了一新型設計概念命名為主動式防護環以及相關的電路實體實施例以增加積體電路對閂鎖效應的免疫能力。透過新增加的感測電路與 ESD 元件或主動式緩衝器在正/負閂鎖電流測試擾動刺激下可產生根據正負刺激大小對應的導通電流以抵銷外界的刺激，此新提出的設計已在 0.6 微米 5 伏製程下驗證，確實有較傳統防護環設計更高的抵抗外界觸發式閂鎖效應發生的能力。

第五章則是總結了本篇論文的主要結果，並且提出一些關於未來可以改善或新應用的討論。本論文所提出的新型設計，皆搭配實體晶片進行驗證，並有相關論文和專利的發表。

DESIGN AND IMPLEMENTATION TO IMPROVE LATCHUP IMMUNITY OF CMOS INTEGRATED CIRCUITS

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Abstract

Latchup is a common problem in the CMOS IC product design and may lead to the damage or the malfunction of the chip. It is originated from the conducting of the internal parasitic P-N-P-N structure by the applied external voltage or current perturbation. Large current may be generated this time and causes the short through between the junctions and the open for the connections (as contacts, vias, or the metal lines) through the power line to the damaged devices. Besides, to prevent the destroying action and the threat brought by the Electrostatic Discharge (ESD) stress, all I/O PADs require to equip the corresponding ESD protection. Therefore, for the mass producing IC products, it is necessary to pass the tests defined in the JEDEC standards toward the latchup, ESD, and OLT items to guarantee enough reliability and lifetime of the product deliver to the customer.

When IC circuits are applied in the high-voltage (HV) environment (as for the Power IC design like the AC-DC and DC-DC converters), the utilized devices need to have the sufficient tolerance toward the voltage difference between the terminals. The voltages between the junctions also need to be smaller than the breakdown voltage. Considering the maximum applying voltage from the specs of HV pins, appropriate HV process and devices are chosen to implement the design. Low-voltage (LV) devices and circuit blocks as interface between the high-voltage and low-voltage environment may still be used to reduce the area consumption. Under such background, the layout arrangement to realize the chip and the EOS problem induced from the mis-conducting of certain transistors by the external triggers as in the latch-up test require more care in the design procedure of the qualified IC product.

In this dissertation, the main topic concentrates on the design to prevent the damage or failure brought by the external triggers as applied in the latch-up I-test. The content includes a brief introduction to the background of the latch-up and few prior arts and organize few proposed works includes: (1) layout consideration and circuit solution to prevent EOS failure induced by latchup test in a high-voltage integrated circuits (2) latch-up protection design with corresponding complementary current to suppress the effect of external triggers (3) active guard ring to improve latch-up immunity

In chapter 2, a practical industry case of EOS failure induced by latchup test in a high-voltage integrated circuits (IC) is presented. By using proper layout modification and additional circuit, the unexpected EOS failure, which is caused by negative-current-triggered latchup test, can be successfully solved. The new design with proposed solutions has been verified in 0.6-um 40-V BCD process to pass the test for at least 500-mA trigger current which shows high negative-current-latch-up immunity without overstress damage, compared with the protection of only guard ring. Such solutions can be adopted to implement high-voltage-applicable IC product to meet the industry requirement for mass production of IC manufactures and applications.

In chapter 3, a method to support complementary current at the pad under latch-up I-test is designed and fabricated to improve the robustness against latchup in the integrated circuits (ICs). By inserting additional junctions to form parasitic bipolar sensors, the external trigger can be monitored and the ESD-protection devices can be applied to provide such current and decrease the related perturbation to the internal circuits. The proposed design and the previous work with single guard ring have been fabricated in the same 0.5-um 5-V process. The experimental results confirm the enhanced latch-up tolerance of this work and the practicability in the SOC era.

In chapter 4, a new design concept named as active guard ring and related circuit implementation to improve the latch-up immunity of integrated circuits (IC) are proposed. By using additional sensing circuit and active buffer to turn on the ESD protection transistors, the large-dimension ESD (or I/O) devices can provide or receive extra compensation current to the negative or positive current perturbation during the latch-up current test (I-test). The new proposed solution has been verified in 0.6-um 5-V process to have much higher latch-up resistance compared with the conventional prevention method of guard ring in CMOS technology.

Chapter 5 summarizes the main results of this dissertation. Future work and the expansion for the proposed designs have also been discussed in this section. The related

papers have also been published or submitted to several international journals and the design for active guard ring has also been applied for patent.

Acknowledgment

在研究所的生涯中，首先要感謝我的指導教授柯明道教授，因為有老師多年來耐心的指導與鼓勵，使我能順利從碩士班到博士班，一步步地完成學業。除了在專業領域和論文內容中提供非常珍貴又悉心的指導和引導，老師認真嚴謹的研究和做事態度，更是我心目中的榜範。

感謝交通大學吳重雨教授擔任我的口試召集人、吳介琮教授、陳柏宏教授、中山大學王朝欽教授、晶焱科技姜信欽博士、聯合大學陳勝利教授、臺灣師範大學林群祐教授等在百忙之中抽空擔任我的口試委員，並給予珍貴的指導與建議，讓此博士論文更加完整。

在這段求學的過程中，『通嘉科技股份有限公司』給予了我研究上的支持與協助，從實驗晶片的下線及量測設備的支援協助，使得我實驗研究能夠順利完成。在此特別要感謝李皓民董事長、莊明男副總、周炯峰副總、李敬贊經理、劉益盛經理、鐘淑珍同仁、DN1 全體部門同仁、CAD 部門同仁等人所給予的支持與鼓勵，使本論文的研究成果得以成功驗證，並順利發表於國際期刊與國際研討會。

感謝 307 實驗室的所有人，特別是柯教授研究群畢業和現在碩一碩二及博士班所有在學的學弟妹們及卓助理。能和大家相處一起度過 meeting 和聚餐的時光是很快樂的事，謝謝顯峰還有一起參加生日聚餐的嘉岑、界廷、艾飛、志聰、義傑、睿閎、子毅、莞學、柏翰、品歆、美蓮、易翰、鼎洋、彼斯克、卡魯納、珵恩、靖雯、建豪、冠宇、凱能、珊綺、倍如。

感謝在學習歷程中，諸位研究群學長姊，同學，學弟妹，陳世倫博士、許勝福博士、陳榮昇博士、張瑋仁博士、蕭淵文博士、陳世宏博士、顏承正博士、王暢資博士、王資閔博士、陳穩義博士、竹立煒博士、葉致庭博士、邱柏硯博士、黃世豪博士、胡芳綾學姊、李宇軒學長、陳佳惠學姊、廖宏泰學長、許晏維學長、許順維學長、楊國忠學長、翁怡歆同學、張家綾同學、廖勝暉同學、林倍如學妹。

此外，我還要感謝王資閔博士、林群祐教授、兩位學長在論文發表過程中給予的一些寶貴的經驗的指導和鼓勵，讓我在論文完成的過程中能更加順利。

感謝敬愛的父母親蔡哲祥先生及彭玉花女士、哥哥蔡明宏、蔡明傑等親友。有了您們的支持、鼓勵、陪伴和照顧，才能讓我順利完成學業。感謝很好的長輩 Angel 及所有幫助我、陪伴我一同成長的師長、朋友、學長姊、同學、學弟妹們，也謝謝上天。

蔡　惠　雯
謹誌於竹塹交大
一 0 四年　四月

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Chapter 1

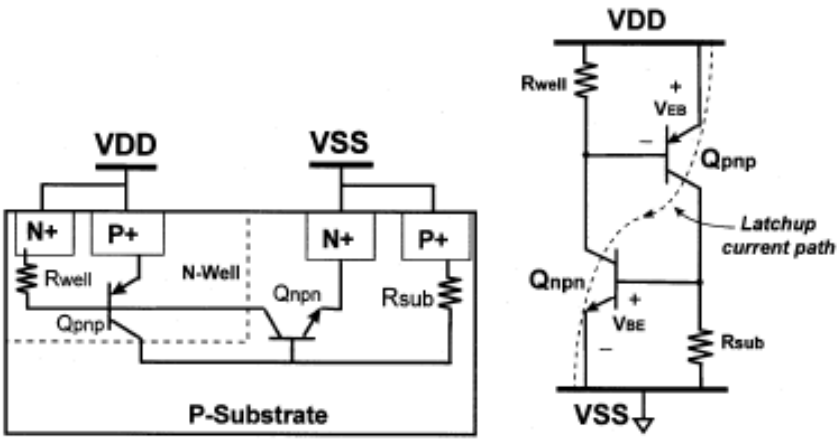
Introduction

In this chapter, the background of this dissertation is discussed. First, the occurrence of latchup and the related tests based on JEDEC standards are described. Then, prior arts which try to enhance the strength for the integrated circuits (ICs) under latch-up tests are introduced. Finally, the rest of the dissertation is organized and overviewed.

1.1 The Occurrence of Latchup and Related Latch-Up Tests Based on JEDEC Standards [1]-[4]

1.1.1 The Occurrence of Latchup

In SOC era, to achieve complicated function requests bring by the embedded system to build up incredible thin, light but powerful electronic product, MOSFET transistors are integrated in a tiny die by thousands. Thus, intrinsic bipolar structures are commonly exist in a CMOS chip and may form the equivalent SCRs (which is also called the PNPN structure) as shown in Fig. 1.1 (a) [1]. The inherent SCR (or named as PNPN structure) formed by the junction between transistors can be modeled as a PNP and an NPN transistor stacked next to each other with equivalent base terminals connected to the supply voltage (VDD) or ground (VSS) through nwell and psub resistors. The simple case of the parasitic PNPN structures can be found at the drain terminal of an inverter as shown in Fig. 1.1 (b). Such parasitic structure may be triggered if the transient noise appears at the power rail/ground or the base terminals of the PNP/NPN are pulled high/low by external overshooting/undershooting voltage/current perturbation from the I/O pads, respectively. Once the parasitic PNPN structure is triggered, large current will be induced by the positive feedback results from the conduction of effective BJTs. Such short circuit failure is named as “latchup” and has been introduced in many books or articles as [2]-[3]. If the junctions, metal lines or the contacts can’t tolerate the induced large current, unrecoverable damages or leakage path may thus affect the normal operation of the IC. Since parasitic PNPN paths are common for chip, we need to watch out and prevent for the latchup failure in design/layout stage. Besides, how to prevent the happen of latchup failure is regarded as an important reliability issue that is required be examined and pass for



(a)

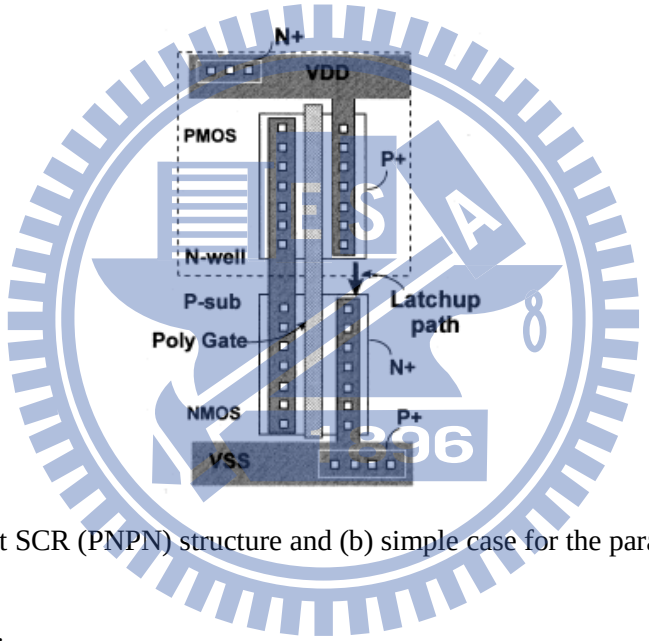
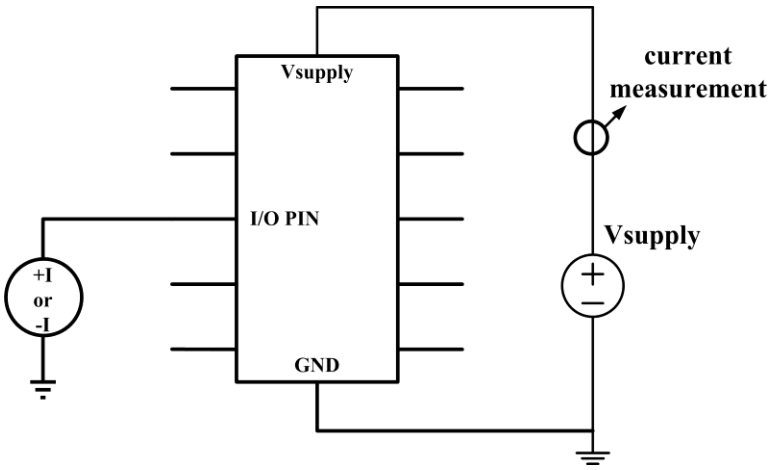


Fig. 1.1 (a) The inherent SCR (PNPN) structure and (b) simple case for the parasitic PNPN path [1].

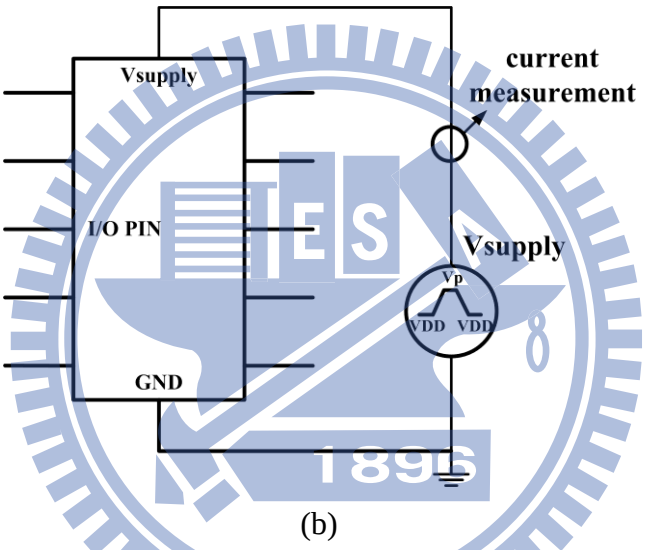
product mass production.

1.1.2 Latch-up Tests in JEDEC Standards

The methodology and specification to verify IC product with qualified latchup immunity have been described in JEDEC standard [4]. The latch-up tests including in the standards are designed to verify whether no trouble is found under different current or voltage perturbation and thus examined the latch-up resistance of the tested IC. The testing items cover the conditions of positive I-test, negative I-test and the overvoltage test for the IC product and can be applied to CMOS, bipolar, BiCMOS and the variations for the related technologies. The verification setup for the positive or negative I-test and the over-voltage test are simplified as shown in Fig. 1.2 (a) and (b), respectively. The external trigger current



(a)



(b)

Fig. 1.2. (a) The simplified verification setups for positive/negative I-test and (b) the over-voltage test.

source is connected to the I/O Pin alternately to test the performance of each pin and the supply voltage is given by a voltage source with its current is monitored. Other untested pins are biased at the maximum high level as specified in the specification of the product. The flow for the latchup test is shown as in Fig. 1.3. The test devices (here means the IC samples) which are ready for the latch-up test will firstly and finally undergo the complete tests (such as the normal tests in the FT(Final) test procedure) to make sure the devices are good before and after the latch-up test. The ATE (Automated test equipment) which is the device tester capable for the full function and parametric verification is used to carry out this task and acquire the data for normal supply current and other stable-state tested performance. The DUT in the diagram means the device under test and it will continue to be subjected to the conditions for the I-test and the over-voltage test. The above mentioned latch-up test is

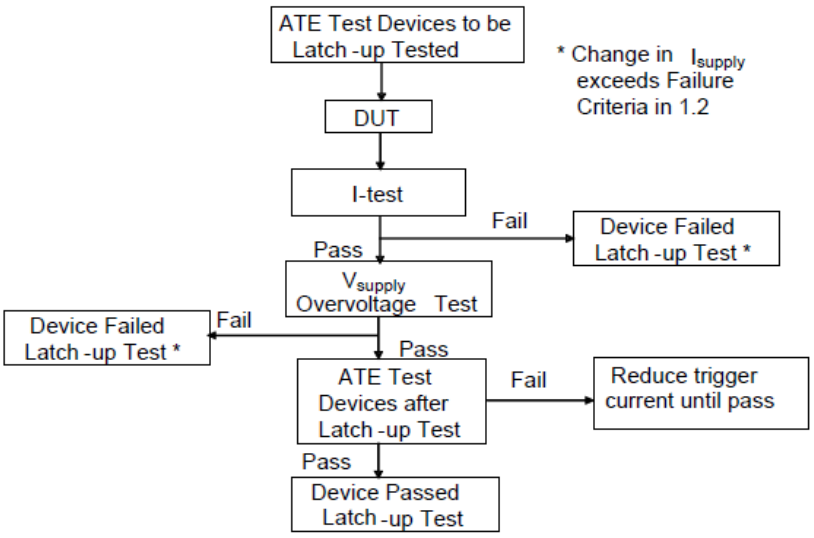


Fig. 1.3. The test flow for latch-up test.

Table 1.1

TRIGGER CHARACTERIZATION IN LATCH-UP I-TEST

Latchup I-test	Range of Stress	Force Current
Positive I-test	I	< 50 mA
	II	50 mA to < 100 mA
	III	100 to 150 mA
	IV	150 to 200 mA
	V	>= 200 mA
Negative I-test	I	> -50 mA
	II	-50 mA to > -100 mA
	III	-100 mA to > -150 mA
	IV	-150 mA to >-200 mA
	V	<= -200 mA
Overt-voltage test	1.5VDD or MSV, whichever is less	

allowed to test combinations or partitions by using at least 3 fresh IC samples for each divided item. Table 1.1 is the characterization of the force current and the over-voltage condition for the latch-up I-test and the over-voltage test specified in the up-to-dated standards. According to Table 1.1, the highest latch-up level with I-test has been updated to be greater than 200mA. Besides, the robustness of 100 mA or 200 mA against latchup is a familiar requirement in the datasheet of IC products. Besides, the supply voltage will be given to 1.5 times of its normal value or the MSV (maximum stress voltage) allowed by the datasheet of the product. The failed devices found after the tests will be sorted out from the

pass samples and won't undergo the rest tests to save the whole testing time. The failure based on abnormal supply current is judged by following (1) & (2) criteria:

$$I_{norm}+10\ mA\ (for\ I_{norm} \leqq 25\ mA) \qquad (1)$$

$$I_{norm}*1.4\ (for\ I_{norm} \geqq 25\ mA) \qquad (2)$$

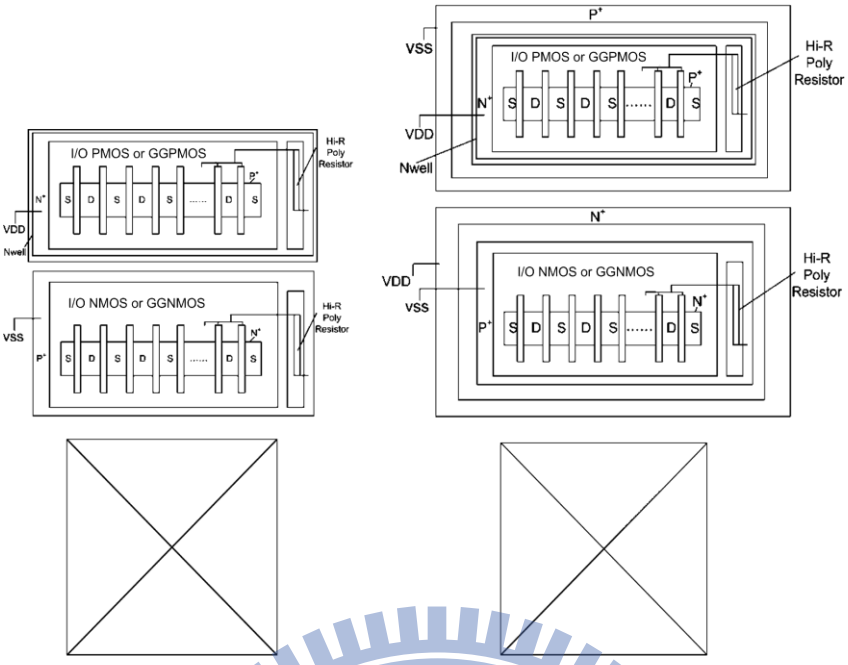
,where I_{norm} is the supply current of the test device under normal operating condition. By passing all the tests defined in the procedure with required trigger level, the IC products are believed to have sufficient latchup immunity in general system operation and is more relieved to be provided to the customers.

1.2 Prior Arts to Increase the Latchup immunity [5]-[19]

According to the recommended range in the JEDEC standards, many companies promote their IC products pass over 200-mA or 100-mA I-test against latchup and regard it as a required performance in the target specifications. To increase the latchup immunity of the chips, several modifications in process as epitaxial wafer [5], retrograde well [6], trench isolation [7]-[9], silicon on insulator (SOI) devices [10] and fabricated with extra isolating layers [11]-[13] have been proposed. However, due to the implementation cost, for most commercial designs, the protection are mainly performed by adding guard rings and adjust the pickups at certain region. Besides of the process and layout, solved the latch-up problems by adopting extra circuits is also an alternative way for its convenience to realize. In follow-up sub-sections, the methods as guard rings and the circuit solutions to achieve the latch-up protection are briefly introduced with few works are also depicted.

1.2.1 The Guard Ring Protection Methods

Fig. 1.4(a) shows the I/O or ESD cells protected by the single guard ring protection [14]-[16]. Compared with no guard ring structure, the bulk terminals of the I/O or ESD cells are placed and surrounded to the whole region of its gate, source, and drain area. The benefits of guard rings are to reduce the beta gain of the lateral parasitic BJT and the relative nwell/psub resistance to increase the latchup immunity. Generally, 2 guard rings are required between adjacent PMOS and NMOS transistors and the I/O cell with single guard ring meet this requirement itself. However, when considering the potentially



(a) (b)

Fig. 1.4. Prior protection work with (a) single guard ring, (b) double guard ring [3], [14]-[17].

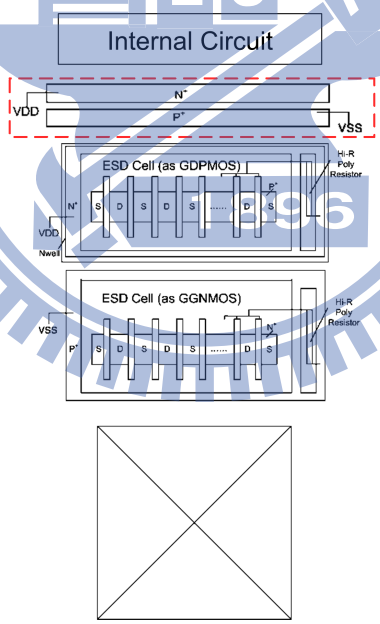


Fig. 1.5. Prior protection work with internal extra guard rings [3].

threat brought by the internal sensitive SCR paths, Fig. 1.4 (b) and Fig. 1.5 are proposed and considered to have higher latchup immunity but also inevitably result in additional layout areas [3], [17]. Moreover, the production cost might be increased especially for high pin-count CMOS ICs. Thus, whether the guard rings or extra guard rings are necessary is determined by whether the I/O cells are latchup free (such as (holding voltage

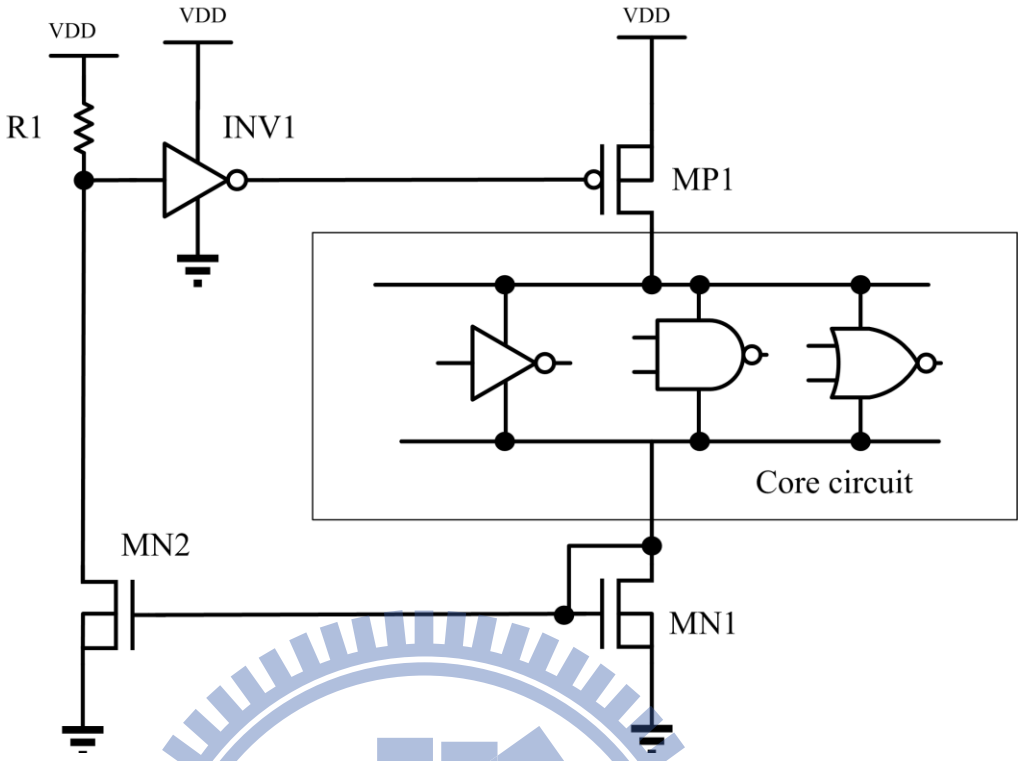


Fig. 1.6. Prior art with latch-up current self-stop circuit [18].

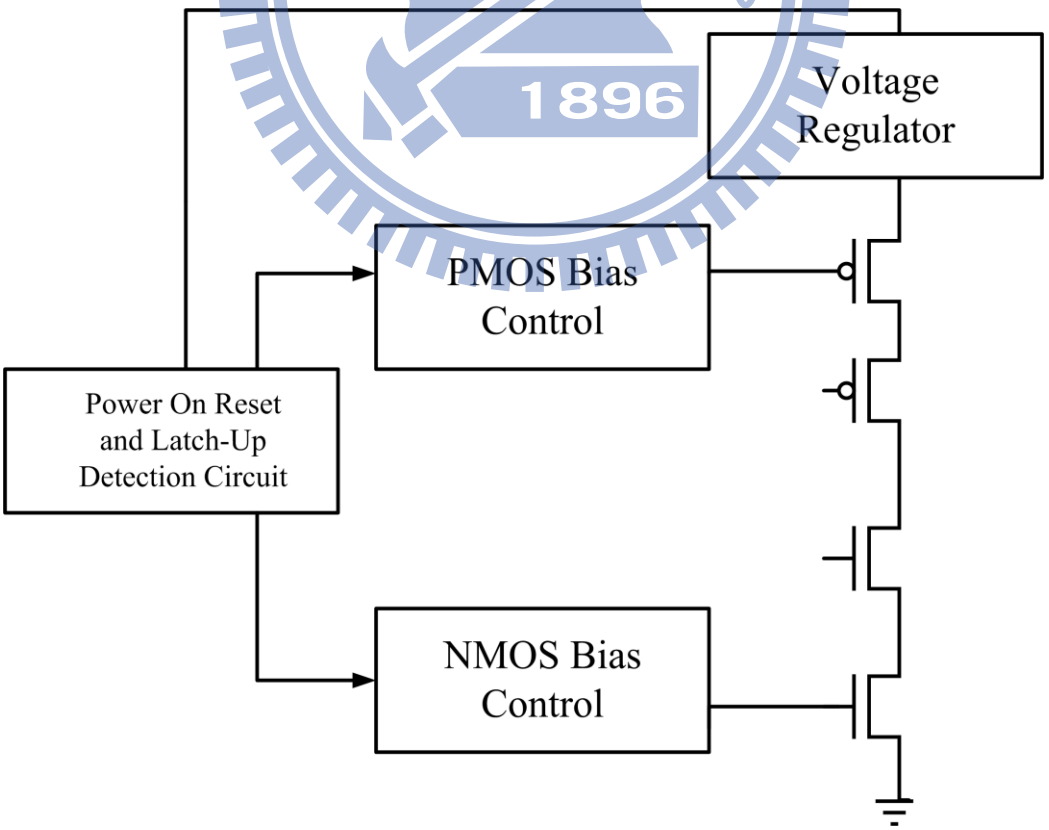


Fig. 1.7. Prior art with latch-up recovery circuit [19].

higher than the VDD normal operating voltage of the I/O cells…etc.) and how sensitive the internal circuits are. Instead of using double guard rings, if simply the single guard ring, or even no guard ring, is enough to help the I/O cells be latchup-free, the layout areas of the I/O cells can be greatly reduced for cost-down purposes. Meanwhile, it is highly emphasized that methods as disposing additional guard rings are only effective upon those areas where the guard rings are located. In other words, for other areas where no guard rings are disposed, its latchup immunity cannot be improved by doing so. Thus, the layout to implement the guard ring and the placement are important when the guard ring protection methods are applied.

1.2.2 Circuit Solution to Avoid Latchup Fired

Besides the solutions to add guard rings, extra insulating layers or some other modification in the layout structure to implement the design, circuit solutions as latch-up current self-stop circuit [18] and the latch-up recovery circuit [19] have also been proposed. Fig. 1.6 shows the prior art with the latch-up current self-stop circuit. The circuit contains a PMOS switch MP1, a diode-connected NMOS MN1 as well as its current mirror pair MN2, and the circuit (INV1 and R1) to bias the gate of the MP1. Once the current flow to the ground becomes abnormal due to the happening of latchup, it is detected by the MN1, MN2 and the MOS switch MP1 is turned off to disturb the current path from the power line to the internal SCR structure and release the latch-up state after the trigger is over. Fig. 1.7 shows the patented latch-up recovery circuit. Similar with the concept in Fig. 1.6, the prior art in Fig. 1.7 detects the latch-up occurrence and shuts down the path to both power and ground. By disturbing the path and also the latch-up status, the prior art also shows the enhancement of the latchup immunity. However, the MOS switches are requested at the prior arts and thus it may take some area to implement the switch with acceptable transient/steady state voltage drops and the power loss. Besides, if other internal powers are required, especially the high voltage supply, additional design may be also required to reduce the effect of external latch-up triggers toward the inherent sensitive PNPN paths which are connected to different internal powers.

1.3 Dissertation Overview

The main object for the proposed designs in this dissertation concentrate on the enhancement of latchup immunity or the prevention for the EOS problem brought by the

external triggers as applied in the latch-up I-test.

The content includes: (1) layout consideration and circuit solution to prevent EOS failure induced by latch-up test in a high-voltage integrated circuits (2) latch-up protection design with corresponding complementary current to suppress the effect of external triggers (3) active guard ring to improve latchup immunity

In chapter 2, a practical industry case suffers EOS failure induced by latchup I-test in a high-voltage integrated circuits (IC) is presented. The novel design adopting the modifications in layout and circuit to prevent the unexpected EOS failure successfully. The proposed work has been verified in 0.6-um 40-V BCD process and verified to pass at least 500-mA latch-up I-test which shows high latchup immunity compared with the traditional protection of only guard ring. The novel idea can be adopted to implement high-voltage-applicable IC product to meet the industry requirement for mass production of IC manufactures and applications.

In chapter 3, a proposed method to provide complementary current at the pad under latch-up I-test is introduced. The inserting additional junctions and the resistors are used to monitor the external triggers. The ESD-protection devices can be applied to provide the required complementary current and decrease the related perturbation to the internal circuits. The proposed design and the previous work have been fabricated in the same 0.5-um 5-V process.

In chapter 4, a novel design named as active guard ring and related circuit implementation are proposed to improve the latchup immunity of integrated circuits (IC). By adopting additional circuit and active buffer to turn on the ESD protection transistors, the large-dimension ESD (or I/O) devices can effectively turned on to generate extra compensation current to the negative or positive current triggers during the latch-up I-test. The new proposed solution has been verified in 0.6-um 5-V process and shows much higher latch-up resistance compared with the conventional prevention method of guard ring in the test results.

Summary for the main results of this dissertation is in chapter 5. Discussions about the future work and the expansion are also arranged in this section.

Chapter 2

Layout consideration and circuit solution to prevent EOS failure induced by latchup test in a high-voltage integrated circuits

A practical industry case of EOS failure induced by latchup test in a high-voltage integrated circuits (IC) is introduced in this chapter. By using proper layout modification and additional circuit, the unexpected EOS failure, which is caused by latchup negative I-test, can be successfully solved. The new design with proposed solutions has been verified in 0.6-um 40-V BCD process to pass the test for at least 500-mA trigger current which shows high negative-current-latchup immunity without overstress damage, compared with the protection of only guard ring. Such solutions can be adopted to implement high-voltage-applicable IC product to meet the industry requirement for mass production of IC manufactures and applications.

2.1 Introduction

As the supply voltage increases while the chip is expected to be conserved in HV IC's, the integration of HV and LV devices becomes one of the trends for HV SOC designs. In the operation of HV environment, the high-voltage-tolerated pre-regulator is usually required to serve as the interface between HV and LV blocks and provides the necessary low supply voltage to the inner low-voltage circuits. However, certain node voltages in HV blocks as the HV pre-regulator may be abnormal since the high-voltage drift Nwell (HVNW) junctions in the HV devices are prone to the sink current brought by the parasitic bipolar transistor, especially during the negative I-test. Moreover, improper layout placement related withapplied at the external supply is higher than the tolerance of LV transistors, it can even lead to ill function of ICs due to the electrical overstress (EOS) which may cause permanent damages [20]-[21] at the metal connections or junctions of LV devices.

To increase the latchup immunity of the chips, guard ring protection introduced in chapter 1 is often used to reduce the substrate current which flows in the inner circuit blocks

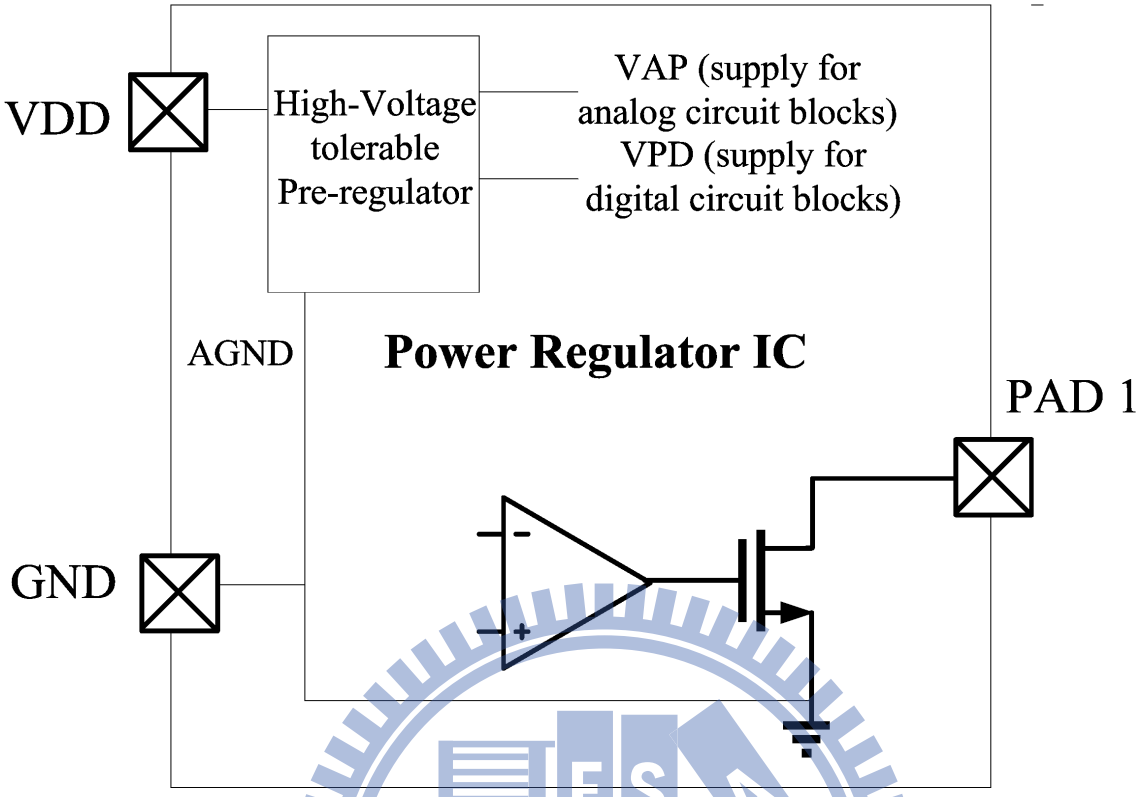


Fig. 2.1. Simplified circuit structure of a practical power regulator IC.

[14], [22]. Prior arts as fabricate devices surrounding with insulating oxide layer (trench) [8]-[9] or lightly doped epitaxial layers grown on heavily doped substrates in [12]-[13] can also eliminate the sink current by breaking the parasitic bipolar structures. However, the protection of guard rings or extra layers increases the chip area or the fabrication cost. Even with the protection of guard rings, wider distance between the trigger source at I/O pin and the inner circuit or inner guard rings are still required [3], which may still be insufficient to the HV devices with deep HVNW junctions.

In this work, a practical industry case of EOS damage induced by the latchup negative I-test in a HV CMOS IC is described. The proper layout modification, the additional circuit solution, and the experimental latchup test have been verified in silicon to illustrate the improvement.

2.2 Negative I-test induced EOS failure with only guard ring protection

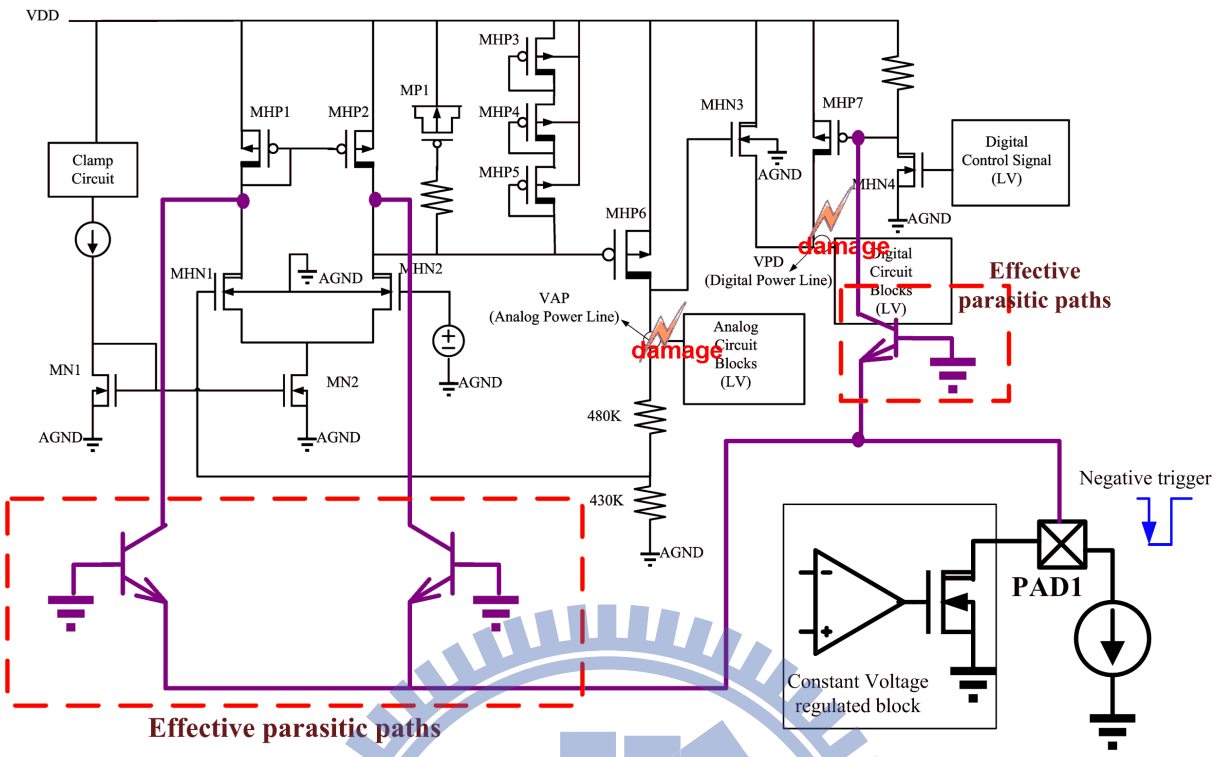
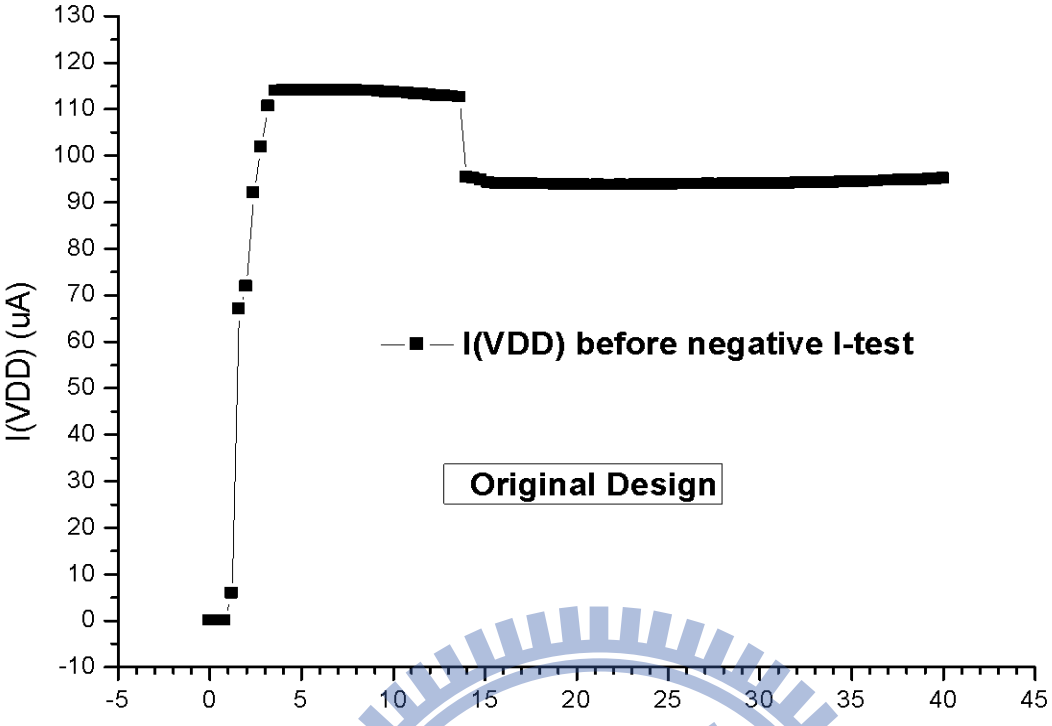
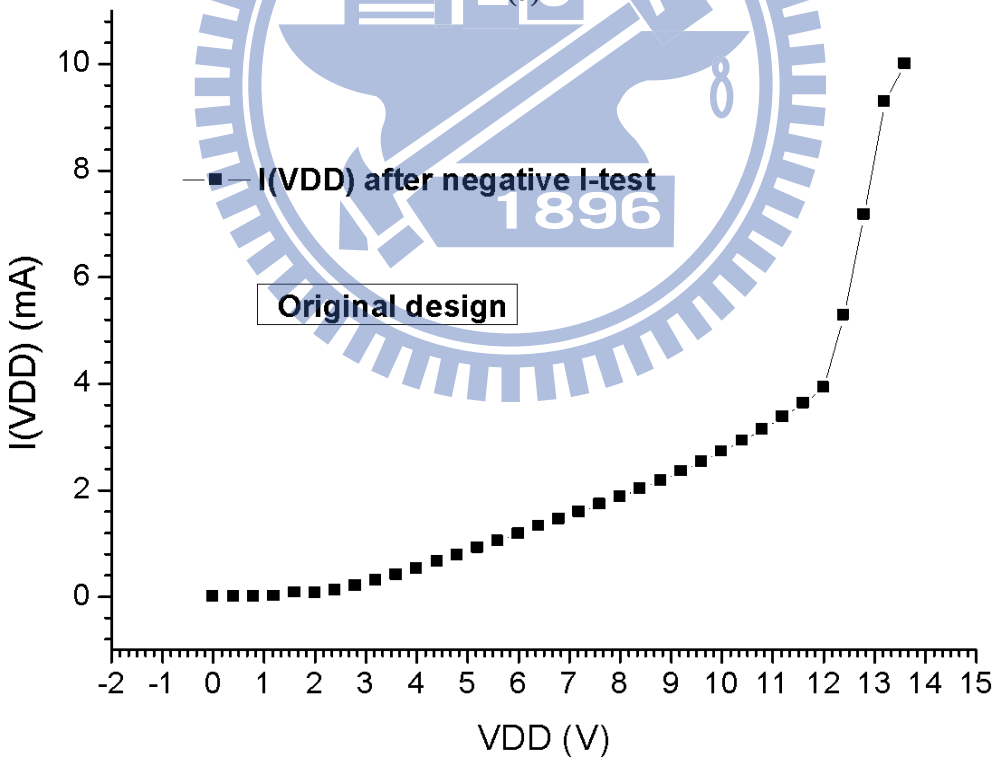


Fig. 2.2 The schematic of high-voltage-tolerable pre-regulator in this practical work with effective parasitic paths from pad1.

To operate at HV environment but maintain the compression of chip area, a simplified structure for practical high-voltage-tolerable IC has circuit blocks shown as Fig. 2.1. The high-voltage-tolerable pre-regulator is composed of HV devices or both HV and LV devices, which is used to generate the necessary low supply voltage such as ~3.3 V (at VAP node) or ~2 V (at VPD node) to the analog or digital LV inner circuit, respectively. The high-voltage-tolerable pre-regulator in the practical work with effected parasitic from pad1 is shown in Fig. 2.2. MHN1 to MHN4 of the schematic in Fig. 2.2 are the HV NMOS transistors which can tolerate drain-to-source voltage difference (|Vds|) up to 40V and MHP1 to MHP7 are the HV PMOS transistors with up to 40-V tolerance of source-to-drain voltage difference (|Vsd|) in a 40-V HV process. MN1, MN2, and MP1 are the 5-V LV devices used to provide the necessary bias current and the compensation for stability. The high-voltage-tolerable pre-regulator is composed of a two-stage amplifier with feedback connection as a typical LDO structure [23]. With the high-voltage-tolerable pre-regulator, the IC can operate normally under the desired HV supply such as 40 V. However, the practical packaged IC is still damaged during latchup test even guard ring protection had been placed between the HV I/O PAD and inner circuit blocks. After applying negative I-test with



(a)



(b)

Fig. 2.3. Measured supply voltage and related current for the original design (without the modification) (a) before, and (b) after, the negative I-test applying at the PAD 1 with 100-mA sink current during the latchup test.

100-mA sink current at some I/O PAD (as the PAD1 shown in Fig. 2.1) with the high supply voltage (such as 30 V) over the tolerable range of LV devices, the practical work shows high abnormal current (up to mA) from the supply VDD to ground as depicted in Fig. 2.3(b) compared with the normal result (under 120 μA) before the test as shown in Fig. 2.3(a). The die photo of the damaged IC is shown in Fig. 2.4(a) and the damages apparently happened at the drain terminals of MHP6 and MHP7 which are the interfaces of high-voltage-tolerable pre-regulator to the LV digital blocks. Fig. 2.4(b) shows the partial layout presented with only HVNW and P+ implement layers that are nearby the PAD 1 in Fig. 2.4(a). The widths of the HVNW junctions in the guard ring and the transistors (including MHN1, MHN2, and MHN4) are 15.9 μm (W1) and 9.2 μm (W2), respectively, as shown in Fig. 2.4(b). The minimum distances between the edges from the HVNW junction at PAD 1 to the HVNW junctions in the guard ring, the transistor MHN1, and MHN4 are also shown in Fig. 2.4(b), which are 20 μm (D1), 118 μm (D2), and 154 μm (D3), respectively.

The reasons for the damages can be attributed to the short-through conductions from the supply voltage VDD to ground GND. Such paths are caused by the conductions of the transistor MHP6 and MHP7. The parasitic NPN structures from the I/O PAD to p-type substrate and internal HVNW layer of the HVNMOS transistors (such as the input pair of the amplifier) are shown as Fig. 2.5(a). With the consideration to avoid the negative impact from mismatch, HV NMOS MHN1 and MHN2 are arranged as MHN1-MHN2-MHN2-MHN1 placement in layout, and the two multipliers of MHN2 share the same drain area to make the die more compressive. The simplified cross-section view is shown in Fig. 2.5(b). When a large negative current is applied at the I/O PAD (as the PAD1 depicted in Fig. 2.4), the parasitic NPN structure attributed by the guard ring is triggered and expected to conduct the most current to the I/O PAD. However, there is still some current induced by another parasitic NPN structure. The node voltages such as the drain terminals of HV NMOS MHN1,2, and 4 are pulled down due to the current flow induced by the sink current source, which is through the N+-HVNW junctions to the substrate as well as the I/O PAD to the source. The amount of induced current is correlated with the amount of sink current at the I/O PAD, the related location of the current source to the affected victim, and the junction area of the parasitic structure. Moreover, due to the layout structure shown in Fig. 2.5(a), the area of the HVNW junction connected to the drain terminal of MHN2 is double compared with that connected to the drain terminal of MHN1. Therefore, more current are sunk at the drain terminal of MHN1 and the voltage of gate terminal for MHP6 is pulled low which leads to the conduction MHP6

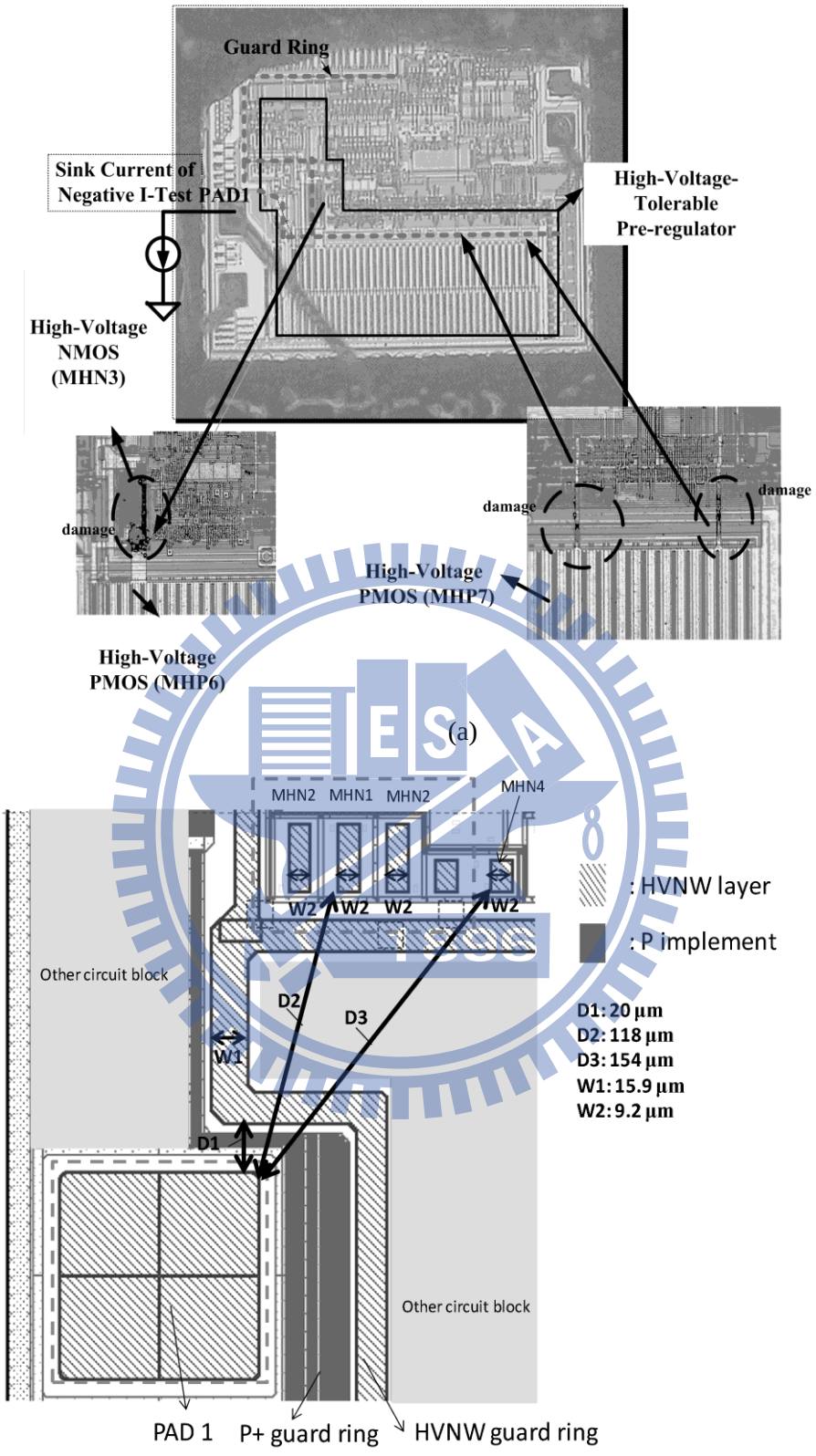


Fig. 2.4 (a). Die photo of the practical IC fabricated in 0.6-um 40-V BCD process with negative I-test induced EOS damages. The dotted line in the photo depicts the guard ring connected to VDD. (b) The partial layout presented with only HVNW and P+ implement layers to show the widths and minimum distances of HVNW junctions from the PAD 1 to the guard ring, transistor MHN1, and MHN4.

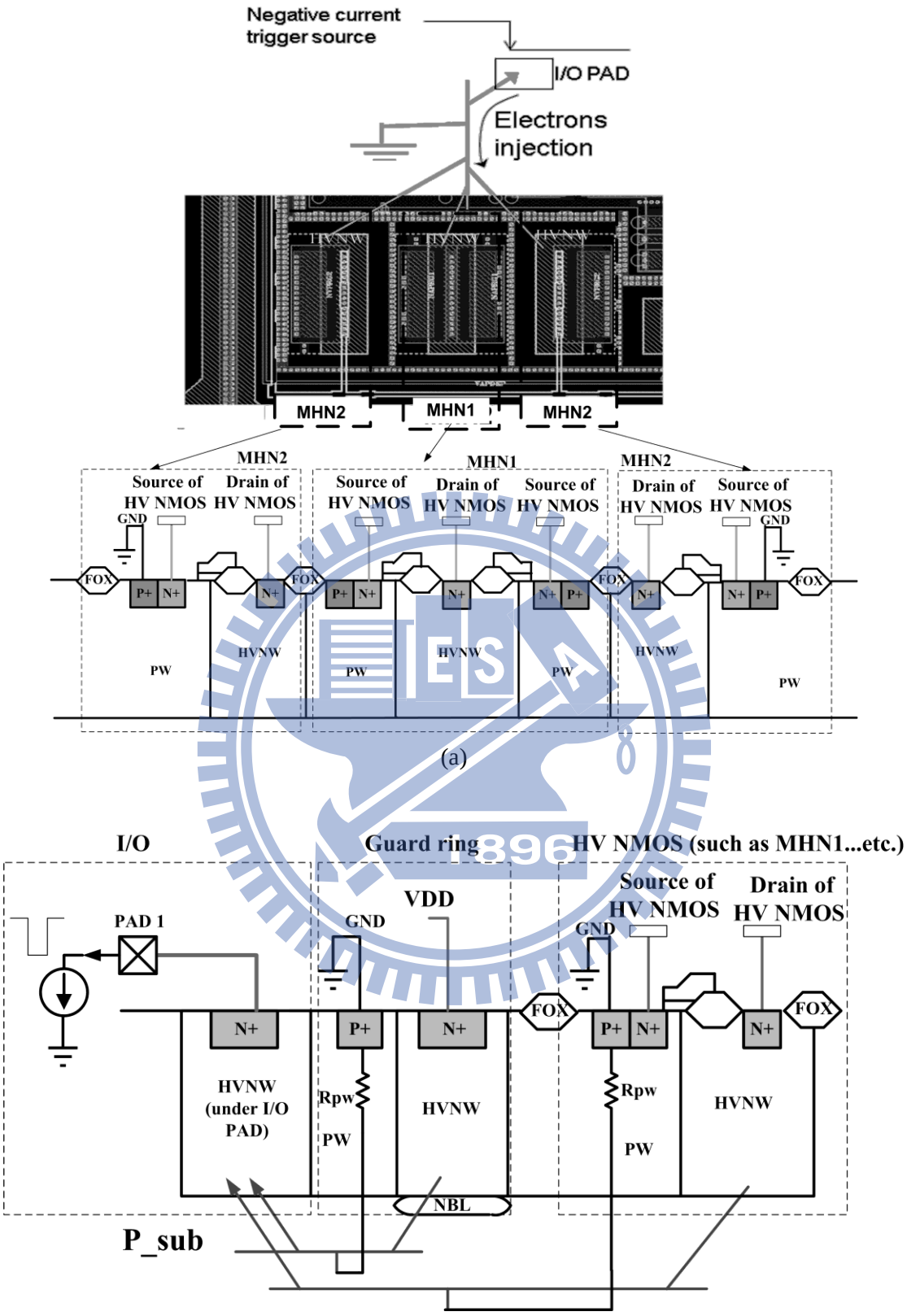


Fig. 2.5 (a) Parasitic NPN structures from I/O PAD to p-type substrate and internal HVNW. (b) The simplified cross-section view to show the parasitic NPN structure.

to cause the overstress failure in the practical work as shown in Fig. 2.4.

2.3 Re-design for elimination of latch-test test induced EOS failure

2.3.1 Modification of layout placement

To prevent such EOS problem in the above mentioned HV IC, the simplified improper layout placement for the input pair MHN1and MHN2 of the original work is shown in Fig. 2.6(a). The proper modification with replacement in layout by metal re-connection is shown in Fig. 2.6(b). The locations of transistor MHN1 and MHN2 are exchanged so that the drain terminal of MHN1 is connected to double area of HVNW junction than that of MHN2. By such replacement, more current can be sunk at the node connected to the drain terminal of MHN1 than that of MHN2. Due to the current mirror structure, the sink current at the drain terminal of MHN1 drawn by the parasitic NPN is turned into the source current at the drain terminal of MHN2 through MHP1 to MHP2 which is also above double than the sink current. Thus, not only the sink current of the drain terminal for MHN2 can be compensated, but also the voltage at the gate terminal of MHP6 is pulled high to obstruct the conductive path caused by MHP6 from external supply VDD to inner supply VAP and VPD.

2.3.2 Modification with additional sensing and compensation circuit

Another method with circuit solution is proposed as shown in Fig. 2.7. The additional circuit is designed to compensate the induced sink current from I/O PAD to the HVNW junction and also the drain terminal of HV NMOS transistors during latchup negative I-test. The proposed circuit contains a sensing part (implemented with HVNMOS MHN5 as well as a resistor) and a current mirror part (implemented with HVPMOS as MHP8~MHP10) to compensate the induced sink current. The HVNMOS MHN5 is gate grounded to turn off HVPMOS MHP8~10 in the normal operation, but offers a sink current by the parasitic NPN structure when the large negative current at PAD 1 is sensed. When induced sink current is larger, the related sensing current is larger and the source to gate voltage of the diode connected HVPMOS MHP8 is also larger to produce more mirrored current at the HVPMOS MHP9 and MHP10. By connecting the drain terminals of the HVPMOS transistors as MHP9

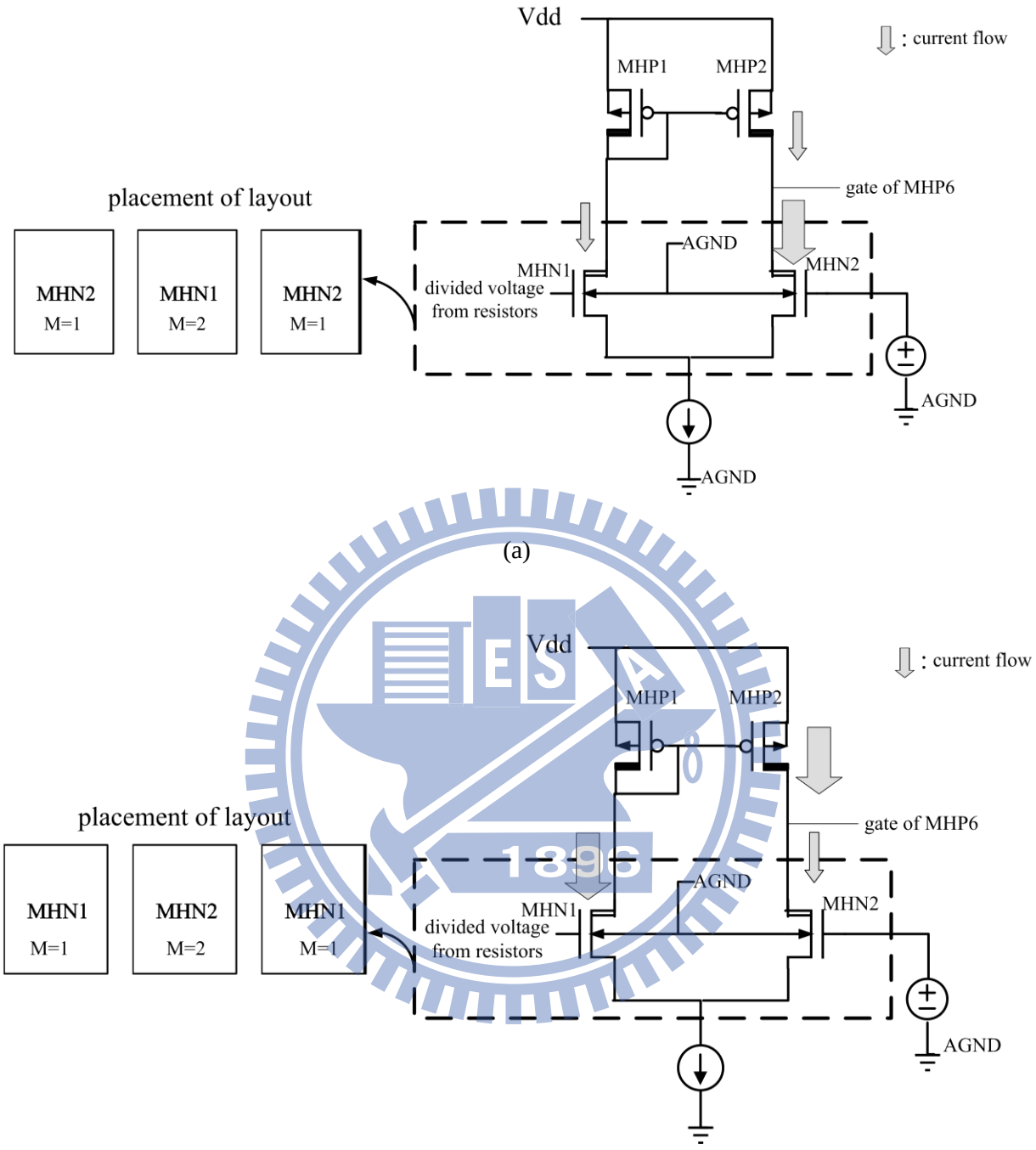


Fig. 2.6. (a) Improper layout placement for the input pair composed of MHN1and MHN2 in the original work. (b) the proper modification of the revised design with replacement in layout by metal re-connection.

and MHP10 to the nodes as the gate terminals of MHP6 and MHP7, the latchup-test-induced sink current can be compensated. Thus, the gate voltages of MHP6 and MHP7 were prevented from pulled low to trigger low impedance paths from external HV supply to inner

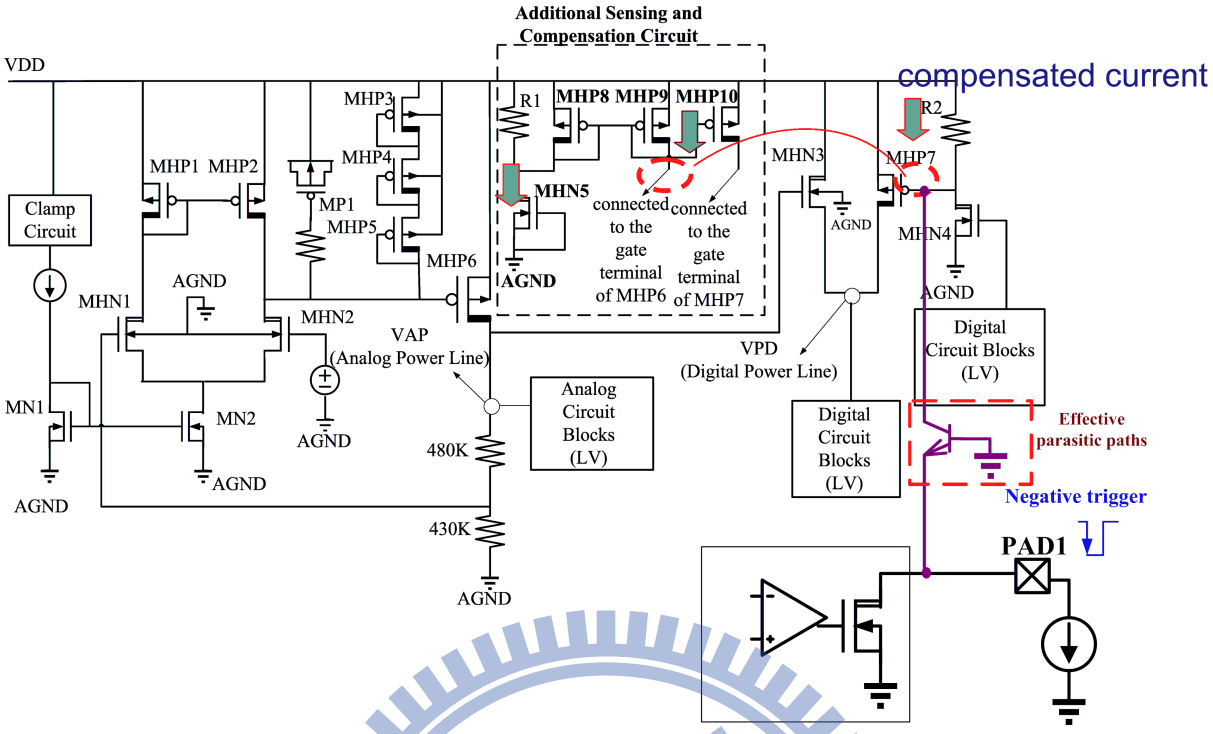


Fig. 2.7. The schematic of the revised design with new proposed sense and compensation circuit.

LV supply. The sensing current can be used to produce a sink current through NMOS current mirror or a digital enable signal to launch protection mechanism to prevent the effect brought by the mis-trigger of certain logic circuit under negative-current-triggered latch-up test.

2.4 Experimental Results and Discussion

The proposed layout replacement and additional circuit solution have been verified with 0.6-um 40-V BCD process in the revised version of the HV IC. Fig. 2.8 shows the measured results of certain signals in the original IC to depict the root cause of the EOS problem, as shown in Fig. 2.3(a) and Fig. 2.4. External voltage VDD is given as 6 V to perform the overstress situation without damaging the IC directly. When a 30-mA sink current is applied at the PAD 1, the inner supply voltage VAP is pulled up from the normal value (~3.3 V) to the voltage near VDD. When a larger sink current is used, the problem remains. The drain voltage of MHN1 is also shown in Fig. 2.8 to see the effected drain voltage of MHN1 with sink current through HVNW junction to HVNMOS devices. Since the inner supply voltage VAP from the pre-regulator is pulled up to ~VDD after the negative I-test, the 5-V LV blocks or the metal line may have reliability problem with high voltage at VDD. It is even damaged

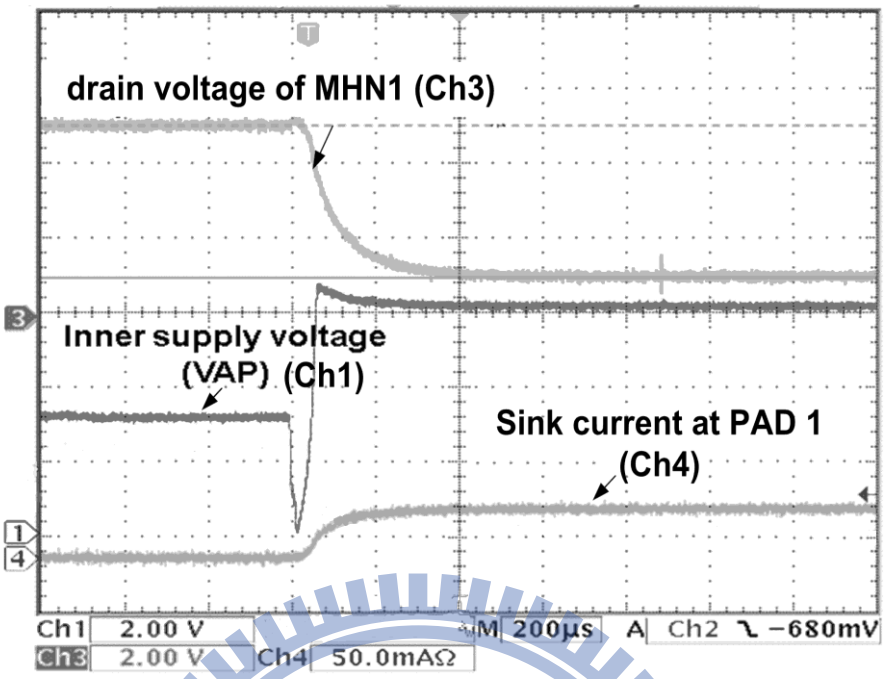


Fig. 2.8. Measured inner supply voltage when a 30-mA sink current is applied at the PAD 1 of the original IC without modification.

directly when the applied voltage at VDD is higher than the breakdown voltage of LV junctions such as ~12 V in the 0.6-um 40-V BCD process. With the exchange of layout locations, the inner supply voltage VAP will be pulled low directly shown as Fig. 2.9 to prevent the damage due to the electrical overstress. The sink current at the PAD 1 is increased to examine if the solution is suitable to prevent the EOS problem for negative I-test with even large current over 500 mA.

The additional sensing and compensation circuits are also applied to the revised version to verify the results shown in Fig. 2.10. While current starts to be sunk at the PAD 1, the inner supply voltage (VAP) in Fig. 2.10 is also pulled down to prevent the overstress to the LV blocks. For the devices of the input pair, proper layout is already enough to eliminate the overstress problem happened at the output of the HV pre-regulator as VAP in Fig. 2.2. However, for the case of the damage happened at the node as VPD in Fig. 2.2, the solution of additional sensing and compensation circuits are also required at the gate of MHP7 to prevent the conduction of MHP7 during negative I-test. Fig. 2.11(a) shows the measured external supply current I(VDD) corresponding to the related supply voltage (VDD) for the revised design with both modifications before the negative I-test. Fig. 2.11(b) presents the measured

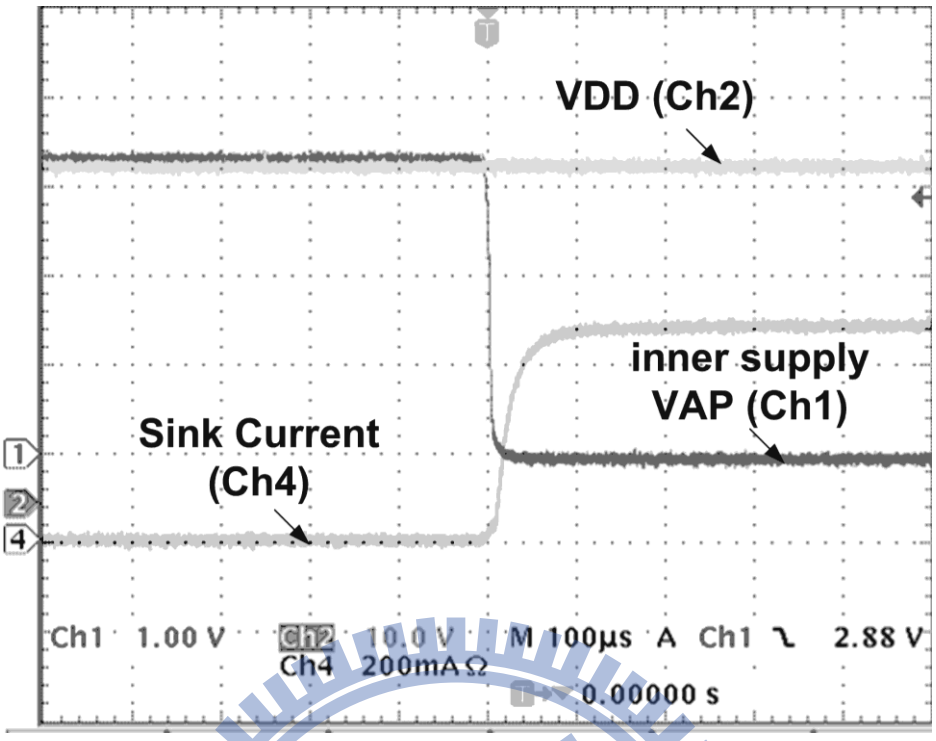


Fig. 2.9. Measured inner supply voltage with a 500-mA sink current at the PAD 1 of the revised design with proper layout at input pair of the pre-regulator.

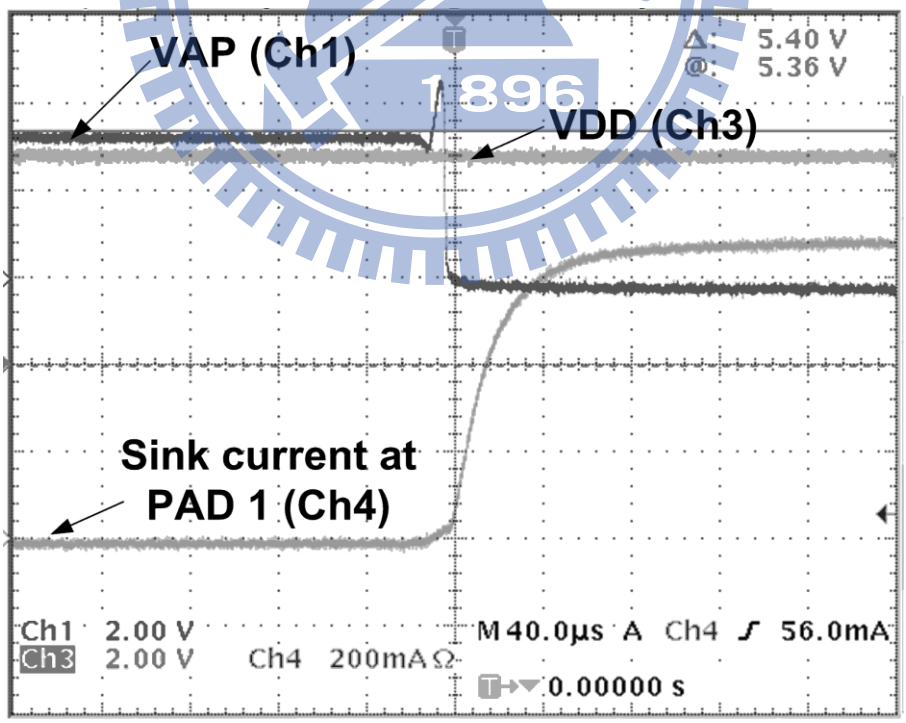
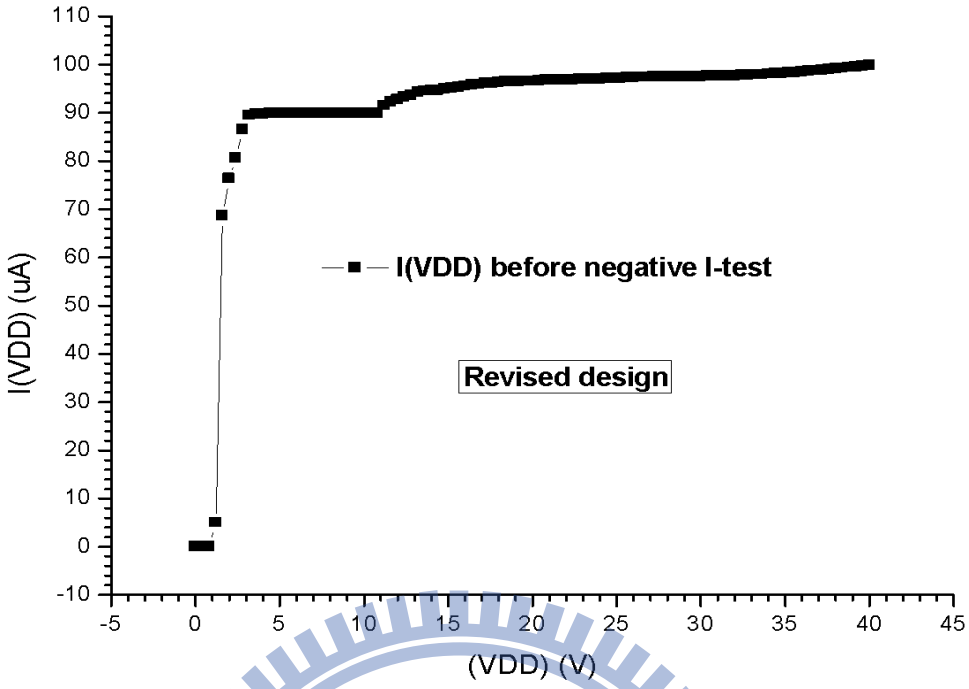
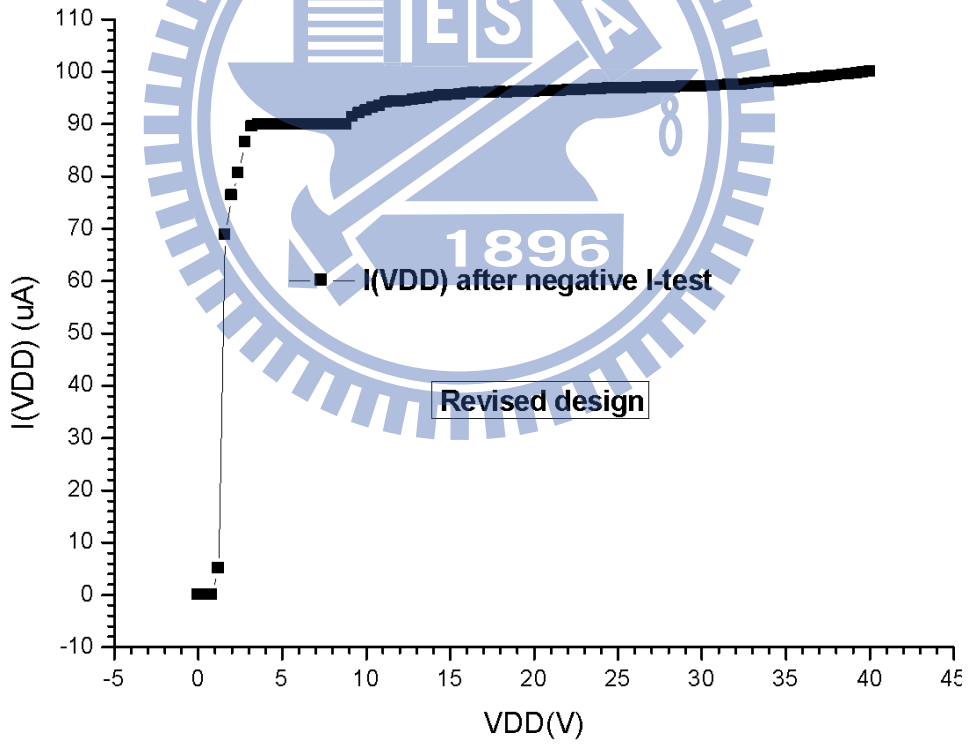


Fig. 2.10. Measured inner supply voltage with a 700-mA sink current at the PAD 1 of the revised design with proper layout at input pair of the pre-regulator.



(a)



(b)

Fig. 2.11. Measured external supply current I(VDD) to the related supply voltage (VDD) for the revised design with the modifications (a) before, and (b) after, the negative I-test with 100-mA sink current at PAD1.

results after 100-mA sink current is applied at VDD during negative I-test at PAD1. As shown in these two figures, the revised design with the modifications has almost the same I-V curve before and after the test, whereas the original design without the modifications suffers large leakage at supply pin which causes the overstress damage. Therefore, both the analog and digital supply voltages of the LV circuits in the revised design can be prevented from the EOS problem to ensure qualified latchup immunity.

2.5 Summary

The proposed modifications to solve the EOS problem induced by the negative I-test have been verified successfully in 0.6-um 40-V BCD process. With proper layout replacement and additional circuit, the inner power VAP and VPD are all prevented from conduction to the HV external supply VDD in the revised design. With the proposed solutions, the implemented chips pass at least 500-mA latch-up test. The proposed solutions in this work are useful to improve the robustness of the circuit in HV environment and also remain qualified latchup immunity of HV circuits in SoC applications.

The content of this chapter was published in [24] (with co-author of Yi-Sheng Liu and Ming-Nan Chuang) and [25].

Chapter 3

Latch-up Protection Design with Corresponding Complementary Current to Suppress the Effect of External Triggers

The robustness against latchup in the integrated circuits (ICs) can be improved by supporting complementary current at the pad under latch-up I-test. By inserting additional junctions to form parasitic bipolar sensors, the external trigger can be monitored and the ESD-protection devices can be applied to provide such current and decrease the related perturbation to the internal circuits. The proposed design and the previous work with single guard ring have been fabricated in the same 0.5-um 5-V process. The experimental results confirm the enhanced latch-up tolerance of this work and the practicability in the SOC era.

3.1 Introduction

In modern CMOS technology, electrostatic discharge protection (ESD) becomes an important design concern of IC products [26], [27]. An input buffer with conventional ESD protection is shown in Fig. 3.1 as an example. To ensure desired ESD level, conventional ESD-protection PMOS and NMOS transistors are added at input pads in ICs. However, besides for ESD performance, the Latchup immunity is also cared in the development of ESD cells. Several prior arts are thus proposed as [28], [29]. For traditional ESD-protection transistors, guard rings typically surround the devices as shown in the cell layout of Fig. 3.2 to decrease the susceptibility of latchup in both the input buffer and the internal circuits [14], [17], [30].

Besides the traditional strategy with guard ring protection, a modification is implemented in this work and verified to have enhanced Latchup immunity. The additional junctions are utilized to pick up some induced currents corresponding to the external trigger currents and turn them into the force to control the existing ESD devices for enhancing the resistance against the external perturbations.

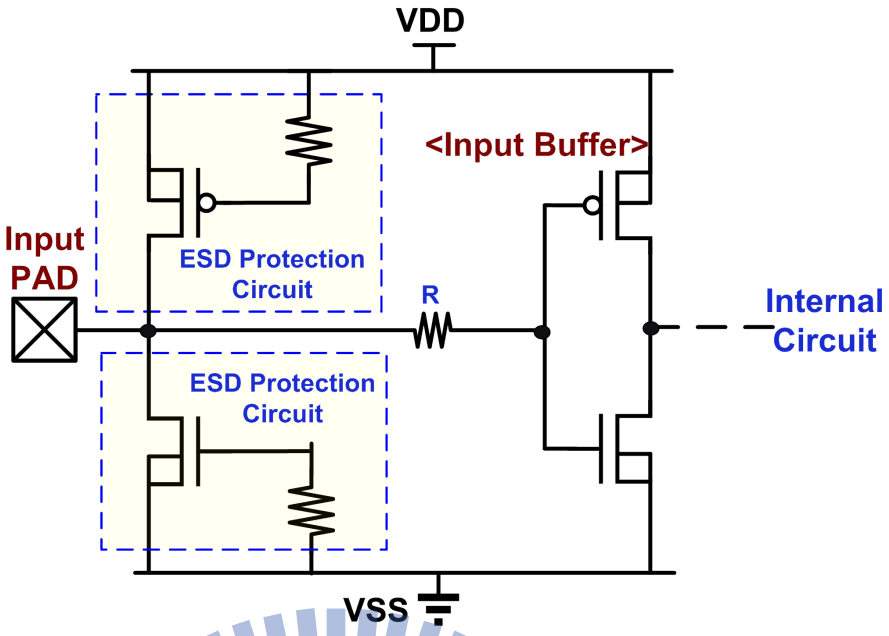


Fig. 3.1. Input buffer with GGNMOS and GDPMOS to provide general ESD protection.

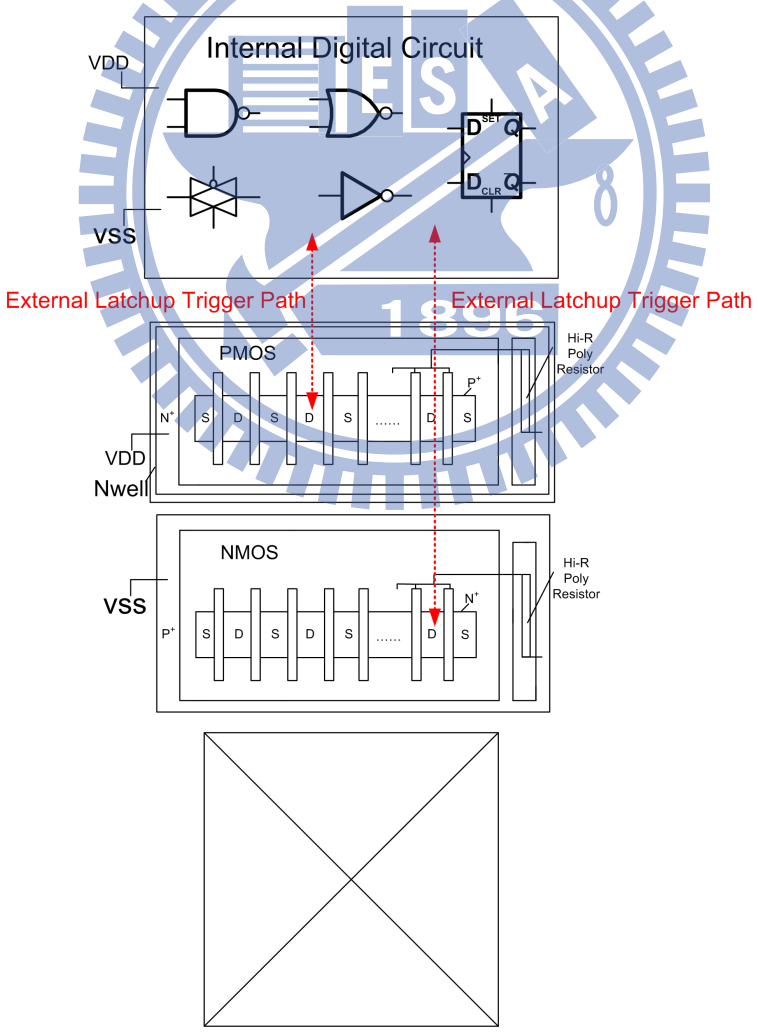


Fig. 3.2. The cell layout of input buffer with guard ring protection and common latch-up paths.

3.2 Latchup at Internal Circuits Induced by The Trigger Current at External Pins

In Fig. 3.3(a) and (b), the simplified cross-section views of traditional ESD-protection cell with guard rings at bulk terminals are shown. The depicted internal p-n-p-n structure represents the simulated detector formed in the internal digital circuits [31]. The related equivalent parasitics which contribute to the trigger of latchup at the internal p-n-p-n structure are also drawn in accordance with the external positive or negative I-test [15], [16]. When sufficient positive current is injected from the input pad as in Fig. 3.3(a), the parasitic $Q_{PNP}1$, $Q_{NPN}1$, and $Q_{PNP}2$ are turned on to pull high the ungrounded terminal of parasitic resistor Rpw. The internal p-n-p-n structure is thus triggered and causes latchup to happen. For negative current is applied at input pad as shown in Fig. 3.3(b) and turns on the $Q_{NPN}2$, the sink current will enlarge the emitter to base voltage of the effective PNP BJT at the

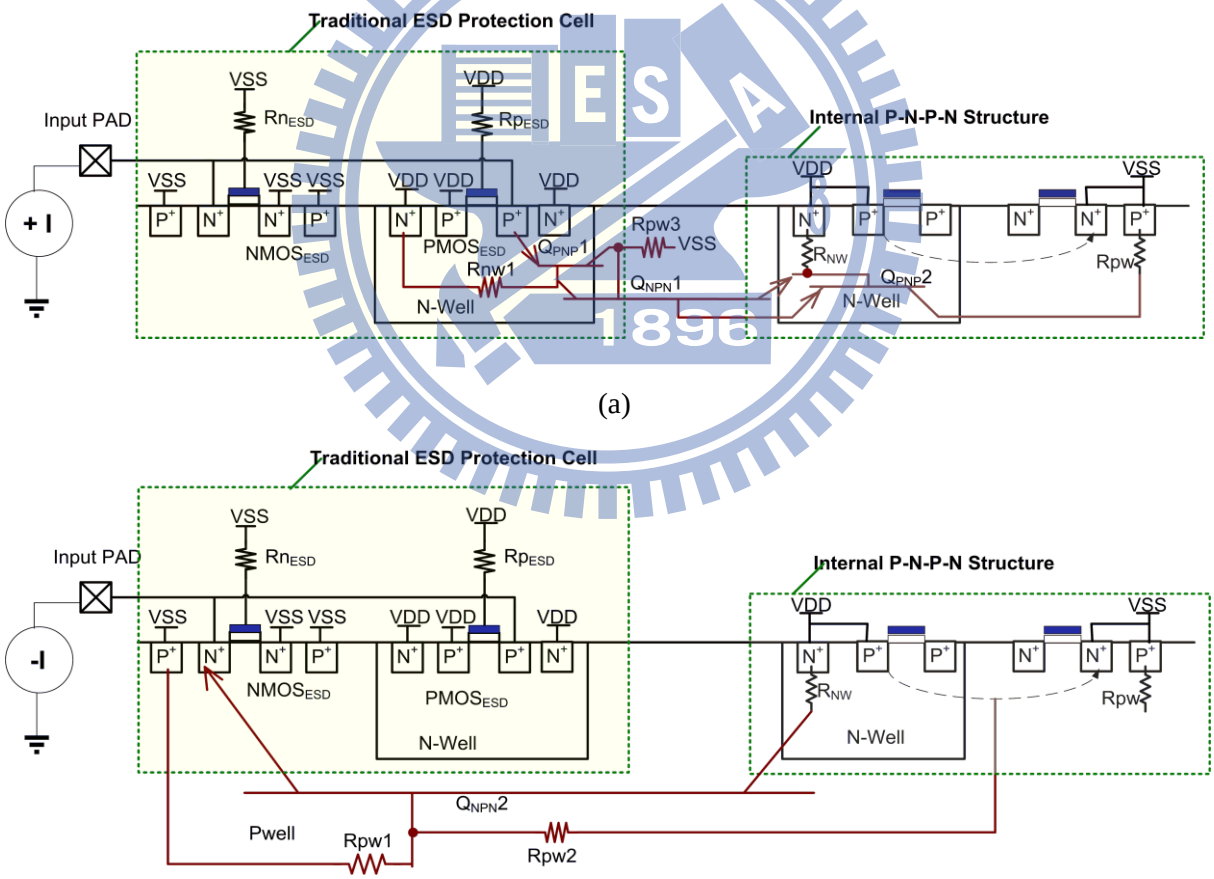


Fig. 3.3 Simplified cross-section views of traditional ESD-protection cell with guard rings to depict the related parasitic trigger paths to the internal P-N-P-N structure under (a) positive I-test and (b) negative I-test.

internal P-N-P-N structure. Once the voltage is over the threshold of the PNP BJT, latchup is fired. For the structures in Fig. 3.3(a) and (b), the conductivity of the body diodes formed between the source and the bulk rings affect the amount of the induced current toward the external transients.

The advantage for the guard ring protection is the easiness for implementation and less area consumption. However, from the experimental results in [3], the testkeys composed of I/O transistors with 500-µm total width, less than 60-µm distance from pmos to sensitive latch-up detector, and protected by 3-µm wide single guard ring perform less than 40-mA immunity for positive I-test in 0.35-µm silicided bulk CMOS process. The similar trends also happen in the analysis among LDMOS and CMOS structure within 2-µm CMOS high-voltage process. The used testkeys in [32] without extra isolation structure between the MOS cells and the internal P-N-P-N structure performs ~30-mA Latchup immunity which is much less than the 100-mA trigger current level in JEDEC standards. In practical design, the performance can be better or worse depends on the sizes of the guard rings, the arrangement of the locations, the doping concentrations of the process, and etc. The devices or junctions between the internal sensitive paths to the pad also affect the final results of external latch-up test for the IC product. Sometimes in high-voltage applications, improper layout arrangements may cause EOS problem induced by the latch-up I-test and thus degrade the expected performance for the designs with guard ring protection [24], [25], [33].

3.3 New Design to Generate Complementary Current Corresponding to External Triggers in Latch-up I-Tests

To enhance the Latchup immunity against the perturbations, a novel design is shown in Fig. 3.4(a). The main function for this structure is to wake up the ESD-protection transistors (Mnesd and Mpesd) during latch-up I-test. Additional junctions are added to build effective bipolar transistor structures Qn_sen and Qp_sen at the gate terminals of Mnesd and Mpesd. The Qn_sen and Qp_sen work as the sensors to detect the amount of latch-up trigger current. One of the layout implementations is shown in Fig. 3.4(b) with related cross-section view as shown in Fig. 3.5. In this case, the additional n+ and p+ junctions located outside the guard ring of Mpesd are planned to be the effective collector terminals of Qn_sen and Qp_sen. The emitter and the base of Qn_sen and Qp_sen are implemented with existing drain terminals of the Mnesd or Mpesd and the substrate or n-well with n+ OD junction as depicted in Fig. 3.5. The collectors are connected to 10-kΩ Hi-R poly resistors (Rnsed or Rpesd) and the gate

terminals of Mnesd or Mpesd, respectively. The operations for the proposed design under positive and negative I-test are shown in Fig. 3.6(a) and (b). The other intrinsic parasitic devices related to the latch-up triggered path are shown as $Q_{PNP}1$, $Q_{PNP}2$, $Q_{NPN}1$, $Q_{NPN}2$ which are also presented in the mentioned cross-section views at Fig. 3.3(a) and (b). When positive trigger current (Ipos_source) is applied from external source, the voltage of PAD is

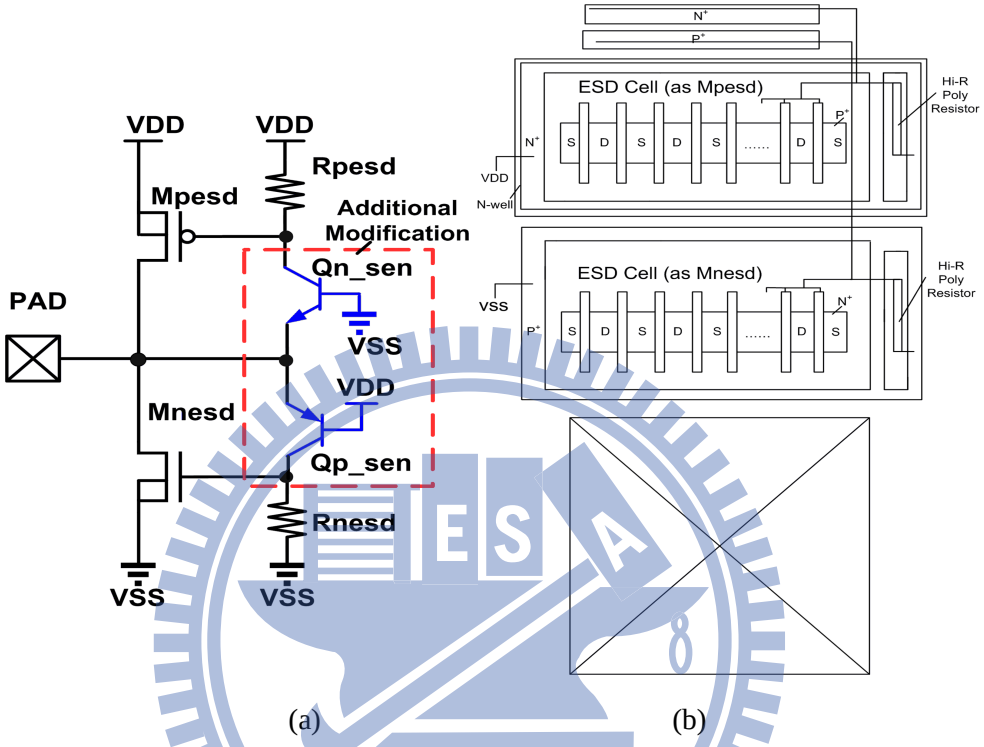


Fig. 3.4. (a) Schematic and (b) layout structure for the proposed design with additional modification.

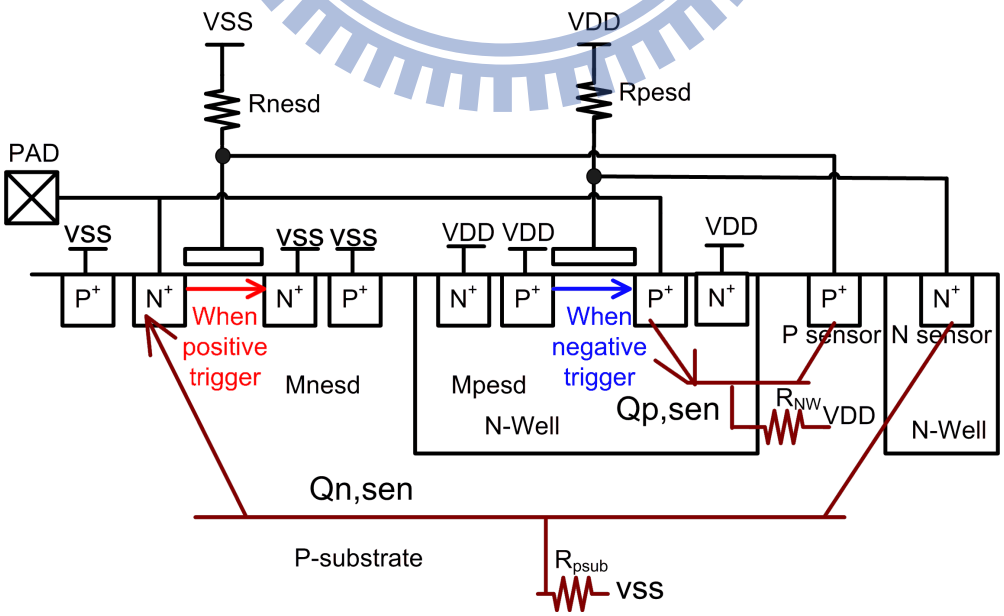


Fig. 3.5. Cross-section view for the proposed design.

pulled over the supply voltage VDD. Therefore, Qp_sen may be turned on and produces sensing current related to the voltage difference between PAD and VDD generated by the trigger current. The external source current separately flows in the chip and can be presented as the composition by

$$Ipos\_source \cong Isink + Ip\_sen + Idb + Ipos\_trigger \quad (3.1)$$

, where the Isink is the current sunk by the Mnesd, Ip_sen is the sensing current through Qp_sen, Idb is the drain to bulk current of Mpesd, and the Ipos_trigger is the trigger current flew to Rpw3a. If the Ipos_trigger is large enough to make the base voltage of NPN bipolar

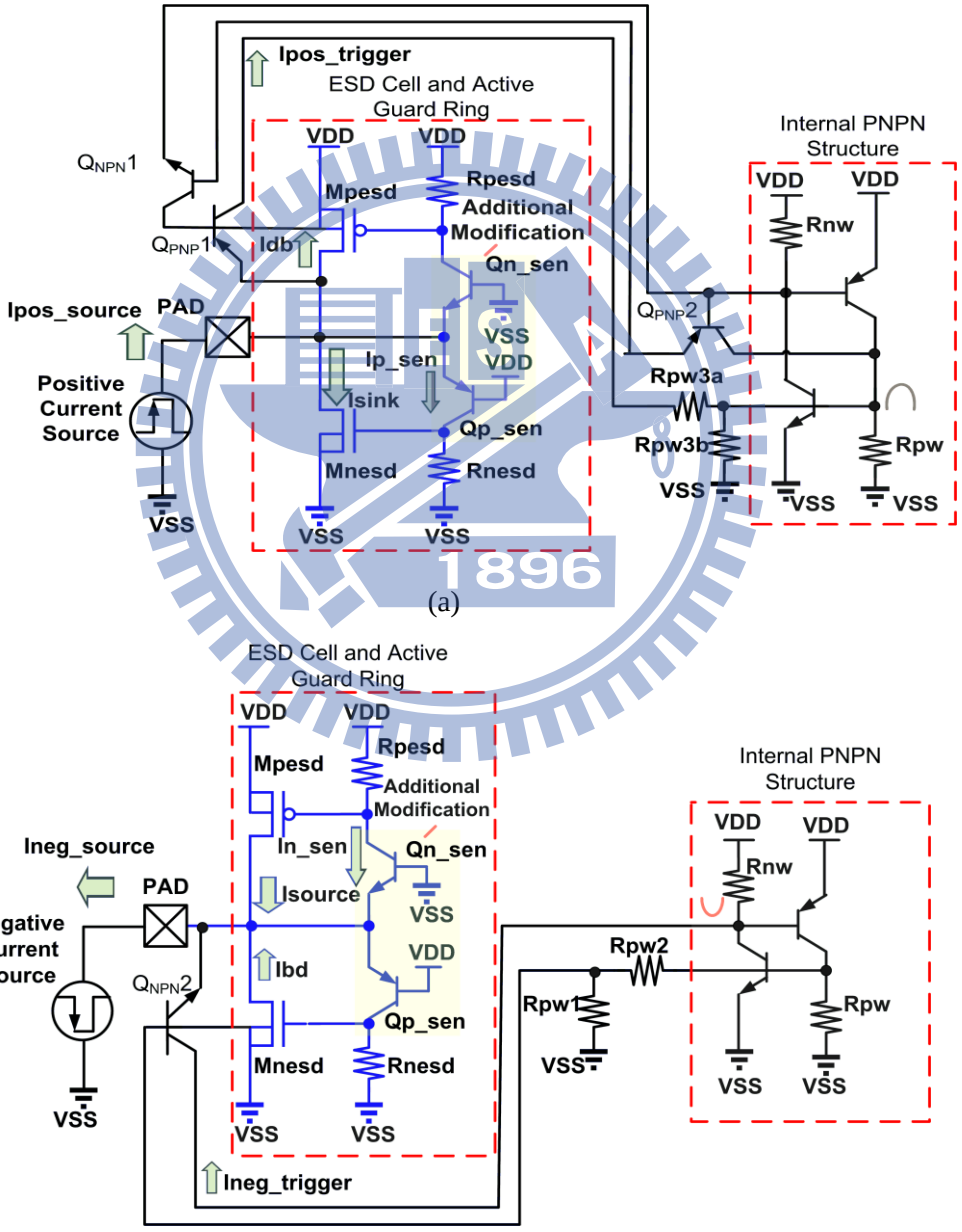


Fig. 3.6. Operations for the proposed design under (a) positive I-test and (b) negative I-test.

transistor in the internal P-N-P-N structure high enough, latchup will be induced. Since Isink shares part of current from external positive source together with Ipos_trigger, the amount of Ipos_trigger is reduced corresponding to same Ipos_source by enhancing the amount of Isink. If Ip_sen is sufficient to pull high the gate terminal of Mpesd and turn on the transistor, quite amount of Isink current can be produced depending on the sizes of the devices. Thus, the Latchup immunity to the positive I-test can be improved with increased Isink generated due to the additional modification. Similar situation is also shown in negative I-test. The trigger current sunk by the external source can be approximately decomposed to several parts as indicated in

$$Ineg\_source \cong Isource + In\_sen + Ibd + Ineg\_trigger \quad (3.2)$$

, where the Isource is the current sourced from the Mpesd, In_sen is the sensing current through Qn_sen, Ibd is the bulk to drain current of Mnesd, and the Ineg_trigger is the trigger current flew from $Q_{NPN}2$. Sufficient Ineg_trigger can bring about enough emitter-to-base voltage to turn on the effective PNP BJT of the internal P-N-P-N structure and thus lead to the occurrence of latchup. From equation (3.2), Ineg_trigger can be reduced apparently if Isource is increased due to the turn-on of Mnesd under same negative trigger current from the PAD. With relatively diminished Ineg_trigger, the proposed design has better performance than the original guard ring design.

3.4 Experimental Results

The proposed design has been verified with the 5-V CMOS devices embedded in a 0.5-μm 5V/15V/25V/40V BCD process. Although the proposed design was not verified with a pure 5-V technology, the proposed design will still work at the pure 5-V CMOS technology. The simplified graph for the structure to investigate the latch-up resistance of the previous and proposed works is shown in Fig. 3.7 [3]. The P-N-P-N cell is used to emulate the latch-up structure in general circuits at internal blocks and are repeatedly placed behind the testkeys. The specified distances (hn, hp, Xn, Xp) in each P-N-P-N cell are 35 μm, 35 μm, 20 μm, and 20 μm, which follow the typical suggested maximum values provided by foundry. Whether latchup is triggered in these cells or not in accordance with different trigger currents is affected by the test cell placed between the pad and the P-N-P-N cells. Thus, those P-N-P-N cells serve as internal latch-up detector to judge Latchup immunity of the testkeys. Fig. 3.8(a) shows the layout photo in the fabricated test chip contains mentioned test structures. Fig. 3.8(b) shows the enlarged layout graph for a test cell with proposed design in the tape-out

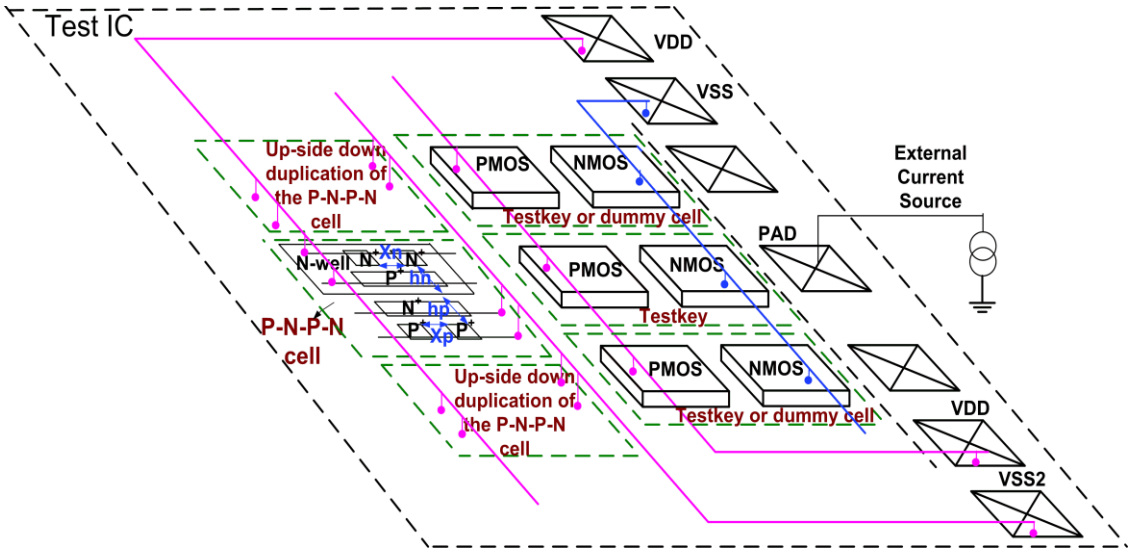
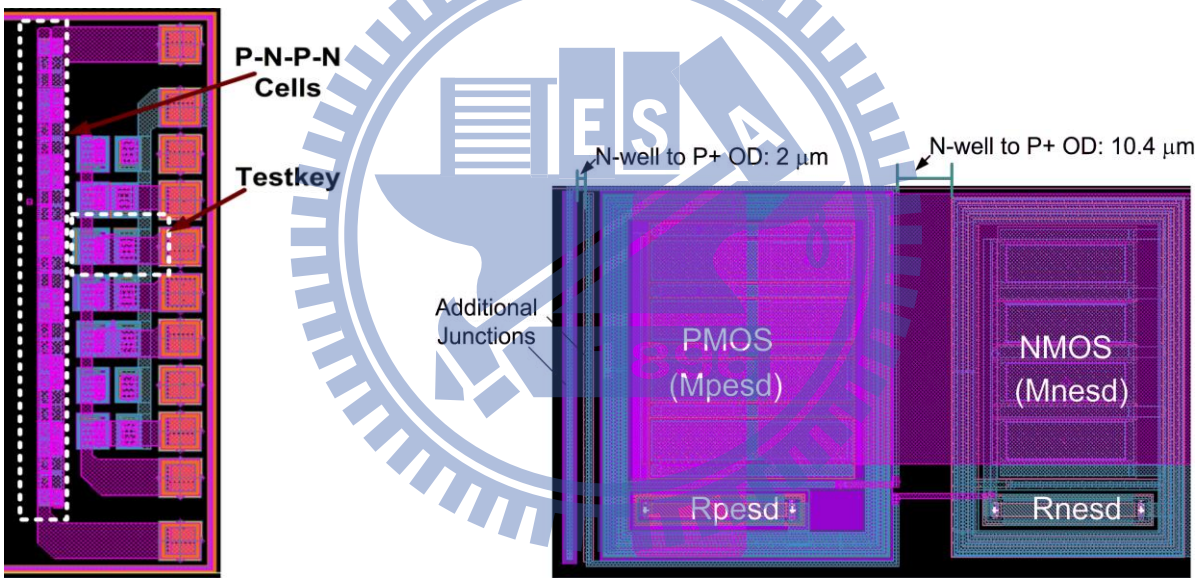


Fig. 3.7. Structure to verify the latch-up resistance of the previous and proposed works.

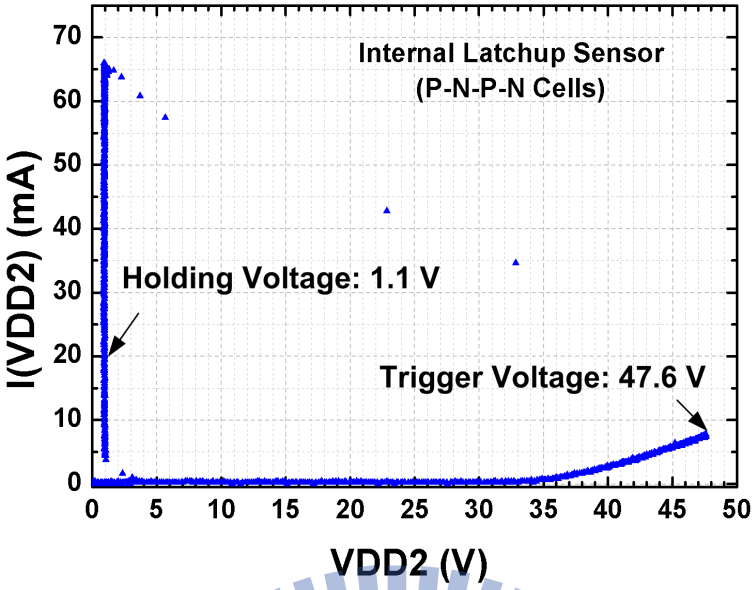


(a) (b)

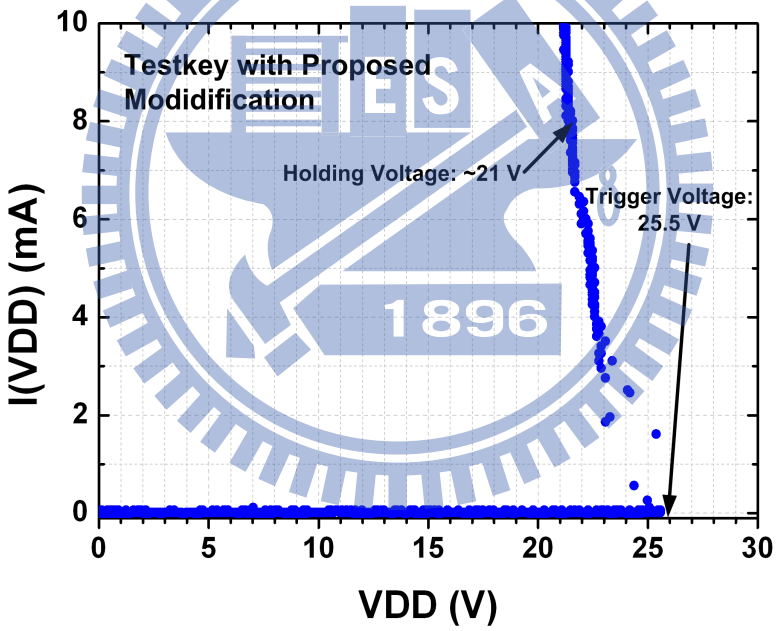
Fig. 3.8. Layout photo for (a) test chip and (b) testkey with proposed design.

chips. The additional junctions are drawn as wide to place one row of contacts on the OD strobes. The distance between the p+ and n+ rings is 10.4 μm and the distance between the testkeys and internal P-N-P-N cells is 30 μm.

The I-V characteristics of the inner P-N-P-N cells and proposed design are measured by the *Tek*370B curve tracer at room temperature. The trigger voltages of these P-N-P-N cells are near 47.6 V and the holding voltages are near 1.1 V as shown in the I-V curve in Fig. 3.9(a). The I-V curve of the proposed work is also presented in Fig. 3.9(b), where the trigger



(a)



(b)

Fig. 3.9. Measured latch-up I-V characteristics of (a) internal latch-up sensor and (b) testkey with proposed modification.

voltage is near 25.2 V and the holding voltage is near 21 V, respectively. The 47-V breakdown voltage is due to the junction breakdown between the n-well layer and the p-type substrate in the given high-voltage process. Besides, in the testkey, the I/O cell is implemented with 5-μm single guard ring around both Mpesd and Mnesd and the related distance between the bulk rings of Mpesd and Mnesd transistors is 10.4 μm. The 21-V high

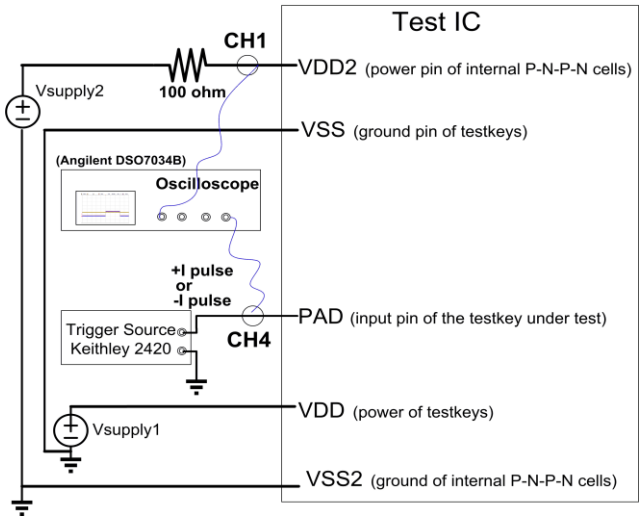
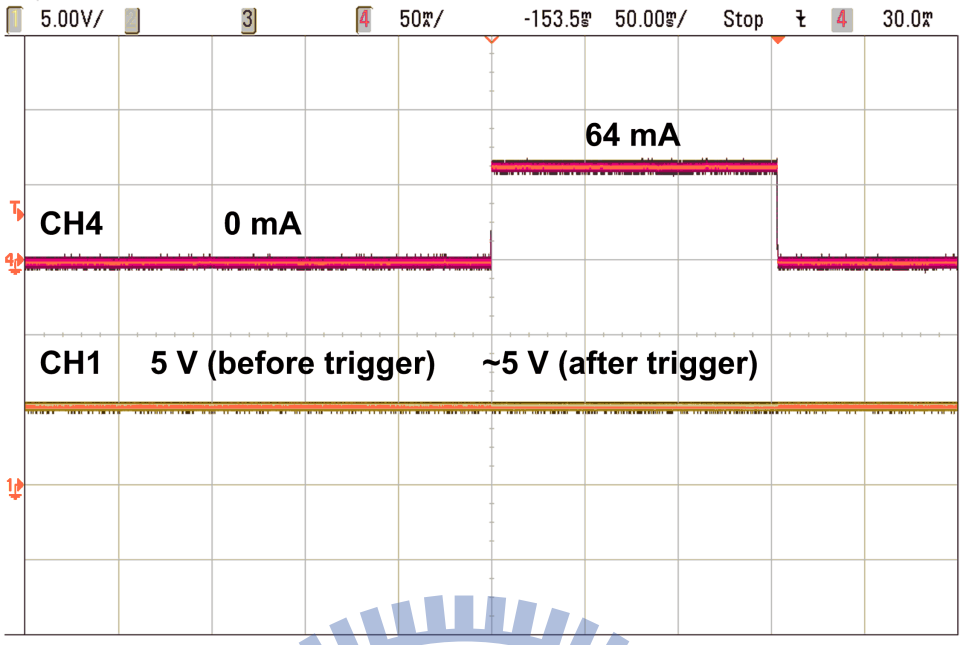


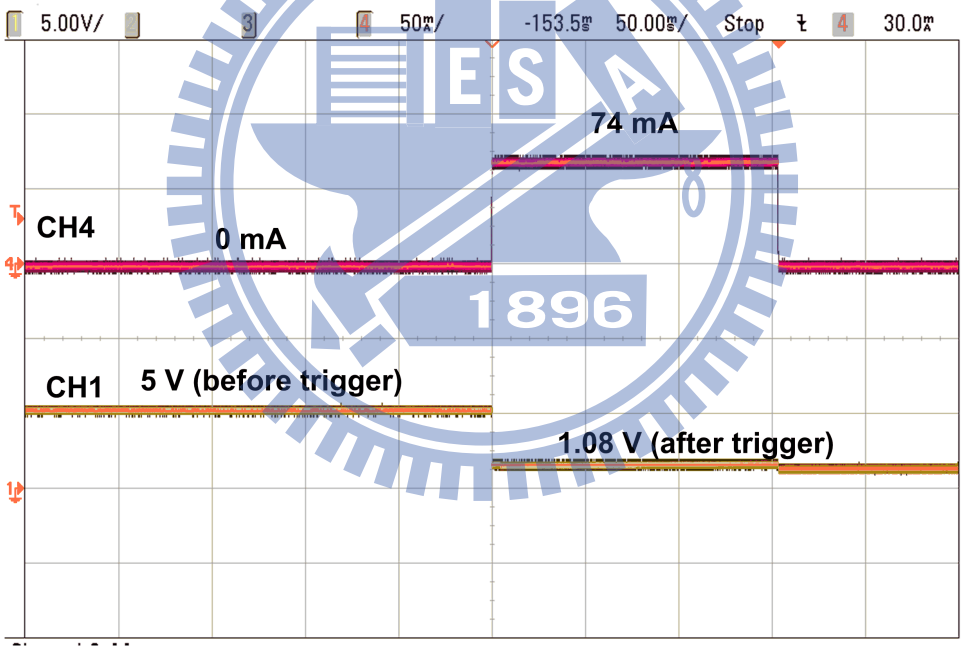
Fig. 3.10. Experimental setup to verify the latch-up resistance for previous art and the designs with proposed modification.

holding voltage of the parasitic SCR path (from VDD to VSS) in the I/O cell is due to the surrounding guard rings and sufficient distance for the PNPN path between the Mpesd and Mnesd in the adopted 0.5μm 5V/15V/25V/40V BCD process. The purpose of the high holding voltage in the I/O cell is to maintain latch-up free at the I/O cell, so that the latch-up performance can be judged accurately due to the triggering of the internal PNPN cells toward different external trigger current levels that applied at the I/O pad. The lathcup occurrence located in the internal circuit blocks (but not located at the I/O cell) was illustrated in Fig.3, when the positive/ negative trigger current is applied to the I/O pad.

The experimental setup to verify the latch-up resistance for the previous art and the design with proposed modification is shown in Fig. 3.10. The *Keithley* 2420 serves as required trigger current source and connected to the pad. Two dc power supplies (Vsupply1 and Vsupply2) are used to bias the supply voltages of test designs and P-N-P-N cells at 5 V, separately. A resistor of 100 Ω is connected between the external power supply and the supply pin of the internal P-N-P-N cells (VDD2) to limit the large latch-up current and avoid immediate damage in the experiments. Measured waveforms from oscilloscope for one implemented testkey with proposed design are shown as Fig. 3.11 and Fig. 3.12 for positive and negative I-test. The total widths for ESD protection PMOS and NMOS are 720 μm and 480 μm. Minimum lengths are also used as 0.6 μm and 0.7 μm for all the NMOS and PMOS in the test chips, respectively. When 64-mA positive trigger current (as CH4) is applied at PAD as shown in Fig. 3.11(a), the voltage at VDD2 (as CH1) keeps at ~5V since latchup is not happened and few current flows through the resistor. When larger trigger current is



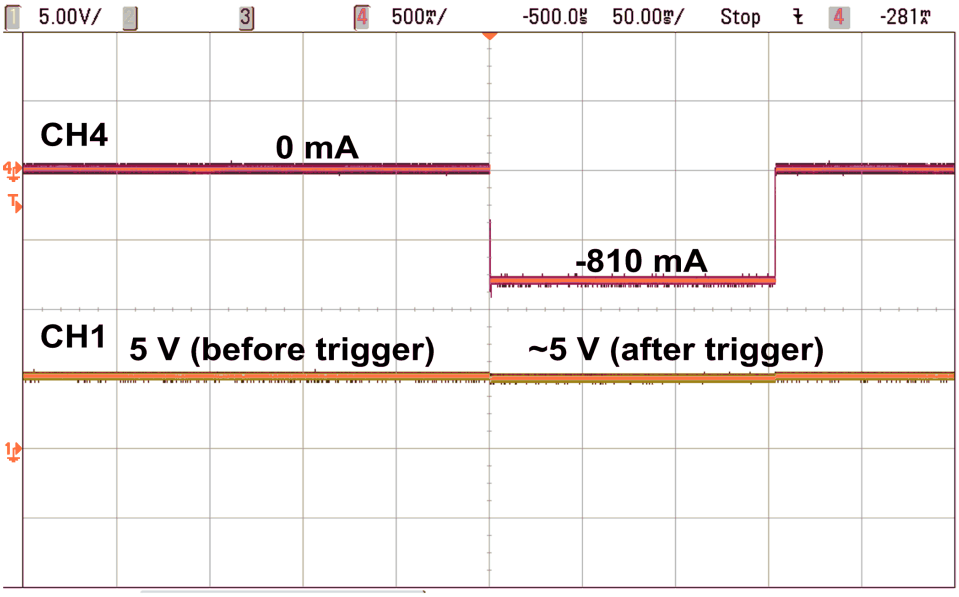
(a)



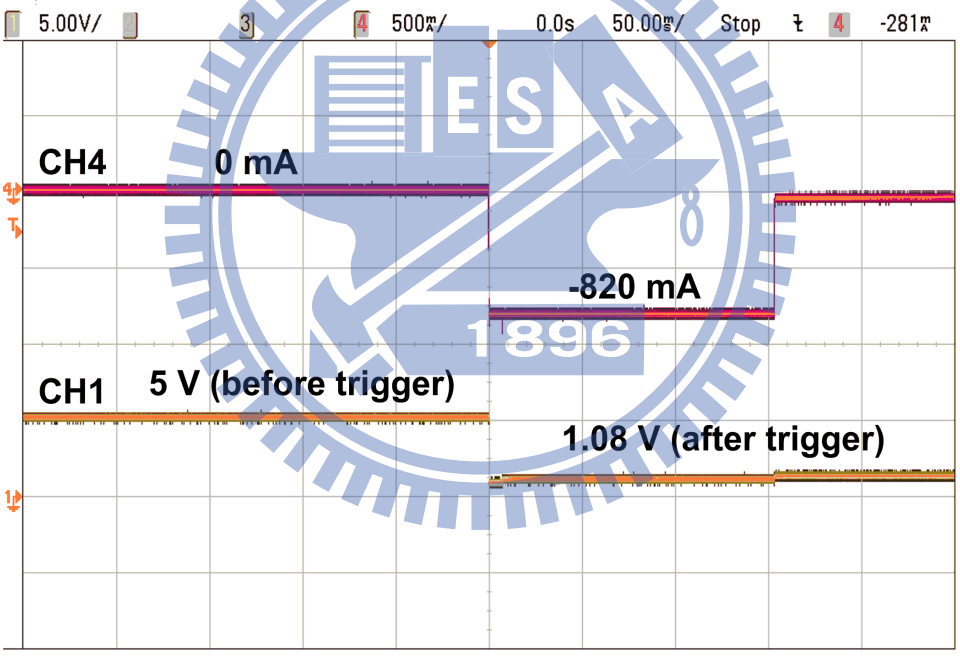
(b)

Fig. 3.11. Measured waveforms of proposed design under positive I-test with (a) 64-mA and (b) 74-mA trigger current applied at input pad.

applied as 74 mA as shown in Fig. 3.11(b), the voltage at VDD2 drops suddenly and keeps near 1.08 V which means latchup happens at the internal P-N-P-N cells. For negative I-test presented in Fig. 3.12(a) and (b), the latchup doesn't happen when -810-mA trigger current is applied while it is occurred as -820-mA current pulse is provided at input pad. With intrinsic



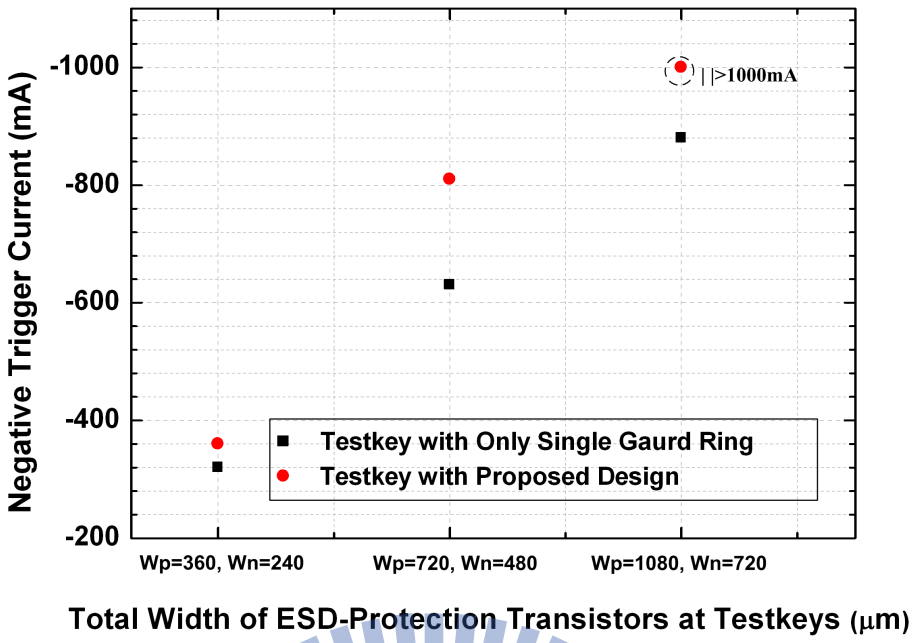
(a)



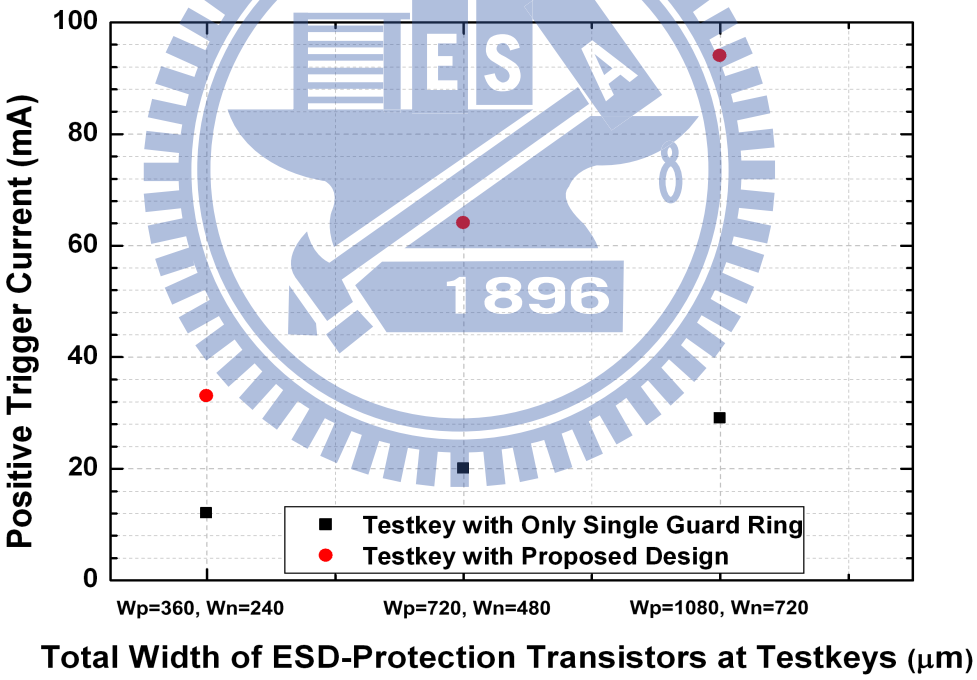
(b)

Fig. 3.12. Measured waveforms of proposed design under negative I-test with (a) 810-mA and (b) 820-mA negative trigger current applied at input PAD.

NPN BJT from the drain terminal of Mnesd to the bulk terminal of Mpesd as current provider and inherently farer distance between internal latch-up sensor to NMOS than to PMOS, the proposed design and the prior art tolerate higher trigger level in negative I-test than in positive I-test. Further organizations for the trigger current to fire latchup and the relations with the dimensions of the ESD-protection transistors in the testkeys are shown in Fig. 3.13(a)



(a)



(b)

Fig. 3.13. Relations between the applied trigger current at input pad to fire latchup and the dimensions of the ESD-protection transistors used in the testkeys (with only single guard ring and with proposed design) under (a) positive I-test and (b) negative I-test.

and (b). The designs with proposed modification has higher Latchup immunity compared with the previous art with only single guard ring at both positive and negative I-test. For total widths as Wp=360 μm and Wn=240 μm, the proposed design can sustain up to ~32-mA

positive current and 360-mA negative current without encountering latchup while the previous art can only tolerate ~13-mA positive trigger current and ~320-mA negative trigger current. When the transistor dimensions are largr, the sustainable current is also increased. For the proposed design with Wp=1080 µm and Wn= 720 µm, the trigger current to induce latchup can be up to ~94 mA and larger than 1000 mA for positive and negative trigger current, respectively. The HBM (human body model) ESD robustness under different pin combinations of ESD test on the I/O pin [34] is also examined and shown in Table II for the testkeys with Wp=360 µm and Wn=240 µm. The weakest mode is ND mode with 3-kv performance and 8-kv performance is achieved in the NS and PD mode. Since the tolerated levels for the listed ESD modes are similar at both designs, it is verified that the additional modification can improve the Latchup immunity without degrading the ESD performances. Besides, the area consumption for the testkey with only single guard ring is 127.57µm*81.09µm while the area for the proposed design is 135.97µm*81.09µm. According to above data, the testkey with the proposed design only slightly larger than the design with single guard ring due to the 6.5% increment.

TABLE 3.1
ESD TESTS OF HBM MODE FOR TESTKEYS

ESD MODE	Types for Testkeys	
	Testkey with Only Single Guard Ring	Testkey with Proposed Design
Positive-to-VSS mode (PS mode)	5.5 kV	5.5 kV
Negative-to-VSS mode (NS mode)	>8 kV	>8 kV
Positive-to-VDD (PD mode)	>8 kV	>8 kV
Negative-to-VDD (ND mode)	3 kV	3 kV

3.5 Summary

The presented design shows an embodiment to activate the existing ESD devices by additional junctions when latch-up current perturbations are applied. With ESD-protection PMOS and NMOS transistors sized as 1080 µm/0.7 µm and 720 µm/0.6 µm for the total width/length, the testkey with proposed design can tolerate ~94-mA positive trigger current and larger than 1000-mA negative trigger current compared with ~29-mA positive and ~890-mA negative current performance for the testkey with only single guard ring protection. The enhancement can be more if the driving abilities of the ESD-protection transistors are improved. The novel design can be combined with the traditional guard ring designs to offer higher Latchup immunity and has been successfully verified in 0.5-µm CMOS process without degradation in ESD levels.

Chapter 4

Active Guard Ring to Improve Latchup immunity

A new design concept named as active guard ring and related circuit implementation to improve the latchup immunity of integrated circuits (IC) are proposed. By using additional sensing circuit and active buffer to turn on the ESD protection transistors, the large-dimension ESD (or I/O) devices can provide or receive extra compensation current to the negative or positive current perturbation during the latch-up current test (I-test). The new proposed solution has been verified in 0.6-um 5-V process to has much higher latch-up resistance compared with the conventional prevention method of guard ring in CMOS technology.

4.1 Introduction

A depiction for the traditional latch-up prevention with guard rings in typical CMOS IC is shown in Fig. 4.1. There is a parasitic PNPN path (latch-up path) formed from the VDD-connected source (P+ diffusion) of PMOS to the VSS-connected source (N+ diffusion) of NMOS in the logic gates of internal circuits. Under the trigger of external current source, there is substrate current flew in or out of the internal circuits corresponding to positive or negative pulse applied at I/O PAD. Such substrate current is the main activator for the occurrence of latchup. With the guard ring surrounding the I/O buffer or ESD protection transistors, certain amount of the latch-up trigger current can be absorbed or released without causing latch-up occurrence at the internal circuits. Nevertheless, the tolerance toward the trigger current is related to the width of guard ring and the distance to the internal latch-up paths. To further enhance the tolerance for latch-up trigger current, methods as mentioned in chapter 1 [5]-[20] had been also proposed. Even if high latchup immunity can be achieved by carefully implemented with special designs, to save the fabrication cost without using extra layers or reducing the width of guard rings are still requested by IC industry.

In this work, an active structure with existing ESD devices to increase the resistance against latchup is proposed and named as “active guard ring”. The ESD-protection NMOS

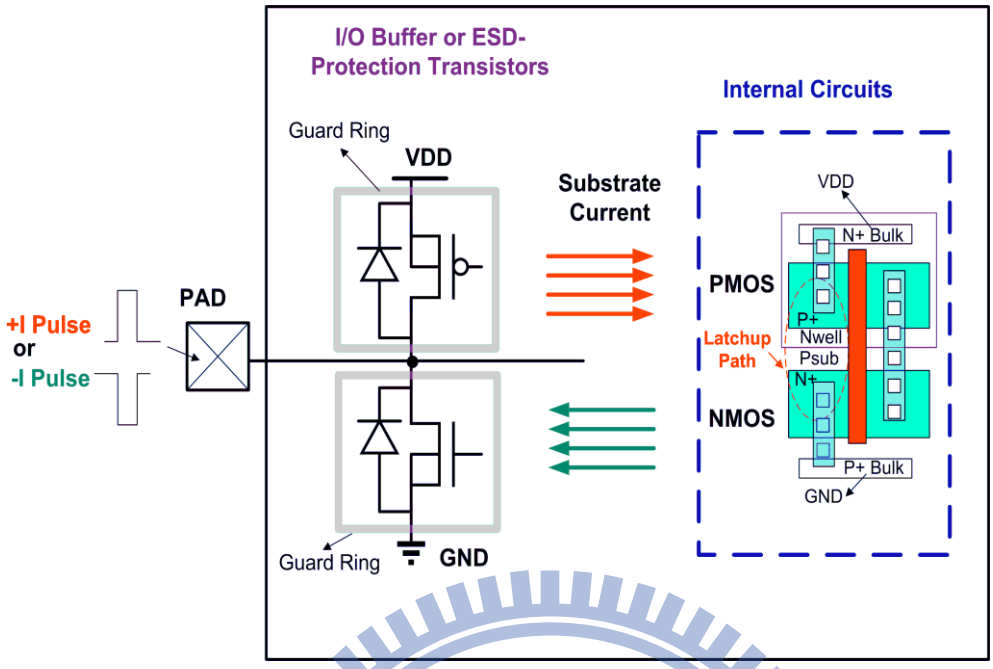


Fig. 4.1. Traditional latch-up prevention in CMOS IC with guard rings to surround the I/O and ESD protection transistors.

and PMOS transistors work not only during ESD stress but also at the latch-up trigger conditions through the help of circuit technique. The concept of "active guard ring" and the novel circuit implementation has been proposed and successfully verified in silicon chip.

4.2 Test Structure and The Latchup immunity of Traditional Design with Guard Ring

Fig. 4.2 shows the brief depiction of the test structure and the related setup with external equipments referenced from [3], [20]. For the test structure, it contains the testkeys and the PNPN cells. The testkeys are composed of large-dimension NMOS and PMOS with guard ring surrounding. The internal PNPN cells work as latchup immunity sensors to investigate the performance of the designed testkeys. The latch-up sensitivity of the internal PNPN cells toward the external trigger source is affected by the structure of the testkeys, as well as the distance between the testkeys and the PNPN cells. The I-V curve of the internal latch-up sensors are measured by the curve tracer (*Tek* 370B) from the VDD2 and VSS2 pads. The measured result is shown in Fig. 4.3. Since the holding voltage is near 1.1 V, large current is generated when latchup happens under 5-V power supply. Thus, the occurrence of latchup can be observed by monitoring the current or voltage condition at VDD2.

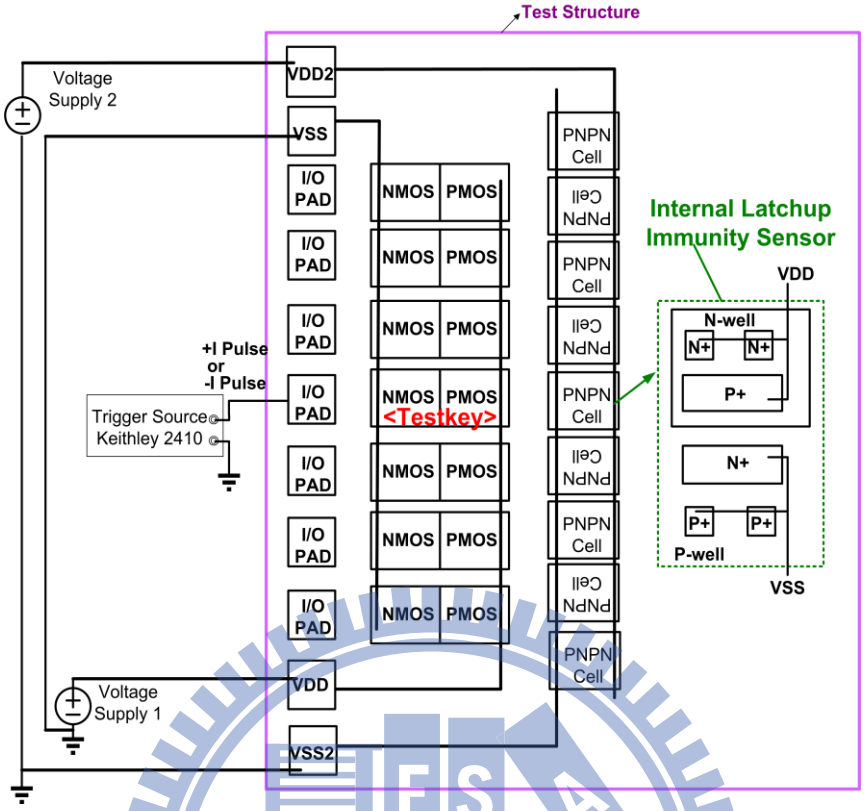


Fig. 4.2. Test structure to investigate the performance of latch-up prevention.

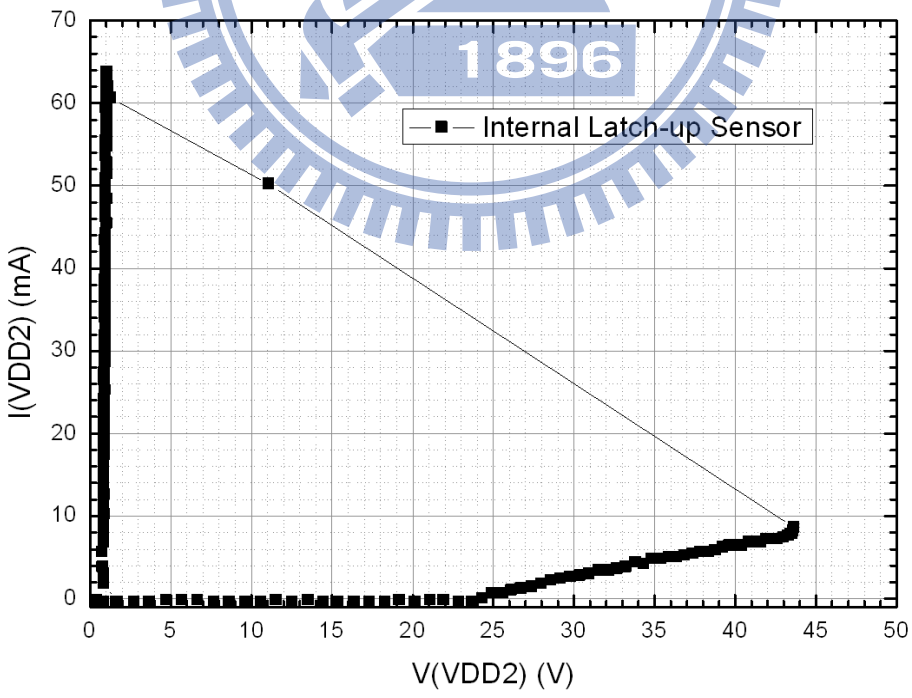
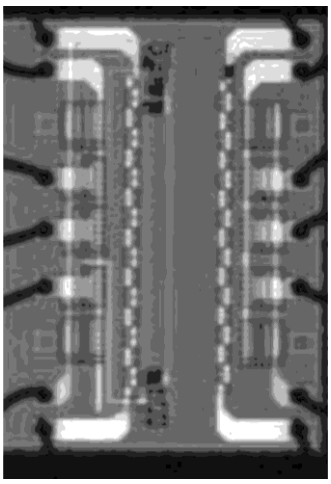
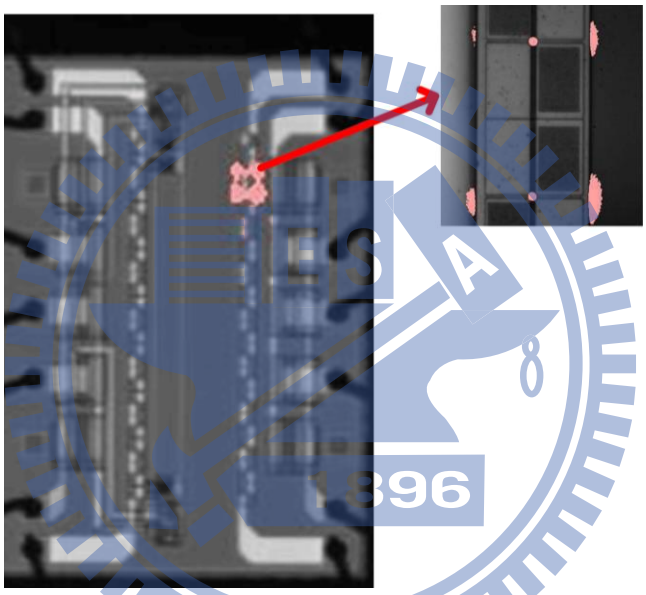


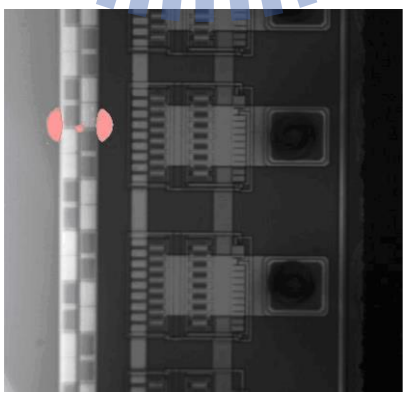
Fig. 4.3. Measured I-V curve of the internal sensor to show the latch-up characteristics, which has a holding voltage of 1.1 V.



(a)



(b)



(c)

Fig. 4.4. (a) Chip photo of the latch-up test structure. (b) EMMI picture on the damaged chip after 5-mA positive current pulse was applied. (c) EMMI picture on the damaged chip after 270-mA negative current pulse was applied.

Some test chips had been fabricated in a 0.6-μm 5-V CMOS process to investigate the performance of the previous work with guard ring [3]. To examine the performance of the test chips, the I/O PAD of testkey under test is applied with trigger current pulse of ~150 ms provided by the Keithley 2410. Besides, the supply voltage (VDD) of the testkeys is given to 5 V and the supply voltage (VDD2) of the PNPN cells is also connected to 5-V voltage source at room temperature, respectively. EMMI analysis is took, after the current pulse is applied to the I/O PAD to investigate the latchup immunity level, to show the location of the abnormal current. Fig. 4.4(a), (b), and (c) show the EMMI pictures after positive or negative trigger current is applied to the I/O PAD. The normal chip photo without any hot spot which also means no abnormal current is shown in Fig. 4.4(a) after 4-mA positive current or 250-mA negative trigger current pulse was applied. The EMMI pictures for the damaged chip after experienced 5-mA current pulse or 270-mA negative current pulse are shown in Fig. 4.4(b) and Fig. 4.4(c), respectively. From the hot spots in Fig. 4.4(b) or Fig. 4.4(c), the abnormal current is attributed to the PNPN path of the latch-up sensor. With the observed results, the traditional work with guard ring has weaker performance in the positive I-test. The tolerance level of the fabricated previous design is even less than 50 mA, which is clarified as the lowest level specified in the JEDEC standard [4].

4.3 Latch-Up Prevention by Active Guard Ring

4.3.1 Concept and Circuit Implementation

Fig. 4.5 shows the concept denominated as “active guard ring” proposed in this work to reduce the injected current that triggers latchup at the internal circuits when latch-up I-test is applied at the I/O pad. Besides of the traditional prevention method with guard ring to surround the I/O buffer and ESD-protection transistors at the I/O pad, the proposed active guard ring design with the adopted circuits actively provides extra sink or compensation currents (Isink and Icomp) corresponding to positive or negative I-test, respectively. The structure for active guard ring is composed of a sensing circuit block and an active buffer. To generate sufficient sink or compensation current without paying the cost of extra silicon area, the existing large-dimension ESD-protection NMOS and PMOS transistors are also adopted as major supporters to the mentioned sink or compensation current. The sensing circuit block is used to monitor whether the positive or negative current pulse is applied. Once the positive or negative trigger current is large enough, the sensing circuit will inform the active buffer

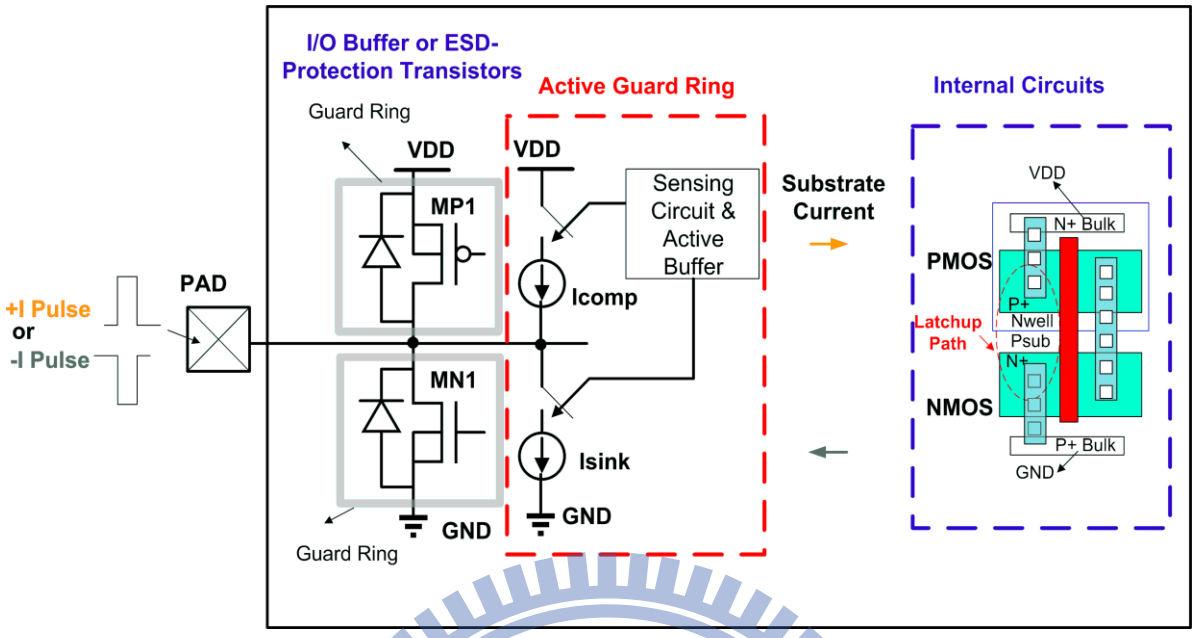


Fig. 4.5. Concept of "active guard ring" to reduce the injected substrate current at the latch-up path of internal circuits during latch-up I-tests.

about the strength of the applied current perturbation at PAD. The active buffer will then control the gate voltages of the large dimension ESD devices to generate the corresponding sink or compensation current.

The circuit implementation to realize the concept of active guard ring is presented in Fig. 4.6(a) and (b). In Fig. 4.6(a), the main embodiment includes the ESD devices (MP1 and MN1), a sensing circuit block, and an active buffer. The sensing circuit block is composed of MPS1, MNS1, RSN, and RSP to detect the information of the trigger current pulse. Besides, the MPS2, MN6, and MN7 are included in the block to mirror the detection results to the active buffer. The active buffer contains driving stages for MP1 and MN1, respectively. To control the gate voltage of MP1 (Vg_mp1), devices as MP2, MP3, MN2, and MN3 are adopted as that shown in Fig. 4.6(a). For the gate driver of MN1, it is made of MP4, MP5, MN4, and MN5.

In normal circuit operation condition without the external latch-up trigger source, the induced current by sensing circuit block is quite small to let MN2/MP4 has much weaker sink/ source force compared to the designed reference source/sink force provided by MP2/MN4. Therefore, the gate voltage of MP1 (Vg_mp1) or MN1 (Vg_mn1) is pulled to high/low to turn off the MP1/MN1.

The reference current force at MP2/MN4 can be generated by connecting VP1/VN1 to a traditional bias current circuit if it exists in the internal circuits. However, instead of the need for a traditional bias current circuit, a series of diode-connected MOS transistors shown in Fig. 4.6 (b), which is composed of MPD1 to MPD5 and MND1 to MND2, can provide the required voltages for VP1, VN1, and VPSG. Since the absolute threshold voltage of the designed PMOS MPD5 is much higher than the threshold voltage of NMOS MN1, even few quiescent current in MPD5 can generate sufficient reference current force in MN4. With the device sizes used in the simulation as described in section 4.3.2, the absolute threshold voltage for MPD5 (|Vthp|) is 0.964 V compared to 0.775 V for MN4 (Vthn). Besides, the summation of the threshold voltages of MPD1 and MPD2 is higher than MP2, so that small current in the diode-connected string makes enough reference current force in MP2. Moreover, the gate terminal of MPS1 (VPSG) is connected to the drain terminal of MPD1 to have a voltage slightly smaller than supply voltage VDD for quickly acting after the external trigger currents are applied. The number of stacked diode-connected MOS transistors is decided by the concern to have small quiescent standby current within the total quiescent current budget.

The detailed operations for the proposed active guard ring during positive and negative I-test are shown in Fig. 4.7(a) and (b), respectively. In Fig. 4.7(a), when sufficient positive current pulse is applied, the voltage at the PAD is raised up with the value over VDD. In such condition, there is current flow from the drain terminal to the bulk terminal of the MP1 (Idb_p) which is a normal path in traditional design. However, since the VPSG is slightly smaller than VDD, the source-to-gate voltages of MPS1 and MPS2 are also large enough to generate corresponding channel currents when PAD voltage is enough larger than VDD. The gate voltages of transistor MN5 and MP3 are thus pulled high and low, respectively. The current mirror, MN3 and MN2, then mirrors the current of MP3 to compare with the current sourced from transistor MP2. Once the mirrored current is larger, the gate voltage of MP1 (Vg_mp1) is pulled low to turn on transistor MP1. Thus, the related source-to-drain current (Isd_mp1) is generated. Similarly, with the assistants of MP5 and MP4, there is also a mirrored current from MN5 to be compared with the drain current of MP4.

While the mirrored current is larger, the gate voltage of MN1(Vg_mn1) is pulled high. Therefore, the transistor MN1 is turned on and produces the related drain-to-source current (Ids_mn1). Due to the generation of Isd_mp1 and Ids_mn1, the amount of the drain-to-bulk current of MP1 (Idb_mp1) and the substrate current injected to the internal circuits are reduced, and thus improves the latchup immunity against the positive I-test.

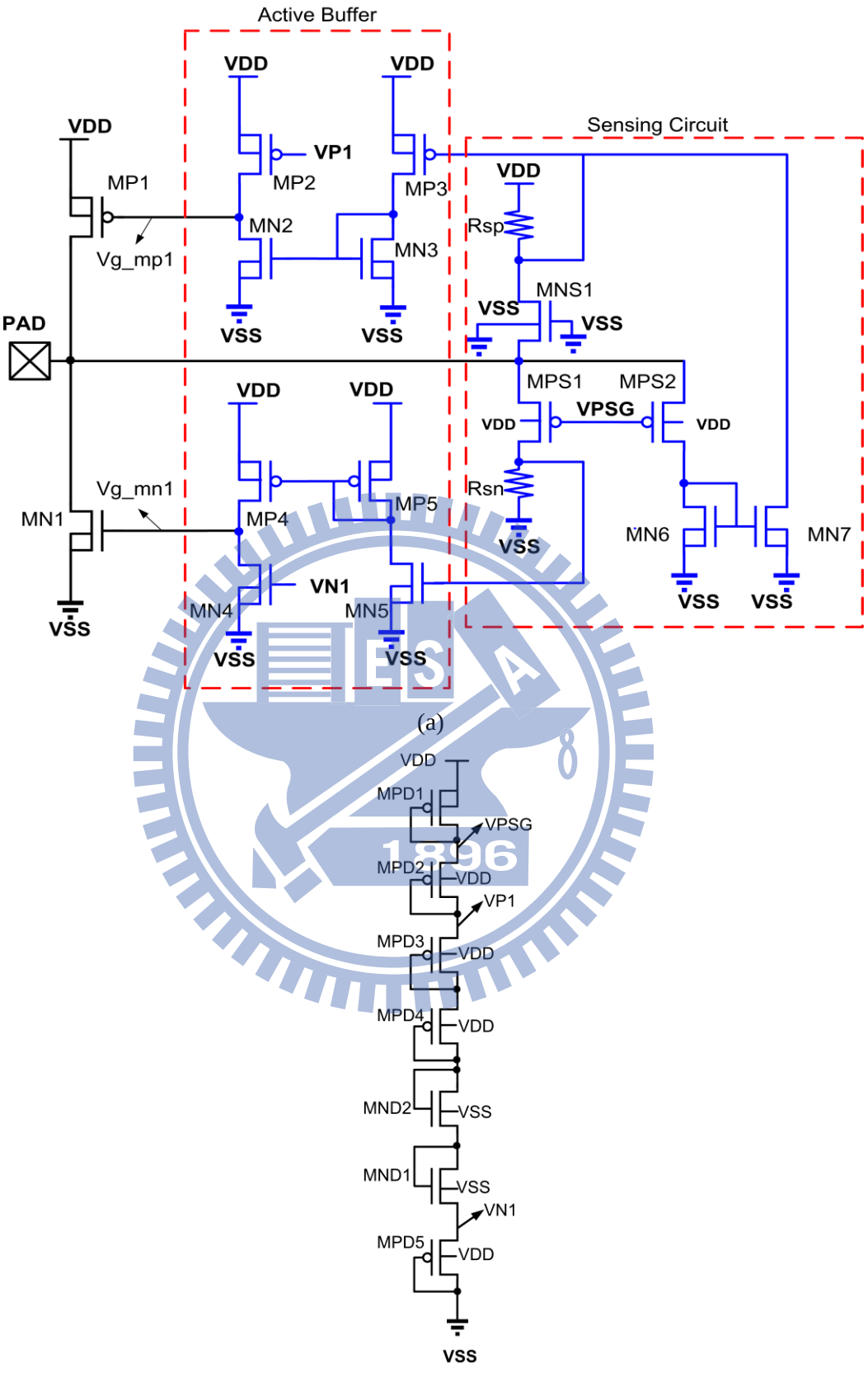


Fig. 4.6.(a) Circuit structure to implement the concept of active guard ring , and (b) the diode-connected MOS string to generate the required voltage biases for VP1, VN1, and VPSG.

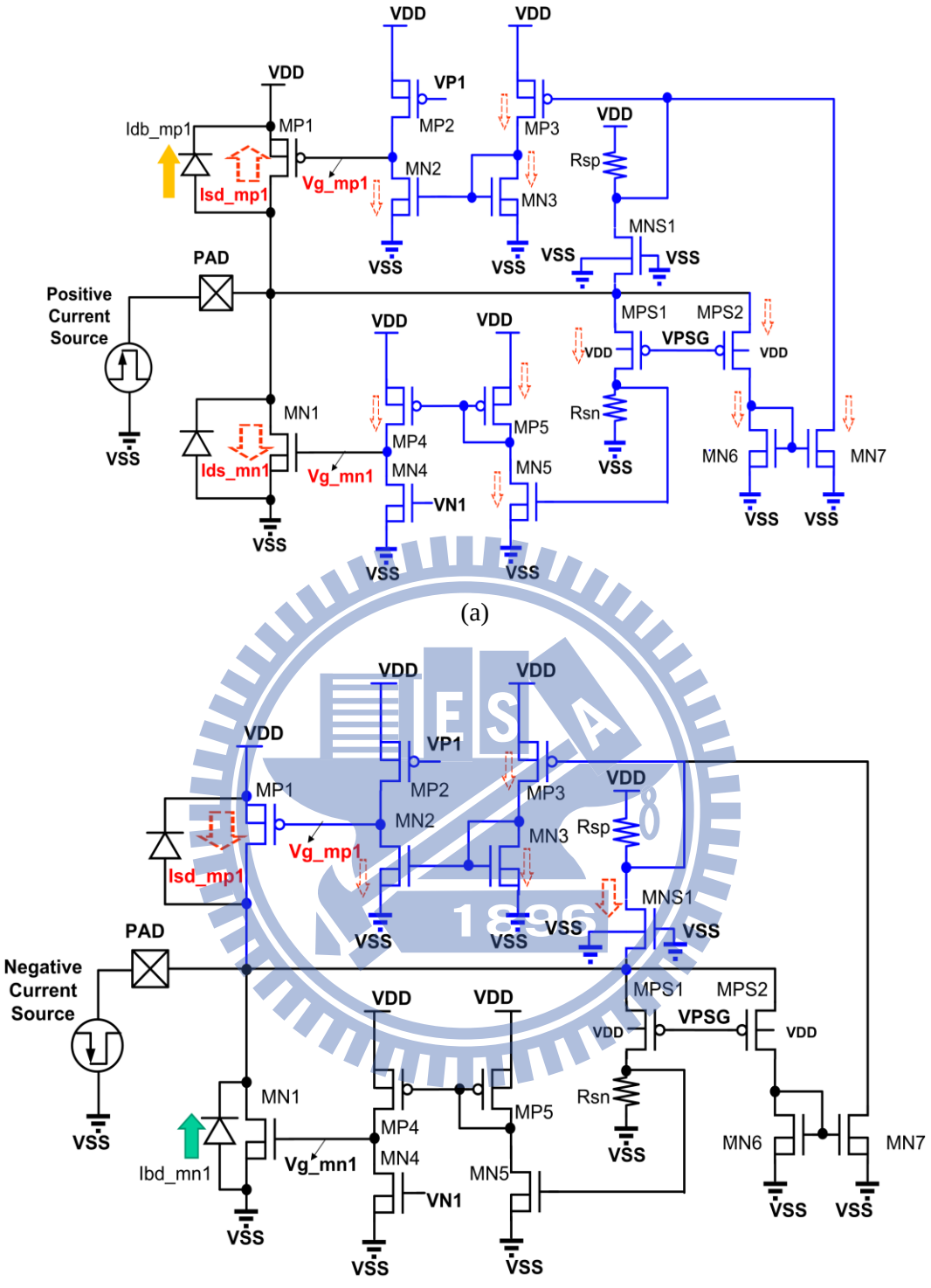


Fig. 4.7. Operations of the proposed work during (a) positive and (b) negative I-test.

When sufficient negative current pulse is applied as depicted in Fig. 4.7(b), the PAD voltage is pulled down to lower than Vss and induces certain current at drain terminal of MNS1. The related voltage difference across the resistor Rsp is thus pulled down the gate voltage of MP3 to generate the corresponding channel currents in transistor MP3 and MN3.

The transistor MN3 then mirrors a current to transistor MN2. If the current flew in MN2 is larger than the current flew from MP2, Vg_mp1 is pulled low to turn on the transistor MP1. Certain amount of current is generated and depicted as Isd_mp1 to compensate the negative I-test current at the pad. Thus, the bulk-to-drain current of MN1 (Ibd_mn1) and the substrate current injected to the internal circuits are reduced. Since the latchup immunity under negative I-test is intrinsically higher as presented in section 4.2, simpler structure to only turn on transistor MP1 is enough.

The proposed work can be co-designed with the power-rail ESD clamp circuit [35] to achieve the whole-chip ESD protection. Once the ESD stress is applied under the PS (ND) modes, the parasitic drain-to-bulk diode or the channel of MP1 (MN1) can conduct the ESD current to the floating VDD (VSS) line and then to the grounded VSS (VDD) through the power-rail ESD clamp circuit. Thus, even adopted with the active guard ring structure, the ESD performance is not degraded with the help of the power-rail ESD clamp circuit.

4.3.2 Simulation

The simulated results in a given 0.6-μm 5-V CMOS process on the proposed "active guard ring" are done by doing a dc sweep at the PAD voltage from -1 V to 6 V under room temperature. The device dimensions of the used transistors and resistors to verify this work are listed in Table 4.1 and Table 4.2. The simulated waveforms for Vg_mp1, Vg_mn1, Isd_mp1, and Ids_mn1 are presented in Fig. 4.8. Since the Vg_mp1 is pulled low and the Vg_mn1 is pulled high while the pad voltage is above 5.73 V, transistor mp1 and mn1 are verified to be turned on. The mentioned sink currents are generated as Isd_mp1 of 65 mA and Ids_mn1 of 200 mA under the pad voltage of 5.73 V, respectively. When the positive trigger current is applied to pull the PAD voltage high enough, those sink currents will help to hold back the increase of PAD voltage. Thus, less substrate injected current flows to the internal circuits.

When the PAD voltage pulls low to beneath -0.63 V, Isd_mp1 of 194 mA is induced as shown in Fig. 4.8. The compensation current increases the PAD voltage against the increase of negative I-test current. The simulated curve of the current from supply voltage I(VDD) according to the variation of the PAD voltage is also shown in Fig. 4.9. From the result in Fig. 4.9, the current of supply voltage I(VDD) is below 1 nA with PAD voltage ranging from 0 to 5 V. Moreover, I(VDD) is less than -1.07 μA and 1.2 μA for PAD voltage ranging from 5 to 5.44 V and 0 to -0.51 V, respectively.

TABLE 4.1

DEVICE DIMENSIONS OF THE TRANSISTORS USED IN THE SILICON VERIFICATION

Circuit Block	Device	(Width*M)/Length
ESD Devices	MP1	(45 μm*18)/0.6 μm
	MN1	(30 μm*18)/0.6 μm
Active Buffer	MP2, MP3	(1.3 μm*1)/0.6 μm
	MN2, MN3	(1.3 μm*2)/0.6 μm
	MP4, MP5	(1.3 μm*3)/0.6 μm
	MN4, MN5	(1.3 μm*1)/0.6 μm
Sensing Circuit	MNS1	(30 μm*2)/1 μm
	MPS1, MPS2	(45 μm*2)/1 μm
	MN6	(5 μm*1)/5 μm
	MN7	(5 μm*1)/0.6 μm
Diode String	MPD1, MPD3	(1.6 μm*3)/1 μm
	MPD2, MPD4, MND1, MND2	(1.6 μm*1)/1 μm
	MPD5	(2 μm*2)/1 μm

TABLE 4.2

RESISTORS USED IN THE SILICON VERIFICATION

Resistor in the Sensing Circuit	Resistance
Rsp	100 kohm
Rsn	100 kohm

More detailed simulated supply currents I(VDD) under the different temperatures and pad voltages for the design without or with the proposed active guard ring are summarized in Table 4.3. From the results in Table 4.3, the proposed design that is able to effectively enhance the latchup immunity has been verified to only consume little quiescent standby current.

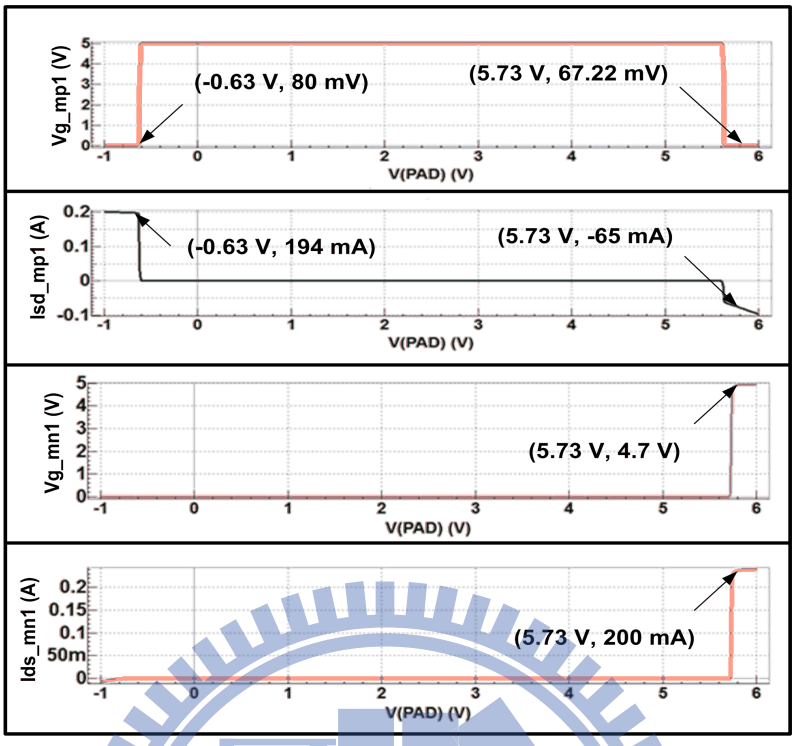


Fig. 4.8. Simulated waveforms of certain voltages and currents in this work with dc sweep at the PAD voltage from -1 V to 6 V.

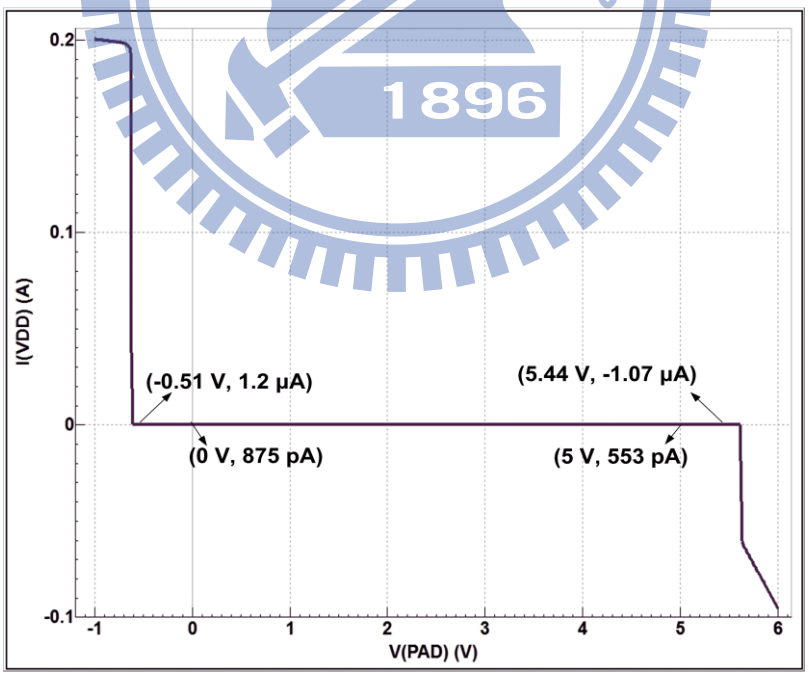


Fig. 4.9. Simulated waveforms for the current I(VDD) from supply voltage according to the variation of PAD voltage.

TABLE 4.3

SIMULATED RESULTS OF SUPPLY CURRENT I(VDD) AT DIFFERENT TEMPERATURES FOR THE WORK WITH AND WITHOUT THE PROPOSED ACTIVE GUARD RING PROTECTION

The design without the proposed active guard ring (only NMOS MN1 and PMOS MP1, kept in off state)				
I(VDD)	-20 ℃	25 ℃	85 ℃	125 ℃
V(PAD)=0V	362.3 pA	364.3 pA	481.7 pA	8.7 nA
V(PAD)=5V	176.7 pA	178.8 pA	183.2 pA	658.1 pA

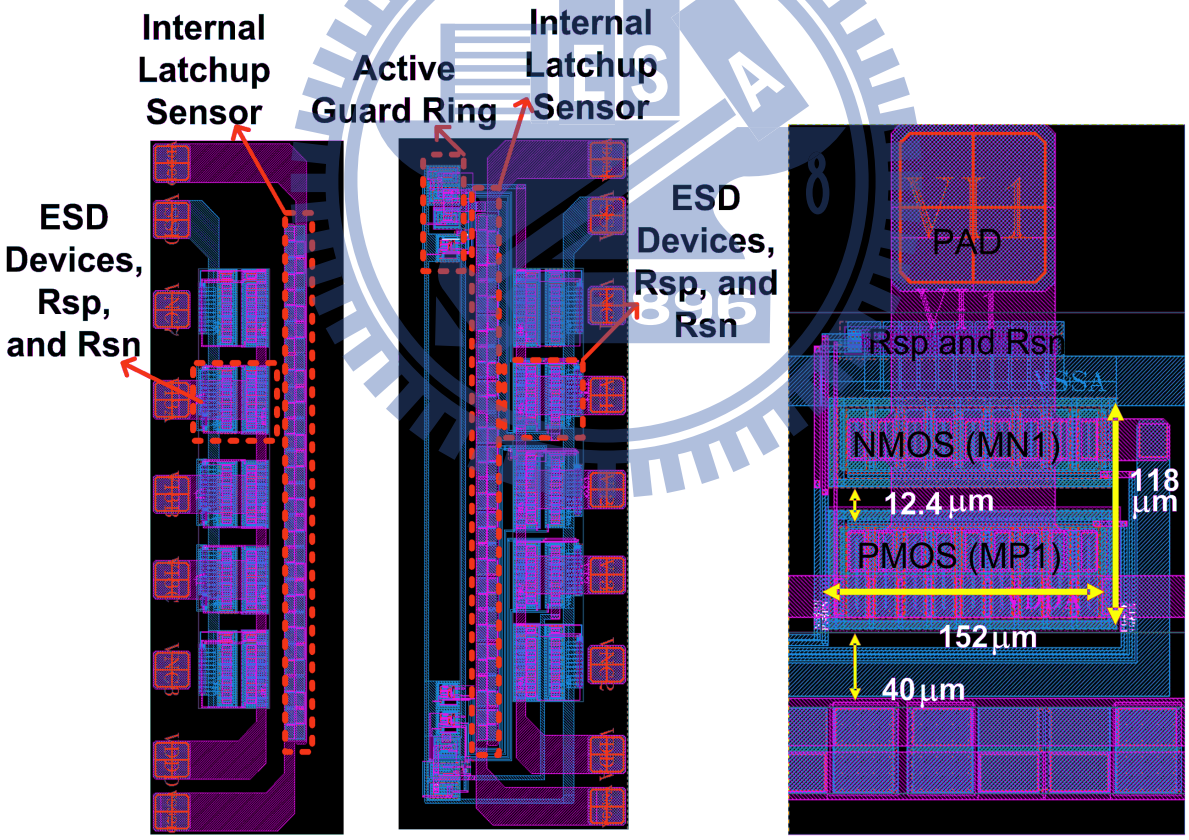
The design with the proposed active guard ring				
I(VDD)	-20 ℃	25 ℃	85 ℃	125 ℃
V(PAD)=0V	660.8 pA	874.3 pA	1 nA	25 nA
V(PAD)=5V	526 pA	553.4 pA	1.5 nA	15.4 nA

4.4 Experimental Results

The test chip to verify the proposed design with active guard ring and the related test structure has been fabricated in a 0.6-μm 5-V CMOS process. The layout top view of the test chip for the testkeys with only guard ring, the testkeys with active guard ring, and the enlarged graph for the ESD devices and resistors (Rsp and Rsn) are shown in Fig. 4.10(a), (b), and (c), respectively. The dimensions of the ESD devices in the new proposed work in Fig. 4.10(b) are the same as that of the previous work in Fig. 4.10(a) with 152μm×118 μm area consumption. The distances of the OD junctions between the bulk terminals of MP1 and MN1 is 12.4 μm. The enlarged layout graphs for the single PNPN cell to detect latch-up

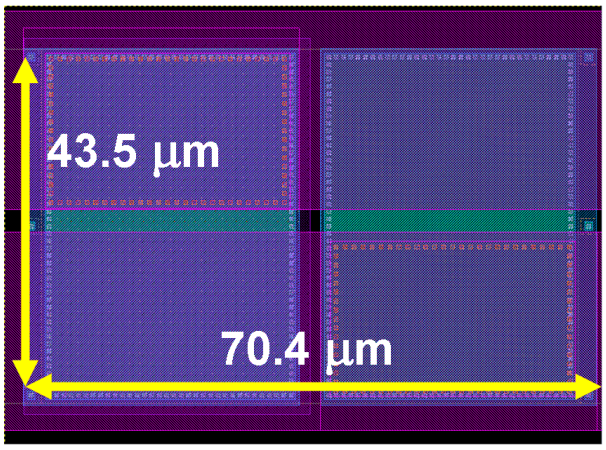
occurrence and the circuit to realize the active guard ring are shown in Fig. 4.11(a) and (b). The area draught for one PNPN cell is about 70.4 μm × 43.5 μm and 0.0132 mm² (90 μm × 78 μm + 45 μm × 63 μm + 56 μm × 60 μm) for the implemented active guard ring. Though some additional area is required in this work, the placement can be flexible and can be merged with other internal circuits together. Since there is no need to put the active guard ring beside the PAD, it is also able to arrange the extra area brought by additional circuits to the dummy or redundant layout area. Thus, the required area near the PAD can be similar to the traditional design for the PAD-limited application.

The measurement setup is similar as that shown in in Fig. 4.2 with 5-V supply at VDD and an external current source applied to the PAD. However, the VDD2 is connected in series with a 100-ohm resistor to the 5-V voltage source instead of directly connected the PAD to the voltage source. The occurrence of latchup can be easily caught by observing the voltage change of VDD2 due to the large abnormal current induced by latchup. The measured

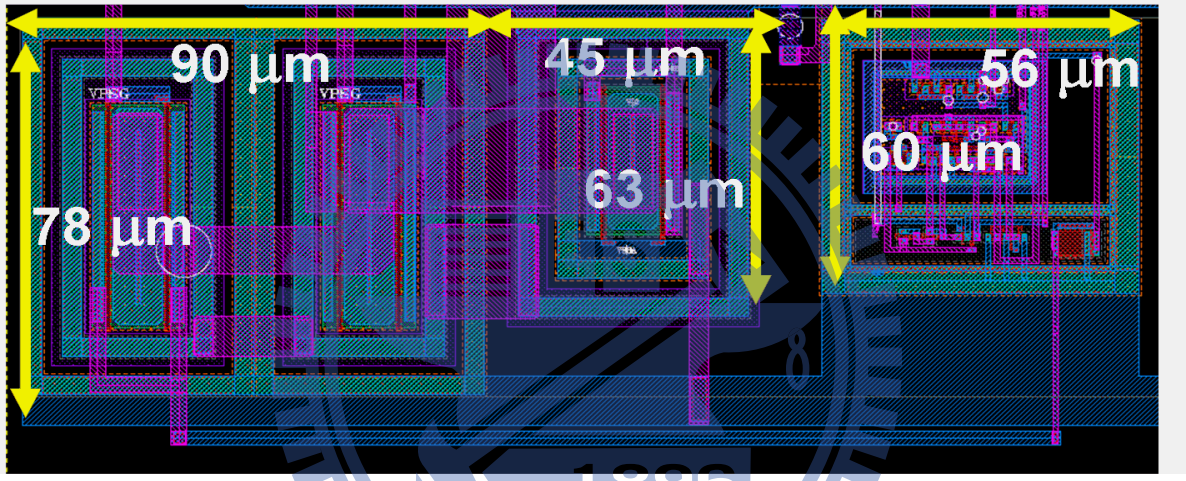


(a) (b) (c)

Fig. 4.10.(a) Layout top view of the testkeys with only single guard ring, (b) the testkeys with proposed active guard ring, and (c) the enlarged graph for the ESD devices and related resistors (Rsp and Rsn) of the testkey.



(a)

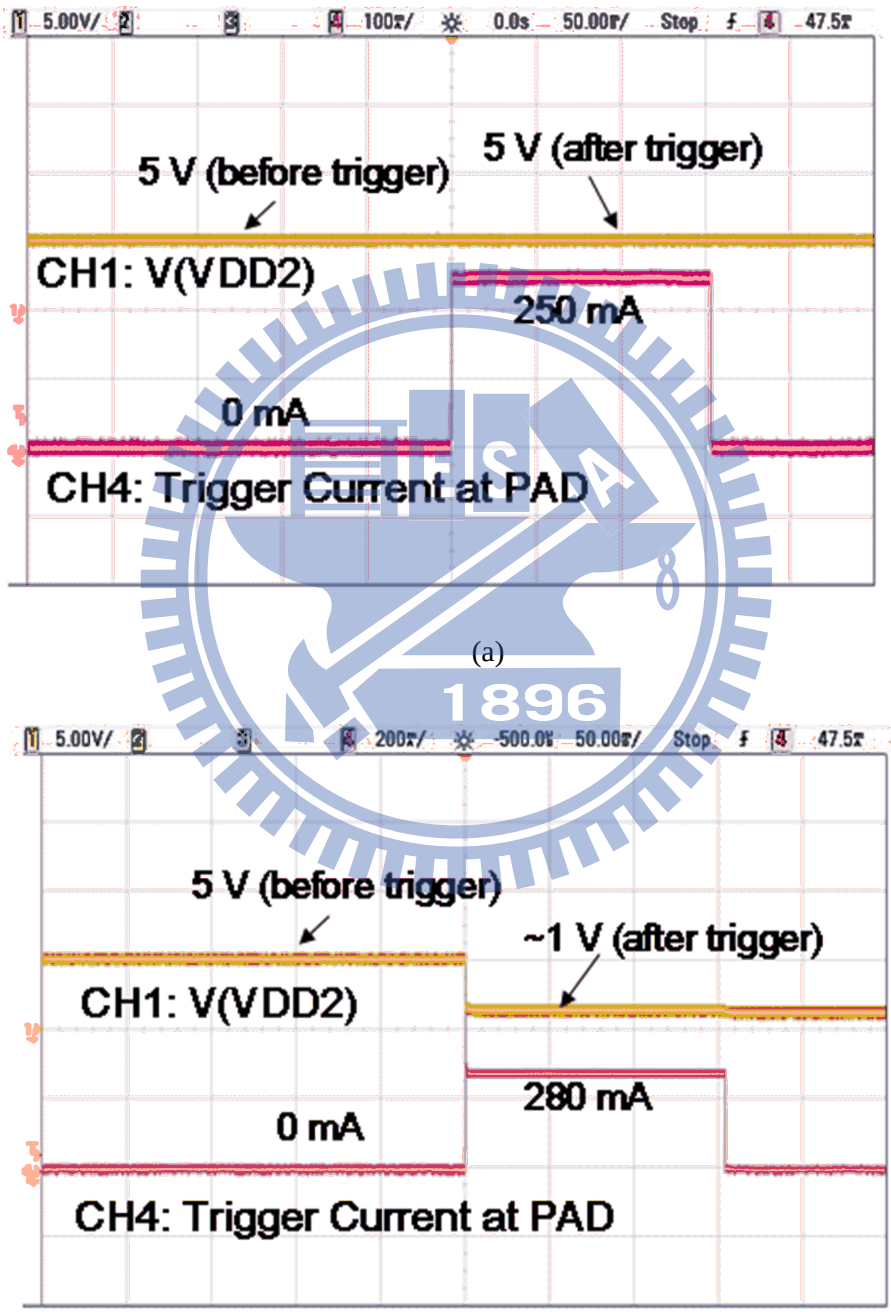


(b)

Fig. 4.11. Enlarged layout graph for (a) a single PNPN cell and (b) the active guard ring.

waveforms under the positive I-test to the test chip with 250-mA and 280-mA trigger currents are shown in Fig. 4.12 (a) and (b), respectively. The voltage of VDD2 is captured as CH1 and the trigger current applied at PAD is recorded as CH4 in the figures. If the trigger current is not over the tolerance of the testkey, the voltage at VDD2 is kept at 5 V as that shown in Fig. 4.12(a). While latchup is triggered at the PNPN cells, the voltage at VDD2 is dropped to ~1 V as that shown in Fig. 4.12(b). Thus, the proposed work is verified to pass the 250-mA but not 280-mA positive I-test from the experimented results. Under the negative I-test, the measured waveforms of the proposed design are shown in Fig. 4.13(a) and (b) under -400-mA and -470-mA trigger current, respectively. Since the VDD2 is kept at 5 V in Fig. 4.13(a), no latchup occurrence at the PNPN cells when the negative I-test current of -400mA is applied. While the VDD2 is dropped to ~1 V after the negative trigger current of -470 mA is applied

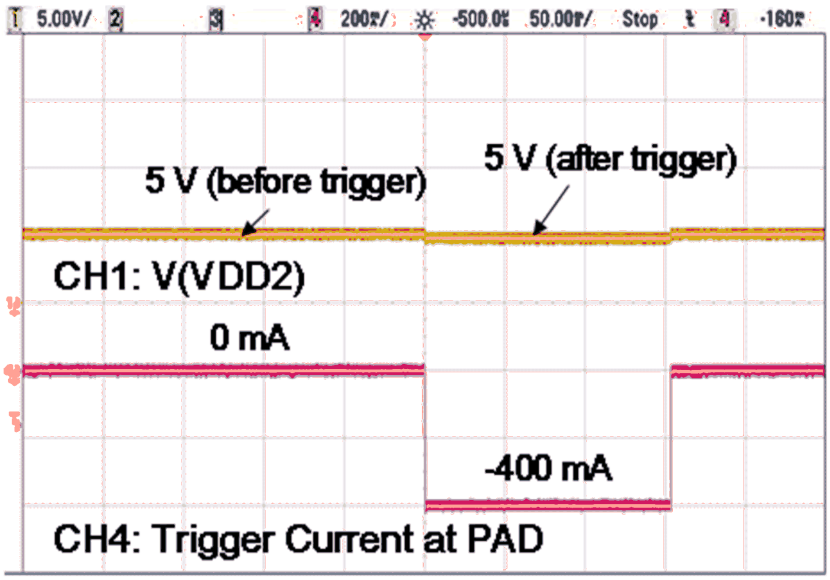
in Fig. 4.13(b), the waveforms show that the proposed design has -400-mA latchup immunity but is failed in the -470-mA current test. Moreover, more detailed examinations to investigate the latchup immunity are done by the latch-up tester with 10-ms pulse width and follow the JEDEC standards. The latchup test results for the testkeys with the traditional prevention of guard ring and the new proposed design of active guard ring are listed in Table 4.4. The tolerance in positive I-test for the proposed design is 260 mA which is much higher



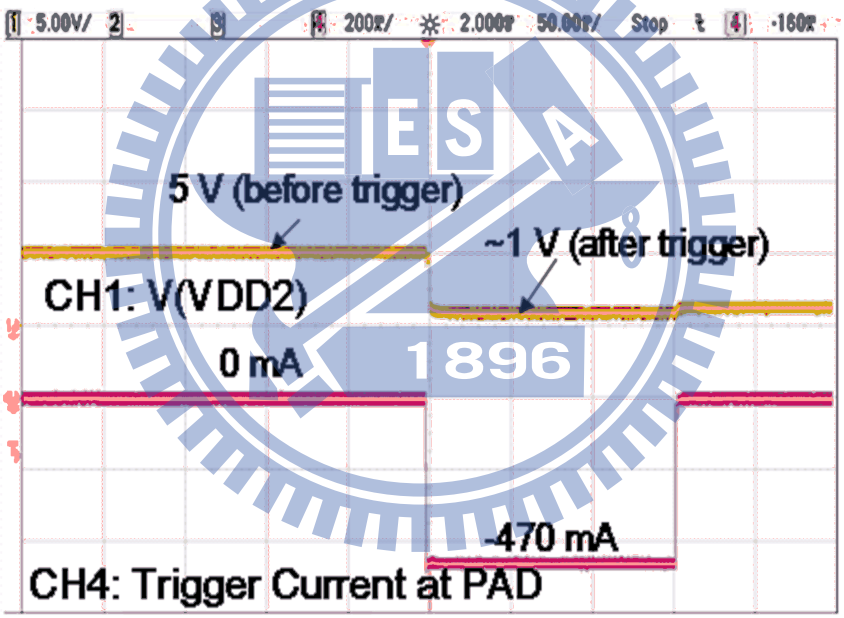
(a)

(b)

Fig. 4.12. Measured waveforms of proposed design with active guard ring under positive I-test with (a) 250-mA, and (b) 280-mA, trigger current applied at the input PAD.



(a)



(b)

Fig. 4.13. Measured waveforms of proposed design with active guard ring under negative I-test with (a) 400-mA and (b) 470-mA trigger current applied at the input PAD.

than the 5-mA performance of the traditional design. Besides, the immunity in the negative I-test of the work with active guard ring is also increased to -430 mA compared to -190 mA for the traditional prevention with guard ring. From the experiment results, the proposed work of active guard ring has been verified to reach the highest level (200 mA for positive I-test and -200 mA for negative I-test) defined in JEDEC standards, which is helpful for IC products with qualified latch-up prevention.

TABLE 4.4

LATCH-UP TEST RESULTS

Latchup I-test	Test Cell with the Traditional Guard Ring		Test Cell with the Proposed Active Guard Ring	
	Pass	Fail	Pass	Fail
Positive I-test	5 mA	10 mA	260 mA	270 mA
Negative I-test	-190 mA	-200 mA	-430 mA	-440 mA

4.5 Discussion

In this work, we realize the proposed active guard ring method with ESD devices of large-dimension MP1 and MN1. Theoretically, we can also adopt the I/O device to implement the MN1 and MP1 with slightly modification at the gate control logic block. The concept is depicted in the following figure (Fig. 4.14) as a simplified example. The "and" logic can be

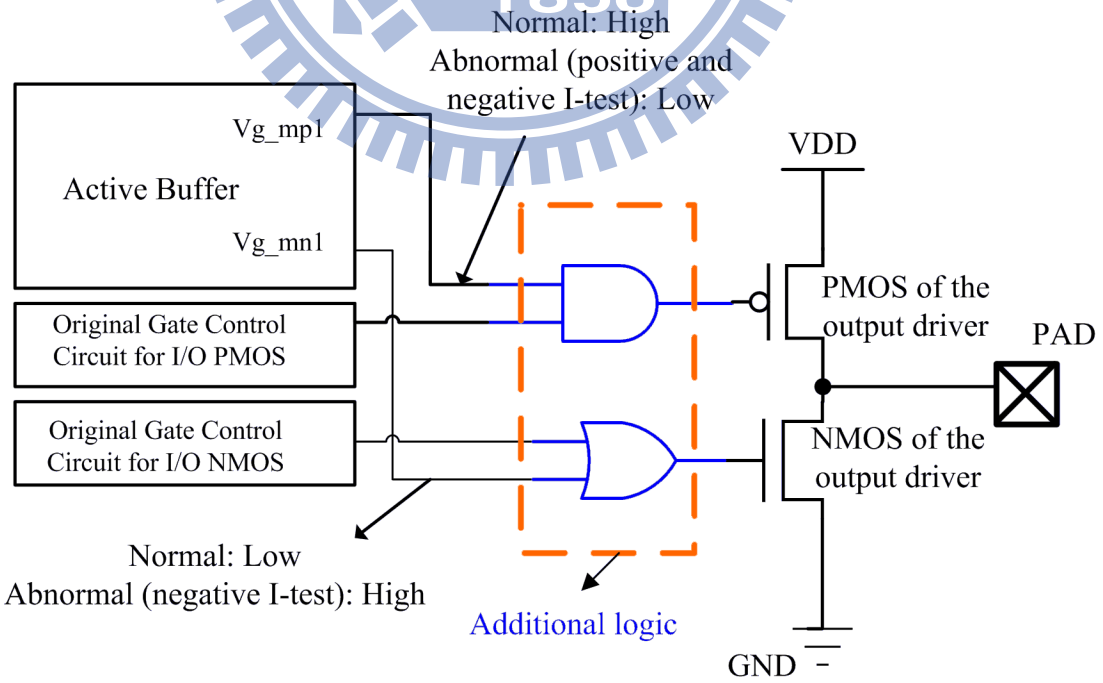


Fig. 4.14. Circuit block to control the gates of PMOS and NMOS in the output buffer co-designed with the circuit of "active guard ring".

used to connect between the Vg_mp1 of the active buffer and the original gate control circuit for the PMOS transistor of the output driver. Besides, the “or” logic can be added between the Vg_mn1 of the active buffer and the original gate control circuit for the NMOS transistor of the output driver. The schematic of active buffer can refer to Fig. 4.6(a). With modification as indicated in the following circuit (Fig. 4.14), the active guard ring structure can be still co-worked well with the output transistors in the I/O buffer.

4.6 Summary

The proposed design of “active guard ring” concept and the practical circuit implementation has been fabricated and successfully verified in a 0.6-μm 5-V CMOS process. The additional sensing and active buffer is developed to activate the existing ESD devices while the external trigger current is applied under the latch-up current test. Similar ideas may also be adopted with I/O cells by adequate modification. From the silicon verification, the testkey with the proposed design can achieve 260-mA and -430-mA immunity for positive and negative I-test, respectively. The proposed active guard ring can significantly enhance the latchup immunity of CMOS ICs with the cost of very small quiescent standby current during the normal circuit operation.

Chapter 5

Conclusions and Future Works

This chapter summarizes the main results and contributions of this dissertation. Suggestions and discussions for future research ways in the fields of applications are also provided in this chapter.

5.1 Main Results of This Dissertation

The main results for the proposed designs concentrate on the enhancement of latchup immunity in this dissertation are summarized as below:

(1) A practical industry case suffers EOS failure induced by latchup I-test in a high-voltage integrated circuits (IC) is presented. The novel design adopting the modifications in layout and circuit to prevent the unexpected EOS failure has been verified successfully. The proposed work has been verified in 0.6-um 40-V BCD process and verified to pass at least 500-mA latch-up I-test which shows high latchup immunity compared with the traditional protection of only guard ring. The novel idea can be adopted to implement high-voltage-applicable IC product to meet the industry requirement for mass production of IC manufactures and applications.

(2) A proposed method to provide complementary current at the pad under latch-up I-test is introduced. The inserting additional junctions and the resistors are used to monitor the external triggers. The ESD-protection devices can be applied to provide the required complementary current and decrease the related perturbation to the internal circuits. The proposed design and the previous work have been fabricated in the same 0.5-μm 5-V process.

(3) A novel design named as active guard ring and related circuit implementation are proposed to improve the latchup immunity of integrated circuits (IC). By adopting additional circuit and active buffer to turn on the ESD protection transistors, the large-dimension ESD (or I/O) devices can effectively turned on to generate extra compensation current to the negative or positive current triggers during the latch-up I-test. The new proposed solution has been verified in 0.6-μm 5-V process and shows much higher latch-up resistance compared

with the conventional prevention method of guard ring in the test results.

5.2 Future Works

Some designs to enhance the latchup immunity have been introduced or proposed as shown in previous sections. The solutions are mainly accomplished by circuits. In [36], an extensive overview for challenges related to latchup is discussed. Due to the limitation of the understanding for the effectiveness of guard ring and the cost-down trade off, the noise or latch-up issue may exist in the early stages to implement the new design and requires more information to solve the problems by splitting tape-out versions to analyze the interaction with parasitic elements and the effect brings by the external triggers. Besides, the adequate design rules of guard rings are not always the same for digital/analog circuits or low-voltage/high-voltage devices and thus experiences gain from previous silicon data are required and important but not certain to be sufficient. The above causes may increase the required revision times/masks or the difficulty to accomplish a qualified IC product to provide to the customers. Compared with the modification in the aspect of process or guard rings focuses on the spatially separation or electrical isolation, the circuit concept used in this dissertation is more flexible in its placement. Thus, the proposed circuit solutions as active guard ring may have the potential to be co-design in the dummy and version unify plan to reduce the demanded masks or times for IC revision in future application.

As for the high-voltage application, facing with more complex conditions between the parasitics and elements, strict and comprehensive design concerns including the ESD issue, the voltage tolerance…etc are required. In such cases, techniques in layout as butted contact or other isolation methods at process may be more common for overall consideration. Besides, for the internal latchup, to protect by electrical isolation methods and to avoid the latchup happening are also really helpful and convenient solutions. However, as the practical case, the circuit solution may still do help for preventing EOS problems. Furthermore, the effect and function for the proposed circuit solutions to “EOS problems” under latchup I-test can be further studied.

Finally, circuit solutions for the issues related to transient latchup can be advanced research directions. According to the JEDEC standards, the minimum rising/falling time is 5-μs and the minimum width is 2 times of the rising time for the trigger current pulses. Since the circuit solutions as active guard ring require certain response time toward the external

triggers, the proposed design may react to the trigger current pulses within the defined timing range of JEDEC standards but may be insensible to the spikes as fast as few ns. Since the circuit solutions as active guard ring are implemented with MOS transistors, the timing related performance can be roughly estimated by the SPICE simulation. How to optimize the proposed design toward different application cases or modified the performance related to the transient latchup issue, and to enhance the latchup immunity by design with SPICE simulation, can be also be considered in the future work.

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論文名稱：提升積體電路栓鎖防疫能力之設計方法與實現

Design and Implementation to Improve Latchup Immunity of CMOS Integrated Circuits

Publication List

(A) Referred Journal Papers:

[1] **H.-W. Tsai** and M.-D. Ker, "Layout consideration and circuit solution to prevent EOS failure induced by latchup test in a high-voltage integrated circuits", *IEEE Trans. Device Mater. Reliab.*, vol. 14, no. 1, pp. 493-497, Mar. 2014.

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(B) International Conference Papers:

[1] **H.-W. Tsai**, M.-D. Ker, Y.-S. Liu, and M.-N. Chuang, "Analysis and solution to overcome EOS failure induced by latchup test in a high-voltage integrated circuits," in *Proc. IEEE Int. Symp. VLSI-DAT*, 2013, pp. 33-36.

[2] **H.-W. Tsai** and M.-D. Ker, "Improve latch-up immunity by circuit solution," accepted by *Proc. of International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA)*, Hsinchu, Taiwan, Jun. 29-Jul. 2, 2015.

[3] **H.-W. Tsai** and M.-D. Ker, "Compensation circuit with additional junction sensor to enhance latchup immunity for CMOS integrated circuits," accepted by *Proc. of 22nd European Conference on Circuit Theory and Design (ECCTD)*, Trondheim, Norway, Aug. 24-26, 2015.

(C) Patent Pending

[1] **H.-W. Tsai** and M.-D. Ker, "Active guard ring structure to improve latch-up immunity," U.S. and R.O.C. patent pending.