# 國立交通大學

## 電子工程學系 電子研究所

## 博士論文

# 系統單晶片應用之靜電放電箝制電路與輸出緩衝器可靠度設計

# Reliability Design of ESD Clamp Circuit and Output Buffer for SoC Applications

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中 華 民 國 一〇二 年 十 月

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博 士 論 文

A Dissertation
Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering

October 2013
Hsinchu, Taiwan, Republic of China

中華民國 一〇二 年 十 月

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## 摘要

全晶片靜電放電防護設計架構中，靜電放電箝制電路(ESD Clamp Circuit)在靜電放電的轟擊下，能有效提供一靜電電流放電路徑，為影響整體靜電放電耐受度(ESD Robustness)的主要電路區塊。然而當進入奈米製程製作時，傳統的靜電放電箝制電路面臨到嚴重的閘極漏電流影響，進而使電路失去功能並產生更嚴重的能量損耗。為此，於論文第二章中，提出替代和改善方案，其中包括使用金屬-金屬間電容替代金氧半導體電容和利用電路技巧方法解決傳統靜電放電箝制電路的閘極漏電流問題。

另外，不同於奈米製程下所產生的問題，隨著系統單晶片應用的趨勢，高壓互補式金氧半製程已廣泛使用於系統單晶片製作，然而在高壓的操作環境下，元件低持有電壓(Holding Voltage)將造成類似閉鎖效應(Latchup-Like)的危險，尤其是將這些元件作為電源間靜電放電防護元件使用。因此於論文第三章中，為解決一實際案例於觸控面板(Touch Panel)控制電路的高操作電壓環境下，元件低持有電壓特性產生的類似閉鎖效應，提出一新型高壓靜電放電箝制電路。該新型設計可以提高持有電壓，並高於觸控面板控制電路的操作電壓。因此，新型設計可以避免產生類似閉鎖效應的危險。

當半導體元件相關參數持續微縮，內部核心電路元件的操作電壓亦會隨著持續下降以符合元件可靠度。然而在系統單晶片的電路區塊中，並非所有的電路應用皆隨著製程演進而降低操作電壓。因此在晶片系統中，還存在許多電路必須操作於一較高電壓環境中。在考量不同操作電壓環境對電路可靠度的影響，一般的輸入/輸出介面電路將不再適用。為了解決輸入/輸出介面於不同電壓操作下所產生的電路可靠度問題，系統單晶片應用中，必須要有混合電壓共容輸入/輸出緩衝器(Mixed-Voltage I/O Buffer)的使用。此外，另有相關具有可承受高電壓能力的邏輯電路被開發，使其能處理高電壓訊號。然

而數位電路應用中，最基本的電路單元為互補式邏輯閘(Complementary Logic Gate)，如能在混合電壓共容輸出緩衝器應用上，注入互補式邏輯的原理，將能設計出具有混合電壓共容能力之新型態邏輯閘。因此於論文第四章中，延續先前的兩倍電壓共容輸出緩衝器的相關研究，提出新型兩倍電壓共容邏輯閘的設計，並只使用一倍電壓元件，其中包括兩倍電壓共容反閘(NOT Gate)、反及閘(NAND Gate)、反或閘(NOR Gate)。

此外，進入奈米製程後，元件尺寸和各項參數級距更細微的情況下，電路將會更容易受製程、電壓、溫度變異而影響。對於提供一驅動訊號的輸出緩衝器來說，電路輸出驅動訊號的迴轉率(Slew rate)極易受到製程、電壓、溫度變異而變動，如要使輸出驅動訊號能有較穩定的迴轉率，必須加入電路補償機制。因此，於論文第五章中提出一新型具製程、電壓、溫度變異補償之兩倍電壓共容輸出緩衝器。為了能偵測兩倍電壓操作環境的變異情況，補償電路必須具有可處理兩倍電壓訊號的能力，而前章節所提出的兩倍電壓共容邏輯閘，將能組成兩倍電壓共容製程、電壓、溫度變異補償電路。在兩倍電壓共容輸出緩衝器與兩倍電壓共容製程、電壓、溫度變異補償電路的結合下，兩倍電壓共容製程、電壓、溫度變異補償電路能提供補償碼，使輸出緩衝器在製程、電壓、溫度變異下，能有效調節輸出驅動能力，維持一較穩定之輸出迴轉率。

# Reliability Design of ESD Clamp Circuit and Output Buffer for SoC Applications

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## Abstract

In the whole-chip ESD protection design scheme, the ESD clamp circuit could provide an effective ESD current discharging path under ESD stresses. With a good ESD protection arrangement in the IC, the ESD robustness is mainly decided by the ESD clamp circuit. However, the traditional design suffered the serious gate leakage issue in nanoscale CMOS processes. It results in malfunction and serious power consumption in the circuit. For solving the gate leakage issue in the traditional ESD clamp circuit, new proposed designs are presented in Chapter 2 which included usages of device replacement by metal-oxide-metal capacitor and circuit bias technique.

In addition to the gate leakage issue in nanoscale CMOS processes, another reliability issue occurred in other CMOS technology node. With the development of SoC applications, the high-voltage CMOS technology is widely adapt in the ICs fabrication. But, under a higher operating voltage, the characteristic of low holding voltage in the device will cause the latchup-like failure, especially the devices were used as the ESD protection device in high-voltage CMOS processes. For solving the latchup-like issue in the high-voltage ESD clamp circuit, a new proposed design with latchup-free immunity is presented in Chapter 3. With the new proposed high-voltage ESD clamp circuit, the touch panel control IC is free to the latchup-like issue for the touch panel application.

As MOS devices scaled down, the operating voltage of core devices were also reduced to lower voltage level (below 1.2 V). However, some peripheral components or sus-systems in the SoC application would be still operated in higher voltage levels (above 1.8 V). With different power supply voltages in the system, the conventional I/O buffers are no longer

suitable due to reliability concerns. Therefore, the mixed-voltage I/O buffers are necessary to put into the interface to communicate with other sub-system which has different power domain. Moreover, some logic circuits were also developed with high-voltage tolerant ability to process higher voltage signal. In the digital circuit applications, the basic circuit units are complementary logic gates. If the mixed-voltage output buffer could infuse the logic operation theorem, the logic gates could be designed to have high-voltage tolerant ability. Base on design concepts of the $2xV_{DD}$-tolerant output buffer, new $2xV_{DD}$-tolerant logic gates with only $1xV_{DD}$ devices are presented in Chapter 4, including $2xV_{DD}$-tolerant NOT, NAND, and NOR gates.

When the CMOS process shrinks toward nanoscale, the circuit performance becomes more sensitive to process, voltage, and temperature (PVT) variations. Consequently, for providing the driving signal of an output buffer, the output slew rate will easily be varied by PVT variations. In order to keep a stable slew rate of the driving signal, the output buffer needs to combine the compensation mechanism. In Chapter 5, a new $2xV_{DD}$-tolerant output buffer with PVT compensation is proposed. For detecting the PVT variations under $2xV_{DD}$ voltage environment, the compensation circuit needs to have the capability to process $2xV_{DD}$ voltage signal. Simultaneously, the proposed $2xV_{DD}$-tolerant logic gates are able to constitute the $2xV_{DD}$-tolerant PVT compensation circuit. With the compensation code provided by the compensation circuit, the $2xV_{DD}$-tolerant output buffer can adjust the driving ability to keep a more stable output slew rate when facing PVT variations.

# Contents

# List of Tables

## Chapter 2



## Chapter 3

## Chapter 4



## Chapter 5

# List of Figures

## Chapter 1



## Chapter 2

## Chapter 3

## Chapter 4

## Chapter 5

# Chapter 1

## Introduction

Due to the development of System-on-Chip (SoC) and advancement of process technology, varied types of circuit systems could be integrated in a single chip. To implement the circuit systems with different power domain, low-voltage and high-voltage CMOS processes are maturely combined for SoC applications. With the various circuit functions and process technologies integrated in the SoC system, system interfaces will become more complicated. Fig. 1.1 shows the schematic of input/output (I/O) interfaces in the SoC application. Both electrostatic discharge (ESD) protection circuits and mixed-voltage I/O buffers are essential to establish in the integrated circuit (IC) interfaces. However, a portion of circuits would suffer the serious reliability issue. In this chapter, the motivations of the dissertation are discussed. First, the reliability issues of the ESD clamp circuit in different system applications are described. Second, the reliability considerations of the mixed-voltage I/O buffer are introduced. Finally, the organization of this dissertation is presented.

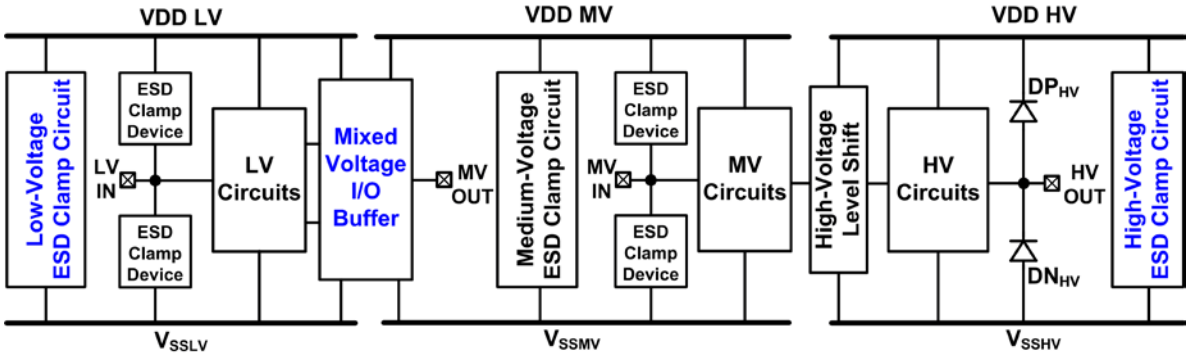
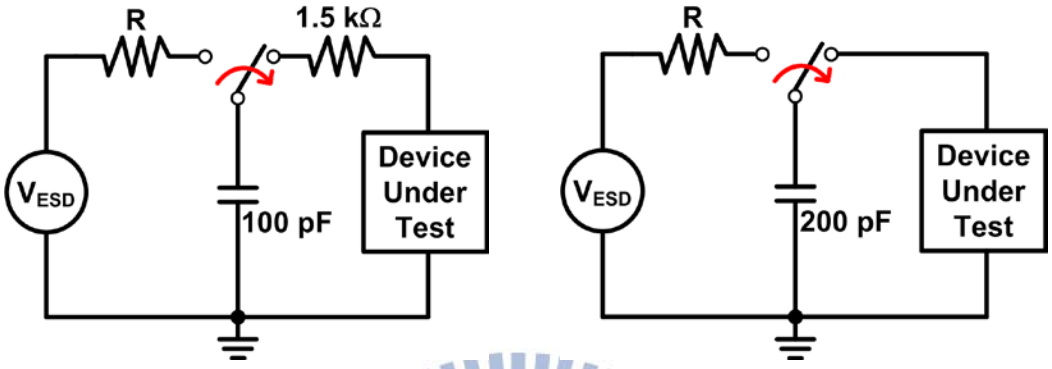



Fig. 1.1. Schematic of I/O interfaces in the SoC system.

## 1.1 Reliability Issues of ESD Clamp Circuit

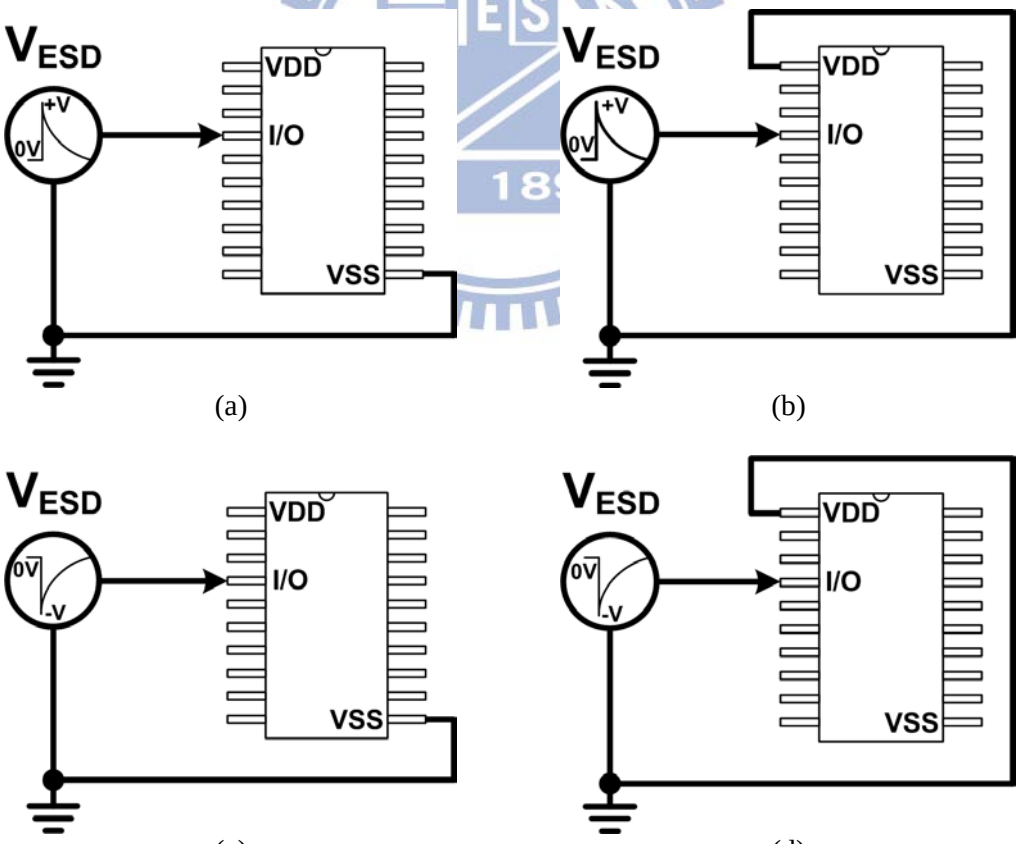
During IC products manufacture, the ESD induced damage has become one of the major reliability issues. To protect the IC products against ESD damage, the on-chip ESD protection circuits are necessary to establish in IC interfaces [1]-[4]. For evaluating the robustness of ICs against ESD events, two chip-level (or component-level) ESD tests are often used, human-body-model (HBM) test [5] and machine-model (MM) test [6]. The equivalent models of HBM and MM ESD tests are shown in Fig. 1.2(a) and 1.2(b), respectively. Due to electrostatic charges would be either positive or negative, there are four ESD test modes at

I/O pins with respect to the grounded $V_{DD}$ or $V_{SS}$ (GND) pins, which are PS (positive-to-$V_{SS}$), PD (positive-to-$V_{DD}$), NS (negative-to-$V_{SS}$), and ND (negative-to-$V_{DD}$) modes as shown in Fig. 1.3. For comprehensive ESD verification, the $V_{DD}$-to-$V_{SS}$ ESD stress had also been specified to verify the whole-chip ESD robustness as shown in Fig. 1.4. To the commercial IC products, the basic chip-level ESD robustness are required 2 kV in HBM test and 200 V in MM test.




(a) (b)

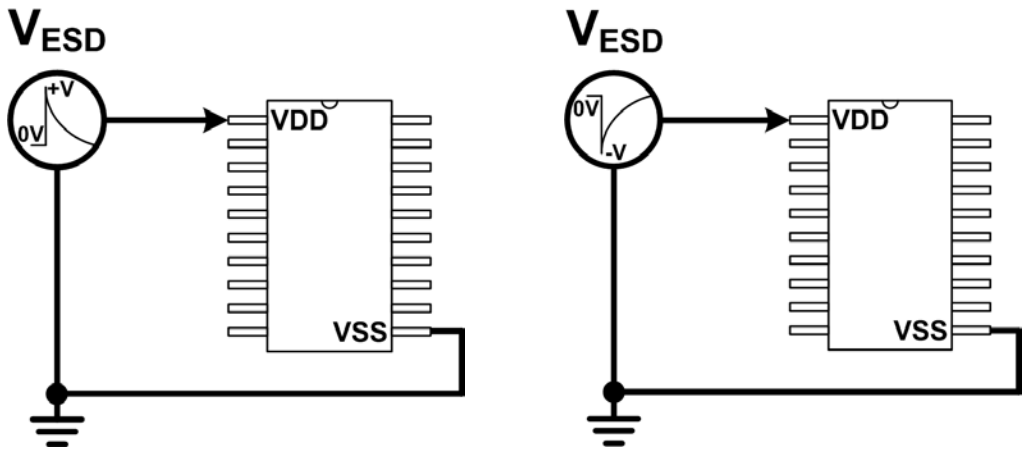
Fig. 1.2. Equivalent models of (a) HBM and (b) MM ESD tests.




(a) (b)

(c) (d)

Fig. 1.3. Four ESD test modes at I/O pins for IC products: (a) positive-to-$V_{SS}$ mode (PS-mode), (b) positive-to-$V_{DD}$ (PD-mode), (c) negative-to-$V_{SS}$ mode (NS-mode), and (d) negative-to-$V_{DD}$ (ND-mode).




(a) (b)

Fig. 1.4. $V_{DD}$-to-$V_{SS}$ ESD test modes: (a) positive mode and (b) negative mode.

The typical on-chip ESD protection scheme is shown in Fig. 1.5. The ESD clamp circuit is designed to provide a current discharging path during ESD stresses and to be kept off under normal power-on conditions. Conventionally, the ESD clamp circuit was often implemented by a RC-based ESD-detection circuit (R, C, $M_P$, and $M_N$) and a main ESD protection device ($M_{NESD}$) with large dimension to achieve high ESD robustness. To efficiently turn on the ESD clamp circuit during ESD events and to completely keep off under normal circuit operating conditions, the RC time constant of the ESD-detection circuit should be designed around ~microsecond (μs). In cooperation with the ESD clamp circuit, the ESD clamp devices at the I/O pads can effectively divert ESD energy to the $V_{DD}$ or the $V_{SS}$ (GND) power lines [7]. Moreover, with the turn-on efficient ESD clamp circuit, the ESD clamp devices at the I/O pads can be further realized with small device dimensions to achieve good enough ESD robustness [8], [9].

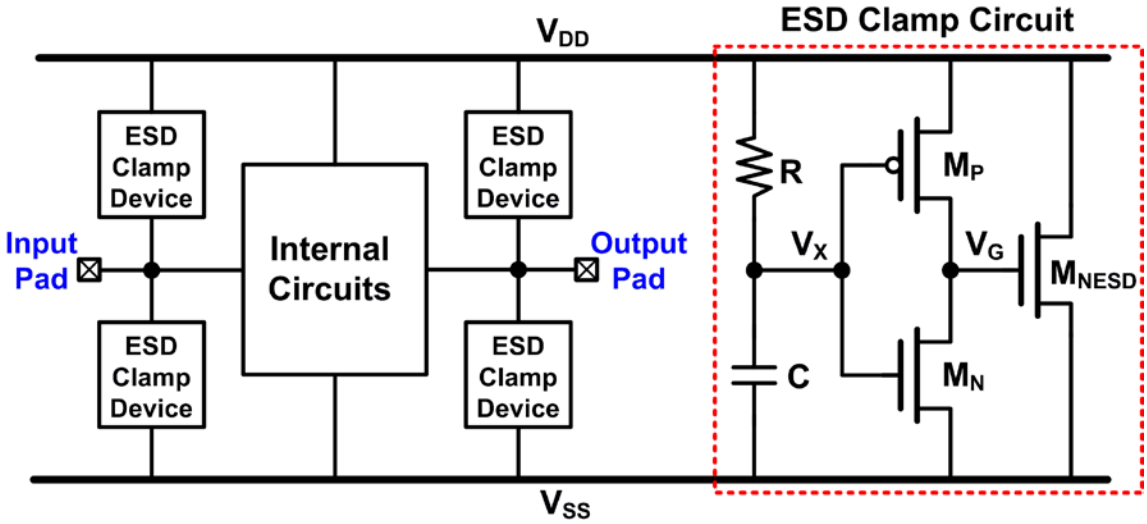
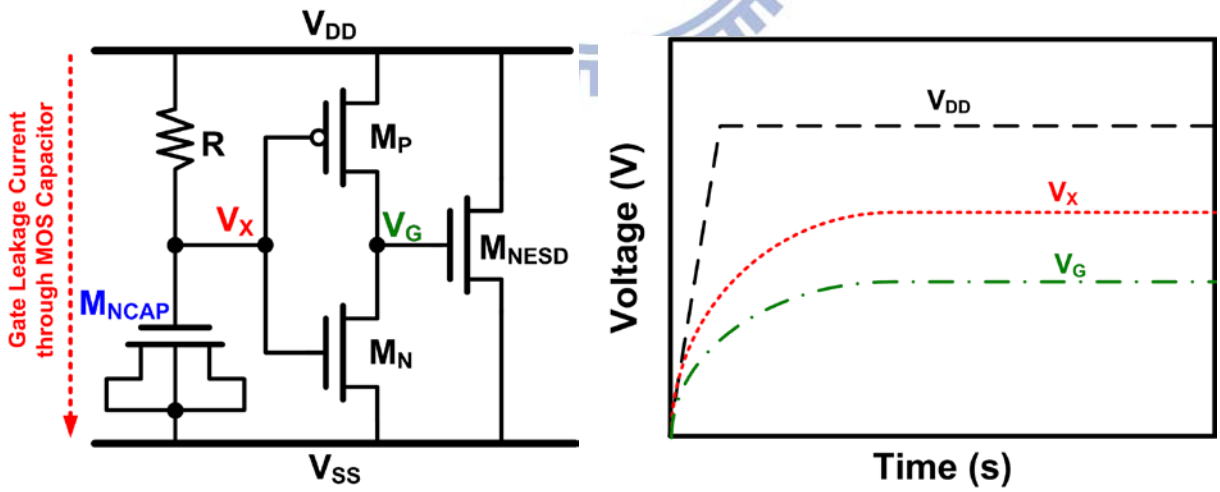



Fig. 1.5. Typical on-chip ESD protection scheme in CMOS ICs.

### 1.1.1. Gate Leakage Issue in the Nanoscale CMOS Process

With the consideration of area efficiency and fabrication cost, the capacitor in the ESD clamp circuit was often realized by the MOS capacitor, because the MOS capacitor has the highest capacitance density per unit area. However, when the CMOS technology shrinks toward nanoscale, MOS devices are also shrunk with low operating voltage and thinner gate oxide thickness. But, thinner gate oxide makes the gate direct tunneling issue more serious to cause obvious gate leakage current in the device [10]-[12]. With the obvious gate leakage current of MOS devices in nanoscale CMOS processes, the ESD clamp circuit with a MOS capacitor was reported to have huge leakage current [13]. For example, a ESD clamp circuit implemented with a thin-oxide NMOS capacitor ($M_{NCAP}$) is shown in Fig. 1.6(a). When a large gate leakage current occurred in the $M_{NCAP}$, the voltage at $V_X$ can not be fully charged to $V_{DD}$ after power-on, as shown in Fig. 1.6(b). Therefore, the PMOS $M_P$ in ESD-detection circuit can not be fully turned off, which causes another leakage path through the inverter $M_P$ and $M_N$. Consequently, the gate voltage $V_G$ of $M_{NESD}$ can not be fully biased to $V_{SS}$. Thus, The partially turned on $M_{NESD}$ (which is always designed with large device dimension) will conduct more leakage current from $V_{DD}$ to $V_{SS}$ under normal circuit operating conditions. Therefore, new design of ESD clamp circuit to against gate leakage issue in nanoscale CMOS processes is one of the research topics in this dissertation.




(a) (b)

Fig. 1.6. Gate leakage issue in the ESD clamp circuit: (a) Traditional ESD-detection circuit with NMOS capacitor ($M_{NCAP}$) (b) terminal voltages of the circuit with leaky $M_{NCAP}$.

### 1.1.2. Latchup-Like Issue in the High-Voltage CMOS Process

To effectively provide the protection capability of a ESD device, Fig. 1.7 shows the ESD protection design window with the required conditions. The trigger voltage ($V_{t1}$) should be smaller than the gate oxide breakdown voltage ($V_{BD}$) to ensure successful protection without damage at internal circuits, and the holding voltage ($V_h$) should be higher than the operating voltage ($V_{DD}$) to accomplish a latchup-free design. Thus, an efficient ESD protection device's I-V curve must be located in the region II. However, in the high-voltage CMOS processes, the characteristic of low holding voltage in the device has been reported to have the latchup-like issue under a higher operating voltage, especially the devices were used as the ESD protection device [14]-[18]. In this case, the high-voltage ESD clamp circuit for touch panel control IC suffered the latchup-like failure. As the latchup phenomenon occurred in normal circuit operating conditions, the circuit could not be recovered to normal functionality. Therefore, new design of high-voltage ESD clamp circuit with latchup-free immunity is another research topic in this dissertation.

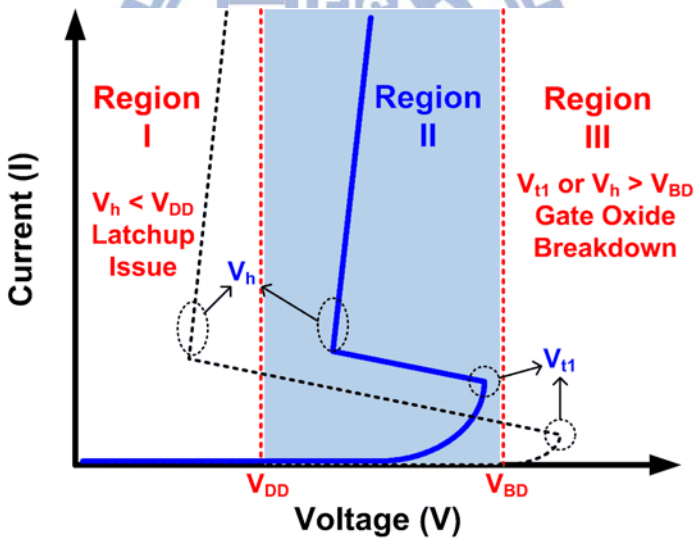



Fig. 1.7. I-V characteristics of the ESD protection device design window.

## 1.2 Reliability Considerations of Mixed-Voltage I/O Buffer

In order to achieve lower power consumption, higher operating speed, and higher integration capability, CMOS devices have been continually scaled down with thinner gate oxide thickness and smaller channel length. Thus, the operating voltage of core devices will be also reduced to a lower voltage level (below 1.2V) to conform gate oxide reliability. However, some peripheral components or sub-systems in the SoC application would be still

operated in higher voltage levels (above 1.8V). With the different power supply voltages in the system, the conventional I/O buffers are no longer suitable due to reliability concerns. Several reliability issues had been reported, such as gate oxide overstress [19]-[21], hot-carrier degradation [22], [23], and the undesired leakage current paths [24]. Fig. 1.8 shows the conventional I/O buffer with $1xV_{DD}$ MOS devices. When an external $2xV_{DD}$ signal is applied to the I/O pad, leakage paths will be occurred in the conducted channel and parasitic P+-to-N-Well diode at pull-high PMOS ($M_{P1}$). Moreover, the pull-low NMOS ($M_{N1}$) and the input buffer to internal circuit will be overstressed by the $2xV_{DD}$ voltage signal. To solve the gate oxide reliability issue, several mixed-voltage I/O buffers realized by only low-voltage (thin-oxide) devices had been reported [25]–[32].

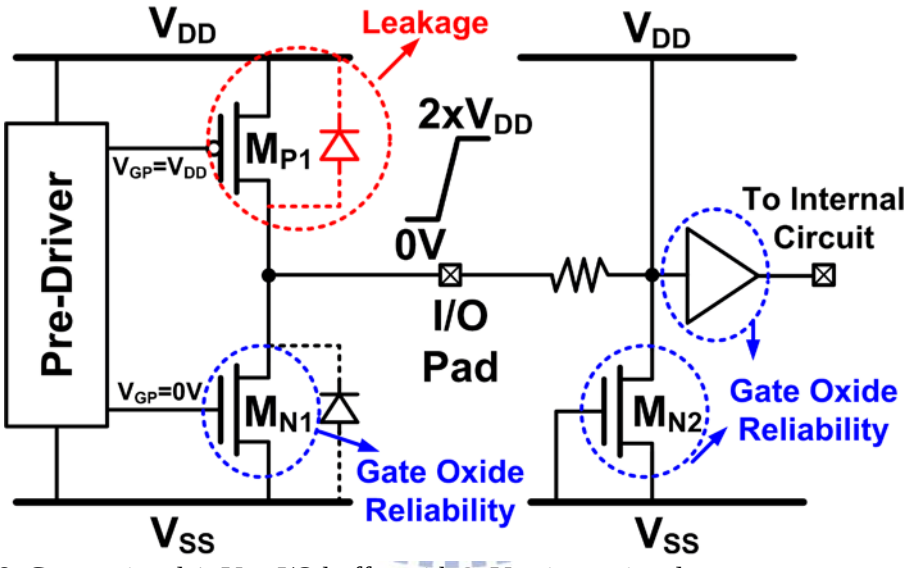



Fig. 1.8. Conventional $1xV_{DD}$ I/O buffer with $2xV_{DD}$ input signal.

In addition to the device reliability issues, the circuit performance with the scaled-down MOS devices becomes more sensitive to process, voltage, and temperature (PVT) variations. Moreover, a recent study had been reported that the die-package stress also influences device or circuit performance [33]. Thus, circuit performance becomes more difficult to meet the required specifications in advanced CMOS processes. To improve the yield, the PVT variations had been taken into consideration in lots of circuit design scenarios, especially in signal processing, data transmitting, and clock generating [34]-[39]. Consequently, for providing the driving signal of an output buffer, the slew-rate of the driving signal is easily varied by PVT variations. Several previous studies of output buffer with PVT compensation provided useful methods to keep the output slew rate within an acceptable range [40]-[45]. However, those methods are not feasible in the mixed-voltage I/O interfaces, because the

devices would suffer the gate oxide overstress issue under a operating voltage higher than $1xV_{DD}$. In order to mitigate the slew rate variation occurred by PVT variations, the $2xV_{DD}$-tolerant output buffer with PVT compensation is the final research topic in this dissertation.

## 1.3 Organization of This Dissertation

To overcome those reliability issues in the ESD clamp circuits and the mixed-voltage output buffer, new designs are developed and verified in this dissertation. This dissertation contains 6 chapters. Chapter 1 presents the backgrounds and the motivations.

In chapter 2, three proposed designs to solve the gate leakage issue in ESD clamp circuit are presented. In the first design, a metal-oxide-metal (MOM) capacitor is implemented through the metal interconnects to replace the leaky thin-oxide MOS capacitor. Instead of device replacement, a new design concept to decrease the gate leakage current is presented. By applying a bias circuit to decrease the voltage across the MOS capacitor, the gate leakage current of MOS capacitor could be mitigated to further decrease the leakage current in ESD clamp circuit. As a result, the second design with a diode string bias circuit is proposed. Although the second design consists with the thin-oxide MOS capacitor, the bias circuit can successfully reduce the impact of the gate leakage issue from thin-oxide MOS capacitor. However, without a direct DC path to ground for MOS capacitor in the circuit, the circuit trigger ability is decreased under ESD events. For this reason, the third design is proposed to improve the trigger ability. With the feedback-control bias circuit, the third design can enhance the trigger ability, and it has excellent capability to suppress the gate leakage issue.

In Chapter 3, a new high-voltage ESD clamp circuit to overcome the latchup-like failure for touch panel control IC is proposed. For increasing the holding voltage of the ESD protection device, the ESD protection device is modified to stack with high-voltage and low-voltage NMOS devices. Thus, the holding voltage can be adjusted by two different devices to a suitable range. With the new proposed design, the holding voltage is increased to higher than the operating voltage of the touch panel control IC. Therefore, the proposed design is free to the latchup-like issue.

In Chapter 4, new $2xV_{DD}$-tolerant NOT, NAND, and NOR gates are proposed. With the design concept of the dynamic source bias technique infused with logic operation theorem, the $2xV_{DD}$-tolerant logic gates can successfully be realized with only $1xV_{DD}$ devices. Under the $2xV_{DD}$ operating voltage, the proposed $2xV_{DD}$-tolerant logic gates can safely receive the

$2xV_{DD}$ voltage signals and provide the correct $2xV_{DD}$ logic functions without suffering the gate oxide overstress issue.

In chapter 5, a new $2xV_{DD}$-tolerant output buffer with PVT compensation is proposed. By implemented the design concepts of dynamic source bias and gate-controlled techniques, all circuit blocks could be realized with only $1xV_{DD}$ devices without the gate oxide overstress issue. The proposed design incorporates with a $2xV_{DD}$-tolerant output buffer, a $2xV_{DD}$-tolerant PVT detector, and a $2xV_{DD}$-tolerant 8-to-3 encoder. Therefore, the $2xV_{DD}$-tolerant output buffer with PVT compensation can successfully operate under the $2xV_{DD}$ voltage power domain and adjust the driving capability against PVT variations.

In chapter 6, the main achievements of this dissertation are summarized. Some suggestions for the future works are also addressed in this chapter.

# Chapter 2

# Design of Low-Leakage ESD Clamp Circuits

For solving the gate leakage issue in the ESD clamp circuit, two modification concepts are presented. In the first one, the MOS capacitor could be replaced by another capacitor without gate leakage issue. Thus, the ESD clamp circuit with MOM capacitor is proposed. In the second one, the gate leakage current could be decreased by reducing the voltage across the MOS capacitor. Therefore, two ESD clamp circuits with different bias circuits are proposed.

## 2.1. Background

Since the structure consisting of metal, oxide, and semiconductor, three gate direct tunneling mechanisms were reported to explain the gate leakage phenomena in CMOS devices [10]-[12]. As shown in Fig. 2.1, three mechanisms are electron tunneling from the conduction band (ECB), electron tunneling from the valence band (EVB), and hole tunneling from the valence band (HVB). When the gate oxide thickness is scaled down, the tunneling carriers across the potential barrier are increased with a great proportion to result in the gate leakage current. In nanoscale CMOS processes, the gate oxide thickness of MOS devices was only a few nanometers, which had been reported to have obvious gate leakage current [10]-[12].

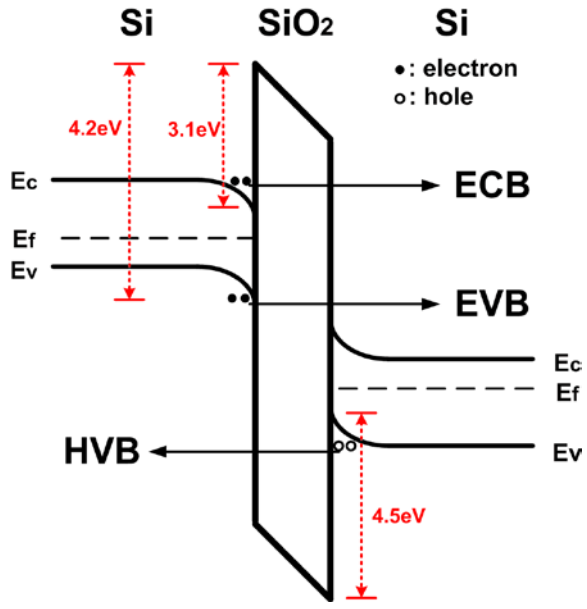



Fig. 2.1. Gate direct tunneling mechanisms in a Si/$SiO_2$/Si structure.

With obvious gate leakage current in MOS devices, ICs would generate the redundant power consumption or even the IC function may not work correctly due to the gate voltage could be discharged through the leaky gate terminal. Therefore, the gate leakage issue have been considered in many circuit design scenarios. In the highly integrated digital circuits, the gate leakage current contributes a significant off-state leakage to greatly increase the total power consumption [46]-[48]. In the analog circuits, the impacts of gate leakage include the limited current gain, mismatch, and noise [49]. In addition to those circuit design fields, the ESD protection circuits also suffer the gate leakage issue, which causes large leakage current in the ESD clamp circuits [13]. Since the gate leakage can not be ignored, the gate direct tunneling model had been included in the BSIM4 MOSFET SPICE model for circuit simulation [50].

To observe the gate leakage issue in MOS capacitor by HSPICE simulation, two traditional ESD-detection circuits with ideal capacitor and NMOS capacitor are compared as shown in Fig. 2.2. The device dimensions used in this simulation list in Table 2.1. Fig. 2.3 shows the simulated waveforms of ESD-detection circuits with a 65-nm CMOS process HSPICE model. Without the gate leakage of an ideal capacitor in the ESD-detection circuit, the terminal $V_X$ can be biased to near the power-supply voltage ($V_{DD}$) of 1 V. The simulated overall leakage current from $V_{DD}$ is only 304 nA at 25°C. However, with a leaky thin-oxide NMOS capacitor in the ESD-detection circuit, the terminal $V_X$ can not be biased to $V_{DD}$. Thus, the simulated overall leakage current is increased up to 586 μA at 25°C.

The simulated results had demonstrated the impact of gate leakage issue. Since the ICs with lower power consumption are preferred, any redundant leakage current must be eliminated. Thus, the gate leakage issue in the ESD clamp circuit should be solved.

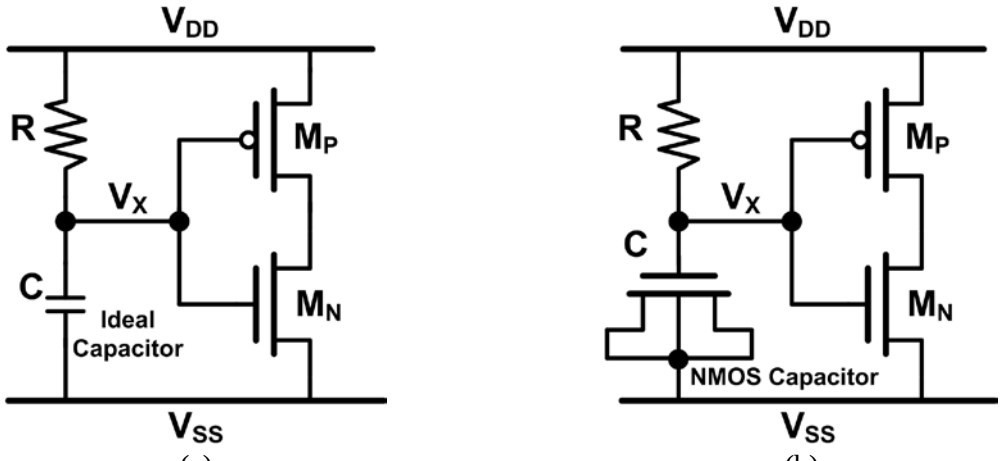
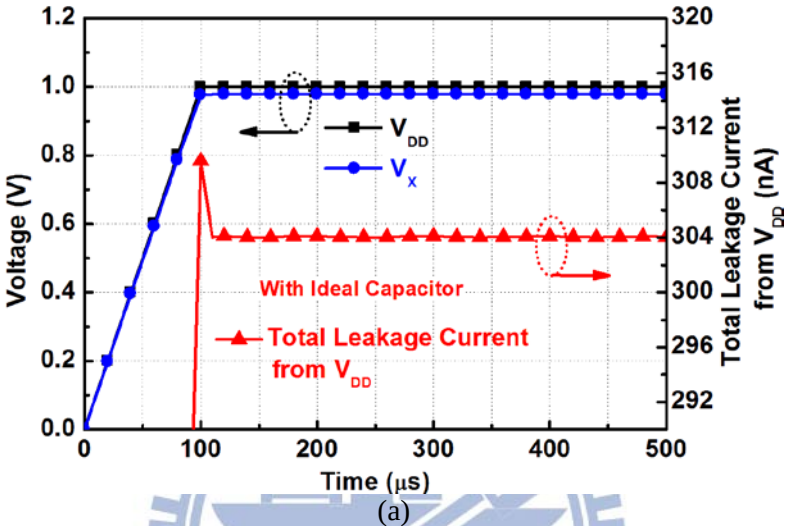


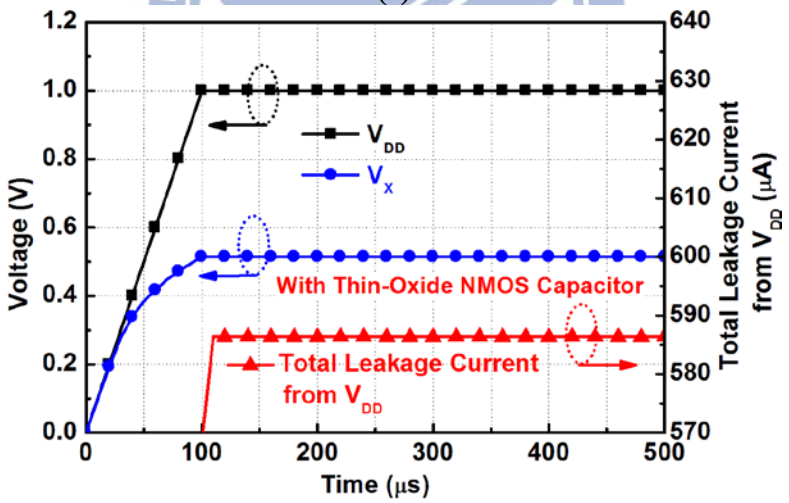

Fig. 2.2. Circuit schematic of traditional RC-based ESD-detection circuit with (a) ideal capacitor and (b) NMOS capacitor.

Table 2.1
Device dimensions used in ESD-detection circuits for HSPICE simulation

| Type | R | C | $M_P$ (W/L) | $M_N$ (W/L) |
|---|---|---|---|---|
| With Ideal Capacitor | 100 kΩ | 2 pF | $\frac{100\ \mu m}{0.15\ \mu m}$ | $\frac{20\ \mu m}{0.15\ \mu m}$ |
| With NMOS Capacitor | 100 kΩ | 2pF $\left(\frac{29\ \mu m}{28\ \mu m}\right)$ | $\frac{100\ \mu m}{0.15\ \mu m}$ | $\frac{20\ \mu m}{0.15\ \mu m}$ |




(a)




(b)

Fig. 2.3. Simulated transient waveforms of the ESD-detection circuit with (a) ideal capacitor and (b) thin-oxide NMOS capacitor under normal power-on conditions in a 65-nm CMOS process.

## 2.2. ESD Clamp Circuit with Extremely-Low Leakage Capacitor

Capacitor is one of the basic components in IC applications. To meet different purposes of circuit applications, various types of capacitors have been developed with their own characteristics. Due to the limitation of capacitance per unit area, capacitors always occupy a considerable chip area in the whole circuit layout of CMOS ICs. Therefore, saving the chip

area is the important consideration in capacitor selection of CMOS ICs. Nowadays, three kinds of capacitors are commonly used in IC applications, which are MOS capacitor, metal-insulator-metal (MIM) capacitor, and metal-oxide-metal (MOM) capacitor. Among those capacitors, because of thin gate oxide structure, MOS capacitor has the highest capacitance density per unit area. However, due to the disadvantages of nonlinearity, higher temperature coefficient, lower breakdown voltage, and sensitive to process variations, it could not be suitable for all circuit applications. As a result, MIM capacitor and MOM capacitor were created to overcome those disadvantages for circuit applications, which need reliable capacitor characteristics [51]-[56]. When the CMOS process shrinks toward nanoscale, the capacitance density of the MOS capacitor ideally will be increased when the gate oxide becomes thinner. But, thinner gate oxide makes the gate direct tunneling issue more serious to cause obvious gate leakage current in the devices. To avoid the influence of gate leakage issue, the simple method is using the thick-oxide device to realize the MOS capacitor. However, without using the dual oxide devices in some special purposes for circuit applications, the capacitors can only be realized by MIM or MOM capacitors. But, the capacitance densities of MIM and MOM capacitors are much lower than that of the MOS capacitor. Consequently, using MIM or MOM capacitors would increase more chip area to IC products. Fortunately, with the dimension shrinkage in advanced CMOS processes, the lateral and vertical intervals between metal interconnects are decreased, and the parasitic capacitance between metal interconnects are increased. This feature assists the MOM capacitor to extend its capacitance density. Furthermore, with the layout structure near the fractal geometries, the MOM capacitor can have the largest capacitance density in advanced CMOS processes [51].

### 2.2.1 Investigation of Metal-Layer Capacitors in a 65-nm CMOS process

With the parallel-plate structure, the MIM capacitor is composed of two metal plates and a dielectric layer between them, as shown in Fig. 2.4. In order to realize the structure with a shorter distance (D) and a different dielectric material ($\varepsilon_X$) to enhance the capacitance density, the fabrication of MIM capacitor needs additional fabrication masks to define the top and bottom metal plates. Different to the MIM capacitor, the MOM capacitor is realized through the metal interconnections, as shown in Fig. 2.5. Ideally, every pair of metal lines can form the MOM capacitor. In the early generation of CMOS processes, the lateral and vertical intervals between metal layers were not close enough, the capacitance density of MOM

capacitor was very low. However, with the dimension shrinkage in advanced CMOS processes, the parasitic capacitance between metal interconnections is increased significantly. For example, in a 0.25-μm CMOS technology, the minimum width (W) and space (S) of metal layers is 0.4 μm. When the technology shrank to 65-nm, the minimum W and S of metal layers were decreased to 0.1 μm. Besides, the MOM capacitor can be stacked with several metal layers ($M_Y$) to increase the capacitance density in advanced CMOS technology.

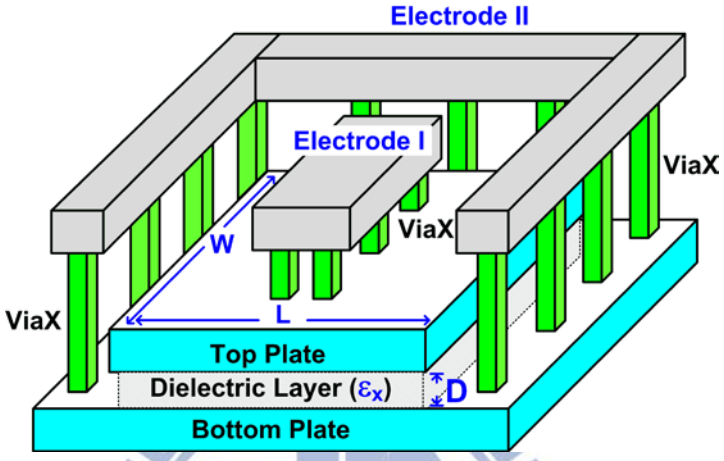



Fig. 2.4. Schematic of MIM capacitor.

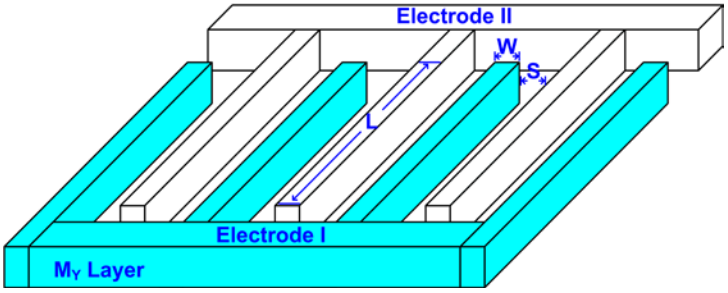



Fig. 2.5. Schematic of MOM capacitor.

Various types of MOM capacitors have been developed with different configurations to increase the horizontal or vertical surface area [57]-[61]. The structure of MOM capacitor used in this work is shown in Fig. 2.6 [59]. In the same metal layer, the lateral capacitance ($C_{LY}$) between the adjacent metal lines is shown in Fig. 2.7(a). In different metal layers, the vertical capacitance ($C_{AY-1}$) is shown in Fig. 2.7(b). With this kind of arrangement, the MOM capacitor takes the advantage of both the lateral and vertical fields to extend the capacitance density. The capacitance is estimated as

$$C_{Lateral} = L \times (F_X - 1) \times C_{LY},$$

$$C_{Vertical} = L \times F_X \times C_{AY-1}, \text{ and}$$

$$C_{Total} = C_{Lateral} + C_{Vertical}. \quad (2.1)$$

The $F_X$ is finger numbers. L is metal length. $C_{LY}$ is coupling capacitance per unit length between the metal lines in the same metal layer. The $C_{AY-1}$ is area capacitance per unit length between metal layers. Table 2.2 shows the estimated results of device layout area with different capacitors. With more metal layers stacked, the MOM capacitor can have the smallest area to achieve the desired capacitance.

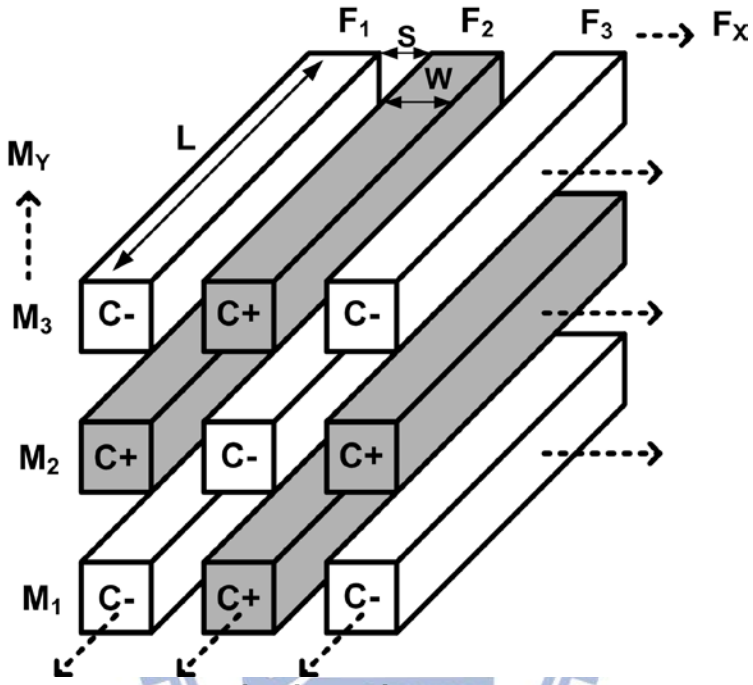



Fig. 2.6. MOM capacitor structure used in this work.

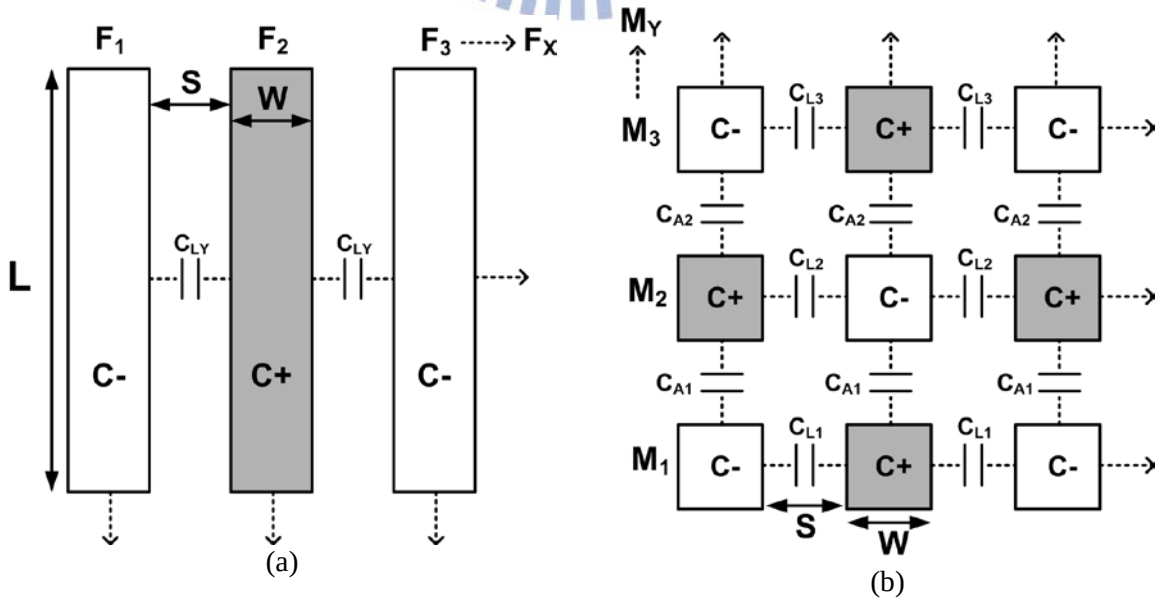



Fig. 2.7. MOM capacitor structure layout (a) top view and (b) cross-sectional view.

Table 2.2
Estimated layout area of capacitors with different capacitances in a 65-nm CMOS process

| Capacitor Type | $C_{eq}$ | $M_Y$ | Area | Capacitor Type | $C_{eq}$ | $M_Y$ | Area |
|---|---|---|---|---|---|---|---|
| MOM Cap. | ~ 1 pF | 3 | ~ 27 μm x 28 μm | MIM Cap. | ~ 1 pF | | ~ 25 μm x 25 μm |
| | | 4 | ~ 23 μm x 24 μm | | ~ 2 pF | | ~ 34 μm x 34 μm |
| | | 5 | ~ 21 μm x 22 μm | | ~ 5 pF | | ~ 52 μm x 52 μm |
| | ~ 2 pF | 3 | ~ 36 μm x 37 μm | MOS Cap. (NMOS 1V) | ~ 1 pF | | ~ 26 μm x 28 μm |
| | | 4 | ~ 32 μm x 33 μm | | ~ 2 pF | | ~ 34 μm x 37 μm |
| | | 5 | ~ 29 μm x 30 μm | | ~ 5 pF | | ~ 48 μm x 55 μm |
| | ~ 5 pF | 3 | ~ 57 μm x 58 μm | | | | |
| | | 4 | ~ 50 μm x 51 μm | | | | |
| | | 5 | ~ 45 μm x 46 μm | | | | |

## 2.2.2 Low-Leakage ESD clamp Circuit with MOM capacitor

The proposed low-leakage ESD clamp circuit with MOM capacitor ($C_1$) is shown in Fig. 2.8, which consists of the ESD-detection circuit with MOM capacitor and the substrate-triggered silicon-controlled rectifier (STSCR) as the ESD protection device. Without the thin gate oxide in the P-N-P-N structure, SCR has very low leakage current under normal circuit operating conditions. Besides, SCR had been proven to have the highest ESD robustness under the smallest device size [62]. The cross-sectional view of the STSCR device is shown in Fig. 2.9.

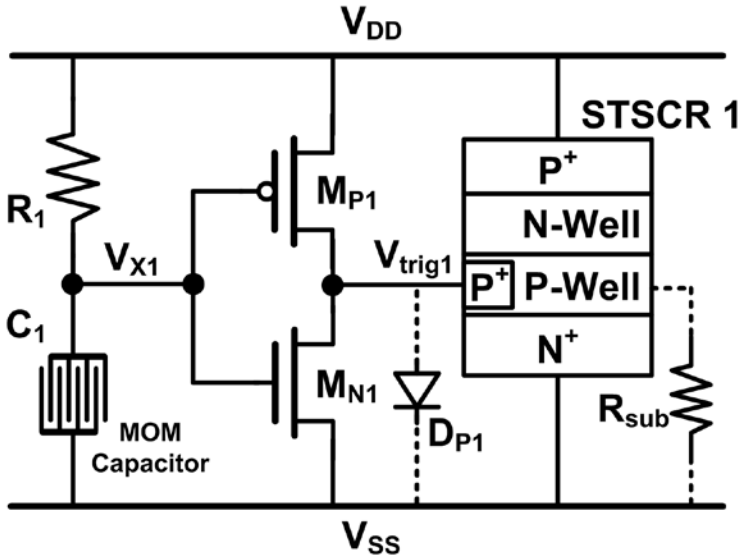



Fig. 2.8. Low-leakage ESD clamp circuit with MOM capacitor ($C_1$).

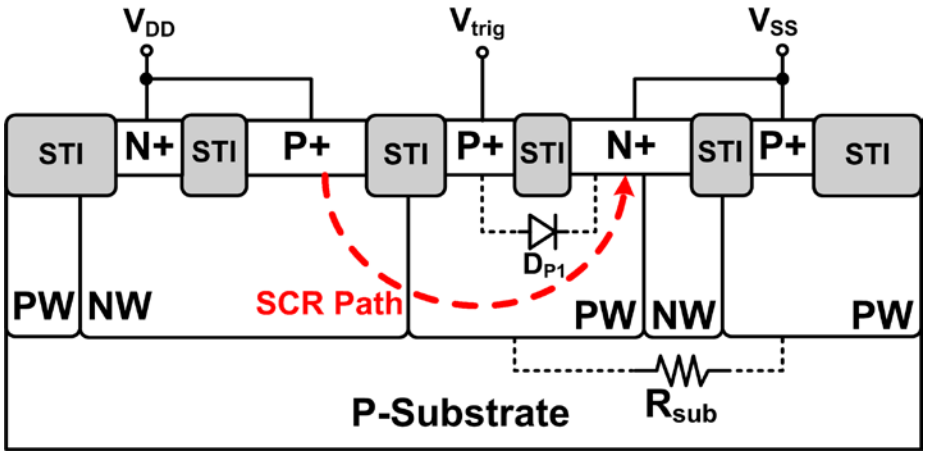



Fig. 2.9. Device cross-sectional view of STSCR.

Under the normal $V_{DD}$ power-on conditions, the $V_{DD}$ power-on voltage waveform has a rise time in the order of millisecond (ms). With a slow rise time of the normal power-on transient, the voltage level at $V_x$ can follow up the $V_{DD}$ voltage waveform in time to keep $M_{P1}$ off. Simultaneously, the $M_{N1}$ is turned on because its gate terminal is connected to $V_x$. Therefore, no trigger current will inject to the STSCR. The STSCR can be kept off under normal circuit operating conditions. To observe the behavior under normal power-on conditions, Fig. 2.10 shows the simulated transient waveforms of the low-leakage ESD-detection circuit with MOM capacitor in a 65-nm HSPICE model. With a rise time of 0.1 ms and the power-supply voltage of 1 V, the Vx can follow the power-on waveform to near $V_{DD}$ voltage of 1 V. Thus, the simulated overall leakage current of the ESD-detection circuit is only 307 nA at 25 °C.

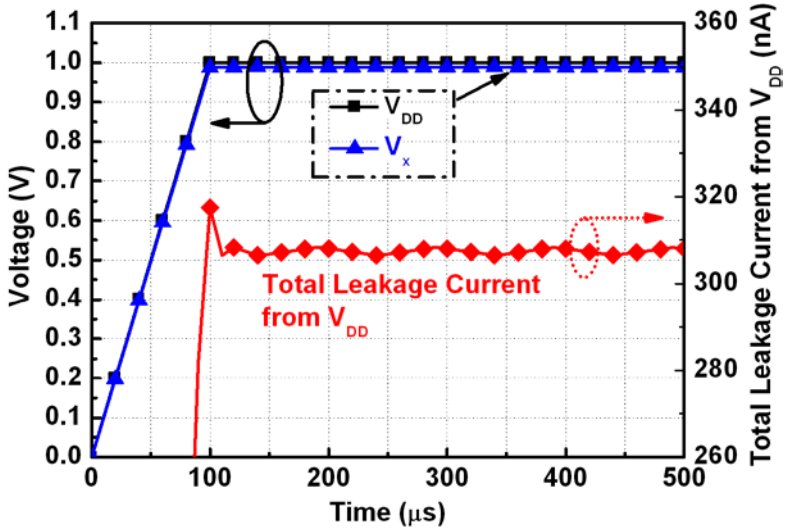



Fig. 2.10. Simulated transient waveforms of the ESD-detection circuit under normal power-on conditions.

Under the ESD-stress event, the ESD voltage has a rise time in the order of nanosecond (ns). Due to the RC delay, the voltage level of $V_X$ will be much slower than the voltage level at $V_{DD}$ when the ESD stress is conducted across $V_{DD}$ and $V_{SS}$ power lines. With the relatively lower voltage level kept at $V_X$, the PMOS ($M_{P1}$) in the ESD-detection circuit will turn on to provide the trigger signal into the STSCR. Consequently, the turned-on STSCR will provide a low-impedance path to discharge ESD current from $V_{DD}$ to $V_{SS}$. Although the equivalent circuit model of STSCR device is needed to preciously simulate the quasi-static trigger point and the clamping voltage during high-current conditions, the P-well/N+ diode ($D_P$) and P-substrate resistor ($R_{sub}$) can be used to represent the STSCR device before it turned on. Thus, the trigger ability of ESD-detection circuit with $D_{P1}$ and $R_{sub}$ can be simulated. To observe the circuit behavior under the ESD-like stress conditions, Fig. 2.11 shows the simulated transient waveforms of the low-leakage ESD-detection circuit with MOM capacitor in a 65-nm HSPICE model. When a 5-V voltage pulse with 10-ns rise time and 100-ns pulse width is applied to $V_{DD}$, which is used to simulate the rising edge of ESD event before device oxide breakdown, the ESD-detection circuit can successfully provide the trigger current of ~40 mA for the STSCR.

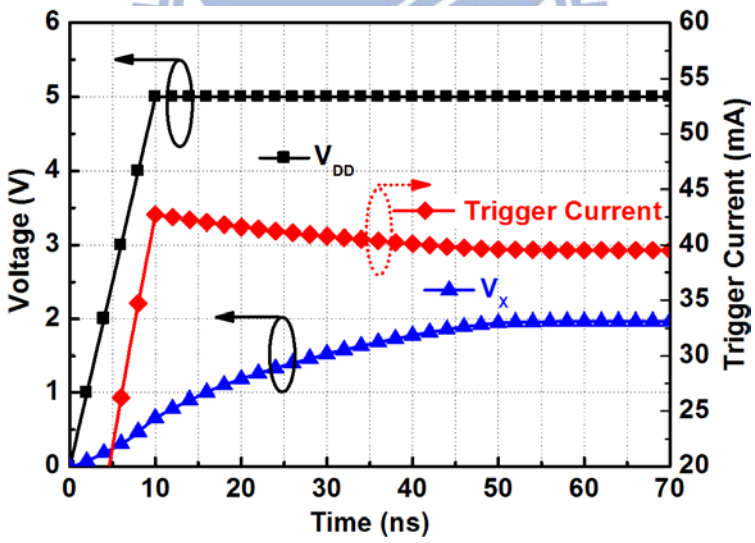



Fig. 2.11. Simulated transient waveforms of the ESD-detection circuit under ESD-like stress conditions.

### 2.2.3 Experimental Results

To investigate the capacitance of different metal-layer capacitors, the test devices of MIM and MOM capacitors had been fabricated in the silicon chip with a 65-nm CMOS process. In addition, for observing the gate leakage of MOS capacitor, the stand-alone PMOS and NMOS capacitors were also included in the test chip. Moreover, to investigate the impact

of gate leakage issue in RC-based ESD-detection circuit, two ESD clamp circuits with MOM capacitor and thin-oxide NMOS capacitor were implemented in the test chip with only thin-oxide devices, as shown in Fig. 2.12. All device dimensions used in the ESD clamp circuits are listed in Table 2.3. With a capacitance of 2 pF, the layout area of MOM capacitor realized with 3 metal layers is 36 μm x 37 μm. The thin-oxide NMOS capacitor was implemented with a similar layout area of 34 μm x 37 μm (channel width $W_C$ = 29 μm and channel length $L_C$ = 28 μm). Except the capacitor, all devices used in these two circuits have the identical device dimensions. The chip micrograph of test devices and the fabricated ESD clamp circuits is shown in Fig. 2.13.

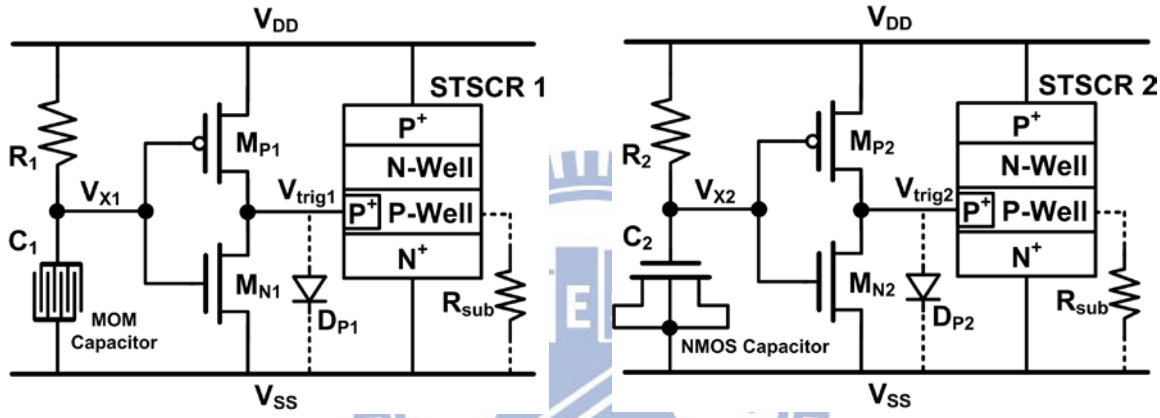



Fig. 2.12. RC-based ESD clamp circuit with (a) MOM capacitor and (b) thin-oxide NMOS capacitor.

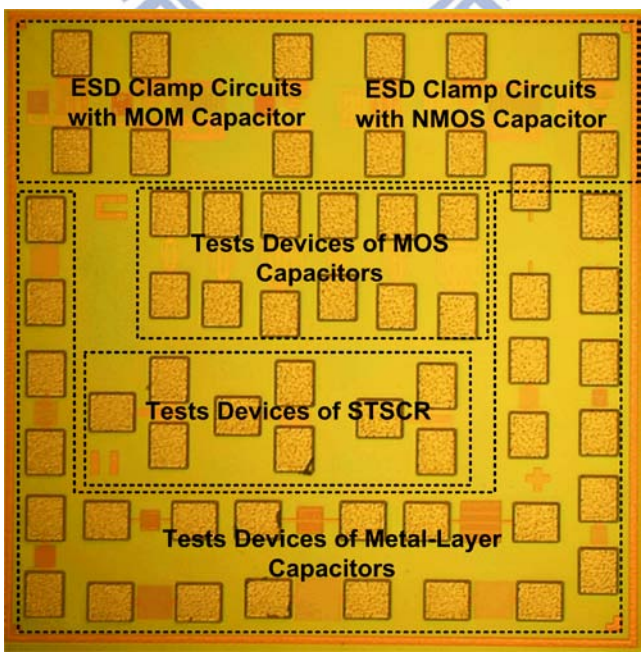



Fig. 2.13. Chip micrograph of the fabricated test devices and the ESD clamp circuits in a 65-nm CMOS process.

Table 2.3
Device dimensions used in the ESD clamp circuits

| Circuit Type | Resistor | Capacitor (Area) | PMOS | NMOS | ESD Device |
|---|---|---|---|---|---|
| With MOM Capacitor Fig. 2.12(a) | $R_1$ | $C_1$ | $M_{P1}$ | $M_{N1}$ | STSCR 1 |
| | 100 kΩ | 36 μm / 37 μm | 100 μm / 0.15 μm | 20 μm / 0.15 μm | 40 μm / 7.8 μm |
| With NMOS Capacitor Fig. 2.12(b) | $R_2$ | $C_2$ | $M_{P2}$ | $M_{N2}$ | STSCR 2 |
| | 100 kΩ | 34 μm / 37 μm | 100μm / 0.15 μm | 20 μm / 0.15 μm | 40 μm / 7.8 μm |

### 2.2.3.1 Measured Capacitance of Metal-Layer Capacitors

Table 2.4 shows the measured capacitance of two metal-layer capacitors under the bias voltage ($V_B$) at -1 V, 0 V, and 1 V (at a reference frequency of 100-kHz and temperature of 25 °C). Even the temperature was heated to 125 °C, each capacitor has the stable capacitance as the values shown in Table 2.4. However, with the different reference frequencies in the measurement, the capacitance variations of two capacitors are quite different. The measured capacitances under the reference frequencies of 100-kHz and 500-kHz at 0-V bias are summarized in Table 2.5. More capacitance variation is observed in MOM capacitors when the frequency is increased. The maximum variation in MOM capacitor is 0.88 %, but the variation in MIM capacitor is only 0.1 %.

In addition to the capacitor's structure, the dielectric materials within two capacitors are also different. Due to the MOM capacitor is realized from the metal interconnects, the dielectric layers are mainly formed by $SiO_2$ and low-k materials [63]. But, in the MIM capacitor, the dielectric layer was often implemented with the high-k materials to increase the capacitance density [64]. Some relative studies had been reported that the frequency dependencies were various with different materials to cause the capacitance loss [52], [65]. However, the characteristics of different materials were not further analyzed in this work. Besides, compared to the evaluated capacitances, more capacitances are measured in MOM capacitors. Thus, the accuracy of capacitance estimation (2.1) in MOM capacitor should be further improved. However, the occupied area of MOM capacitor actually can be the smallest one when more metal layers were used.

Table 2.4

Measured capacitances of MIM and MOM capacitors under the bias voltage of -1 V, 0 V, and 1 V (at reference frequency of 100-kHz)

| Type | $C_{eq}$ | $C_{measured}$ | | | $M_Y$ | Area | $C_{measured}$ per unit area |
|---|---|---|---|---|---|---|---|
| | | $V_B$ = -1 V | $V_B$ = 0 V | $V_B$ = 1 V | | | |
| MOM Cap. | ~ 1 pF | ~ 1.14 pF | ~ 1.14 pF | ~ 1.14 pF | 3 | 27 μm x 28 μm | ~ 1.51 fF/μm$^2$ |
| | | ~ 1.15 pF | ~ 1.15 pF | ~ 1.15 pF | 4 | 23 μm x 24 μm | ~ 2.08 fF/μm$^2$ |
| | | ~ 1.17 pF | ~ 1.17 pF | ~ 1.17 pF | 5 | 21 μm x 22 μm | ~ 2.53 fF/μm$^2$ |
| | ~ 2 pF | ~ 2.27 pF | ~ 2.27 pF | ~ 2.27 pF | 3 | 36 μm x 37 μm | ~ 1.70 fF/μm$^2$ |
| | | ~ 2.30 pF | ~ 2.30 pF | ~ 2.30 pF | 4 | 32 μm x 33 μm | ~ 2.18 fF/μm$^2$ |
| | | ~ 2.35 pF | ~ 2.35 pF | ~ 2.35 pF | 5 | 29 μm x 30 μm | ~ 2.70 fF/μm$^2$ |
| | ~ 5 pF | ~ 5.71 pF | ~ 5.71 pF | ~ 5.71 pF | 3 | 57 μm x 58 μm | ~ 1.73 fF/μm$^2$ |
| | | ~ 5.72 pF | ~ 5.72 pF | ~ 5.72 pF | 4 | 50 μm x 51 μm | ~ 2.24 fF/μm$^2$ |
| | | ~ 5.74 pF | ~ 5.74 pF | ~ 5.74 pF | 5 | 45 μm x 46 μm | ~ 2.77 fF/μm$^2$ |
| MIM Cap. | ~ 1 pF | ~ 0.997 pF | ~ 0.997 pF | ~ 0.997 pF | | 25 μm x 25 μm | ~ 1.60 fF/μm$^2$ |
| | ~ 2 pF | ~ 1.973 pF | ~ 1.973 pF | ~ 1.973 pF | | 34 μm x 34 μm | ~ 1.71 fF/μm$^2$ |
| | ~ 5 pF | ~ 4.990 pF | ~ 4.990 pF | ~ 4.990 pF | | 52 μm x 52 μm | ~ 1.85 fF/μm$^2$ |

Table 2.5

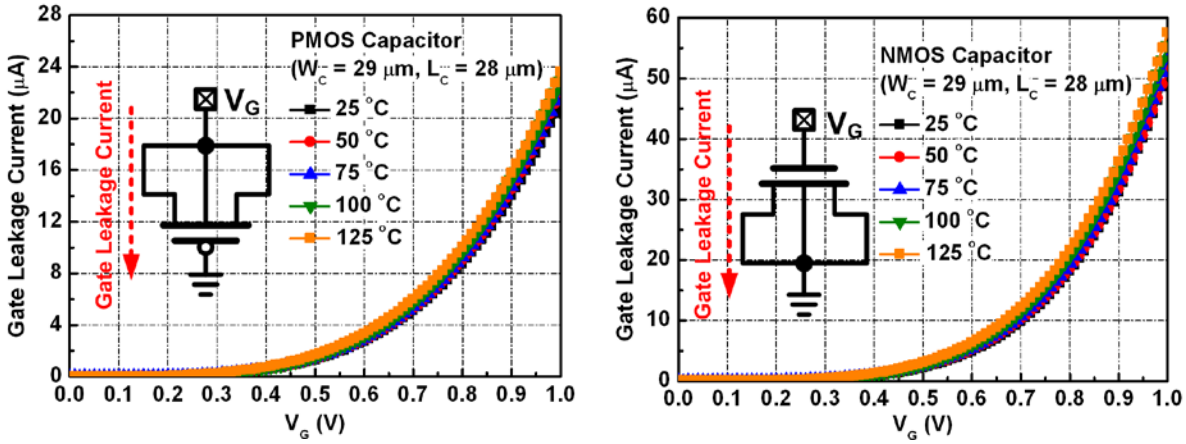
Measured capacitances of MIM and MOM capacitors under different reference frequencies

| Type | $C_{eq}$ | $C_{Measured}$ | | | $M_Y$ | Area | $C_{measured}$ per unit area | |
|---|---|---|---|---|---|---|---|---|
| | | @ 100 kHz | @ 500 kHz | Variation | | | @ 100 kHz | @ 500 kHz |
| MOM Cap. | ~ 1 pF | ~ 1.14 pF | ~ 1.13 pF | ~ 0.88% | 3 | 27 μm x 28 μm | ~ 1.51 fF/μm$^2$ | ~ 1.49 fF/μm$^2$ |
| | | ~ 1.15 pF | ~ 1.14 pF | ~ 0.87% | 4 | 23 μm x 24 μm | ~ 2.08 fF/μm$^2$ | ~ 2.07 fF/μm$^2$ |
| | | ~ 1.17 pF | ~ 1.16 pF | ~ 0.85% | 5 | 21 μm x 22 μm | ~ 2.53 fF/μm$^2$ | ~ 2.51 fF/μm$^2$ |
| | ~ 2 pF | ~ 2.27 pF | ~ 2.25 pF | ~ 0.85% | 3 | 36 μm x 37 μm | ~ 1.70 fF/μm$^2$ | ~ 1.69 fF/μm$^2$ |
| | | ~ 2.30 pF | ~ 2.28 pF | ~ 0.87% | 4 | 32 μm x 33 μm | ~ 2.18 fF/μm$^2$ | ~ 2.16 fF/μm$^2$ |
| | | ~ 2.35 pF | ~ 2.33 pF | ~ 0.85% | 5 | 29 μm x 30 μm | ~ 2.70 fF/μm$^2$ | ~ 2.68 fF/μm$^2$ |
| | ~ 5 pF | ~ 5.71 pF | ~ 5.67 pF | ~ 0.7% | 3 | 57 μm x 58 μm | ~ 1.73 fF/μm$^2$ | ~ 1.72 fF/μm$^2$ |
| | | ~ 5.72 pF | ~ 5.68 pF | ~ 0.7% | 4 | 50 μm x 51 μm | ~ 2.24 fF/μm$^2$ | ~ 2.23 fF/μm$^2$ |
| | | ~ 5.74 pF | ~ 5.69 pF | ~ 0.85% | 5 | 45 μm x 46 μm | ~ 2.77 fF/μm$^2$ | ~ 2.75 fF/μm$^2$ |
| MIM Cap. | ~ 1 pF | ~ 0.997 pF | ~ 0.996 pF | ~ 0.1% | | 25 μm x 25 μm | ~ 1.60 fF/μm$^2$ | ~ 1.59 fF/μm$^2$ |
| | ~ 2 pF | ~ 1.973 pF | ~ 1.972 pF | ~ 0.05% | | 34 μm x 34 μm | ~ 1.71 fF/μm$^2$ | ~ 1.71 fF/μm$^2$ |
| | ~ 5 pF | ~ 4.990 pF | ~ 4.986 pF | ~ 0.08% | | 52 μm x 52 μm | ~ 1.85 fF/μm$^2$ | ~ 1.84 fF/μm$^2$ |

### 2.2.3.2 Leakage Current Measurement

Figs. 2.14(a) and 2.14(b) show the measured gate leakage currents of the stand-alone thin-oxide (1-V) PMOS and NMOS capacitors ($W_C$ = 29 μm and $L_C$ = 28 μm) with the gate oxide thickness of ~20 Å in a 65-nm CMOS process. Under 1 V bias across the MOS capacitor, the gate leakage currents of PMOS and NMOS capacitors at 25 °C are 21.2 μA and 50.9 μA, respectively. The leakage currents among the fabricated capacitors under 1 V bias and different temperatures are summarized in Table 2.6. With such huge leakage current through the MOS capacitor, the thin-oxide MOS capacitor is no longer suitable for circuit

applications in the 65-nm CMOS process. On the contrary, without the thin-oxide structure in MIM and MOM capacitors, these two capacitors' leakage currents are quite low (< 20 pA).




(a) (b)

Fig. 2.14. Measured gate leakage current of the thin-oxide (a) PMOS and (b) NMOS capacitor in a 65-nm CMOS process under different temperatures.

Table 2.6
Measured leakage currents amount fabricated capacitors under different temperatures

| Leakage Current at $V_G$ = 1V | 25 °C | 50 °C | 75 °C | 100 °C | 125 °C |
|---|---|---|---|---|---|
| NMOS Cap. (~ 2pF) ( Layout area of 34 μm x 37 μm) | 50.9 μA | 51.3 μA | 53.3 μA | 55.5 μA | 57.6 μA |
| PMOS Cap. (~ 2pF) (Layout area of 34 μm x 37 μm) | 21.2 μA | 22.0 μA | 22.2 μA | 22.9 μA | 23.6 μA |
| MIM Cap. (~ 2pF) (Layout area of 34 μm x 34 μm ) | < 20 pA | < 20 pA | < 20 pA | < 20 pA | < 20 pA |
| MOM Cap. (~ 2pF) (Layout area of 36 μm x 37 μm ) | < 20 pA | < 20 pA | < 20 pA | < 20 pA | < 20 pA |

The leakage currents between two ESD clamp circuits under different temperatures with $V_{DD}$ of 1 V are compared in Fig. 2.15. The leakage currents are also summarized in Table 2.7. Comparing with the leakage current of the stand-alone thin-oxide NMOS capacitor, much higher leakage current (828 μA at 25 °C) was observed in the ESD clamp circuit with NMOS capacitor, which indicates that the leaky MOS capacitor certainly causes extra leakage paths in the ESD-detection circuit. On the contrary, with extremely-low leakage current in MOM capacitor, the ESD clamp circuit with MOM capacitor has the lowest leakage current of only 358 nA. The total leakage current of the ESD protection design with MOM capacitor is three orders smaller than that with NMOS capacitor from low temperature to high temperature.

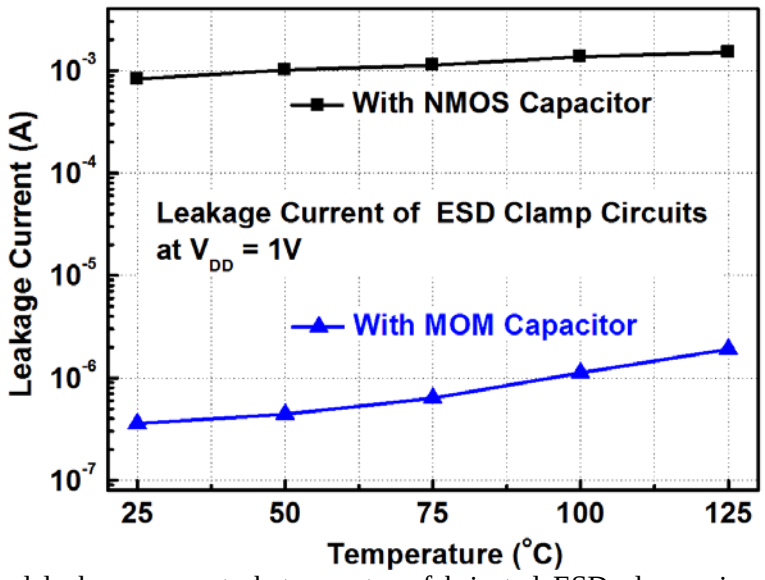



Fig. 2.15. Measured leakage currents between two fabricated ESD clamp circuits under different temperatures.

Table 2.7

Measured leakage currents and ESD robustness of the ESD clamp circuits

| Circuit Type | Leakage Current at $V_{DD}$ = 1V | | | | | ESD Robustness | |
|---|---|---|---|---|---|---|---|
| | 25 °C | 50 °C | 75 °C | 100 °C | 125 °C | HBM | MM |
| With NMOS Capacitor | 828 μA | 1.01 mA | 1.13 mA | 1.36 mA | 1.13 mA | 4 kV | 350 V |
| With MOM Capacitor | 358 nA | 441 nA | 633 nA | 1.12 μA | 1.91 μA | 4 kV | 350 V |

### 2.2.3.3 ESD Robustness

To investigate the turn-on behavior of the ESD protection device with ESD-detection circuit during ESD event, the transmission line pulse (TLP) with 100-ns pulse width and 10-ns rise time was used to measure the second breakdown current ($I_{t2}$) of ESD protection circuits [66]. The TLP-measured I-V characteristics of the STSCR with and without the ESD-detection circuit are shown in Fig. 2.16. Without any trigger signal, the original trigger voltage ($V_{t1}$) of stand-alone STSCR (width = 40 μm) device is 10.7 V, and the $I_{t2}$ is 2.3 A. With the trigger signal from ESD-detection circuit, the $V_{t1}$ of the STSCR device is significantly reduced to 3 V and the $I_{t2}$ is 2.5 A. The lower $V_{t1}$ of the ESD clamp circuit ensures its effective ESD protection capability. In addition, the holding voltage of STSCR is ~2.5 V, so the proposed ESD clamp circuit is free from latchup issue in the CMOS ICs with $V_{DD}$ of 1 V. The human-body-model (HBM) and machine-model (MM) ESD levels of these two ESD clamp circuits are evaluated by the ESD simulator. Measured ESD levels are also

listed in Table 2.7. The failure criterion is defined as 30 % shift in the leakage current under 1-V $V_{DD}$ bias. The ESD clamp circuit with STSCR of only 40-μm width can achieve ESD robustness of 4 kV in HBM test and 350 V in MM test.

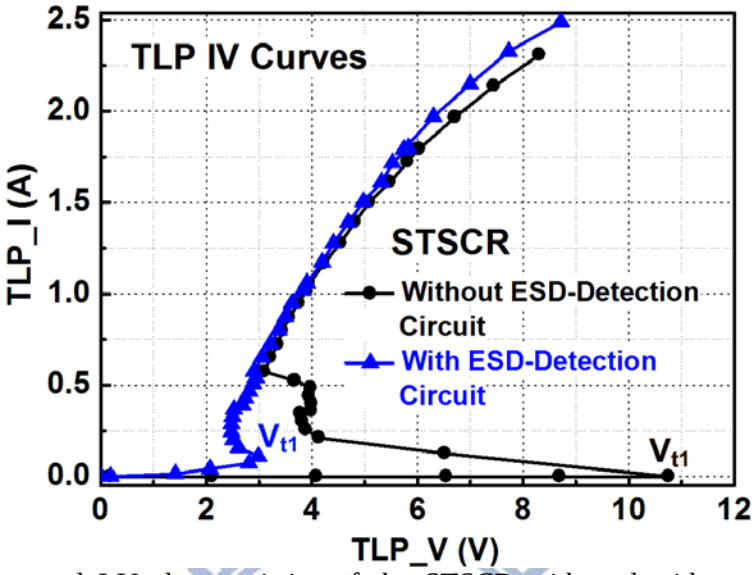



Fig. 2.16. TLP-measured I-V characteristics of the STSCR with and without the ESD-detection circuit.

## 2.3. Gate Leakage Restraint by Circuit Technique for ESD Clamp Circuit

The previous study had addressed the impact of gate leakage on the ESD clamp circuit, and it also reported a modified design to solve the gate leakage issue [13]. As shown in Fig. 2.17, an additional PMOS restorer ($M_{PR1}$) in the ESD-detection circuit had been proposed to pull high the voltage level at $V_{X3}$. As a result, $M_{P3}$ could be effectively turned off under normal circuit operating conditions and to decrease the overall leakage current. With the similar idea, another design used the feedback circuit to reduce the required capacitor size in ESD-detection circuit [67]. Moreover, the other design used the current amplification technique in ESD-detection circuit which could further reduce the required capacitor size [68]. By those circuit techniques, the impact of the leaky MOS capacitor in nanoscale CMOS processes could be mitigated by decreasing the capacitor's size. Thus, those ideals could be adapt to decrease the leakage current in ESD clamp circuits. However, the voltage across the MOS capacitor in ESD-detection circuit is still at a high voltage level under normal circuit operating conditions. The gate leakage current through the MOS capacitor still exists in those previous designs.

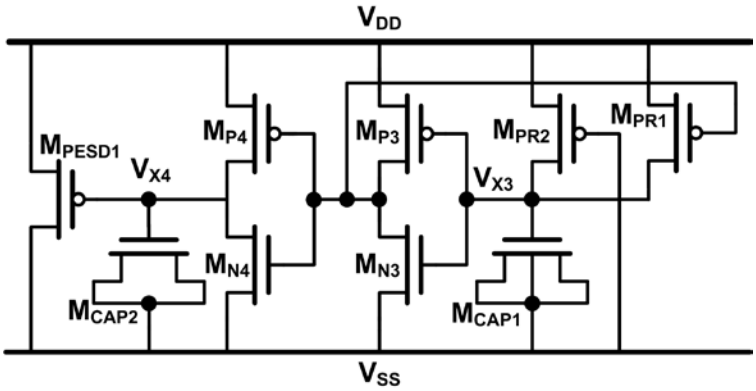



Fig. 2.17. Modified ESD clamp circuit with the PMOS restorer ($M_{PR1}$).

### 2.3.1 Gate Direct Tunneling Components in BSIM4 MOSFET Model

Various gate direct tunneling components included in BSIM4 MOSFET model are illustrated in Fig. 2.18. Those components are gate-to-substrate current ($I_{gb}$), the edge direct tunneling current ($I_{gd}$ and $I_{gs}$), and the gate-to-channel current ($I_{gc}$). Considering to drain and source bias effect, $I_{gc}$ is split to $I_{gcd}$ and $I_{gcs}$.

The $I_{gb}$ is partitioned into two conditions when MOS devices in accumulation ($I_{gbacc}$) or in inversion ($I_{gbinv}$). Two current functions are given by

$$I_{gbinv} = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gb} \cdot V_{aux} \cdot \exp\left[-B \cdot TOXE(AIGBINV - BIGBINV \cdot V_{oxdepinv}) \cdot \left(1 + CIGBINV \cdot V_{oxdepinv}\right)\right] \quad \text{.....(2.2)}$$

$$I_{gbinv} = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gb} \cdot V_{aux} \cdot \exp\left[-B \cdot TOXE(AIGBINV - BIGBINV \cdot V_{oxdepinv}) \cdot \left(1 + CIGBINV \cdot V_{oxdepinv}\right)\right] \quad \text{.....(2.3)}$$

The $I_{gd}$ and $I_{gs}$ are given by

$$I_{gd} = W_{eff} DLCIGD \cdot A \cdot T_{oxRatioEdge} \cdot V_{gd} \cdot V_{gd'} \cdot \exp\left[-B \cdot TOXE \cdot POXEDGE \cdot (AIGD - BIGD \cdot V_{gd'})(1 + CIGD \cdot V_{gd'})\right] \quad \text{..... .....(2.4)}$$

$$I_{gs} = W_{eff} DLCIG \cdot A \cdot T_{oxRatioEdge} \cdot V_{gs} \cdot V_{gs'} \cdot \exp\left[-B \cdot TOXE \cdot POXEDGE \cdot (AIGS - BIGS \cdot V_{gs'})(1 + CIGS \cdot V_{gs'})\right] \quad \text{..... .....(2.5)}$$

The Igc is given by

$$I_{gc} = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gse} \cdot V_{aux} \cdot \exp\left[-B \cdot TOXE(AIGC - BIGC \cdot V_{oxdepinv}) \cdot \left(1 + CIGC \cdot V_{oxdepinv}\right)\right] \quad \text{..(2.6)}$$

When considerate of drain and source bias effect, the Igcd and Igcs are given by

$$I_{gcd} = I_{gc0} \cdot \frac{1 - (PIGCD \cdot V_{dseff} + 1) \cdot \exp(-PIGCD) + 1.0e^{-4}}{PIGCD^2 \cdot V_{dseff}{}^2 + 2.0e^{-4}} \quad \text{..... .....(2.7)}$$

$$I_{gcs} = I_{gc0} \cdot \frac{PIGCD \cdot V_{dseff} + \exp(-PIGCD) - 1 + 1.0e^{-4}}{PIGCD^2 \cdot V_{dseff}{}^2 + 2.0e^{-4}} \quad \text{.....(2.8)}$$

The $I_{gc0}$ means the $I_{gc}$ current without the drain to source voltage (Vds) bias.

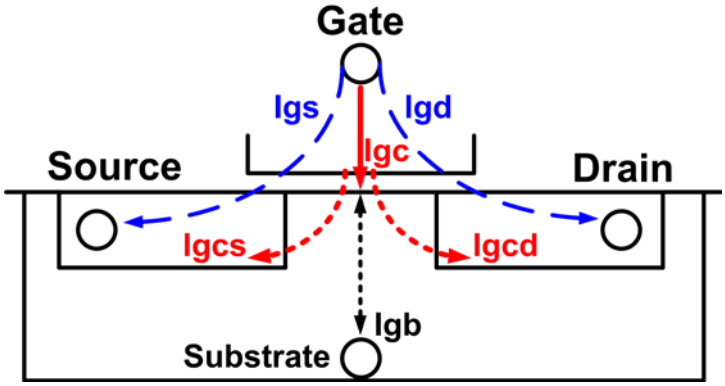



Fig. 2.18. Illustration of gate direct tunneling components in MOSFET.

### 2.3.2 Low-Leakage ESD Clamp Circuit with Circuit Bias Technique

Although those previous works could mitigate the gate leakage issue, the ESD-detection circuits still used the MOS capacitor configuration. When the ESD-detection circuit with MOS capacitor fabricated in the nanoscale low-voltage CMOS process, the MOS capacitor always conducts some leakage current, because there is still a voltage drop across the MOS capacitor under normal circuit operating conditions. When observing the equations of gate direct tunneling currents in BSIM4 MOSFET model, each current is increased with a great proportion to the voltage across the MOS capacitor. If the voltage across the MOS capacitor could be reduced, the leakage current will be decreased. Based on this concept, new low-leakage ESD clamp circuits with the circuit bias technique are proposed.

#### 2.3.3.1 Diode-String Bias Circuit

Fig. 2.19 shows the proposed low-leakage ESD clamp circuit with diode string bias circuit. It consist with a new low-leakage ESD-detection circuit with diode-string bias circuit and a STSCR as ESD protection device, where the MOS capacitor ($M_{CAP3}$) is connected between the $V_{A1}$ and $V_{B1}$ nodes. The diode string bias circuit is formed with diode-connected PMOS transistors ($M_{diode}$). The static current through $M_{diode}$ could be mitigated by increasing device channel length and number of the stacked PMOS transistors. With enough diode-connected PMOS transistors bias at $V_{B1}$ terminal, the voltage across the MOS capacitor could be decreased to reduce the gate leakage current. Thus, the impact of leaky MOS

capacitor could be mitigated to further enhance the turn-off ability in the circuit.

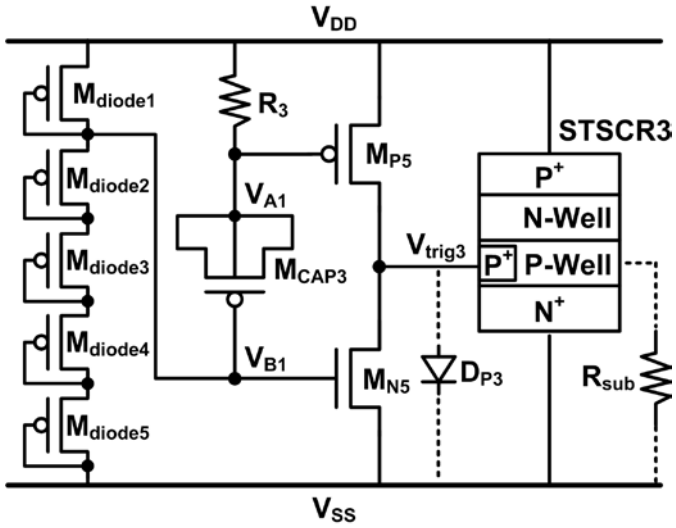



Fig. 2.19. Proposed low-leakage ESD clamp circuit with diode string bias circuit.

To observe the circuit behavior under power-on conditions, Fig. 2.20 shows the simulated transient waveforms of the low-leakage ESD-detection circuit with diode-string bias circuit in a 65-nm HSPICE model. Due to the bias circuit provides the bias voltage at $V_{B1}$ terminal, the voltage across the MOS capacitor is decreased. Moreover, the diode string bias circuit could limit the leakage current from MOS capacitor. Therefore, the leakage current through the $M_{CAP3}$ could be significantly reduced. Without large leakage current through the $M_{CAP3}$, the voltage at $V_{A1}$ terminal can be charged to $V_{DD}$ to fully turn off the inverter PMOS ($M_{P5}$). As a result, the simulated leakage current shows a low leakage current of 215 nA under $V_{DD}$ of 1 V at 25 °C.

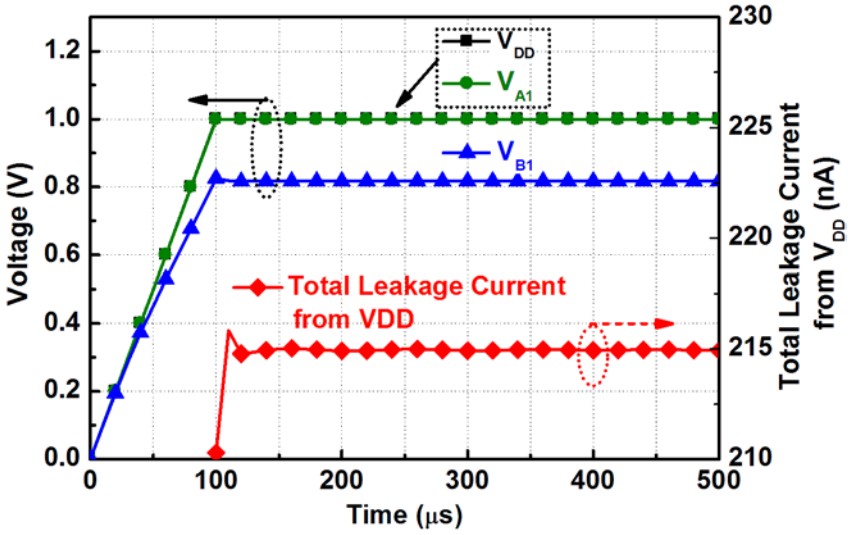



Fig. 2.20. Simulated transient waveforms of the low-leakage ESD-detection circuit with diode string bias circuit under normal power-on conditions.

Since RC-delay and the PMOS $M_{P5}$ is initially turned-on, the proposed design could provide the trigger current for STSCR during ESD stresses. To observe the circuit behavior under ESD-like stress conditions, Fig. 2.21 shows the simulated transient waveforms of low-leakage ESD-detection circuit with diode-string bias circuit in a 65-nm HSPICE model. When a 5-V voltage pulse with 10-ns rise time and 100-ns pulse width is applied to $V_{DD}$, the proposed low-leakage ESD-detection circuit can successfully provide the trigger current for the STSCR. However, without a direct DC path to ground for MOS capacitor, and the quick turn-on diode string, the $V_{A1}$ and $V_{B1}$ voltages are immediately coupled up. Therefore, the trigger ability of the low-leakage deign is decreased.

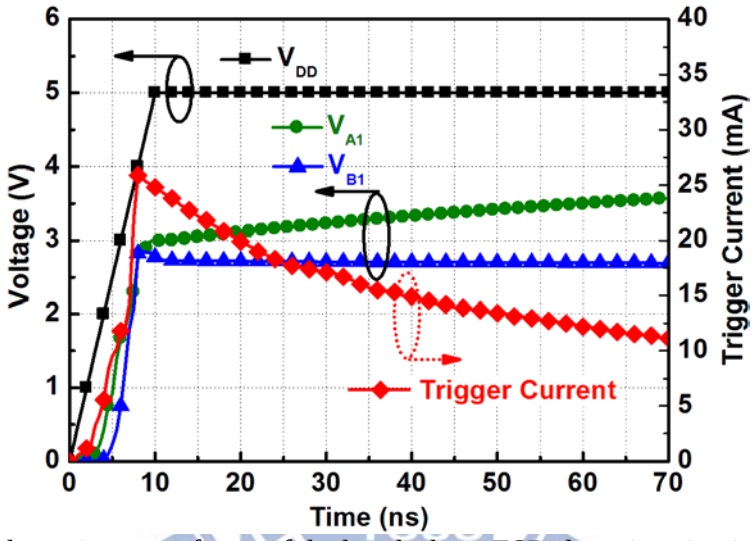



Fig. 2.21. Simulated transient waveforms of the low-leakage ESD-detection circuit with diode string bias circuit under ESD-like stress conditions.

### 2.3.3.2 Feedback-Control Bias Circuit

To improve the trigger ability in the ESD-detection circuit, a new low-leakage ESD clamp circuit with feedback-control bias circuit is proposed in Fig. 2.22. In this new low-leakage ESD-detection circuit, the RC-based ESD-detection circuit and the feedback-control inverter are combined together. Under a slow rise time of the normal power-on transient, the voltage levels at $V_{A2}$ will be able to follow the $V_{DD}$ voltage in time to keep the PMOS $M_{PS}$ off. Moreover, the parasitic P-substrate resistor ($R_{sub}$) and P-well/N+ diode ($D_{P4}$) at trigger node $V_{trig4}$ in the STSCR can pull the $V_{trig4}$ to $V_{SS}$. Therefore, the $M_{P7}$ would be turned on to drive $V_{B2}$ to $V_{DD}$. With the $V_{B2}$ voltage of $V_{DD}$, the PMOS $M_{P6}$ can be fully turned off. Consequently, there is no voltage drop across MOS capacitor $M_{CAP4}$ and no circuit leakage path exists in the new ESD-detection circuit. To observe the circuit behavior under normal power-on conditions, Fig. 2.23 shows the simulated transient waveforms of the

low-leakage ESD-detection with feedback-control bias circuit in a 65-nm HSPICE model. With a rise time of 0.1 ms and the power-supply voltage of 1 V, the relative circuit functions let $V_{A2}$ and $V_{B2}$ follow up the $V_{DD}$ voltage to fully turn off $M_{P6}$ and $M_{PS}$. Thus, the simulated overall leakage current under $V_{DD}$ of 1 V is only 104 nA at 25 °C.

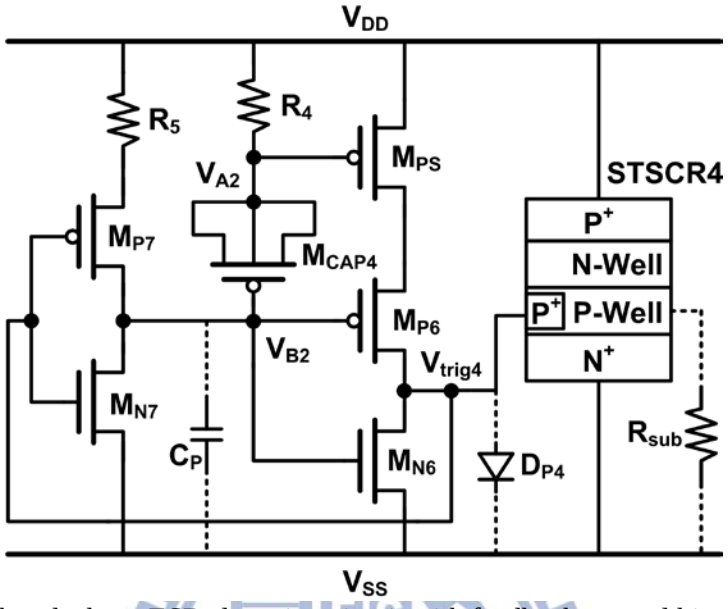



Fig. 2.22. Proposed low-leakage ESD-detection circuit with feedback-control bias circuit.

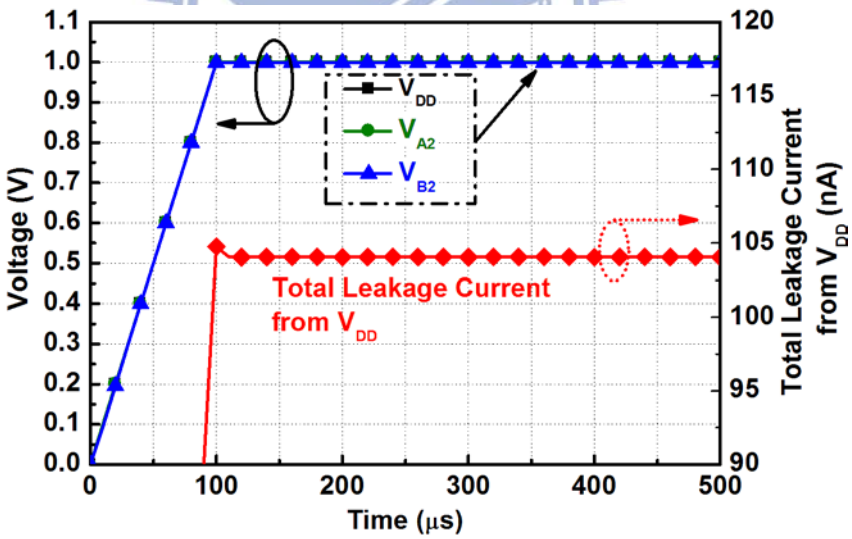



Fig. 2.23. Simulated transient waveforms of the low-leakage ESD-detection circuit with feedback-control bias circuit under normal power-on conditions.

Before ESD event, the capacitor should have no voltage across it, and the nodes $V_{A2}$ and $V_{B2}$ have the same voltage levels (~0V) at the beginning. Therefore, the PMOS $M_{P6}$ and $M_{PS}$ have the ability to initially turn on. Besides, the voltage division divided by $R_4$ and $M_{CAP4}$, or even the parasitic capacitor ($C_P$) are able to let $V_{A2}$ and $V_{B2}$ at a relatively low voltage levels when facing the fast transient of ESD pulse. With the $V_{A2}$ and $V_{B2}$ at relatively low voltage

levels, the $M_{P6}$ and $M_{PS}$ can be turned on to generate the trigger signal to trigger on the STSCR and also to turn on the NMOS $M_{N7}$. As $M_{N7}$ turned on, $V_{B2}$ will be further kept at low voltage level. Moreover, through the leaky $M_{CAP4}$, the voltage at $V_{A2}$ is also kept at low voltage level. Therefore, $M_{P6}$ and $M_{PS}$ can be continually turned on to provide trigger current to STSCR. Something that is worth to be mentioned, by using the leaky MOS capacitor in the new ESD-detection circuit, the new proposed circuit can continually provide the trigger current into STSCR. With such a circuit arrangement, the leakage current of the leaky MOS capacitor becomes one advantage in this ESD-detection circuit under ESD stresses. Fig. 2.24 shows the simulated transient waveforms of the low-leakage ESD-detection circuit with feedback-control bias circuit under ESD-like stress conditions. When a 5-V voltage pulse with 10-ns rise time and 100-ns pulse width is applied to $V_{DD}$, the new ESD-detection circuit successfully provide the trigger current into the STSCR. Due to the circuit functions and the leaky MOS capacitor's characteristic, the simulated trigger current is continually provided.

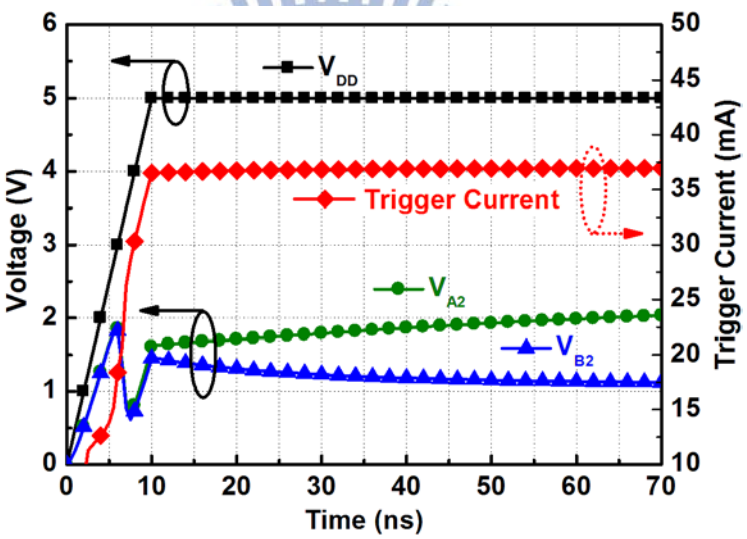



Fig. 2.24. Simulated transient waveforms of the low-leakage ESD-detection circuit with feedback-control bias circuit under ESD-like stress conditions.

### 2.3.3 Experimental Results

Four test circuits of low-leakage ESD clamp circuit with diode-string bias circuit (Low-Leakage Design I), low-leakage ESD clamp circuit with feedback-control bias circuit (Low-Leakage Design II), traditional ESD clamp circuit (Traditional Design), and modified ESD clamp circuit with PMOS restorer (Modified Design With Restorer) had been drawn in the test chip and fabricated in a 65-nm CMOS process, as shown in Fig. 2.25. All devices are fully-silicided thin-oxide (1-V) device without using the additional silicide-blocking mask. The main device dimensions are listed in Table 2.8. The chip micrograph of the fabricated

ESD clamp circuits and test devices is shown in Fig. 2.26. Each ESD clamp circuit drawn in the layout format of I/O cell occupies the same cell area of 30 μm × 110 μm.

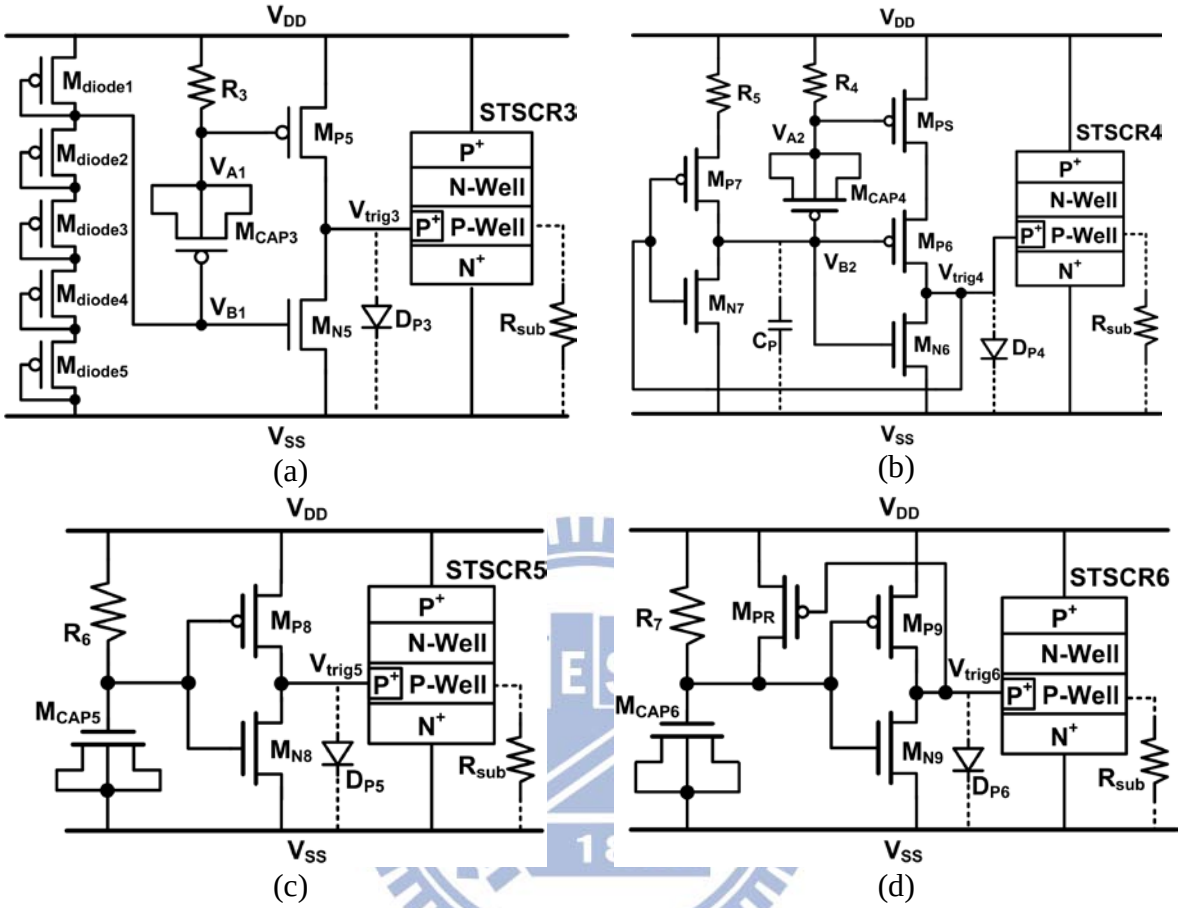



Fig. 2.25. Four test circuits of low-leakage ESD clamp circuit with diode-string bias circuit (Low-Leakage Design I), low-leakage ESD clamp circuit with feedback-control bias circuit (Low-Leakage Design II), traditional ESD clamp circuit (Traditional Design), and modified ESD clamp circuit with PMOS restorer (Modified Design With Restorer).

Table 2.8
Main device dimensions of fabricated ESD clamp circuits

| | | | | | | |
|---|---|---|---|---|---|---|
| Low-Leakage Design I Fig. 2.25(a) | $R_3$ | $M_{CAP3}$ (W / L) | $M_{P5}$ (W / L) | $M_{N5}$ (W / L) | $M_{dioden}$ (W / L) | STSCR3 (W x L x M) |
| | 20 kΩ | 30 μm / 25 μm | 100 μm / 0.15 μm | 5 μm / 0.15 μm | 0.2 μm / 1 μm | 60 μm x 3.9 μm x 2 |
| Low-Leakage Design II Fig. 2.25(b) | $R_4$ | $M_{CAP4}$ (W / L) | $M_{P6}$ (W / L) | $M_{N6}$ (W / L) | $M_{PS}$ (W / L) | STSCR4 (W x L x M) |
| | 20 kΩ | 30 μm / 25 μm | 100 μm / 0.15 μm | 5 μm / 0.15 μm | 100 μm / 0.15 μm | 60 μm x 3.9 μm x 2 |
| Traditional Design Fig. 2.25(c) | $R_6$ | $M_{CAP5}$ (W / L) | $M_{P8}$ (W / L) | $M_{N8}$ (W / L) | | STSCR5 (W x L x M) |
| | 20 kΩ | 30 μm / 25 μm | 100 μm / 0.15 μm | 5 μm / 0.15 μm | | 60 μm x 3.9 μm x 2 |
| Modified Design With Restorer Fig. 2.25(d) | $R_7$ | $M_{CAP6}$ (W / L) | $M_{P9}$ (W / L) | $M_{N9}$ (W / L) | $M_{PR}$ (W / L) | STSCR6 (W x L x M) |
| | 20 kΩ | 30 μm / 25 μm | 100 μm / 0.15 μm | 5 μm / 0.15 μm | 5 μm / 0.15 μm | 60 μm x 3.9 μm x 2 |

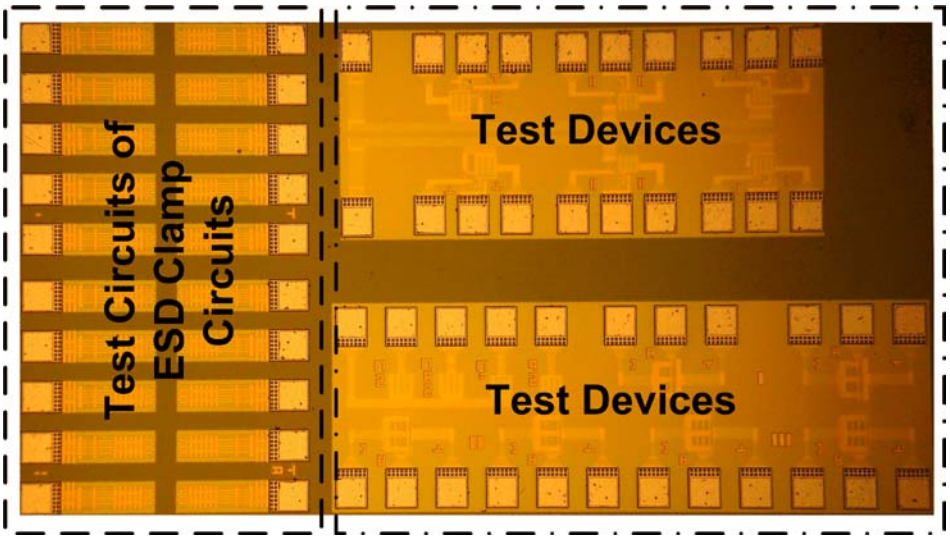


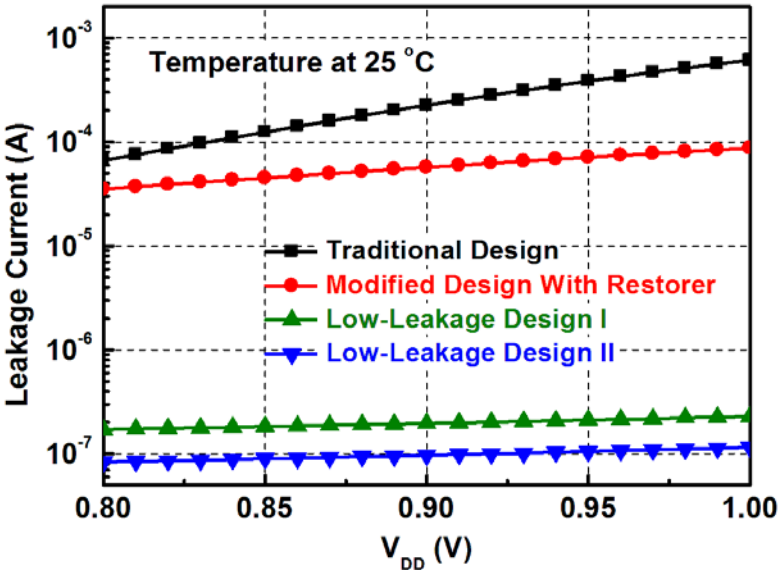
Fig. 2.26. Chip micrograph of the fabricated ESD clamp circuits and test devices.

#### 2.3.3.1 Leakage Current Measurement

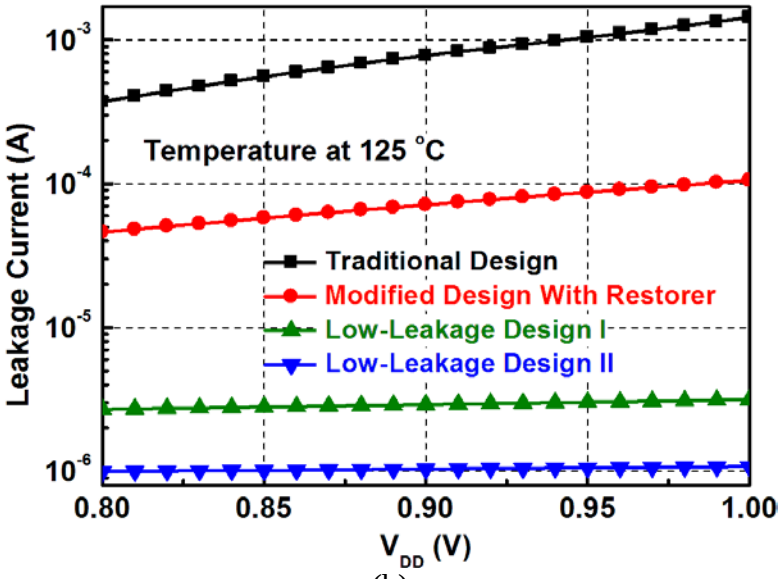
The measured overall leakage currents among those fabricated ESD clamp circuits under $V_{DD}$ voltages from 0.8 V to 1.0 V at 25 °C and 125 °C are shown in Figs. 2.27(a) and 2.27(b), respectively. The leakage currents of those ESD clamp circuits under 1-V $V_{DD}$ voltage at 25 °C and 125 °C are also summarized in Table 2.9. Although the leakage current is reduced in the modified design with PMOS restorer (Fig. 2.25(d)), it is still as high as 88 μA under 1-V $V_{DD}$ bias at 25 °C. Compared with the traditional design and the modified design with restorer, the leakage current of low-leakage design I is 228 nA (3.14 μA) at 25 °C (125 °C) and the leakage current of low-leakage design II is 116 nA (1.08 μA) at 25 °C (125 °C). According to the measured results, the low-leakage design II has the best capability to suppress the gate leakage issue of thin-oxide MOS capacitor in the ESD clamp circuit.

Table 2.9
Measured leakage currents among the fabricated ESD clamp circuits

| Leakage Current at $V_{DD}$ = 1V | 25 °C | 125 °C |
|---|---|---|
| Traditional Design | 613 μA | 1.43 mA |
| Modified Design With Restorer | 88 μA | 106 μA |
| Low-Leakage Design I | 228 nA | 3.14 μA |
| Low-Leakage Design II | 116 nA | 1.08 μA |




(a)




(b)

Fig. 2.27. Measured leakage currents among those fabricated ESD clamp circuits at (a) 25°C and (b) 125°C.

### 2.3.3.2 ESD Robustness

The HBM and MM ESD levels of fabricated ESD clamp circuits are listed in Table 2.10. The failure criterion is defined as 30 % shift in the leakage current under 1-V $V_{DD}$ bias. The ESD test results have confirmed that the proposed low-leakage designs have good ESD level of over 8 kV in HBM test and over 750 V in MM test. The TLP-measured I-V characteristics of low-leakage design I and low-leakage design II are shown in Fig. 2.28. Without any trigger signal, the original $V_{t1}$ of the STSCR device is as high as 10.2 V. With the new low-leakage ESD-detection circuits, the $V_{t1}$ of the STSCR device can be significantly reduced. The second

breakdown currents $I_{t2}$ of two designs are over 5 A. Thus, the lower $V_{t1}$ and higher $I_{t2}$ ensure its effective ESD protection capability.

Table 2.10
Measured HBM and MM ESD robustness among the fabricated ESD clamp circuits

| ESD Robustness | HBM | MM |
|---|---|---|
| Traditional Design | 6 kV | 600 V |
| Modified Design With Restorer | > 8 kV | 750 V |
| Low-Leakage Design I | > 8 kV | 750 V |
| Low-Leakage Design II | > 8 kV | 800 V |

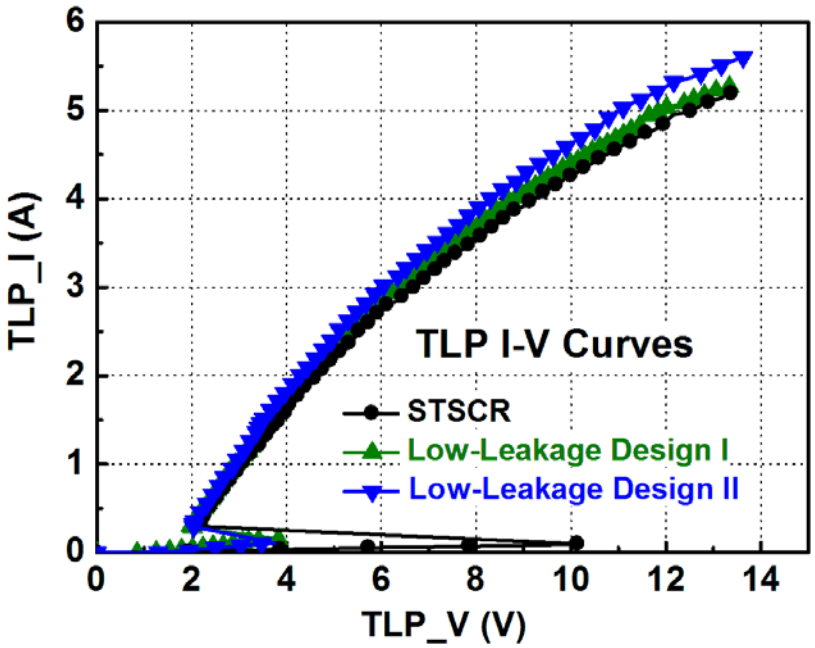


Fig. 2.28. TLP-measured I-V characteristics of low-leakage ESD clamp circuits.

#### 2.3.3.3 Turn-on Verification and Transient-Induced Latch-Up (TLU) Measurement

To verify the turn-on speed of two low-leakage ESD clamp circuits, a voltage pulse with fast rise time is applied to the $V_{DD}$ node to emulate the ESD-like stress. When a 5-V ESD-like voltage pulse with 2-ns rise time and 100-ns pulse width is applied to $V_{DD}$ with $V_{SS}$ grounded, the ESD-detection circuit starts to inject the trigger current to turn on the STSCR. Thus, the turned-on STSCR provides a low-impedance path to clamp the $V_{DD}$ power line at lower voltage level. Each low-leakage design can rapidly clamp the voltage level to around ~2.5 V

within 5 ns as shown in Fig. 2.29. With low enough clamped voltage level, the internal circuits can be well protected by the low-leakage designs under ESD stresses. In addition, with the clamping voltage of ~2.5 V, the STSCR does not have the latchup trouble in 1-V IC applications.

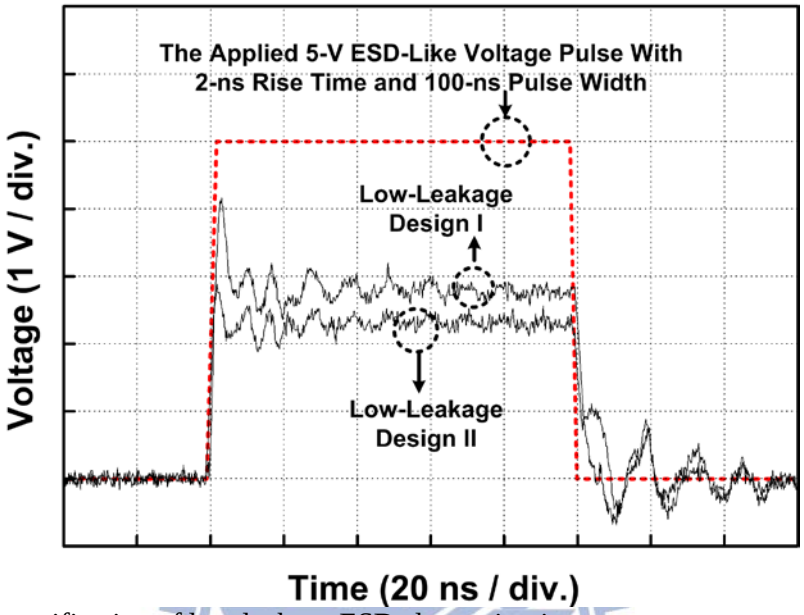
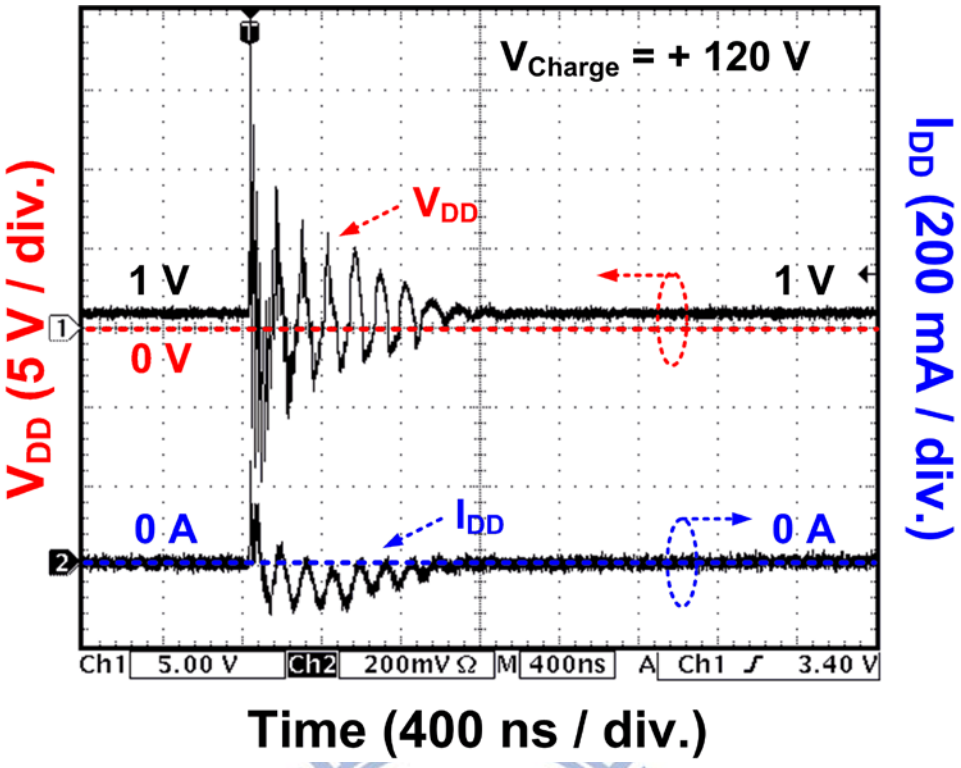
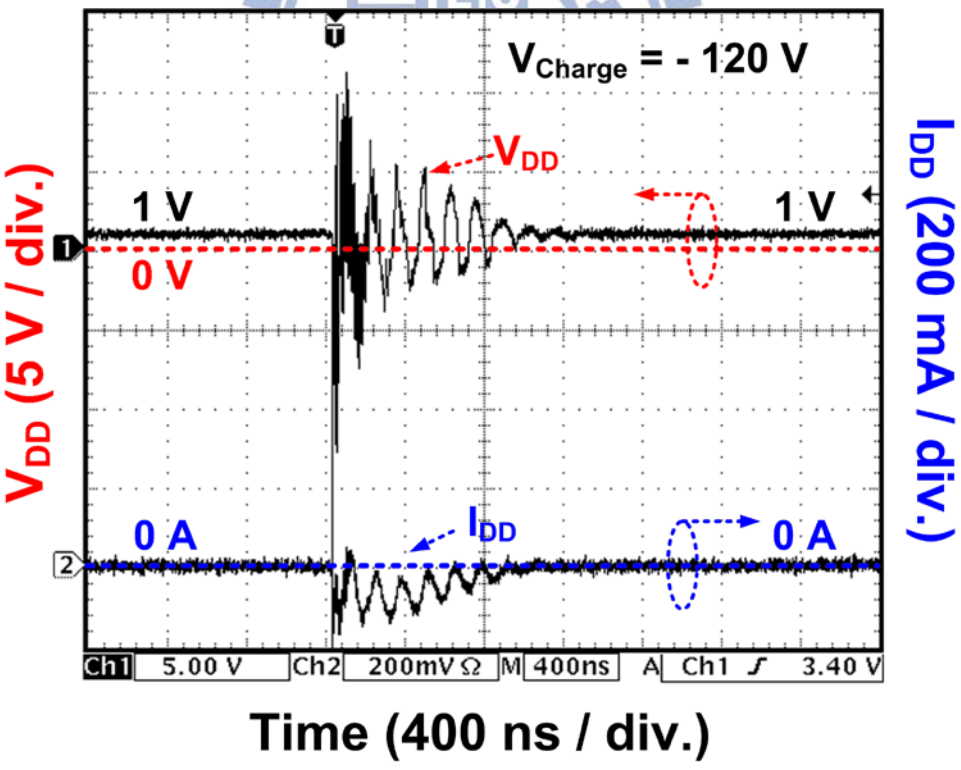



Fig. 2.29 Turn-on verification of low-leakage ESD clamp circuits.

Transient-induced latchup (TLU) test has been used to investigate the susceptibility of ICs against the noise transient or glitch on the power lines under normal circuit operating conditions. The component-level TLU measurement setup [69] can accurately simulate the ESD-induced noises on the power lines of CMOS ICs under system-level ESD test. The ESD clamp circuit with the latch technique was reported to enhance circuit performance [67]. Nevertheless, transient-induced latchup-like failure may happen in such circuit structure. With the charge voltage ($V_{Charge}$) around 10 V (negative or positive) under the TLU test, the latchup-like failure on some ESD clamp circuits has been studied [70]. The low-leakage dsign II also combined the feedback control as a latch structure, but it will not suffer such latchup-like issue. Any latchup-like issue will be quickly released by the $R_{sub}$ and $D_{P4}$ at the $V_{trig4}$ node of STSCR, when it is operated in the normal circuit operating conditions. The TLU measured results of the low-leakage design II are shown in Fig. 2.30. After the TLU test, the $V_{DD}$ voltage level is returned back to 1 V and the $I_{DD}$ current is kept at 0 A. Even with the $V_{Charge}$ as high as 120 V (negative or positive) in the TLU test, the latchup-like issue is not occurred in the low-leakage design II.




(a)




(b)

Fig. 2.30. Measured $V_{DD}$ and $I_{DD}$ waveforms of the low-leakage design II under TLU test with $V_{Charge}$ of (a) +120 V and (b) -120 V.

## 2.4. Discussion

When comparing the evaluated results of MOM capacitor (Table 2.2), more capacitance was observed in the measured results (Table 2.4). In equation (2.1), each finger's edge capacitance was ignored. To obtain more accurate capacitance in this structure, the capacitance estimation of MOM capacitor should be fixed to the following equations, where $C_{FE}$ is the capacitance from all finger's edge. Thus, the maximum capacitance variation is decreased from 14.9% to 5.8% as shown in Table 2.11.

$$C_{Lateral} = L \times (F_X - 1) \times C_{LY},$$

$$C_{Vertical} = L \times F_X \times C_{AY-1},$$

$$C_{FE} = F_X \times M_Y \times C_{Edge}, \text{ and}$$

$$C_{Total} = C_{Lateral} + C_{Vertical} + C_{FE}. \quad (2.9)$$

Table 2.11
The percentage of capacitance variation within the estimations

| $M_Y$ (Metal Layers) | | 3 | 4 | 5 | 3 | 4 | 5 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|---|---|---|---|
| $C_{Measured}$ | | 1.14 pF | 1.15 pF | 1.17 pF | 2.27 pF | 2.30 pF | 2.35 pF | 5.71 pF | 5.72 pF | 5.74 pF |
| Capacitance Variation | In (2.1) | 12.3 % | 13 % | 14.5 % | 11.9 % | 13 % | 14.9 % | 12.4 % | 12.6 % | 12.9 % |
| | In (2.2) | 1.8 % | 2.6 % | 3.4 % | 2.6 % | 2.2 % | 2.6 % | 5.8 % | 4.8 % | 4.2 % |

From the perspective on commercial IC products, to achieve strong reliability is necessary for product qualification. In order to against the influence of process variations and various operation environments, the circuit design demands more reliable considerations. Although the experimental results showed satisfied ESD robustness in the low-leakage ESD clamp circuit with feedback-control bias circuit (Fig. 2.22), some modifications could be added into the design to enhance circuit ability. Fig. 2.31 shows a kind of modification with gate-couple technique. When the ESD pulse is applied to the $V_{DD}$ with $V_{SS}$ grounded, the voltage of $V_C$ will be coupled up and turns on the $M_{N3}$ to force the $V_B$ to low voltage level. Therefore, the modified design will provide trigger signal more effectively than before. With suitable gate-couple technique design, the response capability of the low-leakage ESD detection circuit with feedback-control bias circuit under ESD event will be enhanced.

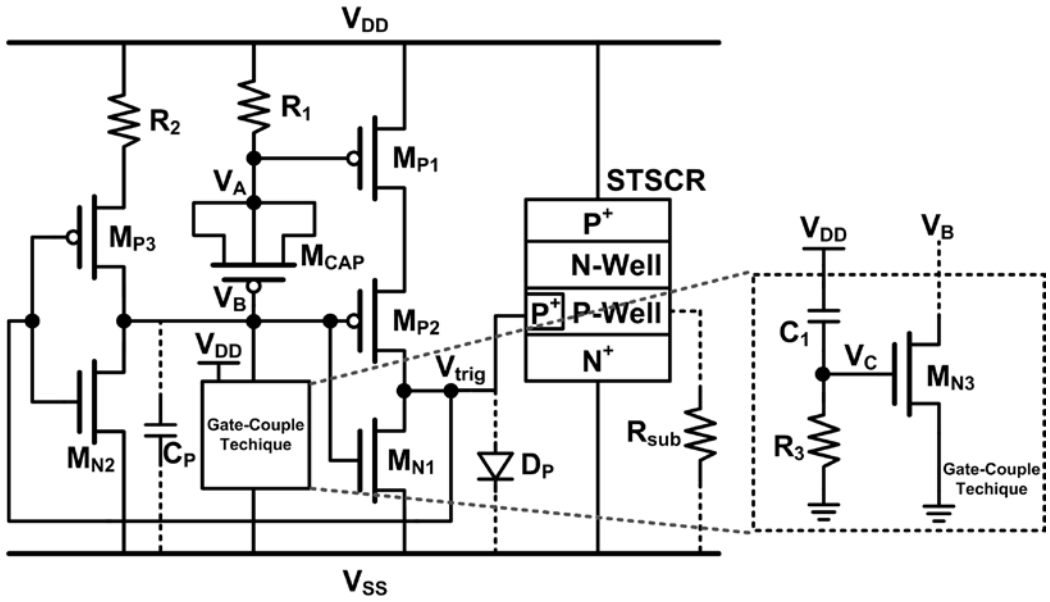



Fig. 2.31. Modified design of low-leakage ESD clamp circuit with feedback-control bias circuit.

Among the proposed low-leakage ESD clamp circuits, some features are compared in the Table 2.12.

Table 2.12
Comparisons of low-leakage ESD clamp circuits

| ESD Clamp Circuit | | Area | Additional Mask | Leakage Current | Implement Complexity | Fabrication Cost |
|---|---|---|---|---|---|---|
| With Metal-Layer Capacitor | MIM | Large | Yes | Low | Low | High |
| | MOM | Medium | No | Low | Meium | Low |
| With Circuit Bias Technique | Design I | Small | No | Low | Meium | Low |
| | Design II | Medium | No | Very Low | High | Low |

## 2.5. Summary

In this chapter, two modification concepts for low-leakage ESD clamp circuit had been proposed and verified in 65-nm CMOS processes. By using the metal interconnects in advanced CMOS processes, the MOM capacitor can be easily realized without the additional fabrication masks in processes. When more metal layers stacked, the MOM capacitor can have the smallest area to achieve the desired capacitance. With the advantages of higher capacitance density and lower fabrication cost, the MOM capacitor is more suitable for general circuit applications in nanoscale CMOS processes. By using the MOM capacitor instead of the thin-oxide MOS capacitor to solve the gate leakage issue, the traditional RC-based ESD clamp circuit is still the most simple structure and useful circuit for the ESD

protection design. On the other hand, by using the circuit technique to provide the voltage bias, the gate leakage issue in thin-oxide MOS capacitor can also be solved. Moreover, accompanying with effective circuit arrangement, the gate leakage of the leaky MOS capacitor becomes one advantage for ESD clamp circuit to improve the trigger ability. All the propose designs can successfully eliminate the gate leakage issue and provide good enough ESD robustness.

# Chapter 3

# ESD Clamp Circuit against Latchup-Like Failure in High-Voltage CMOS Process

Due to the parasitic bipolar acting, the holding voltage of high-voltage devices had been discovered to be smaller than the operating voltage. With such device's characteristics, the ICs will suffer latchup-like failure, especially the high-voltage devices were implemented in the ESD protection circuits. In this Chapter, a new high-voltage ESD clamp circuit designed with lachup-free immunity is proposed and verified in a 1.8-V/3.3-V/12-V double-diffused drain MOS (DDDMOS) process. With the proposed circuit modification, the holding voltage of high-voltage ESD clamp circuit is raised to larger than the operating voltage of 12 V. Thus, the proposed design is free to the latchup-like issue in the application of touch panel control IC.

## 3.1 Background

With the combination of display panel and touch control interface, touch panel applications have been widely used in computer, communication, and consumer electronics products. Among various types of touch panel technologies, projected-capacitive type has become a main adoption for high-end products due to the superior sensitivity, durability, and multi-touch functionality. Within the different capacitance sensing methods, the most common method is mutual-capacitance sensing, because it allows unambiguous touching with higher resolution [71]. Fig. 3.1 illustrates the schematic of touch panel with mutual-capacitance sensing. The transmitter (TX) provides driving signals to TX electrode, and the driving signals also inject the relative signals into the receiver (RX) electrode through the mutual-capacitance array, then the controller system processes the signals sensed from RX interface to recognize the touched positions. Fig. 3.2 shows the mutual-capacitance sensing method, when the finger touches the panel, the local electrostatic field is changed and alters the capacitance of the mutual capacitor ($C_M$). Thus, the capacitance difference will cause the RX signal to be different from other positions those are not touched. But, the capacitance variation after finger touched is much smaller than the capacitance of the parasitic capacitor, it results in the touch sensing system to have a low signal-to-noise ratio (SNR) and to be sensitive to noise couple especially in large panel applications. To solve

those problems, a simple method is enlarging the voltage level of TX driving signal, then the amplitude ($A_{RX}$) of RX signal will also be increased to raise the signal processing margin. Therefore, the TX interface should be implemented with high-voltage CMOS processes to provide higher voltage driving signals, and this method has been widely adapted in the touch panel control ICs.

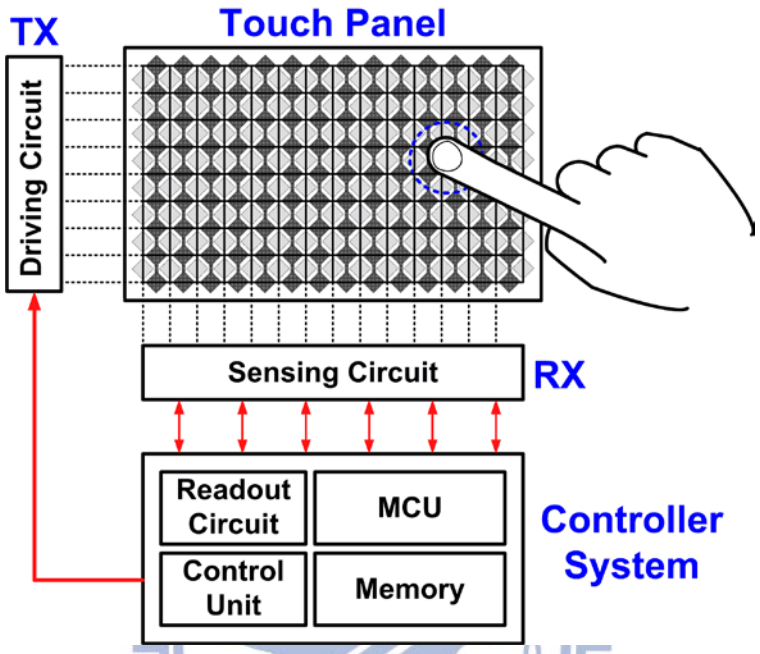



Fig. 3.1. Schematic of touch panel with mutual-capacitance sensing.

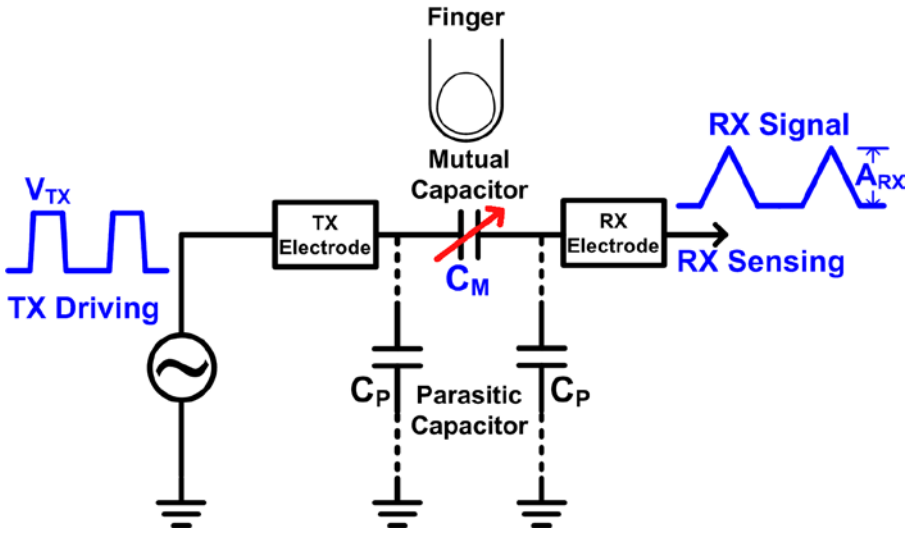



Fig. 3.2. Illustration of mutual-capacitance sensing method.

During the IC manufacture, the electrostatic discharge (ESD) induced damage has become one of the major reliability issues. As a result, the ESD protection circuits were implemented for all I/O and power ($V_{DD}$/$V_{SS}$) pins in this touch panel control IC against ESD

damage. For evaluating the robustness of ICs against ESD events, two chip-level ESD tests were used to verified the product ESD reliability, HBM test and MM test. Besides, a different type of system-level ESD test is established for the end products to confirm the robustness of electronic systems [72]. With the first version of ESD protection design, the touch panel control IC successfully achieved the chip-level ESD robustness at least 4 kV in HBM test and 400 V in MM test. However, after the system-level ESD test in a demo equipment, the touch panel control IC started to generate large leakage current and the 12-V high-voltage output provided by the charge pump circuit could not reach the correct voltage level. After the failure analysis, the failure location was found in the high-voltage ESD clamp circuit.

## 3.2 ESD Protection in the Touch Panel Control IC

In the touch panel control IC, the most part of I/O pins are RX and TX. Figs. 3.3 and 3.4 show the schematics of ESD protection design for RX and TX pins in the touch panel control IC. The ESD clamp devices for RX pin are realized by pure diodes $D_{P1}$ and $D_{N1}$, as well as the ESD clamp circuit is consist of a RC-based ESD detection circuit ($R_1$, $M_{NC1}$, $M_{P2}$ and $M_{N2}$) and a large NMOS device ($M_{NESD1}$) as the ESD protection device. In the TX pin, the ESD protection structure is similar to RX pin. But, in order to sustain in a high operating voltage of 12 V, the diodes ($D_{HP1}$ and $D_{HN1}$) are realized by high-voltage diodes and the ESD clamp circuit is composed of high-voltage MOS devices ($M_{HNC1}$, $M_{HP2}$, $M_{HN2}$, and $M_{HNESD1}$). In the touch panel control IC, the 12-V high-voltage power supply for TX interfaces is provided by an on-chip charge pump circuit. To protect the power pin against ESD stresses, the high-voltage ESD clamp circuit is also implemented at the high-voltage power output ($V_{HV}$) as shown in Fig. 3.5.

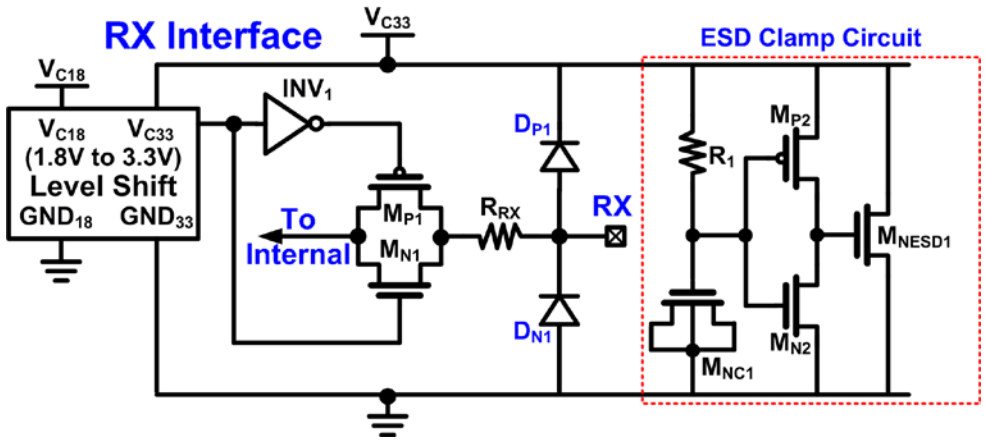



Fig. 3.3. Schematic of ESD protection design for RX pins.

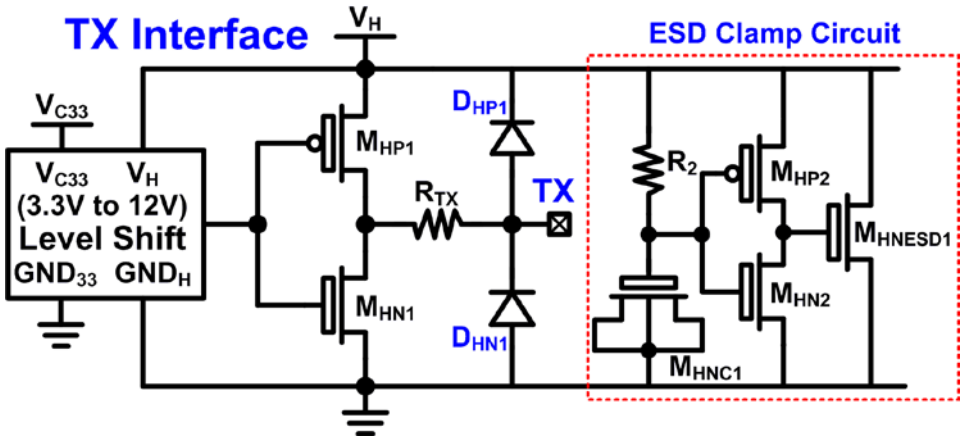



Fig. 3.4. Schematic of ESD protection design for TX pins.

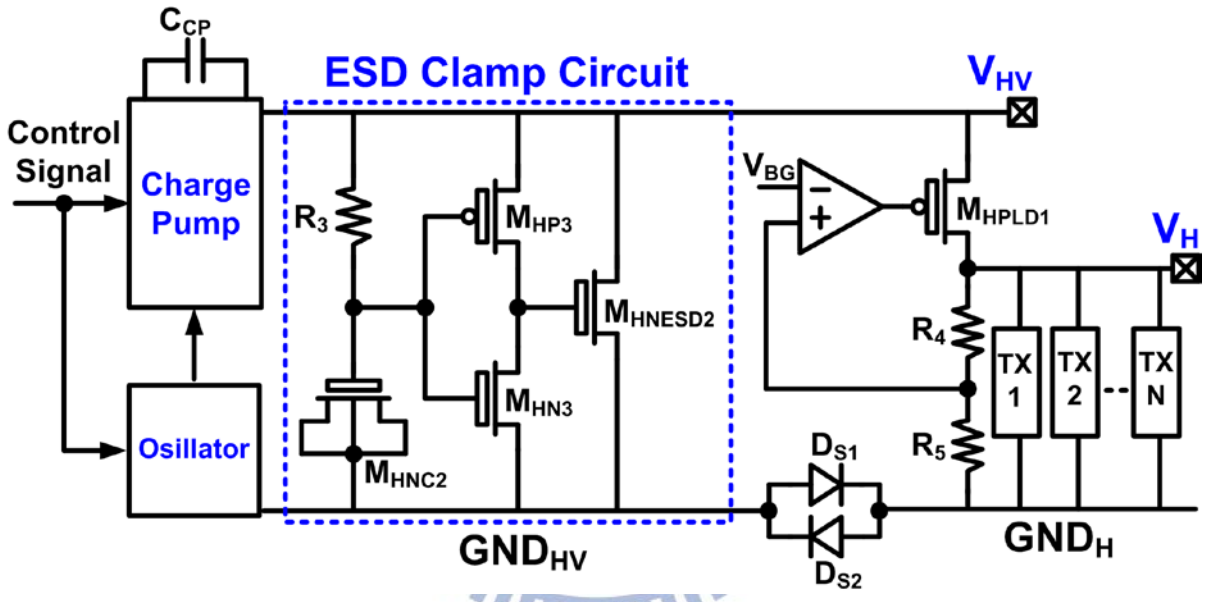



Fig. 3.5. ESD clamp circuit for high-voltage power output ($V_{HV}$).

For the commercial IC products, the typical chip-level ESD robustness are required 2 kV in HBM test and 200 V in MM test. The touch panel control IC was fabricated in a 1.8-V/3.3-V/12-V DDDMOS process. All device dimensions used in ESD protection circuits are listed in Table 3.1.

Table 3.1
Device dimensions of ESD protection circuits in RX/TX pins

| ESD Protection Design | ESD Clamp Device | | ESD Clamp Circuit | | | | |
|---|---|---|---|---|---|---|---|
| RX | $D_{P1}$ | $D_{N1}$ | $R_1$ | $M_{NC1}$ | $M_{P2}$ | $M_{N2}$ | $M_{NESD1}$ |
| | W=18.5 μm L=66 μm | W=18.5 μm L=57 μm | 100 kΩ | W=20 μm L=5 μm | W=42 μm L=0.4 μm | W=16 μm L=0.4 μm | W=864 μm L=0.44 μm |
| TX | $D_{HP1}$ | $D_{HP1}$ | $R_2$ | $M_{HNC1}$ | $M_{HP2}$ | $M_{HN2}$ | $M_{HNESD1}$ |
| | W=20 μm L=74 μm | W=18.4 μm L=57 μm | 100 kΩ | W=70 μm L=21.5 μm | W=200 μm L=1.67 μm | W=40 μm L=1.67 μm | W=840 μm L=1.67 μm |

Table 3.2
Measured HBM/MM ESD robustness of the RX/TX pins in the Touch Panel Control IC

| ESD Test Model | PS-mode | | PD-mode | | NS-mode | | ND-mode | | $V_{DD}$-to-$V_{SS}$ | |
|---|---|---|---|---|---|---|---|---|---|---|
| | RX | TX | RX | TX | RX | TX | RX | TX | Low-Voltage Power Pins | High-Voltage Power Pins |
| HBM (kV) | 5 | 4 | 5 | 4 | 5 | 4 | 5 | 4 | 8 | 6 |
| MM (V) | 500 | 400 | 500 | 400 | 500 | 400 | 500 | 400 | 800 | 500 |

Table 3.2 shows the measured chip-level ESD robustness of the touch panel control IC. From the measured results, each RX, TX, low-voltage (1.8-V/3.3-V) power, and high-voltage (12-V) power pin can achieve at least 4 kV in HBM test and 400 V in MM test. With such robust ESD levels, the IC products can have good production yield during the end product assembly. Different to the chip-level ESD test for IC products, the system-level ESD test is established for electronic systems, including the end products or demo equipments. When the touch panel control ICs assembled into the demo equipment, each function was correctly presented in the touch panel system. However, after the system-level ESD test with the air-discharge mode of ±15 kV, the touch panel system started to have some malfunctions, which occurred in the touch panel control IC. The high-voltage power pin began to generate a large leakage current in the stand-by mode and the 12-V high-voltage output which provided by the charge pump circuit could not reach the correct voltage level. Moreover, some damaged spots were clearly inspected at the pin $V_{HV}$ as shown in Fig. 3.6.

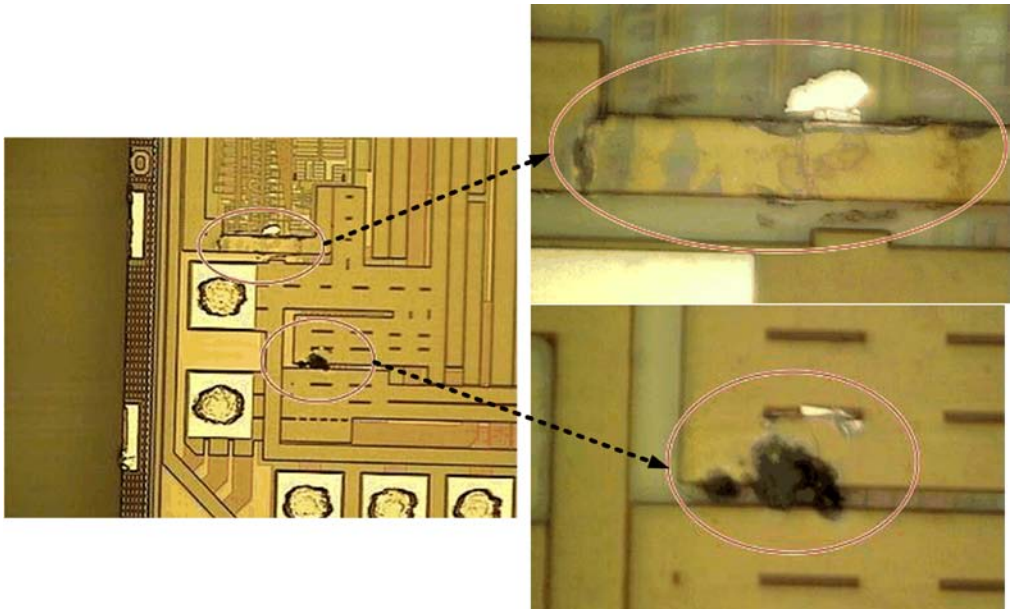


Fig. 3.6. OM photograph at $V_{HV}$ pin after system-level ESD test.

To further observe the certain failure point, the scanning electron microscope (SEM) experiment was used. The SEM photograph on the touch panel control IC after the system-level ESD test with the air-discharge mode of ±15 kV is shown in Fig. 3.7. In the SEM photograph, the failure point was found in the high-voltage ESD clamp circuit. Comparing to the layout top view of the high-voltage ESD clamp circuit (as shown in Fig. 3.8), the failure point was only located on the drain sides of the $M_{HNESD2}$ in multiple-finger layout style.

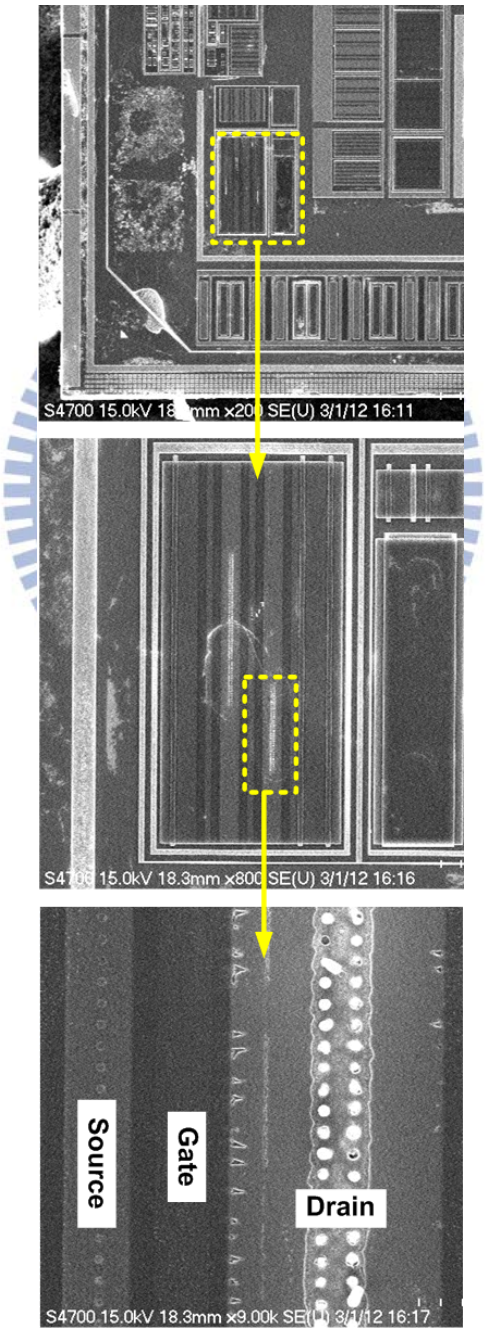



Fig. 3.7. SEM photograph of the high-voltage ESD clamp circuit after the system-level ESD test with the air-discharge mode of ±15 kV.

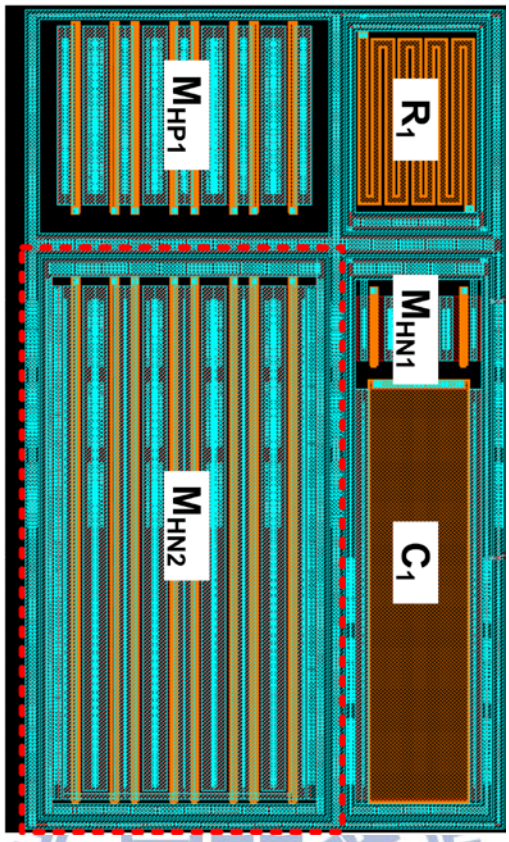



Fig. 3.8. Layout top view of the high-voltage ESD clamp circuit.

For analyzing the characteristics and turned-on behavior of ESD protection device under ESD stress, the TLP system with 100-ns pulse width and 10-ns rise time has been widely used to observe the parameters, such as trigger voltage ($V_{t1}$), holding voltage ($V_h$), and secondary breakdown current ($I_{t2}$). The TLP-measured I-V curve of the low-voltage power pin from $V_{C33}$ to $GND_{33}$ is shown in Fig. 3.9. With several power pads arranged in RX interfaces, the TLP $I_{t2}$ is as high as ~6 A. In addition, the TLP-measured I-V curve of the high-voltage power pin from $V_{HV}$ to $GND_{HV}$ is shown in Fig. 3.10. As the TLP voltage exceeded the trigger voltage $V_{t1}$ at ~15 V, the snapback is occurred when the parasitic bipolar junction transistor (BJT) was triggered on. Presently, the voltage is dropped and kept at a lower voltage level of ~8.8 V, as the holding voltage $V_h$ shown in Fig. 3.10. Although the $I_{t2}$ can achieve ~4 A, the 8.8 V of $V_h$ is lower than the operating voltage of 12 V. With a holding voltage smaller than the operating voltage, it has been reported that the system will suffer the latchup-like issue in CMOS ICs [14]-[18]. This phenomenon often leads to IC function failure or even destruction by burning out. Due to the failure point was only focused on the drain sides of $M_{HNESD2}$, the parasitic NPN BJT $Q_1$ inherent in the high-voltage NMOS $M_{HNESD2}$, as shown in Fig. 3.11, was turned on after the system-level ESD test. Consequently, a large current was continually conducted from the turned-on path and finally burning out the $M_{HNESD2}$ device.

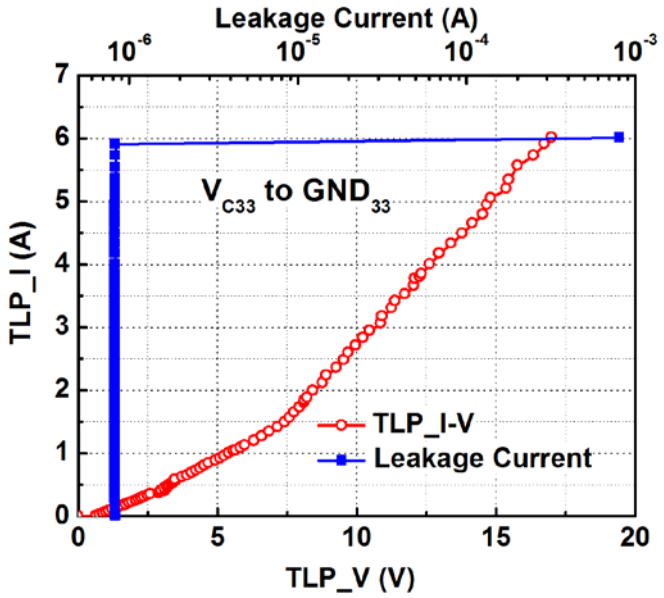



Fig. 3.9. TLP-measured I-V curve of the low-voltage power pin from $V_{C33}$ to $GND_{33}$.

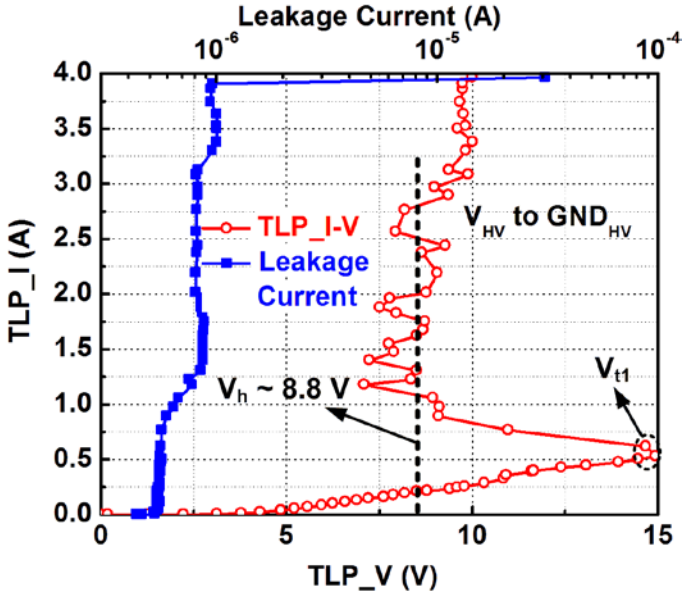



Fig. 3.10. TLP-measured I-V curve of the high-voltage power pin from $V_{HV}$ to $GND_{HV}$.

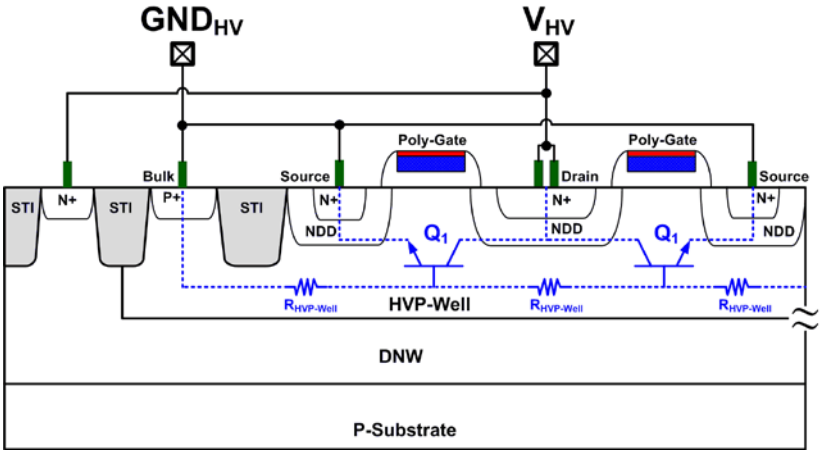



Fig. 3.11. Device cross-sectional view of the $M_{HNESD2}$.

## 3.3 High-Voltage ESD Clamp Circuit with Latchup-Free Immunity

### 3.3.1 Modification of High-Voltage ESD Clamp Circuit

Before restarting to design a new solution in the coming tape-out shuttle, a circuitry modification was attempted to remedy the latchup-like issue. Due to the latchup-like phenomenon was caused by the parasitic NPN BJT turned-on, the direct way is fixing the metal connections to isolate the NPN BJT path within the $M_{HNESD2}$. By using the focused-ion-beam (FIB) experiment to cut the source-side metal connection, the parasitic path is only formed with a reverse diode ($D_1$) from $V_{HV}$ to $GND_{HV}$, as shown in Fig. 3.12. In general CMOS processes, the reverse diode junction breakdown voltage will greater than the operating voltage but smaller than gate oxide breakdown voltage. The TLP-measured I-V curve of the modified solution in the high-voltage ESD clamp circuit after the FIB cutting is shown in Fig. 3.13. Without the parasitic NPN BJT turned-on, the snapback condition is disappeared in the I-V curve. Moreover, the clamping voltage is always larger than the operating voltage of 12 V after the $D_1$ breakdown. Thus, it did not suffer the latchup-like issue. However, using the reverse diode to realize the ESD protection could not obtain good ESD protection ability. The $I_{t2}$ is only 1.06 A in the TLP measurement. Furthermore, without an effective ESD current discharging path, the ESD robustness did not achieve the basic specifications of 2 kV in HBM test and 200 V in MM test. Therefore, a new re-design to have latchup-free immunity and good enough ESD protection capability is strongly needed.

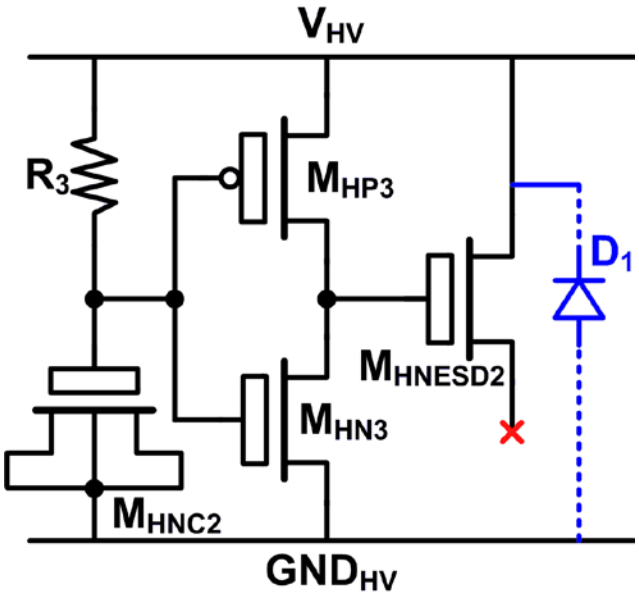



Fig. 3.12. Modified solution in high-voltage ESD clamp circuit.

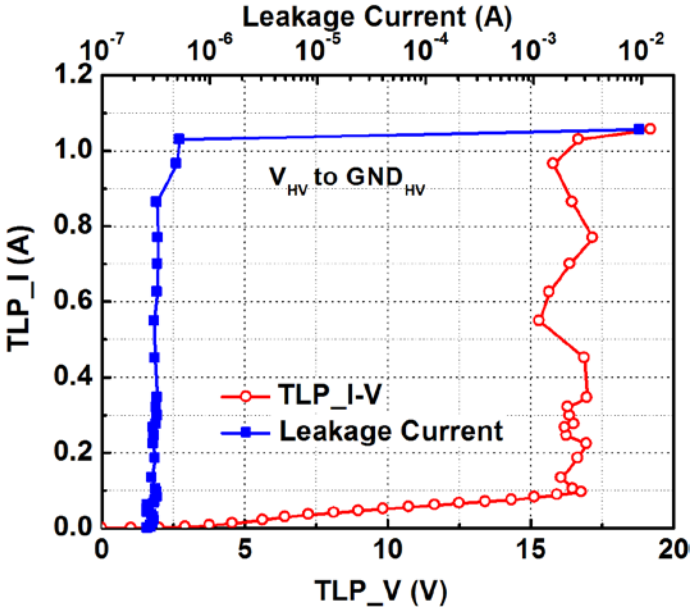


Fig. 3.13. TLP measured I-V curve of the modified high-voltage ESD clamp circuit.

### 3.3.2 Proposed Design of High-Voltage ESD Clamp Circuit with Latchup-Free Immunity

In a single ESD protection device, the holding voltage of the turned-on parasitic NPN BJT in NMOS device could be estimated by

$$V_{H1} = V_{P1} + V_{CEQ1}. \tag{3.1}$$

The $V_{P1}$ is the voltage generated by the turned-on current ($I_{ON}$) through the parasitic resistance within the junction and metal connections. The $V_{CEQ1}$ is the voltage potential inherent in the turned-on BJT from collector to emitter, as shown in Fig. 3.14(a). To increase the holding voltage of the circuit, the ESD protection device could be modified to have a stack structure. As a result, two parasitic NPN BJTs will be stacked to increase the total holding voltage, as shown in Fig. 3.14(b). Ideally, the holding voltage of stacked structure will be twice than single structure. The holding voltage of the stacked structure could be given by

$$V_{H2} = V_{P1} + V_{CEQ1} + V_{P2} + V_{CEQ2}. \tag{3.2}$$

However, with both high-voltage NMOS devices stacked will decrease the ESD protection ability due to the higher clamping voltage to cause higher overshooting voltage during ESD events. Moreover, a much higher holding voltage will also decrease the ESD robustness because the higher heat will be generated during ESD current discharging. To overcome aforementioned disadvantages, a new design with high-voltage and low-voltage ESD protection NMOS devices stacked is proposed. Fig. 3.15 shows the circuit schematic of

the new proposed high-voltage ESD clamp circuit. The proposed design is composed with a RC-based ESD detection circuit ($R_6$, $M_{HNC3}$, $M_{HP4}$, and $M_{HN4}$) and the stacked ESD protection NMOS devices ($M_{HNESD3}$ and $M_{NESD2}$). Different from the 12-V NMOS device ($M_{HNESD3}$), the $M_{NESD2}$ is a 3.3-V NMOS device. To avoid $M_{NESD2}$ easily be damaged through the turned-on $M_{HP4}$ during ESD zapping, the $R_7$ is connected to the gate terminal of the $M_{NESD2}$. The circuit cross-sectional view of the stacked NMOS devices is shown in Fig. 3.16. Two parasitic NPN BJTs $Q_1$ and $Q_2$ are inherent in the $M_{HNESD3}$ and $M_{NESD2}$, respectively. Thus, the holding voltage can be adjusted by two different devices to a suitable range.

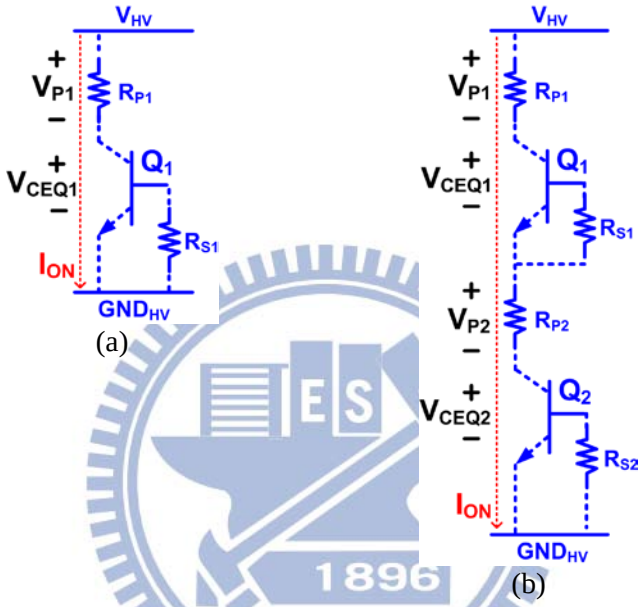



Fig. 3.14. Estimation of holding voltage with (a) single NMOS device and (b) stacked NMOS devices.

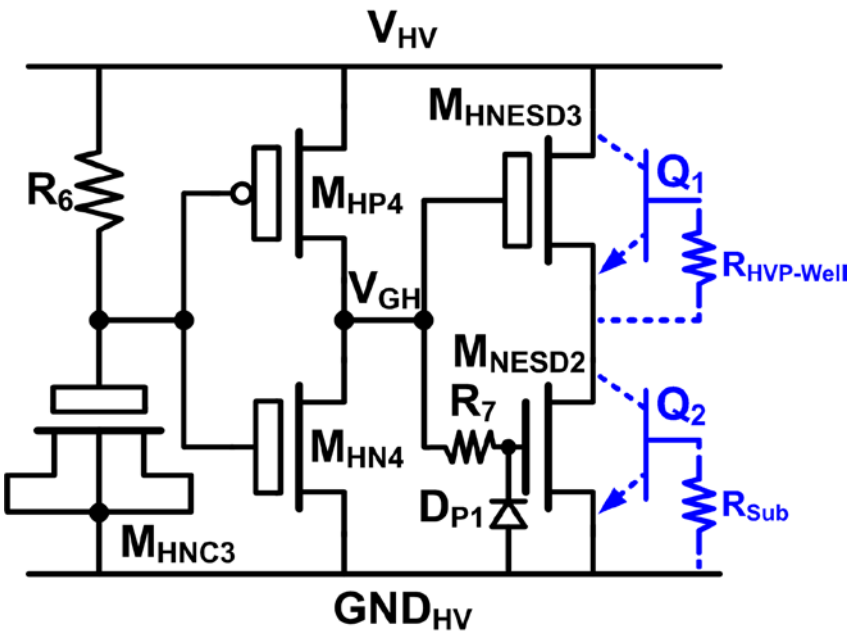



Fig. 3.15. New proposed high-voltage ESD clamp circuit against latchup-like issue.

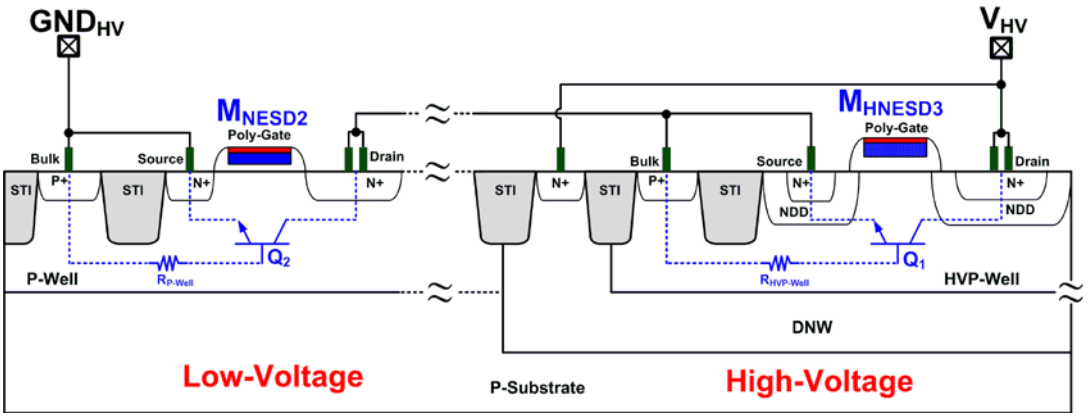



Fig. 3.16. The cross-sectional view of the stacked NMOS devices with a high-voltage (12-V) NMOS $M_{HNESD3}$ and a low-voltage (3.3-V) NMOS $M_{NESD2}$.

## 3.4 Experimental Results

The new proposed high-voltage ESD clamp circuit had been implemented in the touch panel control IC, where the IC product was fabricated in a 1.8-V/3.3-V/12-V DDDMOS process. Fig. 3.17 shows the whole chip micrograph. The layout top view of the new proposed high-voltage ESD clamp circuit is also shown in Fig. 3.17 and the occupied silicon area is 90 μm × 205 μm. All device dimensions used in the new proposed design are listed in Table 3.3. With the new proposed design, the IC product can still achieve the chip-level ESD robustness at least 4 kV in HBM test and 400 V in MM test. Moreover, the touch panel system module can pass the system-level ESD test with the air-discharge mode of ±15-kV without the latchup-like failure.

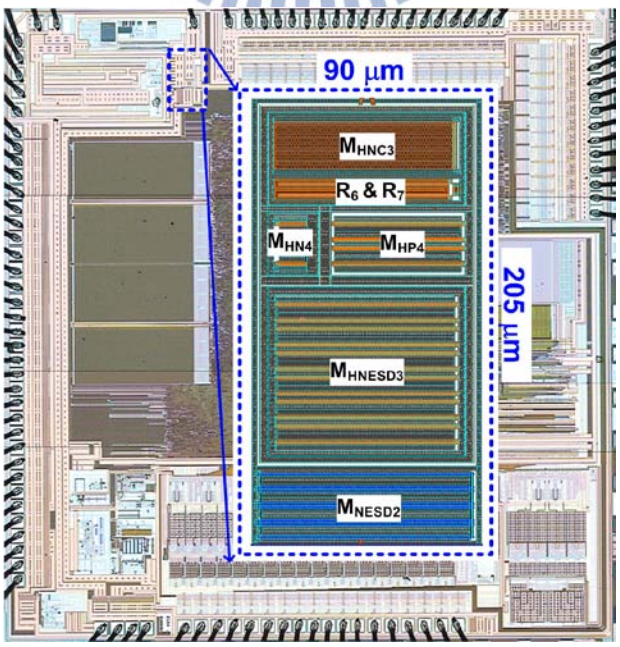



Fig. 3.17. Chip micrograph of the touch panel control IC with new proposed high-voltage ESD clamp circuit.

Table 3.3
Device dimensions of the new proposed high-voltage ESD clamp circuit

| Device | Dimension |
|---|---|
| $R_6$ | 100 kΩ |
| $R_7$ | 200 Ω |
| $M_{HP4}$ | W=200 μm / L=1.67 μm |
| $M_{HN4}$ | W=40 μm / L=1.67 μm |
| $M_{HNC3}$ | W=70 μm / L=21.5 μm |
| $M_{HNESD3}$ | W=840 μm / L=1.67 μm |
| $M_{NESD2}$ | W=500 μm / L=0.5 μm |

To investigate the holding voltage of the new proposed design, the TLP measured I-V curve is shown in Fig. 3.18. In the beginning, the TLP current is raised by the MOSFET channel turned on. When the TLP voltage increased to ~18.6 V, the parasitic NPN BJTs are triggered on to cause snapback. After the snapback occurred, the voltage is clamped to ~13.8 V and the $I_{t2}$ is achieved up to 4.1 A. Therefore, the holding voltage is actually raised by two stacked NMOS devices. Because the holding voltage of 13.8 V is larger than operating voltage of 12 V, the touch panel control IC is free to the latchup-like failure in the touch panel applications.

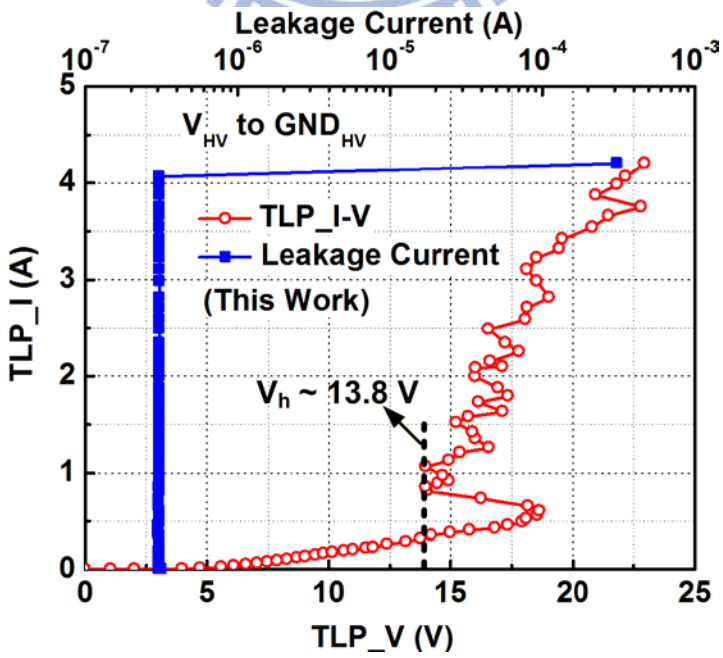



Fig. 3.18. Measured TLP I-V curve of the new proposed high-voltage ESD clamp circuit with latchup-free immunity.

## 3.5 Summary

A new high-voltage ESD clamp circuit is proposed and verified with a 1.8-V/3.3-V/12-V DDDMOS process. By stacked high-voltage and low-voltage ESD protection NMOS devices, the holding voltage is increased from 8.8 V to 13.8 V without extra process modification. Therefore, the touch panel control IC in demo equipment can pass the system-level ESD test with the air-discharge mode of ±15-kV. In addition to the purpose of free to latchup-like issue, the proposed design also maintain a good chip-level ESD robustness of 4 kV in HBM test and 400 V in MM test.

# Chapter 4

## Design of $2xV_{DD}$-Tolerant Logic Gates with Only $1xV_{DD}$ Devices

The novel $2xV_{DD}$- tolerant NOT, NAND, and NOR logic gates had been proposed and verified in a 90-nm CMOS process with only $1xV_{DD}$ devices. With the dynamic source bias technique, the logic gates can be created to have $2xV_{DD}$ tolerant capability. Thus, the new $2xV_{DD}$-tolerant logic gates can operate under $2xV_{DD}$ voltage environment without suffering the gate oxide reliability issue.

### 4.1 Background

In CMOS technologies, a single type of MOS devices can only be operated within a regular $V_{DD}$ voltage region to meet reliability specification. When the operating voltage exceeds $V_{DD}$, the device will suffer the gate oxide overstress issues [19]-[21]. However, with good arrangement of operation control and device combination, the circuits can be operated in the higher supply voltage. For communicating to other chips with different power domain, some I/O interface circuits had been successfully developed with high-voltage tolerant capability by using only $1xV_{DD}$ (thin-oxide) devices [25]-[32]. Moreover, some logic circuits were also developed to have high-voltage tolerant ability for some special purposes. For example, Fig. 4.1 shows the Schmitt trigger circuit in a 3.3-V application with only 1/2.5-V devices [73], and Fig. 4.2 shows a transmission gate for a flash memory application [74].

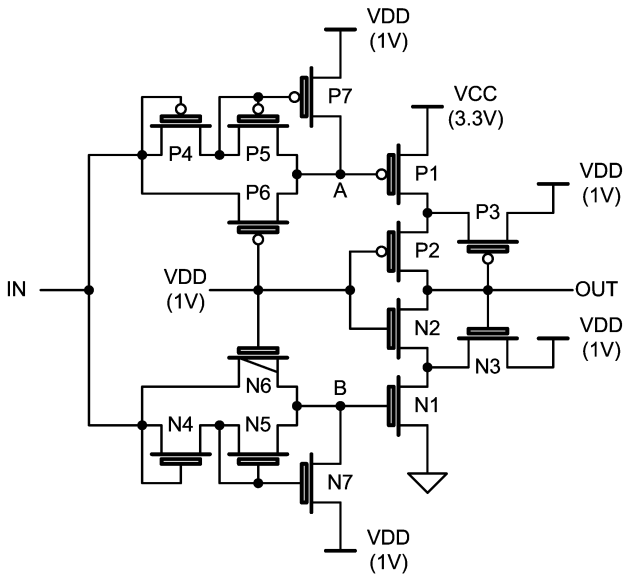



Fig. 4.1. Schmitt trigger circuit in a 3.3-V application with only 1/2.5-V devices.

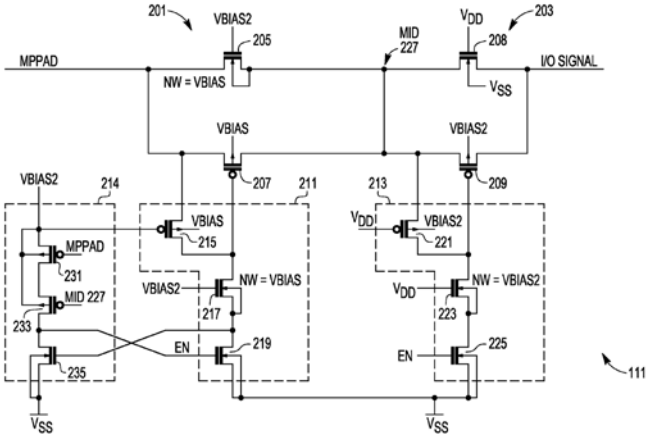
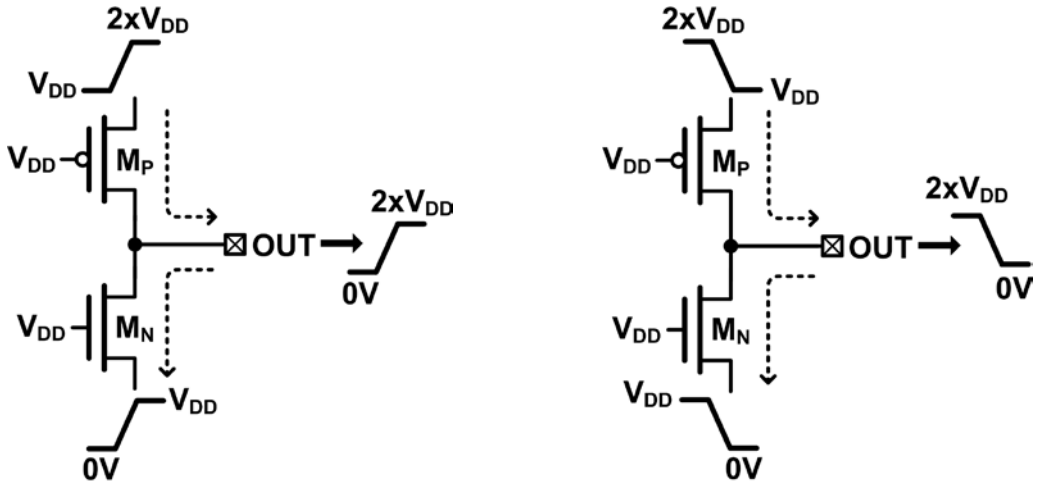



Fig. 4.2. High-voltage tolerant transmission gate for a flash memory application.

In the digital circuit applications, the basic circuit units are the complementary logic gates. If effective device combinations and correct operation steps could be implemented in the circuit, the logic gates with only $1xV_{DD}$ devices could be designed to operate under the $2xV_{DD}$ voltage signal. Figs. 4.3(a) and 4.3(b) show the design concepts of the dynamic source bias technique when the circuit output (OUT) driving to logic high and logic low. With the $M_P$ and $M_N$ gate voltage biased at $V_{DD}$, the $M_P$ and $M_N$ can be turned on or turned off by changing device's source voltage. For transmitting a logic high signal (0V-$2xV_{DD}$), by applying a 0V-$V_{DD}$ signal at $M_N$'s source and a $V_{DD}$-$2xV_{DD}$ signal at $M_P$'s source, the OUT can successfully transmit a digital signal of 0V-$2xV_{DD}$. On the other hand, for transmitting a logic low signal ($2xV_{DD}$-0V), the $V_{DD}$-0V and $2xV_{DD}$-$V_{DD}$ signals are needed for source terminals of $M_N$ and $M_P$, respectively. Therefore, with such source voltage bias arrangements, the logic gates implemented by only $1xV_{DD}$ devices can be successfully operated under $2xV_{DD}$ voltage signal without suffering the aforementioned reliability issues.




(a) (b)

Fig. 4.3. Dynamic source bias technique when driving the signal to (a) logic high and (b) logic low.

## 4.2 2x$V_{DD}$-Tolerant Logic Gates

By implementing the dynamic source bias technique into the circuit, complementary logic gates can be modified to have 2x$V_{DD}$ tolerant capability. Fig. 4.4 shows the 2x$V_{DD}$-tolerant NOT gate. $M_P$ and $M_N$ with gate voltages of $V_{DD}$ are used to conduct logic level to output and avoid gate oxide overstress issue during operation. $M_{PP}$ and $M_{NN}$ are used to decide the function of logic gate. $M_{NSB1}$ ($M_{PSB1}$) is used to bias the source voltage of $M_P$ ($M_N$) at $V_{DD}$ when $M_{PP}$ ($M_{NN}$) is turned off during operation. Since the device operation voltage is not allowed to exceed 1x$V_{DD}$ range, the 0V-2x$V_{DD}$ input signal needs to be separated to a 0V-$V_{DD}$ and a $V_{DD}$-2x$V_{DD}$ control signal for pull-low path and pull-high path, respectively. Fig. 4.5 illustrates the proposed level converter I, which can convert the 0V-2x$V_{DD}$ voltage signal to two required voltage range. When the input signal IN is transmitting from 0V to $V_{DD}$-Vth, where $V_{th}$ is MOS device's threshold voltage, $M_{N1}$ and $M_{P2}$ are turned on. Therefore, $IN_L$ is conducting the voltage signal from 0V to $V_{DD}$-Vth and $IN_H$ is biased at $V_{DD}$. When IN signal keeps transmitting from $V_{DD}$+$V_{th}$ to 2x$V_{DD}$, $M_{N2}$ and $M_{P1}$ are turned on. Thus, $IN_H$ is conducting the voltage from $V_{DD}$ to 2x$V_{DD}$ and $IN_L$ is biased at $V_{DD}$. By the proposed level converter I, the 0V-2x$V_{DD}$ voltage signal can successfully be separated to a 0V-$V_{DD}$ voltage signal $IN_L$ and a $V_{DD}$-2x$V_{DD}$ voltage signal $IN_H$. Then, the $IN_L$ signal is connected to the $M_{NN}$ and $M_{PSB1}$ at pull-low path, while the $IN_H$ signal is connected to the $M_{PP}$ and $M_{NSB1}$ at pull-high path (as shown in Fig. 4.4).

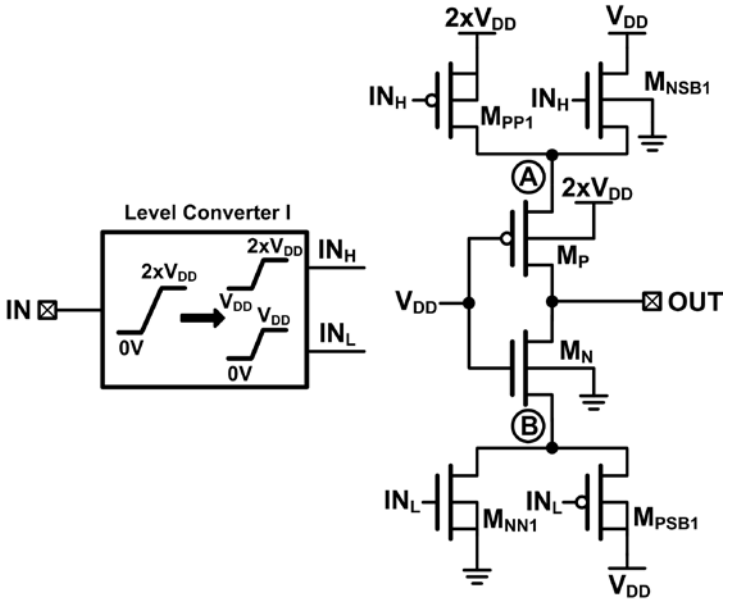



Fig. 4.4. Circuit schematic of NOT gate with 2x$V_{DD}$ tolerant capability.

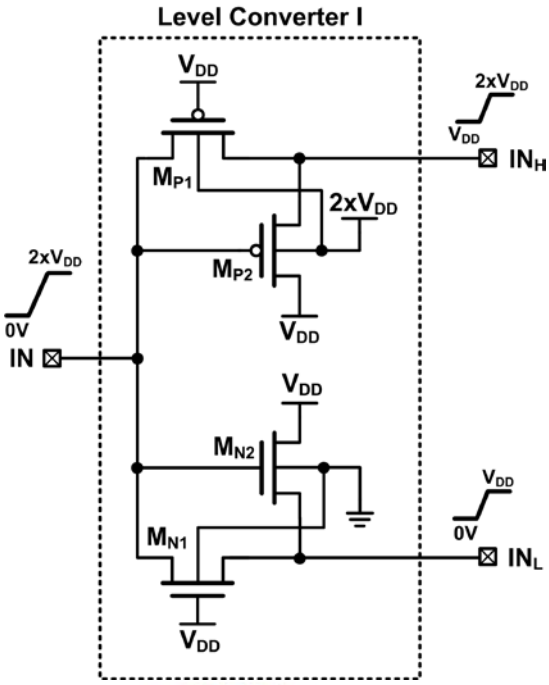



Fig. 4.5. Circuit implementation of level converter I.

With this configuration, the voltage across each MOS device does not exceed $1xV_{DD}$ voltage range. Moreover, the output voltage signal can be driven to the required $2xV_{DD}$ magnitude. For example, when the 2xvdd-tolerant not gate input signal IN is 0V, the $IN_L$ signal is also 0V to turn off the $M_{NN}$ and turn on $M_{PSB1}$. At the same time, the $IN_H$ signal is driven to $V_{DD}$ to turn on $M_{PP}$ because the source voltage is $2xV_{DD}$. Therefore, the output voltage of the $2xV_{DD}$-tolerant NOT gate is driven to $2xV_{DD}$ and the voltage at node B is biased to $V_{DD}$. On the other hand, when input signal IN is $2xV_{DD}$, the $IN_L$ signal is $V_{DD}$ to turn on the $M_{NN}$ and turn off $M_{PSB1}$. At the same time, the $IN_H$ signal is driven to $2xV_{DD}$ to turn off $M_{PP}$ and turn on $M_{NSB1}$. Therefore, the output voltage of the $2xV_{DD}$-tolerant NOT gate is driven to 0V and the voltage of node A is biased to $V_{DD}$. Whether the output voltage is pulled high to $2xV_{DD}$ or pulled low to 0V, each two terminals of all MOS devices do not exceed a $1xV_{DD}$. Thus, gate oxide overstress issue can be completely avoided in the proposed $2xV_{DD}$-tolerant NOT gate.

With the same design concepts, the NAND and NOR logic gates can also be modified to have $2xV_{DD}$ tolerant capability. Figs. 4.6 and 4.7 show the $2xV_{DD}$-tolerant NAND and NOR gate, respectively. $M_P$ and $M_N$ with gate voltage of $V_{DD}$ are also used to conduct logic level to the output and avoid gate oxide overstress issue. $M_{PP1}$, $M_{PP2}$, $M_{NN1}$, and $M_{NN2}$ are used to define the function of logic gate. $M_{NSB1}$ and $M_{NSB2}$ ($M_{PSB1}$ and $M_{PSB2}$) are used to bias the source voltage of $M_P$ ($M_N$) at $V_{DD}$ when the pull-low or pull-high path is turned off during operation.

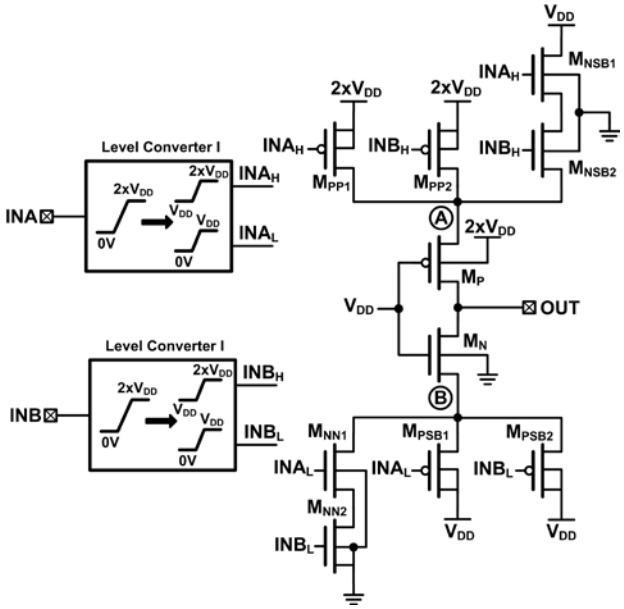



Fig. 4.6. Circuit schematic of NAND gate with $2xV_{DD}$ tolerant capability.

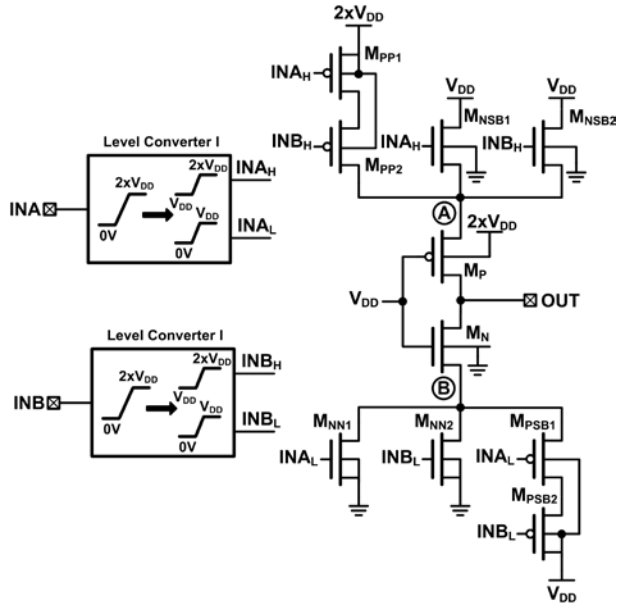
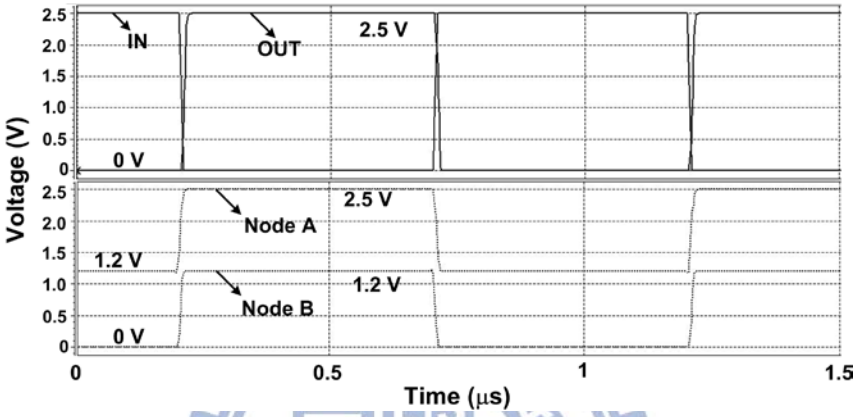


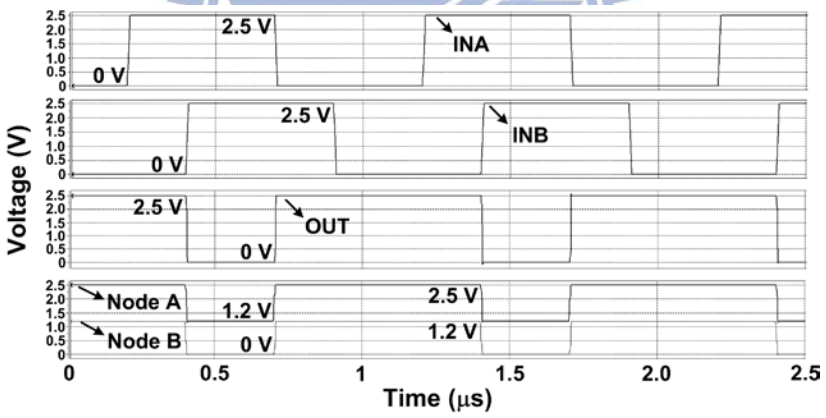

Fig. 4.7. Circuit schematic of NOR gate with $2xV_{DD}$ tolerant capability.

In order to achieve the correct logic operation, the function defining devices and source biasing devices need to have complementary structure when the logic gates have more than one input. For example, with the series connection of NMOS $M_{NN1}$ and $M_{NN2}$ in the $2xV_{DD}$-tolerant NAND gate's pull-low path, the source bias PMOS $M_{PSB1}$ and $M_{PSB2}$ should be in parallel connected at the source terminal of $M_N$, as shown in Fig. 4.6. Even though the pull-low path is turned off when input $IN_A$ and $IN_B$ are with opposite logic signals, node B still can be biased to the safe voltage of $V_{DD}$ by $M_{PSB1}$ or $M_{PSB2}$. Based on this design methodology, all complementary logic gates with different input numbers could be modified to have $2xV_{DD}$ tolerant capability.

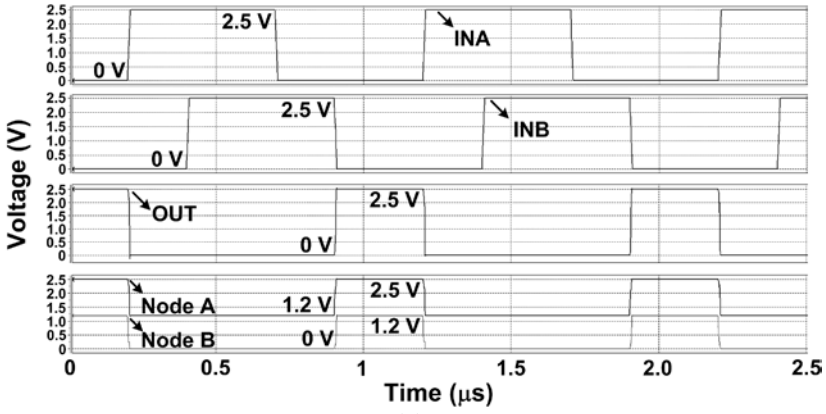
Figs. 4.8(a), 4.8(b), and 4.8(c) show the simulated voltage waveforms of $2xV_{DD}$-tolerant NOT, NAND, and NOR gates, respectively. Besides, the corresponding circuit logics and devices' behavior of each $2xV_{DD}$-tolerant logic gate are summarized in Tables 4.1, 4.2, and 4.3. Implementing in a 90-nm CMOS process, the normal operation voltage ($1xV_{DD}$) for core devices is 1.2 V, while the I/O devices' operation voltage of 2.5V is as $2xV_{DD}$. In the simulated results, each $2xV_{DD}$-tolerant logic gate performs the correct logic operation. From monitoring the terminal voltage, each MOS device is operated within $1xV_{DD}$ voltage range. Thus, gate oxide overstress issue is not encountered in the proposed logic gates.




(a)




(b)




(c)

Fig. 4.8. Simulated voltage waveforms of $2xV_{DD}$-tolerant (a) NOT gate, (b) NAND gate, and (c) NOR gate, with signal voltage level of 2.5 V ($2xV_{DD}$).

Table 4.1
Corresponding circuit logics and devices' behavior in proposed $2xV_{DD}$-tolerant NOT gate

| $2xV_{DD}$ NOT Gate | Pull-High | Pull-Low |
|---|---|---|
| IN | 0 | $2xV_{DD}$ |
| $IN_L$ | 0 | $V_{DD}$ |
| $IN_H$ | $V_{DD}$ | $2xV_{DD}$ |
| Node A | $2xV_{DD}$ | $V_{DD}$ |
| Node B | $V_{DD}$ | 0 |
| OUT | $2xV_{DD}$ | 0 |
| $M_{PP}$ | ON | OFF |
| $M_{PSB1}$ | ON | OFF |
| $M_P$ | ON | OFF |
| $M_{NN}$ | OFF | ON |
| $M_{NSB1}$ | OFF | ON |
| $M_N$ | OFF | ON |

Table 4.2
Corresponding circuit logics and devices' behavior in proposed $2xV_{DD}$-tolerant NAND gate

| $2xV_{DD}$ NAND Gate | Pull-High | Pull-High | Pull-High | Pull-Low |
|---|---|---|---|---|
| (INA, INB) | (0, 0) | (0, $2xV_{DD}$) | ($2xV_{DD}$, 0) | ($2xV_{DD}$, $2xV_{DD}$) |
| ($INA_L$, $INB_L$) | (0, 0) | (0, $V_{DD}$) | ($V_{DD}$, 0) | ($V_{DD}$, $V_{DD}$) |
| ($INA_H$, $INB_H$) | ($V_{DD}$, $V_{DD}$) | ($V_{DD}$, $2xV_{DD}$) | ($2xV_{DD}$, $V_{DD}$) | ($2xV_{DD}$, $2xV_{DD}$) |
| Node A | $2xV_{DD}$ | $2xV_{DD}$ | $2xV_{DD}$ | $V_{DD}$ |
| Node B | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | 0 |
| OUT | $2xV_{DD}$ | $2xV_{DD}$ | $2xV_{DD}$ | 0 |
| $M_{PP1}$ | ON | ON | OFF | OFF |
| $M_{PP2}$ | ON | OFF | ON | OFF |
| $M_{PSB1}$ | ON | ON | OFF | OFF |
| $M_{PSB2}$ | ON | OFF | ON | OFF |
| $M_P$ | ON | ON | ON | OFF |
| $M_{NN1}$ | OFF | OFF | OFF | ON |
| $M_{NN2}$ | OFF | ON | OFF | ON |
| $M_{NSB1}$ | OFF | OFF | ON | ON |
| $M_{NSB2}$ | OFF | OFF | OFF | ON |
| $M_N$ | OFF | OFF | OFF | ON |

Table 4.3
Corresponding circuit logics and devices' behavior in proposed $2xV_{DD}$-tolerant NOR gate

| $2xV_{DD}$ NOR Gate | Pull-High | Pull-Low | Pull-Low | Pull-Low |
|---|---|---|---|---|
| (INA, INB) | (0, 0) | (0, $2xV_{DD}$) | ($2xV_{DD}$, 0) | ($2xV_{DD}$, $2xV_{DD}$) |
| ($INA_L$, $INB_L$) | (0, 0) | (0, $V_{DD}$) | ($V_{DD}$, 0) | ($V_{DD}$, $V_{DD}$) |
| ($INA_H$, $INB_H$) | ($V_{DD}$, $V_{DD}$) | ($V_{DD}$, $2xV_{DD}$) | ($2xV_{DD}$, $V_{DD}$) | ($2xV_{DD}$, $2xV_{DD}$) |
| Node A | $2xV_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ |
| Node B | $V_{DD}$ | 0 | 0 | 0 |
| OUT | $2xV_{DD}$ | 0 | 0 | 0 |
| $M_{PP1}$ | ON | ON | OFF | OFF |
| $M_{PP2}$ | ON | OFF | OFF | OFF |
| $M_{PSB1}$ | ON | OFF | OFF | OFF |
| $M_{PSB2}$ | ON | OFF | ON | OFF |
| $M_P$ | ON | OFF | OFF | OFF |
| $M_{NN1}$ | OFF | OFF | ON | ON |
| $M_{NN2}$ | OFF | ON | OFF | ON |
| $M_{NSB1}$ | OFF | OFF | ON | ON |
| $M_{NSB2}$ | OFF | ON | OFF | ON |
| $M_N$ | OFF | ON | ON | ON |

## 4.3 Experimental Results

The new proposed $2xV_{DD}$-tolerant logic gates had been fabricated in a 90-nm CMOS process with only 1.2-V devices. The micrograph of test chip is shown in Fig. 4.9. The measured voltage waveforms of $2xV_{DD}$-tolerant NOT, NAND, and NOR gates are shown in Figs. 4.10(a), 4.10(b) and 4.10(c), respectively. The input data rate verified in those figures is 1 MHz. The measured results have demonstrated that the proposed $2xV_{DD}$-tolerant logic gates can be safely operated with the voltage signals of 2.5 V (as $2xV_{DD}$) to provide the correct logic functions.

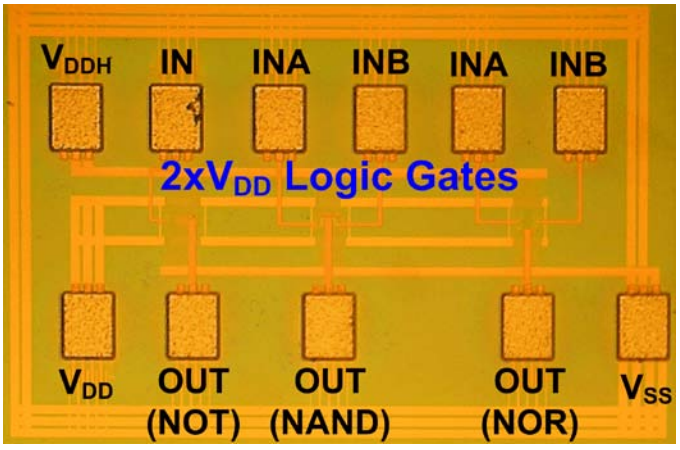
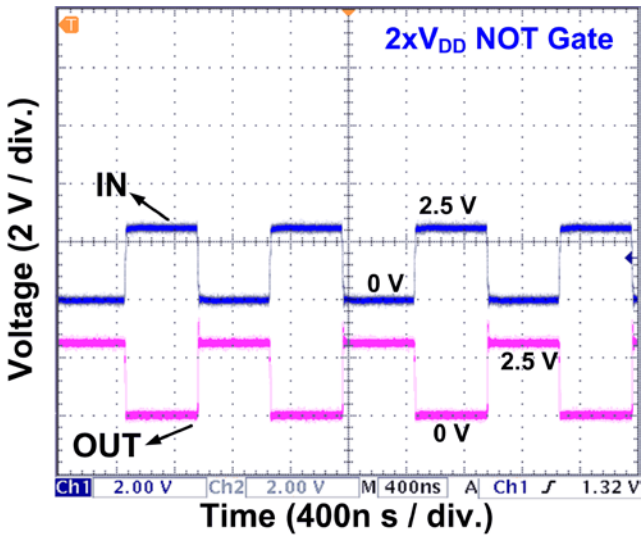
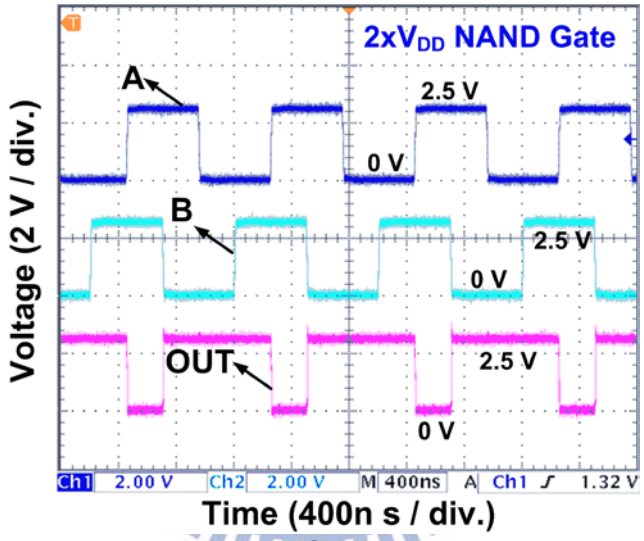


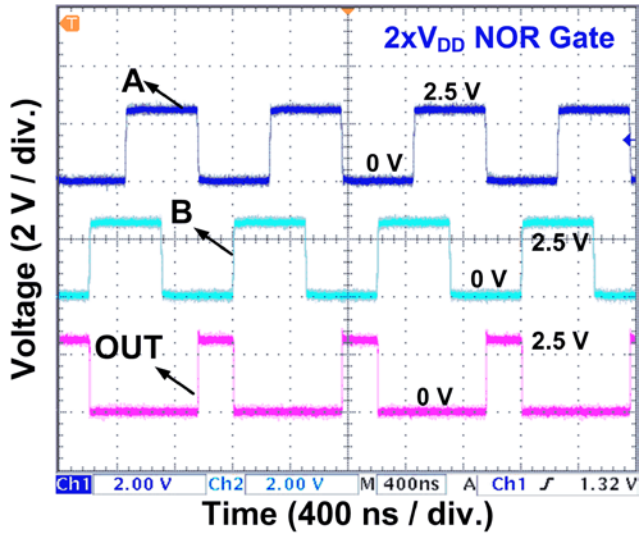

Fig. 4.9. Chip micrograph of the $2xV_{DD}$-tolerant logic gates fabricated in a 90-nm CMOS process with only 1.2-V devices.




(a)




(b)




(c)

Fig. 4.10. Measured voltage waveforms of $2xV_{DD}$ -tolerant (a) NOT gate, (b) NAND gate, and (c) NOR gate.

## 4.4 Summary

Novel $2xV_{DD}$-tolerant logic gates have been proposed and verified in a 90-nm CMOS process with only 1.2-V ($1xV_{DD}$) devices. By using the dynamic source bias technique, the CMOS logic gates are realized to have $2xV_{DD}$ tolerant capability without suffering gate oxide reliability issue. Measured results have demonstrated that the proposed $2xV_{DD}$-tolerant logic gates can be safely operated with the voltage signals of 2.5 V to provide the correct logic functions. The proposed $2xV_{DD}$-tolerant logic gates can be used in the applications of microelectronic systems facing the mixed-voltage environments.

# Chapter 5

# Design of $2\times V_{DD}$-Tolerant Output Buffer with PVT Compensation Realized by Only $1\times V_{DD}$ Thin-Oxide Devices

A new $2\times V_{DD}$-tolerant output buffer with process, voltage, and temperature (PVT) compensation is proposed and verified in a 90-nm CMOS process. Consisting of the dynamic source bias and gate-controlled technique, the proposed $2xV_{DD}$ output buffer realized by only $1xV_{DD}$ devices can successfully transmit and receive $2\times V_{DD}$ voltage signal. Utilizing the $2xV_{DD}$-tolerant logic gates, the PVT variation detector has been implemented to detect PVT variations from $2\times V_{DD}$ voltage environment and to provide the compensation control for the $2\times V_{DD}$-tolerant output buffer without suffering the gate oxide overstress issue.

## 5.1 Background

In order to achieve lower power consumption, higher operating speed, and higher integration capability, CMOS devices have been continually scaled down with thinner gate oxide and smaller channel length. As a result, the core circuit devices will be operated in a low voltage level (below 1.2V) in the advanced CMOS technologies. However, some peripheral components or sub-systems in the SoC application would be still operated in higher voltage levels (above 1.8V). With the different power supply voltages in the system, the conventional I/O buffer circuits are no longer suitable due to reliability concerns. Several reliability issues had been reported, such as gate oxide overstress [19]-[21], hot-carrier degradation [22], [23], and the undesired leakage current paths [24]. Therefore, the mixed-voltage I/O buffers are necessary to put into the interface to communicate with other sub-system which has different power domain. In the mixed-voltage I/O buffer, some devices could be directly replaced by the thick-oxide devices to solve the aforementioned reliability issues. However, using both the thick-oxide and thin-oxide devices within a chip increases the fabrication cost. To reduce the fabrication cost, several mixed-voltage I/O buffers realized by only low-voltage (thin-oxide) devices have been reported [25]–[32].

With the scaled-down CMOS devices, the circuit performance becomes more sensitive to PVT variations. In addition to the PVT variations, a recent study had been reported that the die-package stress also influences device or circuit performance [33]. Thus, the circuit

performance becomes more difficult to meet the required specifications in advanced CMOS processes. To improve the yield, the PVT variations have been taken into consideration in lots of circuit design scenarios, especially in signal processing, data transmitting, and clock generating [34]-[39]. Consequently, for providing the driving signal of an output buffer, the slew rate of the driving signal is easily varied by PVT variations. Thus, several studies of output buffer with PVT compensation had been proposed to keep the output slew rate within an acceptable range [40]-[45]. However, those methods are not feasible in the mixed-voltage I/O interfaces, because the devices in the compensation circuit would suffer the gate oxide overstress issue under the operating voltage higher than $1xV_{DD}$. Although some timing delay problems caused by PVT variation can be solved by increasing the output buffer's size, too large output buffers have another issue called simultaneous switching noise (SSN) [75], [76]. This problem arises when the output buffers with too large device dimensions are fabricated in the fast-fast (FF) corner and operated at normal operating conditions.

To maintain a stable driving slew rate in the mixed-voltage output buffer, the compensation mechanism should be added in the circuit. For detecting the PVT variations under the mixed-voltage operating conditions, the PVT compensation circuits should also be designed to have mixed-voltage tolerant capability. In this work, a new $2xV_{DD}$-tolerant output buffer with PVT compensation realized by only $1xV_{DD}$ devices is proposed.

## 5.2 Dynamic Source Bias and Gate-Controlled Techniques

The dynamic source bias technique had been presented in chapter 4. By using the same circuit implementation method, the output buffer with only $1xV_{DD}$ devices could be realized to have $2xV_{DD}$-tolerant ability in transmitting mode. In addition to the source bias, the gate voltage bias at output buffer devices should also be considered when receiving a $2xV_{DD}$ voltage signal in the receiving mode. Figs. 5.1 and 5.2 show the design concepts of the dynamic source bias and gate-controlled techniques to achieve a $2xV_{DD}$-tolerant output buffer with transmitting and receiving modes. Comparing Fig. 5.1(a) and Fig. 5.1(b) in the transmitting mode, with the gate voltage of $V_{DD}$ at $M_P$ and $M_N$, $M_P$ and $M_N$ can be turned on or turned off by changing their source voltages to transmit the $0V$-$2xV_{DD}$ or $2xV_{DD}$-$0V$ signals.

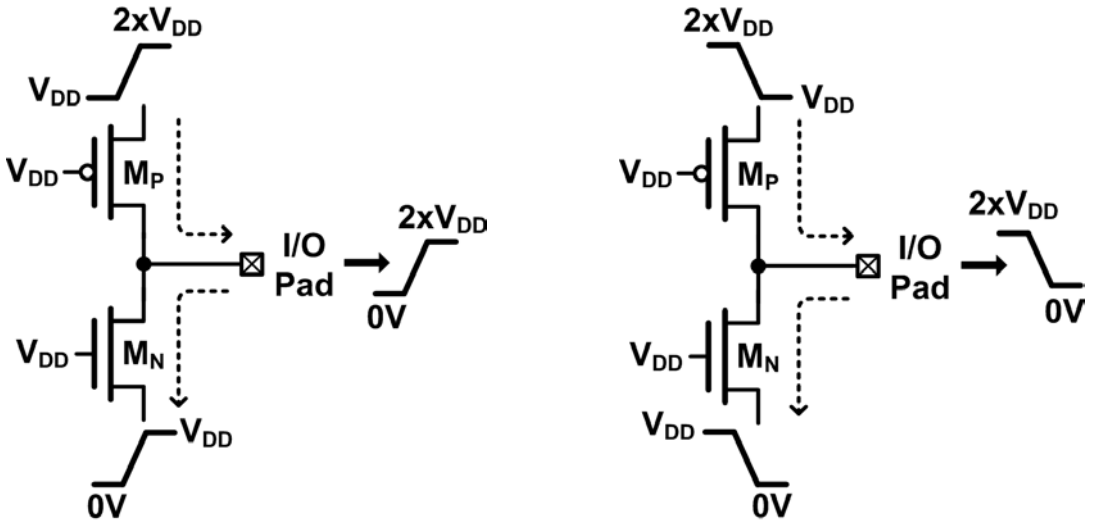



Fig. 5.1. Dynamic source bias technique in the transmitting mode when I/O pad transmits (a) the logic high and (b) the logic low signals.

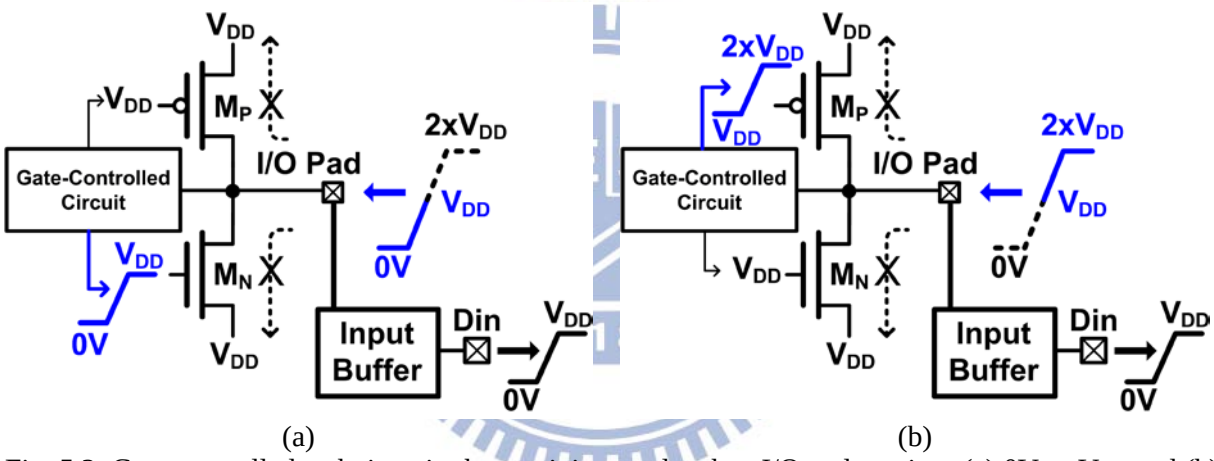



Fig. 5.2. Gate-controlled technique in the receiving mode when I/O pad receives (a) 0V-to-$V_{DD}$ and (b) $V_{DD}$-to-2x$V_{DD}$ signals.

For the receiving mode, in order to receive the 0V-2x$V_{DD}$ voltage signal without gate oxide overstress issue and turn off $M_P$ and $M_N$ to avoid unnecessary circuit leakage path, the source voltages of $M_P$ and $M_N$ should be biased at $V_{DD}$. Besides, the gate biases of $M_P$ and $M_N$ should be controlled according to the received signal voltage. For example, when receiving the voltage signal from 0V-$V_{DD}$ as shown in Fig. 5.2(a), the gate voltage of $M_P$ should be $V_{DD}$ and the gate voltage of $M_N$ should be 0V-$V_{DD}$. When receiving the voltage signal from $V_{DD}$-2x$V_{DD}$ as shown in Fig. 5.2(b), the gate voltage of $M_P$ should be $V_{DD}$-2x$V_{DD}$ and the gate voltage of $M_N$ should be $V_{DD}$. Therefore, the channel of $M_P$ and $M_N$ can not be turned on to cause leakage current in the receiving mode. With the dynamic source bias and gate-controlled techniques, the output buffer implemented by only 1x$V_{DD}$ devices can transmit or receive 0V-2x$V_{DD}$ voltage signals without suffering the aforementioned reliability

issues.

## 5.3 2xV$_{DD}$-Tolerant Output Buffer with PVT Compensation

The proposed 2xV$_{DD}$-tolerant output buffer with PVT compensation is shown in Fig. 5.3. It incorporates with a 2xV$_{DD}$-tolerant output buffer [30], a 2xV$_{DD}$-tolerant PVT variation detector, and a 2xV$_{DD}$-tolerant 8-to-3 encoder. The 2xV$_{DD}$-tolerant PVT variation detector detects the PVT variations under the 2xV$_{DD}$ voltage environment in the chip. Then, the circuit digitize the PVT variations into a compensation code in the specific environment. After, the compensation code is encoded by the 2xV$_{DD}$-tolerant 8-to-3 encoder to generate the 3-bit control signals for the output buffer. According to the 3-bit control signals to turn on or turn off the segmented output drivers, the output buffer can adjust the driving capability to mitigate the impacts caused by PVT variations.

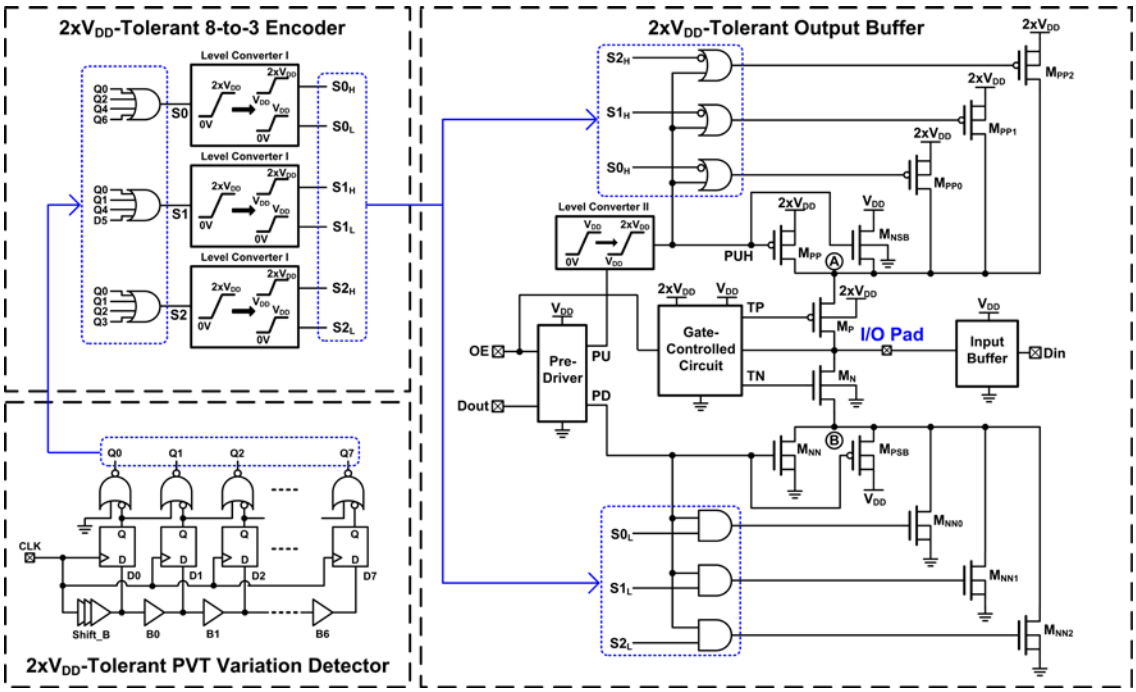



Fig. 5.3. Proposed 2xV$_{DD}$-tolerant output buffer with PVT compensation.

### 5.3.1 2xV$_{DD}$-Tolerant Output Buffer

In the 2xV$_{DD}$-tolerant output buffer, the functions include transmitting a 2xV$_{DD}$ voltage signal with 1xV$_{DD}$ voltage input signal and receiving a 2xV$_{DD}$ voltage signal. With the same design concept of dynamic source bias, the the 0V-2xV$_{DD}$ voltage signal is also separated to a 0V-V$_{DD}$ and a V$_{DD}$-2xV$_{DD}$ control signals. The 0V-V$_{DD}$ voltage signal PD from the pre-driver input of Dout is utilized to control the pull-low path of driving NMOS M$_{NN}$ and the source voltage bias PMOS M$_{PSB}$. Besides, this 0V-V$_{DD}$ voltage signal at PU is converted to

$V_{DD}$-2x$V_{DD}$ voltage signal at PUH by the level converter II (as shown in Fig. 5.4) to control the pull-high path of driving PMOS $M_{PP}$ and the source voltage bias NMOS $M_{NSB}$. Thus, the source voltages of $M_P$ and $M_N$ can be biased to the required values during the transmitting and receiving modes. For example, in the transmitting mode, the transmitting enable signal OE is $V_{DD}$ and Dout is 0V, the PD and PU signals are driven to $V_{DD}$ to turn on $M_{NN}$ and turn off $M_{PSB}$. At the same time, the PUH signal is converted to 2x$V_{DD}$ to turn off $M_{PP}$ and turn on $M_{NSB}$. Therefore, the output voltage at I/O pad is 0V and the voltage at node A is $V_{DD}$. On the other hand, with OE signal 0V in receiving mode, the PD signal is 0V, the PU signal is $V_{DD}$, and the PUH signal is 2x$V_{DD}$. Therefore, the $M_{PSB}$ and $M_{NSB}$ are turned on to bias nodes A and B to $V_{DD}$.

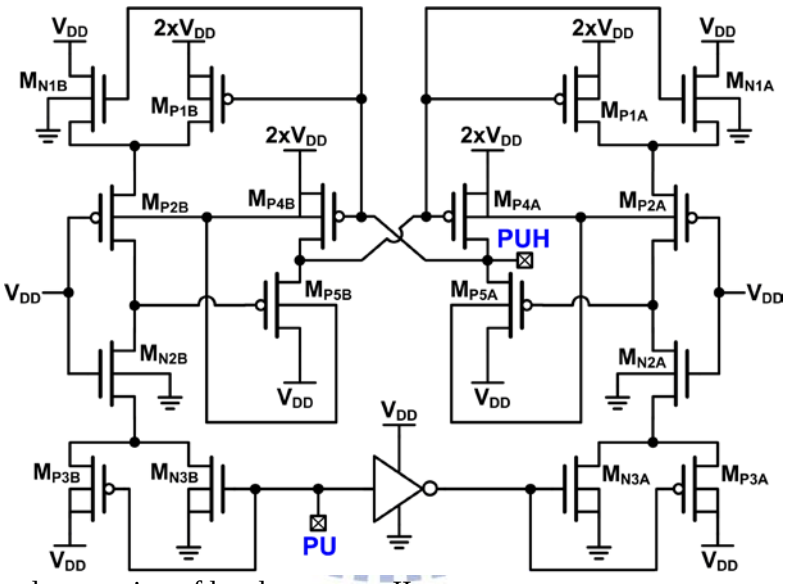


Fig. 5.4. Circuit implementation of level converter II.

To generate the required gate bias voltage of $M_P$ ($M_N$) at TP (TN), the gate-controlled circuit was proposed as illustrated in Fig. 5.5. In transmitting mode (OE signal is $V_{DD}$), the gate-controlled circuit biases the voltages at TP and TN to $V_{DD}$. In receiving mode (OE signal is 0V), TP and TN are adjusted to the required voltages. For example, when the I/O pad is 2x$V_{DD}$, the upper part transistors of $M_{G5}$, $M_{G2}$, and $M_{G3}$ are turned on to bias TP at 2x$V_{DD}$.On the other hand, the under part transistors of $M_{G9}$, $M_{G7}$, and $M_{G8}$ are turned on to bias TN voltage at $V_{DD}$. With the dynamic source bias and gate-controlled techniques, the 2x$V_{DD}$-tolerant output buffer actually can transmit and receive a 0V-2x$V_{DD}$ voltage signal without the gate oxide overstress issue. To implement PVT compensation, the output driver is modified to multi-stages and the number of turned-on stages is decided by the compensation code. In this work, the output drivers contain three stages and the ratio of $M_{PP0}$ ($M_{NN0}$), $M_{PP1}$

($M_{NN1}$), and $M_{PP2}$ ($M_{NN2}$) is 1:2:4 to meet 3-bit compensation codes.

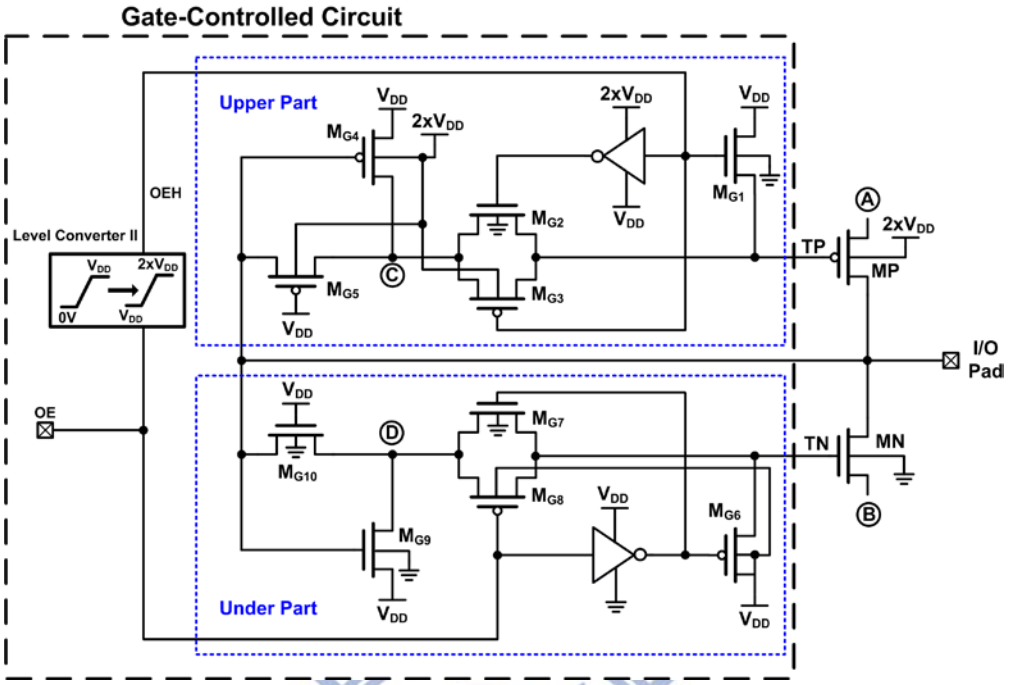



Fig. 5.5. Gate-controlled circuit for the proposed $2xV_{DD}$-tolerant output buffer.

### 5.3.2 $2xV_{DD}$-Tolerant PVT Variation Detector

In the prior PVT compensation techniques [40]-[45], the most convenient method is to detect the delay time which influenced by PVT variations. The PVT variation detector quantifies the delay time of the delay chain to generate a compensation code [43], [45]. Then, the multiple output stages are turned on according to the compensation signal to adjust the driving capability. With this kind of PVT variation detector, the output driver can control the slew rate within one clock cycle time. Besides, each circuit block of the PVT variation detector can easily be consisted with complementary logic circuits. However, applying the prior PVT variation detector to detect the variations under $2xV_{DD}$ voltage environment would suffer the gate oxide overstress issue. In this work, the PVT variation detector is modified to tolerant $2xV_{DD}$ voltage by using the proposed $2xV_{DD}$-tolerant logic gates. The proposed $2xV_{DD}$-tolerant PVT detector is also shown in Fig. 5.3. Each logic circuit consists of $2xV_{DD}$-tolerant logic gates to have $2xV_{DD}$ tolerant capability. The delay chain buffers (Shift_B and B0-B6) are composed of $2xV_{DD}$-tolerant NOT gates, and the register (positive edge-triggered D flip flop) is composed of eight $2xV_{DD}$-tolerant NAND gates. Thus, the proposed PVT detector can be operated under the $2xV_{DD}$ voltage domain and receive the $2xV_{DD}$ clock signal.

In the beginning, the reference clock (CLK) delivers the 0V-2x$V_{DD}$ clock signal into the delay chain buffers. Then, the output signal from each delay buffer is loaded to the register at the clock rising edge. Since the propagation delay of the delay buffer depends on PVT variations, more compensation for driving capability is needed with more logic high signals loaded into the registers. Finally, the data in the registers are used to generate an 8-bit pre-control signal D0 to D7 by the series 2x$V_{DD}$-tolerant NOR gates. For example, in the fastest condition, no logic high signal is loaded into the register; the pre-control signal presents the code "00000000". On the other hand, the logic high signals are loaded into all registers in the slowest condition, leading to the pre-control code of "10000000". To provide the correct compensation codes within one clock cycle time, the delay time of the buffers needs to meet the following requirements.

$$\left[T_{total\_delay\_min} = \left(T_{Shift\_B} + 7T_B\right)_{\min}\right] > \frac{1}{2}T_{Clock}, \tag{5.1}$$

$$\left[T_{total\_delay\_max} = \left(T_{Shift\_B} + 7T_B\right)_{\max}\right] < T_{Clock}, \tag{5.2}$$

$$7T_B < \frac{1}{2}T_{Clock} \tag{5.3}$$

The total delay time is formed by the shift buffer ($T_{Shift\_B}$) and seven buffers ($7T_B$). The minimum delay time $T_{total\_delay\_min}$ in the fastest condition should be longer than 1/2 clock cycle time ($T_{Clock}$), as shown in Fig. 5.6. The maximum delay time $T_{total\_delay\_max}$ in the slowest condition should be shorter than one clock cycle time, as showing in Fig. 5.7. Besides, the delay time of buffers $7T_B$ (B0~B6) should be shorter than 1/2 clock cycle time to avoid loading wrong bits to the registers.

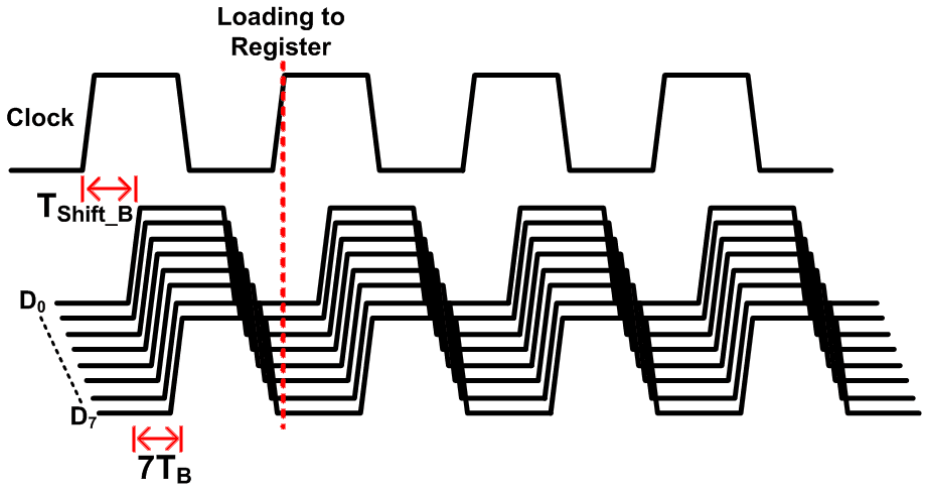



Fig. 5.6. Timing chart of the delay buffers in the fastest condition.

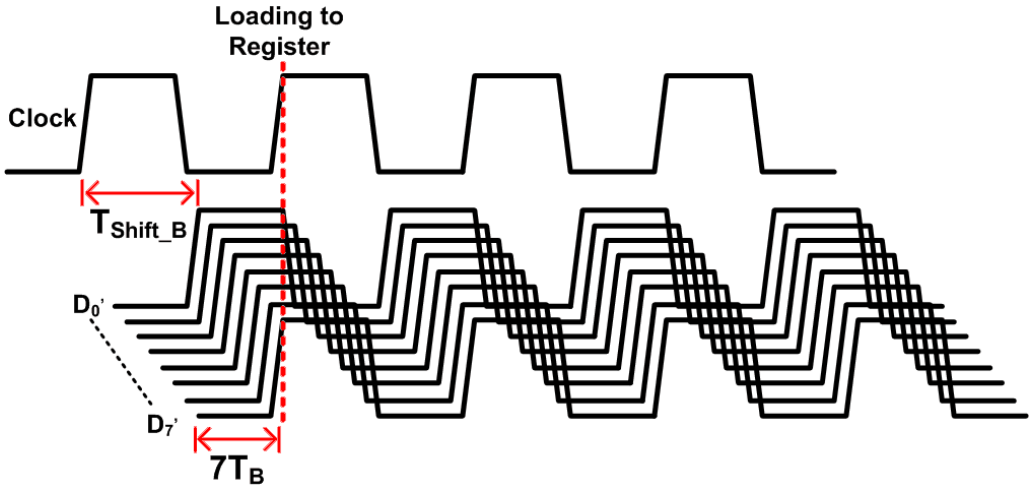


Fig. 5.7. Timing chart of the delay buffers in the slowest condition.

### 5.3.3 2x$V_{DD}$-Tolerant 8-to-3 Encoder

To control the 3-stages output drivers, the 8-bit pre-control signal needs to be encoded to a 3-bit compensation code. Table 5.1 shows the truth table of this encoder. According to the truth table, the encoder can be realized with three 4-input 2x$V_{DD}$-tolerant NOR gates as shown in Fig. 5.3. Moreover, the compensation code provided by the 8-to-3 encoder with 2x$V_{DD}$ voltage signal also need to be separated to two operating voltage regions to control the pull-high stages and pull-low stages of the output drivers. In this design, the encoded signals S0-S2 are separated to $S0_L$-$S2_L$ with 0V-$V_{DD}$ region to control the pull-low stages ($M_{NN0}$, $M_{NN1}$, and $M_{NN2}$) and $S0_H$-$S2_H$ with the $V_{DD}$-2$V_{DD}$ region to control the pull high stages ($M_{PP0}$, $M_{PP1}$, and $M_{PP2}$).

Table 5.1
Truth table of 2x$V_{DD}$-tolerant 8-to-3 encoder

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | S0 | S1 | S2 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

### 5.3.4 Circuit Simulations

The circuit behaviors are verified by HSPICE simulation with device model in a 90-nm CMOS process. The $1xV_{DD}$ voltage is 1.2 V and the 2.5 V is as $2xV_{DD}$ voltage. Fig. 5.8(a) shows the simulated voltage waveforms of the $2xV_{DD}$-tolerant output buffer with a 125-MHz 0V-1.2V voltage signal at Dout and 15-pF loading at I/O pad in transmitting mode. During transmitting mode, the gate-controlled circuit successfully provides the 1.2V gate bias voltage. With the dynamic source voltage at node A (1.2V-2.5V) and node B (0V-1.2V), the 0V-2.5V voltage signal can successfully transmit to I/O pad. Fig. 5.8(b) shows the simulated voltage waveforms with a 125-MHz 0V-2.5V voltage signal at I/O pad in receiving mode. Nodes A and B are biased at 1.2V. The gate-controlled circuit provides the 1.2V-2.5V bias voltage at TP and 0V-1.2V bias voltage at TN. The corresponding circuit logics and devices' behavior of the proposed $2xV_{DD}$-tolerant output buffer in two operation modes are summarized in Table 5.2. According to the simulated results, the maximum voltage across any two terminals of each transistor in the proposed $2xV_{DD}$-tolerant output buffer is kept within $1xV_{DD}$. Therefore, the proposed $2xV_{DD}$-tolerant output buffer with only $1xV_{DD}$ devices can be successfully operated in $2xV_{DD}$ voltage domain without suffering the gate oxide reliability issue.

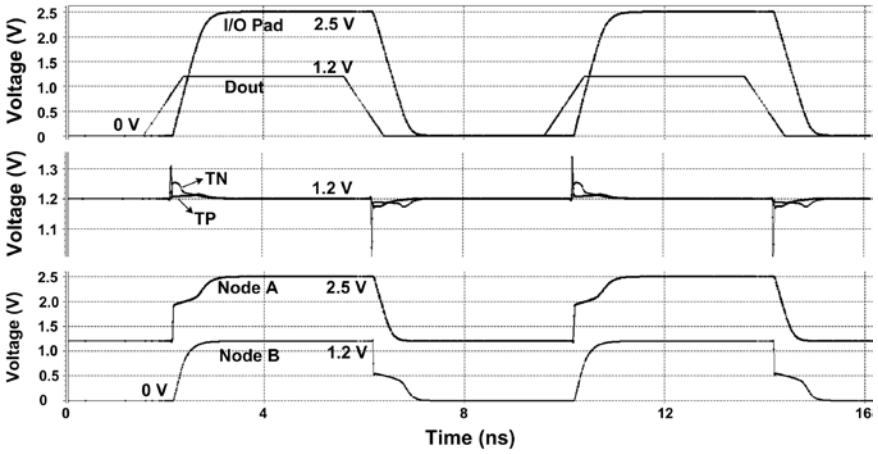
In order to observe the compensation efficiency, the slew rates of the output waveforms without and with PVT compensation are compared. The rise and fall slew rates are defined as following equations.

$$SR_{rise} = \frac{0.9 \times V_{DDH} - 0.1 \times V_{DDH}}{T_{rise}}, \tag{5.4}$$

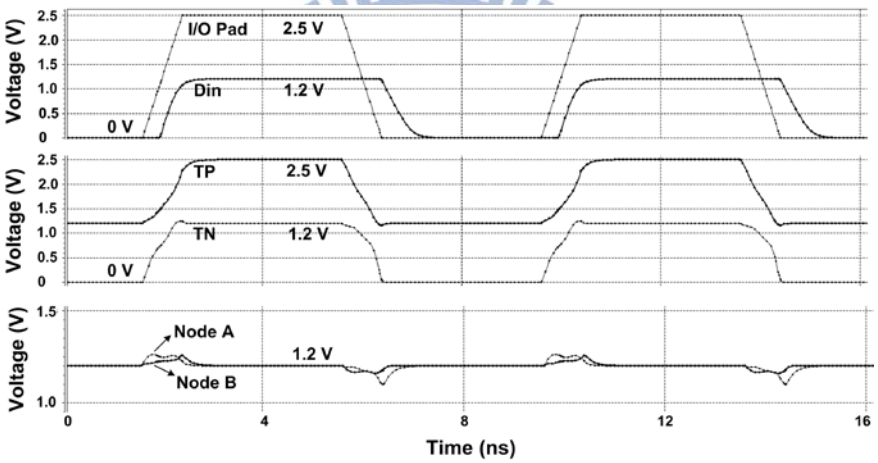
$$SR_{fall} = \frac{0.9 \times V_{DDH} - 0.1 \times V_{DDH}}{T_{fall}}. \tag{5.5}$$

The $V_{DDH}$ is 2.5V, $SR_{rise}$ is the slew rate when output transits from $0.1xV_{DDH}$ to $0.9xV_{DDH}$, and $SR_{fall}$ is the slew rate when output transits from $0.9xV_{DDH}$ to $0.1xV_{DDH}$. Tables 5.3 and 5.4 list the simulated slew rates of the proposed $2xV_{DD}$-tolerant output buffer without and with PVT compensation. The process variation includes three process corners, which are fast-fast (FF), typical-typical (TT), and slow-slow (SS). Five supply voltages within ±10% variation from the normal value are used in the simulation with the step of 5% $V_{DD}$ voltage. The temperature conditions from 0°C to 125°C are applied with the step of 25°C. As listed in Table 5.3 and Table 5.4, without PVT compensation, the maximum variation of $SR_{rise}$ ($SR_{fall}$) is 1.92V/ns (2.02V/ns). However, after applying PVT compensation, the maximum variation

of $SR_{rise}$ ($SR_{fall}$) is decreased to 1.2V/ns (1.15V/ns). The corresponding compensation codes (S0, S1, s2) which generated in the proposed $2xV_{DD}$-tolerant PVT variation detector are listed in Table 5.5.




(a)




(b)

Fig. 5.8. Simulated voltage waveforms of the proposed $2xV_{DD}$-tolerant output buffer in (a) transmitting mode and (b) receiving mode.

Table 5.2
Corresponding circuit logics and node voltages of the proposed $2xV_{DD}$-tolerant output buffer

| Operation Mode | Dout | PUH | PD | Node A | Node B | TP | TN | I/O Pad |
|---|---|---|---|---|---|---|---|---|
| Transmitting | 0V | $2xV_{DD}$ | $V_{DD}$ | $V_{DD}$ | 0V | $V_{DD}$ | $V_{DD}$ | 0V |
| | $V_{DD}$ | $V_{DD}$ | 0V | $2xV_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $2xV_{DD}$ |
| Receiving | | $2xV_{DD}$ | 0V | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | 0V | 0V |
| | | $2xV_{DD}$ | 0V | $V_{DD}$ | $V_{DD}$ | $2xV_{DD}$ | $V_{DD}$ | $2xV_{DD}$ |

Table 5.3
Simulated output slew rate of the proposed 2x$V_{DD}$-tolerant output buffer without PVT compensation

| FF | Supply Voltage ($V_{DD}$/$V_{DDH}$) | | | | |
|---|---|---|---|---|---|
| | (1.08/2.25) | (1.14/2.375) | (1.2/2.5) | (1.26/2.625) | (1.32/2.75) |
| 25 °C | 2.25 / 2.31 | 2.53 / 2.60 | 2.82 / 2.88 | 3.11 / 3.16 | 3.41 / 3.40 |
| 50 °C | 2.18 / 2.22 | 2.45 / 2.49 | 2.73 / 2.76 | 3.00 / 3.03 | 3.29 / 3.30 |
| 75 °C | 2.12 / 2.13 | 2.37 / 2.38 | 2.64 / 2.64 | 2.91 / 2.90 | 3.19 / 3.16 |
| 100 °C | 2.06 / 2.04 | 2.31 / 2.28 | 2.56 / 2.28 | 2.82 / 2.77 | 3.09 / 3.02 |
| 125 °C | 2.00 / 1.95 | 2.24 / 2.18 | 2.49 / 2.41 | 2.74 / 2.65 | 3.00 / 2.90 |
| TT | Supply Voltage ($V_{DD}$/$V_{DDH}$) | | | | |
| | (1.08/2.25) | (1.14/2.375) | (1.2/2.5) | (1.26/2.625) | (1.32/2.75) |
| 25 °C | 1.95 / 1.89 | 2.21 / 2.15 | 2.48 / 2.41 | 2.75 / 2.68 | 3.02 / 2.95 |
| 50 °C | 1.89 / 1.82 | 2.14 / 2.06 | 2.40 / 2.31 | 2.66 / 2.57 | 2.93 / 2.83 |
| 75 °C | 1.84 / 1.74 | 2.08 / 1.98 | 2.33 / 2.22 | 2.58 / 2.46 | 2.84 / 2.71 |
| 100 °C | 1.79 / 1.67 | 2.03 / 1.90 | 2.26 / 2.13 | 2.50 / 2.36 | 2.76 / 2.60 |
| 125 °C | 1.75 / 1.61 | 1.97 / 1.82 | 2.20 / 2.04 | 2.44 / 2.26 | 2.68 / 2.48 |
| SS | Supply Voltage ($V_{DD}$/$V_{DDH}$) | | | | |
| | (1.08/2.25) | (1.14/2.375) | (1.2/2.5) | (1.26/2.625) | (1.32/2.75) |
| 25 °C | 1.65 / 1.56 | 1.89 / 1.73 | 2.14 / 1.97 | 2.39 / 2.23 | 2.65 / 2.48 |
| 50 °C | 1.61 / 1.51 | 1.84 / 1.66 | 2.08 / 1.90 | 2.32 / 2.14 | 2.57 / 2.38 |
| 75 °C | 1.57 / 1.47 | 1.79 / 1.60 | 2.02 / 1.82 | 2.25 / 2.05 | 2.49 / 2.29 |
| 100 °C | 1.53 / 1.43 | 1.74 / 1.54 | 1.96 / 1.75 | 2.19 / 1.97 | 2.42 / 2.19 |
| 125 °C | 1.49 / 1.38 | 1.70 / 1.48 | 1.91 / 1.68 | 2.13 / 1.89 | 2.36 / 2.10 |

Table 5.4
Simulated output slew rate of the proposed 2x$V_{DD}$-tolerant output buffer with PVT compensation

| FF | Supply Voltage ($V_{DD}$/$V_{DDH}$) | | | | |
|---|---|---|---|---|---|
| | (1.08/2.25) | (1.14/2.375) | (1.2/2.5) | (1.26/2.625) | (1.32/2.75) |
| 25 °C | 2.20 / 2.10 | 2.43 / 2.36 | 2.70 / 2.61 | 2.98 / 2.86 | 3.26 / 3.12 |
| 50 °C | 2.40 / 2.43 | 2.36 / 2.26 | 2.62 / 2.51 | 2.90 / 2.75 | 3.17 / 3.00 |
| 75 °C | 2.61 / 2.69 | 2.63 / 2.61 | 2.56 / 2.41 | 2.75 / 2.64 | 3.08 / 2.88 |
| 100 °C | 2.78 / 2.88 | 2.86 / 2.89 | 2.85 / 2.78 | 2.75 / 2.53 | 3.00 / 2.76 |
| 125 °C | 2.93 / 3.00 | 3.04 / 3.08 | 3.08 / 3.06 | 3.05 / 2.92 | 2.93 / 2.64 |
| TT | Supply Voltage ($V_{DD}$/$V_{DDH}$) | | | | |
| | (1.08/2.25) | (1.14/2.375) | (1.2/2.5) | (1.26/2.625) | (1.32/2.75) |
| 25 °C | 2.63 / 2.67 | 2.44 / 2.37 | 2.39 / 2.21 | 2.65 / 2.45 | 2.91 / 2.70 |
| 50 °C | 2.76 / 2.79 | 2.65 / 2.62 | 2.66 / 2.55 | 2.58 / 2.36 | 2.83 / 2.59 |
| 75 °C | 2.69 / 2.68 | 2.82 / 2.80 | 2.88 / 2.81 | 2.87 / 2.72 | 2.76 / 2.50 |
| 100 °C | 2.80 / 2.75 | 2.96 / 2.92 | 3.07 / 3.01 | 3.10 / 3.00 | 3.07 / 2.87 |
| 125 °C | 2.90 / 2.79 | 3.08 / 2.99 | 3.22 / 3.13 | 3.30 / 3.20 | 3.32 / 3.16 |
| SS | Supply Voltage ($V_{DD}$/$V_{DDH}$) | | | | |
| | (1.08/2.25) | (1.14/2.375) | (1.2/2.5) | (1.26/2.625) | (1.32/2.75) |
| 25 °C | 2.56 / 2.45 | 2.75 / 2.66 | 2.83 / 2.52 | 2.65 / 2.48 | 2.57 / 2.30 |
| 50 °C | 2.65 / 2.50 | 2.69 / 2.56 | 2.81 / 2.69 | 2.87 / 2.73 | 2.86 / 2.65 |
| 75 °C | 2.59 / 1.40 | 2.80 / 2.63 | 2.95 / 2.81 | 3.06 / 2.91 | 3.09 / 2.92 |
| 100 °C | 2.67 / 2.42 | 2.88 / 2.68 | 3.07 / 2.89 | 3.21 / 3.04 | 3.29 / 3.12 |
| 125 °C | 2.61 / 2.33 | 2.82 / 2.57 | 2.99 / 2.77 | 3.33 / 3.12 | 3.40 / 3.25 |

Table 5.5
Simulated compensation codes from the proposed 2x$V_{DD}$-tolerant PVT variation detector

| FF | Supply Voltage ($V_{DD}$/$V_{DDH}$) | | | | |
|---|---|---|---|---|---|
| | (1.08/2.25) | (1.14/2.375) | (1.2/2.5) | (1.26/2.625) | (1.32/2.75) |
| 25 °C | (0, 0, 0) | (0, 0, 0) | (0, 0, 0) | (0, 0, 0) | (0, 0, 0) |
| 50 °C | (0, 0, 1) | (0, 0, 0) | (0, 0, 0) | (0, 0, 0) | (0, 0, 0) |
| 75 °C | (0, 1, 0) | (0, 0, 1) | (0, 0, 0) | (0, 0, 0) | (0, 0, 0) |
| 100 °C | (0, 1, 1) | (0, 1, 0) | (0, 0, 1) | (0, 0, 0) | (0, 0, 0) |
| 125 °C | (1, 0, 0) | (0, 1, 1) | (0, 1, 0) | (0, 0, 1) | (0, 0, 0) |
| TT | Supply Voltage ($V_{DD}$/$V_{DDH}$) | | | | |
| | (1.08/2.25) | (1.14/2.375) | (1.2/2.5) | (1.26/2.625) | (1.32/2.75) |
| 25 °C | (0, 1, 0) | (0, 0, 1) | (0, 0, 1) | (0, 0, 0) | (0, 0, 0) |
| 50 °C | (0, 1, 1) | (0, 1, 0) | (0, 0, 1) | (0, 0, 0) | (0, 0, 0) |
| 75 °C | (1, 0, 0) | (0, 1, 1) | (0, 1, 0) | (0, 0, 1) | (0, 0, 0) |
| 100 °C | (1, 0, 1) | (1, 0, 0) | (0, 1, 1) | (0, 1, 0) | (0, 0, 1) |
| 125 °C | (1, 1, 0) | (1, 0, 1) | (1, 0, 0) | (0, 1, 1) | (0, 1, 0) |
| SS | Supply Voltage ($V_{DD}$/$V_{DDH}$) | | | | |
| | (1.08/2.25) | (1.14/2.375) | (1.2/2.5) | (1.26/2.625) | (1.32/2.75) |
| 25 °C | (1, 0, 1) | (1, 0, 0) | (0, 1, 1) | (0, 1, 0) | (0, 0, 1) |
| 50 °C | (1, 1, 0) | (1, 0, 1) | (1, 0, 0) | (0, 1, 1) | (0, 1, 0) |
| 75 °C | (1, 1, 1) | (1, 1, 0) | (1, 0, 1) | (1, 0, 0) | (0, 1, 1) |
| 100 °C | (1, 1, 1) | (1, 1, 1) | (1, 1, 0) | (1, 0, 1) | (1, 0, 0) |
| 125 °C | (1, 1, 1) | (1, 1, 1) | (1, 1, 1) | (1, 1, 0) | (1, 0, 1) |

## 5.4 Experimental Results

The proposed mixed-voltage output buffer with PVT compensation has been fabricated in a 90-nm CMOS process with only 1.2-V devices. Fig. 5.9 shows the die photo of the whole 2x$V_{DD}$-tolerant output buffers with and without PVT compensation. In order to observe the 2x$V_{DD}$-tolerant PVT variation detector's behavior, the circuit also has been fabricated stand-alone in test chip as shown in Fig. 5.10.

### 5.4.1 Measured Results of 2x$V_{DD}$-Tolerant PVT Variation Detector

Fig. 5.11 shows the measurement setup to verify the compensation function of 2x$V_{DD}$-tolerant PVT variation detector. The pulse generator Agilent 8133A was used to provide the clock signal. When changing the supply voltage and temperature during measurement, the compensation codes from S0 to S2 will be displayed on the LED. Since the foundry only provides the test chips fabricated in the typical TT process corner, the measured results are merely available in this process corner. The measured compensation codes are summarized in Table 5.6. After changing the supply voltage and temperature, the compensation code is observed, and the compensated quantity is increased as the operating

condition become worse.

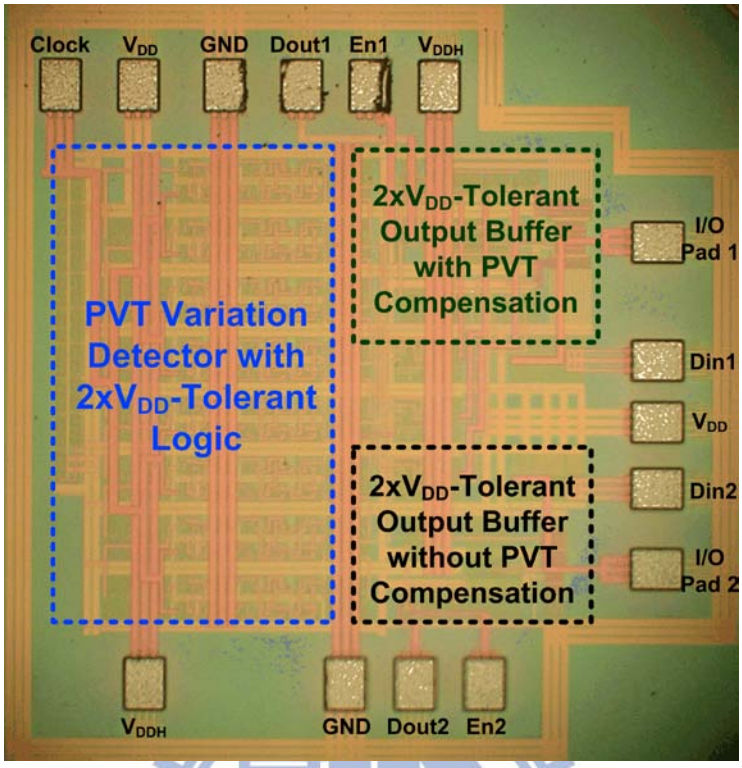



Fig. 5.9. Die photo of the $2xV_{DD}$-tolerant output buffers with and without PVT compensation.

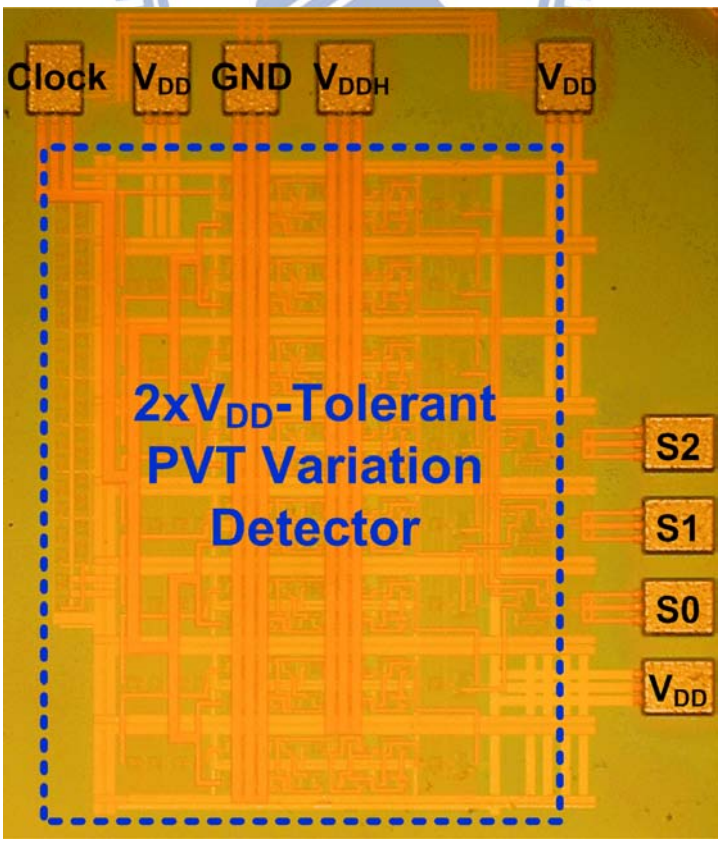



Fig. 5.10. Die photo of the stand-alone $2xV_{DD}$-tolerant PVT variation detector.

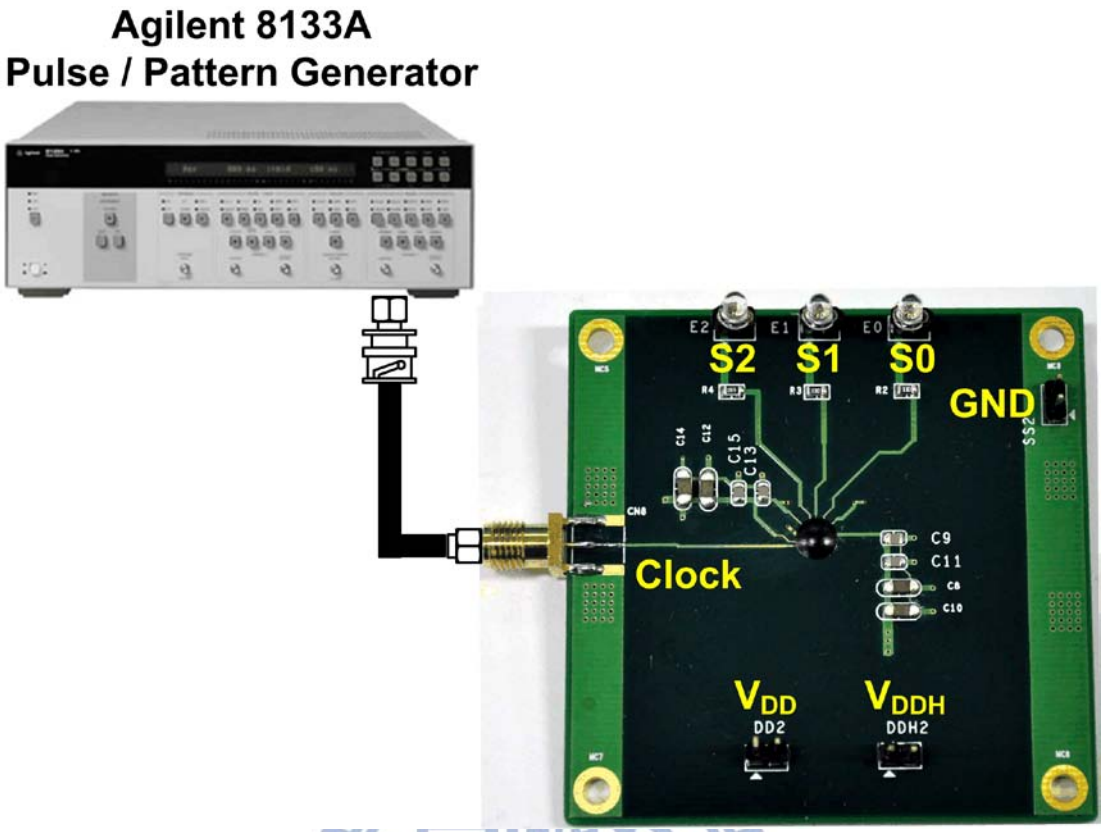



Fig. 5.11. Measurement setup for the 2x$V_{DD}$-tolerant PVT variation detector.

Table 5.6
Measured compensation codes from the proposed 2x$V_{DD}$-tolerant PVT variation detector

| TT | Supply Voltage ($V_{DD}$/$V_{DDH}$ ) | | | | |
|---|---|---|---|---|---|
| | (1.08/2.25) | (1.14/2.375) | (1.2/2.5) | (1.26/2.625) | (1.32/2.75) |
| 25 °C | (1, 0, 1) | (1, 0, 0) | (0, 1, 1) | (0, 1, 0) | (0, 0, 1) |
| 50 °C | (1, 1, 0) | (1, 0, 1) | (1, 0, 0) | (0, 1, 1) | (0, 1, 0) |
| 75 °C | (1, 1, 1) | (1, 1, 0) | (1, 0, 1) | (1, 0, 0) | (0, 1, 0) |
| 100 °C | (1, 1, 1) | (1, 1, 1) | (1, 1, 0) | (1, 0, 1) | (1, 0, 0) |
| 125 °C | (1, 1, 1) | (1, 1, 1) | (1, 1, 1) | (1, 1, 0) | (1, 0, 1) |

### 5.4.2 Measured Results of 2x$V_{DD}$-Tolerant Output Buffer with PVT Compensation

The measurement setup of the 2x$V_{DD}$-tolerant output buffers with and without PVT compensation is shown in Fig. 5.12. The pulse generator Agilent 8133A was also used to

provide a $1xV_{DD}$ input signal for Dout, and the $2xV_{DD}$ output signal will be generated at I/O pad. Then, the supply voltage and temperature will be altered during measurement to observe the variation of the output waveforms with and without the PVT compensation.

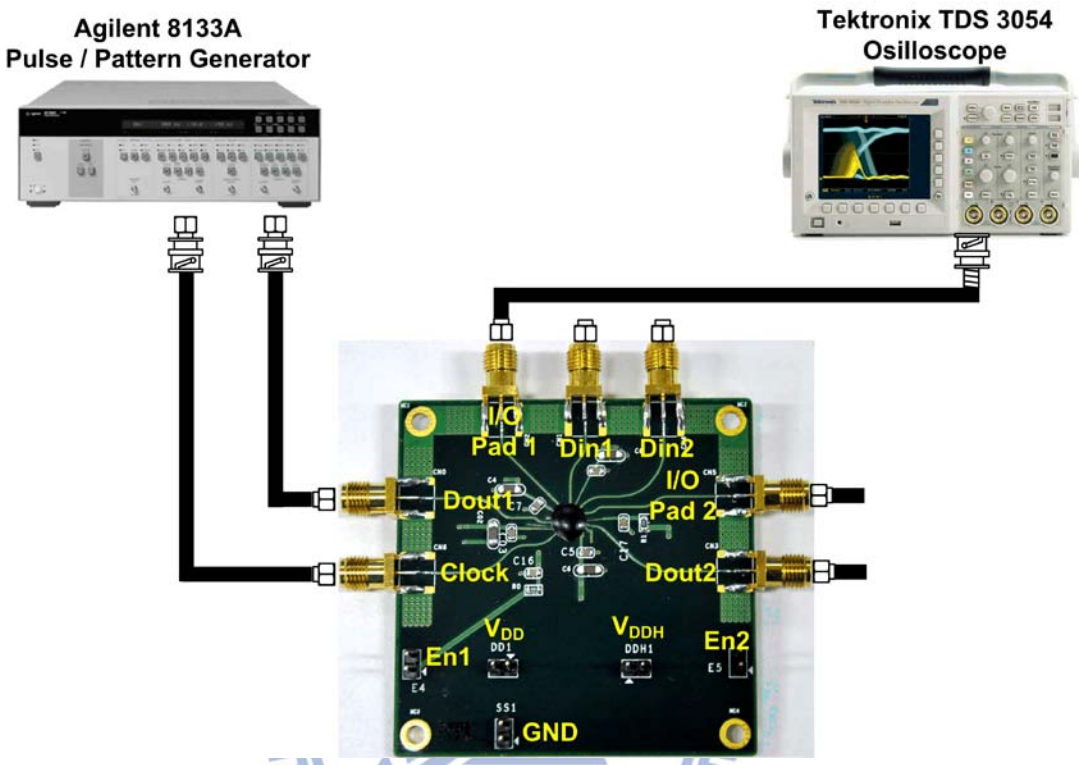
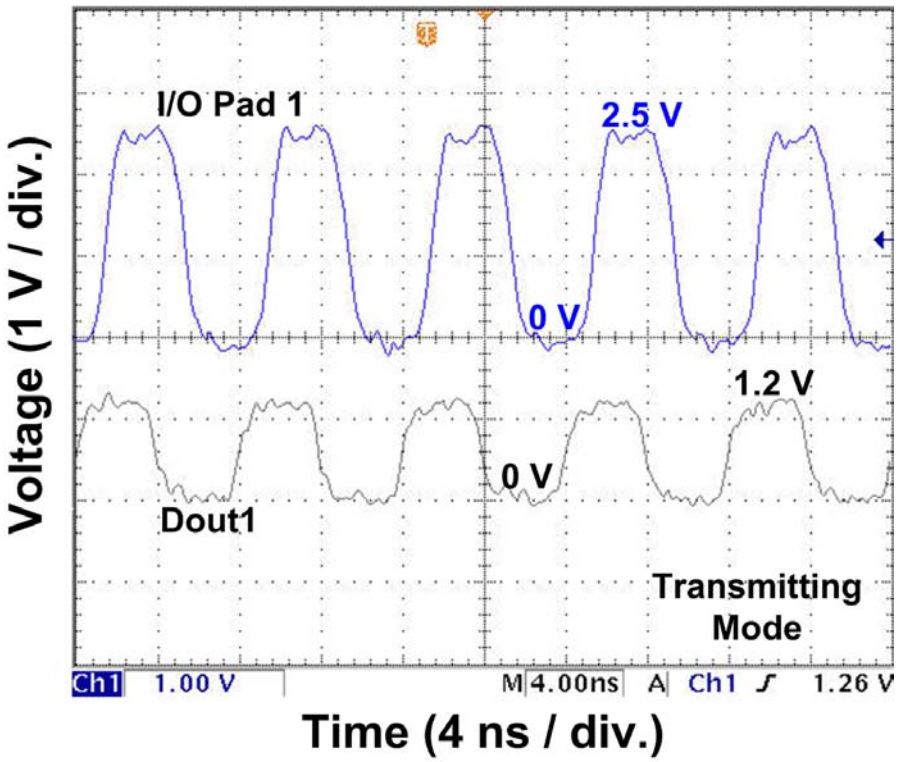
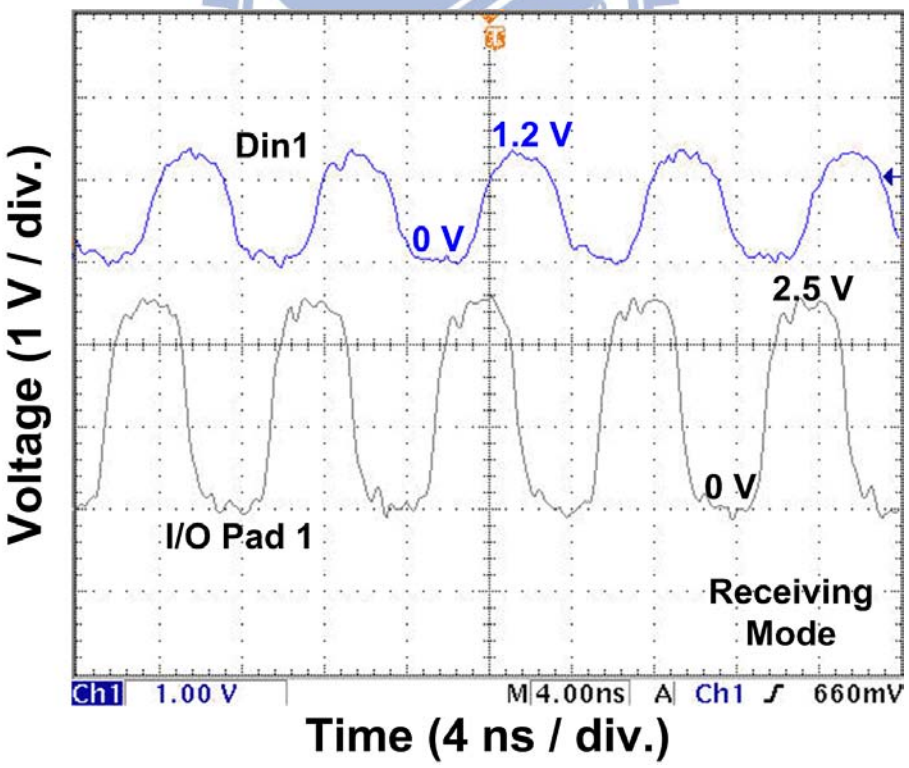



Fig. 5.12. Measurement setup for the $2xV_{DD}$-tolerant output buffers with and without PVT compensation.

To verify the main functions of a $2xV_{DD}$-tolerant output buffer, Figs. 5.13(a) and 5.13(b) show the measured output voltage waveforms in transmitting mode and receiving mode, respectively. In the $2xV_{DD}$-tolerant output buffer with PVT compensation, the output driving capability and the function of PVT variation detection were designed with a 125-MHz input signal. Thus, the waveform data rate verified in those figures is 125-MHz. As showing in Fig. 5.13(a), when a 0V-1.2V voltage signal is provided to Dout1, the proposed $2xV_{DD}$-tolerant output buffer can successfully transmit a 0V-2.5V voltage signal at I/O pad 1 in transmitting mode. In the receiving mode, the proposed $2xV_{DD}$-tolerant output buffer can successfully receive the 0V-2.5V voltage signal at I/O pad 1, as showing in Fig. 5.13(b), where the input data was successfully converted to a 0V-1.2V voltage signal at Din1. Measured results have demonstrated that the proposed $2xV_{DD}$-tolerant output buffer can provide the correct functions.




(a)




(b)

Fig. 5.13. Measured results of the proposed $2xV_{DD}$-tolerant output buffer in (a) transmitting mode and (b) receiving mode.

To observe the efficiency of PVT compensation with varied supply voltages, Figs. 5.14(a), 5.14(b), and 5.14(c) show the measured output waveforms with different supply voltages at temperature of 25°C. With the $V_{DD}/V_{DDH}$ voltage of 1.32V/2.75V, the PVT detector provides the compensation code of "001" to the buffer (as listed in Table 5.6). However, under this higher operating voltage condition, the output waveforms with and without PVT compensation do not have obvious difference, as shown in Fig. 5.14(a). When $V_{DD}/V_{DDH}$ voltage is changed to 1.2V/2.5V, the PVT detector provides the compensation code of "011" to the buffer (as listed in Table 5.6). Comparing the output waveforms with PVT compensation, the output waveform without PVT compensation is significantly degraded, as shown in Fig. 5.14(b). When $V_{DD}/V_{DDH}$ voltage is further decreased to the worst case of 1.08V/2.25V, the output waveform without PVT compensation is degraded more seriously, as shown in Fig. 5.14(c).

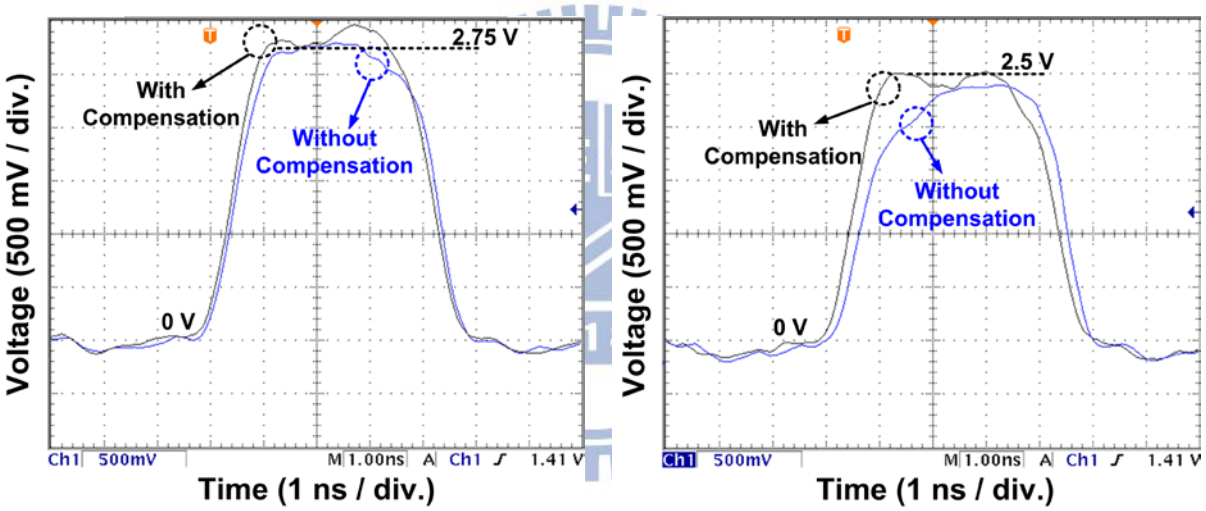



Fig. 5.14. Measured output waveform of the proposed $2xV_{DD}$-tolerant output buffer with $V_{DD}/V_{DDH}$ voltage of (a) 1.32-V/2.75-V, (b) 1.2-V/2.5-V, and (c) 1.08-V/2.25-V.

To observe the efficiency of PVT compensation under different temperatures, Figs. 5.15(a) and 5.15(b) show the measured output waveform with $V_{DD}/V_{DDH}$ of 1.2V/2.5V at 25°C and 125°C, respectively. Without PVT compensation, the output waveform has seriously degradation at high temperature. On the other hand, with PVT compensation to adjust the driving capability against PVT variation, the output waveform is more preferable.

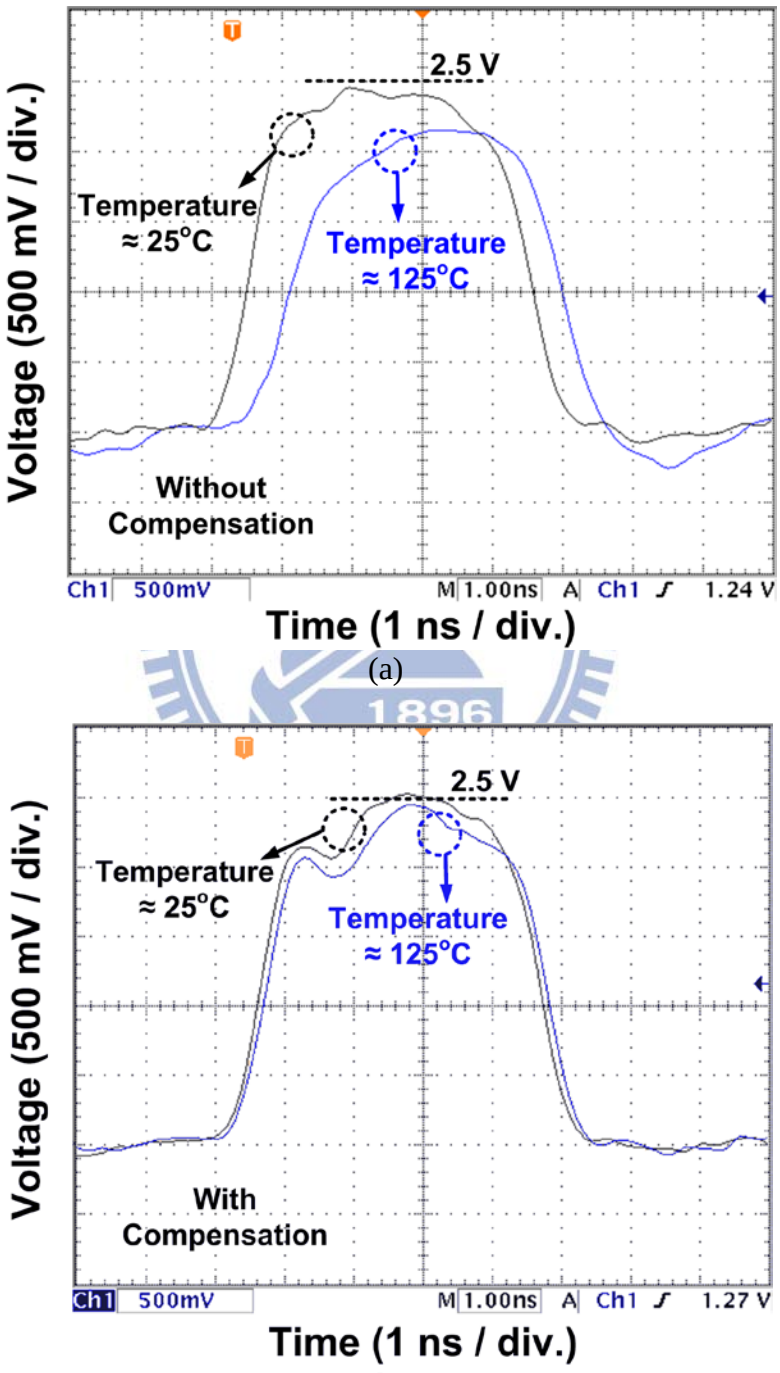



Fig. 5.15. Measured output waveforms of the proposed 2x$V_{DD}$-tolerant output buffer (a) without PVT compensation and (b) with PVT compensation, under different temperatures.

## 5.5 Discussion

Between the proposed design and the prior studies of mixed-voltage I/O buffers, some features are compared in the Table 5.7. The proposed design can successfully mitigate serious PVT variation issue, but the PVT detection circuit would occupy more silicon area as compared to the prior works of mixed-voltage I/O buffers.

In this work, the delay time provided by the delay chains can easily be quantified to generate the compensation code, but some limitations exist in this structure. To provide the correct compensation code to the output buffer, the delay time of delay cell is dependent on the clock cycle time, so there is an upper limit on the operating frequency. With this limitation, this structure cannot compensate the circuits that have different operating frequencies. Besides, the percentage of delay time formed by the PMOS and NMOS cannot be discriminated. So, the PVT detector provides the same control signal to PMOS and NMOS drivers. Namely, this structure would not correctly adjust the driving capability in the slow-fast (SF) or fast-slow (FS) conditions, in which NMOS and PMOS has variation in the opposite direction.

Table 5.7
Comparison on the features among the mixed-voltage I/O buffers

| Mixed-Voltage I/O Designs | N-Well Bias | Gate-Oxide Reliability Issue | Extra Device Used | Transmit | Receive | PVT Compensation | Area | Power Consumption |
|---|---|---|---|---|---|---|---|---|
| Ref. [25] | Yes (Dynamic Bias) | Yes | No | $1xV_{DD}$ | $2xV_{DD}$ | No | Small | Low |
| Ref. [26] | No (Fixed Bias) (Extra Pad) | No | Yes (Depletion PMOS) | $1xV_{DD}$ | $2xV_{DD}$ | No | Small | Low |
| Ref. [27] | Yes (Dynamic Bias) | No | No | $1xV_{DD}$ | $2xV_{DD}$ | No | Small | Low |
| Ref. [28] | Yes (Dynamic Bias) | No | No | $1xV_{DD}$ | $2xV_{DD}$ | No | Small | Low |
| Ref. [29] | No (Fixed Bias) | No | No | $1xV_{DD}$ | $2xV_{DD}$ | No | Small | Low |
| Ref. [30] | No (Fixed Bias) | No | No | $2xV_{DD}$ | $2xV_{DD}$ | No | Medium | Medium |
| Ref. [31] | Yes (Dynamic Bias) | No | No | $1/2xV_{DD}$~ $3xV_{DD}$ | $1/2xV_{DD}$~ $3xV_{DD}$ | No | Medium | Medium |
| Ref. [32] | Yes (Dynamic Bias) | No | No | $1/2xV_{DD}$~ $3xV_{DD}$ | $1/2xV_{DD}$~ $3xV_{DD}$ | No | Medium | Medium |
| This Work | No (Fixed Bias) | No | No | $2xV_{DD}$ | $2xV_{DD}$ | Yes | Large | High |

## 5.6 Summary

A new $2xV_{DD}$-tolerant output buffer with PVT compensation had been proposed and verified in a 90-nm CMOS process with only 1.2-V devices. With dynamic source bias and gate-control techniques, the $2xV_{DD}$-tolerant output buffer can be implemented by using only $1xV_{DD}$ devices. Moreover, $2xV_{DD}$-tolerant PVT detector can be realized by the $2xV_{DD}$-tolerant logic gates to detect the PVT variation in the $2xV_{DD}$ voltage domain and to provide the compensation function for the $2xV_{DD}$-tolerant output buffer. With the compensation functions to turn on or turn off the segmented output drivers, the output buffer can adjust the driving capability and keep a stable output slew rate to mitigate the impacts caused by PVT variations.

# Chapter 6

# Conclusion and Future Works

## 6.1 Conclusion

In this dissertation, the reliability issues of ESD clamp circuits and mixed-voltage output buffer within the SoC applications have been studied. For solving the reliability issues in each circuit application, new proposed designs have been proposed and successfully verified in the silicon chips.

In Chapter 2, two modification concepts for low-leakage ESD clamp circuit had been realized and verified in 65-nm CMOS processes. The MOM capacitor can easily be realized through the metal interconnects without the additional fabrication masks. Moreover, the capacitance density of the MOM capacitor can exceed the MIM capacitor, when more metal layers are used in advanced CMOS processes. With the advantages of higher capacitance density and lower fabrication cost, the MOM capacitor is more suitable for general circuit applications in nanoscale CMOS processes. By using the MOM capacitor instead of the thin-oxide MOS capacitor in the ESD clamp circuit, the leakage current was decreased from 828 μA to 358 nA at 25 °C. Under a STSCR drawing with 40 μm width, the low-leakage ESD clamp circuit with MOM capacitor achieved ESD robustness of 4 kV in HBM test and 350 V in MM test. In addition to the device replacement, two low-leakage ESD clamp circuits with diode string bias and feedback-control bias circuit were proposed. With the diode string bias circuit to decrease the voltage across the MOS capacitor, the overall leakage current was 228 nA at 25 °C. Under a STSCR drawing width of 120 μm, the low-leakage ESD clamp circuit with diode string bias achieved ESD robustness of 8 kV in HBM test and 750 V in MM test. With the feedback-control bias circuit to further cancelled the voltage across the MOS capacitor, the overall leakage current was only 116 nA at 25 °C. Under the same drawing width of STSCR, the low-leakage ESD clamp circuit with feedback-control bias circuit achieved ESD robustness of over 8 kV in HBM test and 800 V in MM test.

In Chapter 3, the lower holding voltage of the ESD protection circuit in the high-voltage process had been investigated by the TLP measurement. In this case, it caused the touch panel control IC suffering the latchup-like failure under normal circuit operating conditions. For the IC application with high-voltage power supply of 12 V, the new high-voltage ESD clamp circuit had been proposed and verified with a 1.8-V/3.3-V/12-V DDDMOS process. By

stacked high-voltage and low-voltage ESD protection NMOS devices, the holding voltage was increased from 8.8 V to 13.8 V without extra process modification. Therefore, the touch panel control IC in demo equipment can pass the system-level ESD test with the air-discharge mode of ±15-kV without the latchup-like failure. In addition to the purpose of free to latchup-like issue, the proposed design also maintained good enough chip-level ESD robustness of 4 kV in HBM test and 400 V in MM test.

In Chapter 4, novel $2xV_{DD}$-tolerant logic gates had been proposed and verified in a 90-nm CMOS process with only 1.2-V ($1xV_{DD}$) devices. By using the dynamic source bias technique, the CMOS logic gates were realized to have $2xV_{DD}$ tolerant capability without suffering gate oxide reliability issue. Measured results had demonstrated that the proposed $2xV_{DD}$ tolerant logic gates can be safely operated with the voltage signals of 2.5 V to provide the correct logic functions. The proposed $2xV_{DD}$-tolerant logic gates can be used in the applications of microelectronic systems facing the mixed-voltage environments. The circuit solution proposed in this work can be generally applied to all CMOS processes to realize $2xV_{DD}$-tolerant logic gates with only $1xV_{DD}$ devices.

In Chapter 5, a new $2xV_{DD}$-tolerant output buffer with PVT compensation had been proposed and verified in a 90-nm CMOS process with only $1xV_{DD}$ devices. With dynamic source bias and gate-control techniques, the $2xV_{DD}$-tolerant output buffer can be implemented by using only $1xV_{DD}$ devices without suffering gate oxide overstress issue. Moreover, $2xV_{DD}$-tolerant PVT variation detector and $2xV_{DD}$-tolerant 8-to-3 encoder can be realized by the $2xV_{DD}$-tolerant logics gates to detect the PVT variations in the $2xV_{DD}$ voltage domain and provide the compensation function for the $2xV_{DD}$-tolerant output buffer. With the compensation functions to turn on or turn off the segmented output drivers, the proposed output buffer can adjust the driving capability and keep a stable output slew rate to provide preferable output waveforms.

## 6.2 Future Works

In the measurements of chapter 2, each low-leakage ESD clamp circuit can achieve high TLP $I_{t2}$ and ESD robustness by the triggered-on STSCR. When looking at the TLP I-V curves, it could be found that the turned-on resistance was too high to cause large clamping voltage (as shown in Figs. 2.16 and 2.28). But, large clamping voltage will be harmful to the internal circuits which need to be protected. Without the whole-chip verification, the stand-alone circuit measurement could not present the real ESD protection capability. Thus, some future

works need to proceed. In order to observe the objective ESD protection ability, the low-leakage ESD clamp circuits should be implemented within input/output interfaces (including the monitor devices as internal circuits) to do whole-chip verifications. Moreover, for enhancing the ESD protection capability, the modifications of STSCR with lower turned-on resistance should be further studied.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Reliability Design of ESD Clamp Circuit and Output Buffer for SoC Applications


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# Publication List

## (A) Referred Journal Papers:

1. M.-D. Ker and **Po-Yen Chiu**, "New low-leakage power-rail ESD clamp circuit in a 65-nm low-voltage CMOS process," *IEEE Trans. on Device and Materials Reliability*, vol. 11, no. 3, pp. 474-483, Sep. 2011.
2. M.-D. Ker and **Po-Yen Chiu**, "Design of $2\times V_{DD}$-tolerant I/O buffer with PVT compensation realized by only $1\times V_{DD}$ thin-oxide devices," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 60, no. 10, pp. 2549-2560, Oct. 2013.
3. **Po-Yen Chiu** and M.-D. Ker, "Metal-layer Capacitors in the 65-nm CMOS process and the application for low-leakage power-rail ESD clamp circuit," *Microelectronics Reliability, in press*, 2013.
4. M.-D. Ker, **Po-Yen Chiu**, W.-T. Shieh, C.-C. Wang, C.-T. Tsai, S.-C. Wen, and I.-J. Wei, "ESD protection design against latchup-like failure for touch panel control IC in a 12-V double-diffused drain MOS process," submitted to *Trans. on Device and Materials Reliability*.

## (B) International Conference Papers:

1. Y.-W. Hsiao, M.-D. Ker, **Po-Yen Chiu**, C. Huang, and Y.-K. Tseng, "ESD protection design for giga-Hz high-speed I/O interfaces in a 130-nm CMOS process," in *Proc. IEEE International SOC Conference*, 2007, pp. 277-280.
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7. **Po-Yen Chiu** and M.-D. Ker, "Design of $2\times V_{DD}$ logic gates with only $1\times V_{DD}$ devices in nanoscale CMOS technology," in *Proc. IEEE International SOC Conference*, 2013.

## (C) Local Conference Papers:

1. **Po-Yen Chiu** and M.-D. Ker, "Impact of gate leakage current on power-rail ESD clamp circuit in nanoscale CMOS technology," in *Proc. Electronic Technology Symposium*, 2009.
2. Y.-R. Wen, **Po-Yen Chiu**, and M.-D. Ker, "提昇多指狀靜電放電保護元件導通均勻度之佈局設計," in *Proc. Taiwan ESD and Reliability Conference*, 2009, pp. 65-70.
3. **Po-Yen Chiu** and M.-D. Ker, "Low-leakage power-rail ESD clamp circuit," in *Proc. Electronic Technology Symposium*, 2011.
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## (D) Patents:

1. M.-D. Ker, **Po-Yen Chiu**, and C. Huang, "ESD detection circuit and related method thereof," US Patent 7,884,617, Feb. 8, 2011.
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